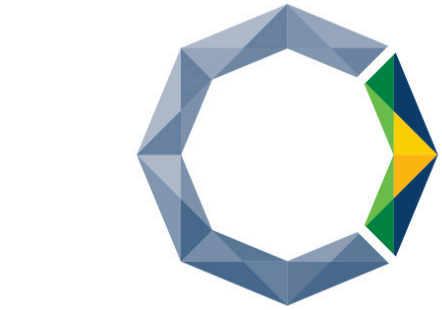

CalPolyPomona

College of Engineering

California Polytechnic State University Pomona

Department of Electrical & Computer Engineering

Digital Circuit Design Lab Verilog

ECE 3300L

Lab Report #1

Experiment #1

Presented By: Kobe Aquino & Daniel Mondragon

Presented to Mohamed Aly

June 18th, 2025

Synthesis Screenshots:

Here is a screen capture of our synthesis screenshot. The full document has been included in our github.

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	0	0	0	63400	0.00
LUT as Logic	0	0	0	63400	0.00
LUT as Memory	0	0	0	19000	0.00
Slice Registers	0	0	0	126800	0.00
Register as Flip Flop	0	0	0	126800	0.00
Register as Latch	0	0	0	126800	0.00
F7 Muxes	0	0	0	31700	0.00
F8 Muxes	0	0	0	15850	0.00

* Warning! LUT value is adjusted to account for LUT combining.

Group Video Link:

Here is the following link to our Lab 1 Group Demonstration Video:

https://youtu.be/vsz192ahRBg

Reflections:

The first lab of the semester had us design a simple program that introduced the fundamentals of how the FPGA board interacts with Verilog through the Vivado program. We directly connected a 16-bit input of switches, to a 16-bit output of LED's. This directly correlates to how its respective switch, when turned on, will light up its respective LED. Mapping the correct pins is important for this lab because any incorrect configuration can lead to potential errors with the program. Overall, this lab gave the foundation of understanding the design flow, creating verilog, and debugging software and hardware complications.