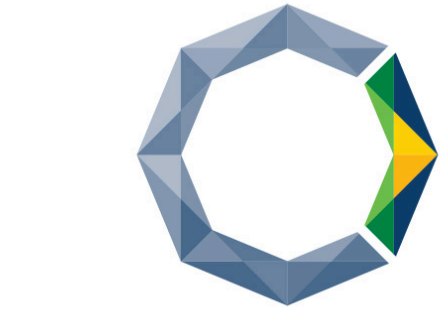

CalPolyPomona

College of Engineering

California Polytechnic State University Pomona

Department of Electrical & Computer Engineering

Digital Circuit Design Lab Verilog

ECE 3300L

Lab Report #1

Experiment #1

Presented By: Kobe Aquino & Daniel Mondragon

Presented to Mohamed Aly

June 18th, 2025

Synthesis Screenshots:

Here is a screen capture of our synthesis screenshot. The full document has been included in our github.

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	0	0	0	63400	0.00
LUT as Logic	0	0	0	63400	0.00
LUT as Memory	0	0	0	19000	0.00
Slice Registers	0	0	0	126800	0.00
Register as Flip Flop	0	0	0	126800	0.00
Register as Latch	0	0	0	126800	0.00
F7 Muxes	0	0	0	31700	0.00
F8 Muxes	0	0	0	15850	0.00

* Warning! LUT value is adjusted to account for LUT combining.

Group Video Link:

Here is the following link to our Lab 1 Group Demonstration Video:

Reflections:

Just a few sentences here of what we learned