

# Let's Chat

A COMPETITION ON  
AI & EVERYTHING

# Digital IC Design Challenge: Large Language Models for RTL Code Generation

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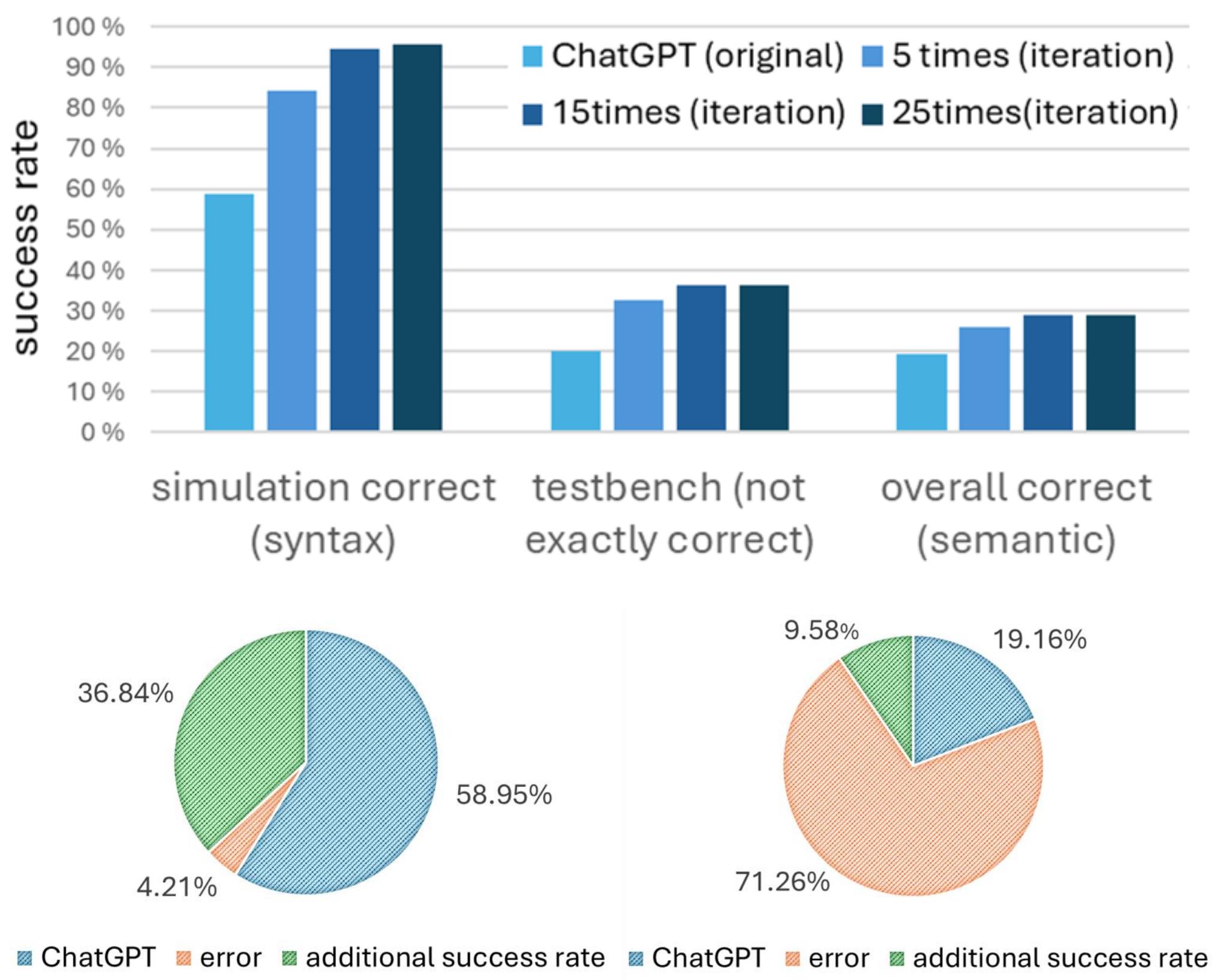
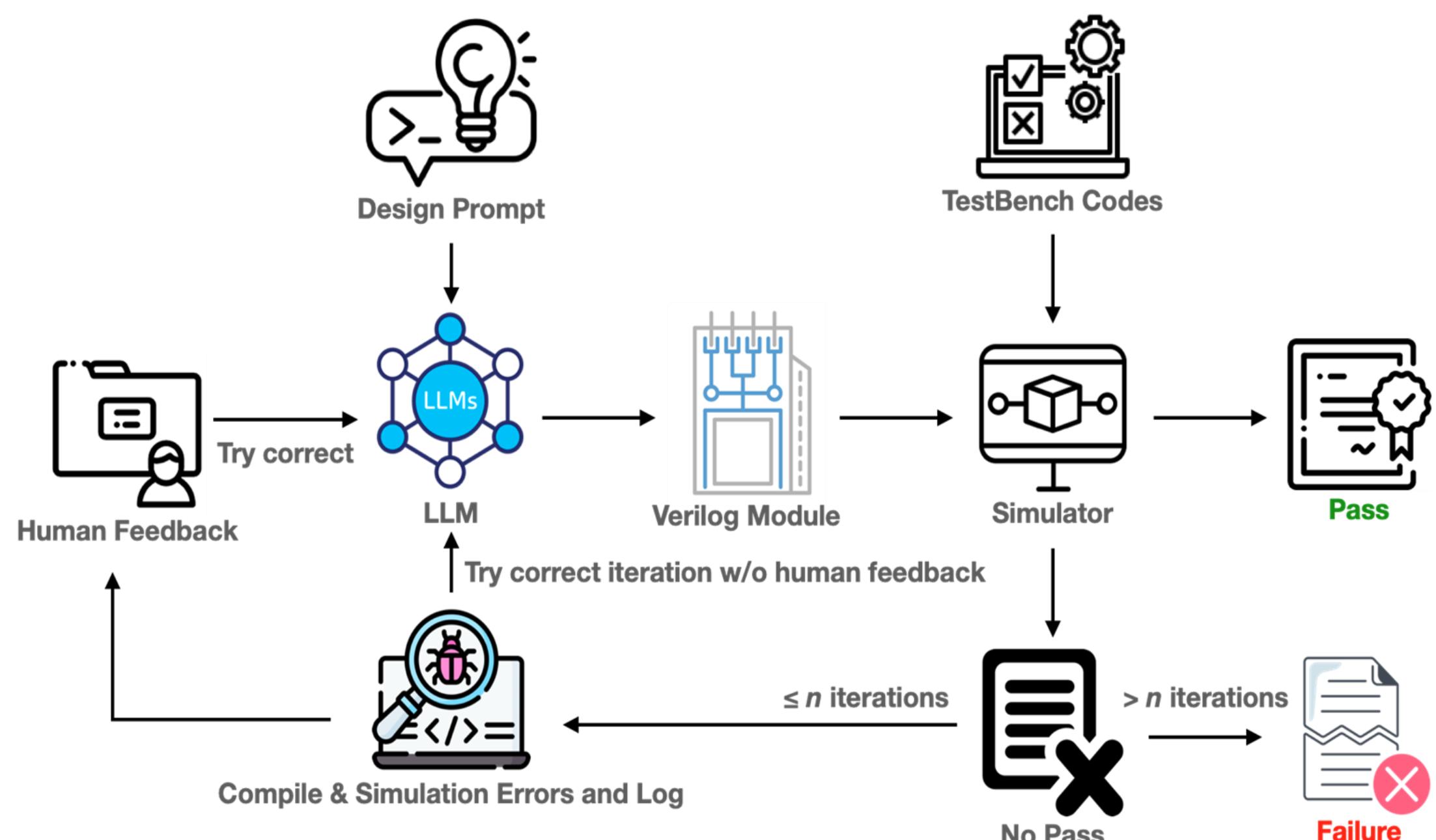
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## Introduction

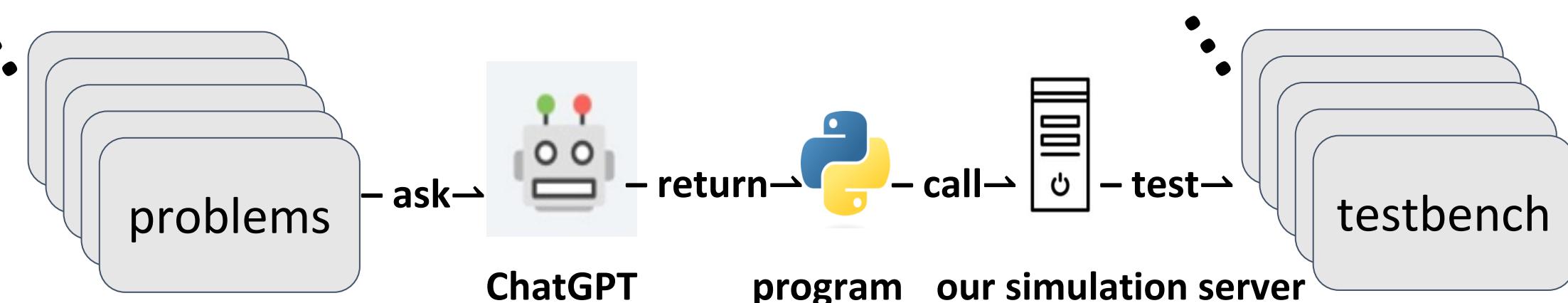
In the domain of digital IC design, RTL code (Verilog) design and verification are essential tasks. This project aims to evaluate the ability of LLMs to generate functionally correct Verilog modules by combining the interactive capabilities of LLMs and the output from Verilog simulators to generate Verilog. We show that incorporating context from EDA tools improves the effectiveness, yielding 1.5X more accurate Verilog modules, compared to open-loop generation by LLMs without augmented retrieval.

## System Flow



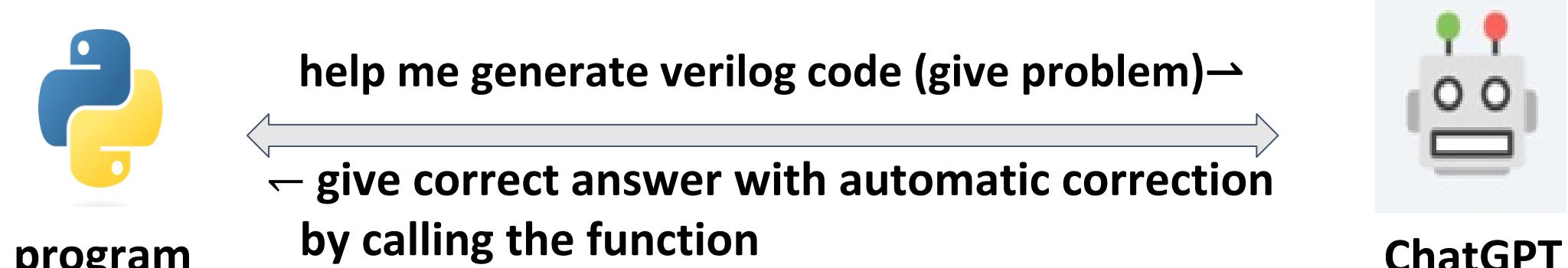
## Study Details

**Design prompt** - A set consisting of 95 kinds of circuit design problems, to ensure the samples are large enough to analyze. There are also 95 testbenches in our project.



## ChatGPT Function calling -

ChatGPT can call a function we provide to guide the process of Verilog code generation until the syntax is correct, which improves system efficiency significantly.



## ChatGPT Statistics -

ChatGPT help us analyze the massive data by obtaining all results and instructions.

## Main Discoveries

- We observed data convergence between 15 to 25 iterations, so we limit tests to a maximum of 25.
- While Syntax correct rate is around 96%, we found that some syntax errors persist even after 25 iterations.
- We achieved a higher success rate when only returned the previous error messages and Verilog module to ChatGPT.
- After 25 iterations, the success rate compared to original success increased by 1.62X (syntax correctness), 1.8X (testbench improvement), 1.5X (overall correctness).

## Takeaway

- LLMs are good at handling syntax error, but poor at semantic.
- There is a long way to go before LLMs can generate semantically correct digital circuit designs.



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