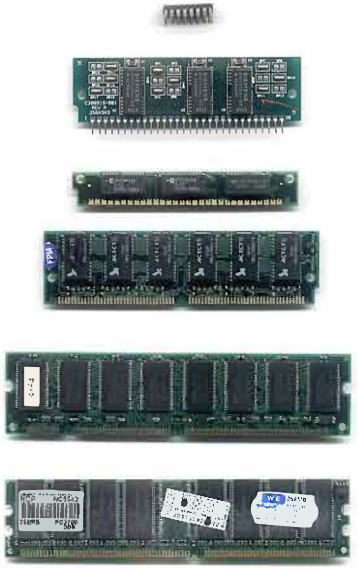
Memory Classification

With respect to the way of data access we can classify memories as:

- random access memories (RAM),
- sequentially accessible memory (SAM),
- direct access memory (DAM),
- contents addressable memory (CAM).

Access time - the interval of time between the instant of data read/write request, and the instant at which the delivery of data is completed or its storage is started.

RAM modules



SAM/DAM memories:

HDDs

tape memories

CD-, DVD-ROMS.

CAM memories find applications in:

switches, routers etc.

CPUs in cache controllers

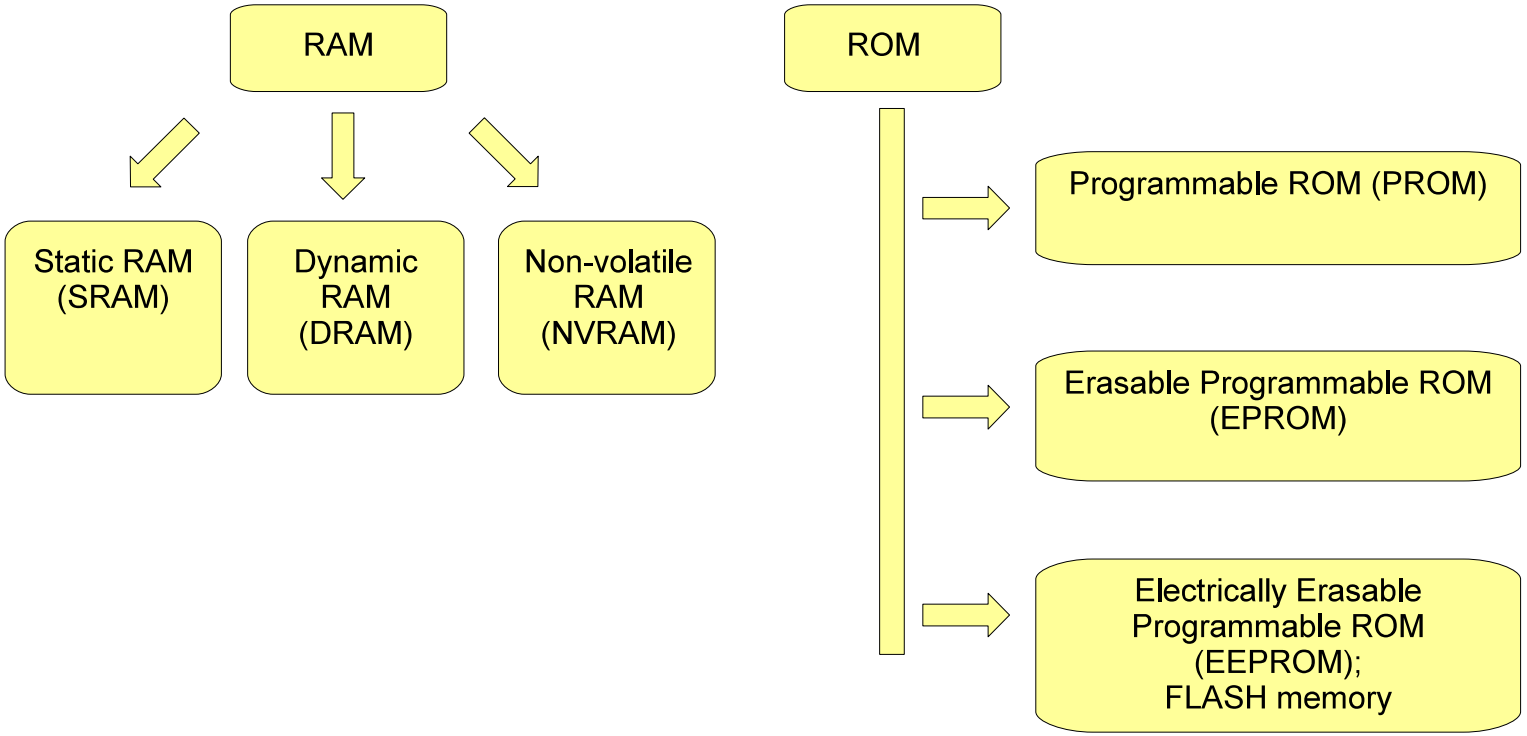
Source of images: Wikipedia.

Memory Classification

Random access memory - the access time to any piece of data is independent to the physical location of data. Access time is constant.

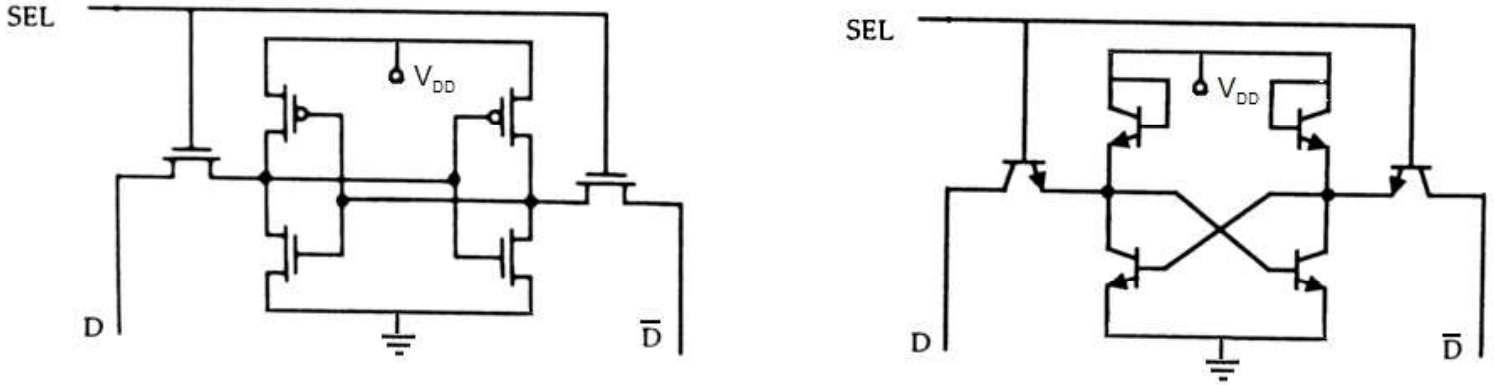
Random access memories can be further classified as:
- read-write memories (usually referred to as RAMs),
- read-only memories (ROM).

Among random access and read-only memories we distinguish:



Random Access Memories

Static random access memories (SRAM) - one-bit memory cells use bistable latches for data storage and hence, unlike for dynamic RAM, there is no need to periodically refresh memory contents.



Schematics of one-bit cell for static random access memory*

In order to **write** data into SRAM cell it is required to activate line SEL and provide bit of information and its inverse at inputs D and $\overline{D}$ respectively.

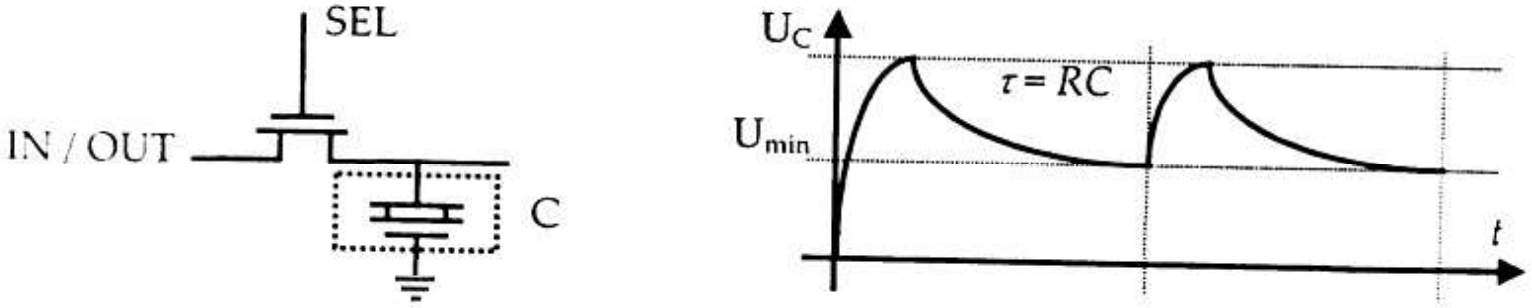
Reading operation requires to activate SEL line. The bit of data is available at D line.

Pros and Cons:
- faster and less power hungry than DRAMs,
- more expensive (6 transistors per cell).

*Source of images: J. Biernat, "*Computer Architecture*", OWPW, Wroclaw, 2005.

Random Access Memories

Dynamic random access memories (DRAM) - each one-bit memory cell uses a capacitor for data storage. Since capacitors leak there is a need to refresh the contents of memory periodically (usually once in τ=0,5 ÷ 2 ms).



Memory cell for dynamic random access memory*

Both **read** and **write** operations require to open the transistor by providing high voltage on line SEL. The bit of data to be written must be given at line IN/OUT. During reading operation the bit of data is available at the same line.

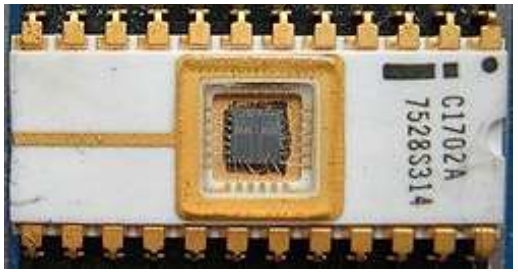
Pros and Cons:
- less expensive (only one transistor per cell),
- slower than SRAM.

*Source of images: J. Biernat, "*Computer Architecture*", OWPW, Wroclaw, 2005.

Read Only Memories

Programmable read only memories (PROM) - are programmed during manufacturing process. The contents of each memory cell is locked by a fuse or antifuse (diodes). PROMs are used for permanent data storage.

Erasable read only memories (EPROM) - there is a possibility to erase EPROM with ultraviolet light (about 20 minutes) what sets all bits in memory cells to 1. Programming requires higher voltage. Memory cells are built with floating gate transistors. Data can be stored in EPROMs for about 10 years.



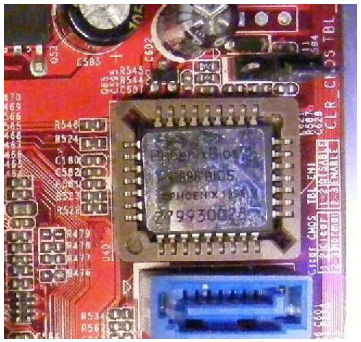
Example of EPROM chip with glass window admitting UV light

Electrically erasable read only memories (EEPROM) - erasing does not require ultraviolet light but higher voltage and can be applied not to the whole circuit but to each memory cell separately.

*Source of images: Wikipedia.

Other Types of RAMs

Non-volatile random access memory (NVRAM) - with this name we refer generally to any memory which does not lose information when power is turned off. Except from ROMs, NVRAM also include conventional volatile random access memories with battery backup such as BIOS memory (Basic Input Output System).



BIOS memory chip with battery*

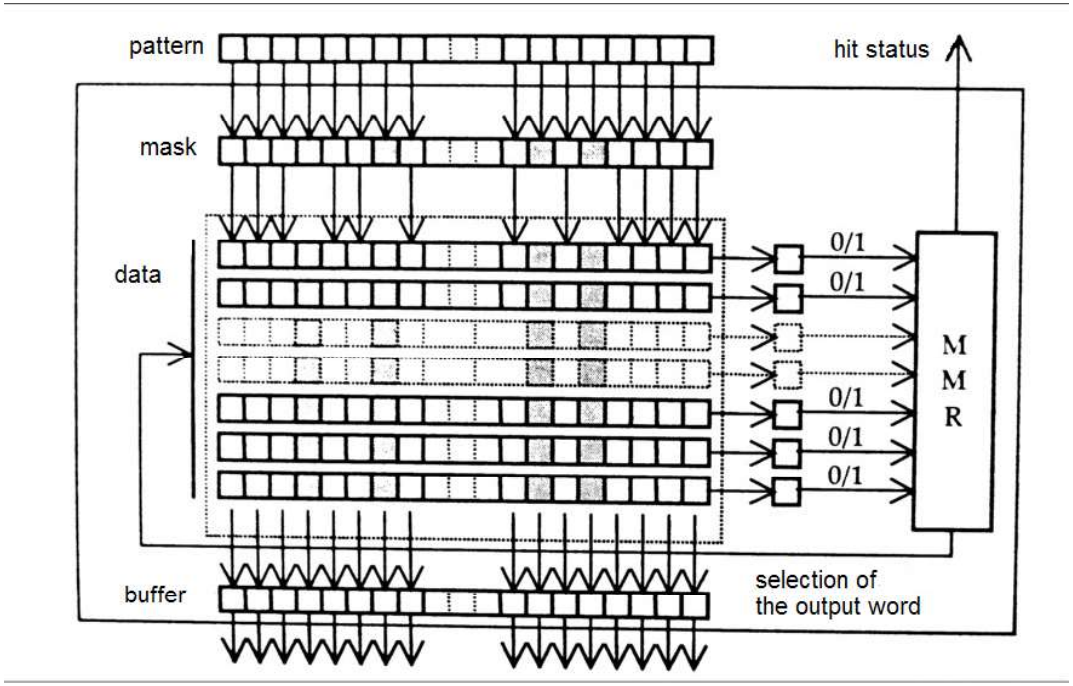
Flash memory (FLASH) - by this name the cheaper variant of EEPROM is described. In case of FLASH memory not separate bytes but blocks of bytes are being erased at the same time. It makes the construction of such memories cheaper in comparison to regular EEPROMs.

Exemplary applications of FLASH memories: pendrives, memory cards

*Source of images: Internet.

Content Addressable Memories

Content addressable memories (CAM) - also known as associative memories; it is a type of computer memory used in applications requiring high speed searching. Such memory replies with “hit” or “lack-of-hit” status when some data vector (pattern) is given at its input. Searching consists in comparing of all data words stored in memory with the given pattern. The mask word indicating all essential bits also must be taken under consideration. If search finishes with hit one of the compliant words is copied to the output buffer. Which word it is determined by the multiply match resolver (MMR).



Logical structure of an associative memory*

*Source of image: J. Biernat, “*Computer Architecture*”, OWPW, Wroclaw, 2005.

CAM/SAM

Applications of CAMs:
- network routing and switching devices where fast resolving of data recipients` addresses is required,
- CPU and disk drive cache memories.

Sequentially addressable memories (SAM) - access to data is realised in a sequential fashion. Fully sequential are buffers organised as FIFO, LIFO, etc. queues. They find their applications in devices controllers, microprocessors, etc.

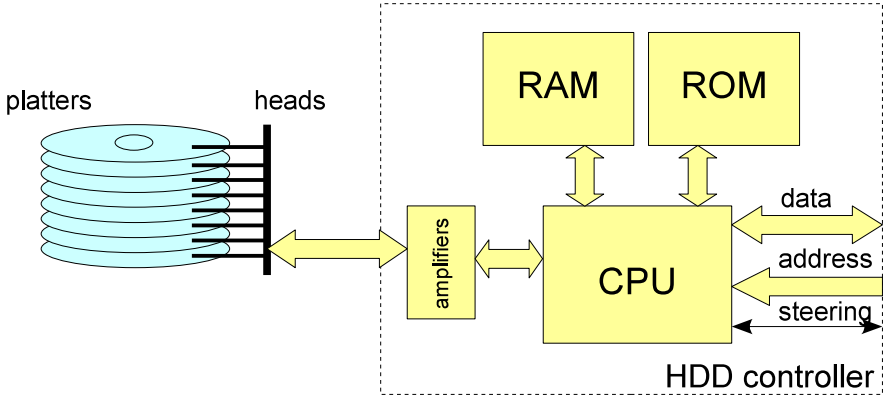
Direct access memory (DAM) - in literature usually by this term authors refer to memories with block organised data. Access to blocks is direct. However data within blocks is accessed sequentially. As examples we can indicate: magnetic and optical disk drives, tape memories, etc.

Sequentially Accessible Memory

Hard disk drive (HDD) - is a kind of mechanical device memory where data is encoded in the form of magnetic impulses on platters covered with magnetising ferromagnetic material.

Hard disk drive memory

The typical HDD consists of: stepper and linear motors, read-and-write heads, platters and disk controller. The controller includes central processing unit, RAM and ROM memories and data amplifiers circuits. Communication between CPU and HDD requires transmission of data, commands (to appropriate registers of HDD controller) and status words.



Sequentially Accessible Memory

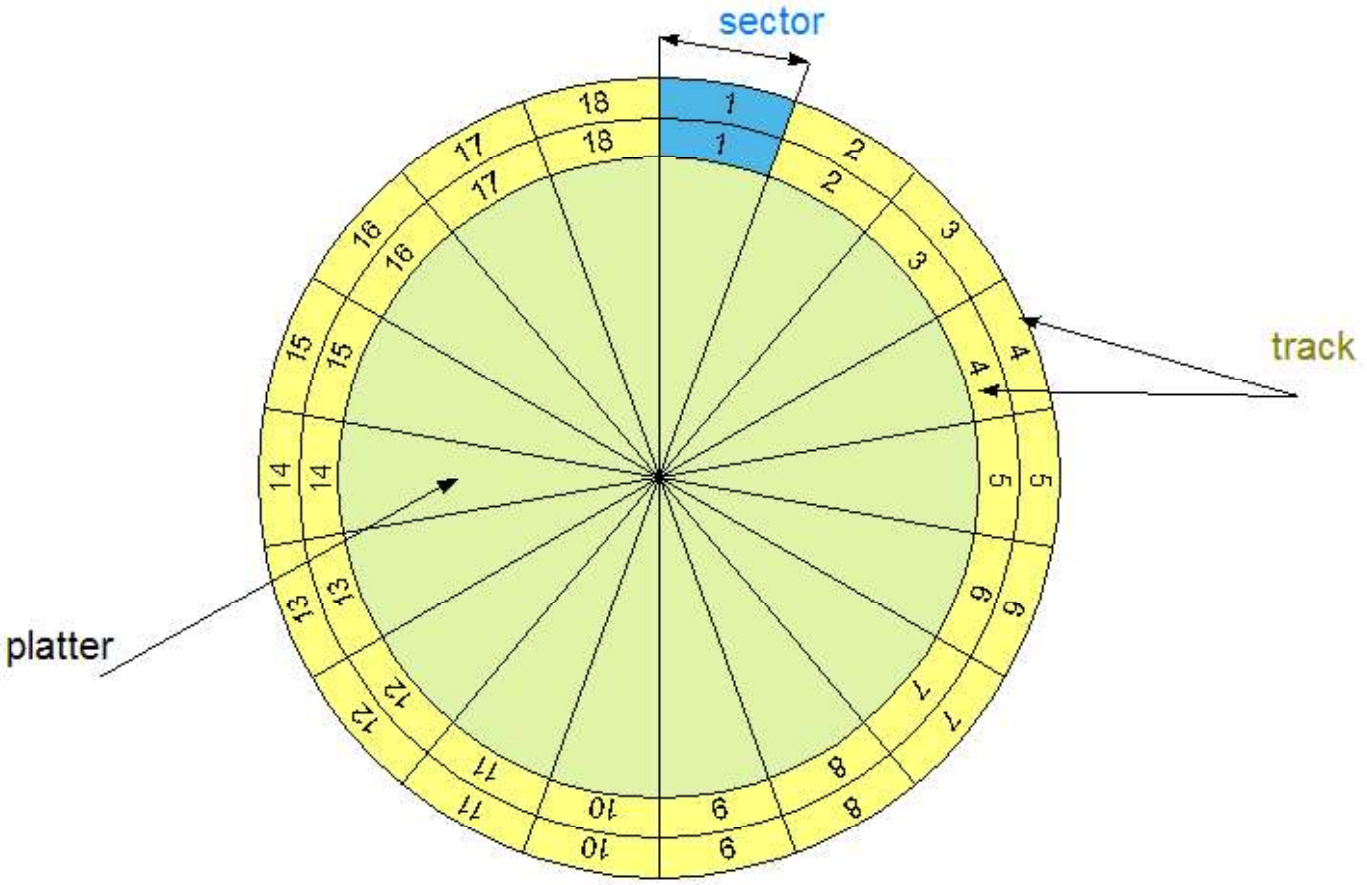
Physical organisation of disks:

head - corresponds with one side of a platter;

track - circular area on platter where data is stored;

sector - a fragment of track that is the smallest portion of data to be read or written on disk;

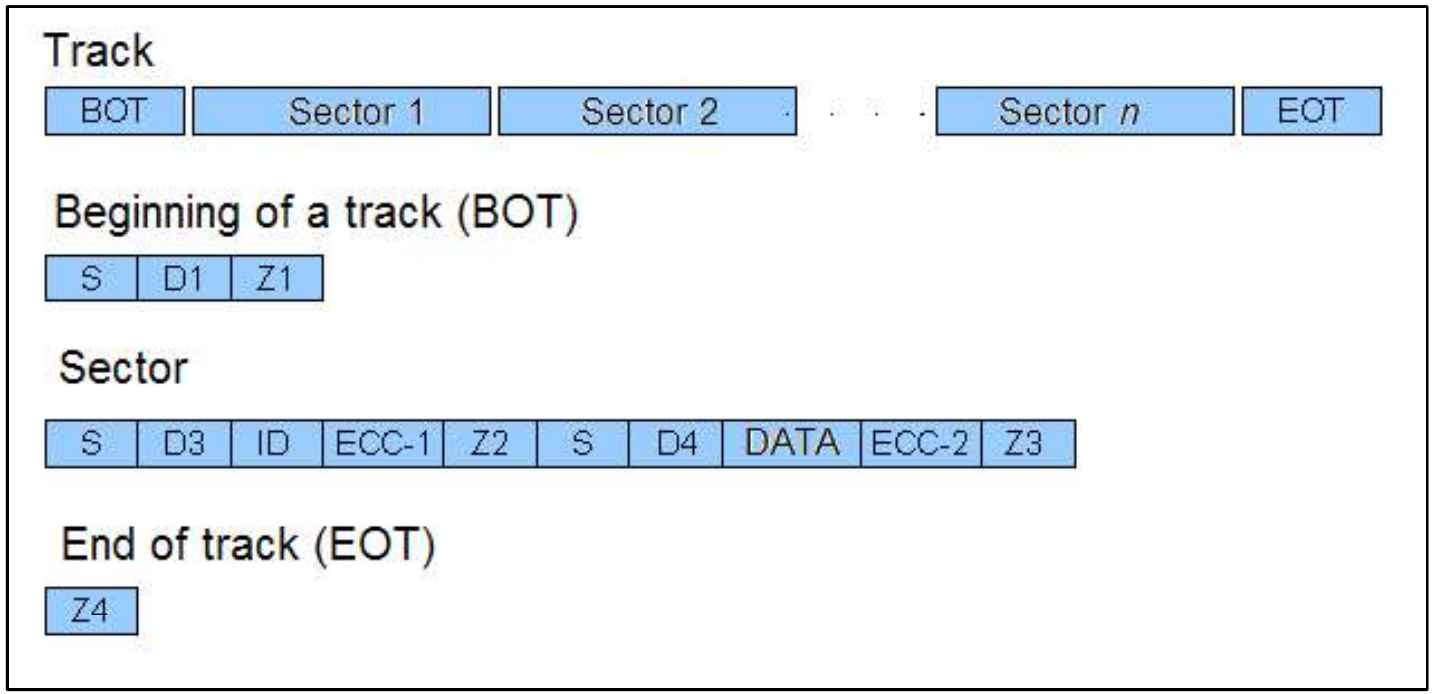
cylinder - a set of tracks with the same number belonging to different platters.



Physical organisation of a disk

disk_capacity = number_of_heads*number_of_tracks*number_of_sectors*512 [B]

Sequentially Accessible Memory



Structure of a disk track

S (BOT) - 11 bytes 00h, **D1 –** 0A1FCh, **Z1 –** 12 bytes 0FFh,

S – 10 bytes 00h, **D3 –** 5EA1h, **ID –** sector address ID: byte 1 – track number, byte 2 – head number, byte 3 – sector number, byte 4 – sector status (invalid sector, sector replacement in spare area), **ECC-1, 2 –** byte of error correction code (correction up to 11 errors), **Z2 –** 5 bytes 00h, **D4 –** 5EA1h, **DATA –** 512 bytes, **Z3 –** 3 bytes 00h and 17 bytes 0FFh, **Z4 –** about. 93 bytes 00h.

Sequentially Accessible Memory

The remaining track fields play the following roles: S - head-controller synchronisation field; D1, D2, D3 and D4 - signatures indicating the beginnings of specific parts of a track; Z1, Z3 - gaps compensating the variation in platter rotating speed.

Such track structure is determined during low level formatting.

During manufacturing process disks are checked for invalid (damaged) sectors. Each disk contains in its -1 track the list of invalid sectors. That list is called **Grown Error List** (GEL). There exist a big variety of tools that allow to peek into GEL on disk.

Each track contains spare area for sector replacements. Hence invalid sectors in a track can be replaced with simple operation of sector skipping (called **sector-slipping**). Such operation is transparent to operating system.

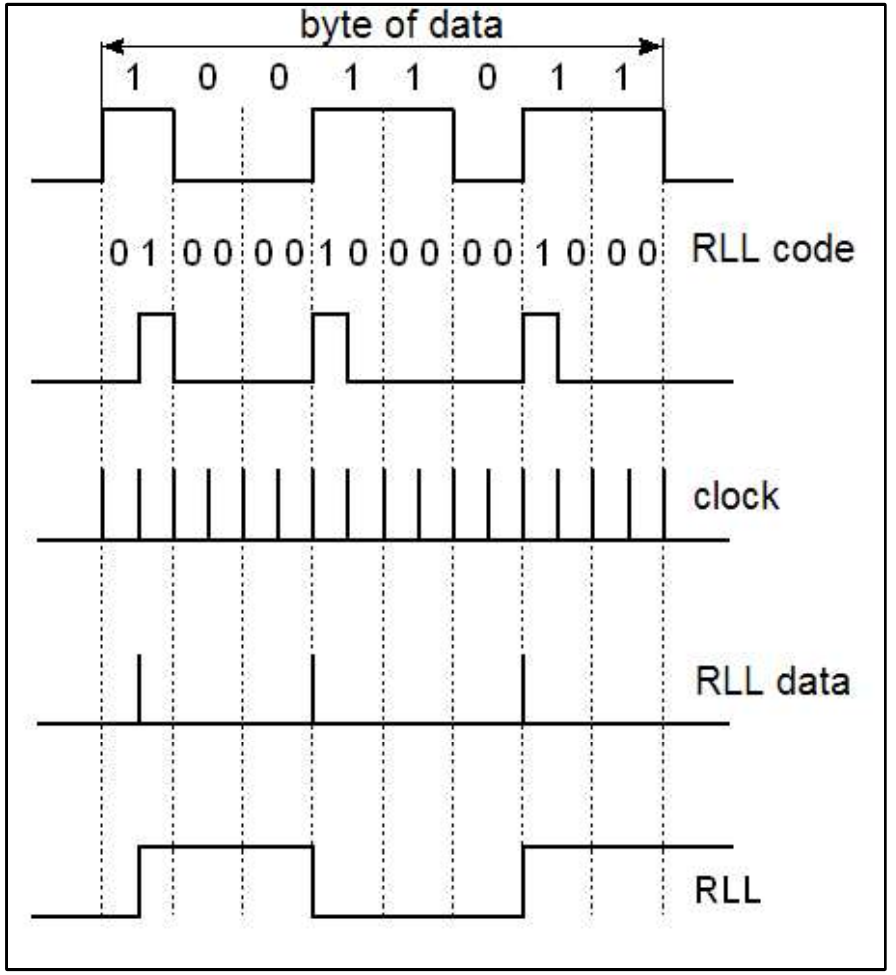
Error correction codes (ECC) - constitute additional protection for data stored in sectors and allow to correct up to 11 faulty bits.

Sequentially Accessible Memory

RLL data recording technique

Run Length Limited (RLL) is a technique applied to data recording on magnetic disks. Each input byte is divided into parts, i.e. chains of bits, that obtain their new bit chain representatives. Such sequences of bits are written on a magnetic layer. Bits with value of 1 correspond with a change in direction of a magnetic field.

Input data	RLL representatives
000	000100
10	0100
010	100100
0010	00100100
11	1000
011	001000
0011	00001000



Example:

10011011 -> (10) + (011) + (011) ->

(0100) + (001000) + (001000)

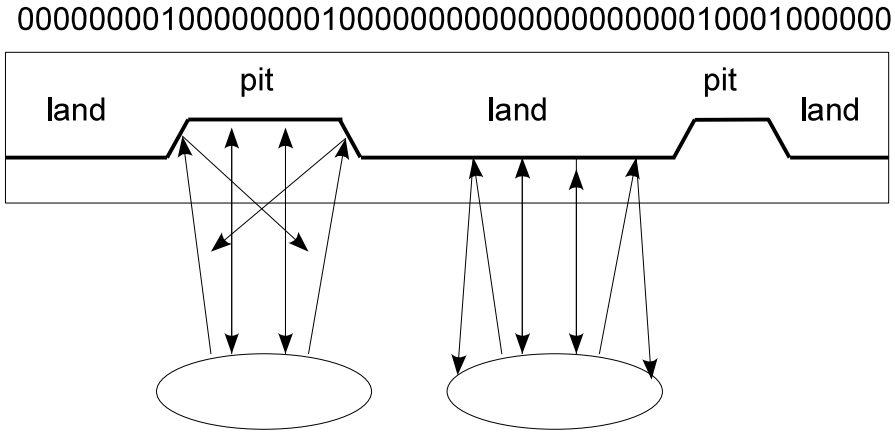
Sequentially Accessible Memory

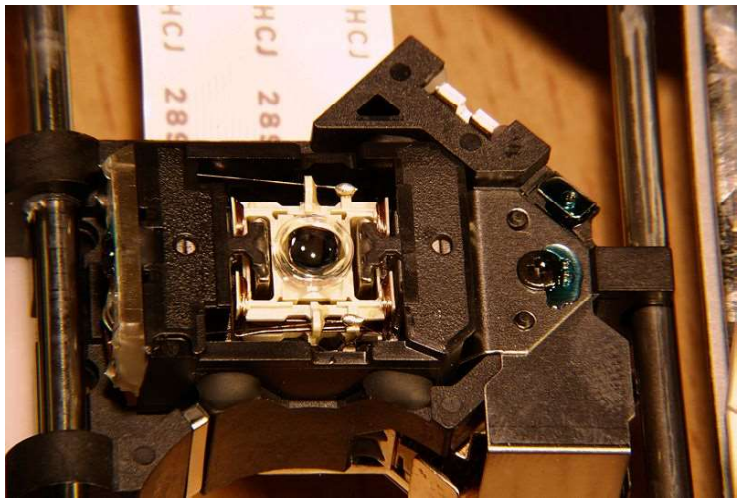
CD-ROMs

In compact disks for data storage one spiral track is used. Data is stored on the disc as the series of microscopic indentations (“pits”) that cause destructive interference of laser light resulting in reduction of intensity of the reflected beam.

The linear data density is constant what means that the linear rotational speed of the disk is linear. Such approach requires more complicated reading/writing circuits.

The track is divided into sectors each storing 2352 bytes. First 12 bytes contain synchronisation data and next four a sector header. The following 2kB are predestined for user data storage and immediately behind we have: 4 bytes of CRC codes, 8 bytes filled with zeros and 278 bytes of ECCs.





Laser structure*

*Source of image: Wikipedia.