ET4 171 Processor Design Project

I. Assignment

The goal of the project is to improve the performance of a MIPS-based computing platform (Plasma) by focusing on computer architecture and computer arithmetic relevant aspects. To evaluate your new design, you are given a set of benchmarks from the GMPbench and MiBench suites, and remote access to a Virtex4 ML410 FPGA board. As a starting point for this project you have to use the virtual machine provided, which includes all the necessary files and tools for the ET4 171 Processor Design Project.

II. Schedule

The project kickoff meeting will take place on **April 26th from 10:45 to 12:30** in EWI-Lecture Hall Data. During this meeting, the project teams will be formed and I'll present the project assignment in more details. Given that the project has to be completed in the 4th quarter of the academic year you have to keep the pace with the following schedule:

April 26th	**Kickoff Meeting**
May 16th/ 17th	**Milestone Group Meetings**
June 15th	**Report Submission**
June 22nd	**Project Presentation**

III. (Recommended) Approach

Before you start the core redesign you should first exercise the Plasma platform in order to get familiar with the toolset and with the VHDL description, as well as to evaluate the performance of the baseline design, and its potential for improvement. To assist you in that the virtual machine includes:

1. A prototype design of a minimal SoC (System-on-a-Chip) containing the Plasma processor implemented on the Virtex4 ML410 FPGA board.
2. A project manual that assists you in the simulation, synthesis, and implementation of the SoC, describes the remote evaluation procedure on the Virtex4 ML410 FPGA board, and briefly documents the components of the SoC prototype design.
3. The C source code, assembly listing and simulation set-up for the evaluation benchmarks.

After you are sure that you master those aspects you may proceed with the core optimization. Generally speaking, there are several avenues you may follow in order to improve the performance of the Plasma

core. In this project however you should try to focus on computer arithmetic relevant issues as well as on (micro) architectural aspects. In view of that you can concentrate on the following aspects:

1. **Improve the arithmetic parts of ALU.** The Plasma core contains a 32-bit serial multiplier/divider (*rtl/mult.vhd*) that takes 32 cycle to compute the result. You can significantly improve the multiplier/divider's performance.

2. **Decrease the critical path delay.** You can find the timing information of the SoC from the "Synthesis Report" in ISE. Maybe you can improve the performance in the critical path, which will increase the frequency significantly. Bear in mind that between the benchmark score and the maximum clock frequency of the SoC there is a linear dependence. Thus, if an optimization can make the frequency to be improved 1.2 times, a 1.2 times benchmark score can be achieved.

3. **Architectural improvements.** There are plenty of opportunities to improve the components of the processor core and the memory subsystem. You may also operate changes on the Plasma core architectural features that may improve the performance and do not require compiler changes. Changes of the instruction set architecture can also be pursued, with the afferent architectural and compiler changes.

In general, you may follow any other path as long as: (i) it results in performance improvements, and (ii) you do computer architecture & arithmetic relevant work.

When you make any change into the Plasma core, a simulation is required before you synthesize this project to make sure your design runs correctly. Follow the instructions in the project manual to do the simulations.

If your design is bug free you may follow the implementation procedure described in the project manual to evaluate your design on FPGA. To be more effective you may skip the final step in early stages of the project when the ISE synthesis report provides you enough information to further change your design. However, when you are converging to the final solution you need to upload the design in the FPGA in order to get performance evaluation scores.

IV. Milestone Meeting

The milestone meeting is per group and it is meant to be a midterm status check. **It is NOT optional!**

For the milestone meeting you have to:

- Get familiarized with the project set-up and the FPGA server.
- Carry on the performance evaluation of the base-line processor design on the FPGA server with the provided benchmark suite.
- Increase the cache size from 4KB to 8KB, and 16KB. Evaluate the performance impact of the cache capacity extension.

- Modify the cache mapping mechanism such that 4MB of the main memory can be cached. Evaluate the performance of the enhanced designs for 4KB, 8KB, and 16KB caches.
- Identify at least two more possible improvement avenues.

For the milestone meeting you are required to present a short progress report that:

- Describes and comments the impact of memory hierarchy changes on the platform performance.
- Presents the improvement approach that you decided to follow (justify your choices), the expected performance improvement, and the work status (up to date achievements).

Apart of the meetings you can always send e-mail to the ET4171 lab team, make use of our "open door" policy, and/or make an appointment.

V. Project Submission

In your final submission, you should include:

- The report – preferably a bookmarked pdf - (naming convention: et4171_2017_report_g#, with # being the group number);
- An archive (naming convention: et4171_2017_src_g#, with # being the group number) containing:
    - the rtl folder with your modified design,
    - the ISE folder with the .xise and .ucf files.
- If any other modifications are carried out, those files should be provided as well, e.g., the folder my_patches for compiler related modifications.

The report should include the following:

1. The general idea behind you overall optimization proposal. Related to the parts that you decided to change or to append you have to answer (at least) these questions: What, how, and why?
2. The design of the improved and/or appended part(s). There is no need to go at the gate level! The basic algorithm you decided to implement and the RTL designs are in general enough. In case some parts are relevant you may go to full adder/gate level if this is essential for your proposal.
3. Performance results for the baseline design (the original Plasma system) and your improved core. Those should include the following: Detailed implementation results including timing information, critical path information, resource utilization information from ISE report, and power consumption figures.

4. A comparison between your design and the baseline design which includes the basic metrics, i.e., area (A), critical path delay (deduced from clock frequency) (D), benchmarks scores in terms of execution clock cycles (BSs), power consumption (P), as well as compound metrics, e.g., A*D and P*D products, etc. Comment on the obtained results and try to identify which improvement is contributing to which figure of merit.

5. Conclusions.

The report may also include, but it is not mandatory, suggestion for this project! Your feedback is very much appreciated.

VI. Final Presentation

Each group has to give a 20-minute presentation of their project in the context of a symposium to be held on June 22nd 2017. Details on the scheduling will be available in due time. In the presentation, you have to highlight the main ideas behind your proposal and present the results. After the presentation 5 minutes are reserved for questions from the auditorium.

VII. Evaluation Procedure

The projects functionality will be verified and checked for (including between groups) plagiarism.

If the project is not functional you **DO NOT** pass the course. Plagiarism can also make you fail.

Your final score for the project is determined based on the following criteria:

- The performance of your design (DP). The benchmark scores you report are important. The higher the benchmark score you get the better but this is not the only relevant aspect. In the performance evaluation, we also take into consideration the other metrics with more emphasis on the compound ones.
- The technical merit of your approach (TM). Aspects as innovation level and implementation quality are considered.
- The report (R). Report organization, content, and language are important aspects at this point.
- The presentation (P). Here we also look at the capability to ask questions and to answer questions from the auditorium.

The ET4 171 final grade is computed as:

$$Grade = 0.35 * DP + 0.35 * TM + 0.20 * R + 0.10 * P - C.$$

C can assume values between 0 and 1 and reflects:

- The lack of collaboration within the group;
- The amount of consultancy you asked for during the project completion.

If the group is functioning like a team and you do not ask too much help C is 0.