

# Implementing Neural Networks on Memory-based Reconfigurable Logic Device (MRLD)

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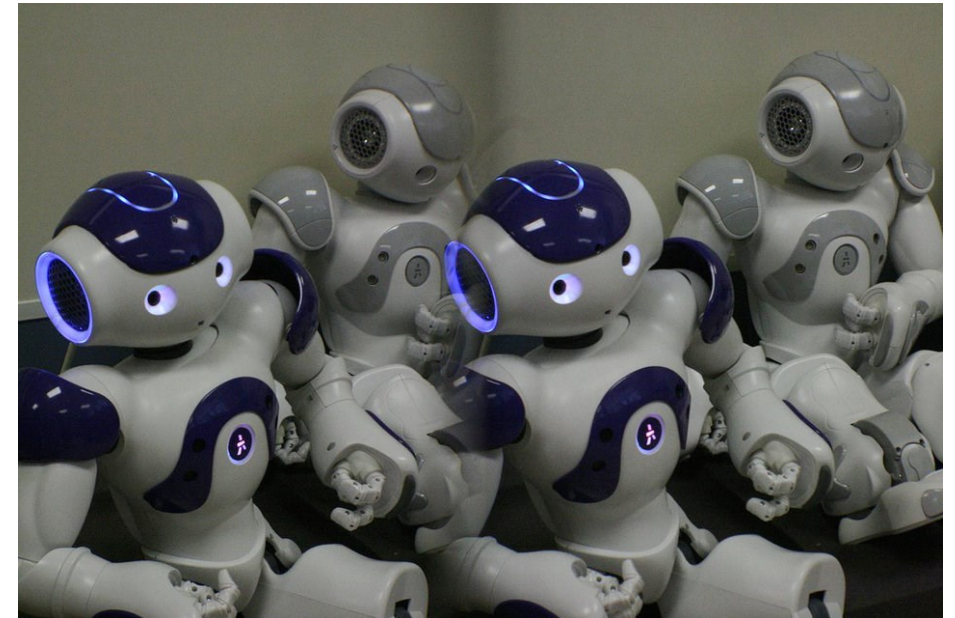
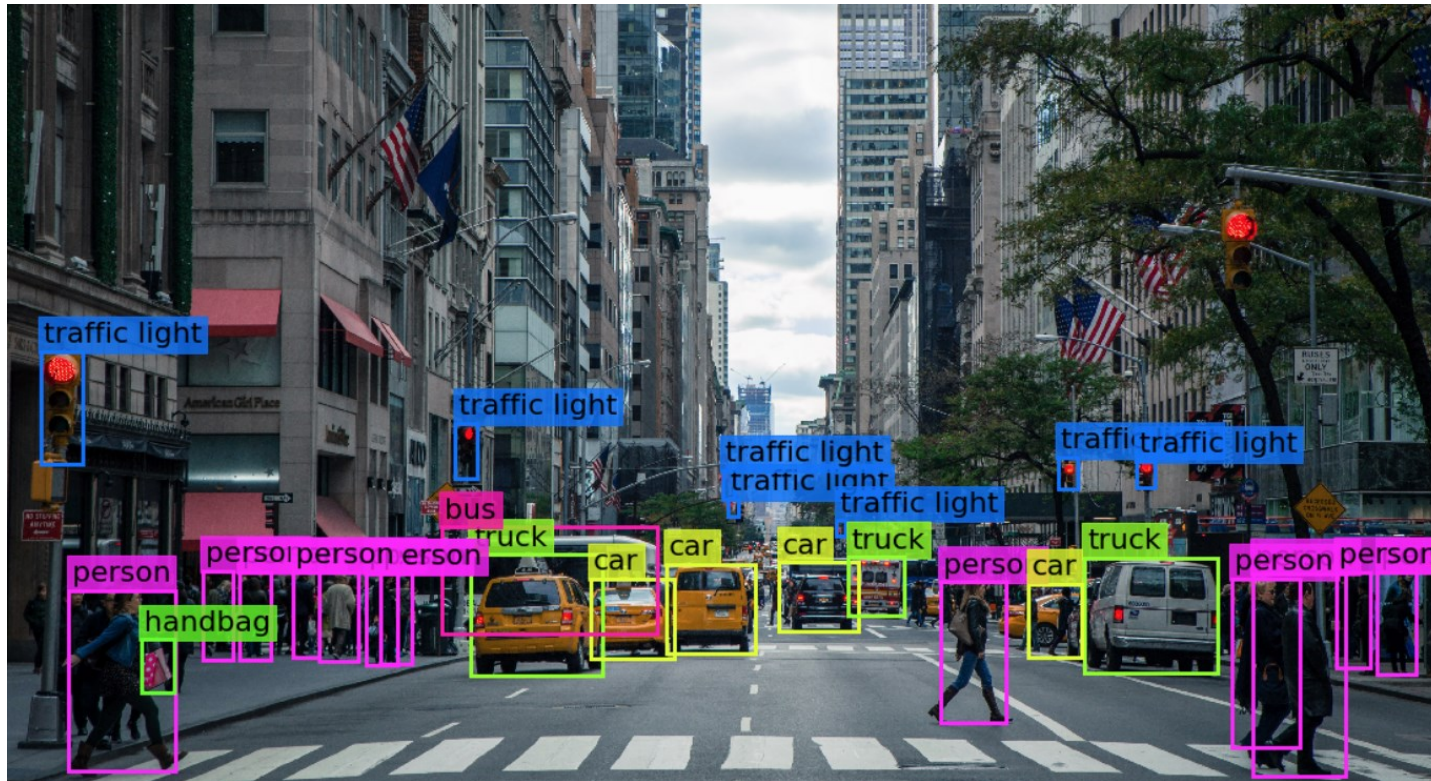
*September 18, 2020*

# Outline

- Introduction
- What is MRLD
- The basic operation of Neuron in MRLD
- MRLD-based Neural Network: MNN
- Experimental results
- Conclusions

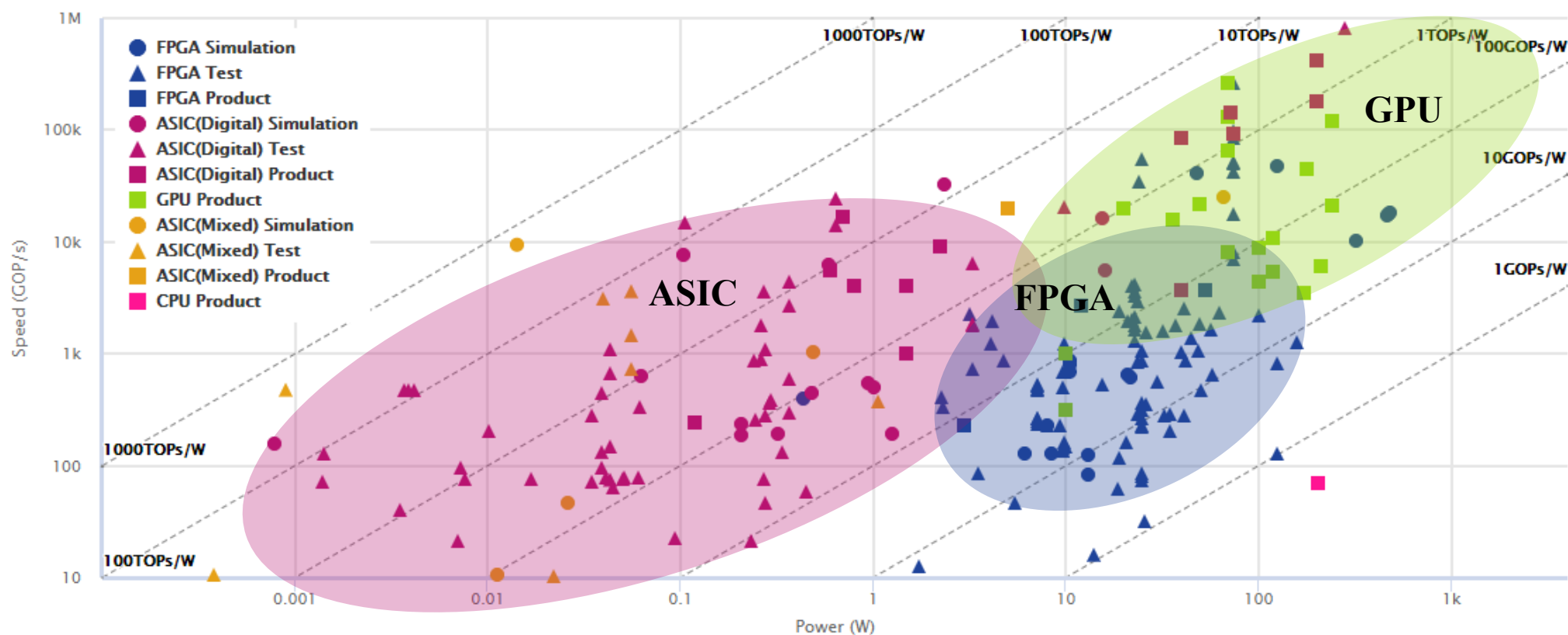
# Background

- Neural networks (NNs) algorithm has achieved significant contributions.
  - Computer vision, speech recognition, robotics.



# Background

- NNs usually with **Millions of parameters** → requires **high-performance** computing device.
- **Hardware design** for NNs is gaining great attentions.
- GPUs: high speed, high power, ASIC: low power, high development cost .
- **Reconfigurable devices**: flexible and scalable (such as FPGA) .



Neural Network Accelerator Comparison

<http://nicsefc.ee.tsinghua.edu.cn/projects/neural-network-accelerator/>

# Background

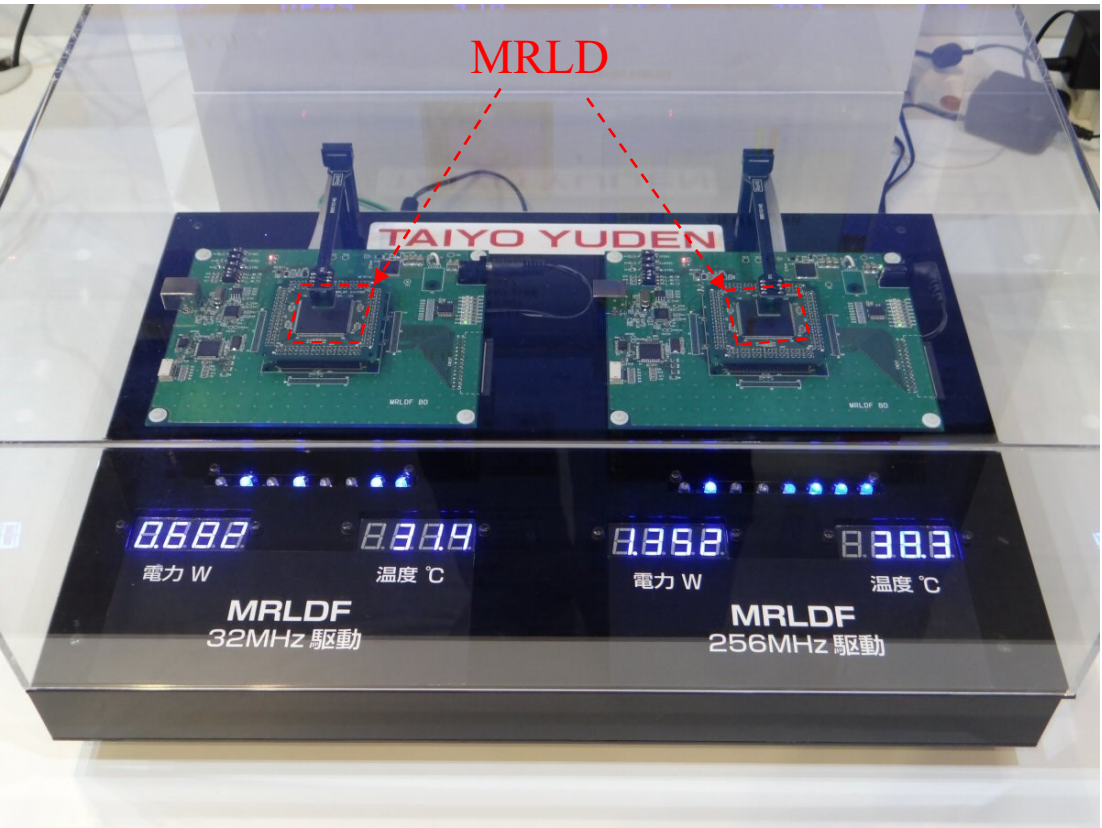
- For edge devices  
(e.g.: battery-powered mobile devices, robots, etc.) → high-performance, low power is required.





# Background

- MRLD is a new type of **reconfigurable device**.
- Compared with existing technology FPGA, **high speed**, **low power**, and **low cost**.



5 times faster than FPGA and 1/10 the power consumption

<https://xtech.nikkei.com/dm/atcl/event/15/091100139/100200019/>

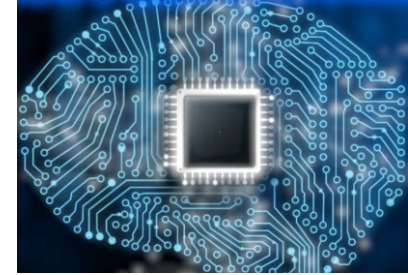
	GPUs	ASICs	FPGAs	MRLDs
high speed	○	△	△	○
low power	×	◇	△	○
Flexible and scalable	△	×	○	○

Expression degree: ○ > ◇ > △ > ×

[https://www.yuden.co.jp/resource/data/ProductMovie/jp/MRLD\\_PV\\_Yuden\\_J\\_S\\_1807.mp4](https://www.yuden.co.jp/resource/data/ProductMovie/jp/MRLD_PV_Yuden_J_S_1807.mp4)

# Motivation & Purpose & Objective

- MRLD is a promising alternative Edge AI device for NNs application.



- Purpose

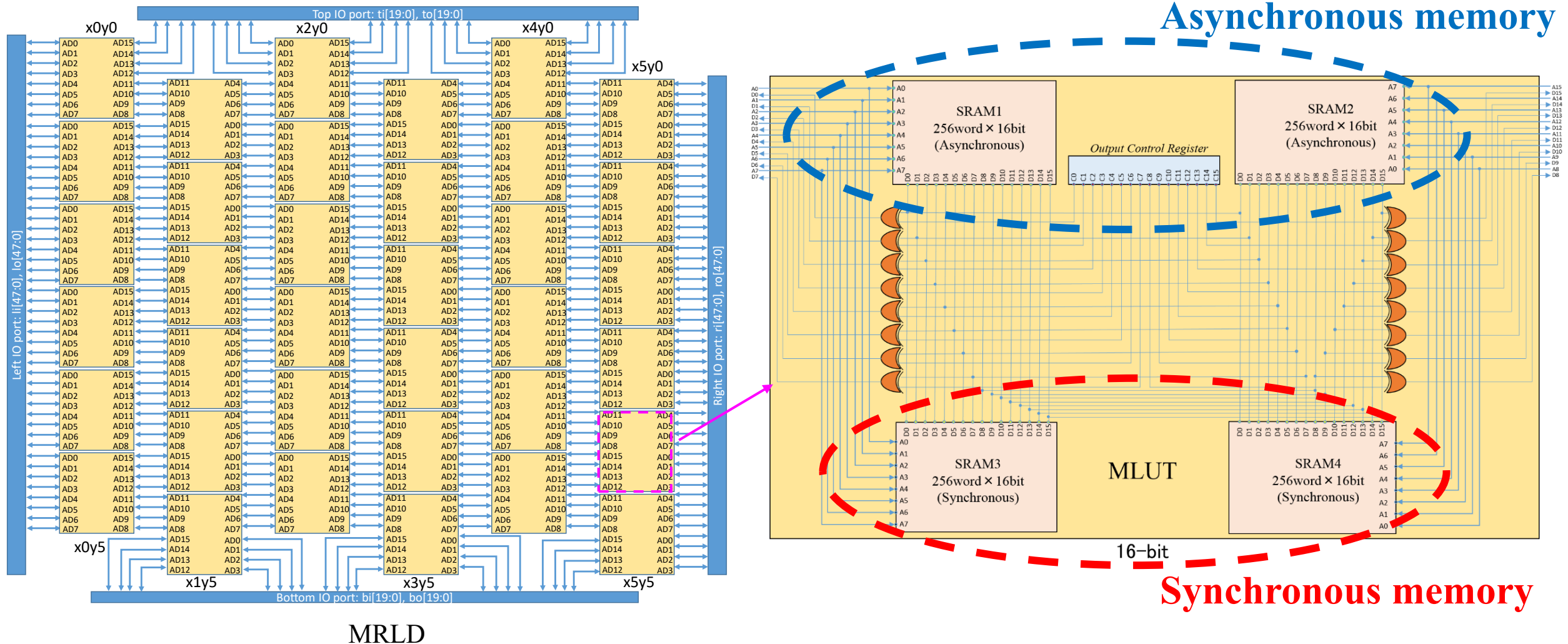
Develop the approaches for implementing the neural network into the MRLD

- Objective

- 1. Analyzing the basic operation of NN neurons in MRLD**
- 2. Propose a novel network structure to adapt the special structure of MRLD**

# What is MRLD

- An MRLD (Memory-based Reconfigurable Logic Device) is composed of multiple general-purpose memory cells (MLUTs: Multiple Look Up Tables) arranged in an array.



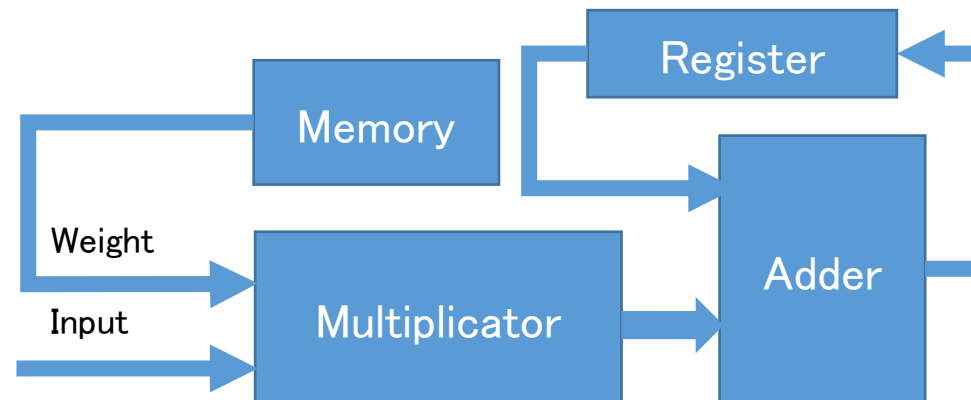
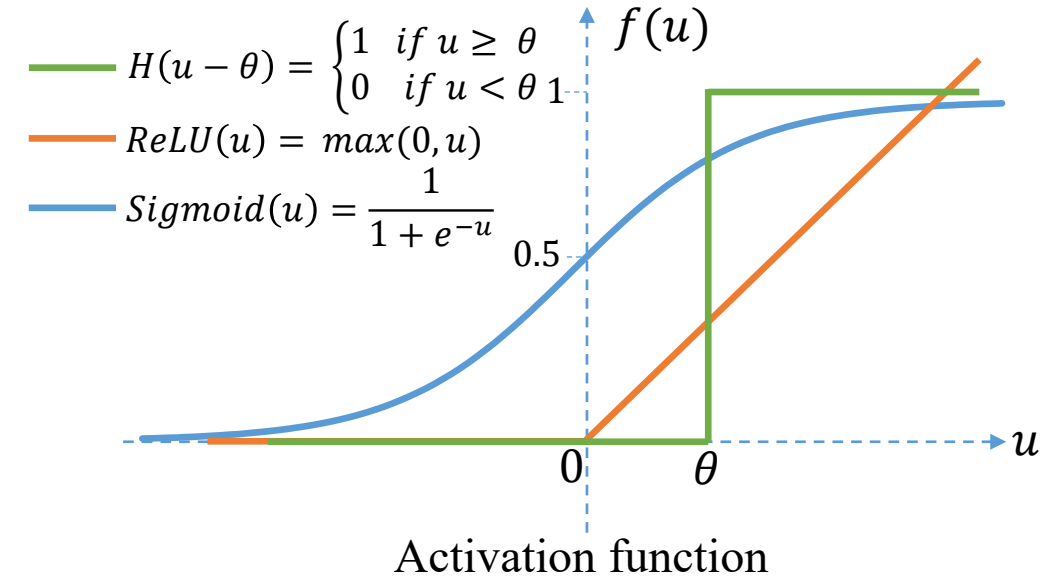
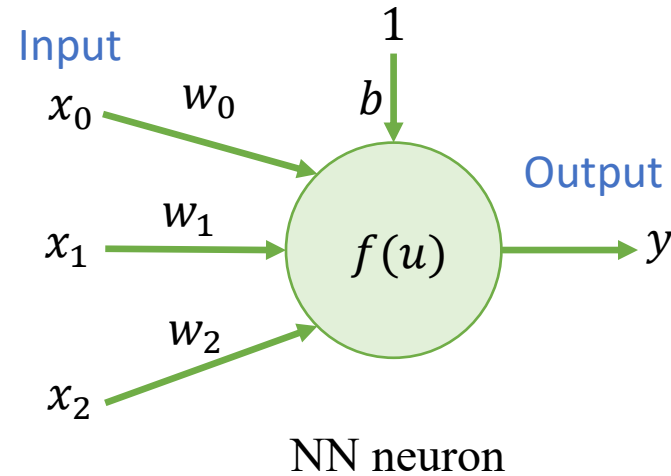




# The traditional hardware design for NNs

- The multiply-accumulate operation circuit , memory are necessary for NNs hardware design in traditional design method.

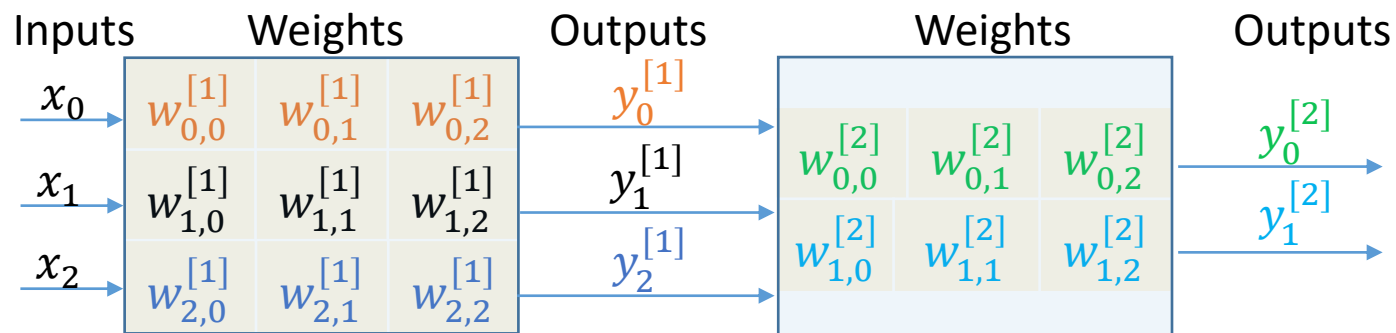
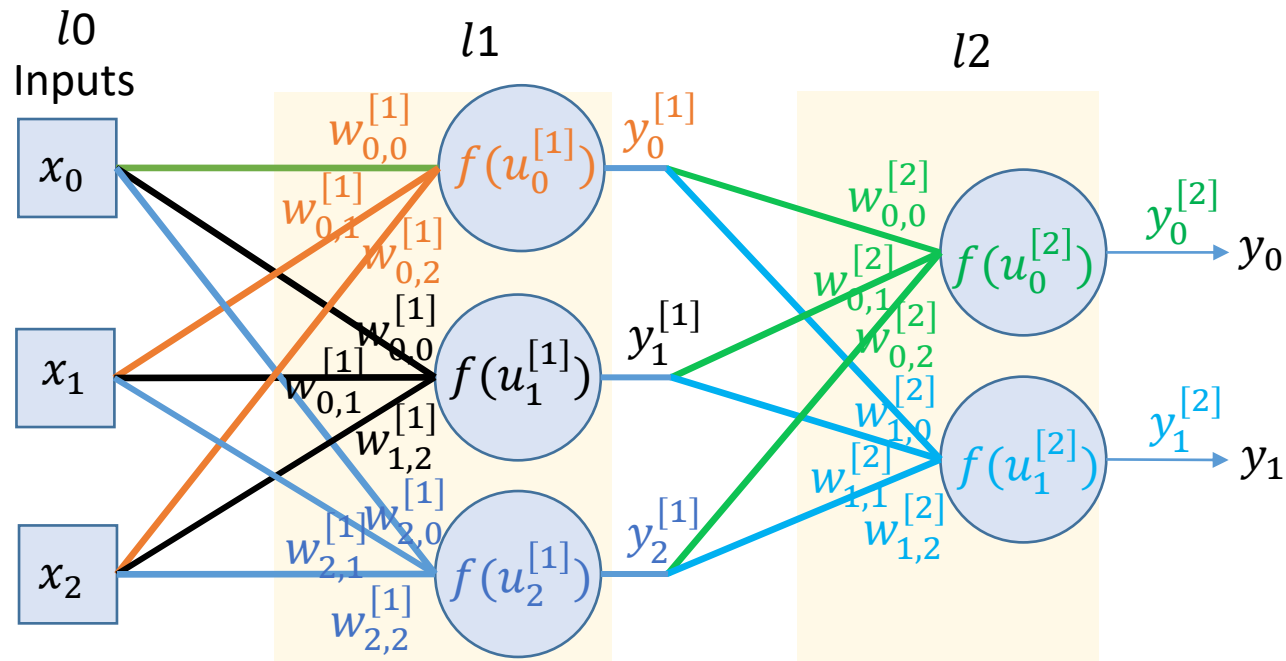
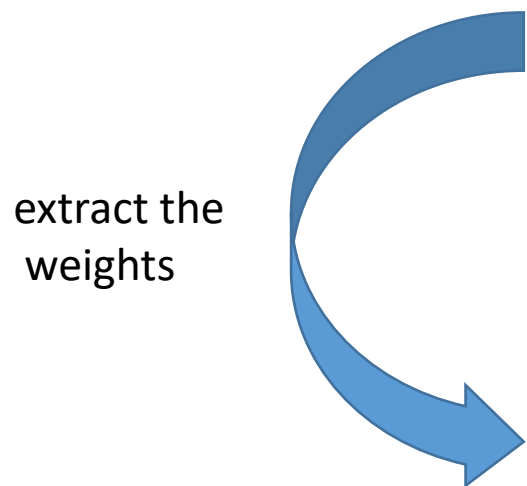
$$u = \sum_{i=0}^N w_i * x_i + b$$
$$y = f(u)$$



Traditional hardware design: Multiply-add and memory for neuron

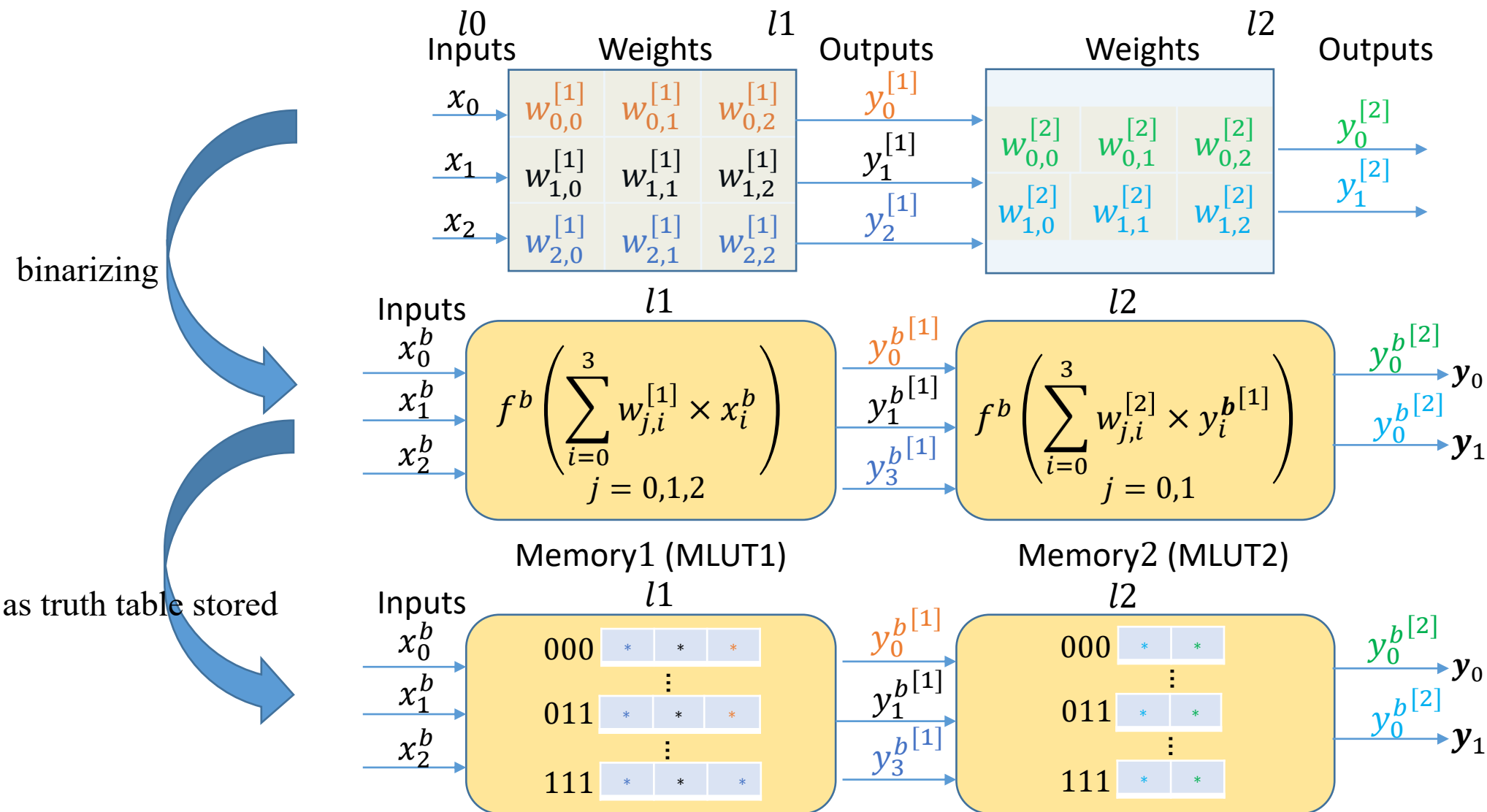
# The basic operation of Neuron in MRLD

- The weights can be extracted and form a mapping for  $x$  and output  $y$ .



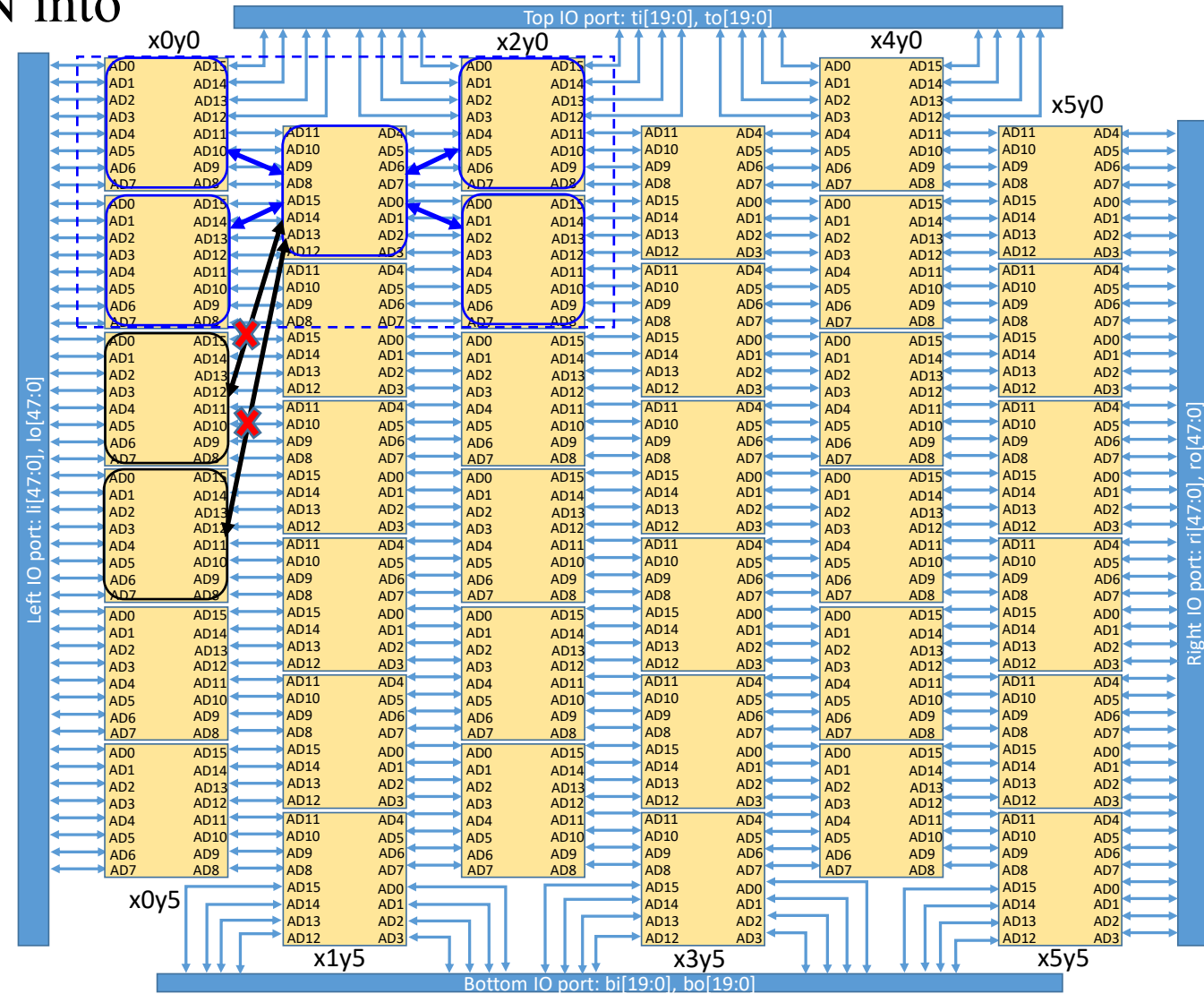
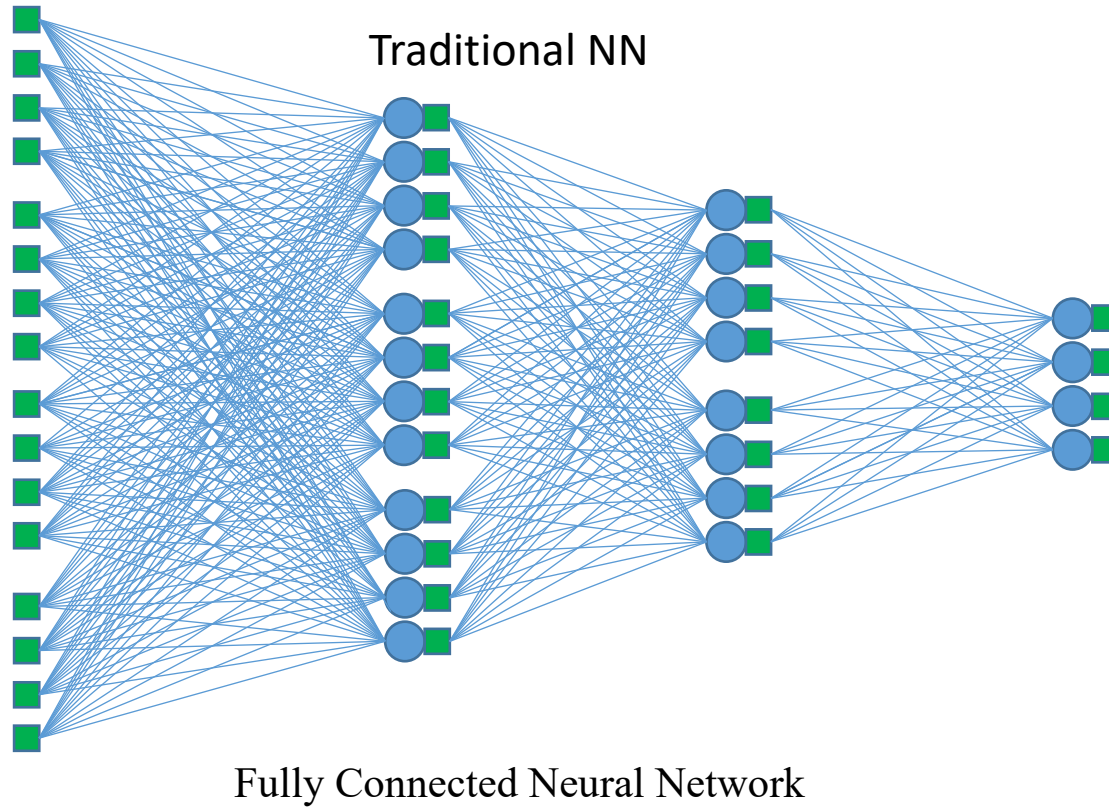
# The basic operation of Neuron in MRLD

- In MRLD, the NN neurons can be calculated in truth table form by binarizing inputs and outputs of NN which does not require constructing any logic circuits.



# For the MRLD structure: Traditional NN is not suitable

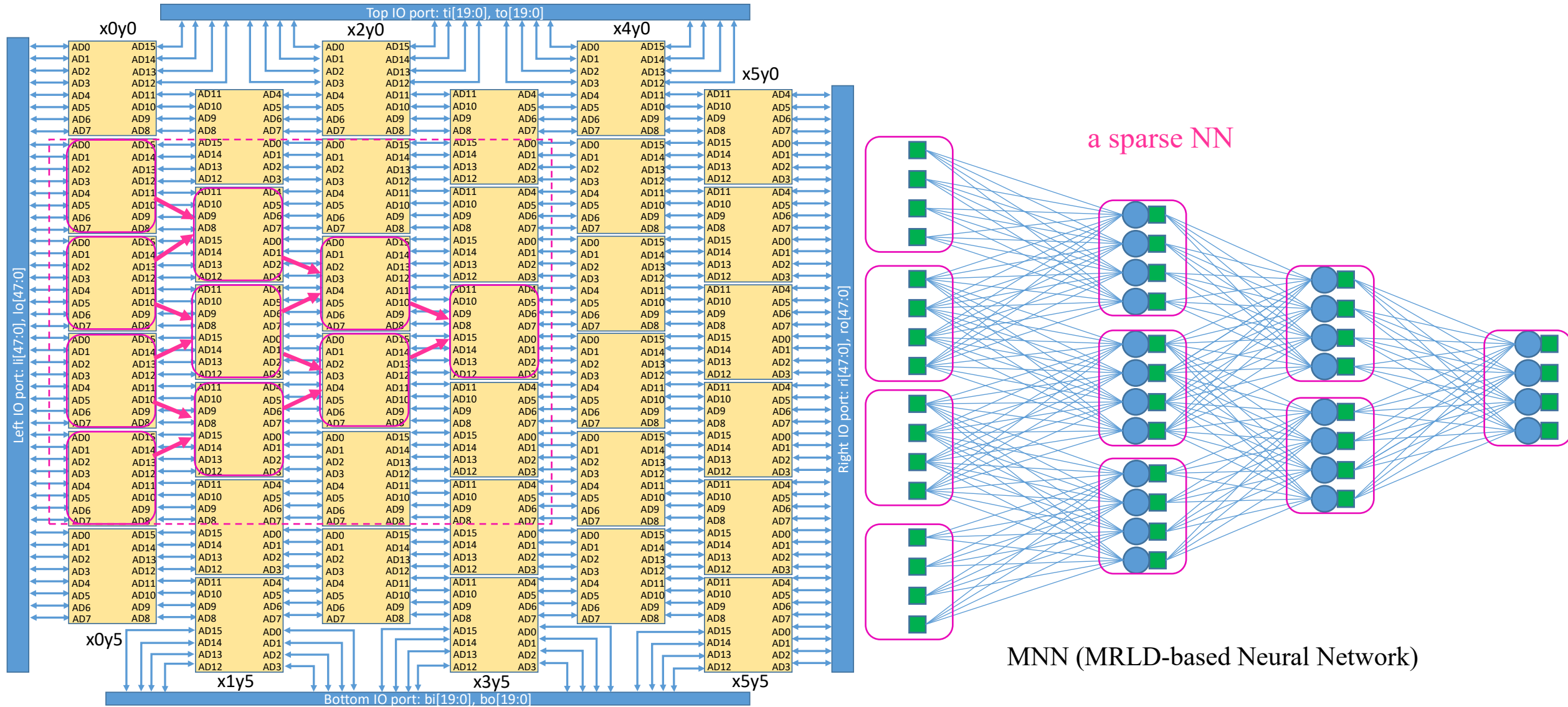
- It's difficult to construct the traditional NN into the MRLD with the fully connection way



MLUT connection structure in MRLD

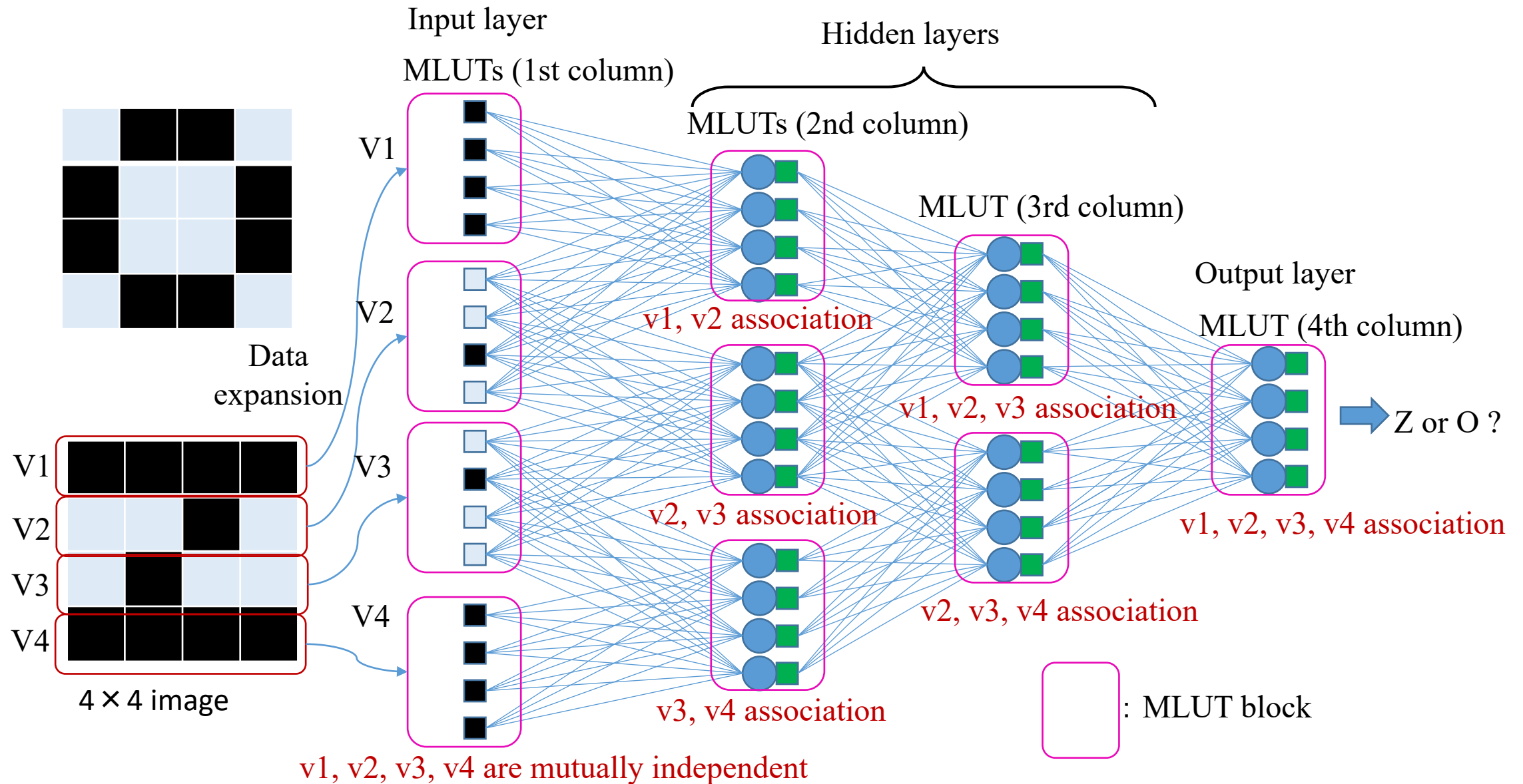


# To adapt the MRLD structure: MNN ( MRLD-based Neural Network )

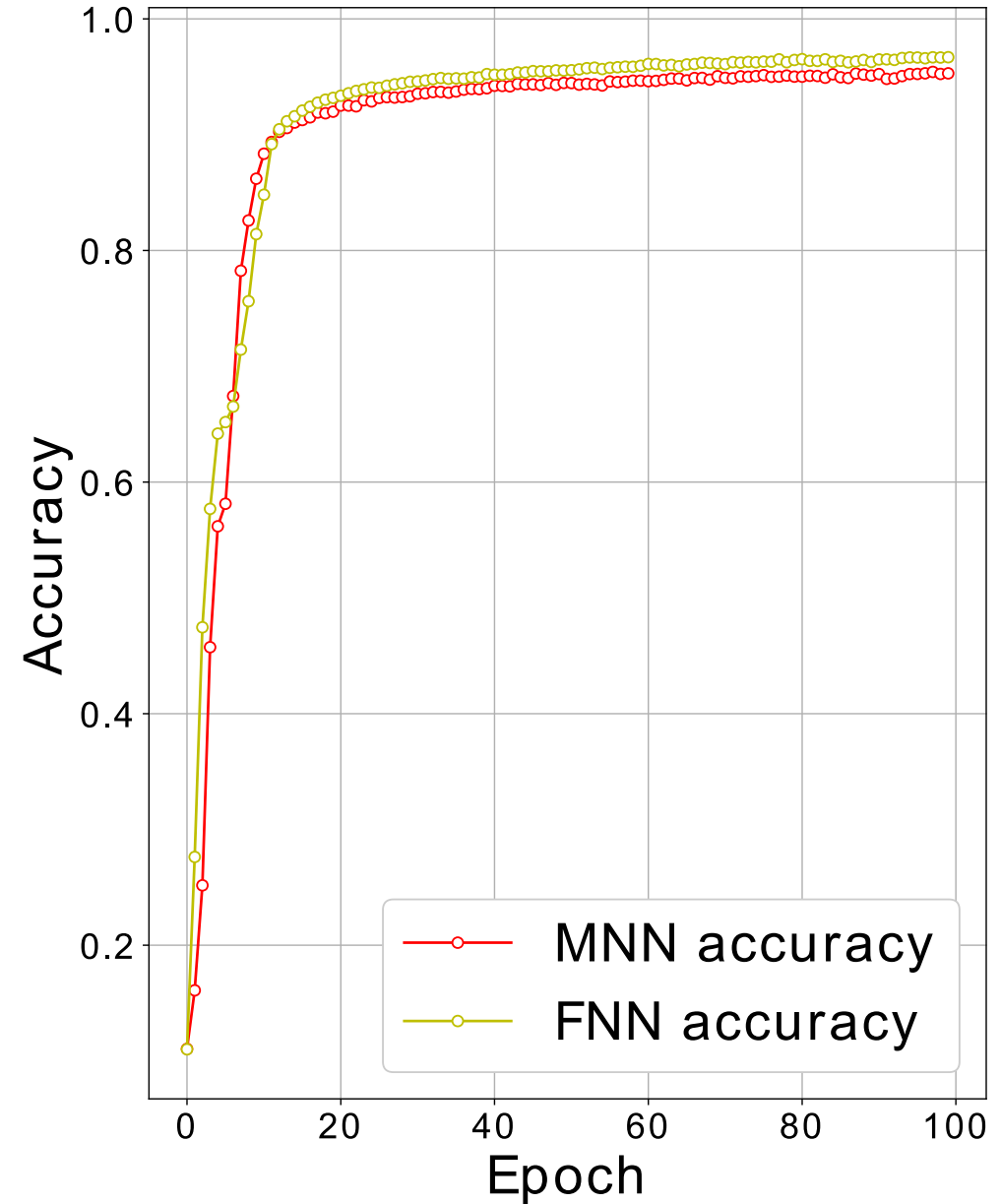
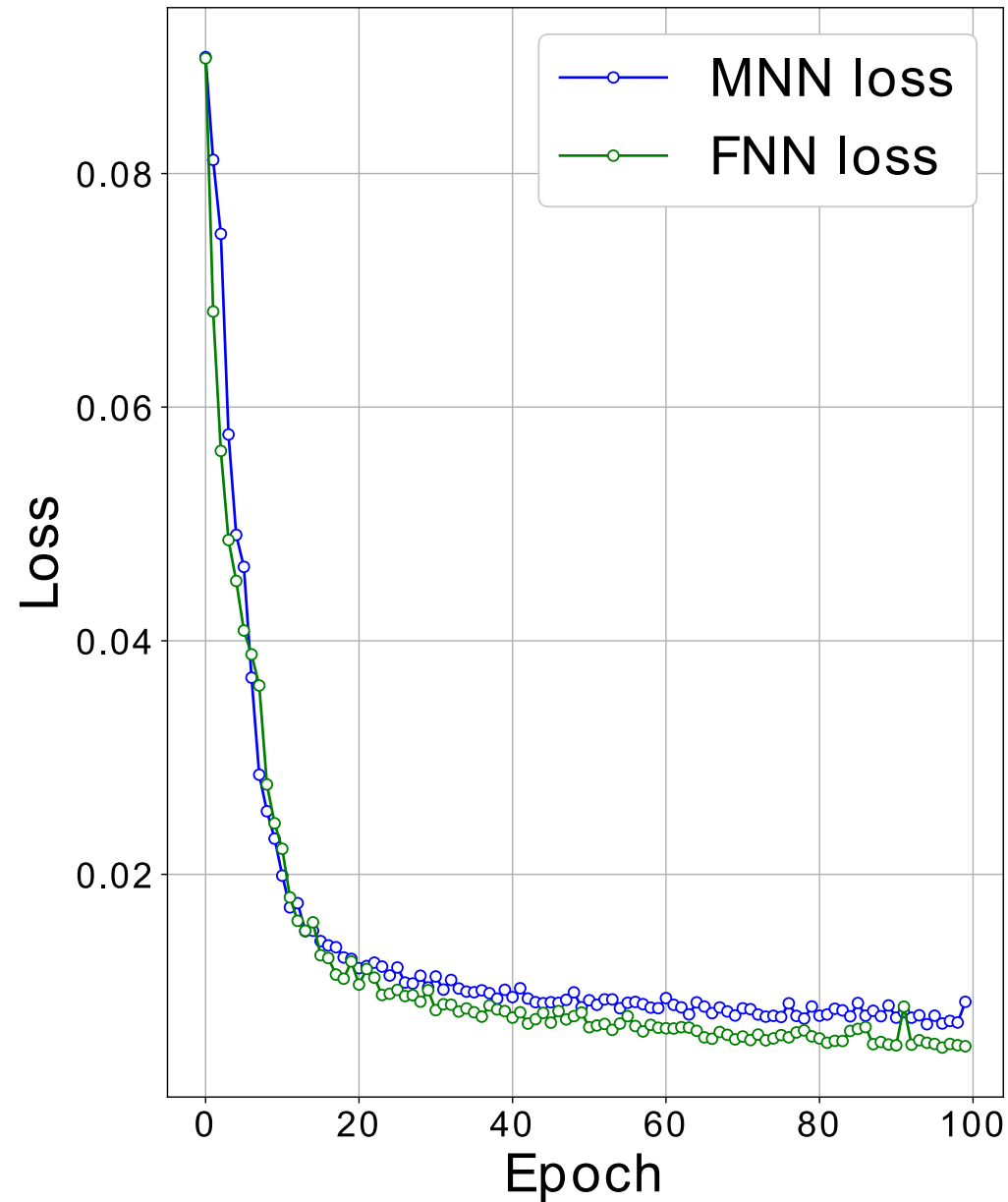


MLUT connection structure in MRLD

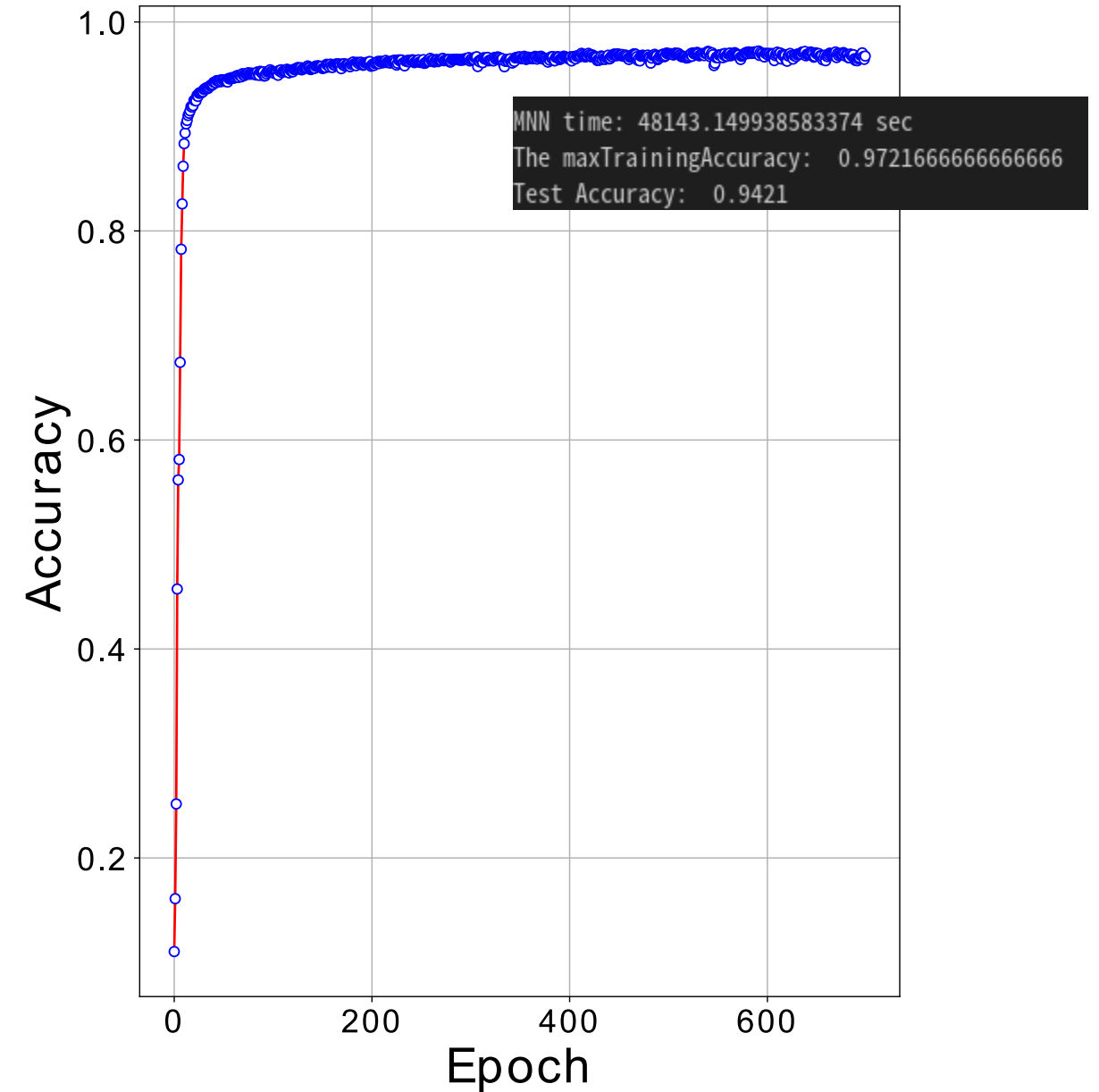
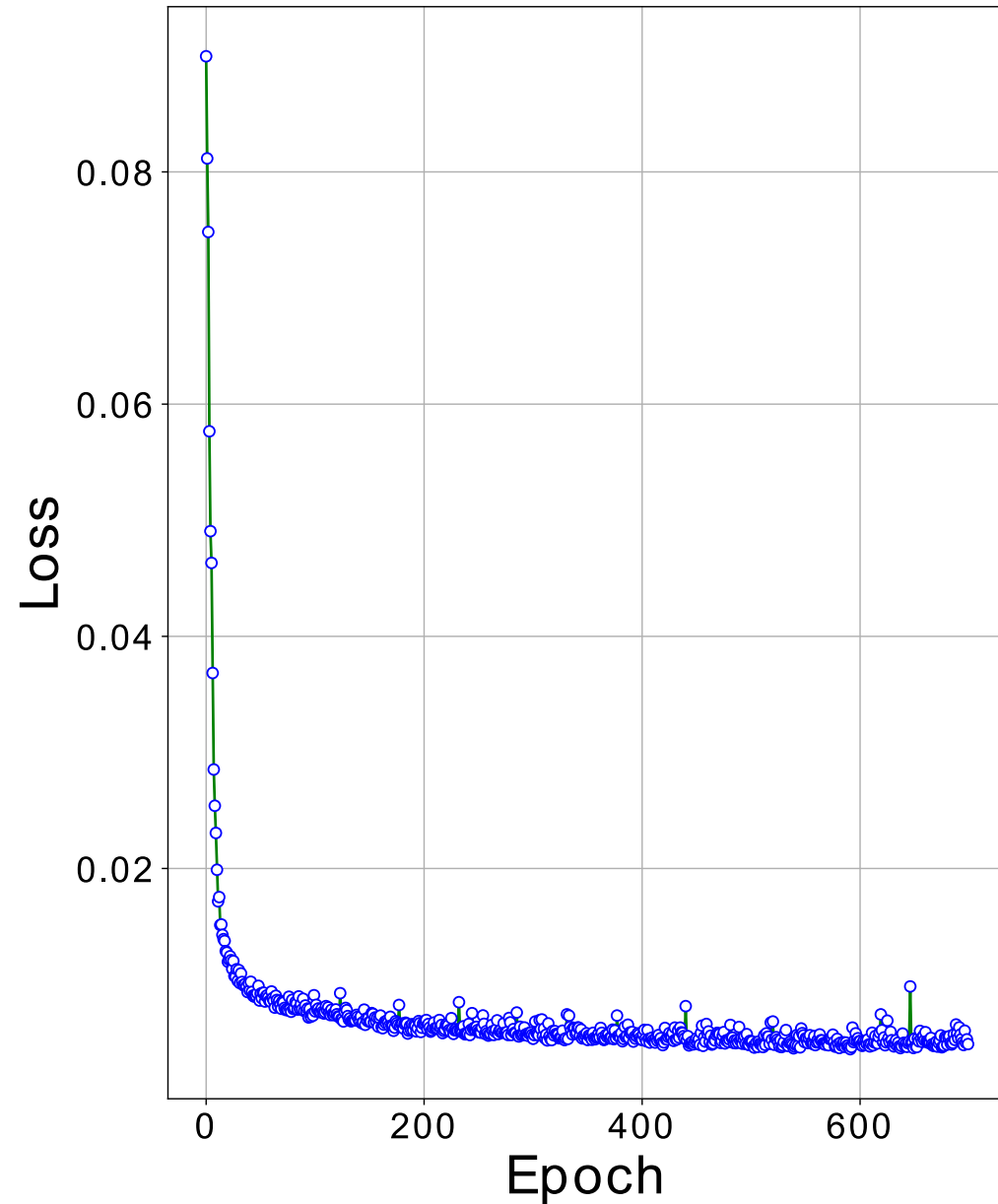
# MRLD-based Neural Network: MNN



# Experimental results (using MNIST)--The MNN and FNN training result in 100 epochs



# Experimental results (using MNIST)-- The MNN training result in 700 epochs



# Conclusions

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- Introduced the MRLD device which is applied the next-generation Edge AI devices.
- Analyzed the NN neuron's operation principle in MRLD
- Proposed a novel network structure MNN (MRLD-based Neural Network) to adapt the MRLD structure
- Performed a recognition training experiment using the MNIST dataset to confirm the effectiveness of the MNN.
- In our future work, we will analyze and design the method for image and data of any size that can be recognized in MNN in MRLD



Thank you for your listening