Doctoral Thesis Summary

Thesis Title:

Study on the High Reliability of Memory-based Programmable Logic Device

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Summary

Memory-based Programmable Logic Device (MPLD) is a new-type reconfigurable device that is under development for the edge computing device of IoT and AI applications [1]. MRLD is constructed by an array of MLUTs (multiple lookup tables), as shown in figure 1. The MLUTs consist of general SRAMs (asynchronous, synchronous), and are connected with neighbors by their address-inputs/data-outputs called the AD interconnects. In the MLUT block, the address inputs of the SRAMs are wrapped by an address transition detector (ATD) circuit to detect the address changes coming from the data outputs of its adjacent MLUTs at high speed.

The long-term reliability of MPLD is threatened by 1) the various production defects on the MLUTs array, and 2) the aging-caused delay degradation of time-critical circuit ATD embedded in the MLUT.

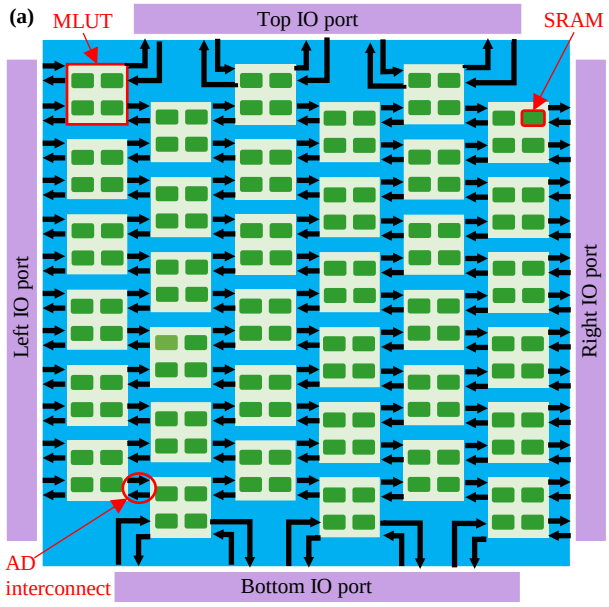
In the production of MPLD, the manufacturing defects existing at AD interconnect between MLUTs including short, bridge, or open would cause significant yield loss and reliability degradation. Since the address inputs of an MLUT come from the data outputs of its adjacent MLUTs, a defect at the AD interconnect would change the value of the address inputs of MLUTs and cause access error thus resulting in logic faults in the configuration operation mode.

When MPLD works in the field for a long term or under a severe environment, various aging phenomena such as the HCI (hot carrier injection) and BTI (bias temperature instability) [2][3] would threaten the long-term reliability [4] of MPLD. In each MLUT, the asynchronous SRAMs use the ATD circuit to detect the input address change to execute asynchronous operations. Since the ATD is extremely sensitive to the delay variation, aging phenomena would cause extra delay and increase the threshold voltage of the transistors in ATD then slow down the switching speed [5], which might cause false detection of the address change.

To guarantee the long-term reliability of the MPLD, this study proposed 1) the test approach to detect and identify the AD interconnect defects in the MLUTs array under the production phase, and 2) a reconfigurable delay monitor technique to detect the aging-induced delay of MLUTs in the field.

In our previous research [6][7], we proposed the test method to detect stuck-at and bridge interconnect faults in the MLUT array in fewer test configurations with high fault coverage. Identifying the fault location also plays an essential role in improving the manufacturing process and helps the user to void the use of a faulty MLUT block when the MPLD is put into practical use. Therefore, this study extends the previous test methods in [6][7] to address not only fault detection but also the fault diagnosis of MPLD [8]. As shown in figure 2, the proposed test method creates route maps in MPLD for the propagation of the interconnect fault by configuring the pre-designed test cubes into the MPLD, and excites fault by applying pre-generated external walking-zero/one vector to the external input ports of MPLD. Any interconnect faults can be identified by propagating the fault effect to the external output ports of MPLD.

The proposed delay monitor method configures a novel designed ring oscillator (RO) logic into MPLD, as shown in figure 3, to measure the aging-induced delay variations when the device is under practical use [9].



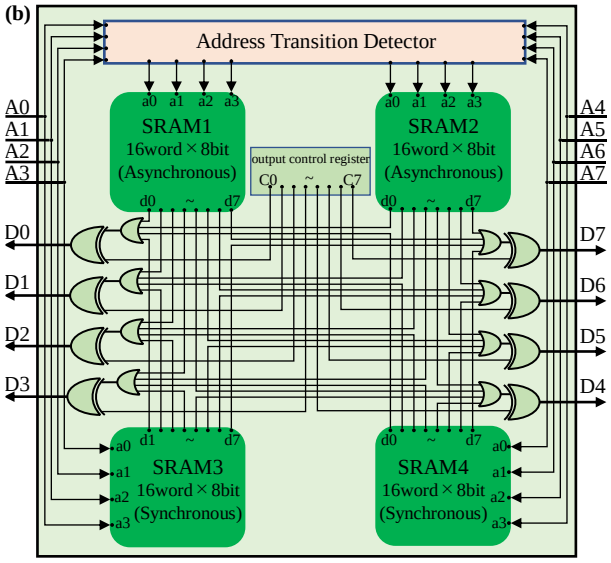


Figure 1 MPLD Architecture: (a) MPLD, (b) MLUT

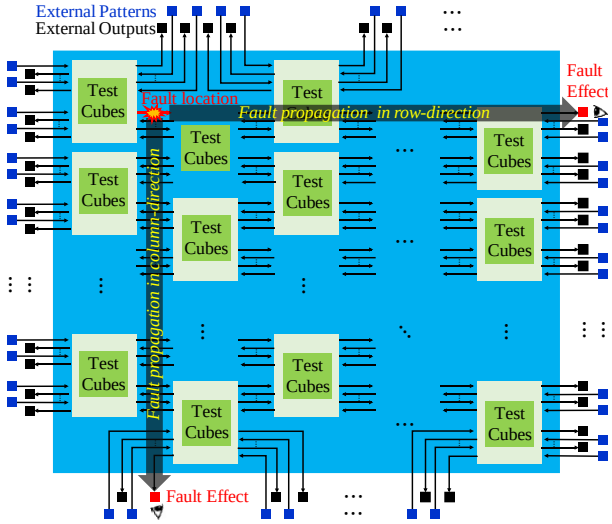


Figure 2 Test method

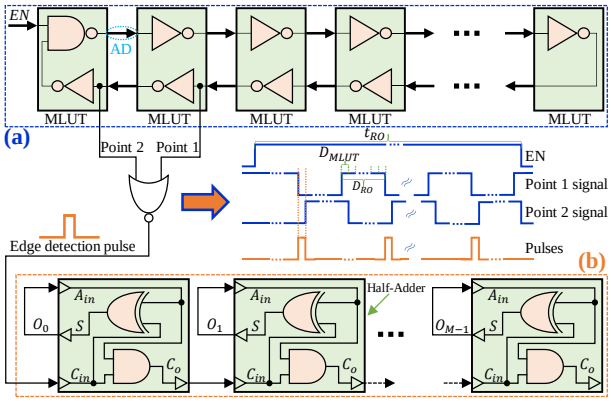


Figure 3 Delay measure method; (a) RO in MLUTs, (b) counter for RO.

References

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