

# ***ATS Doctoral Thesis Award***

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*Semi-Final of 2023 TTTC's E. J. McCluskey Doctoral Thesis Award*

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## **Study on the High Reliability of MPLD (Memory-based Programmable Logic Device)**

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# Outline

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## **1. What's MPLD**

- Architecture, Working principle

## **2. Reliability Issues of MPLD**

- Manufacturing and Aging defects

## **3. Manufacturing Defect Testing**

- Detection & Localization for Interconnect faults

## **4. Aging Defect Testing**

- LUT-based Delay-Monitoring

## **5. Conclusions**

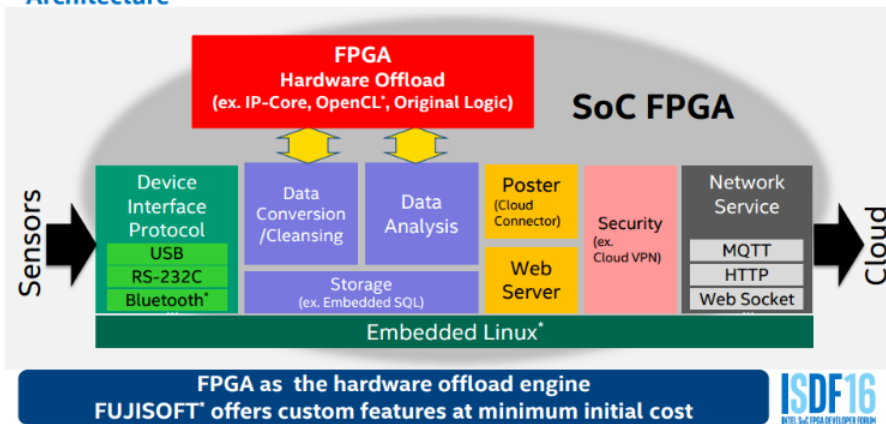
# Demand for Reconfigurable Devices

Reconfigurable devices (e.g.: FPGAs) are gaining increased attention in IoT, Automotive, and AI field

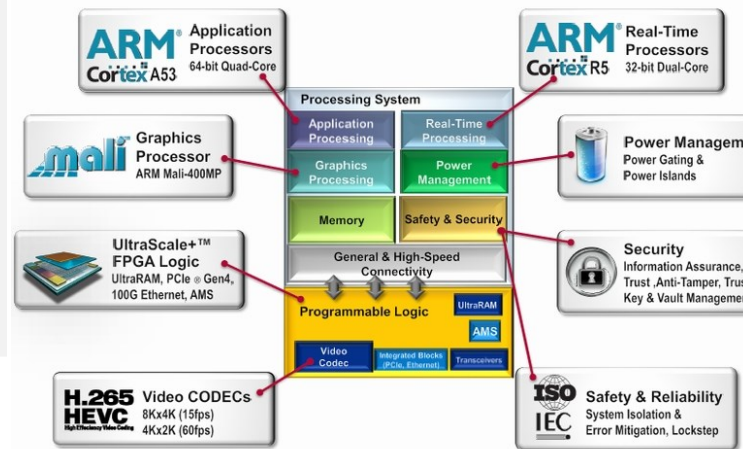
- ★ Flexibility and scalability
- ★ High performance (parallel computing)
- ★ Better time to market
- ★ Low design cost (shortening of development cycle)

## IoT Edge Computing

Edge Computing GW and IoT Solution: Architecture

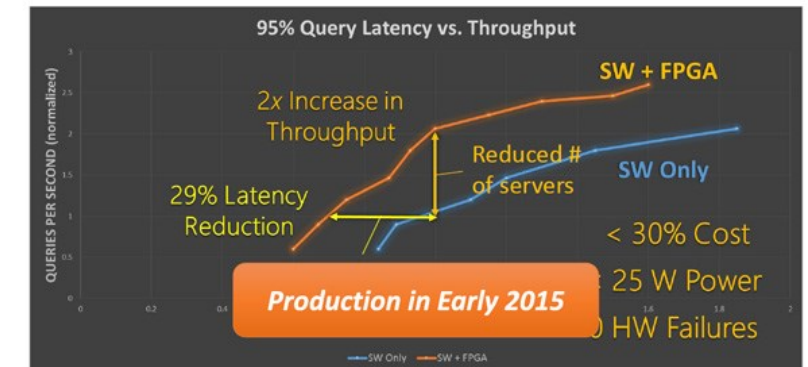


## Xilinx's Automotive Solution: Zynq UltraScale+ MPSoC



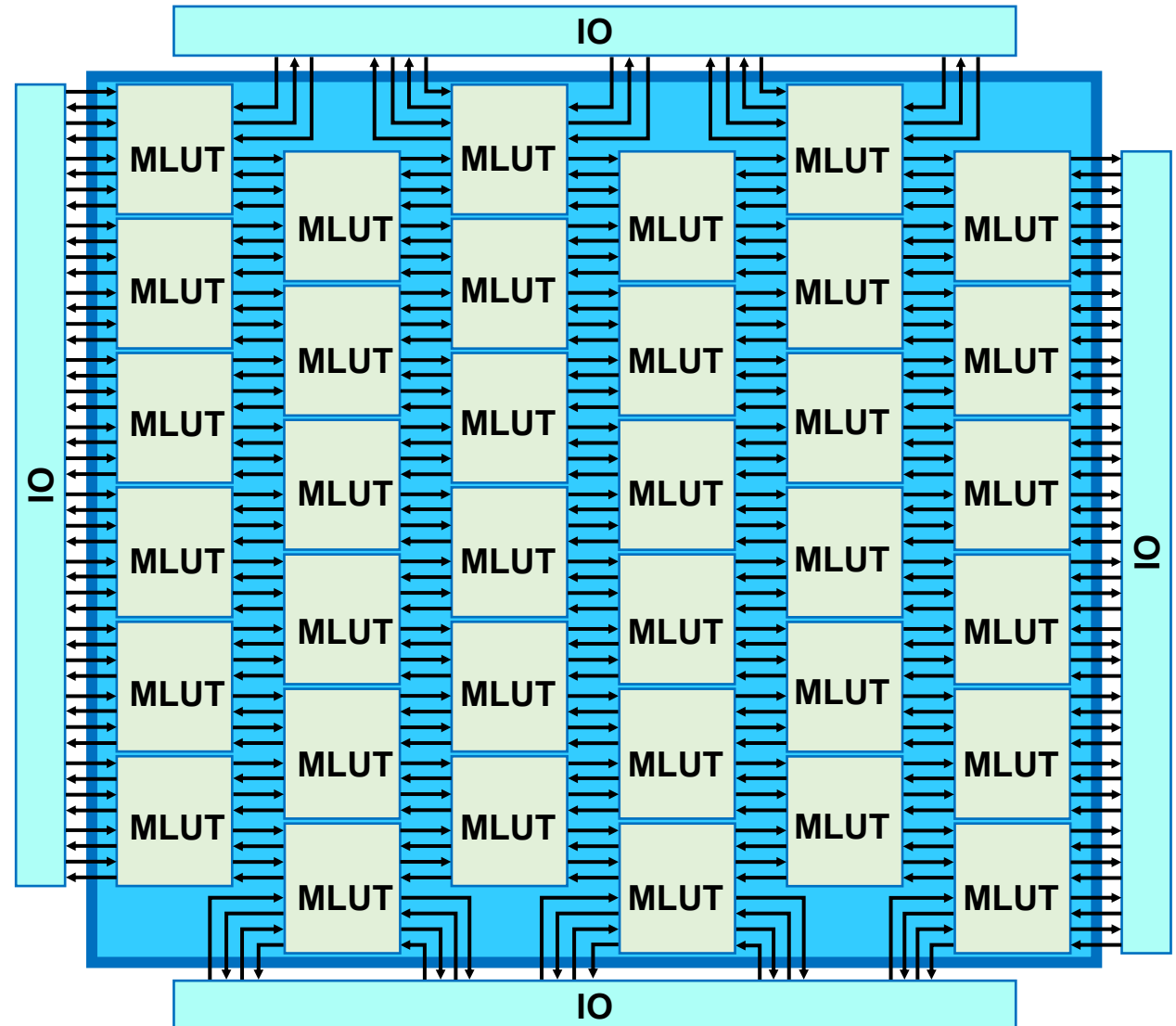
## Bing Intelligent Search Engine FPGA accelerator

Accelerating Large-Scale Services – Bing Search  
1,632 Servers with FPGAs Running Bing Page Ranking Service (~30,000 lines of C++)



# 1. What's MPLD ~ Architecture~

- A new type reconfigurable device
- Memory-based Programmable Logic Device (MPLD)
- constructed only by **MLUT** (Multiple Look-Up-Table) array in a special interconnect structure.

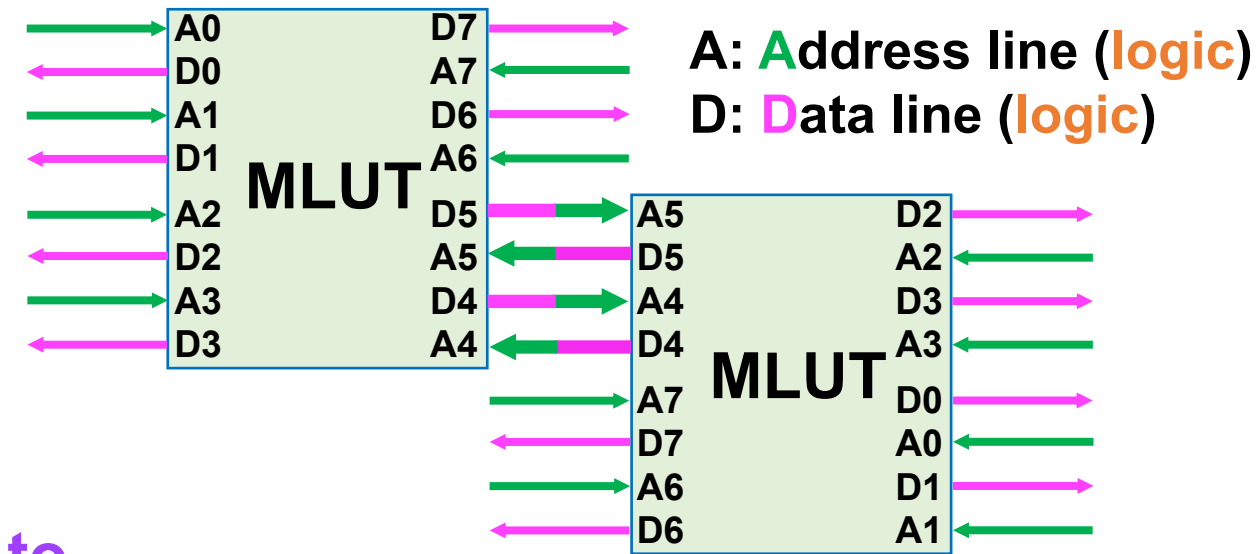


# 1. What's MPLD ~ Architecture~

## --- AD-pair Interconnect Structure

- Address lines and Data lines alternately connect with others

- Logic data output of a MLUT connects to address input of its neighbor MLUTs

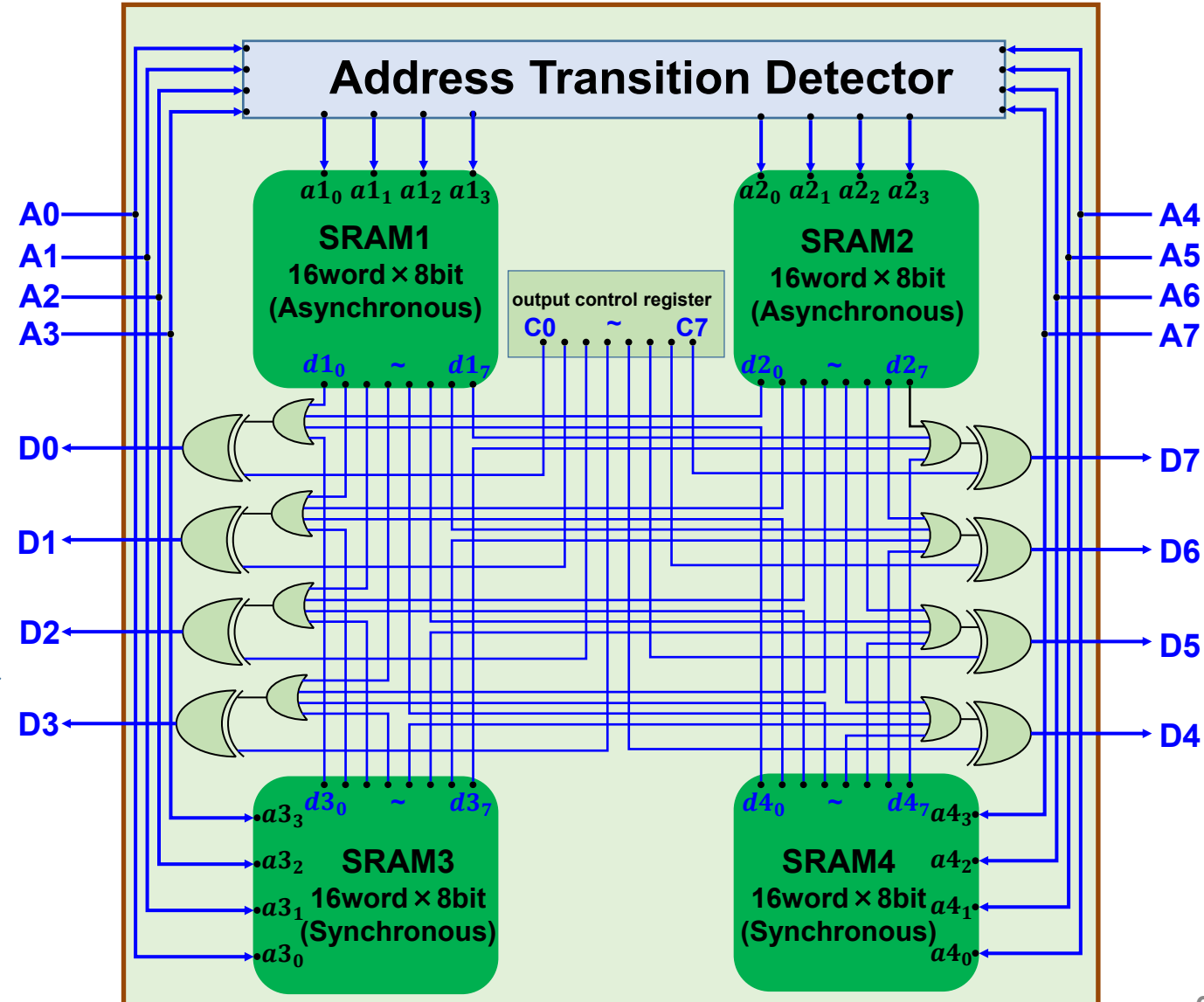
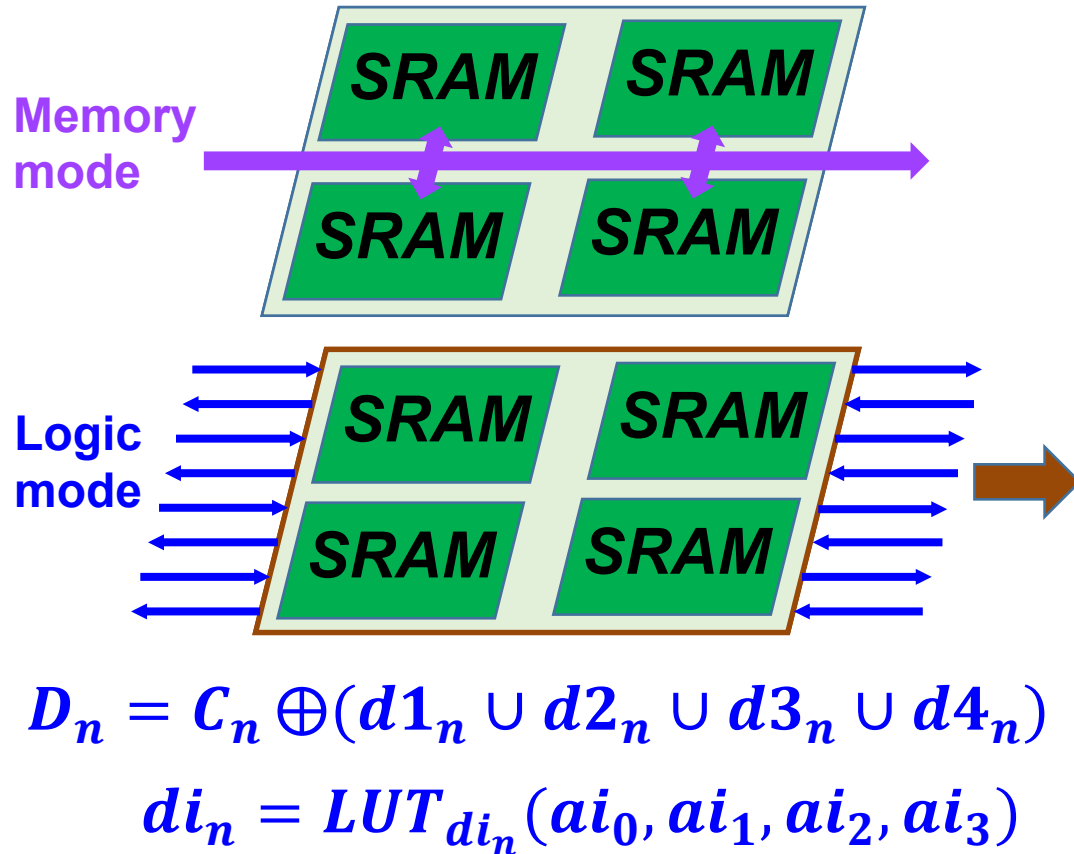


Interconnect Structure  
(AD-pair Interconnect)

# 1. What's MPLD ~ Architecture ~

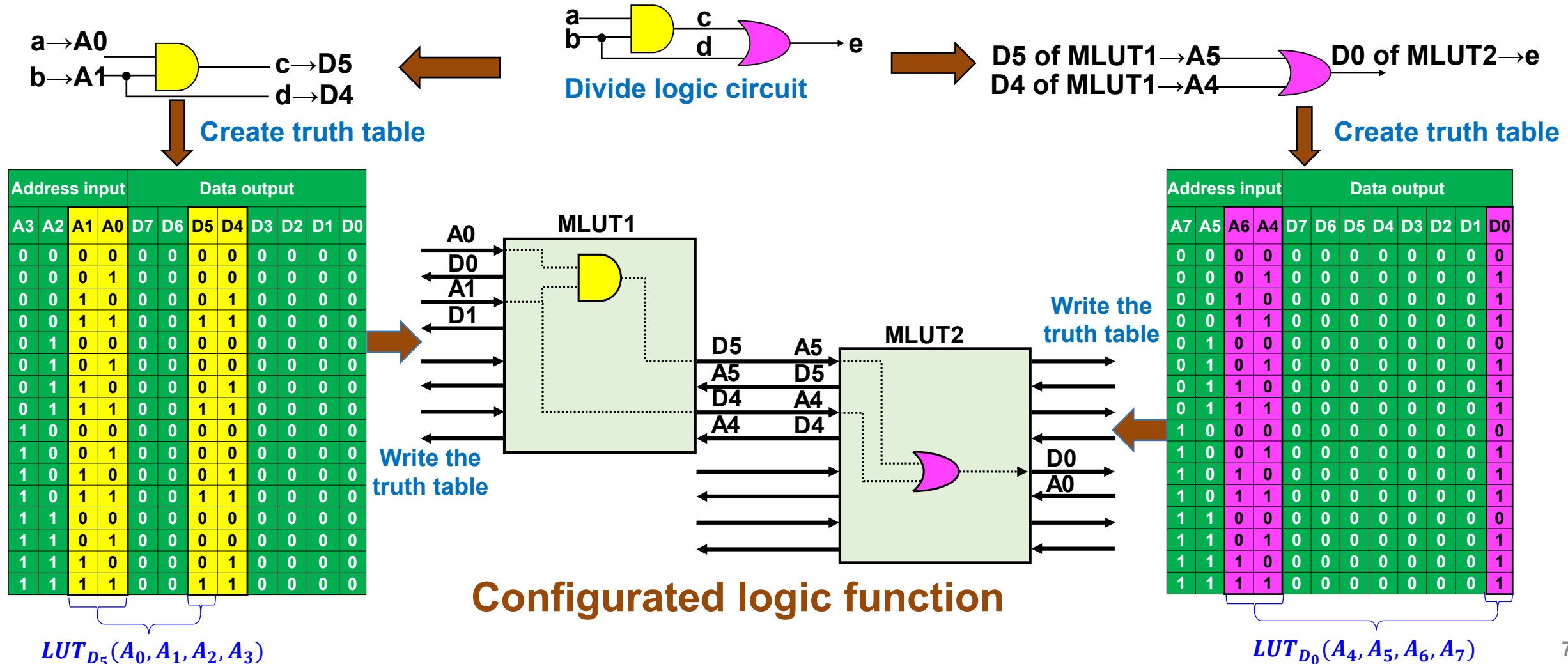
## --- MLUT structure

- basic reconfigurable elements
- multiple SRAM blocks
- memory mode or logic mode
- each SRAM works as LUTs



# 1. What's MPLD ~ Working principle ~

- Configure the **logic function** by writing the **truth table** of the logic circuit (including wiring logic) into the **SRAM of MLUT**



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- Detection & Localization for Interconnect faults

## 4. Aging Defect Testing

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## 5. Conclusions



# 3. Reliability Issue in MPLD ~ Manufacturing ~

## Factors:

- Manufacturing Phase

- Defect in MLUT (SRAM)

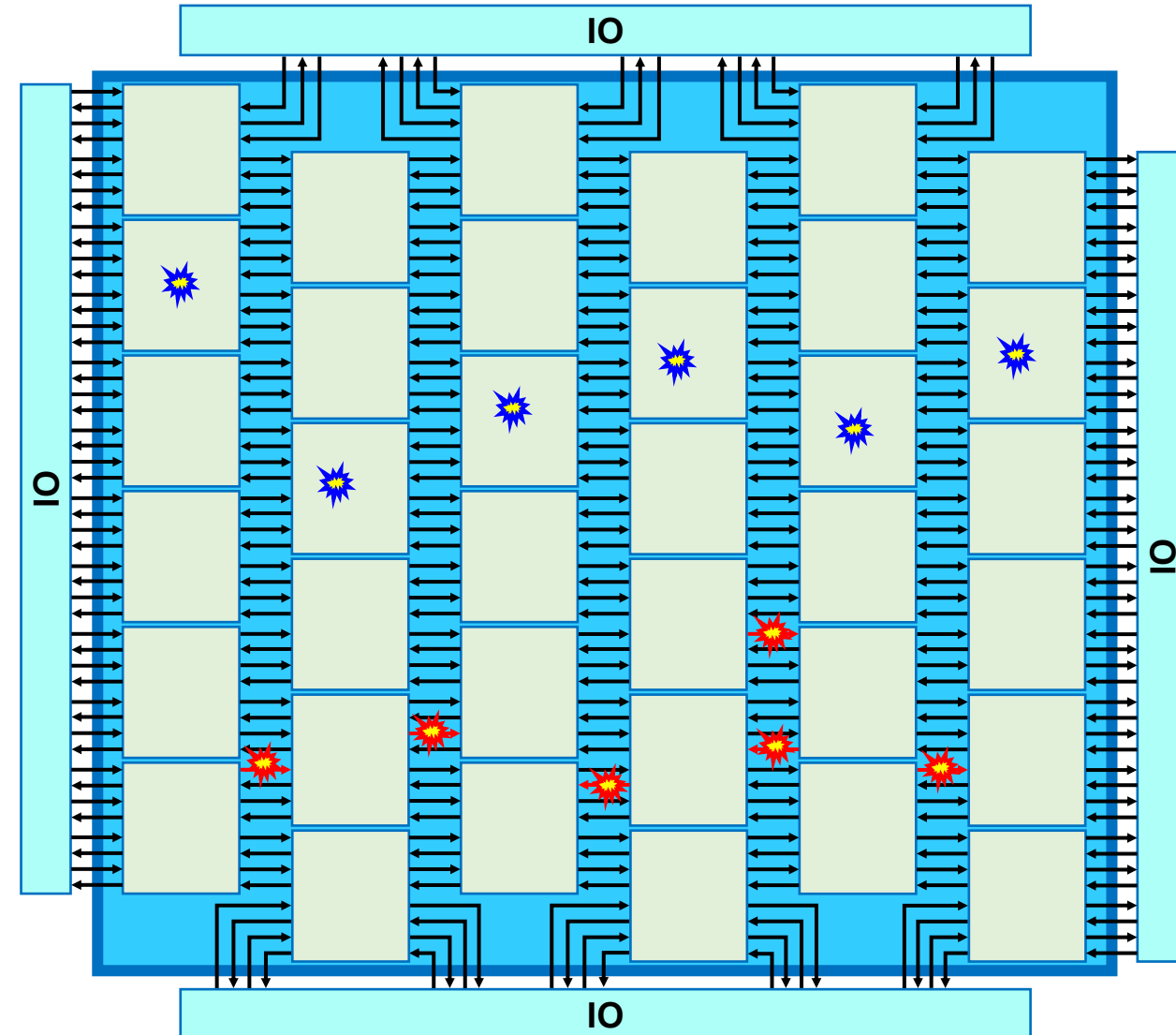
- ✓ Conventional Memory testing

- Defect between MLUTs

- Interconnect defect on Address and Data lines

(short, bridge, open, etc.)

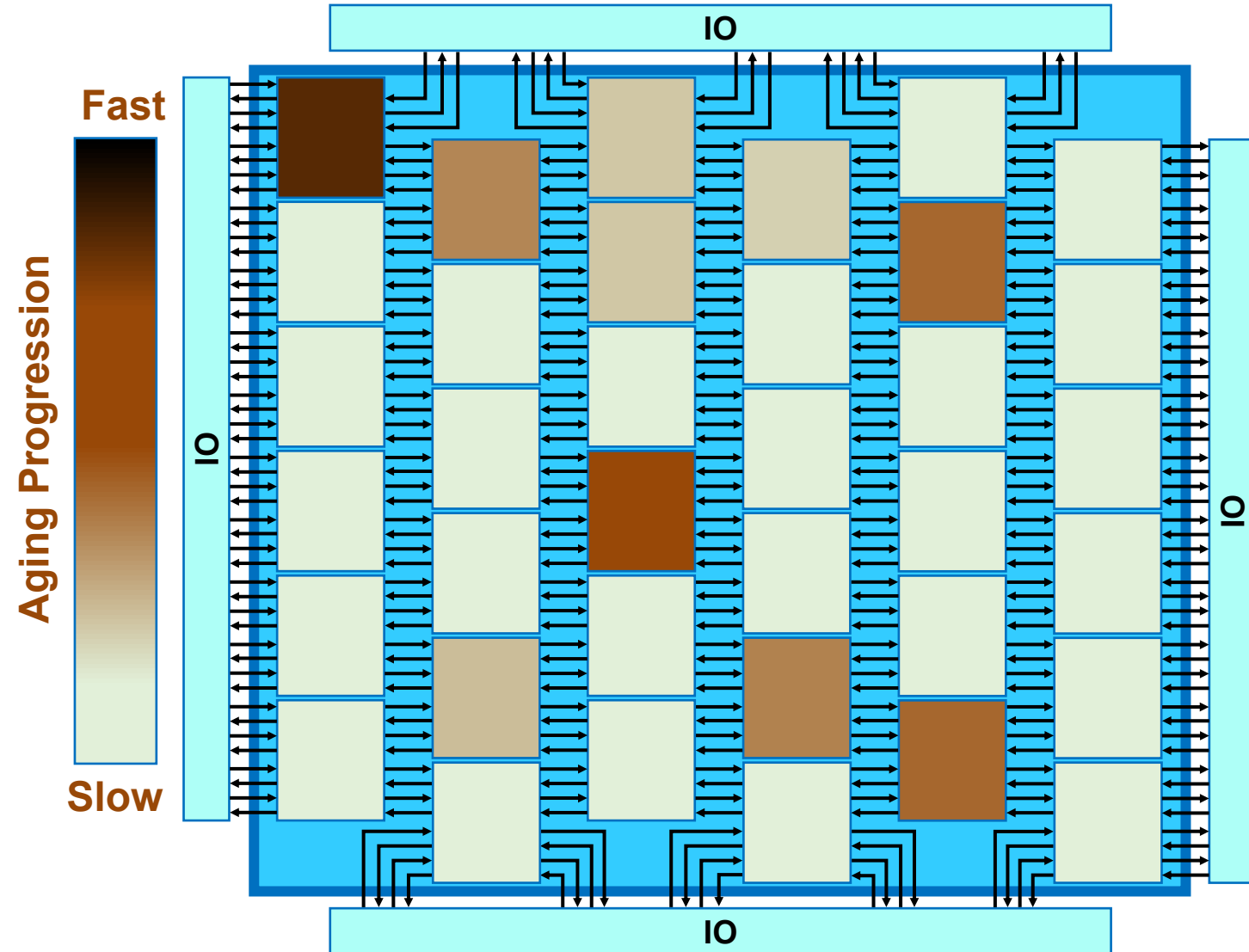
yield loss and reliability degradation



# 3. Reliability Issue in MPLD ~ Aging ~

## Factors:

- Application phase (in field)
  - Aging in memory elements
    - HCI, BTI, etc.
    - Aging-induced delay
  - Different aging progress
    - system failure
    - logic circuit performance (e.g.: sudden system down/reset)



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## **3. Manufacturing Defect Testing**

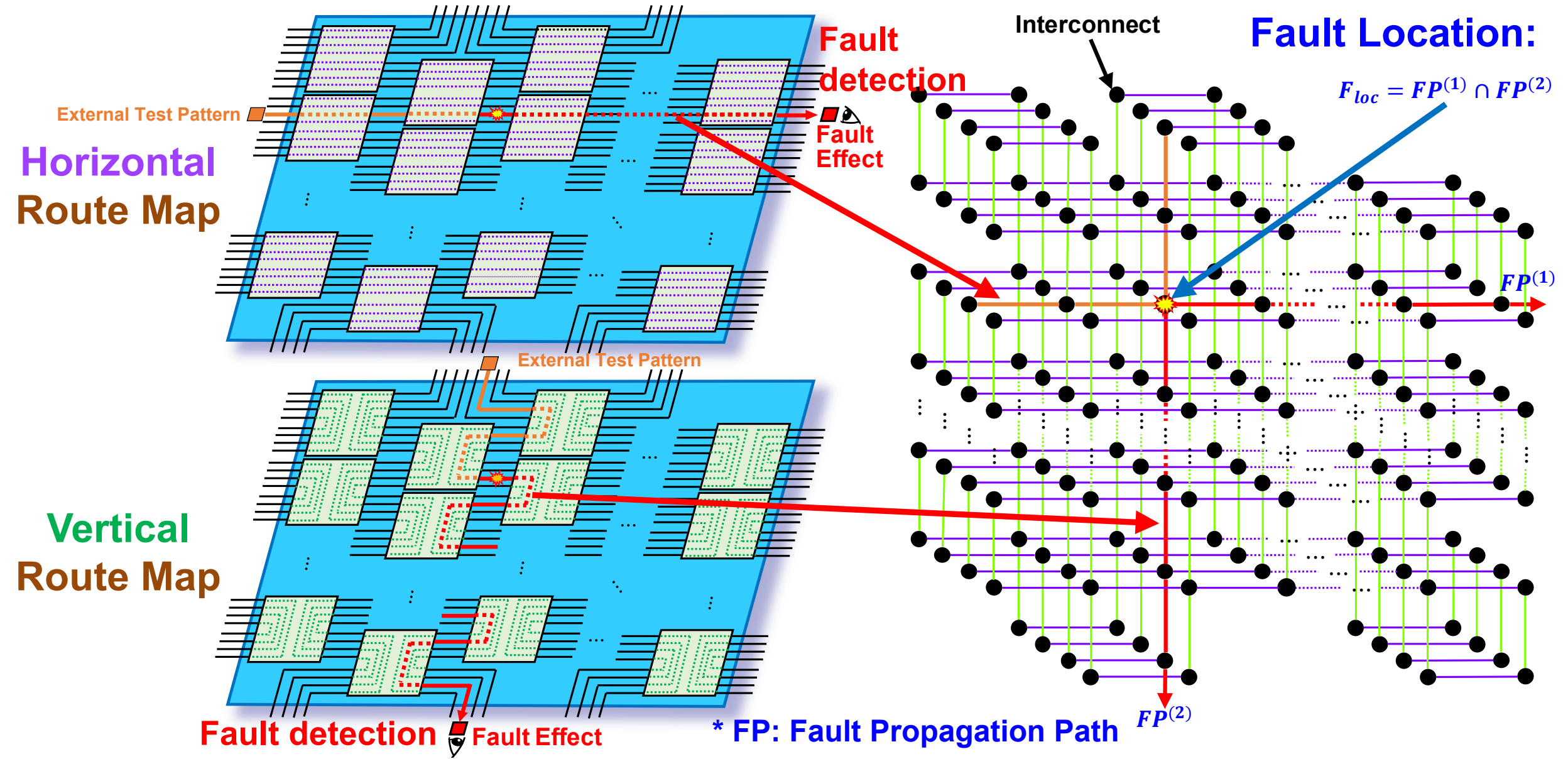
- **Detection & Localization for Interconnect faults**

## 4. Aging Defect Testing

- LUT-based Delay-Monitoring

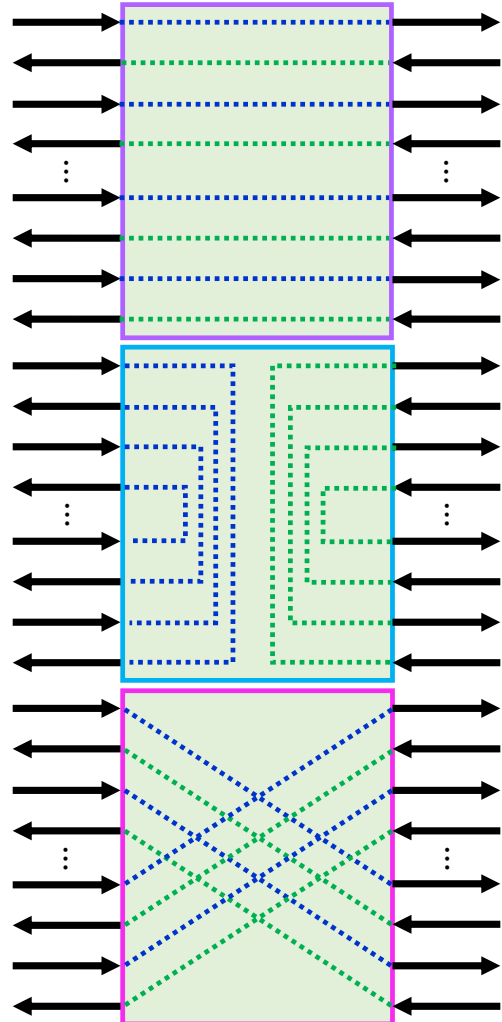
## 5. Conclusions

# 4. Manufacturing Defect Testing ~ Basic Idea ~



# 4. Manufacturing Defect Testing ~ Test Cube ~

- **Route Map (rm)** is created by **Test Cube (TC)** stored into SRAM of MLUTs
- **truth table1** route **low-order address**; **truth table2** route **high-order address**



Route Maps	Test Cubes		
$rm_1$ : horizontal route map	$TC^{(1)}$	truth table1	$D_{m-1:m/2} = A_{0:m/2-1}$
			$D_{m/2-1:0} = all-0$
		truth table2	$D_{m-1:m/2} = all-0$
			$D_{m/2-1:0} = A_{m/2:m-1}$
$rm_2$ : vertical route map	$TC^{(2)}$	truth table1	$D_{m-1:m/2} = all-0$
			$D_{m/2-1:0} = A_{0:m/2-1}$
		truth table2	$D_{m-1:m/2} = A_{m/2:m-1}$
			$D_{m/2-1:0} = all-0$
$rm_3$ : diagonal route map	$TC^{(3)}$	truth table1	$D_{m-1:m/2} = A_{m/4:m/2-1} \cdot A_{0:m/4-1}$
			$D_{m/2-1:0} = all-0$
		truth table2	$D_{m-1:m/2} = all-0$
			$D_{m/2-1:0} = A_{3m/4:m-1} \cdot A_{m/2:3m/4-1}$

# 4. Manufacturing Defect Testing ~ External Test Pattern~

- **External Test Patterns** for exciting the *stuck-at* and *bridge* interconnect faults by applying *walking-zero/one vectors*.

Fault Types	External Test Patterns (walking-zero/one vectors)
<i>stuck-at-1</i>	<i>all-zero vector: 0...0</i>
<i>stuck-at-0</i>	<i>all-one vector: 1...1</i>
<i>AND-bridge</i>	<i>shift one-cold vector: ...101...</i>
<i>OR-bridge</i>	<i>shift one-hot vector: ...010...</i>

# 4. Manufacturing Defect Testing ~ Testing Procedure~

*Definitions:*

- $N_{rm}$ : number of route maps.
- $rm_i$ : route map  $i$ ;  $i \in [1, N_{rm}]$ .
- $TC^{(i)}$ : test cubes creating  $rm_i$ .
- $N_{FE}^{(i)}$ : number of observed fault effects under  $rm_i$ .
- $FP_k^{(i)}$ : fault propagation path  $k$  obtained under  $rm_i$ ;  $k \in [1, N_{FE}^{(i)}]$ .
- $FP^{(i)}$ : fault propagation path set under  $rm_i$ .
- $F_{loc}$ : fault location.

*Process:*

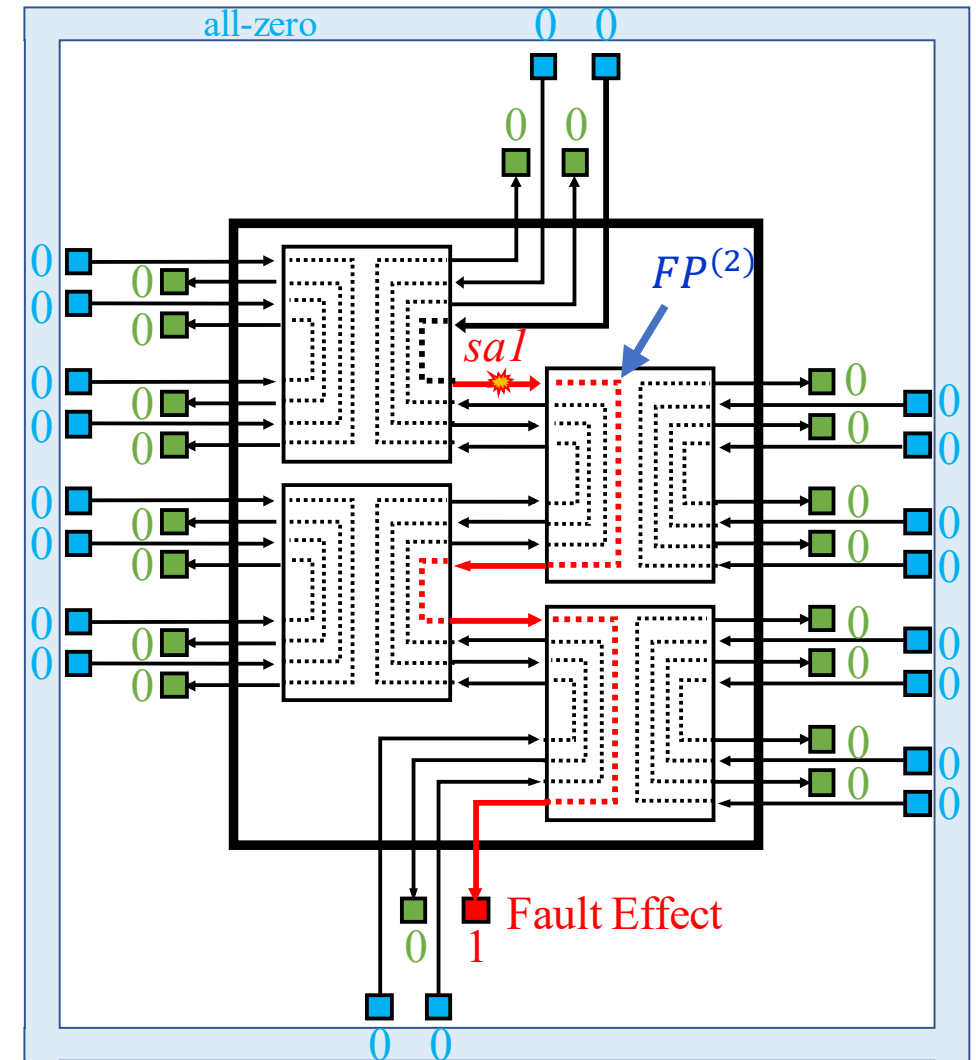
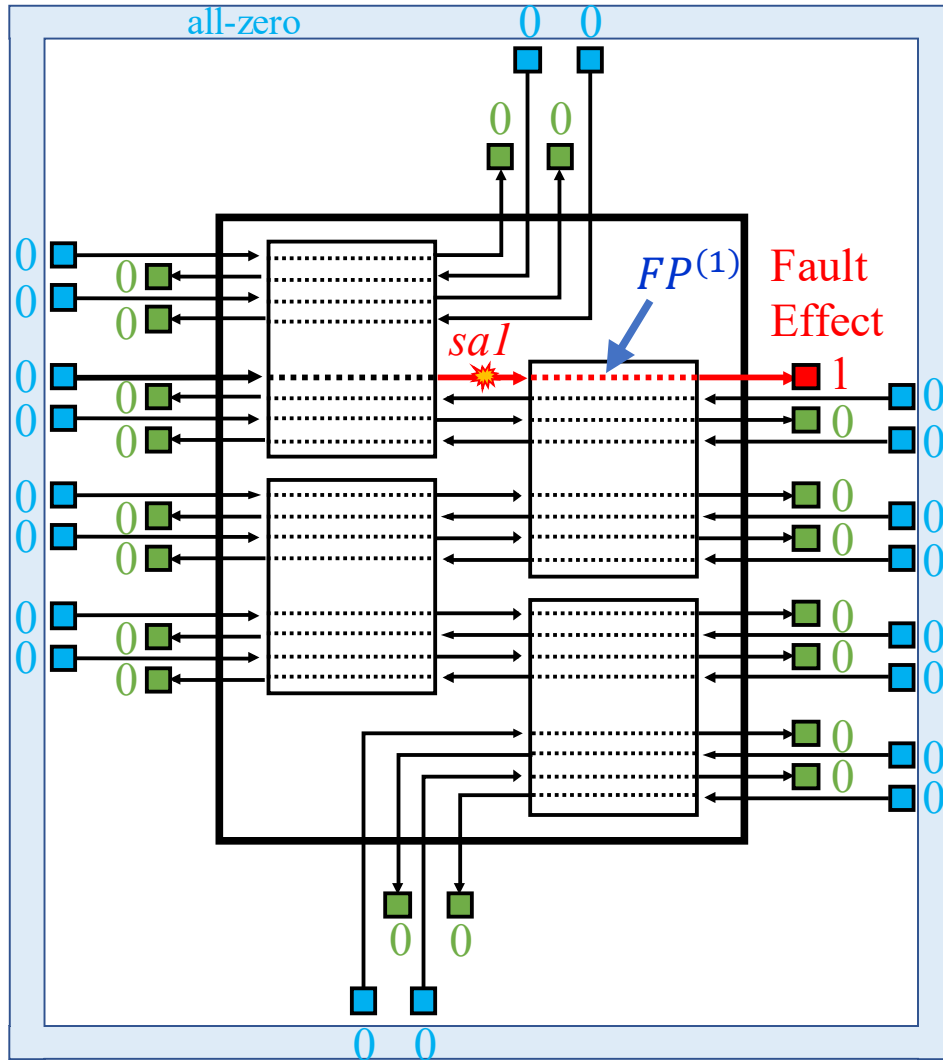
(1) Test under  $rm_i$  for  $i \in [1, N_{rm}]$ :

- (a) Configure  $TC^{(i)}$  into each MLUT to create  $rm_i$ .
- (b) Apply external test patterns to the input ports of MPLD.
- (c) Observe fault effects. If  $N_{FE}^{(1)}=0$ , end testing (fault-free).
- (d) Obtain the fault propagation path set:  $FP^{(i)} = \bigcup_{k=1}^{N_{FE}^{(i)}} FP_k^{(i)}$ .

(2) Identify fault location:  $F_{loc} = \bigcap_{i=1}^{N_{rm}} FP^{(i)}$ .

# 4. Manufacturing Defect Testing ~ example ~

## --- testing stuck-at-1 fault

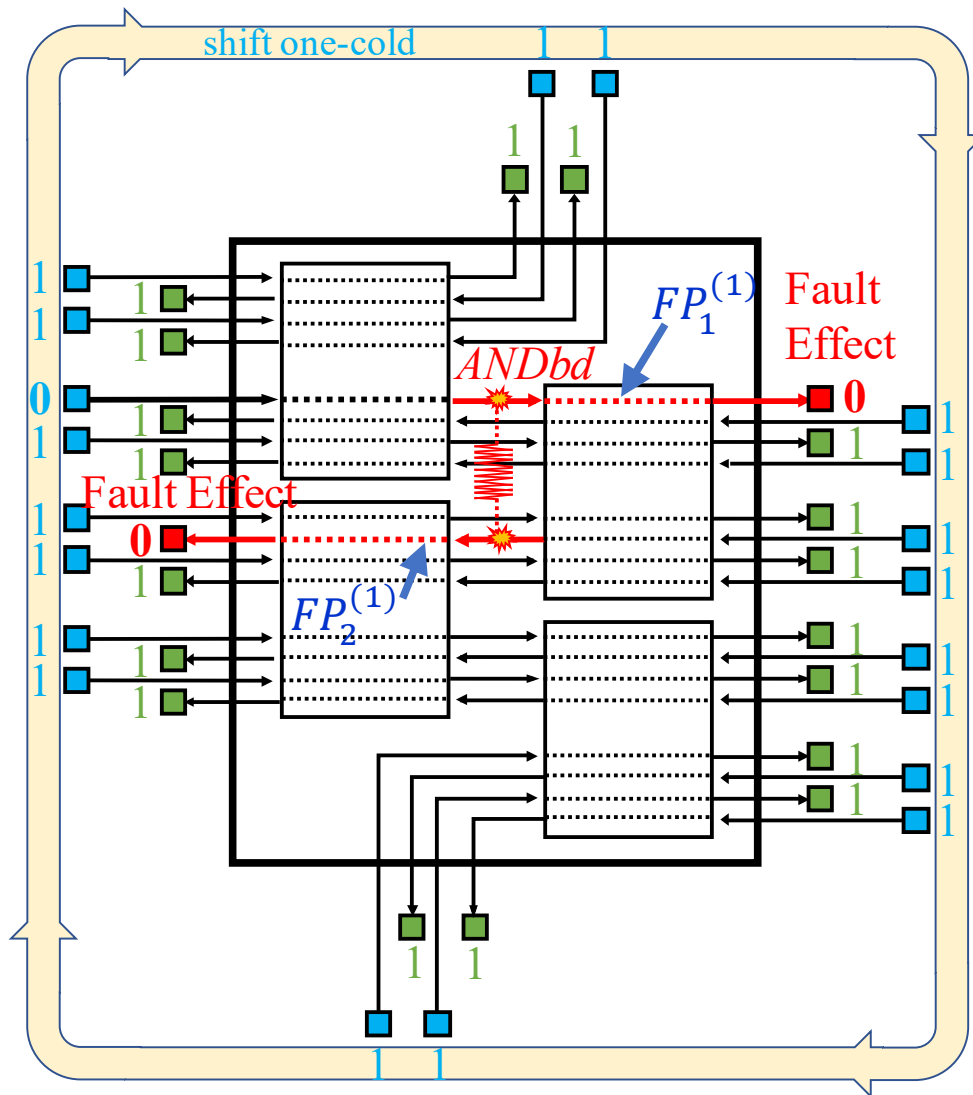


$$F_{loc} = FP^{(1)} \cap FP^{(2)}$$

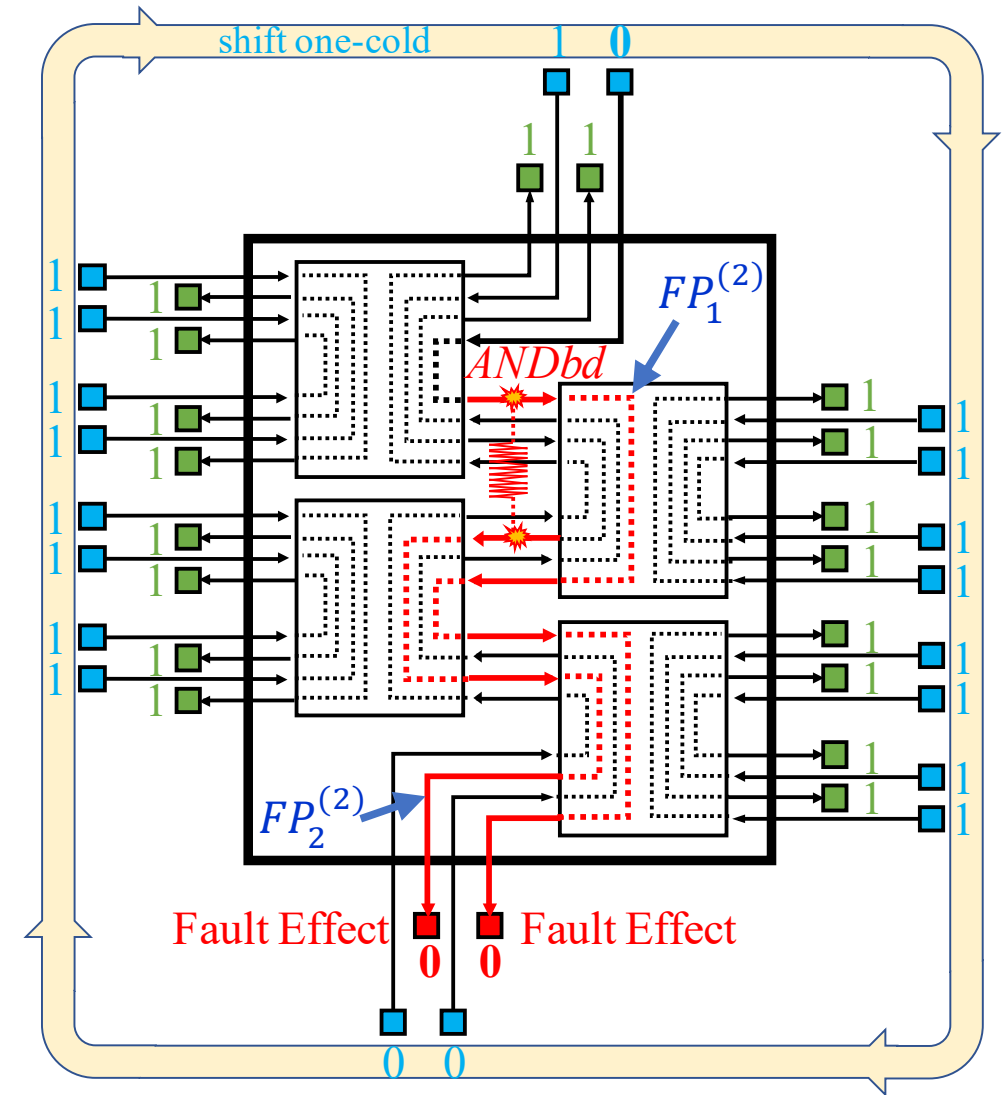


# 4. Manufacturing Defect Testing ~ example ~

## --- AND-bridge fault



$$F_{loc} = FP^{(1)} \cap FP^{(2)}$$



$$(FP^{(1)} = \bigcup_{k=1}^2 FP_k^{(1)}, \quad FP^{(2)} = \bigcup_{k=1}^2 FP_k^{(2)})$$

# 4. Manufacturing Defect Testing ~ simulation ~

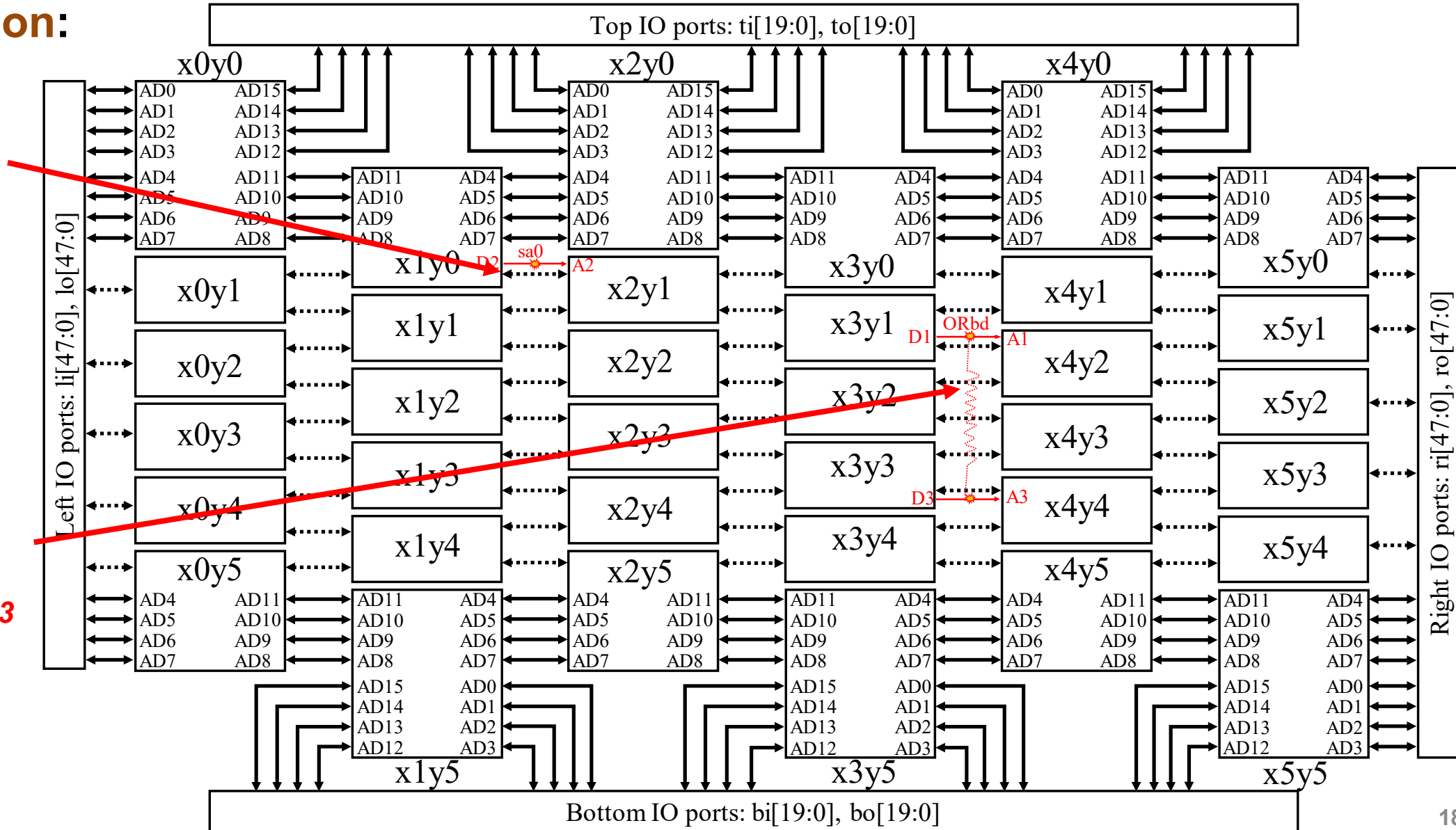
## ● fault injection:

stuck-at-0  
at

$x_2y_1A_2$

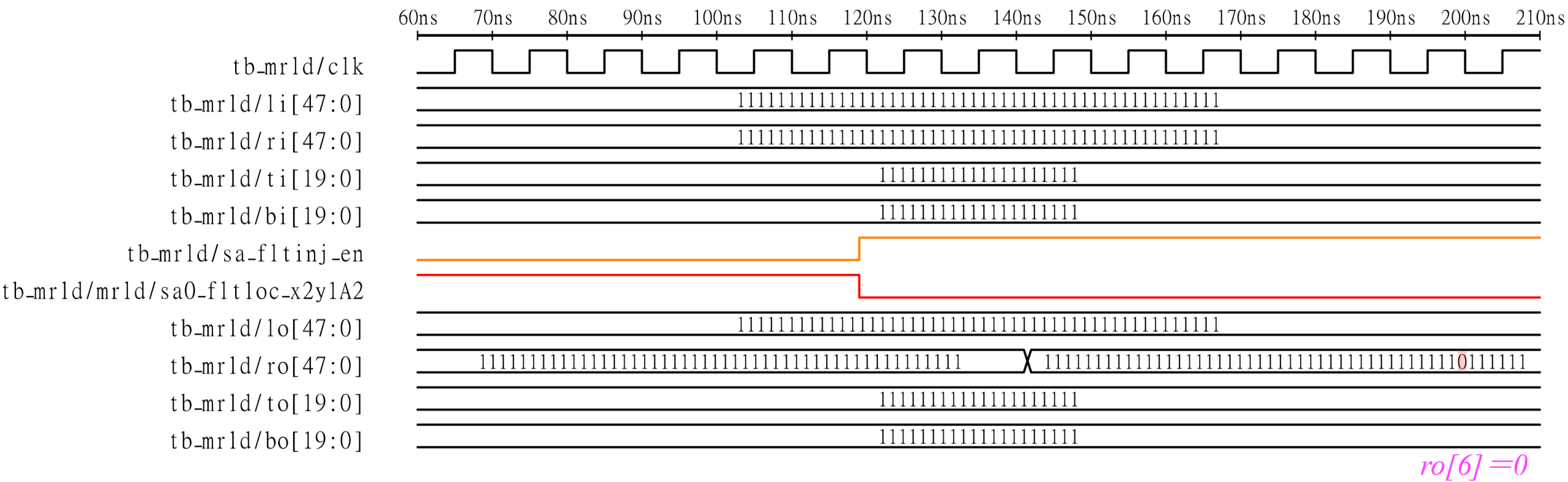
OR-bridge  
between

$x_4y_2A_1$ ,  $x_4y_4A_3$



# 4. Manufacturing Defect Testing ~ simulation ~ --- stuck-at-0 fault

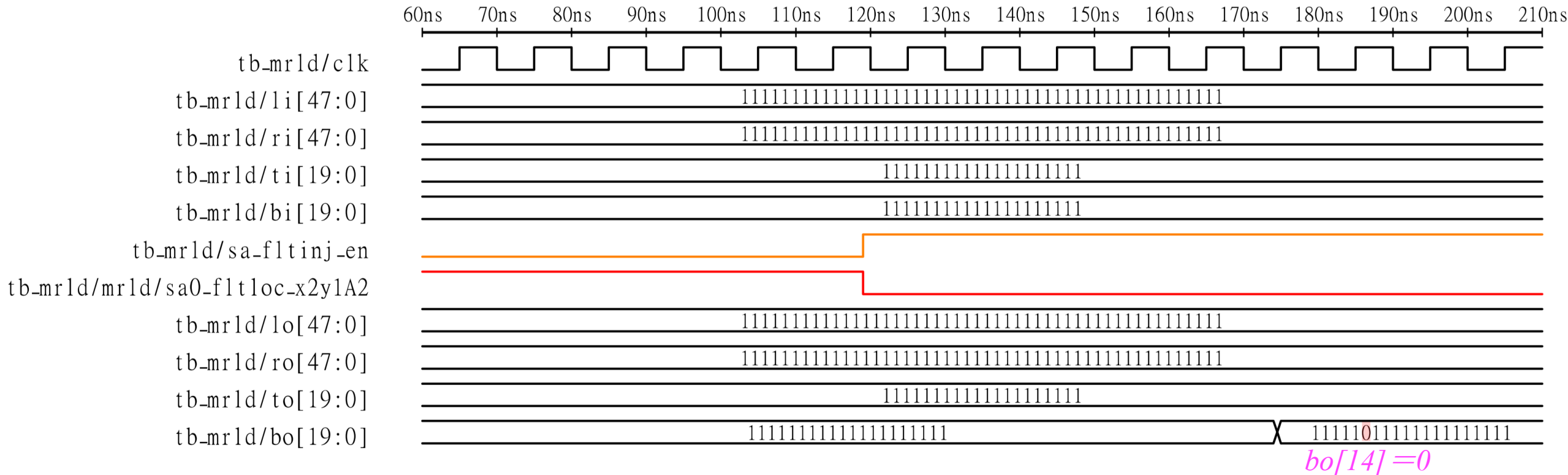
## Testing under Horizontal Route Map



$$FP^{(1)} = \{li[10] \rightarrow x_1y_0A_{13} \rightarrow \mathbf{x_2y_1A_2} \rightarrow x_3y_0A_{13} \rightarrow x_4y_1A_2 \rightarrow x_5y_0A_{13} \rightarrow \mathbf{ro[6]}\},$$

# 4. Manufacturing Defect Testing ~ simulation ~ --- stuck-at-0 fault

## Testing under Vertical Route Map

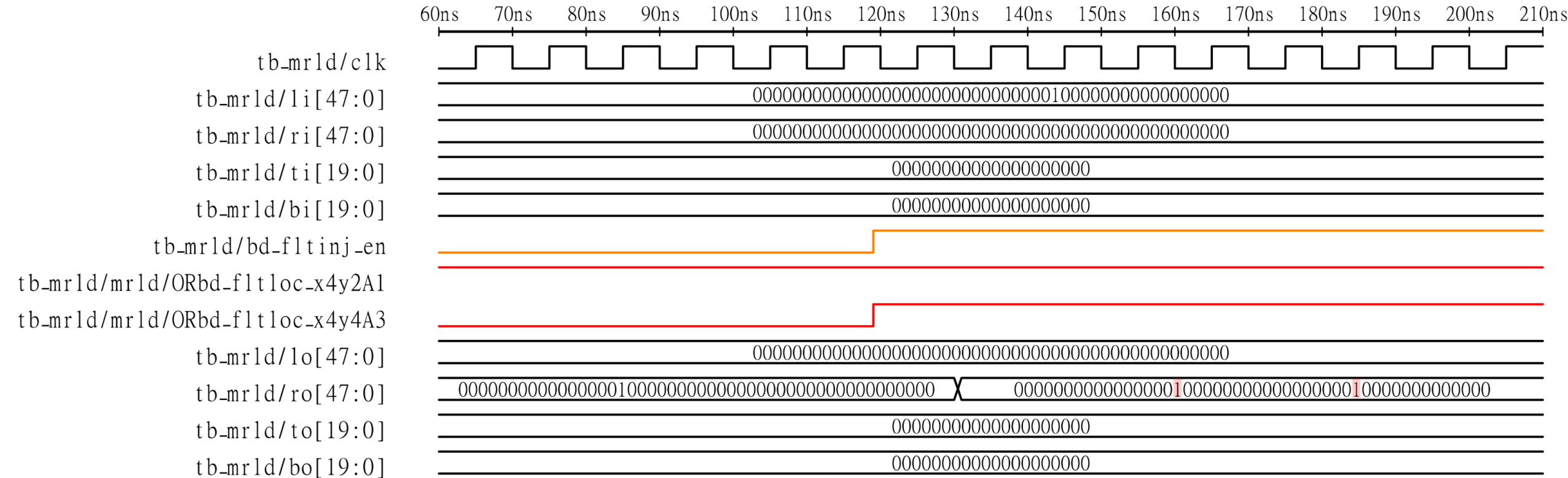


$$FP^{(2)} = \{ti[14] \rightarrow x_1y_0A_5 \rightarrow \mathbf{x_2y_1A_2} \rightarrow x_1y_1A_5 \rightarrow x_2y_2A_2 \rightarrow x_1y_2A_5 \rightarrow x_2y_3A_2 \rightarrow x_1y_3A_5 \rightarrow x_2y_4A_2 \rightarrow x_1y_4A_5 \rightarrow x_2y_5A_2 \rightarrow x_1y_5A_5 \rightarrow \mathbf{bo[14]}\}$$

$$F_{loc} = \bigcap_{i=1}^2 FP^{(i)} = FP^{(1)} \cap FP^{(2)} = \mathbf{x_2y_1A_2}$$

# 4. Manufacturing Defect Testing ~ simulation ~ --- OR-bridge fault

## Testing under Horizontal Route Map



$ro[13] = 1$

$ro[31] = 1$

$$FP_1^{(1)} = \{li[17] \rightarrow x_1y_1A_{14} \rightarrow x_2y_2A_{14} \rightarrow x_3y_1A_{14} \rightarrow \mathbf{x_4y_2A_1} \rightarrow x_5y_1A_{14} \rightarrow \mathbf{ro[13]}\}$$

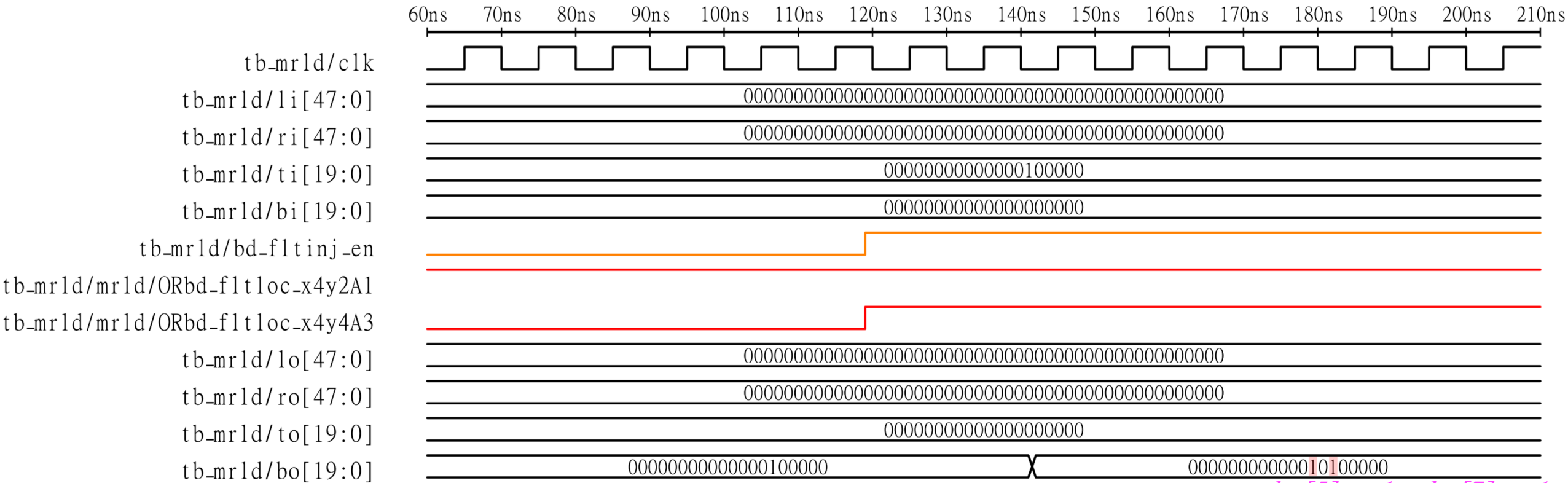
$$FP_2^{(1)} = \{li[35] \rightarrow x_1y_3A_{12} \rightarrow x_2y_4A_3 \rightarrow x_3y_3A_{12} \rightarrow \mathbf{x_4y_4A_3} \rightarrow x_5y_3A_{12} \rightarrow \mathbf{ro[31]}\}$$

$$FP^{(1)} = \bigcup_{k=1}^2 FP_k^{(1)} = FP_1^{(1)} \cup FP_2^{(1)}$$

# 4. Manufacturing Defect Testing ~ simulation ~

## --- OR-bridge fault

### Testing under Vertical Route Map



$bo[5] = 1$   $bo[7] = 1$

$$FP_1^{(2)} = \{ti[5] \rightarrow x_3y_0A_6 \rightarrow x_4y_1A_1 \rightarrow x_3y_1A_6 \rightarrow \mathbf{x_4y_2A_1} \rightarrow x_3y_2A_6 \rightarrow x_4y_3A_1 \rightarrow x_3y_3A_6 \rightarrow x_4y_4A_1 \rightarrow x_3y_4A_6 \rightarrow x_4y_5A_1 \rightarrow x_3y_5A_6 \rightarrow \mathbf{bo[5]}\}$$

$$FP_2^{(2)} = \{ti[7] \rightarrow x_3y_0A_4 \rightarrow x_4y_1A_3 \rightarrow x_3y_1A_4 \rightarrow x_4y_2A_3 \rightarrow x_3y_2A_4 \rightarrow x_4y_3A_3 \rightarrow x_3y_3A_4 \rightarrow \mathbf{x_4y_4A_3} \rightarrow x_3y_4A_4 \rightarrow x_4y_5A_3 \rightarrow x_3y_5A_4 \rightarrow \mathbf{bo[7]}\}$$

$$FP^{(2)} = \bigcup_{k=1}^2 FP_k^{(2)} = FP_1^{(2)} \cup FP_2^{(2)}$$

$$F_{loc} = \bigcap_{i=1}^2 FP^{(i)} = FP^{(1)} \cap FP^{(2)} = \{\mathbf{x_4y_2A_1}, \mathbf{x_4y_4A_3}\}$$

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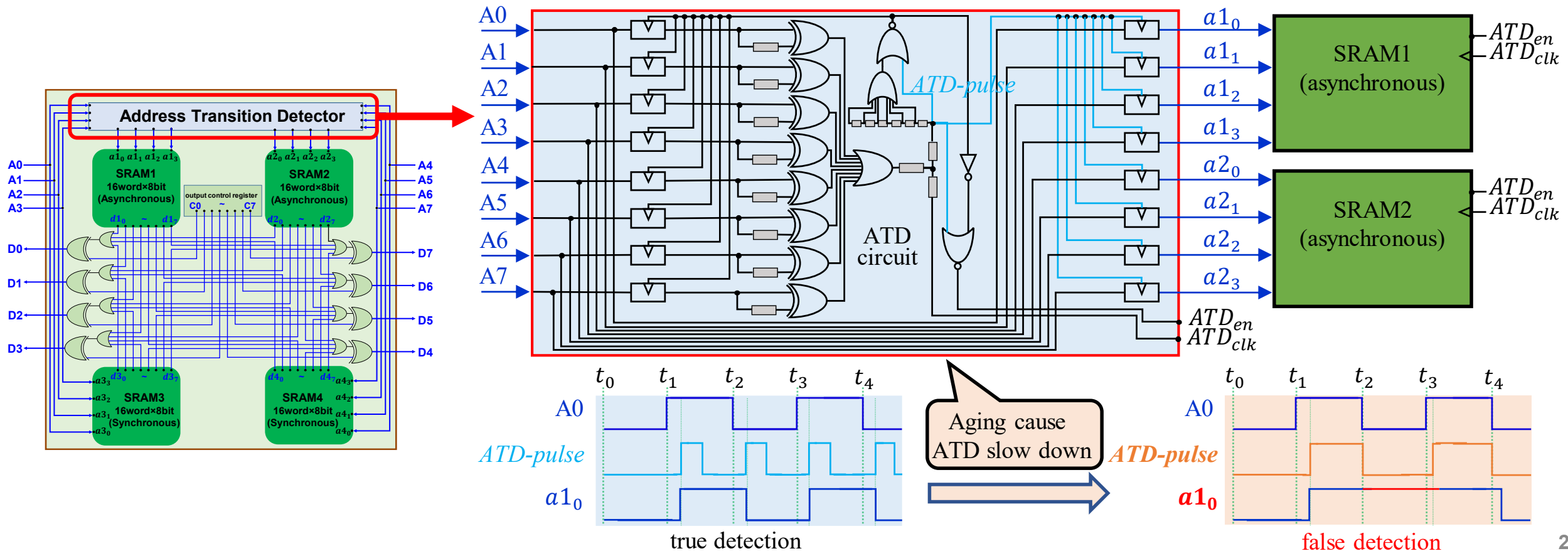
## **4. Aging Defect Testing**

- **LUT-based Delay-Monitoring**

## 5. Conclusions

# 4. Aging Defect Testing ~ ATD Delay~

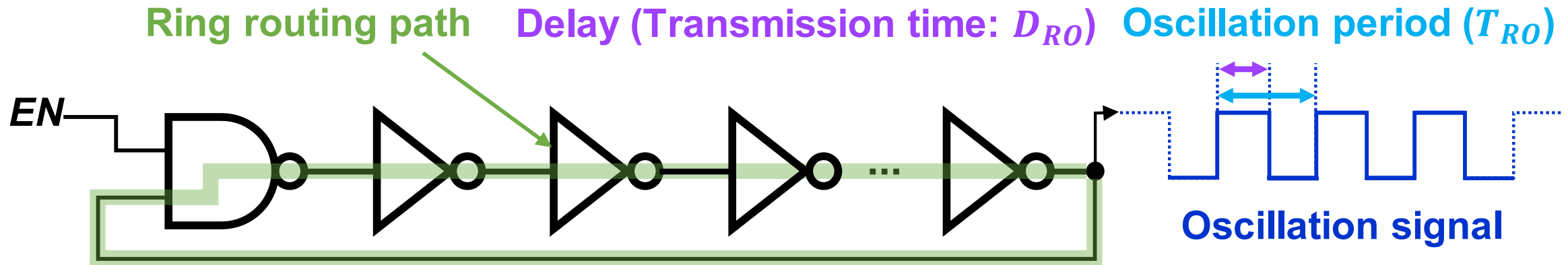
- **ATD** is extremely sensitive to **delay variation**
- **Aging phenomena** increase the threshold voltage of the transistors in ATD
  - slow down the switching speed
  - false detection of the address change





## 4. Aging Defect Testing ~ Ring oscillator (RO) ~

- **Ring oscillator** is effective way as on-chip digital delay sensor
  - to measure circuit delay variation in a target device (such as in ASIC )

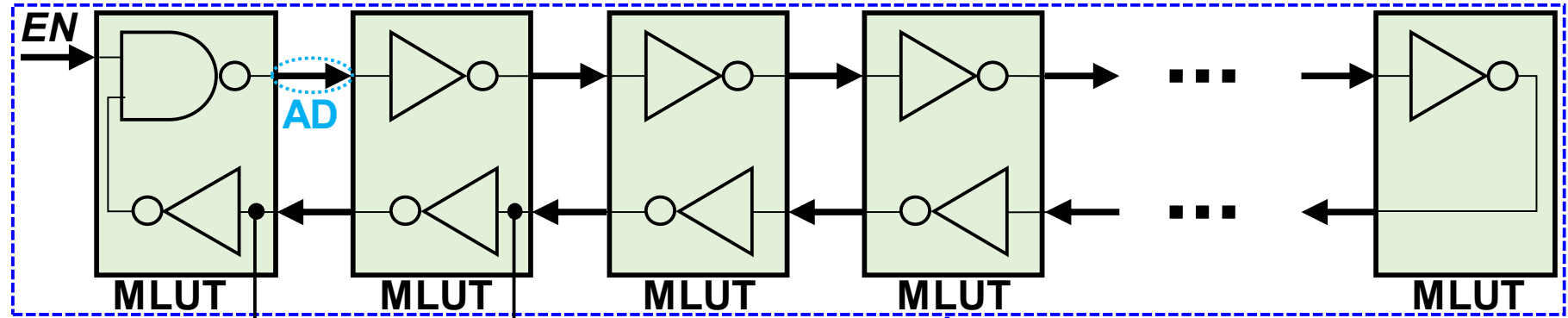


We can calculate Transmission Delay  $D_{RO}$  through the oscillation number  $N_{osc}^{t_{RO}}$  within a certain oscillation operation time  $t_{RO}$ :

$$D_{RO} = \frac{T_{RO}}{2} = \frac{t_{RO}}{2N_{osc}^{t_{RO}}}$$

# 4. Aging Defect Testing ~ LUT-based Delay-Monitoring ~

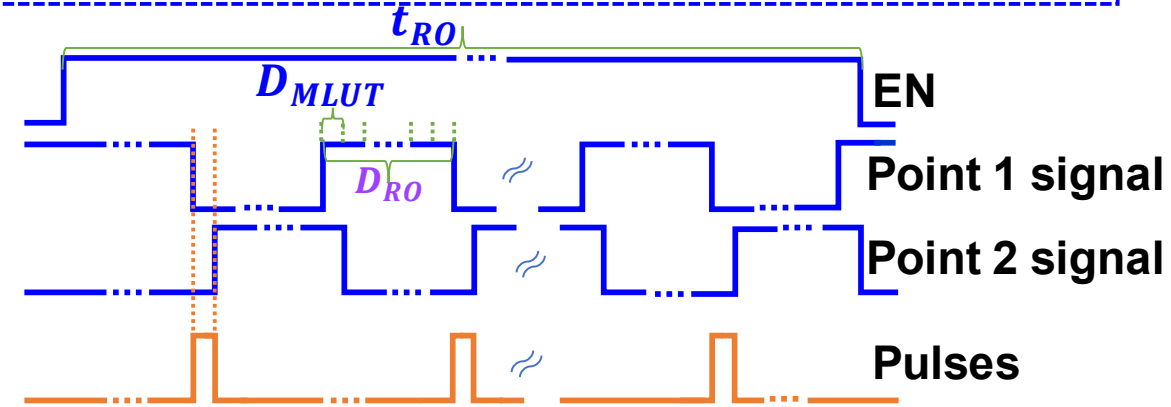
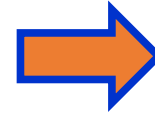
Deploy RO  
in MLUTs



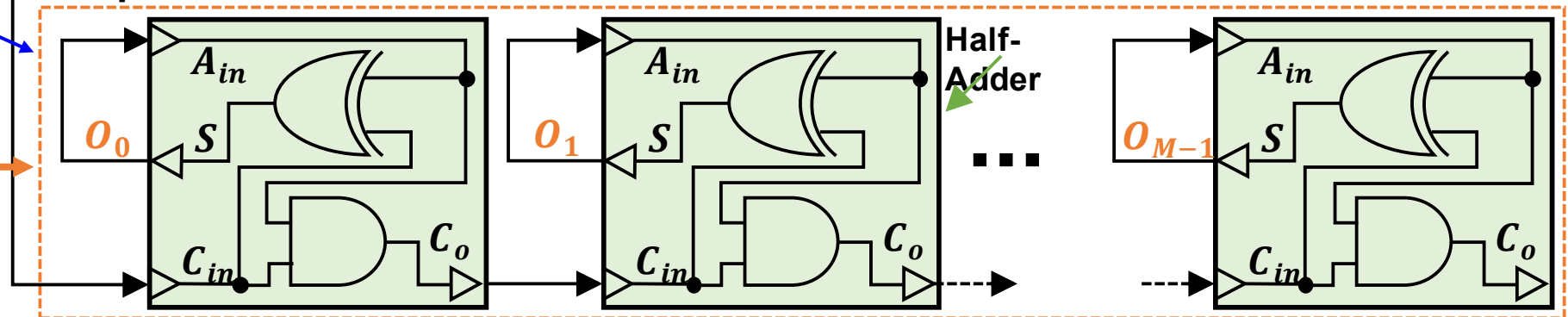
$$D_{MLUT} = \frac{D_{RO}}{N_{AD}} = \frac{t_{RO}}{2N_{OSC}^{t_{RO}} N_{AD}}$$

$$N_{OSC}^{t_{RO}} = (O_{M-1} \cdots O_1 O_0)_2$$

Edge detection  
pulse



Deploy RO Counter  
in MLUTs



# 4. Aging Defect Testing ~ LUT-based Delay-Monitoring ~

## --- Implementation Procedure

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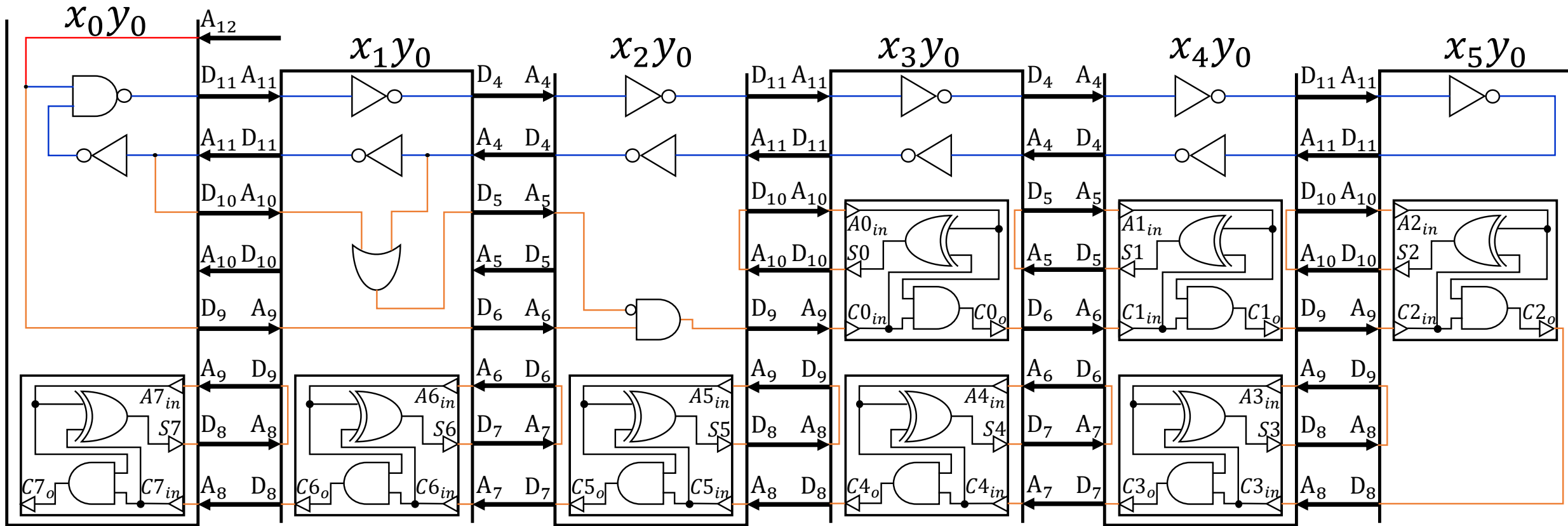
### Implementation Procedure

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- Step 1: select measurement area (MLUTs);*
  - Step 2: deploy RO and counter;*
  - Step 3: create the truth tables for each MLUT in the area;*
  - Step 4: write the truth tables into corresponding MLUTs;*
  - Step 5: set the MPLD to logic operation mode;*
  - Step 6: set oscillation operation time ( $EN=1$ );*
  - Step 7: observe the oscillation number (counter outputs).*
-

# 4. Aging Defect Testing

## ~ Simulation for LUT-based Delay-Monitoring

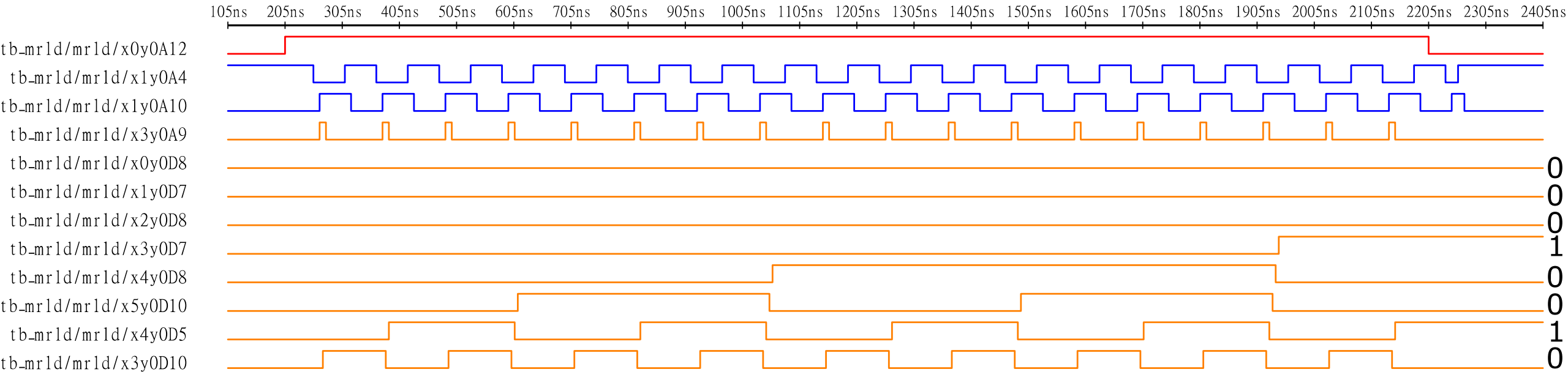


**Logic simulation experiment using ModelSim:**

- 1: route the RO pass through 10 AD interconnects in the measurement area ( $N_{AD}=10$ ).
- 2: inject the **5.5ns delay in the ATD circuit** ( $D_{ATD} = 5.5ns$ ) for each MLUT and the overall oscillation operation time of the RO to **2000ns** ( $t_{RO}$ ).

# 4. Aging Defect Testing

## ~ Simulation result ~



$$N_{OSC}^{t_{RO}} = (00010010)_2 = 18$$

$$D_{MLUT} = \frac{t_{RO}}{2N_{OSC}^{t_{RO}} N_{AD}} = \frac{2000ns}{2 \times 18 \times 10} = 5.5ns$$

confirmed

$$= D_{ATD} = 5.5ns$$

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- To guarantee the long-term reliability of the MPLD device, this study proposed
  - test method
    - to identify the interconnect defects under the production phase
  - LUT-based delay monitoring
    - to detect the aging-caused failures in the field
- To evaluate the proposed methods, this study
  - designed an MPLD with a  $6 \times 6$  MLUTs array
  - performed logic simulations by injecting faults into MPLD
  - confirmed the effectiveness of the proposed methods

Thank you for your listening



# Q&A