Test Point Insertion for Multi-Cycle Power-On Self-Test

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Under the functional safety standard ISO26262, automotive systems require testing in the field, such as the power-on self-test (POST). Unlike the production test, the POST requires reducing the test application time to meet the indispensable test quality (e.g., >90% of latent fault metric) of ISO26262. This article proposes a test point insertion technique for multi-cycle power-on self-test to reduce the test application time under the indispensable test quality. The main difference to the existing test point insertion techniques is to solve the fault masking problem and the fault detection degradation problem under the multi-cycle test. We also present the method to identify a user-specified amount of test points that could achieve the most scan-in pattern reduction for attaining a target test coverage. The experimental results on ISCAS89 and ITC99 benchmarks show 24.4X pattern reduction on average to achieve 90% stuck-at fault coverage confirming the effectiveness of the proposed method.

CCS CONCEPTS • Integrated Circuits • Hardware Test • Design for testability

Additional Keywords and Phrases: LBIST, POST, Multi-cycle Test, ISO26262, Functional Safety

With the rapid evolution of technologies in developing automotive systems toward fully autonomous vehicles, various complex integrated circuits (ICs) are embedded in a car. The functional safety of the automotive system becomes a fundamental requirement as indexed by the ISO26262 standard [1].

Power-on Self-Test (POST) is the most common test solution to ensure the safety of a system. It tests the safety-critical components during the system's startup before running any functional operations. It is thus helpful to detect any potential faults inside the components early to avoid a system failure. For testing automotive ICs, The POST needs to meet several constraints as follows.

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- Indispensable test quality: The ISO26262 standard imposes at least 90% latent fault metric to meet the most stringent automotive safety integrity level (ASIL D) for avoiding a random hardware failure (e.g., stuck-at faults) during the lifetime of ICs [1];
- Limited test application time (TAT): test must be complete during the power-on reset at the engine startup (e.g., 10~50ms);
- Low power: the consideration of power consumption during the test is helpful to avoid false tests under the delay fault model [2];
- Low silicon overhead: suppress the increase of the Design for Test (DFT) hardware due to the ever-increasing complexity of ICs.

In the past, many sophisticated solutions have been introduced to reduce the test volume of the standard LBIST, such as scan structure optimization [3, 4], the weighted random pattern [7, 8], random vector perturbing [9], Bit-flipping [10] and reseeding [11, 12, 13]. Test point insertion (TPI) technology improves the testability of CUT by inserting test logic into the CUT to deal with the detection of random pattern resistant (RPR) faults [14, 15, 16]. Other solutions focus on improving the test scheme of LBIST to enable the test-per-clock testing [17, 18], such as the shadow flip-flops insertion [19], and the Tri-Modal Scan test scheme [20] with reconfigurable scan cell design. Recently the deterministic test compression technology is also applied to the automotive ICs to run a POST or an in-system test [21, 37]. The deterministic compression test requires a modified BIST structure to allow applying the external test patterns generated by ATPG or continuous reseeding for high fault coverage. In this work, we focused on improving the test quality of an on-chip TPG-based LBIST by introducing a multi-cycle test described later to make the standard LBIST comply with the ISO26262 standard.

Multi-cycle test applying more than one clock to run many times function operation after the scan-shift operation is a smart way to complement the quality of the test patterns (scan-in patterns) for test compaction [22, 23, 24], low-power testing [25, 26, 27], and logic diagnosis [28]. In a multi-cycle test, the response of CUT at each capture cycle is applied to the CUT in parallel as a capture pattern at the subsequent capture cycle. This feature is helpful to reduce the volume of scan-in patterns for attaining a target test coverage when the capture patterns can detect any additional faults that are missed by the root scan-in pattern. The multi-cycle test has the behavior to take the CUT closer to its functional operation conditions that can generate functional vectors with lower power consumption, which are very helpful to at-speed testing for delay fault detection [26, 27]. It is also easy to implement the multi-cycle test w/o the extra overhead in terms of software (e.g., modified ATPG for deterministic pattern generation) and hardware (e.g., reseeding logic & memory). Therefore, the multi-cycle test is expected to be a promising test scheme to a trade-off among the test coverage, TAT, silicon area, and low power for POST.

A multi-cycle test may not always be effective for test reduction when the functional sequences generated by the CUT are not helpful to fault detection. Appropriate DFTs that can complement the value of the functional sequences are necessary to enhance the ability of the multi-cycle test to test reduction. Many DFT approaches to improve delay fault detection were presented in the past. In [29], the authors proposed a new scan cell named Transition-Launch Flip-Flop to complement the test vectors by modifying the value of partial FFs after the launch cycle in a two-cycle broadside test. In [30] and [31], the author expanded the approach of [29] to multi-cycle tests and proposed the DFT approaches to enhance the ability of the capture states to delay fault detection by holding [30] or reversing [31] the value of all FFs at the appropriate capture

cycles. These DFT approaches considered the condition/requirement of the hard-to-detect delay faults in the multi-cycle test.

In our previous works [32, 35], we have discussed the fault masking problem and the fault detection degradation problem (FDD) that would obstruct the effect of multi-cycle tests to detect stuck-at faults. It is necessary to solve the problems to reduce the test application time of POST under the indispensable test quality specified in the ISO26262 standard. The main difference between the existing DFT approaches and our works is to solve the Fault Masking and FDD problems for the stuck-at fault detection under the multi-cycle LBIST.

The fault-masking problem denotes that the fault effects excited at the intermediate capture cycles might be masked before the effects are propagated to the final capture cycle for observation. To address this issue, we proposed a novel scan cell named the fault-detection-strengthened FF (FDS-FF) that directly observes and keeps the value of a faulty effect as it arrives at the FF during the capture operations [32, 33, 34].

The FDD denotes that the capability of capture patterns to detect additional stuck-at faults degrades with the increase of the number of capture cycles [35]. In [36], we have proposed a control point insertion (CPI) method to overcome the FDD by inserting control logic into scan FFs that modifies the value captured into the FFs during intermediate cycles, named the FF-CPI. While the basic idea is similar to the DFT proposed in [30, 31], our approach targeted controlling partial FFs but not the whole scan chain. We also proposed an approximate evaluation approach to identify CPs by analyzing the circuit structure without fault simulation. In general, the fault-simulation-based evaluation in [30, 31] needs more processing time than our method. Moreover, in this paper, we expand the FF-CPI approach of [36] to control the internal state of the combinational logic for stuck-at fault detection, which is different from the exiting DFT approaches will be described in Section 4.

This paper consolidates the FDS-FF insertion approach denoted by OP (observation point) insertion and the FF-CPI approach into a complete DFT technique referred to as the test point insertion (TPI). Unlike the conventional TPIs which detect the random pattern resistant faults, our TPI focus on addressing the Fault Masking problem and FDD problem under a multi-cycle LBIST scheme to reduce the volume of scan-in patterns to meet the indispensable test quality specified by ISO26262.

The main contributions of this paper are as follows.

1. We clarify the mechanism of Fault Masking and FDD by analyzing the stuck-at fault detection model in the multi-cycle BIST scheme.
2. We expand the FF-CPI approach to control the internal state of combinational logic by a newly proposed control logic circuit named Self-flipping CP to improve the testability for stuck-at fault detection under multi-cycle tests.
3. We propose a new metric to evaluate the effect of candidate signal lines for CP insertion under the multi-cycle BIST scheme.
4. We introduce an improved probabilistic cost function to estimate the effect of CP and OP insertion.
5. We introduce a consistent procedure to identify a user-specified number of CPs and OPs to achieve the most scan-in pattern reduction for attaining a target test coverage in the multi-cycle BIST scheme.

6. We evaluate the effectiveness of the proposed TPI for shortening the test application time based on the experimental results of ISCAS'89 and ITC'99 benchmark circuits under the single stuck-at fault model.

The remainder of this paper is organized as follows. Section 2 introduces the basic concept of test-per-scan BIST, the multi-cycle test, and its issues. Section 3 describes the fault detection model under multi-cycle BIST. Section 4 presents the TPI approach for multi-cycle BIST. Section 5 shows the experimental results on benchmark circuits. Section 6 concludes the paper.

1 MULTI-CYCLE TEST SCHEME

In this section, we first review the characteristic of scan BIST and multi-cycle BIST and discuss the problems of multi-cycle tests.

1.1 Scan BIST

In a traditional test-per-scan BIST, pseudo-random vectors generated by the on-chip TPG are serially loaded into the scan chains driven by scan-shift clocks, known as scan operation. When all the scan registers are filled up, a complete scan-in pattern is latched to the inputs of the circuit. The circuit is then switched to the functional operation that generates the corresponding functional response at the outputs of the circuit. The FFs will be updated with the functional responses of the circuit when the trigger edge of the functional clock arrives, known as the capture operation. The captured functional response will be unloaded for fault detection as loading the next scan-in pattern. It is easy to observe that test is conducted only once by applying a complete scan-in pattern. Almost all test application time is consumed in the serial scan shift operation for test data delivery.

1.2 Multi-cycle BIST

The multi-cycle test applies more than one functional clock to run many capture operations for every single scan-in pattern. In Figure 1, we show the operations during the multi-cycle test in the time-frame expansion of CUT. Let's define a multi-cycle test by $<s_i, v_i, c_{ij}, o_i>$, where s_i denotes a scan-in pattern; v_i denotes a primary input vector; c_{ij} denotes the responses of CUT captured into the scan chains represented by the capture patterns at the jth functional clock; o_i denotes a scan-out pattern which is the response of the combinational circuit when c_{ij} is applied at the last capture. After a scan-in pattern s_i is loaded into the scan chain in serial, the corresponding response c_{i1} is generated at the outputs of combinational logic (FFs drawn in dashed line) and captured into the FFs in parallel by the functional clock T1. Then, c_{i1} is used as test stimuli and latched to the circuit to generate a new response c_{i2}, and c_{i2} is applied and generate the corresponding response c_{i3} in parallel until the final capture clock is applied. The response captured at the final capture o_i is unloaded for observation. It should be noted that the state of primary inputs v_i will be kept constant and the primary outputs in the intermediate capture cycle are considered unobservable during the capture operation.

From Figure 1, it can be observed that conducting a multi-cycle test for each scan-in pattern $<s_i, v_i>$ could provide more chances to detect additional faults through the functional capture patterns c_{ij}. Therefore, it has promising potential to reduce the number of scan-in patterns for attaining a target test coverage that contributes to shortening the test application time due to fewer scan-shift operations. In addition, since the time of capture operation is negligible compared to the serial scan-shift operation, the reduction of the total test application time for POST is expectable.

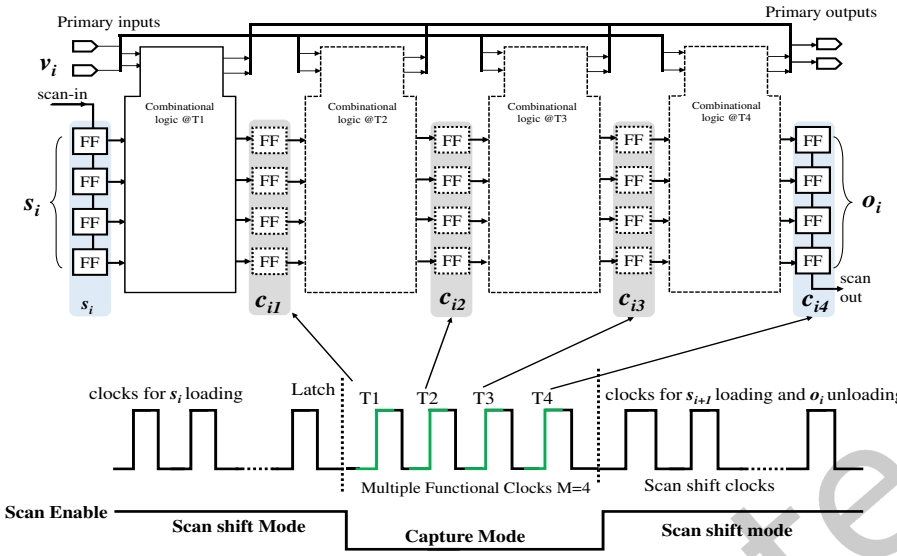


Figure 1. Test operations in multi-cycle BIST

1.3 The Problems of Multi-cycle BIST

In our earlier works, we have raised two issues that would obstruct the effect of multi-cycle test to reduce the scan-in patterns for shortening the TAT of POST, called the Fault Masking [32, 33, 34] and Fault Detection Degradation of Capture Pattern [35, 36], respectively. The following gives a brief overview of these problems for this study.

1.3.1 Fault Masking

Fault Masking denotes that the fault effects excited at the intermediate capture cycles by capture patterns might disappear before these effects are propagated to the final capture cycle for observation. Suppose that a fault *f* is excited at the first capture cycle by the scan-in pattern. To detect *f,* its faulty value has to be propagated through all *M-1* capture cycles until the final capture cycle is applied. When the CUT has a deep combinational logic or the capture operation runs in a large cycle number, the time-expanded propagation path of the faulty value would become too long to be activated for detection, and the faulty value might be masked at certain logic due to the un-controllable logic state during the capture operation. Severe fault-masking would decrease the test quality of the scan-in patterns and capture patterns, and finally, obstruct the effect of the multi-cycle test for reducing the scan-in patterns.

1.3.2 Fault detection degradation problem (FDD)

FDD means the capability of capture patterns to detect more additional stuck-at faults degrades as increasing the number of capture cycles. This is based on the observation that multi-cycle tests can take the CUT closer to its functional operation conditions with small internal transitions when increasing the capture cycles [26]. The functional operation would consequently cause the states of the large number of FFs to become constant when a number of capture cycles are applied. Since the value of FFs is reused as test stimuli at the

subsequent capture cycles, the large number of FFs with constant values would cause the loss of randomness property of the capture patterns that obstructs the detection of additional faults.

2 FAULT DETECTION MODEL IN MULTI-CYCLE BIST

In this section, we give a detailed analysis of the stuck-at fault detection model in a multi-cycle BIST scheme to elucidate the mechanism of Fault Masking and FDD as follows.

For a stuck-at fault F_i, its faulty effect will always exist at each capture cycle during the capture operation, and we express it by f_{ij} in the time-expanded circuit as shown in Figure 2. The faulty effect of F_i at each capture cycle might be excited by the inputs of CUT. We use Pe_{ij} to denote the probability to excite fault F_i at the jth capture cycle. To detect F_i, the excited faulty value of F_i at the jth capture cycle (f_{ij}) must be propagated to the scan FFs for observing after the final capture, and we denote the propagation probability as Pp_{ij}.

In LBIST, Pe_{ij} and Pp_{ij} of a stuck-at fault $F_{i/s}$ can be estimated by computing the $s^{\neg}$ controllability ($C_{ij/s^{\neg}}$) and the observability (O_{ij}) of signal line i through the probabilistic random pattern testability measure such as COP (Controllability Observability Procedure). Hence, the detection probability of $F_{i/s}$ at the jth capture cycle denoted by $Pd_{ij/s}$ can be expressed by $Pd_{ij/s}=C_{ij/s^{\neg}}\times O_{ij}$. For a multi-cycle test with M capture cycles, the fault $F_{i/s}$ would have M times opportunity to be excited by the capture patterns c_{i1}~c_{iM}, and $F_{i/s}$ will be detected out of once the fault is excited and propagated to the outputs. Hence, the detection probability of $F_{i/s}$ denoted by $Pd_{i/s}$ in a multi-cycle test is the complementary probability of the case that $F_{i/s}$ cannot be excited and propagated for detection at all capture cycles, which can be expressed by:

$$Pd_{i/s} = 1 - \prod_{j=1}^{M}(1 - C_{ij/s^{\neg}} \times O_{ij}) \quad (1)$$

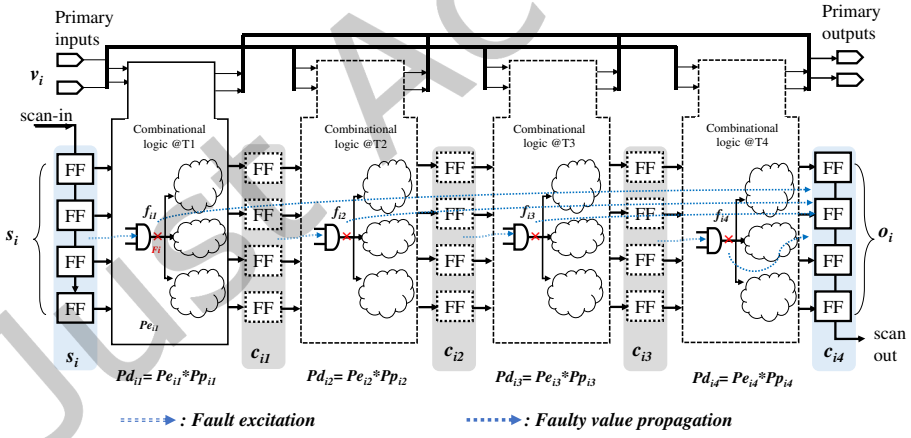


Figure 2. Single stuck-at fault detection in time-expanded circuit

To calculate the controllability and the observability of signal lines at each capture cycle, we transform the CUT to M cycles time-frame expansion combinational circuit. We initialize the 0/1 controllability ($C_{i1/0}$ and $C_{i1/1}$) of PI (primary input) and PPI (pseudo-primary input: FF) at the first capture cycle to 0.5/0.5, then, calculate the value of $C_{ij/0}$ and $C_{ij/1}$ for each gate at each time-frame. The observability of signal line at each

time-frame is calculated starting from the PO (primary output) and PPO (pseudo-primary output) at the last capture cycle with initial value of 1.0, tracing back to the PI and PPI until the first capture cycle.

Compared to the traditional scan test with a single capture, the multi-cycle test shows the potential to improve the probability of fault detection for every single scan-in pattern followed by multiple capture patterns. However, the fault detection in the multi-cycle test depends on the controllability and observability of signal lines in the time-expanded circuit, which is generally deteriorating as increasing the number of capture cycles.

For demonstration, we conducted preliminary experiments on ISCAS89 and ITC99 benchmark circuits to evaluate the average 1-controllability and the observability of signal lines at each capture cycle. Figure 3 shows the results. In Figure 3. a, it can be observed that ITC99 circuits show higher 1-controllability, which implies the internal states of these circuits are easy to be 1, whereas ISCAS89 circuits likely trend to be 0. Figure 3. b shows the standard deviation of 1-controllability of signal lines at each capture cycle corresponding to the results of Figure 3. a, to demonstrate the impact of increasing capture cycles on the controllability. The results show that the standard deviation of 1-controllability becomes higher as increasing the capture cycles, which implies the controllability of more signal lines is biasing toward either 0 or 1; in other words, the value of more signal lines in a large capture cycle would be most likely fixed at 0 or 1 during the tests. For a signal line with stuck-at fault, higher 0-controllability (0-bias) is helpful to excite the *s-1* fault, whereas exciting the *s-0* fault becomes difficult. Moreover, the biased controllability of signal lines in a time frame would also affect the path sensitization for propagating the excited faulty values to the FFs in the current time frame. We insist on it as the root cause of FDD observed in our previous works.

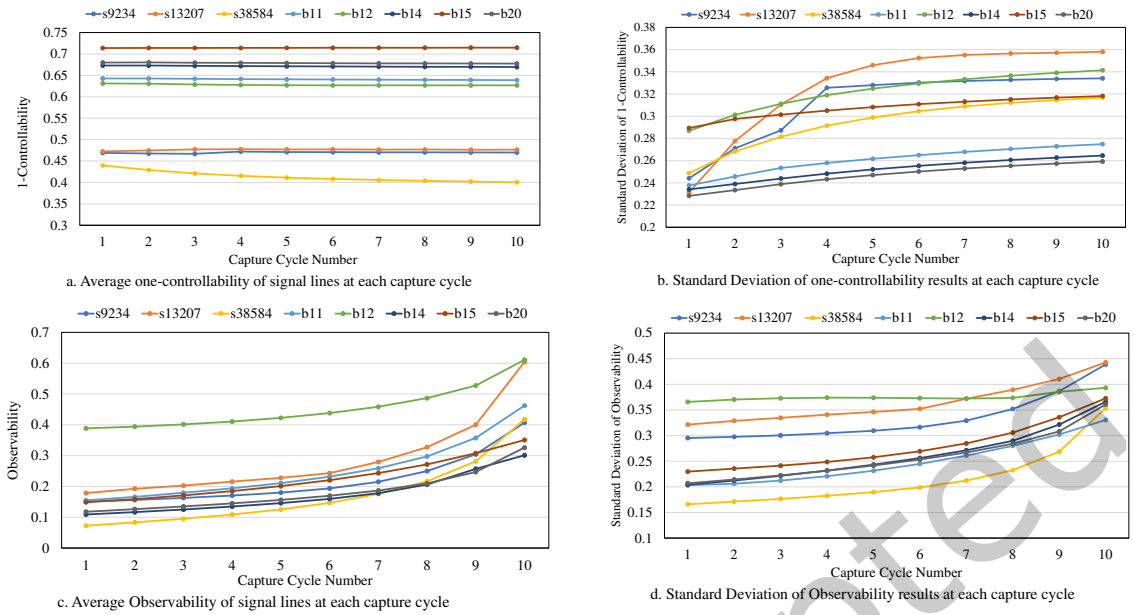


Figure 3. Testability vs. Capture Cycles

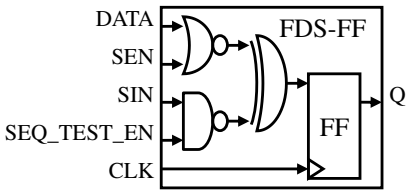
Regarding the observability shown in Figure 3.c and 3.d, it can be observed that in a 10-times expand circuit the value of more signal lines in earlier capture cycles is more difficult to be observed from the outputs (scan FFs) after the final capture. The deterioration of observability of signal lines at early capture cycles causes the faults excited at an early capture cycle difficult to be propagated to the final capture cycle for detection, which is the root cause of the fault masking.

Based on the above analysis, we derive that the primary factor affecting the multi-cycle test to reduce the scan-in patterns for shortening the TAT of POST should be the incompatibility between the controllability and observability in the time-expanded circuit under multiple capture cycles. Where smaller 0/1 controllability bias of signal line at earlier capture cycles with lower observability.

We insist that reconciling the incompatibility of testability under the multi-cycle test is necessary to improve the performance of multi-cycle BIST for scan-in pattern reduction.

3 TEST POINTS FOR MULTI-CYCLE BIST

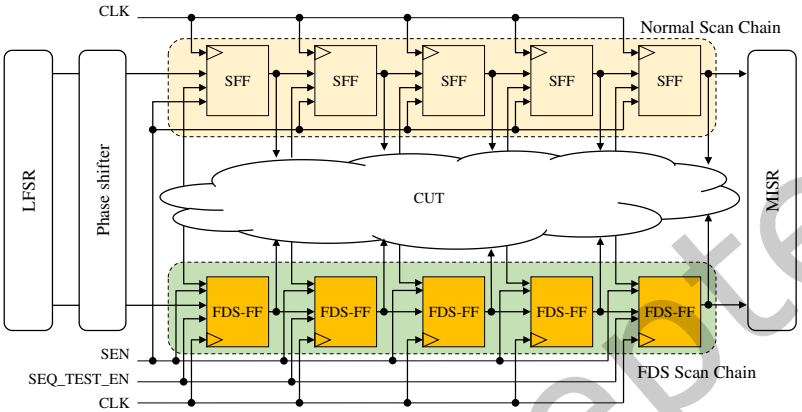
In this section, we introduce the observation point and control point proposed in our previous works [32, 33, 34, 35, 36] to address the Fault Masking and the FDD of the multi-cycle test, respectively.



a. logic design of FDS-FF

Port	Function	Shift Mode	Capture Mode	User Mode
DATA	Data In	don't care	0/1	0/1
SIN	Scan-in	0/1	0/1	don't care
SEN	Scan Enable	1	0	0
CLK	Clock	010	010	010
SEQ_TEST_EN	Sequential Test Enable	1	1	0
Status		!SIN	DATA^!SIN	DATA

b. Operation mode of FDS-FF



c. LBIST with an independent FDS-FFs scan chain

Figure 4. The DFT architecture of FDS-FF insertion for LBIST.

3.1 Observation Point: FDS-FF

To improve the observability of scan FFs at the intermediate capture cycles in the time-expanded circuit, we proposed a new scan-cell design named *fault-detection-strengthened FF (FDS-FF)* that can directly observe and keep the value of FFs captured at each cycle. Figure 4 shows the structure of FDS-FF and the DFT architecture for LBIST with FDS-FF insertion. The output of CUT denoted as DATA is controlled by scan enable signal (SEN) through a NOR gate, and a sequential test controls the scan-in test enable signal (SEQ_TEST_EN) through a NAND gate. The FDS-FF can work in three modes: *Shift*, *Capture*, and *User* mode as shown in the table, where *Shift* and *Capture* modes refer to as the Test mode, and *User* Mode refer to as the functional operation. The CUT will work at the user mode when SEQ_TEST_EN and SEN are set to 0. In Test Mode, SEQ_TEST_EN is set to 1, and the SEN signal controls the shift and the capture modes. If SEN=1, the test pattern is loaded into FF. If SEN=0, the corresponding test responses are captured. It should note that the test responses of CUT captured at each cycle are XORed with the SIN, which is the data stored in the neighbor FF in the scan chain. In this way, the test responses of each cycle can be compacted by the XOR gate, and the compacted test responses will be applied to the next capture cycle as a new test pattern. Since FDS-FFs observe and keep the capture response of CUT during the capture operation, in order to avoid functional timing issues, all FDS-FFs are extracted to constructed into a daisy chain and isolated from the other normal scan chains.

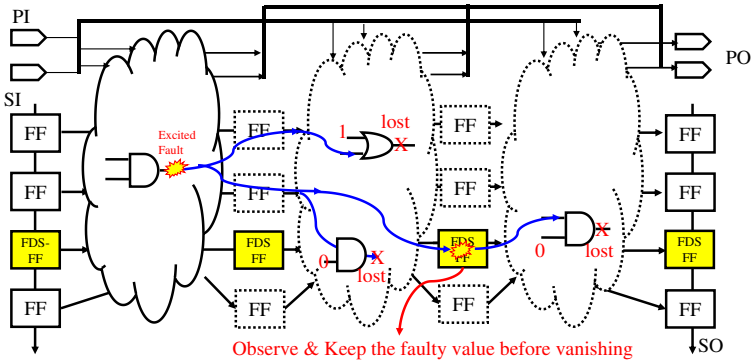


Figure 5. Replace a scan-FF with FDS-FF to address fault masking

Figure 5 shows the effect of FDS-FF to address the fault masking problem. In a time-expanded circuit, some faulty values are successfully propagated to the FF at the intermediate capture cycles, however, would be masked before the final capture. Replacing a scan FF with the FDS-FF is equivalent to inserting an observation point into the time-expanded circuit to observe and keep these faulty values before they are masked. However, it is impractical to replace all scan-FFs with FDS-FFs, the fault effects that never pass through the selected FDS-FFs may disappear if they cannot be propagated to the final capture cycle. Fortunately, replacing a small count of scan cells with FDS-FFs could achieve significant fault detection improvement [33], which is beneficial for low hardware overhead.

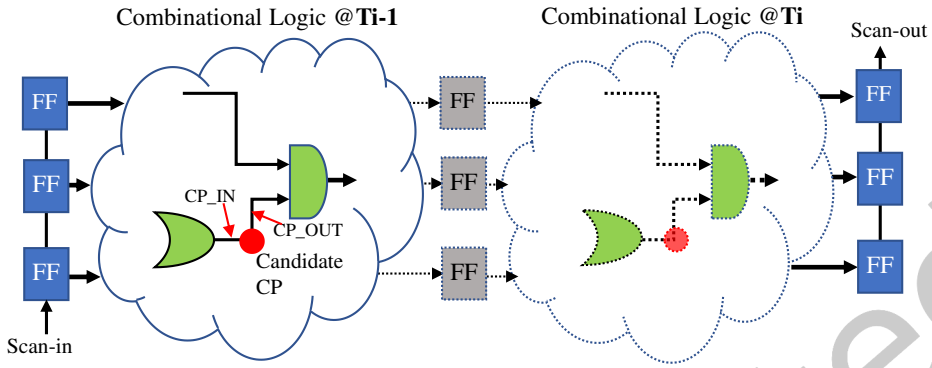
3.2 Control Point: Self-Flipping CP

Insert control points into the circuit to force the target signal line to 0 (0-control) or 1 (1-control) is a popular way to improve the testability of the circuit. However, it would be challenging to adapt the conventional CPI to the time-expanded circuit under multi-cycle BIST because 1) CP with a fixed control value during a complete capture operation is less helpful to relax the controllability biasing; 2) generating the control values for each capture cycle requires complex sequential ATPG; 3) applying the dynamic control value to CP during the capture operation requires intricately designed control logic.

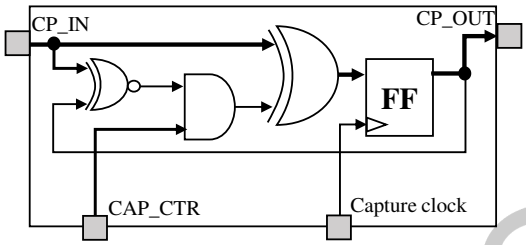
In [35, 36], we have proposed an FF-CPI approach to improve the controllability of the time-expanded circuit by modifying the captured values of partial scan FFs at each capture cycle. The FF-CP compares the state of FF at the current capture cycle with its state at the previous capture cycle and changes the current state to its inverse value if no state transition occurs on the FFs during the capture cycles. In this paper, we expand the FF-CPI approach to control the combinational logic and propose the control logic that can flip the value of the signal line of CP during the capture operation. We call it the Self-Flipping control in this paper described as follows.

Figure 6 shows the design of the Self-Flipping control logic. In the capture mode, the present state (CP_OUT@T_{i-1}: the state of CP after the previous capture cycle) and the new state (CP_IN@T_i: the input value of the candidate CP of the current capture cycle) of the CP are checked whether there is a transition occurs in the current capture cycle or not. If not, the Self-Flipping control logic will generate the inverse value of the input state to the CP output (CP_OUT@T_i). An external control signal “CAP_CTR” is used to

enable the self-Flipping when set to 1. Otherwise, the input value of CP passes through the CP logic to the output. It thus can keep the value of a target signal line at the adjacent time-frame always different to relax the bias of 0/1-controllability caused by successive capture cycles.



a. inserting a self-flipping control point into the time-expanded circuit



b. self-flipping control logic

CAP_CTR	CP_OUT @Ti-1	CP_IN @Ti	CP_OUT @Ti
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1

c. The truth table of self-flipping control logic

Figure 6. Self-Flipping CP insertion for multi-cycle LBIST

It is worth noting that a traditional inversion CP using an XOR gate would be ineffective in reducing the 0/1-controllability bias because the 0/1-controllability of XOR-CP output depends on the input signal line, which is biasing as increasing the capture cycles. While inserting the Self-Flipping CP will cause hardware increase, it operates automatically during the capture cycles w/o any external control, which does not cause the extra cost in updating the ATPG to generate the control vectors.

To implement the proposed multi-cycle LBIST scheme for POST, the unknown values (Xs) generated as switching the operation mode from test and function need to be dealt with carefully. This issue can be addressed by separating the control logic of POST from the test target of POST (CUTs) through wrapper logic. During the test operation, the wrapped control logic of POST will be kept in function mode. When the test is completed, the CUTs will be switched to the functional mode by a system reset through the control logic of POST. The detailed solutions to handle the implementation issues for in-system-testing have been introduced in [37, 38].

4 TP SELECTION FOR MULTI-CYCLE BIST

This section introduces the procedure to determine the locations of CPs and OPs to address the Fault Masking and the FDD problem induced by the controllability biasing and observation deterioration under a multi-cycle LBIST scheme.

While the selection procedure inherits some underlying techniques proposed in our previous works, such as the structure-based evaluation metric and the probabilistic testability analysis of circuits for FDS-FFs and FF-CP insertion, in this paper, we consolidate them into a consistent process for TP selection under multi-cycle BIST through the following efforts:

- We propose a new metric to evaluate the effect of candidate signal lines for CP insertion under a multi-cycle BIST scheme.
- We introduce an improved probabilistic cost function for estimating the effect of candidate TPs.
- We introduce an OP Pruning approach into the TP procedure to improve the efficiency of TP selection under the multi-cycle BIST scheme.

It is worth noting that the proposed TP selection procedure conducts the probabilistic evaluation to identify the candidate CPs and Ops. The proposed TP selection procedure is a time-saving process because it does not use the conventional fault simulation. As a result, we obtain the list of the TPs, then we evaluate the fault coverage achieved under the circuit with TPs by conducting the multi-cycle test fault simulation at one time.

4.1 A new Evaluation Metrics for CP selection

As discussed in Section 3, increasing the number of capture cycles would cause a significant 0/1-controllability bias on signal lines at later capture cycles, which implies the value of more signal lines in a large capture cycle would most likely fix at 0 or 1 in most capture cycle. For a signal line *x*, if setting its value to 0(1) would cause fewer gates with fixed output value in its arrival logic region to FFs than that of setting to 1(0), 0(1)-controllability bias of *x* due to the multiple capture cycles would be helpful to fault excitation and propagation we call it positive bias, 1(0)-controllability bias would obstruct the fault detection called the negative bias. For the signal line shows a negative bias in controllability, it is suggested to insert a self-flipping CP to relax its controllability bias in the multi-cycle test. Following this, we propose the method to calculate the degree of the 0/1 controllability bias when inserting a CP into the signal line.

- *x: a signal line in the combinational circuit*
- $p_{x/0}$*: the probability of line x's value being logic 0*
- $p_{x/1}$*: the probability of line x's value being logic 1, where,* $p_{x/1}+p_{x/0}=1.0$
- $fg_{x/0}$*: the number of gates in the arrival logic region from line x to POs/PPOs whose output value will be fixed, as setting the value of x to 0*
- $fg_{x/1}$*: the number of gates in the arrival logic region from line x to POs/PPOs whose output value will be fixed by setting the value of x to 1*
- *BD(x): the degree of controllability bias at line x that would impact the fault detection, where BD(x)>0 denotes a positive bias, BD(x)<0 denotes a negative bias.*

$$BD(x)=(p_{x/0}-p_{x/1})\times(fg_{x/1}-fg_{x/0}) \qquad (2)$$

- *CD(x): the degree of contribution to relax the controllability bias as forcing the 0/1-controllability of line x to 0.5/0.5. CD(x)>0 denotes a positive contribution, CD(x)<0 denotes a negative contribution that would be achieved by CP insertion.*

$$CD(x)=(p_{x/0}-0.5)\times fg_{x/0}+(p_{x/1}-0.5)\times fg_{x/1}=(0.5-p_{x/0})\times(fg_{x/1}-fg_{x/0}) \quad (3)$$

We use the s27 circuit as an example for illustration, see Figure 7. For signal line *i*, two paths connect with the PPO (FF2) through path 1: $i \rightarrow G5 \rightarrow G7 \rightarrow G8 \rightarrow w$, and path 2: $i \rightarrow G6 \rightarrow G7 \rightarrow G8 \rightarrow w$. When the value of *i* is 1, the output of G5, G6, and G7 will be fixed at 1, 1, 0, respectively, thus $fg_{i/1}$=3. When *i* is 0, the output of G5 and G6 depends on the other input signal lines *n* and *c*, which implies a 0 value at *i* cannot directly cause any fixed gates on the two paths to FFs, thus $fg_{i/0}$=0. The probability of signal line *i's* values $p_{i/1}$ and $p_{i/0}$ can be calculated using the COP measurement, which is 0.25 and 0.75. The degree of controllability bias is hereby *BD(i)* = 0.5×3 = 1.5, which represents that the controllability bias at signal line *i* is positive to fault detection.

For the signal line with positive controllability bias, inserting a CP would cause more fixed gates on the fault propagation paths to FFs with a negative contribution to fault detection, e.g., *CD(i)*=-0.25×3=-0.75. Table 1 gives the evaluation value of some signal lines shown in Figure 7. It can be observed that signal lines *q* and *s* show the negative controllability bias in BIST, and inserting a CP to *s* would achieve the most contribution to fault detection.

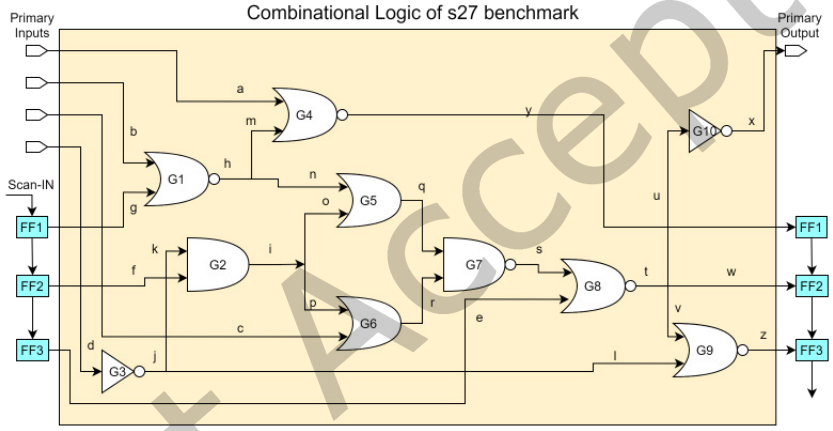


Figure 7. The combinational logic frame of s27 circuit

Table 1: evaluation metrics of signal lines in s27

line #	$fg_{x/0}$	$fg_{x/1}$	$p_{x/0}$	$p_{x/1}$	*BD*	*CD*
h	0	2	0.75	0.25	1	-0.5
i	0	3	0.75	0.25	1.5	-0.75
n	0	1	0.75	0.25	0.5	-0.25
q	3	0	0.56	0.44	-0.36	0.18
s	0	2	0.27	0.73	-0.92	0.46

As shown in Figure 3, the controllability bias on signal line changes at different capture cycles in the multi-cycle BIST. It becomes larger as increase the number of capture cycles. Thus, the degree of

controllability bias of signal line *x: BD(x)* and the contribution of CP insertion to relax the impact of controllability bias on fault detection: *CD(x)* can be easily extended for the multi-cycle test as follows.

$$BD(x) = \frac{fg_{x/1} - fg_{x/0}}{M} \sum_{j=1}^{M} (p_{xj/0} - p_{xj/1}) \quad (4)$$

$$CD(x) = \frac{fg_{x/1} - fg_{x/0}}{M} \sum_{j=1}^{M} (0.5 - p_{xj/0}) \quad (5)$$

where $p_{xj/1}$ and $p_{xj/0}$ denote the probability of line x's value being logic 1/0 at the *j*th capture cycle. We use CD as the evaluation metrics for searching the candidate signal lines for CP insertion under multi-cycle BIST, which is described in the next section.

4.2 TP Selection Procedure for Multi-cycle BIST

The procedure consists of two phases, Phase 1: CP insertion under a time-expanded circuit with full FF-observation, and Phase 2: OP is pruning to remove the impotent observation points (FDS-FF).

In Phase 1, the CP selection will be performed at the time-expanded circuit with full observation where the FFs at intermediate capture cycles are supposed to be observable. This is because the purpose of self-flipping CP insertion is to relax the controllability bias caused by functional operation at each time frame, but not to create long propagation paths that can cross multiple time frames to the final capture cycle for observation which is an arduous task. The algorithm for CP insertion is shown in *Algorithm 1*.

To evaluate the quality of CPs and OPs, cost function *U* as follows is widely used in various TPI techniques.

$$U = \frac{1}{|F|} \sum_{\forall x/s \in F} \frac{1}{Pd_{x/s}} \quad (6)$$

In this work, we expand the cost function considering the fault detection model under the multi-cycle BIST scheme, where the detection probability of the faults at a signal line denoted by $Pd_{x/s}$ is calculated by

$$Pd_{x/s} = 1 - \prod_{j=1}^{M} (1 - (1 - C_{xj/s}) \times O_{xj}) \quad (7)$$

$C_{xj/s}$ and O_{xj} denote the *s-controllability* and observability of signal line *x* at the *j*th time-frame, respectively, computed by COP measure as discussed in Section 3. The difference in *U* before (U^{org}) and after (U^{tp}) inserting a TP can be calculated by the following equation to identify the most effective TP from a candidate TP list.

$$\Delta U = U^{org} - U^{tp} = \frac{1}{|F|} \sum_{\forall i/s \in F} \left(\frac{1}{Pd_{i/s}^{org}} - \frac{1}{Pd_{i/s}^{tp}} \right) \quad (8)$$

In Phase 2, we will remove the impotent observation points from the time-expanded circuit to reduce the hardware overhead caused by FDS-FFs insertion, named OP pruning, as shown by *Algorithm 2*. In OP pruning, the input is the time-expanded circuit with CP insertion achieved at Phase 1 where all scan FFs are replaced with FDS-FFs for observation during multi-cycle captures. We target on reducing the amount of FDS-FFs to a user-specified number N_{op} by restoring the FDS-FFs that do not affect the fault detection to

scan FFs. As shown from line 14 to line 24 of algorithm 2, we compute the cost U of each candidate FDS-FF when temporarily changing it to a scan FF which is equivalent to a wire in the intermediate time-frame circuit, and remove the one which has the least cost increase from the OP list.

The OP pruning is considered effective based on the following observations. 1) The large number of signal lines usually can be observed by multiple FFs; 2) The FFs which have larger observable logic regions could observe more fault effects. 3) The number of FFs in a design is much smaller than that of signal lines, and exploring the inactive FFs would be more time-saving than inserting OPs into the CUT.

ALGORITHM 1: CP insertion

Inputs:
net: original CUT netlist
M: the number of capture cycles
N_{cp}*: Maximum number of CPs*
Outputs:
cplist[N_{cp}*]: Selected CP list*
net_{cp}*: CUT with CP insertion*
Optional parameter:
$CR_{threshold}$*: the threshold of cost reduction (≥0)*
N_{cand}*: number of candidate CP at each iteration of CP decision*
Process:
1: *cplist* ← ∅
2: *cand* ← ∅ */*Candidate CP list for determining a CP*/*
3: *read_circuit (net);*
4: *fix_gate_cal(net); /*computing* $fg_{x/0}$, $fg_{x/1}$**/*
5: *time_expansion (net, M);*
6: *full_observation_point_insertion(net);*
7: while |*cplist*|< N_{cp} do
8: *cop_controllability(*net_{cp}*);*
9: *cop_observability(*net_{cp}*);*
10: *CD_calculate (*net_{cp}*);*
11: *cand* ← ∅*;*
12: for *j=1 to # of available candidate CP* do
13: *cand[j]* ←*unchecked signal line with the largest CD;*
14: end for
15: if *cand*=∅ then
16: *return cplist,* net_{cp}*;* stop the process
17: else
18: U^{org}*=cost_computation(*net_{cp}*,M);*
19: for *k=1 to* N_{cand} do
20: net_{cp}*=insert cand[k] cp to* net_{cp}*;*
21: *update_controllablity_observability(*$net_{cand[k]}$*, M);*
22: ΔU_k=U^{org}*-cost_computation(*net_{cp}*, M);*
23: *Remove cand[k] from* net_{cp}*;*
24: end for
25: If *maximum(*ΔU_k*)>=* $CR_{threshold}$ then

```
26:                         cplist[i]←cand[k];
27:                 end if
28:         end if
29:         insert cplist[i] to net → update net_cp;
30: end while
31: return  cplist, net_cp;
end process
```

ALGORITHM 2: OP Pruning

```
Inputs:
net_cplist: CUT with CP insertion
M: number of capture cycles
N_op:Target number of OPs (FDS-FFs)
Outputs:
oplist[N_op]: FF list for FDS-FFs insertion
net_tp : CUT with TPs (CP and OP)
Optional parameter:
N_cand: # of candidate OPs at each iteration for OP pruning
Process:
1: oplist ← ∅
2: cand ← ∅  /* Candidate target OP list for pruning */
3: read_circuit (net_cp);
4: oplist← all FFs
5: structure_analysis(net_cp);
6: FF_ranking(oplist) /*Ranking the FFs by the approximate evaluation metrics proposed in [39]*/
7: while |oplist|>N_op do
8:         for j=1 to # of available candidate OP do
9:                 cand[j] ←select an OP in the oplist in descending order which is unchecked;
10:        end for
11:        if cand=∅ then
12:                return oplist, net_tp; stop the process
13:        else
14:                U^org=cost_computation(net_tp,M);
15:                for k=1 to N_cand do
16:                        remove cand[k] OP from net_tp;
17:                        update_observability(net_tp);
18:                        ΔU_k=U^org-cost_computation(net_tp, M);
19:                        restore cand[k] OP to net_tp;
20:                end for
21:                If ΔU_k =minimum then
22:                        remove cand[k] OP from net_tp;
23:                        remove cand[k] from oplist;
24:                end if
25:        end if
26: end while
27: return  oplist, net_tp;
end process
```

5 EXPERIMENTAL RESULTS

Experiments are conducted on ISCAS89 and ITC99 benchmark circuits to evaluate the effect of TPI under multi-cycle BIST. A 16-bits internal type LFSR (characteristic polynomial: $X^{16}+X^{15}+X^{13}+X^4+1$) with Phase Shifter generates pseudo-random patterns. A parallel scan structure is introduced into the CUT that consists of multiple scan chains up to 100 FFs in length (when the total number of FFs > 1600, the maximum length of the chain is up to 200). A multi-cycle BIST logic/fault simulator that can simulate at most 50 cycles capture per pattern is implemented in-house for **stuck-at faults** testing. For automotive ICs, the ISO26262 functional safety standard imposes at least 90% latent fault metric (permanent fault) to meet the safety goal ASIL D. Therefore, in this study, we set a target fault coverage 90% and evaluate the effect of the proposed multi-cycle TPI that would make the classical on-chip pseudo-random TPG-based LBIST comply with the ISO26262 standard. Table 2 gives the details of CUTs.

Table 2: Detailed information of benchmark circuits

Circuit	# gate	# FF	# of stuck-at fault	N_{cp} (<1% of gates)	N_{cp} (<5% of FFs)	#OPs (FDS-FFs) (<20% of FFs)
s9234	5597	228	6927	55	11	45
s13207	7951	669	9815	79	33	133
s15850	9772	597	11725	104	29	120
s38417	22179	1636	31180	1141	85	327
s38584	19253	1452	36303	97	72	290
b11	437	31	1322	2	1	6
b12	904	121	2797	9	6	24
b14	4444	245	12811	44	12	49
b15	8338	449	23528	8	8	89
b17	22645	1415	65464	201	70	283
b20	8875	490	25338	88	24	98

5.1 Evaluation of the efficiency of the multi-cycle test

We first performed fault simulations on the regular scan testing with single capture (SCAN) and multi-cycle testing with 2, 4, 6, 8, and 10 capture cycles, respectively, to evaluate the effect of multi-cycle testing for fault detection, using 100k test patterns (scan-in) generated by LFSR. Figure 8 shows the fault coverage of each circuit at different capture cycles when 100k patterns are applied. It can be seen that for most circuits, the multi-cycle test achieved an increase in fault coverage at the 2 and 4 capture cycles. As continuously increasing the capture number to 10 cycles, the increment of fault coverage is slowing down or getting degraded. For s9234, the multi-cycle test shows a significant decrease in fault coverage. It can be explained by the incompatibility of testability shown in Figure 3, where the 10-cycle test caused a little controllability bias, however, significant deterioration of the observability in the expanded circuit.

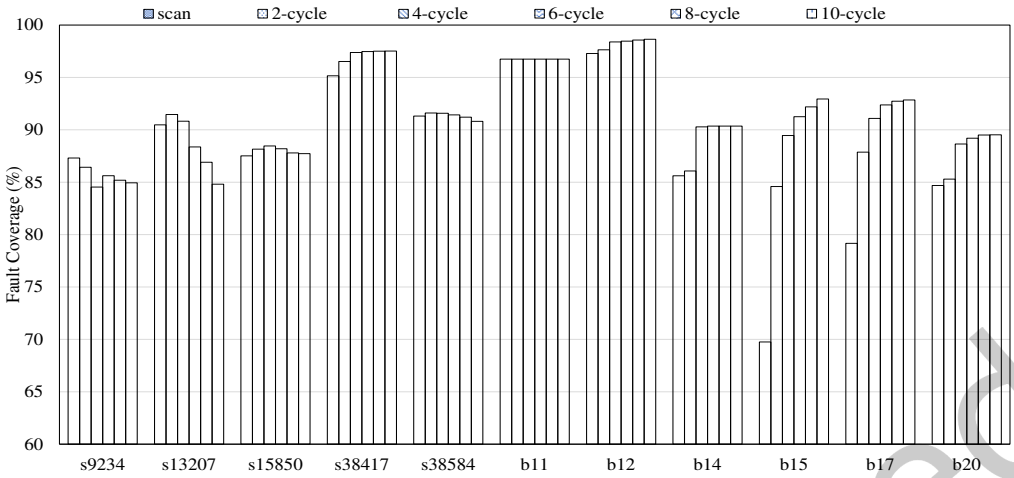


Figure 8: fault coverage of benchmark circuit with 100k patterns

Effect of multi-cycle test on the fault detection of benchmark circuits

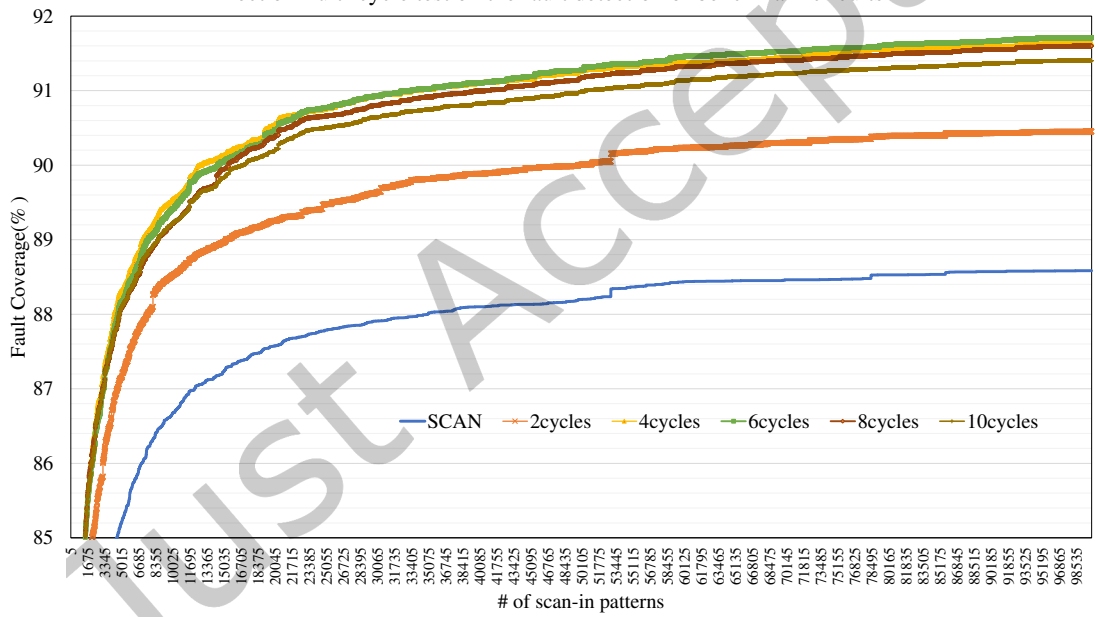


Figure 9: scan testing vs multi-cycle testing

Figure 9 shows the curve of the average fault coverage of all CUTs by increasing the number of patterns. The horizontal and vertical axis shows the pattern number and the corresponding fault coverage, respectively. The average fault coverage of all CUTs confirms that the multi-cycle test has a statistical improvement in fault detection for most benchmark circuits compared with scan testing (SCAN). Applying 4

and 6 capture cycles achieved the most fault coverage improvement, and the increment of fault coverage becomes less as the number of capture cycles increases to 8 and 10 cycles.

The above observations fit the basic feature of multi-cycle testing discussed in Section 3. Multiple capture operations would provide more detection opportunities for the fault that the scan-in pattern cannot detect. Therefore, it is possible to improve the fault detection of the scan-in pattern. However, the deterioration of testability of signal lines in the time-expanded circuit would interfere with future fault detection as increasing the capture cycles. To reinforce the effect of multi-cycle BIST on scan-in pattern reduction, CP insertion and FDS-FFs insertion are introduced, and their effects are described as follows.

5.2 Evaluation of the efficiency of the CPI and the OPI

We conducted the CP selecting and OP pruning algorithm proposed in Section 5 on the benchmark circuits to identify a specified amount of CPs and FDS-FFs, where the maximum number of CPs N_{cp} was set to 1% of the gate number of CUT, and 5% of the FFs, respectively. The expected amount of FDS-FFs is set to 20% of the total number of FFs in the CUT. The number of CPs and FDS-FFs are shown in the fifth and the sixth column of Table 2, respectively. To demonstrate the difference between OPI and CPI, we performed fault simulation under 10 cycles by individually inserting the identified CPs and OPs into the CUTs, denoted by CP-ONLY and OP-ONLY, respectively. CPI&OPI denotes inserting both the CPs and OPs into the CUTs. Figure 10 shows the curve of average fault coverage of the benchmark circuits, increasing scan-in patterns to 100K under different DFT strategies. The figure only presents the curves up to 50K patterns for demonstration. Full observation replaces all FF with FDS-FFs has been conducted on the CUTs w/(w/o) CP insertion denoted by FullOB, CP&FullOB, respectively. While it is not for practical use due to hardware overhead concerns, the results represent the upper bound of the fault coverage possibly achieved by OPI, which is used to evaluate how far the OP pruning has reached in identifying the OPs for FDS-FFs insertion.

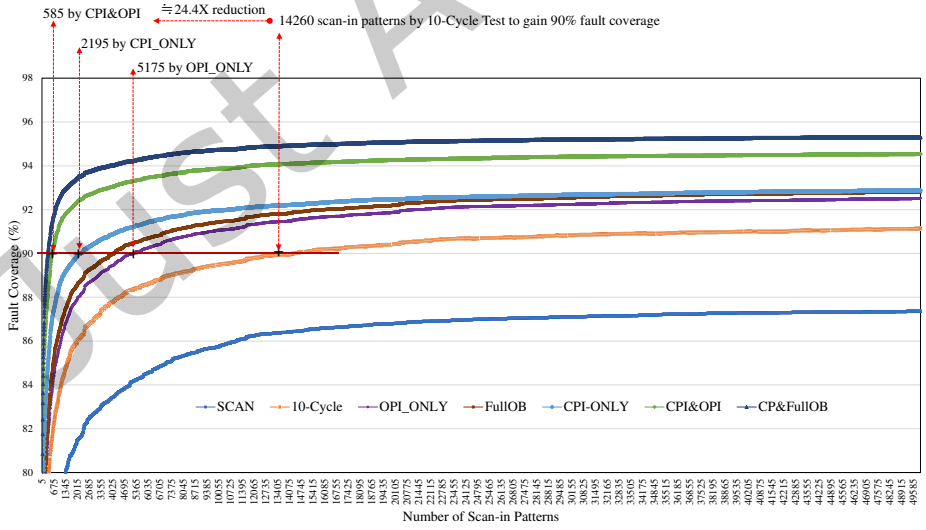


Figure 10: Fault coverage vs. Pattern number (scan testing, multi-cycle testing, OPI and CPI under multi-cycle testing).

Compared to the regular scan test (SCAN), the multi-cycle test w/o TPI denoted by *"10-Cycle"* in the figure achieved a significant fault coverage improvement where a target fault coverage (90%) is attained by applying 14,260 scan-in patterns under a 10-cycle test, which cannot be achieved by scan testing even with more than 100K scan-in patterns. Replacing 20% of FFs with FDS-FFs (OPI-ONLY) further improved the fault coverage and reduced the necessary scan-in patterns to 5,175 for the target 90% fault coverage as well as the effect achieved by full observation (replacing all scan FFs with FDS-FFs). The results demonstrate the effect of FDS-FFs insertion that directly observes the values of FFs at each capture cycle to relax the fault masking problem in the time-expanded circuit.

Note the fault coverage curve of CPI-ONLY in Figure 10, where we inserted 1% of the gate number of CPs into the CUTs, and it shows almost the same fault coverage improvement (≈93%) and much more scan-in pattern reduction (2,195 for 90% fault coverage) than that of OPI-ONLY. The results indicate 1) inserting Self-Flipping CP into the CUT that relaxes the controllability bias in a time-expanded circuit is helpful in improving the fault detection of capture patterns 2) the effect of CPI is limited due to the fault masking problem in the time-expanded circuit. When inserting both the identified CPs and OPs into the CUTs denoted by CPI&OPI, we achieved a sharp increase in fault coverage compared to inserting CPs and OPs individually. The final fault coverage of 100K scan-in patterns increases to 95.01%. The number of scan-in patterns for achieving 90% fault coverage is drastically reduced to 585 (24.4X reduction compared to the multi-cycle test). Note the fault coverage curve of 10-cycle (multi-cycle test) and the CP&FullOB, which represents the upper bound of the fault coverage possibly achieved by CPI&OPI, inserting both the CPs and OPs (CPI&OPI) identified by our proposed method achieved remarkable fault coverage increase and pattern reduction that is very close to the upper bound.

Table 3 and Table 4 show the detailed results of the final fault coverage achieved by applying 100K patterns and the number of scan-in patterns for attaining 90% stuck-at fault coverage, respectively. The experimental results when inserting fewer CPs (<5% of FFs) into the benchmark circuits are also presented in the tables. The results show that the 10-cycle test would cause the fault coverage loss in most ISCAS89 circuits (s9234, s13207, s38584); however, it achieves a significant increase in ITC99 benchmark circuits. Where ISCAS89 circuits show a much more testability bias, increasing the capture cycles are vulnerable to fault masking and FDD problem. While inserting OP or CP individually both improved the fault coverage and reduce the patterns for attaining 90% fault coverage for all circuits, it suggests that combining the CPs and OPs can achieve the most pattern reduction under the multi-cycle BIST scheme. Reducing the number of CPs causes a corresponding degradation in the fault coverage and the scan-in pattern reduction, however, the degradation is small, e.g., when reducing the number of CPs from 201 to 70 for the b17 circuit, the fault coverage with 100k patterns decreased from 97.81% to 96.29%, scan-in patterns for 90% fault coverage increased from 130 to 185. The reduction of scan-in patterns compared to the multi-cycle test is remarkable for shortening the TAT of POST with less hardware overhead.

Table 3: The final fault coverage reached by 100K scan-in patterns

Circuit	Design for Testability Approaches											
	SCAN	10Cycle	OPI_ONLY	FullOB	# of CP<1% of gates				# of CP<5% of FFs			
					# of CPs	CPI-ONLY	CPI&OPI	CP&FullOB	# of CPs	CPI-ONLY	CPI&OPI	CP&FullOB
s9234	87.31	84.94	89.94	90.00	55	82.69	89.68	91.80	11	83.3	87.96	88.02
s13207	90.47	84.81	92.20	92.96	79	86.16	92.75	93.89	33	85.6	90.1	91.01
s15850	87.51	87.73	88.48	90.18	104	85.09	87.41	91.52	29	86.47	87.71	90.77
s38417	95.16	97.52	97.96	98.03	141	98.19	98.66	98.72	85	98.00	98.55	98.62
s38584	91.31	90.81	91.59	92.07	97	91.16	91.70	92.28	72	90.27	90.93	91.53
b11	96.75	96.75	96.75	96.75	2	98.03	98.03	98.03	1	96.82	96.82	96.82
b12	97.28	98.64	98.68	98.68	9	99.18	99.21	99.21	6	97.6	97.6	97.64
b14	85.61	90.36	90.38	90.40	44	93.71	93.96	94.07	12	93.81	94.04	94.08
b15	69.75	92.94	92.95	92.95	8	98.35	98.36	98.36	8	98.35	98.36	98.36
b17	79.17	92.85	92.85	92.86	201	97.76	97.81	97.83	70	96.27	96.29	96.32
b20	84.69	89.52	89.66	89.69	88	93.10	93.61	93.94	24	92.68	93.17	93.22

Table 4: The number of scan-in patterns to achieve 90% fault coverage

Circuit	Design for Testability Approaches											
	SCAN	10-Cycle	OPI_ONLY	FullOB	# of CP<1% of total gates				# of CP<5% of FFs			
					# of CPs	CPI-ONLY	CPI&OPI	CP&FullOB	# of CPs	CPI-ONLY	CPI&OPI	CP&FullOB
s9234	>100K	>100K	>100K	>100K	55	>100K	>100K	9180	11	>100K	>100K	>100K
s13207	20560	>100K	11565	7375	79	>100K	6050	4175	33	>100K	59835	8885
s15850	>100K	>100K	>100K	68905	104	>100K	>100K	2380	29	>100K	>100K	4710
s38417	5780	1710	590	460	141	250	80	55	85	310	85	60
s38584	8180	10645	3700	1960	97	1555	575	305	72	12795	960	330
b11	475	120	120	120	2	45	40	35	1	115	115	105
b12	1280	175	170	170	9	100	45	45	6	260	210	195
b14	>100K	58280	58280	53425	44	1285	870	770	12	885	675	605
b15	>100K	4180	4180	4115	8	285	230	170	8	285	230	170
b17	>100K	4305	4300	4300	201	180	130	100	70	260	185	140
b20	>100K	>100K	>100K	>100K	88	4330	2045	935	24	7480	3740	3685

6 CONCLUSIONS

The multi-cycle BIST has room for improvement to reduce the volume of scan-in patterns. Therefore, this paper investigated the stuck-at fault detection model in the time-expanded circuit.

We revealed that the incompatibility between the controllability and observability of signal line as increasing the capture cycles would induce the fault masking and fault detection degradation problem. Those problems obstruct the effect of multi-cycle tests to test pattern reduction. We introduced the TPI technique to a multi-cycle LBIST scheme focused on reducing the volume of scan-in patterns for a target fault coverage to address this issue. The TPI approach replaces partial scan cells with FDS-FF referred to as OPI to enhance the observability and inserts Self-Flipping control logic into the combinational logic referred to as CPI to relax the controllability bias of signal lines of CUT at the intermediate capture cycles.

To identify the TPs that could achieve the most scan-in pattern reduction, we proposed a metric called the CD (the degree of contribution to relax the controllability) to evaluate the effect of candidate CPI signal lines and introduced an improved probabilistic cost function for estimating the effect of CP and OP insertion under multi-cycle BIST scheme. A TPI procedure including CP insertion and OP pruning is also proposed to identify the effective TPs to achieve the most scan-in pattern reduction. The experimental results on ISCAS89 and ITC99 benchmarks show 24.4X pattern reduction on average that confirming the effectiveness of the proposed TPI for shortening the test application time of POST.

In future work, we will implement the proposed TP selection algorithm to support the industrial design with Renesas Electronics Corp. to evaluate the effectiveness of the multi-cycle LBIST scheme on the commercial automotive MCUs.

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REFERENCES

[1] ISO26262-5:2011. Road vehicles - Functional Safety - Part 5: Product development at the hardware level. Retrieved Sept. 1, 2021 from https://www.iso.org/obp/ui/#iso:std:iso:26262:-5:ed-1:v1:en

[2] Patrick Girard, Nicola Nicolici and Xiaoqing Wen. 2010. Power-Aware Testing and Test Strategies for Low Power Devices. Springer, ISBN 978-1-4419-0927-5. New York, USA.

[3] K. Ichino, T. Asakawa, S. Fukumoto, K. Iwasaki and S. Kajihara. 2001. Hybrid BIST using partially rotational scan. in Proc. ATS, pp. 379-384.

[4] S. Narayanan, R. Gupta, M. A. Breuer: "Optimal Configuring of Multiple Scan Chains", IEEE Trans. on Comp., Sep. 1993, pp.1121-1131

[5] J. Rajski, J. Tyszer, M. Kassab and N. Mukherjee. 2004. Embedded deterministic test. in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, no. 5, pp. 776-792. https://doi: 10.1109/TCAD.2004.826558.

[6] G. Kiefer, H. Vranken, E.-J. Marinissen and H.-J. Wunderlich. 2000. Application of deterministic logic BIST on industrial circuits. in Proc. Intl. Test Conf. (ITC). pp. 105-114.

[7] R. Kapur, S. Patil, T.J. Snethen and T.W. Williams. 1996. A weighted random pattern test generation system. In IEEE Trans. CAD, vol. 15, no. 8, pp.1020-1025.

[8] A. Jas, C.V. Krishna and N.A. Touba. 2004. Weighted pseudorandom hybrid BIST. in IEEE Trans. VLSI, vol. 12, no. 12, pp. 1277-1283.

[9] N.A. Touba and E.J. McCluskey. 2001. Bit-fixing in pseudo-random sequences for scan BIST. in IEEE Trans. CAD, vol. 20, no. 4, pp. 545-555.

[10] H.-J. Wunderlich and G. Kiefer. 1996. Bit-flipping BIST. in Proc. ICCAD, pp. 337-343.

[11] S. Hellebrand, J. Rajski, S. Tarnick, S. Venkataraman and B. Courtois. 1995. Built-in test for circuits with scan based on reseeding of multiple-polynomial linear feedback shift registers. in IEEE Trans. Comput., vol. 44, no.2, pp. 223-233.

[12] C. V. Krishna, A. Jas and N. A. Touba. 2001. Test Vector Encoding Using Partial LFSR Reseeding," in Proc. Intl. Test Conf. (ITC), Baltimore, MD, USA, pp. 885–893.

[13] Pomeranz. 2017. Computation of Seeds for LFSR-Based n-Detection Test Generation. ACM Trans. Des. Autom. Electron. Syst., vol. 22, no. 2, pp. 29:1–29:13.

[14] P. Hayes and A. D. Friedman. 1974. Test Point Placement to Simplify Fault Detection. IEEE Trans. Comput., vol. C–23, no. 7, pp. 727–735.

[15] A.J. Briers and K. A. E. Totton. 1986. Random Pattern Testability by Fast Fault Simulation," in Proc. Intl. Test Conf. (ITC), Washington, DC, USA, pp. 274–281.

[16] H. Vranken, F. S. Sapei and H.-J. Wunderlich. 2004. Impact of Test Point Insertion on Silicon Area and Timing During Layout. in Proc. Design, Automation and Test in Europe Conf. (DATE). Paris, France.

[17] O. Novak and J. Nosek. 2001. Test-per-clock testing of the circuits with scan. Proc. Int. On-Line Test Workshop, pp. 90-92.

[18] S. Milewski, N. Mukherjee, J. Rajski, J. Solecki, J. Tyszer, and J. Zawada. 2017. Full-scan LBIST with capture-per-cycle hybrid test points. in Proc. Intl. Test Conf. (ITC), paper 10.3.

[19] F. Zhang, D. Hwong, Y. Sun, A. Garcia, S. Alhelaly, G. Shofner, L. Winemberg, and J. Dworak. 2016. Putting wasted clock cycles to use: Enhancing fortuitous cell-aware fault detection with scan shift capture. in Proc. Intl. Test Conf. (ITC), paper 2.3.

[20] G. Mrugalski, J. Rajski, J. Solecki, J. Tyszer, and C. Wang. 2017. Trimodal scan-based test paradigm. in IEEE Trans. VLSI Systems, vol. 25, no. 3,

pp. 1112-1125.

[21] Y. Liu, N. Mukherjee, J. Rajski, S. M. Reddy and J. Tyszer. 2020. Deterministic Stellar BIST for Automotive ICs. in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 8, pp. 1699-1710. https://doi: 10.1109/TCAD.2019.2925353.

[22] I. Pomeranz and S. M. Reddy. 1998. Static test compaction for scan-based designs to reduce test application time. In Proc. 7th Asian Test Symp. ATS, pp. 198-203.

[23] X. Lin and R. Thompson. 2003. Test generation for designs with multiple clocks. Proc. Design Autom. Conf., pp. 662-667.

[24] Seiji Kajihara, M. Matsuzono, H. Yamaguchi, Y. Sato, K. Miyase, and X. Wen. 2010. On Test Pattern Compaction with Multi-Cycle and Multi-Observation Scan Test. in Proc. Int'l. Symposium on Com. and Inf. Tech. (ISCIT), Tokyo, pp. 723-726. https://doi:10.1109/ISCIT.2010.5665084

[25] Y. Huang, I. Pomeranz, S. M. Reddy and J. Rajski. 2000. Improving the proportion of At-Speed Tests in Scan BIST. in Proc. Int'l. Conf. on Computer Aided Design, San Jose, pp. 459-463. https://DOI: 10.1109/ICCAD.2000.896514

[26] E. K. Moghaddam, J. Rajski, S. M. Reddy and M. Kassab. 2010. At-Speed Scan Test with Low Switching Activity. in Proc. IEEE 28th VLSI Test Symposium, Santa Cruz, pp.177-182. https://DOI: 10.1109/VTS.2010.5469580

[27] Y. Sato, S. Wang, T. Kato, K. Miyase and S. Kajihara. 2012. Low Power BIST for Scan-Shift and Capture Power. In Proc. IEEE Asian Test Symposium, Niigata, pp. 173-178. https://DOI: 10.1109/ATS.2012.27

[28] I. Pomeranz. 2021. Multicycle Tests with Fault Detection Test Data for Improved Logic Diagnosis. in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. https://doi: 10.1109/TCAD.2021.3079146.

[29] N. Devtaprasanna, A. Gunda, P. Krishnamurthy, S. M. Reddy, and I. Pomeranz. 2005. Methods for improving transition delay fault coverage using broadside tests. in *Proceedings of IEEE International Conference on Test*, pp.256-265. https://doi: 10.1109/TEST.2005.1583983.

[30] I. Pomeranz. 2014. Design-for-testability for multi-cycle broadside tests by holding of state variables. in ACM Transactions on Design Automation of Electronic Systems, vol. 19, issue 2, article 19, pp 1-20.

[31] I. Pomeranz. 2015. Enhanced Test Compaction for Multi-Cycle Broadside Tests By Using State Complementation. in ACM Transactions on Design Automation, November 2015, vol. 21, no. 1, article 13.

[32] S. Wang et al.. 2016. Structure-Based Methods for Selecting Fault-Detection-Strengthened FF under Multi-cycle Test with Sequential Observation. in Proc. IEEE Asian Test Symposium, Hiroshima, pp. 209-214. https://DOI: 10.1109/ATS.2016.40

[33] S. Wang, Y. Higami, H. Iwata, J. Matsushima and H. Takahashi. 2018. Automotive Functional Safety Assurance by POST with Sequential Observation. IEEE Design & Test Magazine. Vol.35, no.3, pp.39-45. https://DOI: 10.1109/MDAT.2018.2799801

[34] S. Wang, Y. Higami, H. Takahashi, H. Iwata, Y. Maeda and J. Matsushima. 2018. Fault-detection-strengthened method to enable the POST for very-large automotive MCU in compliance with ISO26262. in Proc. IEEE 23rd European Test Symposium, Bremen, pp. 1-2. https:// DOI: 10.1109/ETS.2018.8400707

[35] S. Wang, et al.. 2018. Capture-Pattern-Control to Address the Fault Detection Degradation Problem of Multi-Cycle Test in Logic BIST. in Proc. IEEE Asian Test Symposium, Hefei, pp.155-160. https://DOI:10.1109/ats.2018.00038

[36] H.T. Al-Awadhi, T. Aono, S. Wang, Y. Higami, H. Takahashi, H. Iwata, Y. Maeda, J. Matsushima. 2020. FF-Control Point Insertion (FF-CPI) to Overcome the Degradation of Fault Detection under Multi-Cycle Test for POST. IEICE Transactions on Information and Systems, Vol. E103.D, No. 11, pp. 2289-2301. https://DOI:10.1587/transinf.2019EDP7235

[37] P. K. Datla Jagannadha et al.. 2019. Special Session: In-System-Test (IST) Architecture for NVIDIA Drive-AGX Platforms. In IEEE 37th VLSI Test Symposium (VTS), pp. 1-8, https://doi: 10.1109/VTS.2019.8758636.

[38] G. Mrugalski, J. Rajski, J. Tyszer and B. Włodarczak. 2022. X-Masking for In-System Deterministic Test. in IEEE European Test Symposium (ETS), pp. 1-6. https://doi: 10.1109/ETS54262.2022.9810407.