Aging Monitoring for Memory-based Reconfigurable Logic Device (MRLD)

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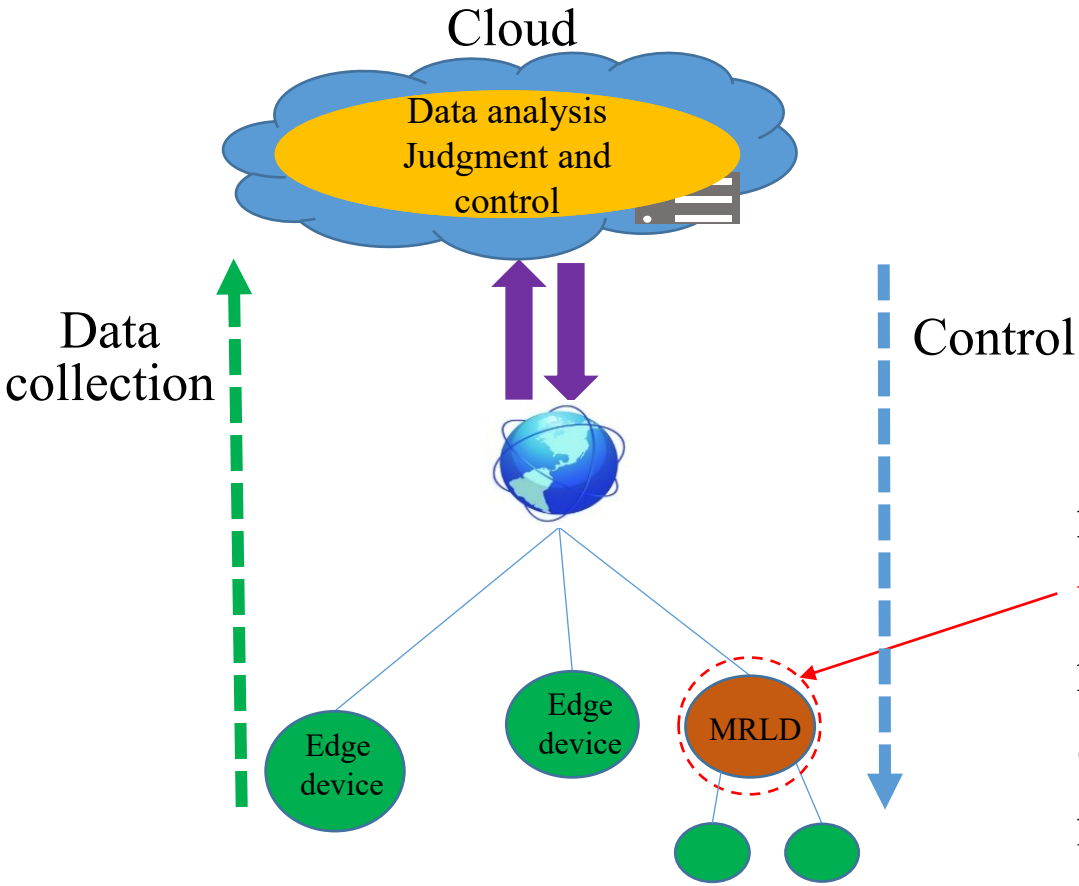
Outline

- Introduction
- What is MRLD
- Aging Issues in MRLD
- Aging monitoring Technique for MRLD
- Experimental results
- Conclusions

Background

- Recently, a reconfigurable logic device MRLD for next-generation IoT edge devices has been developed in order to analyze huge amounts of data in IoT in real-time.
- Field-test technology for detecting aging failures during the operation of MRLD devices has not been established.



In order to guarantee the high reliability of IoT systems, field-test technology that can detect and report the aging state of edge devices early during operation is necessary.

Purpose & Objective

- Purpose: Ensuring high reliability of IoT system

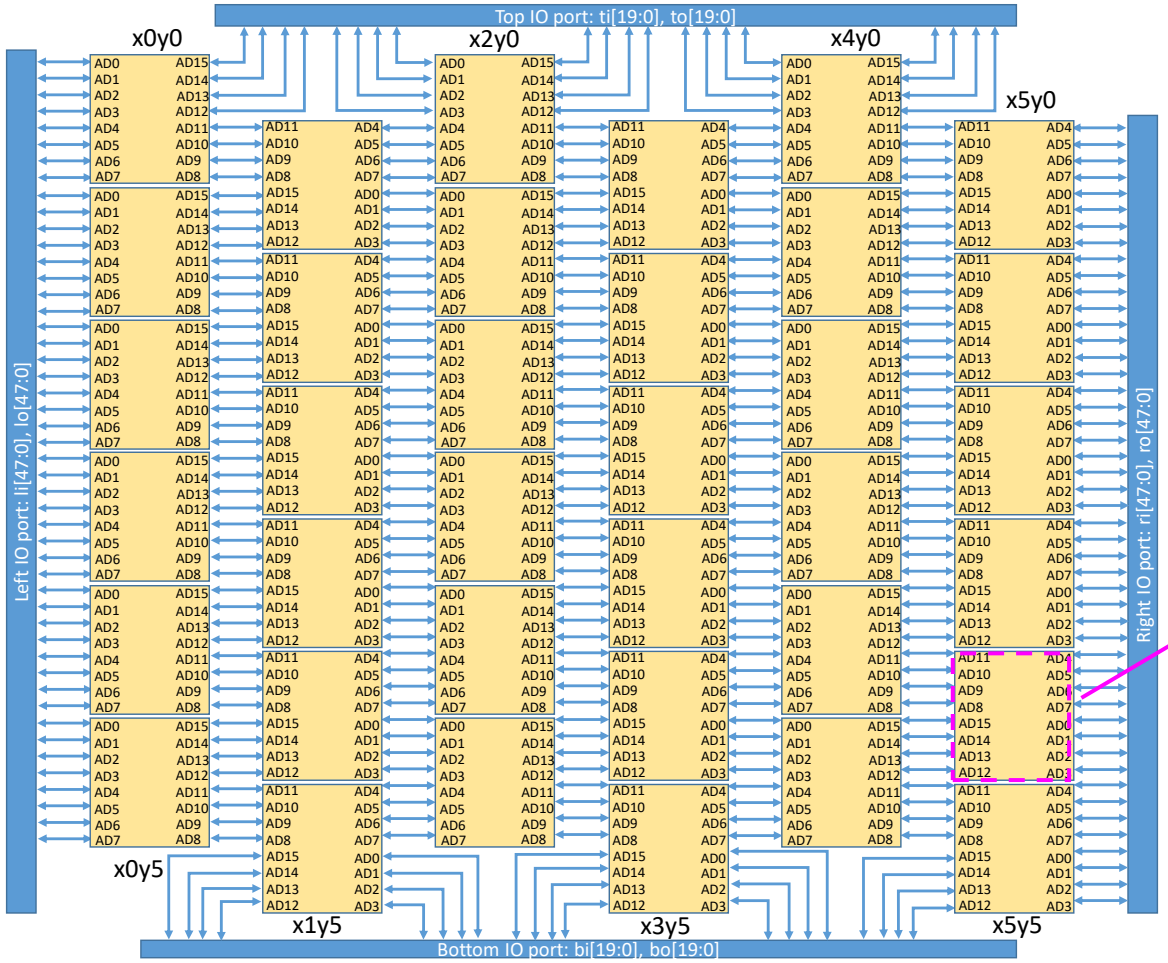
  Propose a method that can detect and report the aging statues of MRLD device during operation early

- Objective
  - Field test technology to measure the aging-induced delay

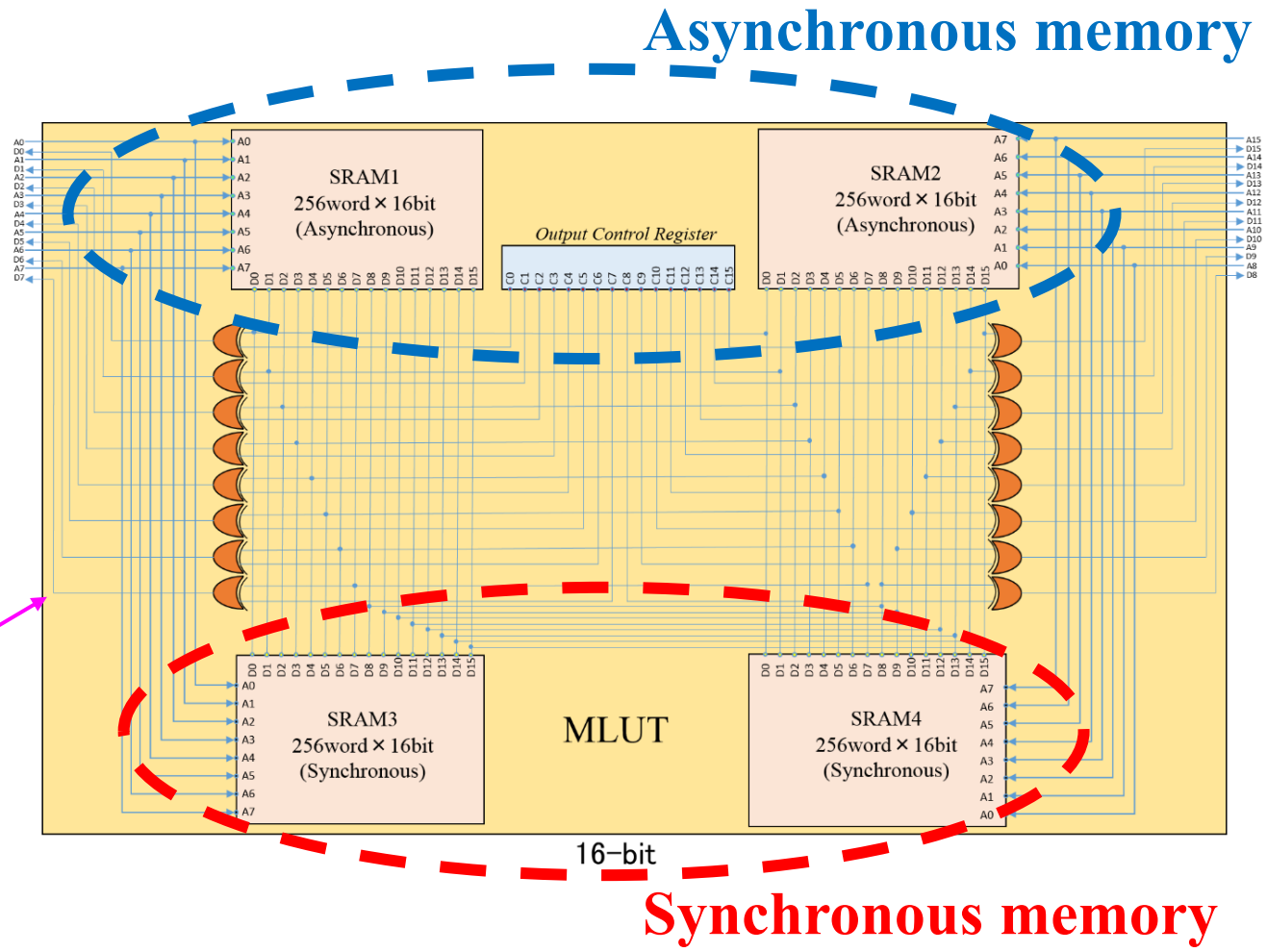
  Propose the design and implementation method of ring oscillator circuit adapt to the MRLD structure

What is MRLD

- An MRLD (Memory-based Reconfigurable Logic Device) is composed of multiple general-purpose memory cells (MLUTs: Multiple Look Up Tables) arranged in an array.
- Compared with existing technology FPGA, it has advantages of high speed, low power consumption, and low cost.

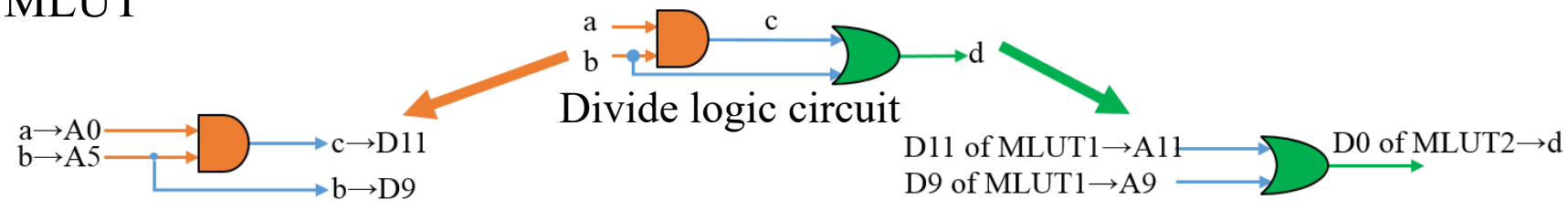


MRLD



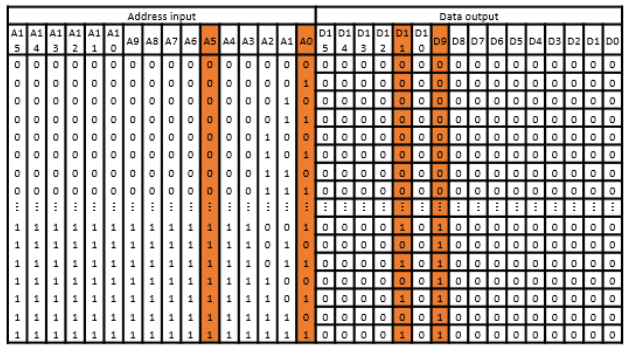
How an MRLD works

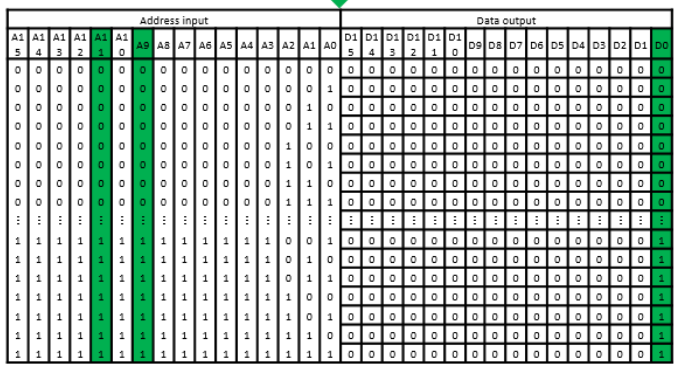
- Configure the logic circuit by writing the **truth table** of the logic circuit (including wiring logic) to the SRAM of MLUT



Crete truth table

Crete truth table





Write the truth table

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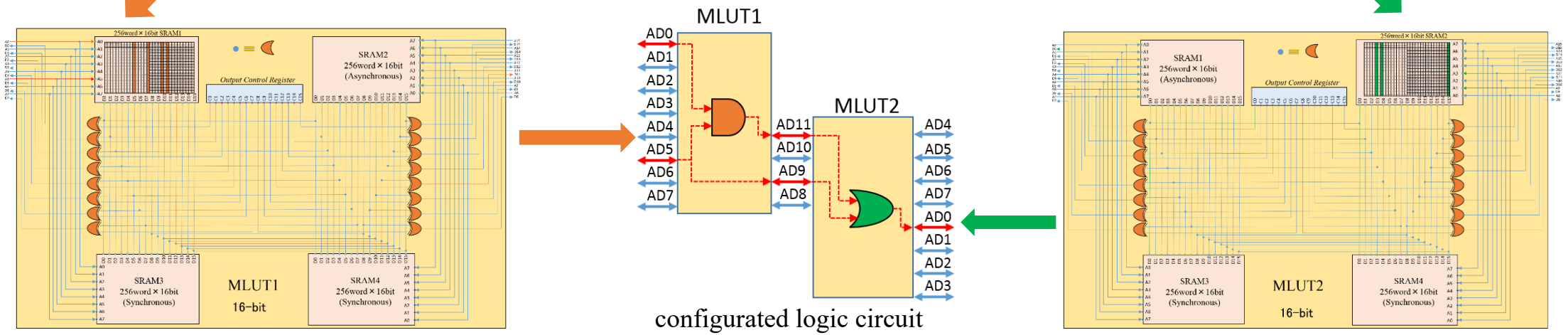
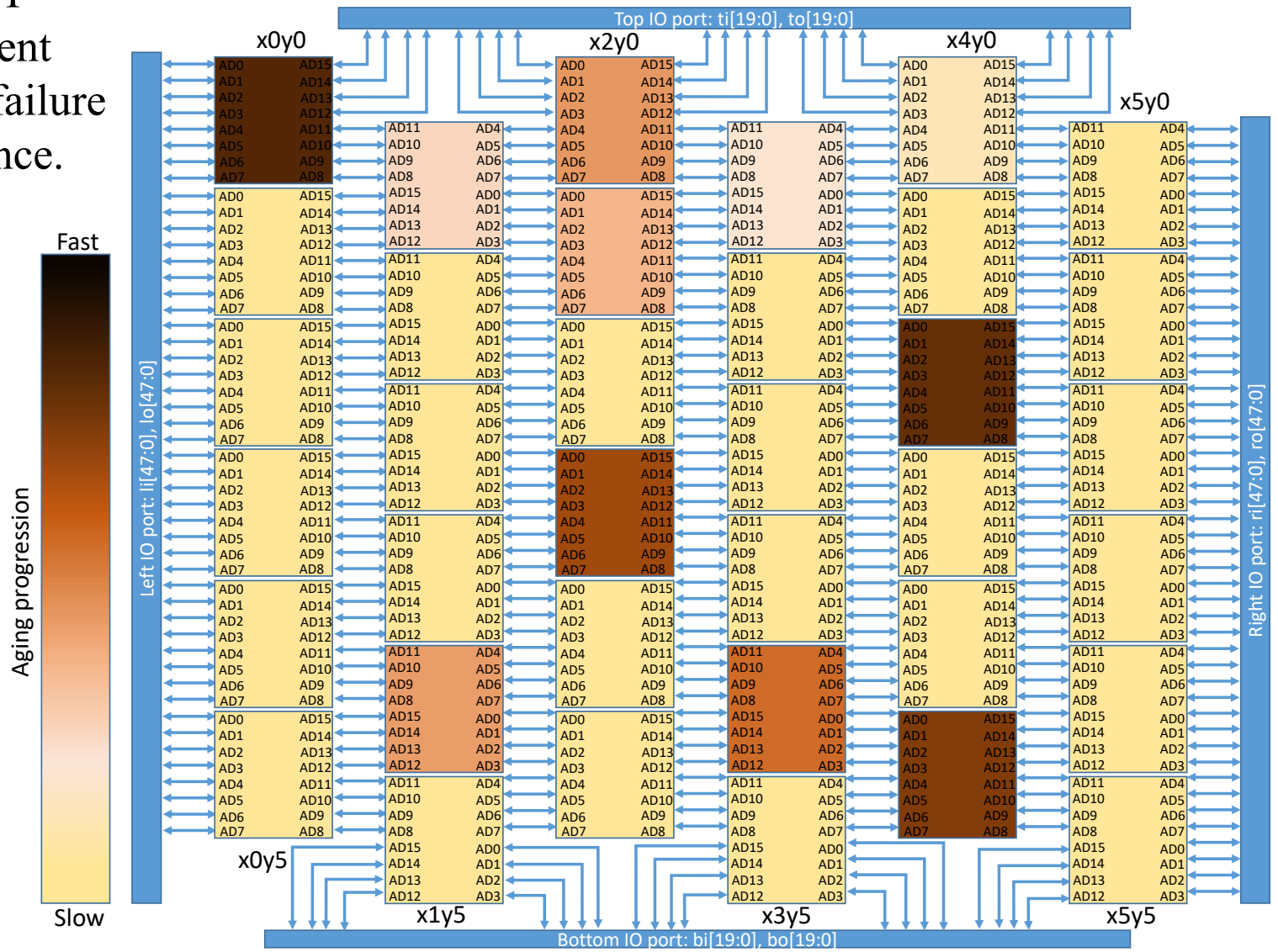


configurated logic circuit

Aging in MRLD

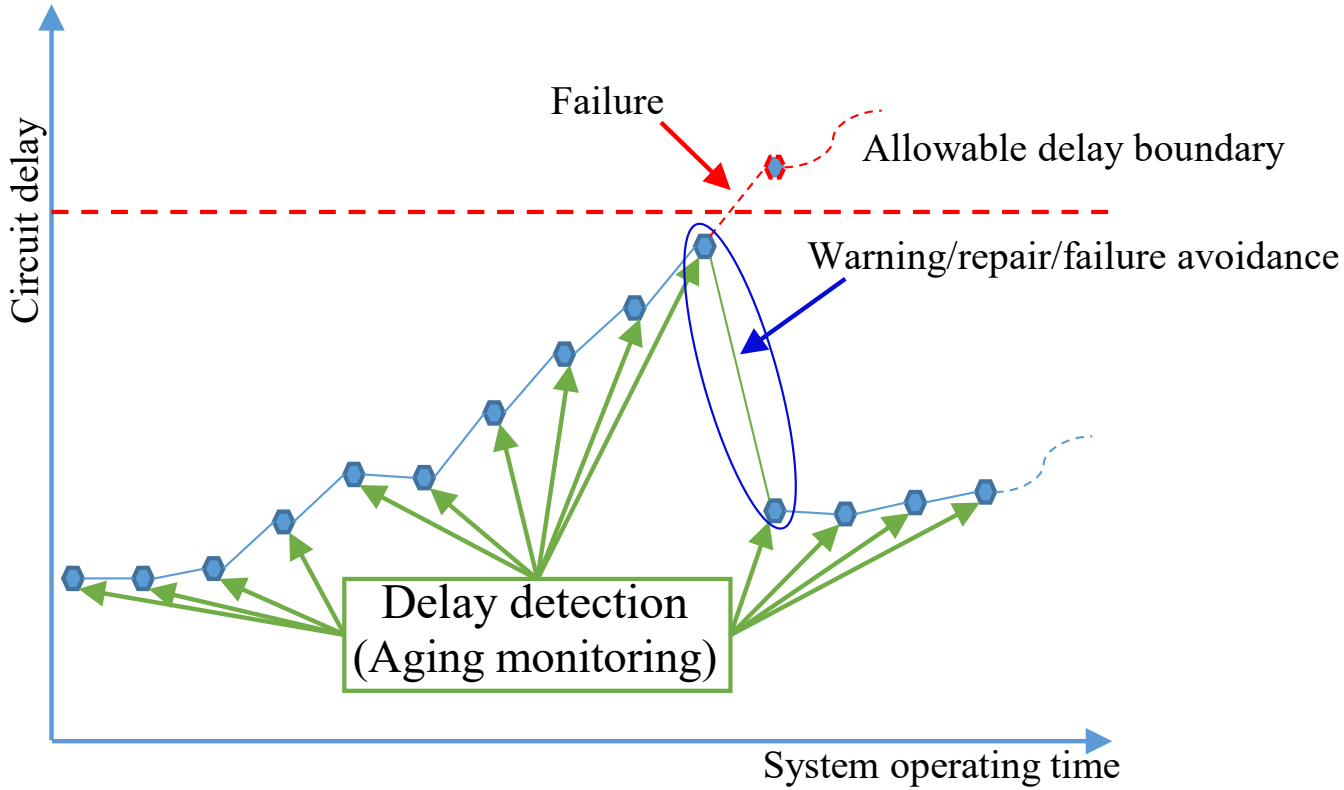
--Discussion of aging issues in MRLD

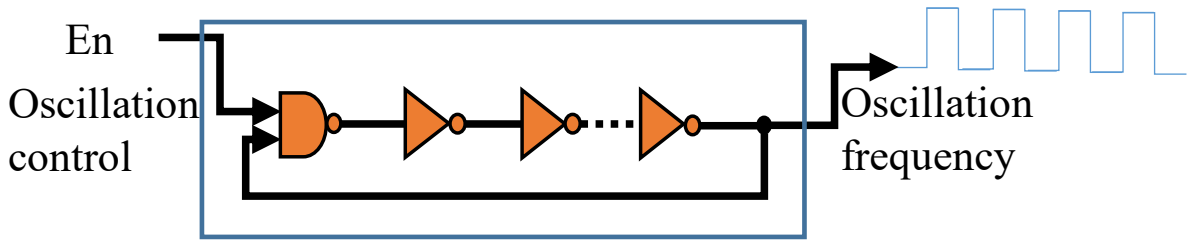
- Various aging phenomena such as HCI, BTI
- The progress of aging in MLUTs are different
- Aging-induced delay would affect system failure and the constructed logic circuit performance. (e.g.: sudden system down/reset)



Aging Monitoring in MRLD

- Delay Monitoring is an effective way to guarantee the reliability of an electronic device in field
- An early warning/report will be issued to the upper system to avoid a system failure or call for maintenances like repair/diagnosis
- Ring-Oscillator (RO) is commonly used as a sensor to monitor the delay variation of circuit affected by temperature, voltage, process or aging on the circuit





Aging Monitoring in MRLD

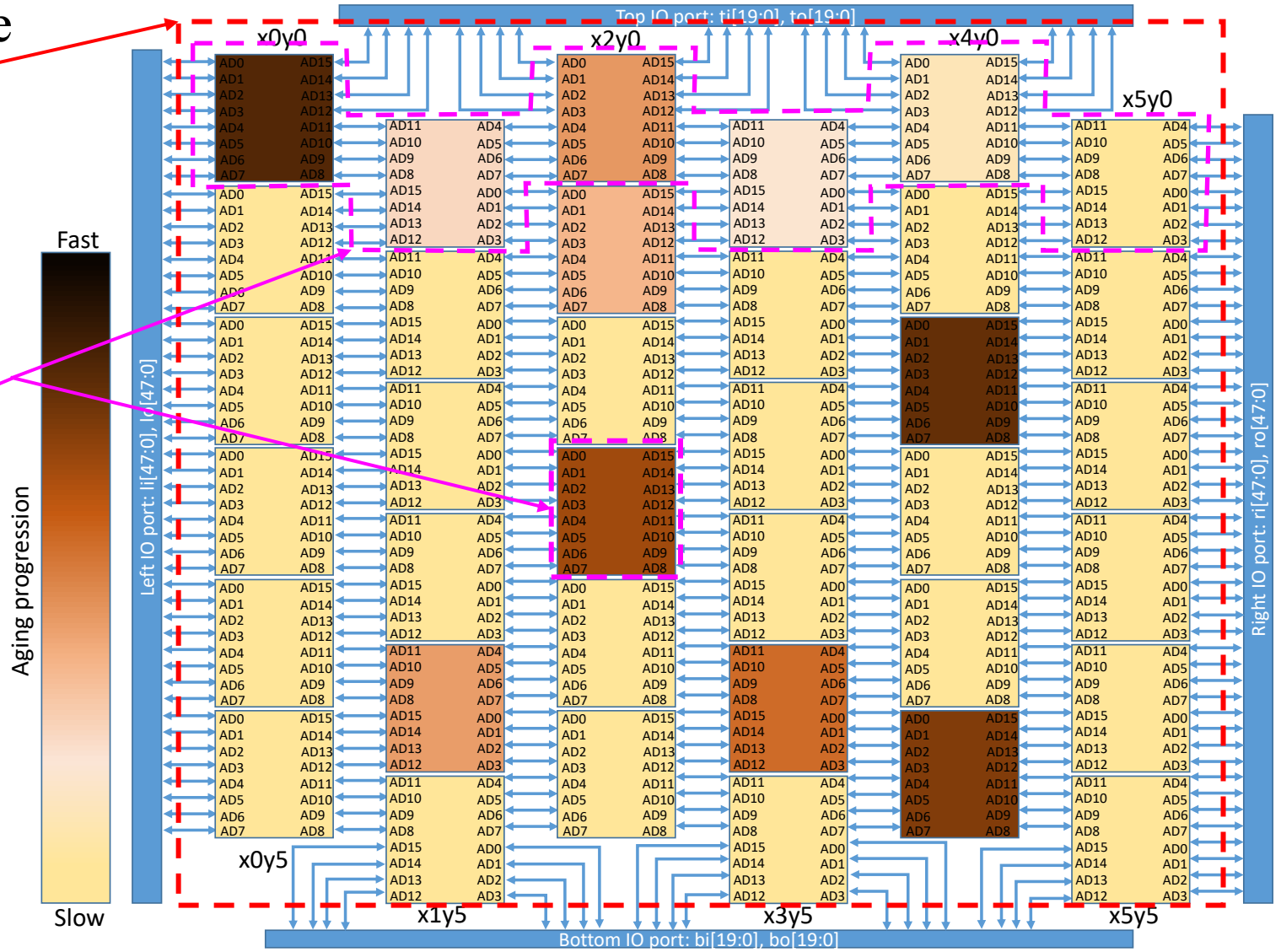
- The progress of aging in MLUTs are different

For performance

- Global Delay:
  - The Average Delay in overall MLUTs Array

To avoid highly degraded MLUTs

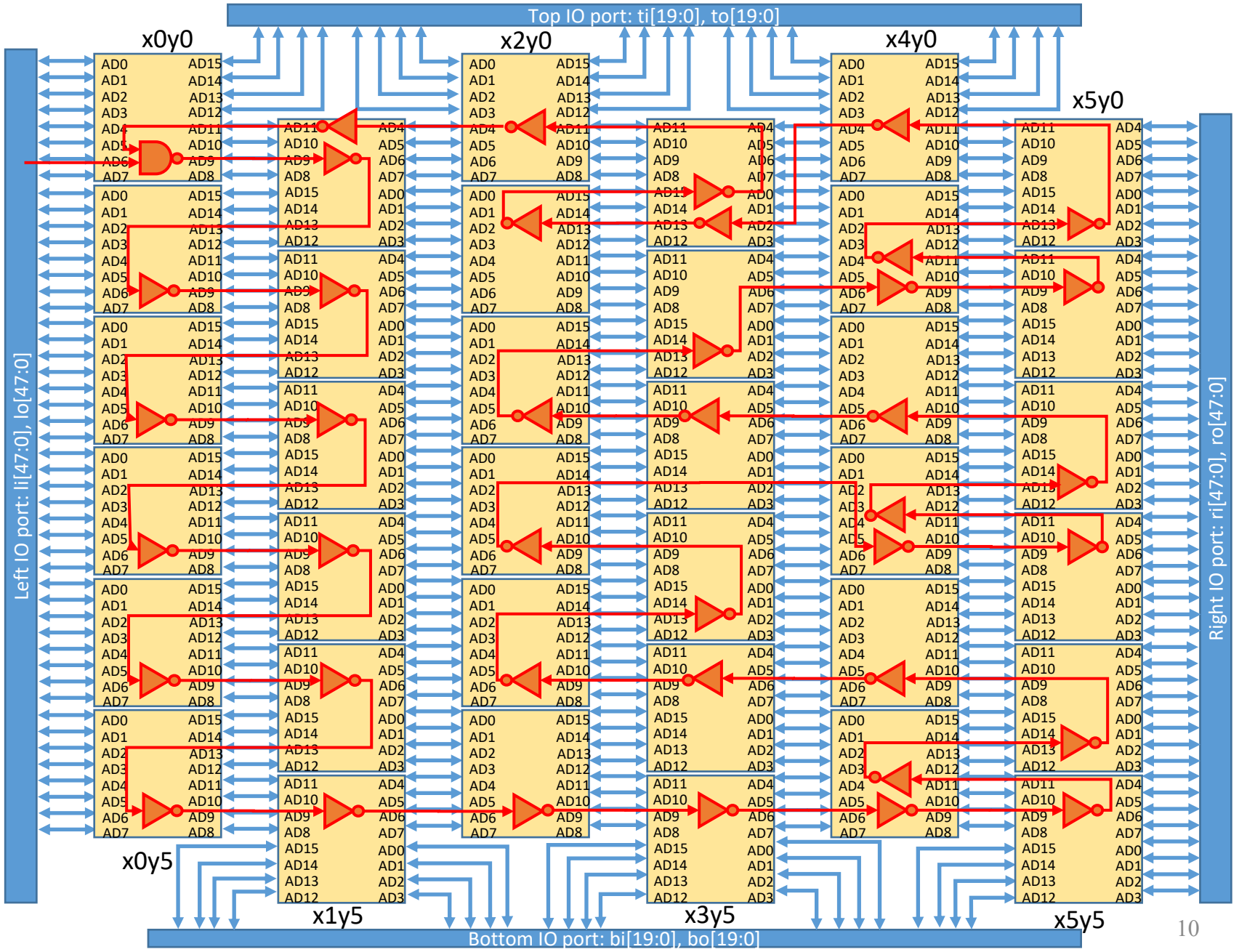
- Local Delay:
  - Delay at each Single MLUT (or Partial MLUTs Array)



RO implementation for Global Delay measurement

- RO circuit structure for Global Delay measurement

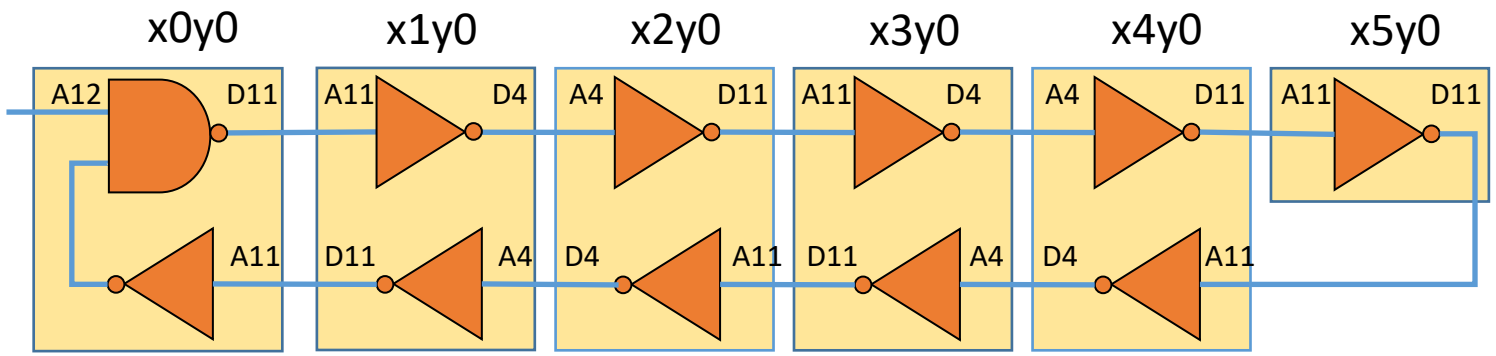
Place RO element (inverters) in individual MLUTs throughout the MLUT array



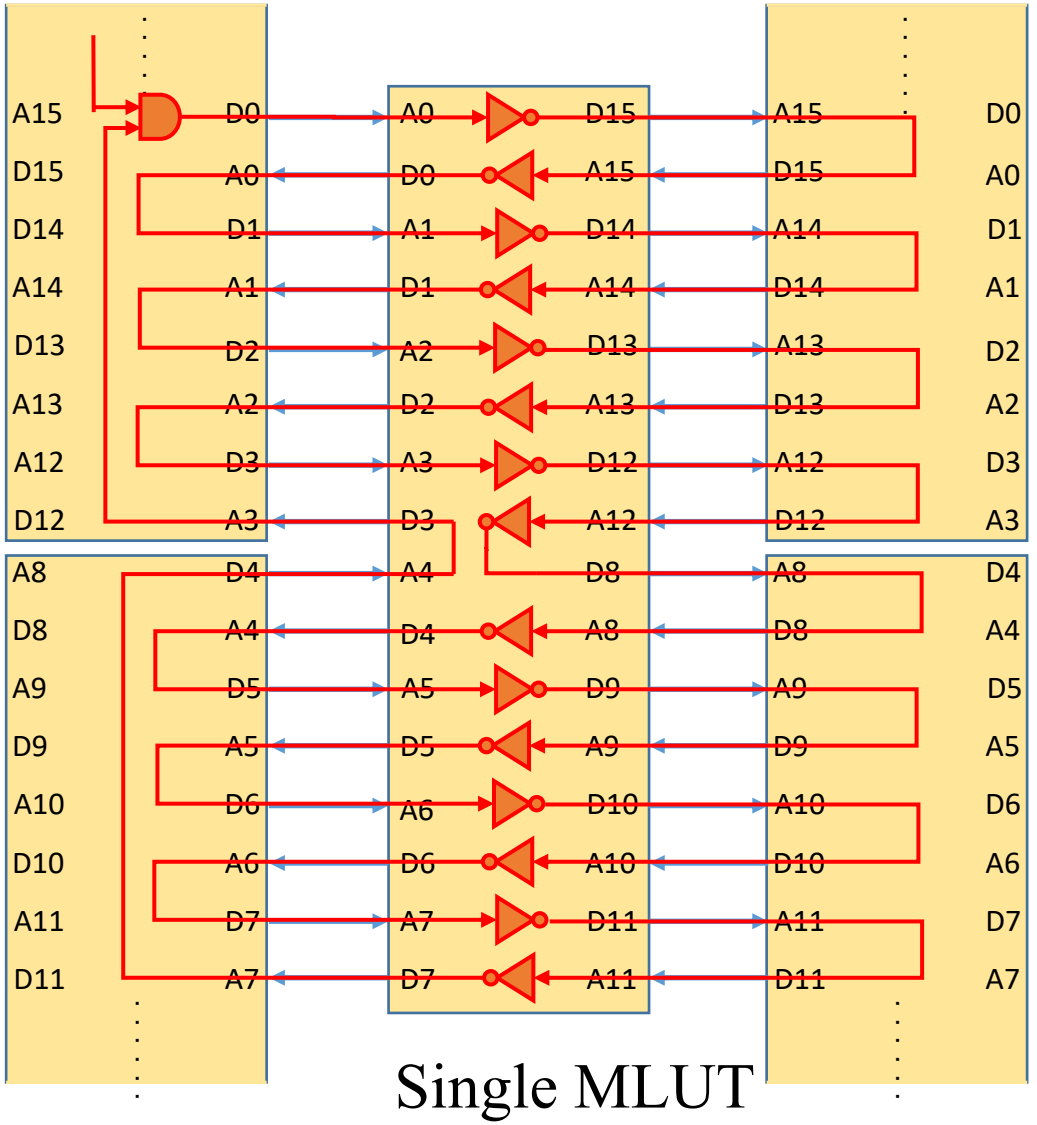
RO implementation method for Local Delay measurement

- RO circuit structure for Local Delay measurement

Place RO in single MLUT alone or partial MLUTs array in MRLD



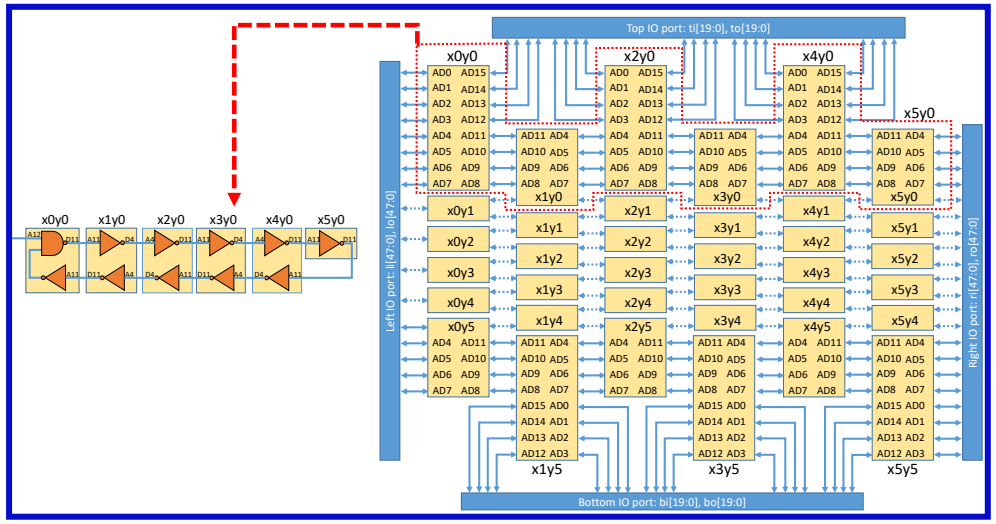
Partial MLUTs array

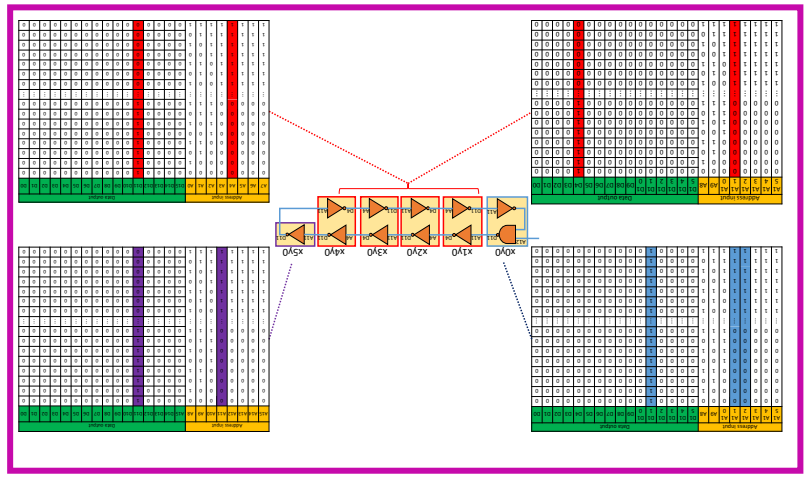


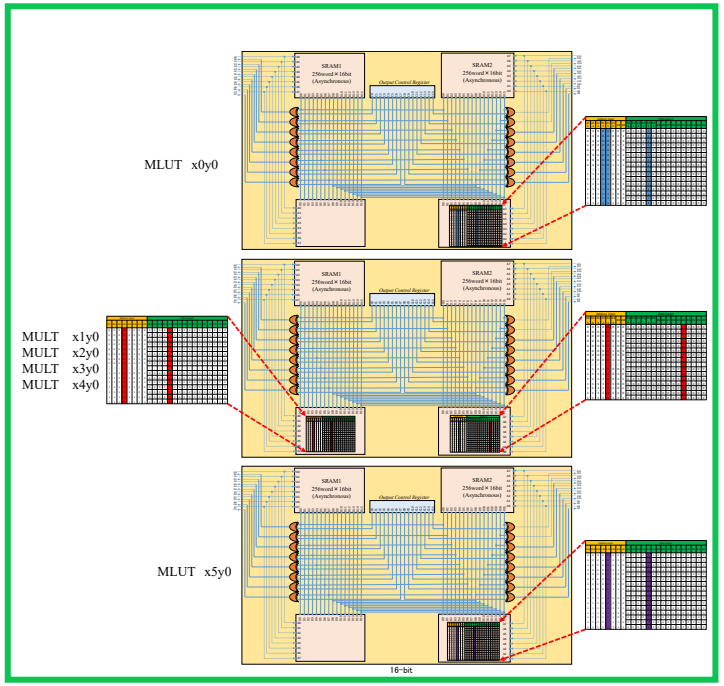
Single MLUT

RO implementation procedure in MRLD

- *Step 1. Select measurement area*
- *Step 2. Design the RO circuit structure and routing for the measurement area*
- *Step 3. Create the truth tables for the target MLUTs*
- *Step 4. Write the RO truth table to the corresponding MLUTs*
- *Step 5. Set the MRLD to logic operation mode, and observe the RO oscillation period from the external output for delay analysis*

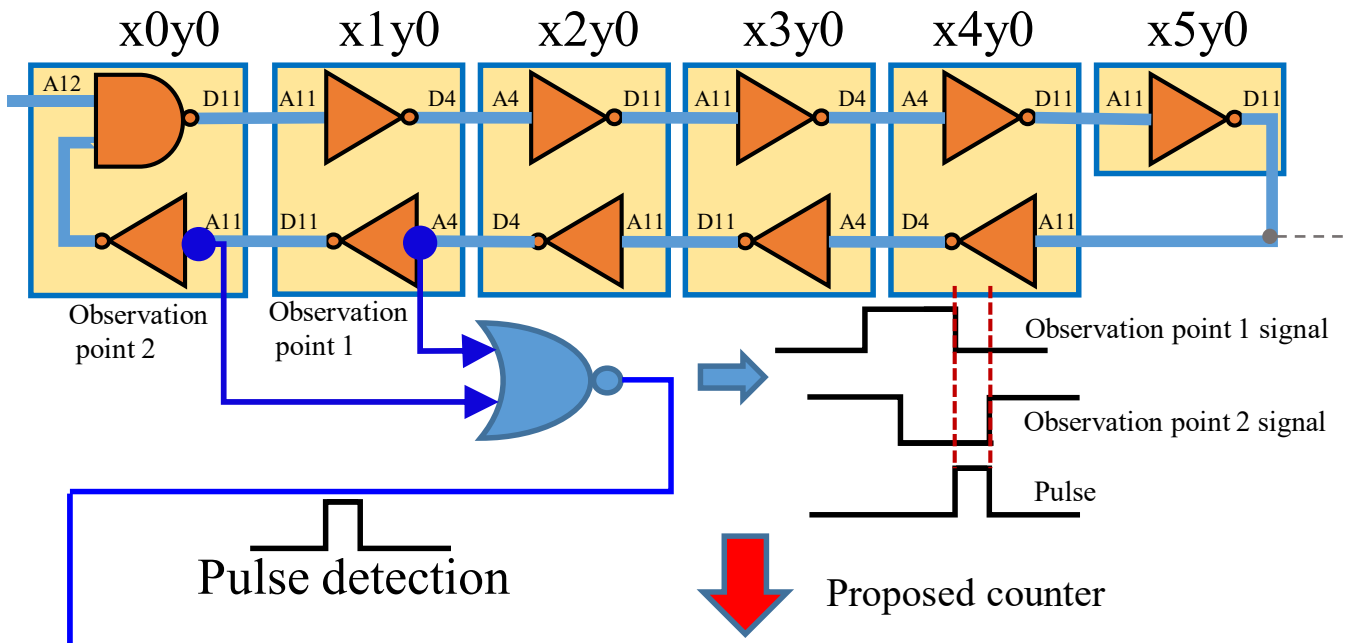


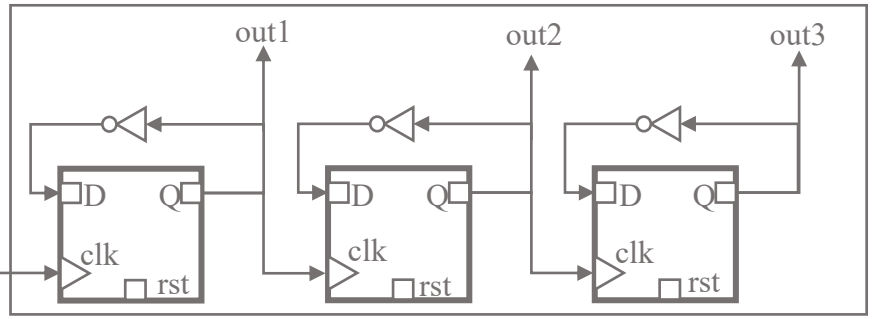




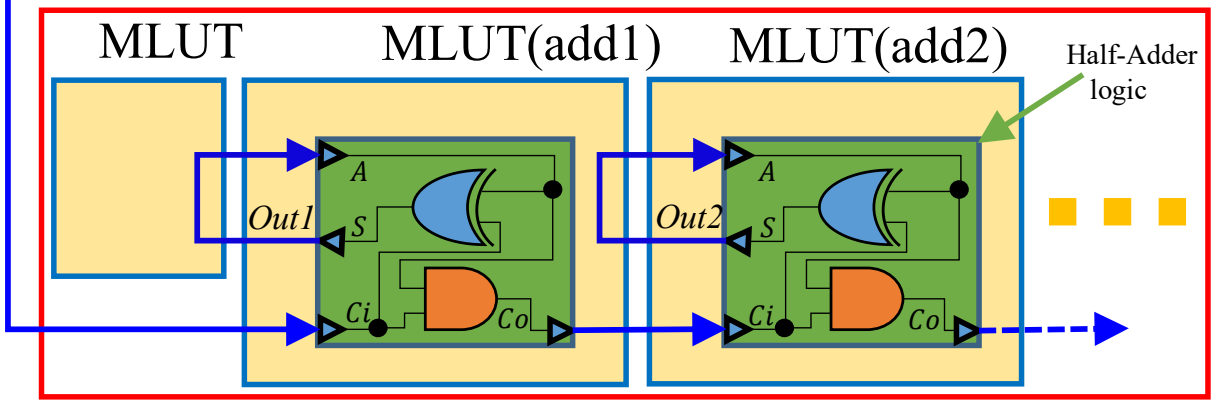
RO oscillation frequency counter in MRLD

- measure the delay of MLUT → measure the oscillation frequency of RO
- conventional counter design, cannot be configured in MLUTs: asynchronous Flip-Flops (FF) is required





Conventional counter



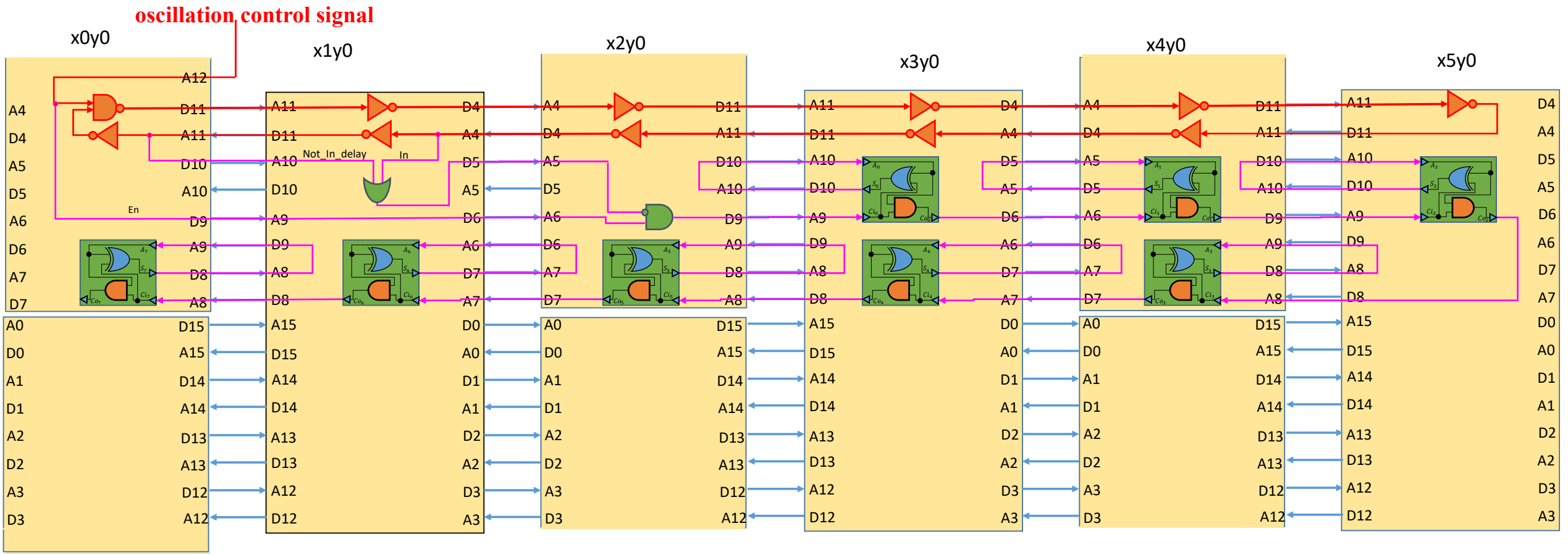
Proposed counter

$$Meas.Delay = \frac{T}{2 \times N \times F}$$

Where, T denotes the overall RO oscillation time, N denotes the stage number of RO, F denotes the number of pulses counted by the counter.

Experimental results -- implement RO circuit and counter into same MLUTs

- one 2-input NAND and 10 inverters
- 8-bit counter



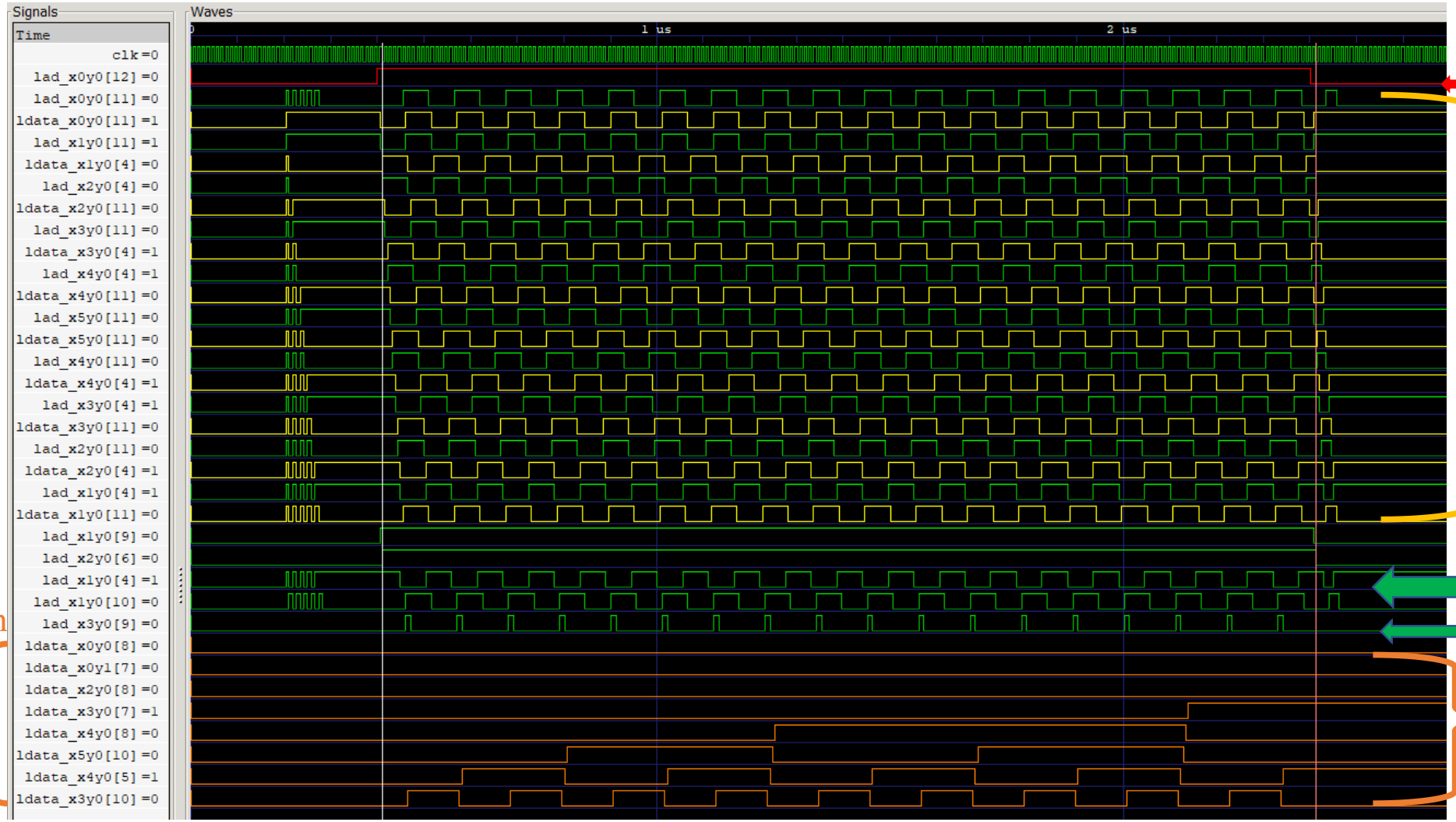
Since the proposed counter circuit has a simple structure, it can be constructed in the same MLUTs as RO → advantageous for saving LUT resources

Experimental results

--Simulation waveform to measure delay for MLUT

- The stage number of implemented RO is 10 (N=10)
- 8-bit counter implemented
- The read time of SRAM cell is set to 5.5ns
- The overall RO oscillation time T is set to 2us

$$Meas.Delay = \frac{T}{2 \times N \times F} = \frac{2000ns}{2 \times 10 \times 18} = 5.6ns$$



Counter waveform

Oscillation control signal = 1: oscillation

RO oscillation waveform

Observation point signal

Detected pulse

$(00010010)_2$ =$(18)_{10}$

The waveform of the RO oscillation and the counter

Conclusions

- Proposed the approach to monitor the aging of MRLD
- Proposed the design and implementation method of a ring oscillator circuit adapt to the structure of the MRLD device
- Design a counter to store the RO oscillation frequency
- Proposed method can effectively measure the delay of the MLUT with very small error
- In our future work, we will make a quantitative analysis on the aging phenomena, and develop a precise simulation method as well as on-chip test method

Thank you for your listening