5.3.1

Since there are 5 bits for the block offset, there are 2^5=32 bytes. Given four bytes is one word, there are 8 words in a block.

5.3.2

Since it is a direct mapped cache, the number of indexes corresponds to the number of entries. There are 5 bits for the indexes, so there are 2^5=32 entries in total.

5.3.4

ADDRESS	TAG	INDEX	HIT OT MISS	REPLACED OR NOT
0	0	0	miss	-
4	0	0	hit	-
16	0	0	hit	-
132	0	100	miss	-
232	0	111	miss	-
160	0	101	miss	-
1024	1	0	miss	replace
30	0	0	miss	replace
140	0	100	hit	-
3100	11	0	miss	replace
180	0	101	hit	-
2180	10	100	miss	replace

So 4 blocks are replaced in total.

5.3.5.

The hit ratio is 4/12, which is 1/3.

5.5.1

The block size of 32 bytes can take 16 byte addresses without having a miss, and then it will have a compulsory miss. So the miss rate is 1/16, the miss rate will decrease if we have larger cache block size, and the kind of miss we experience is compulsory miss.

5.5.2

The miss rate will be 1/(16/2)=1/8, 1/(64/2)=1/32,and 1/(128/2)=1/64, respectively. The locality we are exploiting is spatial locality.

5.6.2

For L1: 0.66+0.08*70=6.26 ns

For L2: 0.9+0.06*70=5.1 ns

5.6.4

0.66+ 0.08*(5.62+0.95*70)=6.4296ns > 6.26ns

So AMAT is worse with the L2 cache.

TCPI

a.

AMAT-instruction: 1+0.1*(10+0.2*80)=3.6 cycles

AMAT-data: 1+0.3*(10+0.2*80)=8.8 cycles

AMAT= (1/1.2)*3.6+(0.2/1.2)*8.8= 4.467 cycles

b.

BCPI: 1+0.2*0.6*1+0.3*0.5*1=1.27 cycles

MCPI: 0.1*(10+0.2*80)+0.2*0.3*(10+0.2*80)=4.16 cycles

TCPI=BCPI+MCPI= 5.43 cycles

c.

By in-lining, 1/6+1/6=1/3 branch instructions are reduced, including jal and jr.

New instruction count is 1M*(1-0.3*1/3)=0.9 M

Now load constitutes 0.2M/0.9M=2/9 of total instructions.

New bad branch predictions are 0.3*0.5*1M- 0.1M=0.05M instructions

New bad branch prediction percentage is 0.05/0.9=1/18

New BCPI=1+(2/9)*0.6*1+(1/18)*1=107/90 cycles

Let instruction cache miss rate be X.

New MCPI= X*(10+0.2*80)+(2/9)*0.3*(10+0.2*80)=78/45+26X

Given new ET<= old ET

0.9M*(107/90+78/45+26X) <= 1M*5.43

Solving the inequality we get X <= 0.119658

So instruction cache miss rate must be <= 0.119658