EE 111L lab 1

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1. Objective

The objective of this lab is to explore the behavior of sinusoidal steady state circuit. In the first part of the experiment, we worked on first order circuits and observe how different components, such as inductor, resistor and capacitor interact in a sinusoidal steady state circuit. In the second part of the experiment, we try to verify the maximum power transfer in a sinusoidal steady state circuit.

2. Experiment: Frequency domain analysis of 1st-order circuits

2.1. Theory

For a sinusoidal steady state circuit, we convert use impedance of the components and convert the equation into a phasor equation. For the resistor voltage in figure 1 below, if we assume Vs= A*sin wt,

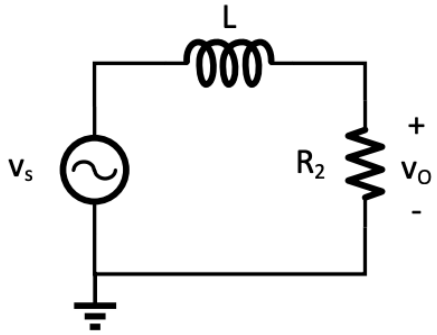


Figure 1. a first order circuit of resistor and inductor

We can write phasor equation as:

$$V0 = Vi * \frac{Z2}{Z1 + Z2} = -jA\frac{R}{R + jLw} = |V0|\cos(wt + \varphi)$$

Solving this equation, we can express the magnitude of V0 as:

$$|V0| = \left|-jA\frac{R}{R + jLw}\right| = \frac{AR}{\sqrt{R^2 + (Lw)^2}}$$

Similarly, the inductor voltage in figure 1 can be expressed as

$$|V_L| = \left|-jA\frac{jLw}{R + jLw}\right| = \frac{wLA}{\sqrt{R^2 + (Lw)^2}}$$

For topology of figure 2 as below,

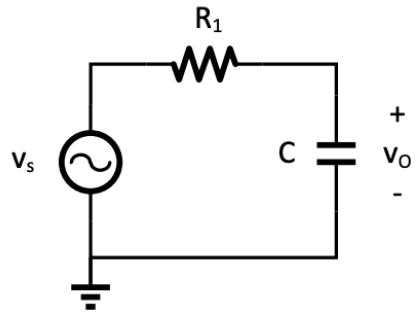


Figure 2. a first order circuit of resistor and capacitor

We can apply the same technique and find voltage across capacitor as

$$|V_c| = \left|-jA\frac{1}{1+jCwR}\right| = \frac{A}{\sqrt{1+C^2w^2R^2}}$$

Similarly, the magnitude of voltage across the resistor in figure 2 is

$$|V_R| = \left|-jA\frac{jCwR}{1+jCwR}\right| = \frac{ARCw}{\sqrt{1+C^2w^2R^2}}$$

2.2 procedure

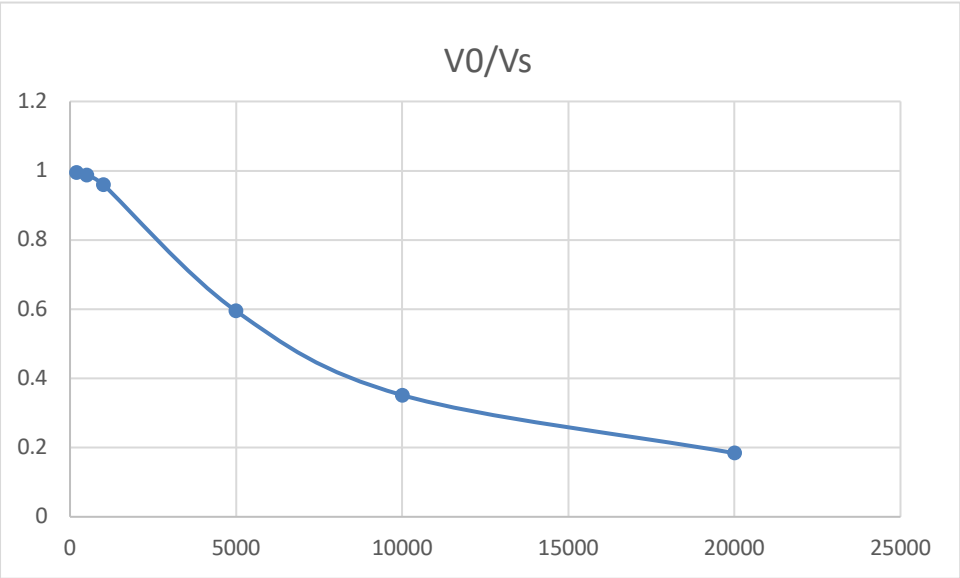
We connect the myDaq with the circuit topology, and use the analog input ports on myDaq to measure the voltage we are interested in. We use function generator to generate the sin wave, and use oscilloscope to measure amplitude and phase.

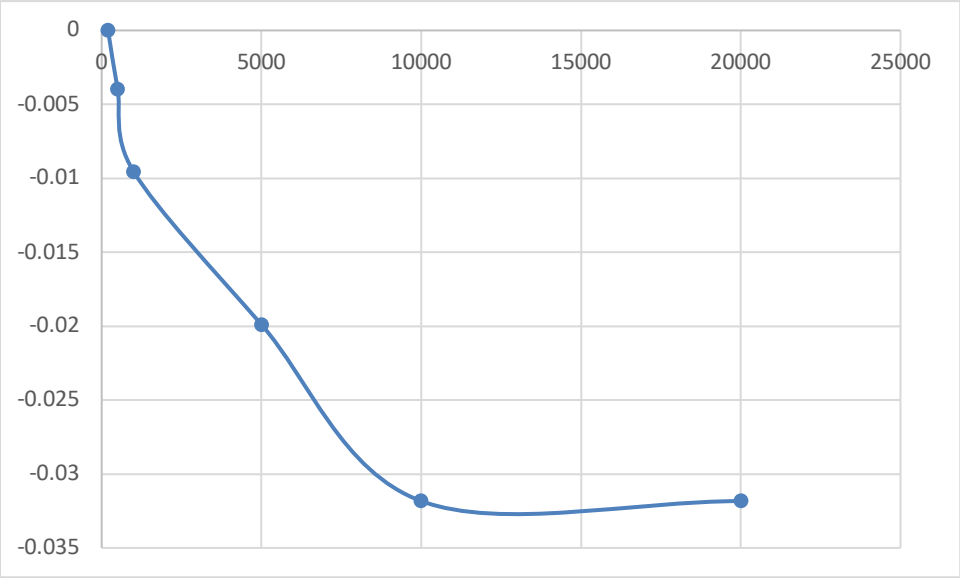
2.3 data

For measurements across capacitor in Figure 2 topology, we get

Frequency (Hz)	200	500	1k	5k	10k	20k
Ch0 output (mV)	200.91	200.43	200.43	199.81	196.47	189.38
Ch1 output (mV)	199.68	198.04	192.38	118.80	69.08	34.85
time between peaks (us)	0	50	60	25	20	10
Vo/Vs	0.993877	0.988075	0.959836	0.59456484	0.35160584	0.18402154
Angle V0/Vs	-7.17959E-09	-0.0039789	-0.0095493	-0.0198944	-0.031831	-0.031831

The plot for magnitude and angle of V0/Vs are as below



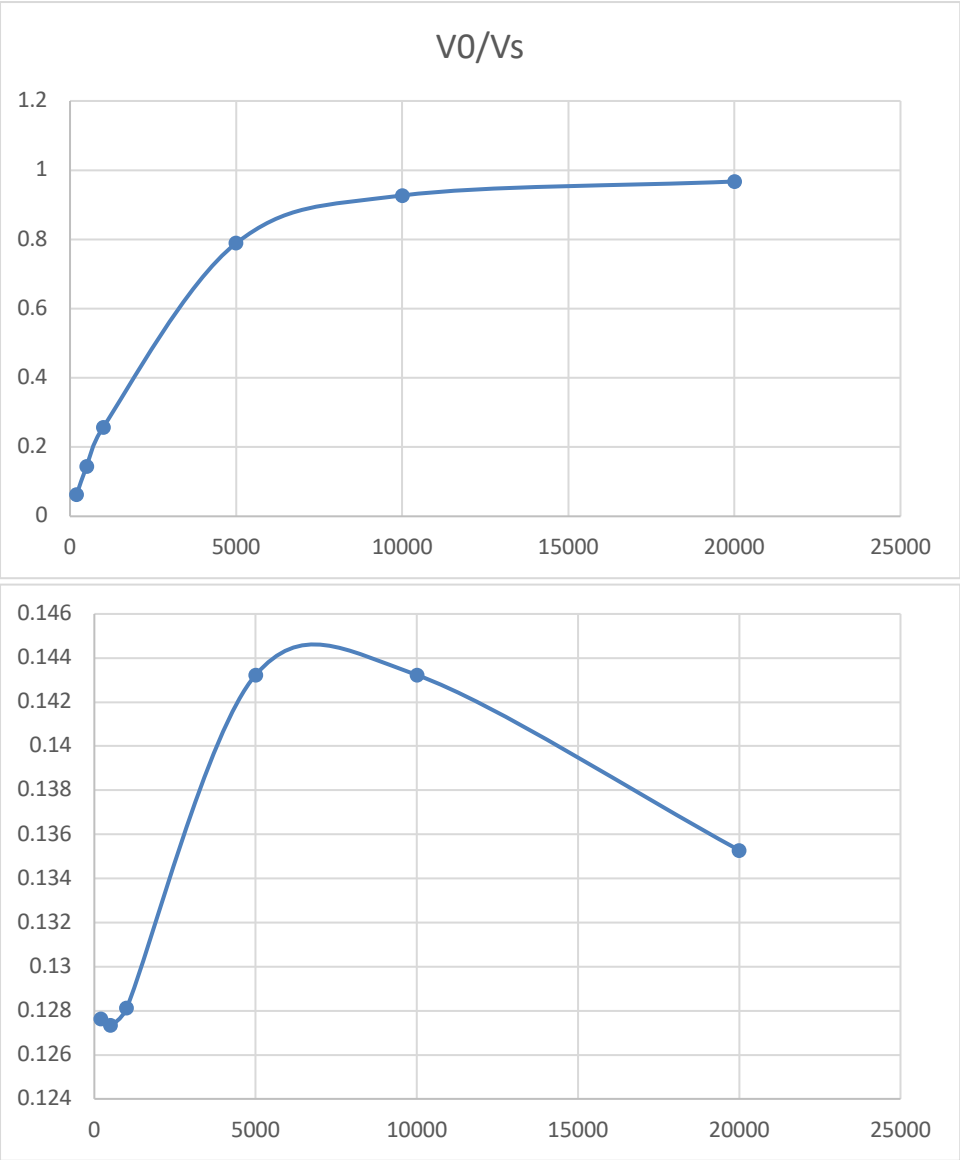


For measurements across resistor in Figure 2 topology, we get

Frequency (Hz)	200	500	1k	5k	10k	20k
Ch0 output (mV)	200.77	200.50	200.77	199.34	198.93	189.72
Ch1 output (mV)	12.68	28.92	51.76	157.26	184.40	183.52
time between peaks	4.01ms	1.6ms	805us	180us	90us	42.5us
Vo/Vs	0.063156	0.1442394	0.257807	0.788903	0.92695	0.96732

Angle V0/Vs	0.12764	0.127323	0.12811	0.14323	0.14323	0.13528

The plot for magnitude and phase of V0/Vs is as below

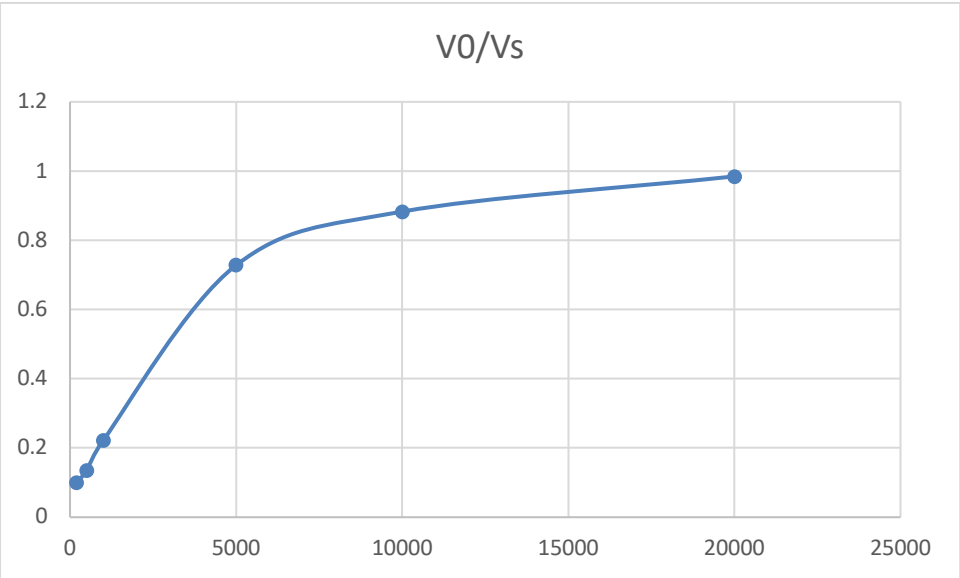


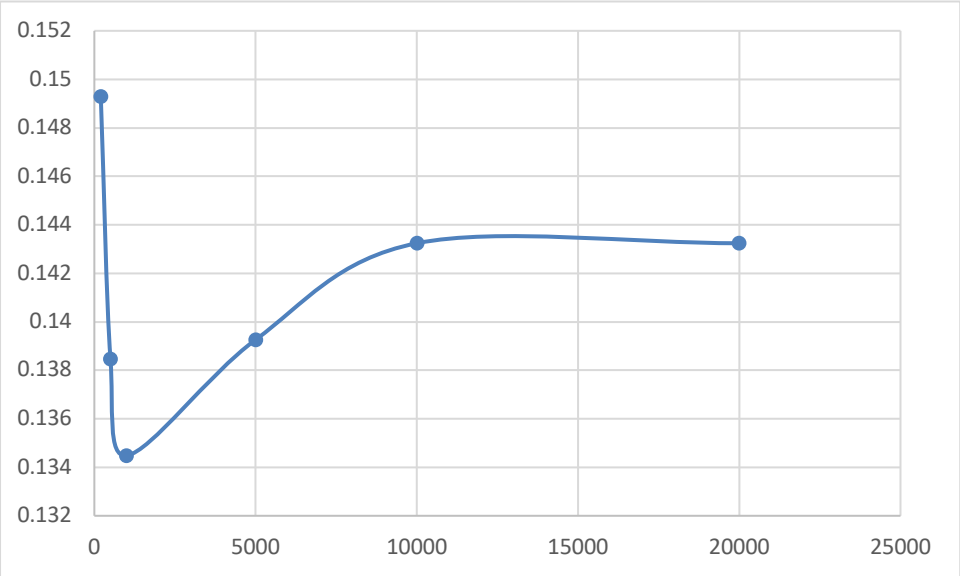
For measurements across inductor in Figure 1 topology, we get

Frequency (Hz)	200	500	1k	5k	10k	20k
Ch0 output (mV)	199.81	199.75	199.20	197.29	195.18	186.93
Ch1 output (mV)	20.05	27.01	44.26	143.62	172.33	184.06
time between	4690	1740	845	175	90	45

peaks (us)						
V0/Vs	0.100345	0.135219	0.22218876	0.72796391	0.88292858	0.98464666
Phase V0/Vs	0.149287	0.138464	0.13448593	0.13926058	0.14323945	0.14323945

The magnitude and phase plot for V0/Vs is as below



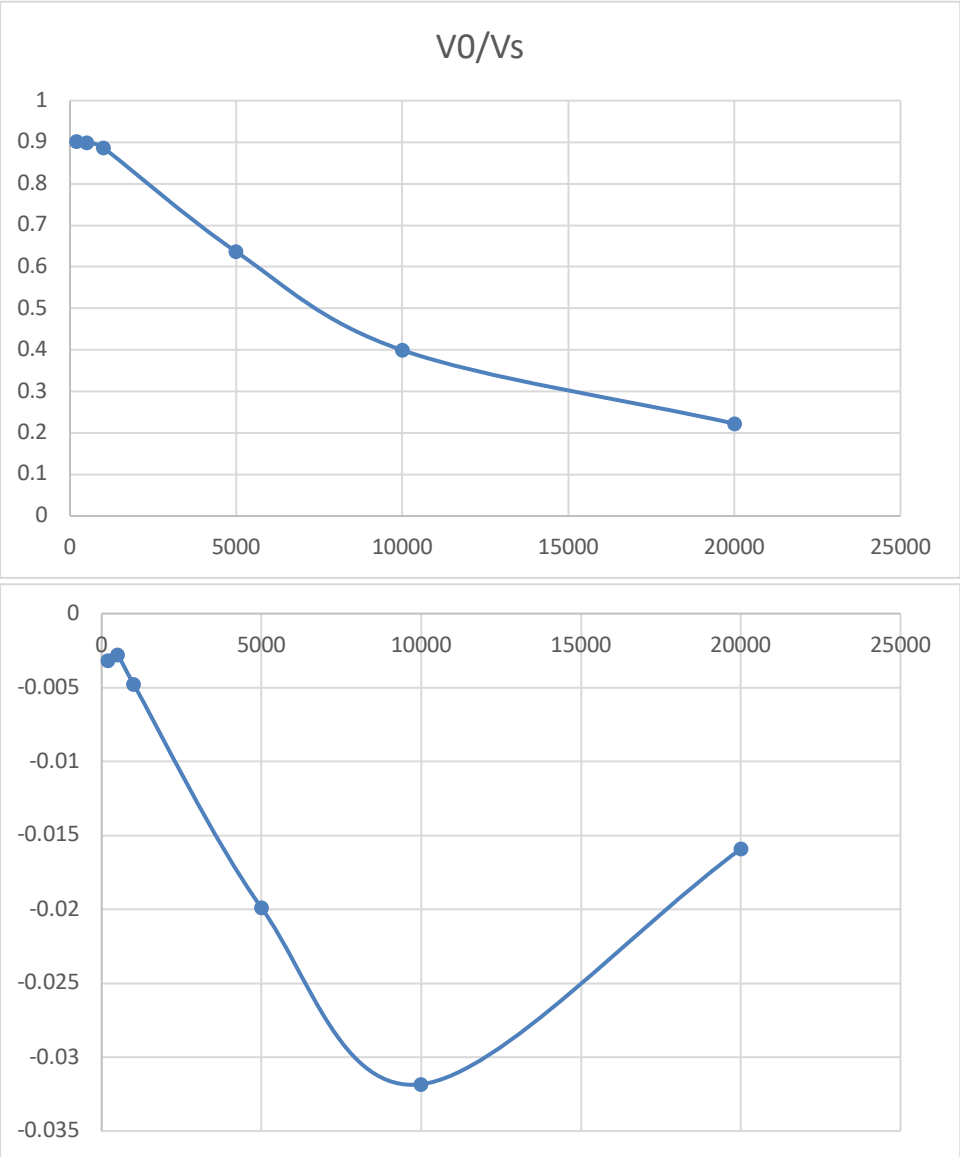


For measurements across resistor in Figure 1 topology, we get

Frequency (Hz)	200	500	1k	5k	10k	20k
Ch0 output (mV)	199.95	199.47	198.93	196.88	194.02	186.18
Ch1	180.31	179.36	176.36	125.28	77.47	41.42

output (mV)						
time between peaks	100	35	30	25	20	5
V0/Vs	0.90177544	0.89918283	0.88654301	0.6363267	0.39928873	0.22247288
Phase of V0/Vs	0.0031831	0.002785	0.004774	0.019894	0.03183099	0.01591549

The plot for magnitude and phase of V0/Vs is as below



2.4 data analysis

Using the equations as mentioned in theory section, we can calculate the theoretical value of V0. For measurements across capacitor in Figure 2 topology, we get

Frequency (Hz)	200	500	1k	5k	10k	20k

Ch0 output (mV)	200.91	200.43	200.43	199.81	196.47	189.38
theoretical Ch1 output (mV)	199.989	199.935	199.7404	193.798	178.1670	140.0142
Theoretical magnitude of V0/Vs	0.995415	0.99753031	0.9965594	0.96991142	0.90684074	0.73932939
Theoretical phase of V0/Vs	-0.0101996	-0.0254945	-0.0509559	-0.249679	-0.4716156	-0.7952988

Here, the excel formula we applied is
=0.1*SQRT(1/(1+10^(-16)*(w)^2*(5.1*1000)^2))*2000

Similarly, We can calculate the theoretical value for other circuit topologies. For measurements across resistor in Figure 2 topology. We get

Frequency (Hz)	200	500	1k	5k	10k	20k
Ch0 output (mV)	200.77	200.50	200.77	199.34	198.93	189.72
Theoretical Ch1 output (mV)	2.03989	5.09834	10.1867	49.4185	90.8652	142.814
Theoretical Vo/Vs	0.01016	0.02542	0.05073	0.24791	0.4567	0.75276
Theoretical phase of V0/Vs	1.560596681	1.54530185	1.51984047	1.32111735	1.09918076	0.7754975

Based on the equation in theory section, the excel formula I applied is
=(2000*0.1*5100*10^(-8)*w)*SQRT(1/(1+10^(-16)*(w)^2*(5.1*1000)^2))

For measurements across inductor in Figure 1 topology, we get

Frequency (Hz)	200	500	1k	5k	10k	20k
Ch0 output (mV)	199.81	199.75	199.20	197.29	195.18	186.93
Theoretical Ch1 output (mV)	1.319971	3.299550	6.596409	32.55975	62.67549	110.1684
Theoretical magnitude of V0/Vs	0.006606	0.0165184	0.0331145	0.165035	0.321116	0.589356

Theoretical phase of V0/Vs	1.564196	1.55429	1.5378	1.40726	1.25204877	0.98742332

For measurements across resistor in Figure 1 topology, we get

Frequency (Hz)	200	500	1k	5k	10k	20k
Ch0 output (mV)	199.95	199.47	198.93	196.88	194.02	186.18
Theoretical Ch1 output (mV)	199.995	199.972	199.891	197.331	189.92	166.921
Theoretical magnitude of V0/Vs	0.99997	0.9998	0.99945	0.98665	0.94962	0.83460
Theoretical phase of V0/Vs	-0.006599904	-0.0164985	-0.032988	-0.1635266	-0.3187476	-0.583373

2.5 error analysis

The error for the four topologies are as below

Frequency	200	500	1k	5k	10k	20k
Experimental Vo/Vs	0.993877	0.988075	0.959836	0.59456484	0.35160584	0.18402154
Theoretical V0/Vs	0.9954	0.997530	0.9965594	0.96991142	0.90684074	0.73932939
Error	0.001530	0.009478	0.0368501	0.38699058	0.61227388	0.75109668

Frequency	200	500	1k	5k	10k	20k
Experimental Vo/Vs	0.063156	0.1442394	0.257807	0.788903	0.92695	0.96732
Theoretical V0/Vs	0.01016	0.02542	0.05073	0.24791	0.4567	0.75276
Error	5.216141	4.674248	4.081943	2.182215	1.029669	0.285031

Frequency	200	500	1k	5k	10k	20k
Experimental Vo/Vs	0.100345	0.135219	0.22218876	0.72796391	0.88292858	0.98464666
Theoretical V0/Vs	0.006606	0.01651	0.0331145	0.165035	0.321116	0.589356
Error	14.1899	7.19012	5.709712	3.41096683	1.74956271	0.67071627

Frequency	200	500	1k	5k	10k	20k
Experimental Vo/Vs	0.901775	0.899182	0.886543	0.6363267	0.399288	0.2224728
Theoretical V0/Vs	0.99997	0.9998	0.99945	0.98665	0.94962	0.83460
Error	0.098197	0.100638	0.112969	0.35506	0.579528	0.733437

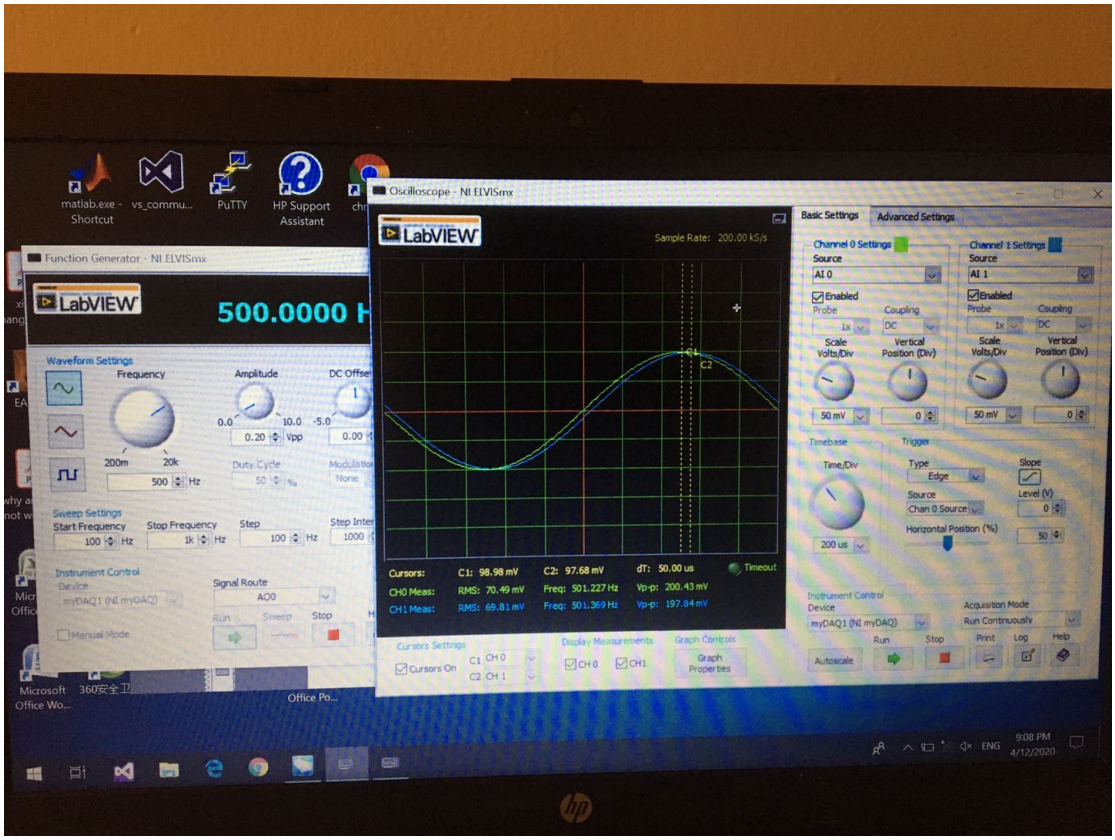
For voltage across the capacitor in Figure 2 topology, the error increases as the frequency increases. In the expression we obtained earlier, i.e., $\frac{A}{\sqrt{1+C^2w^2R^2}}$, the denominator becomes bigger and bigger as frequency increases. However, as I observed on the oscilloscope, at large frequencies such as 20kHz, the function generator produces an amplitude at around 180mV, which deviates from 200mV, thus the A factor in the numerator is affected more when frequency is high, and theoretical value differs from experiment value. This is the same trend of voltage across resistor in Figure 1 topology, i.e. $\frac{AR}{\sqrt{R^2+(Lw)^2}}$, where the numerator also has an amplitude factor and get affected when frequency increases. For voltage across resistor in Figure 2 topology and voltage across inductor in Figure 1 topology, the error decreases as frequency increases, these might be explained by the coefficients in the numerator. Their expressions are $\frac{wLA}{\sqrt{R^2+(Lw)^2}}$ and $\frac{ARCw}{\sqrt{1+C^2w^2R^2}}$. In these two expressions, RC is of the magnitude 10^(-5) and L is of the magnitude 10^(-3), so they could have made the imprecisions produced by A less significant. Due to imprecisions from dT measurements, errors from the phase angle are high.

2.6 discussion

From the general trend, we do see the expected behavior of V0/Vs. For example, for voltage across capacitor in Figure 2 topology, the expression $\frac{A}{\sqrt{1+C^2w^2R^2}}$ shows that V0/Vs will decrease as frequency becomes higher, and this is indeed the trend we observed from data points. For voltage across capcacitor in RC circuit, the phase is lagging. For voltage across resistor in RC circuit, the phase is leading. For voltage across inductor in RL circuit, the phase is leading. For voltage across resistor in RL circuit, the phase is lagging.

2.7 conclusion

This experiment verifies the general trend we expected for the magnitude of V0/Vs in sinusoidal steady state. And we observed the trends under 4 different circuit topologies. The data points are authentic, attached below are photos of my oscilloscope reading and circuit topology. I have verified my ways of calculation with Professor Masoud.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Manual Mode
Oscilloscope - NI ELVISmx
LabVIEW
Sample Rate: 200.00 kS/s
Cursors: C1: 98.98 mV C2: 97.68 mV dT: 50.00 us
CH0 Meas: RMS: 70.49 mV Freq: 501.227 Hz Vp-p: 200.43 mV
CH1 Meas: RMS: 69.81 mV Freq: 501.369 Hz Vp-p: 197.84 mV
Timeout
Cursors Settings
Cursors On
Display Measurements
Graph Controls
Graph Properties
Basic Settings
Advanced Settings
Channel 0 Settings
Channel 1 Settings
Source
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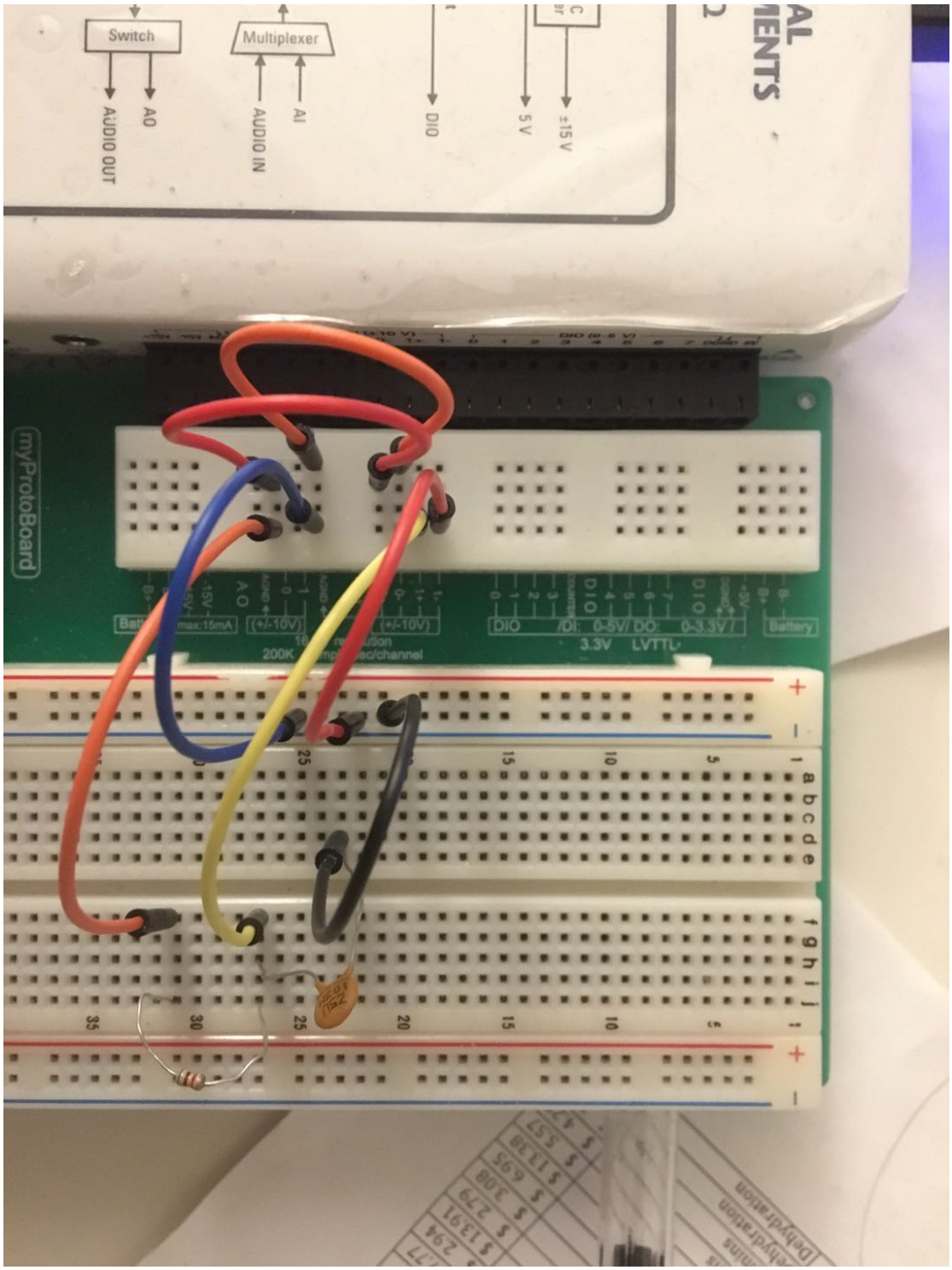


3. experiment: Determining the optimum source resistance for maximum power transfer

3.1 objective

Determine optimum source resistance for max power.

3.2 theory

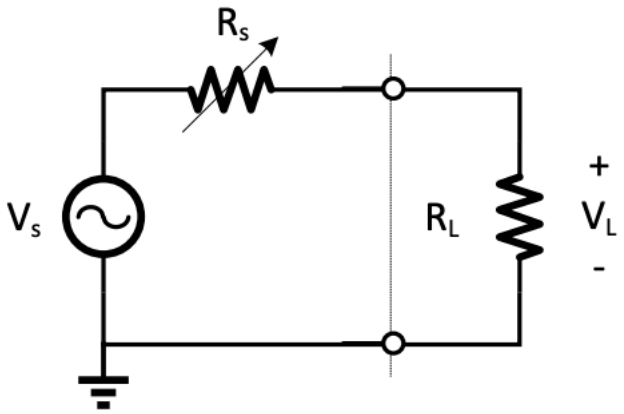


Figure 3. load and source topology

In phasor domain, we know the current in circuit is

$$I_L = \frac{Vs}{Zs + Z_L}$$

And the voltage across the load is

$$V_L = \frac{Z_L}{Zs + Z_L} Vs$$

Thus the average complex power is

$$P_{avg} = V_L * I_L^* = \frac{1}{2} * |Vs|^2 * \frac{Z_L}{|Zs + Z_L|^2}$$

Let Zs=Rs+ (Xs) j, if we take the real part of the above, and take partial derivative with respect to variables we are interested in, we will be able to find optimum source impedance or optimum load impedance.

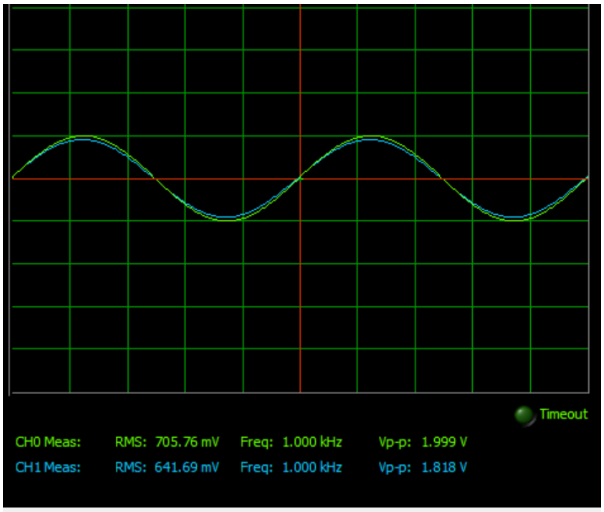
3.3 procedure

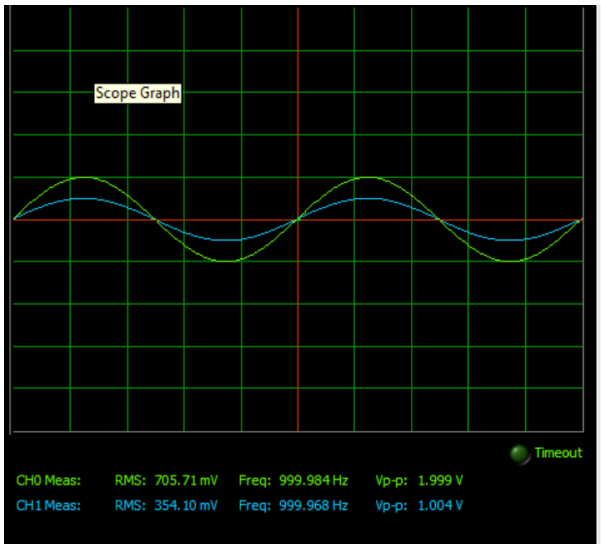
We use different value of source resistance, and connect it with load resistance, and measure the voltage across the load resistance. The topology is Figure 3.

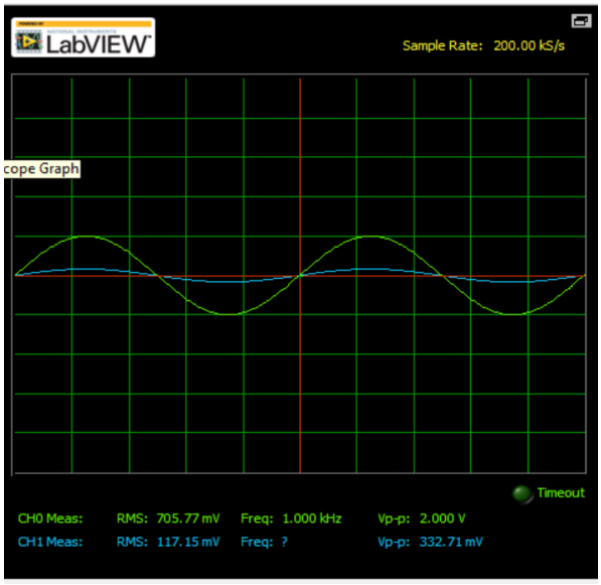
3.4. data

The data we obtained from oscilloscope are as below

Rs	R_L	Ps	P_L	P_L/Ps
1000	10000	4.11766E-06	4.11766E-05	10
10000	10000	1.25387E-05	1.25387E-05	1
50000	10000	6.86206E-06	1.37241E-06	0.2







3.5 data analysis

The average power is given by the equation

$$P_{avg} = Re[V_L * I_L{}^*] = Re[\frac{1}{2} * |Vs|^2 * \frac{Z_L}{|Zs + Z_L|^2}] = \frac{1}{2} * \frac{|V_s|^2 R_L}{(R_{TH} + R_L)^2 + (X_{TH} + X_L)^2}$$

Take derivative of above expression with respect to R_{TH}, we get

$$\frac{\partial P_{avg}}{\partial R_{TH}} = \frac{-2|V_s|^2 R_L (R_{TH} + R_L)}{[(R_{TH} + R_L)^2 + (X_{TH} + X_L)^2]^2}$$

Equate the derivative to 0 we get $R_{TH} = -R_L$
Similarly, we can take derivative of power with respect to X_{TH}, and we get

$$\frac{\partial P_{avg}}{\partial X_{TH}} = \frac{-2|V_s|^2 R_L (X_{TH} + X_L)}{[(R_{TH} + R_L)^2 + (X_{TH} + X_L)^2]^2}$$

Equate the above expression to 0, we get $X_{TH} = -X_L$.
Thus, we know that maximum power on load is reached when the source impedance cancels the load impedance, and therefore makes the combined impedance in circuit smallest.
The average power on the source is given by the equation

$$P_S = \frac{1}{2} * \frac{|V_s|^2 R_{TH}}{(R_{TH} + R_L)^2 + (X_{TH} + X_L)^2}$$

Thus $\eta = \frac{P_L}{P_S} = \frac{R_L}{R_{TH}}$, and when R_L is fixed, the maximum is achieved when R_{TH} is smallest.

3.6 error analysis

Rs	R_L	Ps	P_L	P_L/Ps	Theoretical P_L	Theoretical η
1000	10000	4.11766E-06	4.11766E-05	10	4.13223E-05	10
10000	10000	1.25387E-05	1.25387E-05	1	0.0000125	1
50000	10000	6.86206E-06	1.37241E-06	0.2	1.38889E-06	0.2

Rs	R_L	Error on P_L	Error on η
1000	10000	0.003526144	0
10000	10000	0.00309448	0
50000	10000	0.01186318	0

The error is minimal.

3.7 Discussion

Part a, b and c: max power and max power transfer efficiency are achieved when Rs is 1k. This result agrees with our previous analysis. When Rs is the minimum, the total impedance in the circuit is the lowest, the current is the maximum, and when load resistance is fixed, the

power on load reaches maximum.

3.8 conclusion

The experimental result matches with the theoretical values very well. And the errors are minimal. In this experiment we verified that when load resistance is fixed, maximum power on load is achieved when source resistance is smallest.

4. experiment: Determining the optimum load resistance for maximum power transfer

4.1. objective

Find optimum load resistance for maximum power transfer.

4.2 Theory

We have the same circuit topology as in experiment 3. Except in this experiment source resistance is fixed and load resistance varies. Thus in order to find maximum, we will take the derivative with respect to load impedance

$$\frac{\partial P_{avg}}{\partial X_L} = \frac{-2|V_s|^2 R_L (X_{TH} + X_L)}{[(R_{TH} + R_L)^2 + (X_{TH} + X_L)^2]^2}$$

Equate the above to 0 we get X_{TH}= -X_L
Take derivative of power with respect to R_L, we get

$$\frac{\partial P_{avg}}{\partial R_L} = \frac{|V_s|^2[(R_{TH} + R_L)^2 + (X_{TH} + X_L)^2] - |V_s|^2 R_L 2(R_{TH} + R_L)}{[(R_{TH} + R_L)^2 + (X_{TH} + X_L)^2]^2}$$

When X_{TH}= -X_L , we can simplify the above expression to

$$\frac{\partial P_{avg}}{\partial R_L} = \frac{|V_s|^2[(R_{TH} + R_L)^2] - |V_s|^2 R_L 2(R_{TH} + R_L)}{[(R_{TH} + R_L)^2]^2} = \frac{|V_s|^2({R_{TH}}^2 - {R_L}^2)}{[(R_{TH} + R_L)^2]^2}$$

Equate the above to 0 we get $R_L = R_{TH}$
Thus the maximum load power is achieved when $Z_L = {Z_{TH}}^*$.

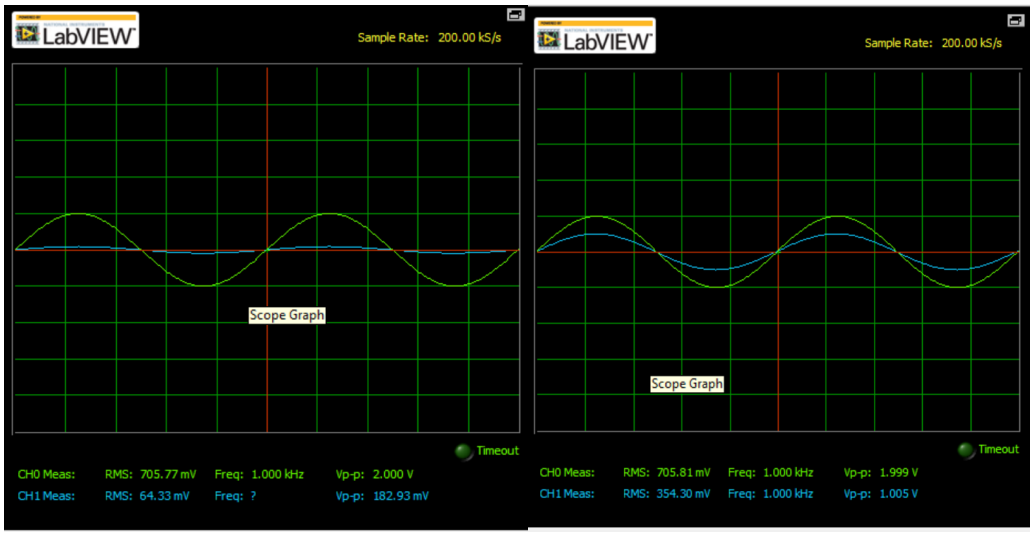
Thus $\eta = \frac{P_L}{P_S} = \frac{R_L}{R_{TH}}$, and when R_{TH} is fixed, the maximum is achieved when R_L is maximum.

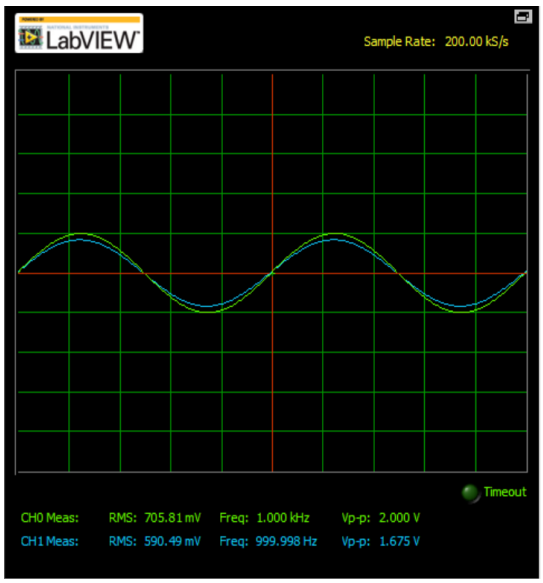
4.3 procedure

Same as 3.3

4.4 data

Rs	R_L	Ps	P_L	P_L/Ps
10000	1000	4.13835E-05	4.13835E-06	0.1
10000	10000	1.25528E-05	1.25528E-05	1
10000	50000	1.39471E-06	6.97357E-06	5





4.5 data analysis

The result from the experiment agrees with our prediction in the theory section. The maximum power happens when the source resistance equals the load resistance, i.e., when they are both 10k. And the max power transfer happens when load resistance is at its maximum.

4.6 error analysis

Rs	R_L	Ps	P_L	P_L/Ps	Theoretical P_L	Theoretical η
10000	1000	4.13835E-05	4.13835E-06	0.05007402	4.13223E-06	0.1
10000	10000	1.25528E-05	1.25528E-05	0.50211396	0.0000125	1
10000	50000	1.39471E-06	6.97357E-06	2.51048477	6.94444E-06	5

Rs	R_L	Error on P_L	Error on η
1000	10000	0.001480434	0
10000	10000	0.00422792	0
50000	10000	0.004193907	0

the error is minimal.

4.7. discussion

Part a, b and c: The experimental results agree with theoretical predictions that, the maximum power is achieved when the resistors have the same value, i.e. when they are both 10k. And maximum power transfer is maximum when load resistance is maximum. These results agree with the analysis in the theory section.

4.8 conclusion

The experimental result matches with the theoretical values very well. And the errors are minimal. In this experiment we verified that when source resistance is fixed, maximum power on load is achieved when load resistance is maximal.