

RFSoC 4X2 Gen3

Variant: Prototype

12/17/2021
V2I1

RELEASED

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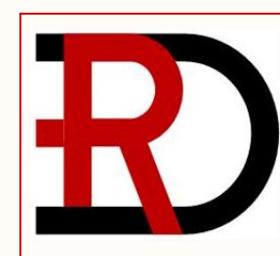
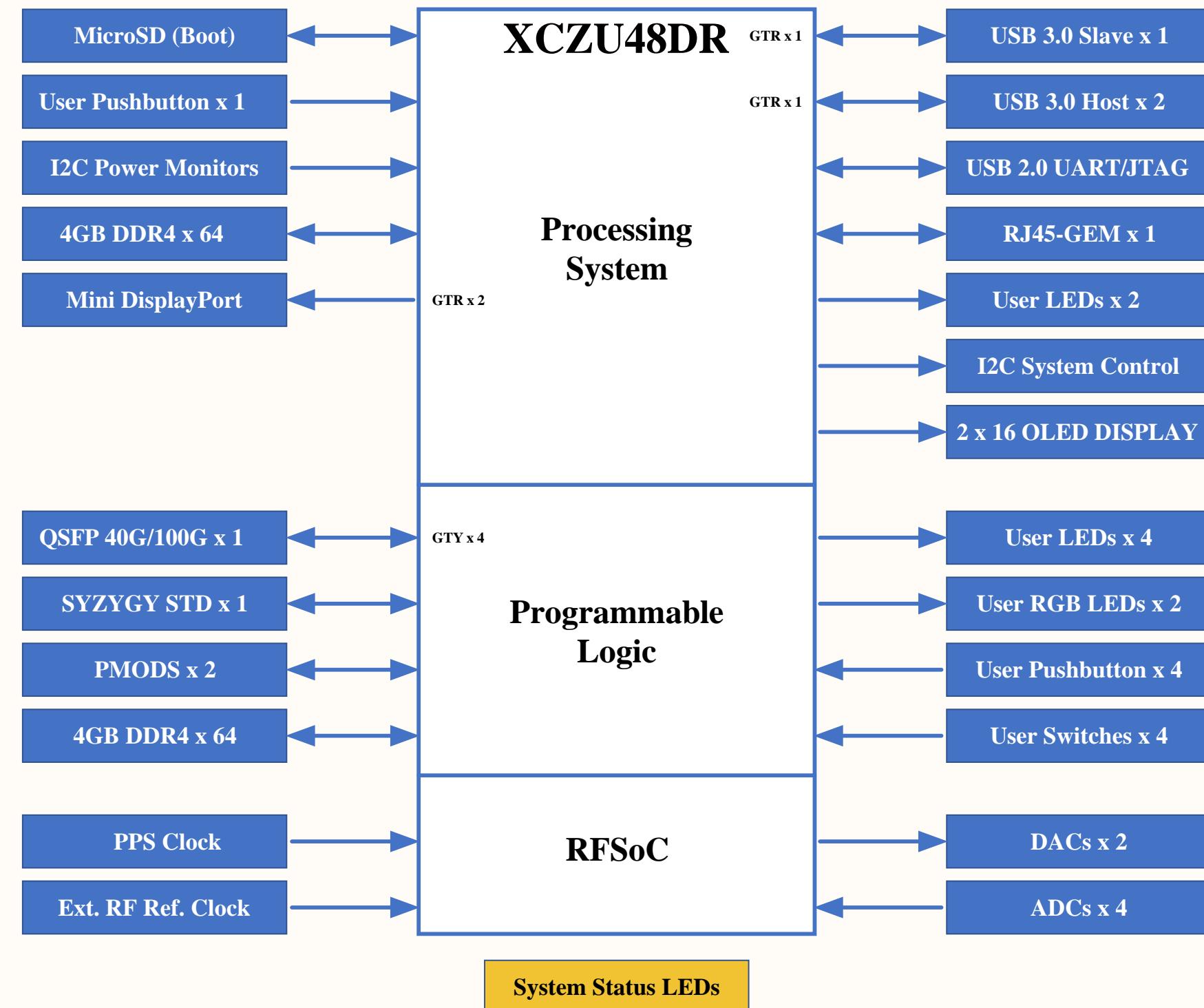
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	Title:	RFSoC 4X2 Gen3	Variant: Prototype
	Page Contents:	[01]- COVER PAGE.SchDoc	
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RFSoC 4X2 Gen3

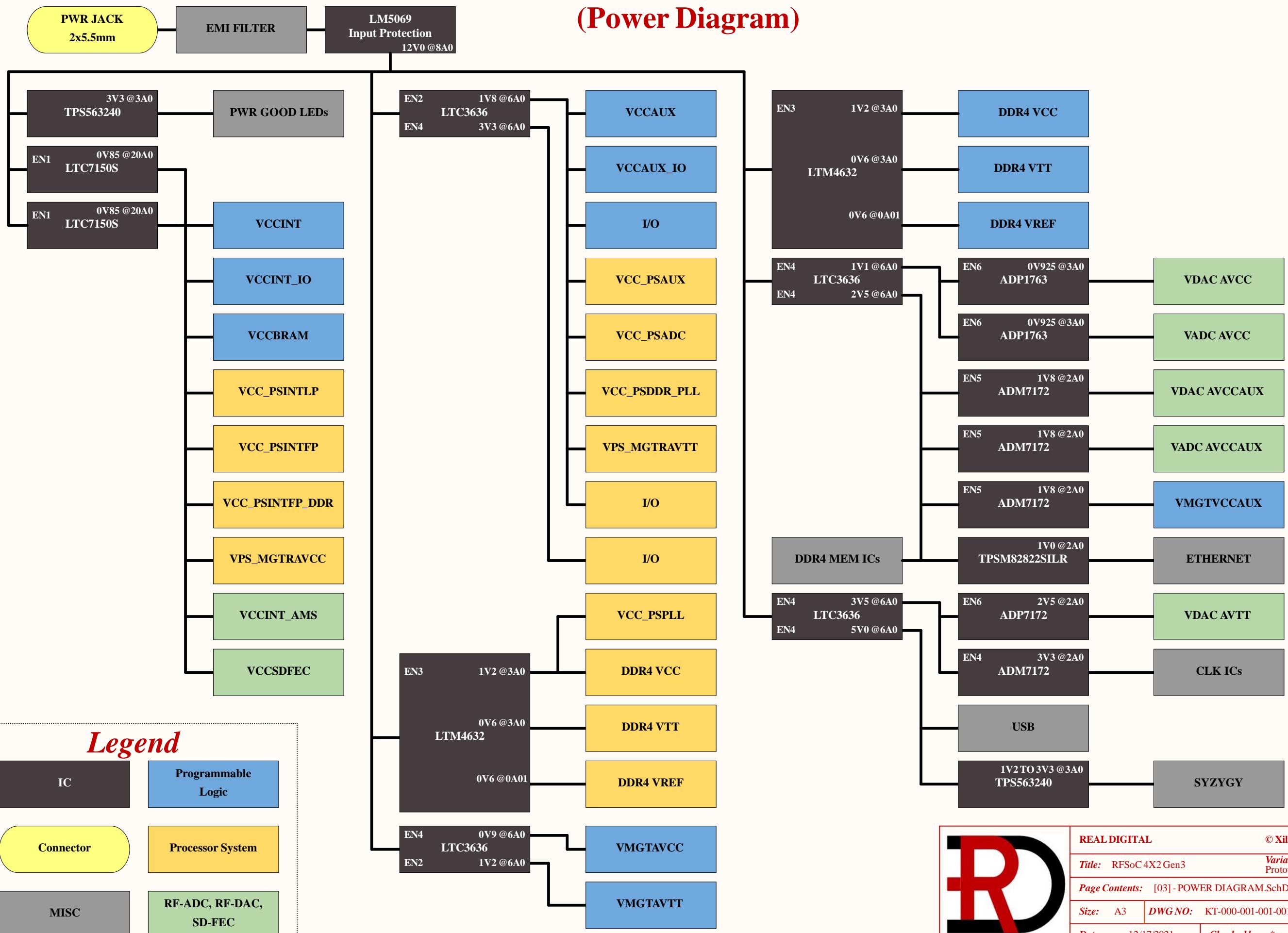
(Block Diagram)



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RFSoC 4X2 Gen3

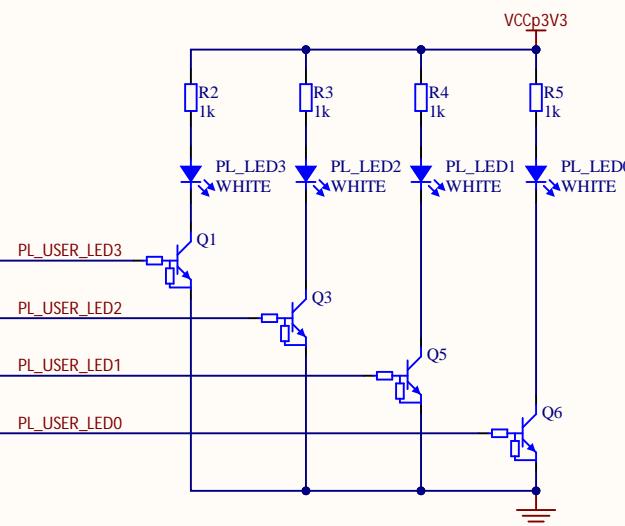
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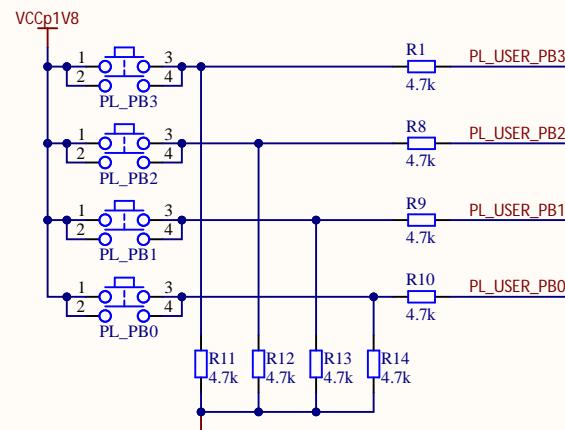
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Page Contents: [03]- POWER DIAGRAM.SchDoc		
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USER IO, LEDs

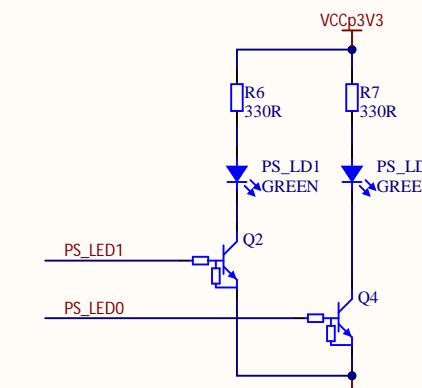
PL user-defined white LEDs



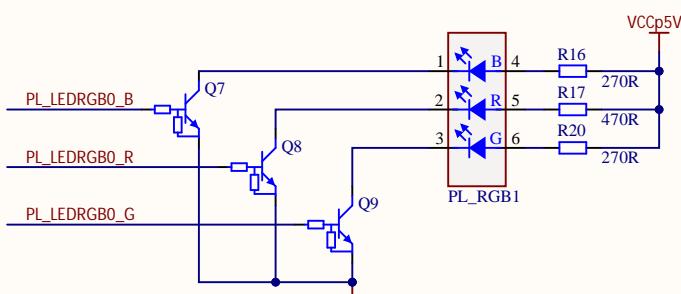
PL user-defined pushbuttons



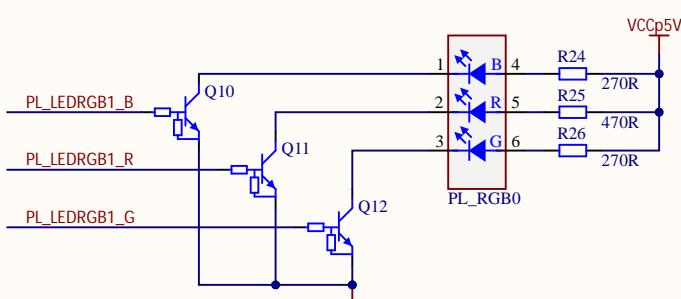
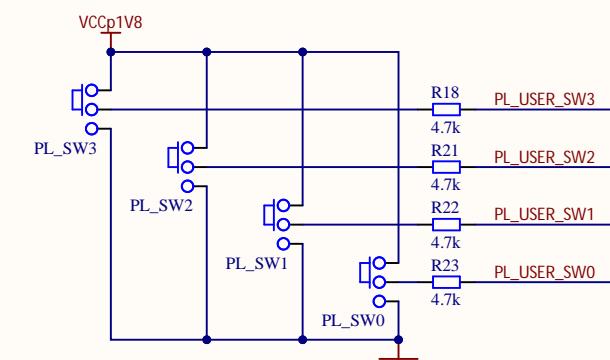
PS user-defined green LEDs



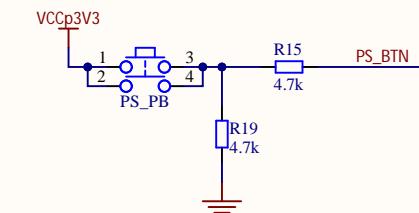
PL user-defined RGB LEDs



PL user-defined switches



PS user-defined pushbutton



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Variant:

Prototype

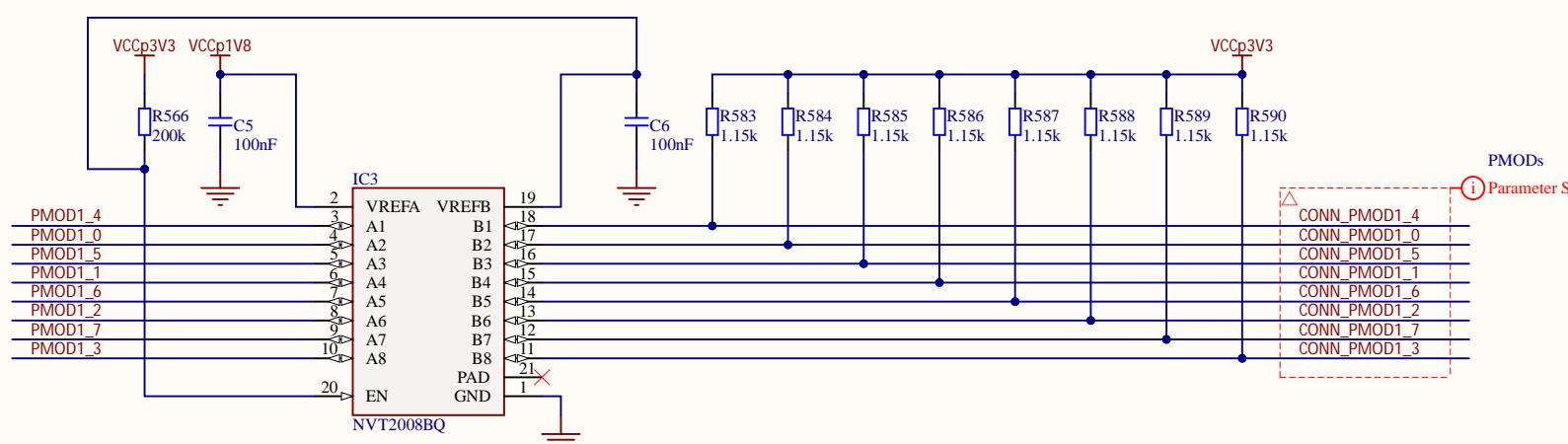
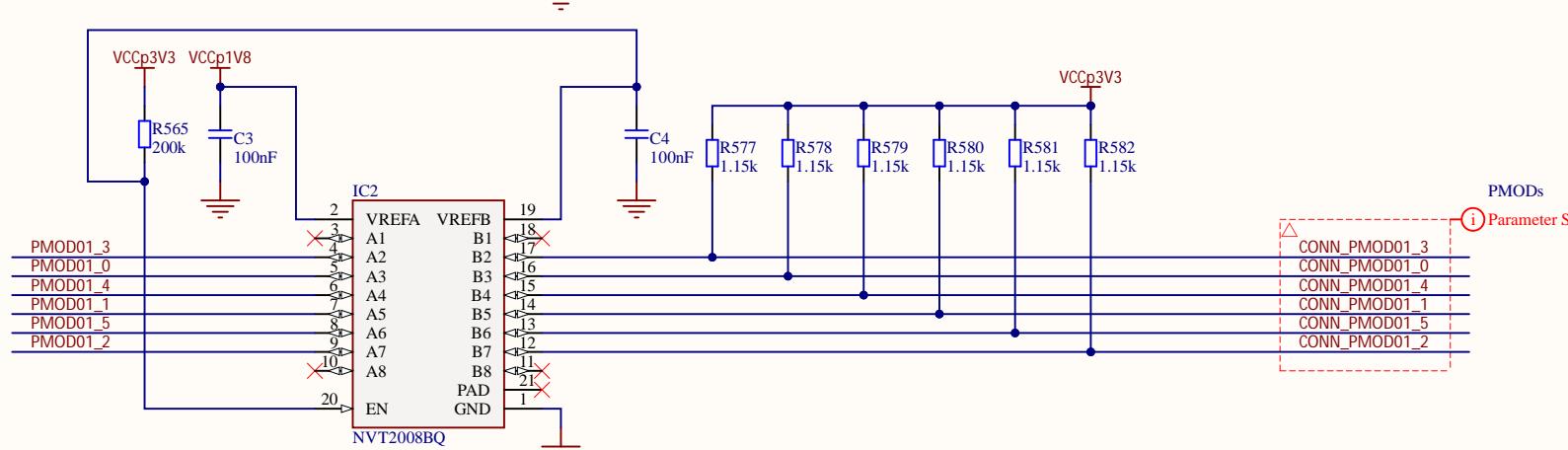
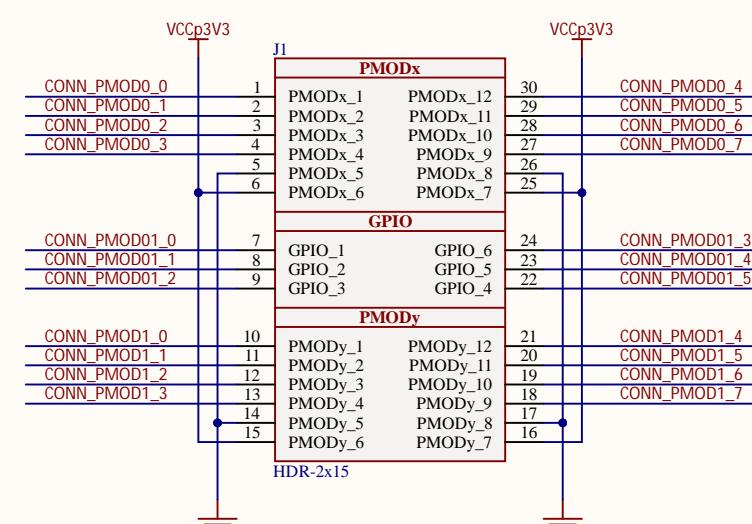
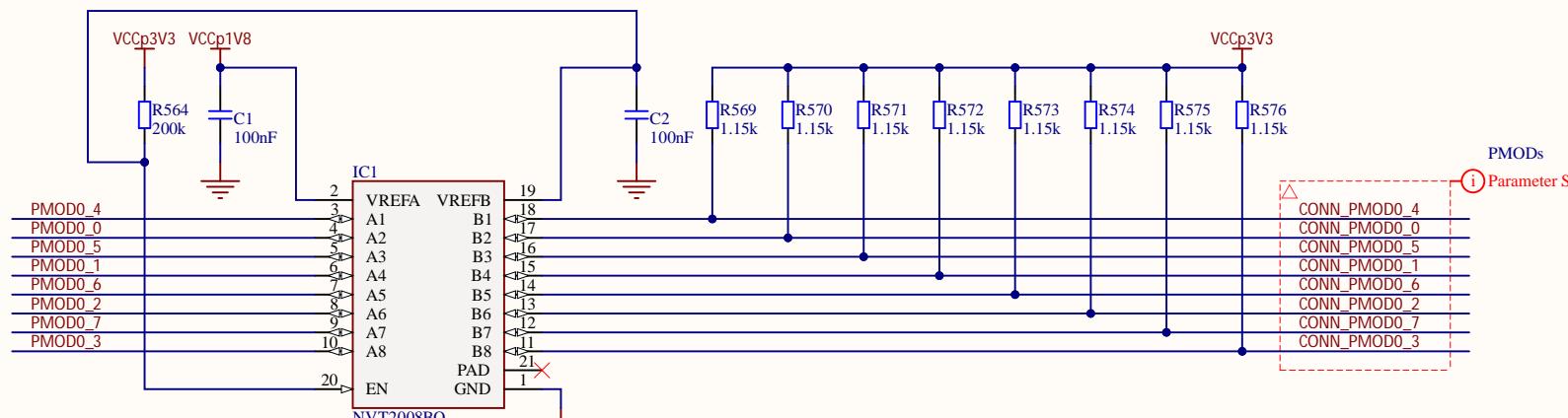
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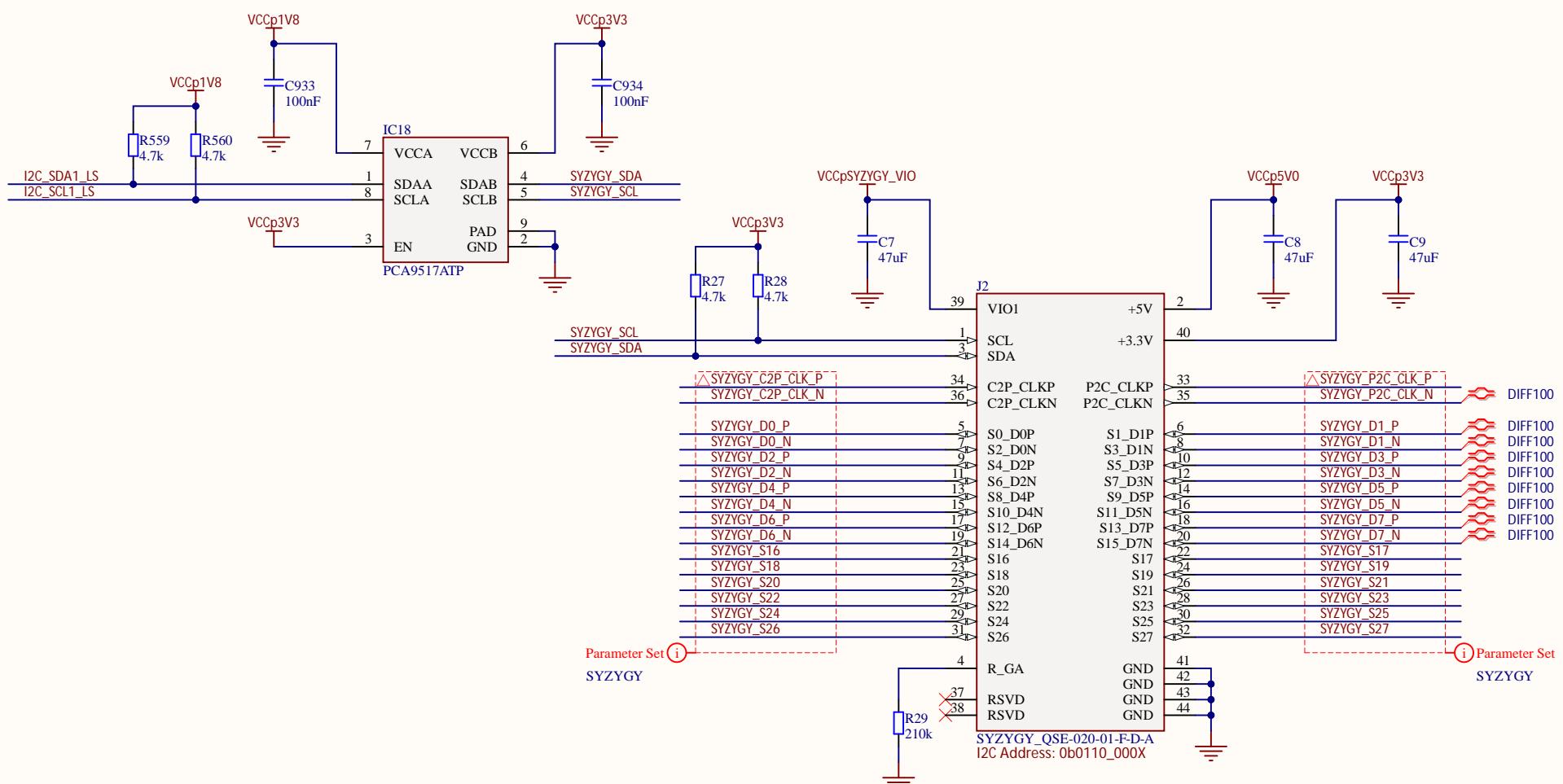
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PMOD HEADERS

A A

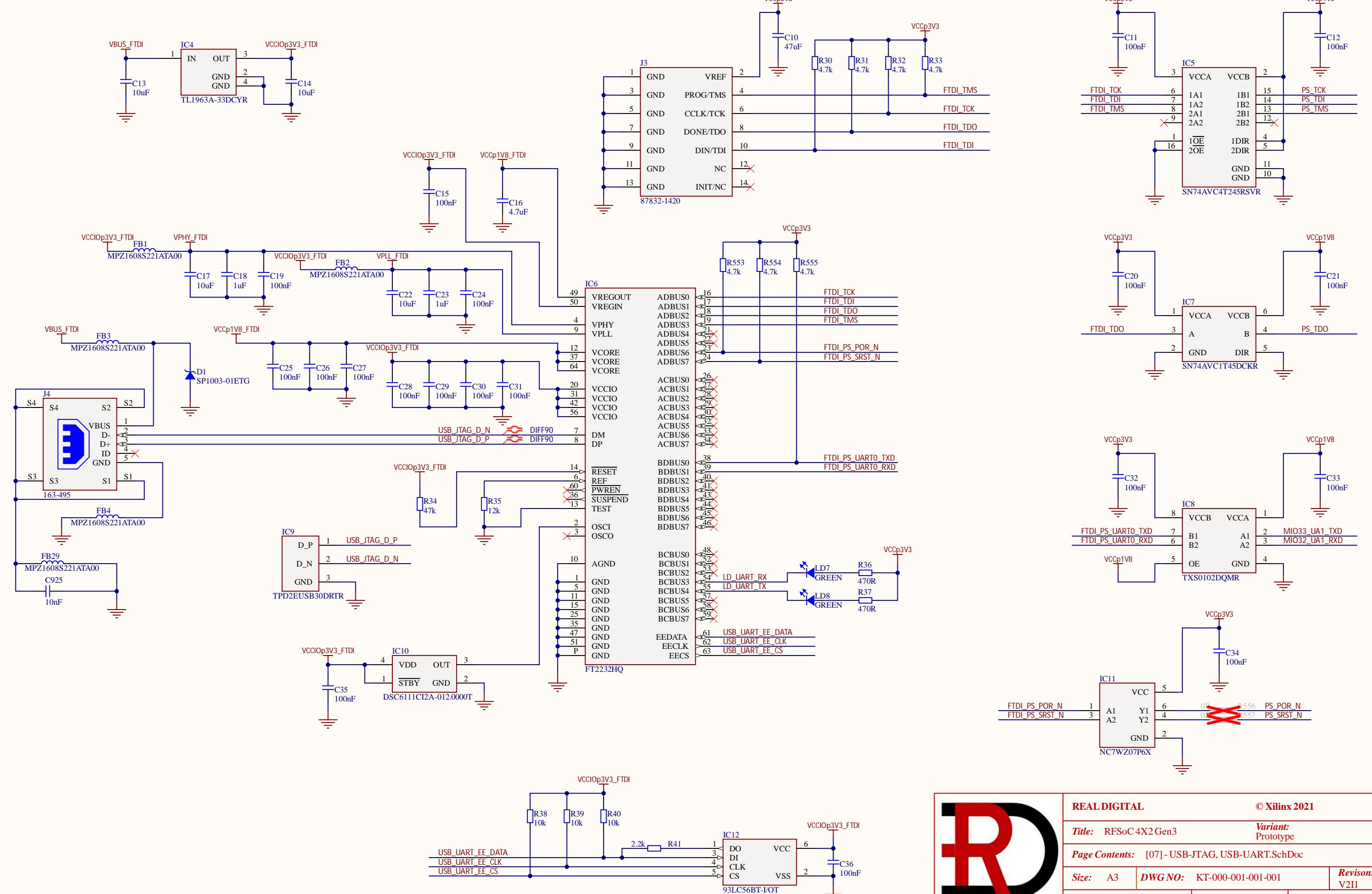


SYZYGY HEADER

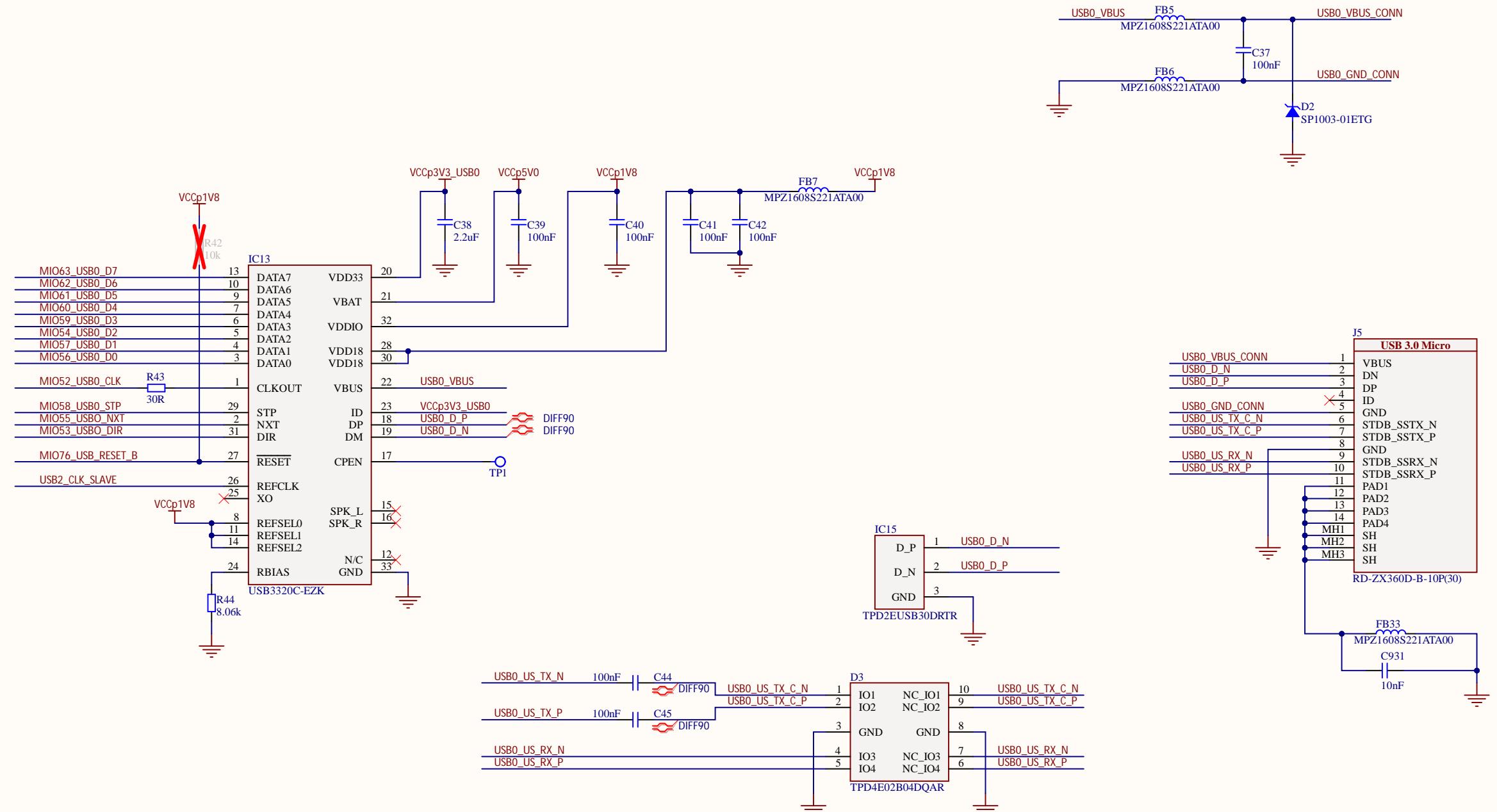


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USB-JTAG, USB-UART

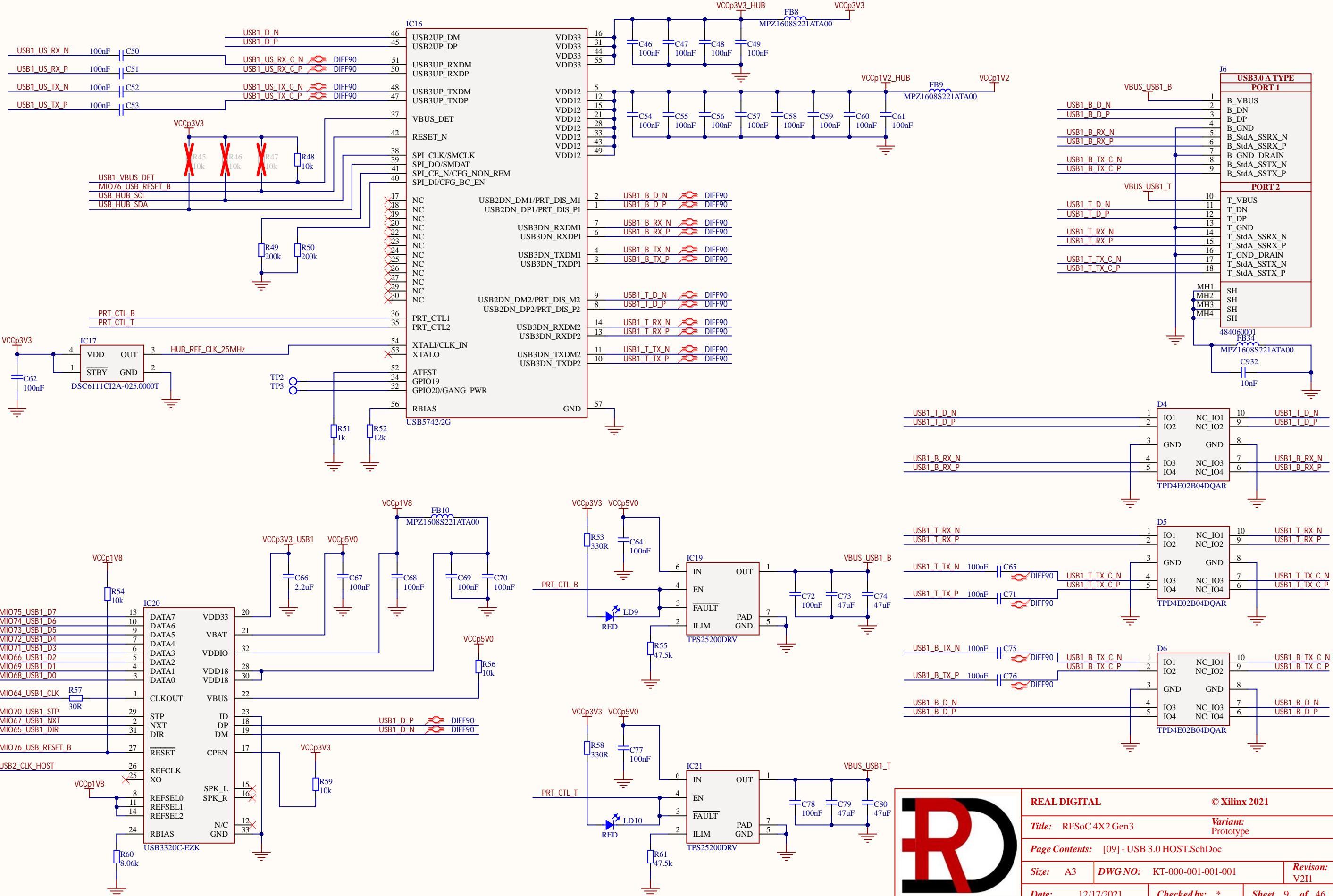


USB 3.0 SLAVE

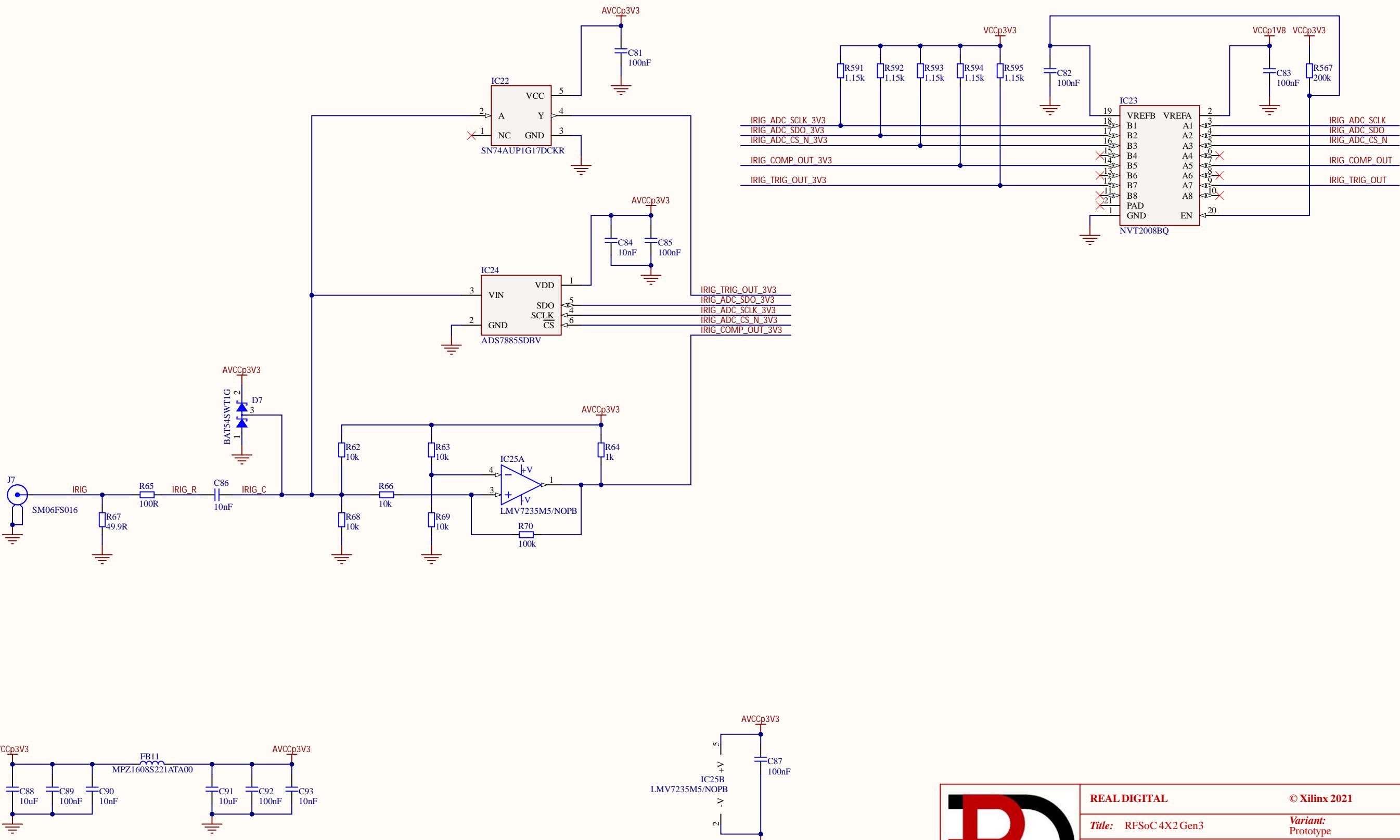


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USB 3.0 HOST



1PPS



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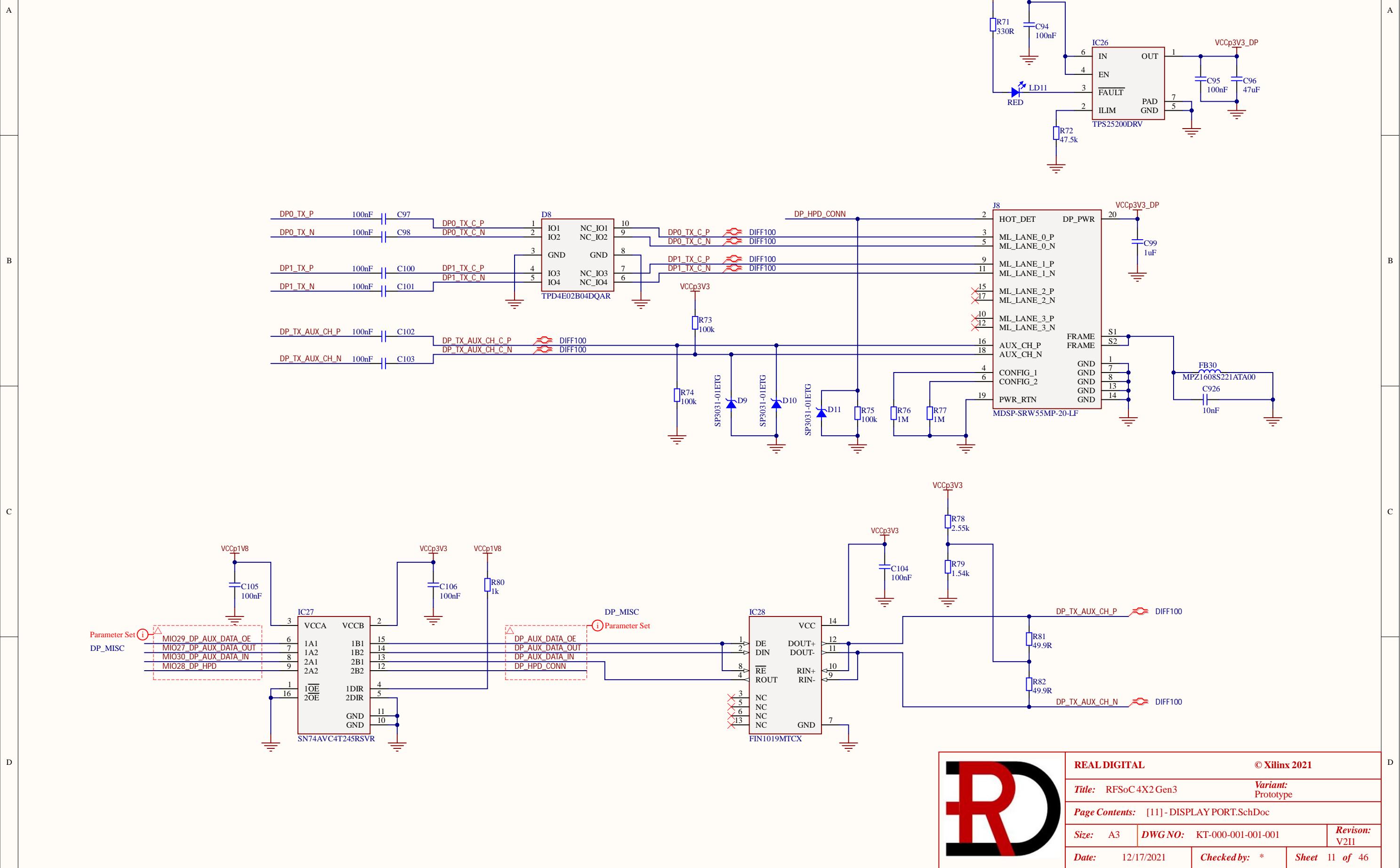
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Prototype

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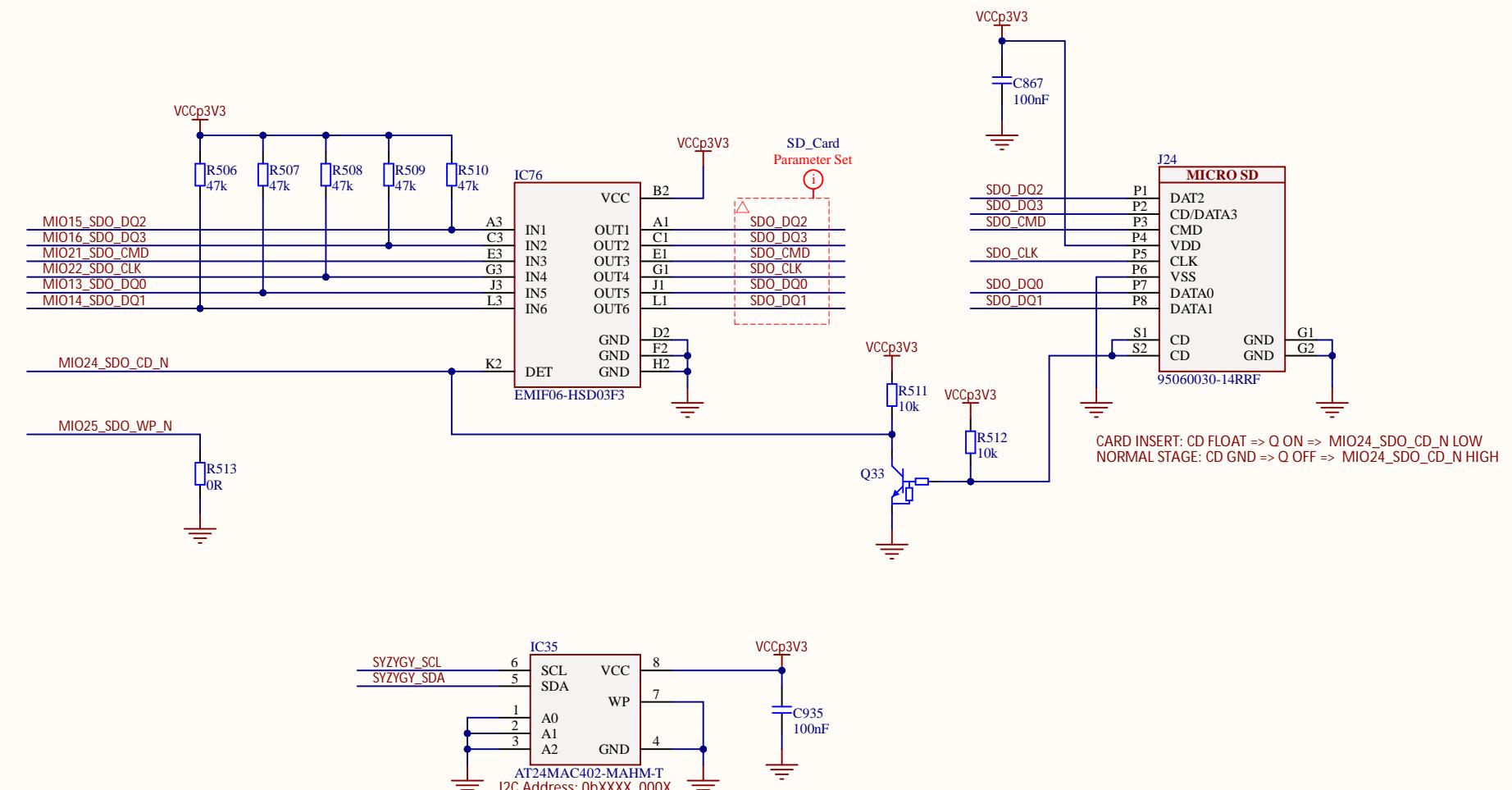
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DISPLAY PORT

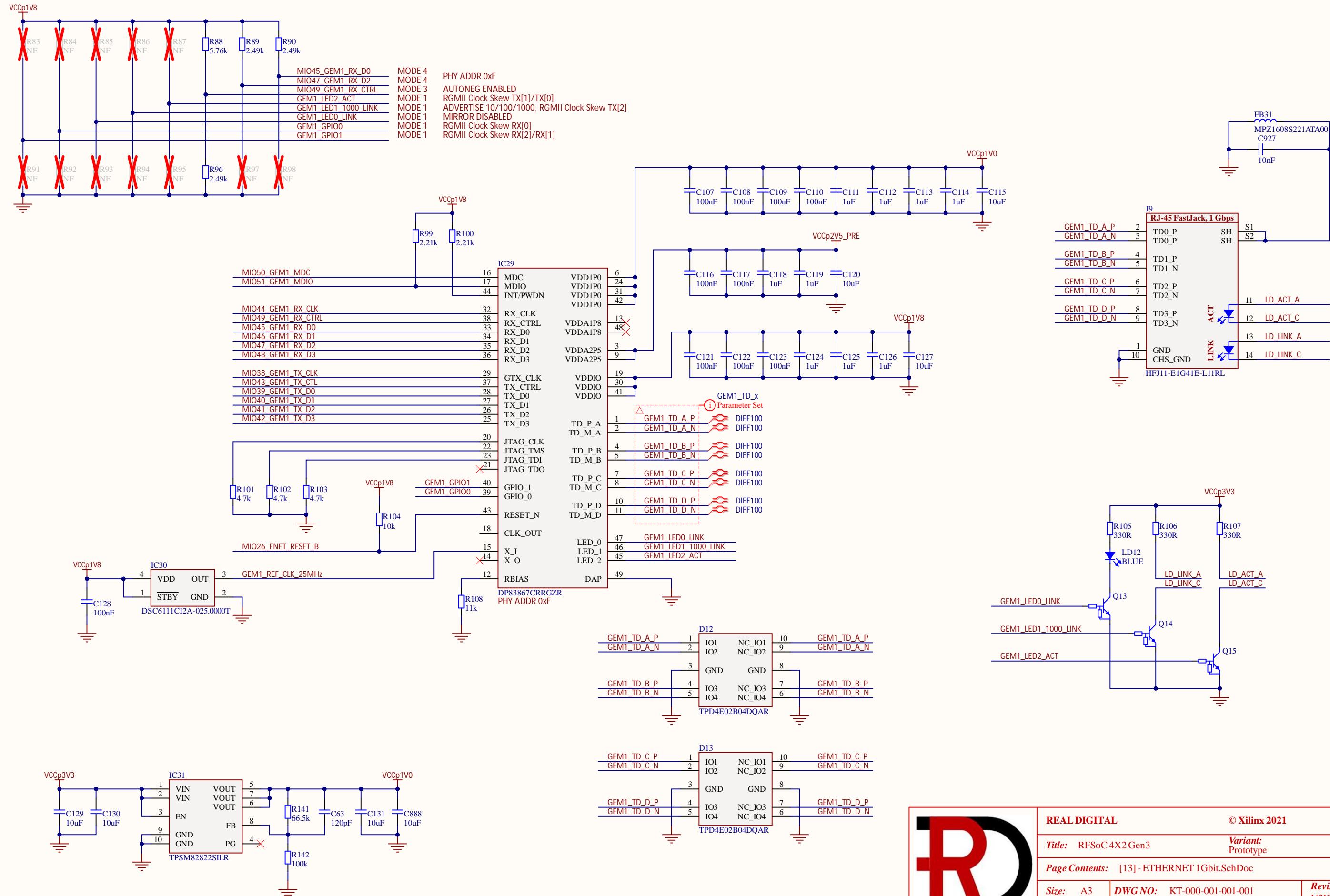


SD CARD



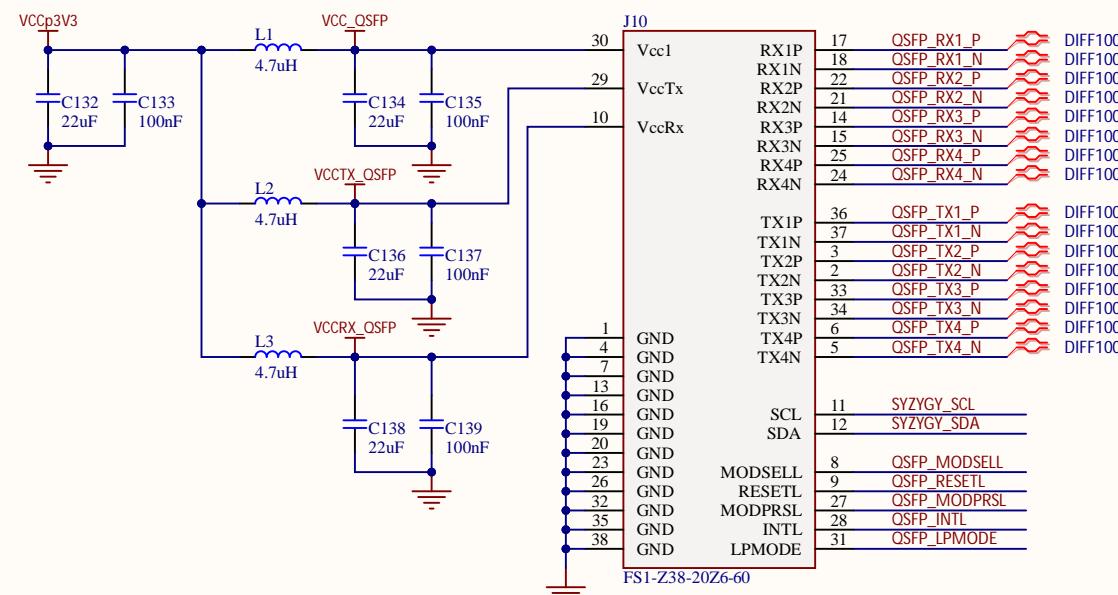
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ETHERNET 1Gbit

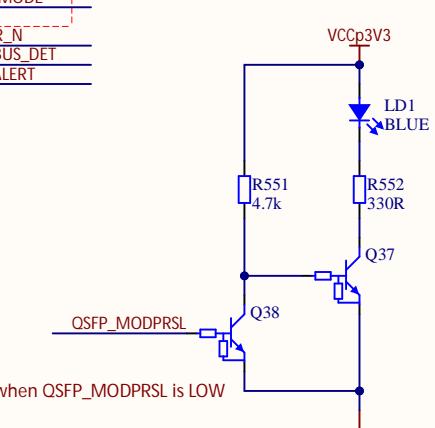
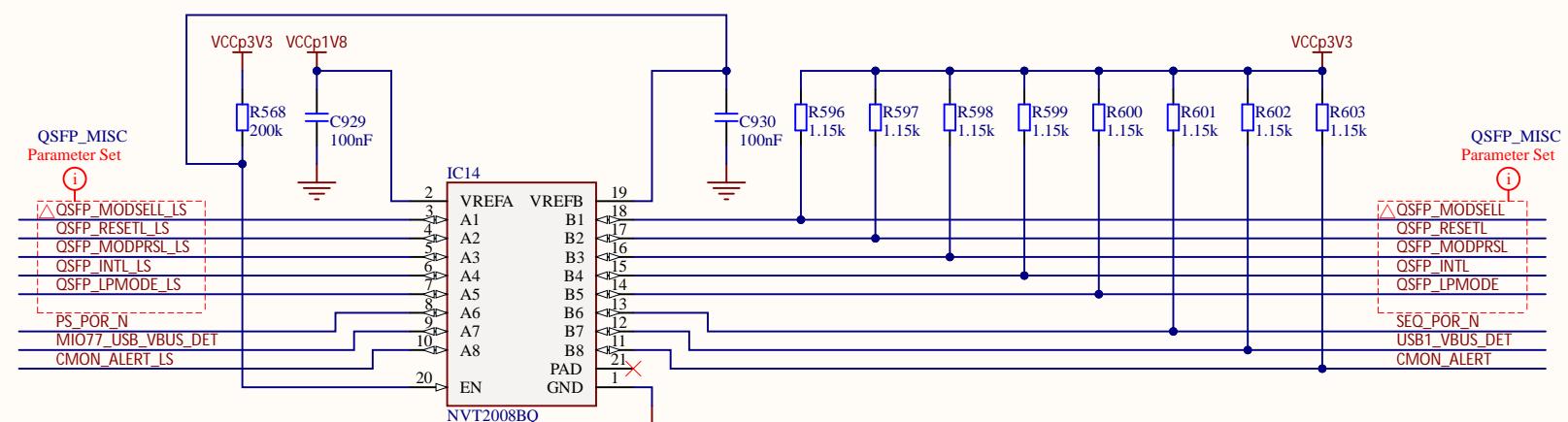
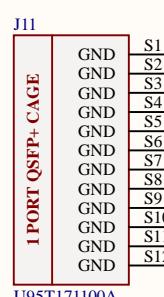


QSFP

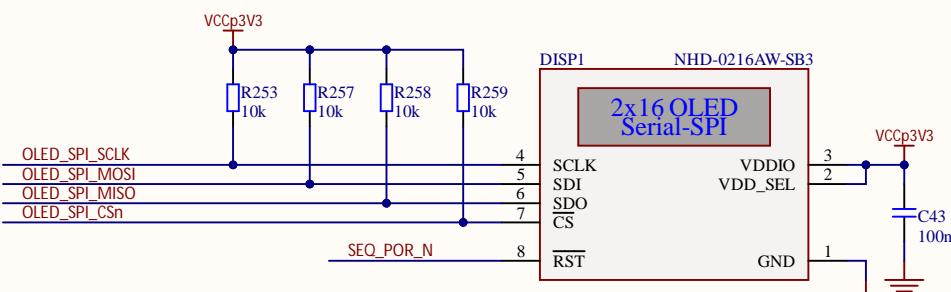
A



B



C



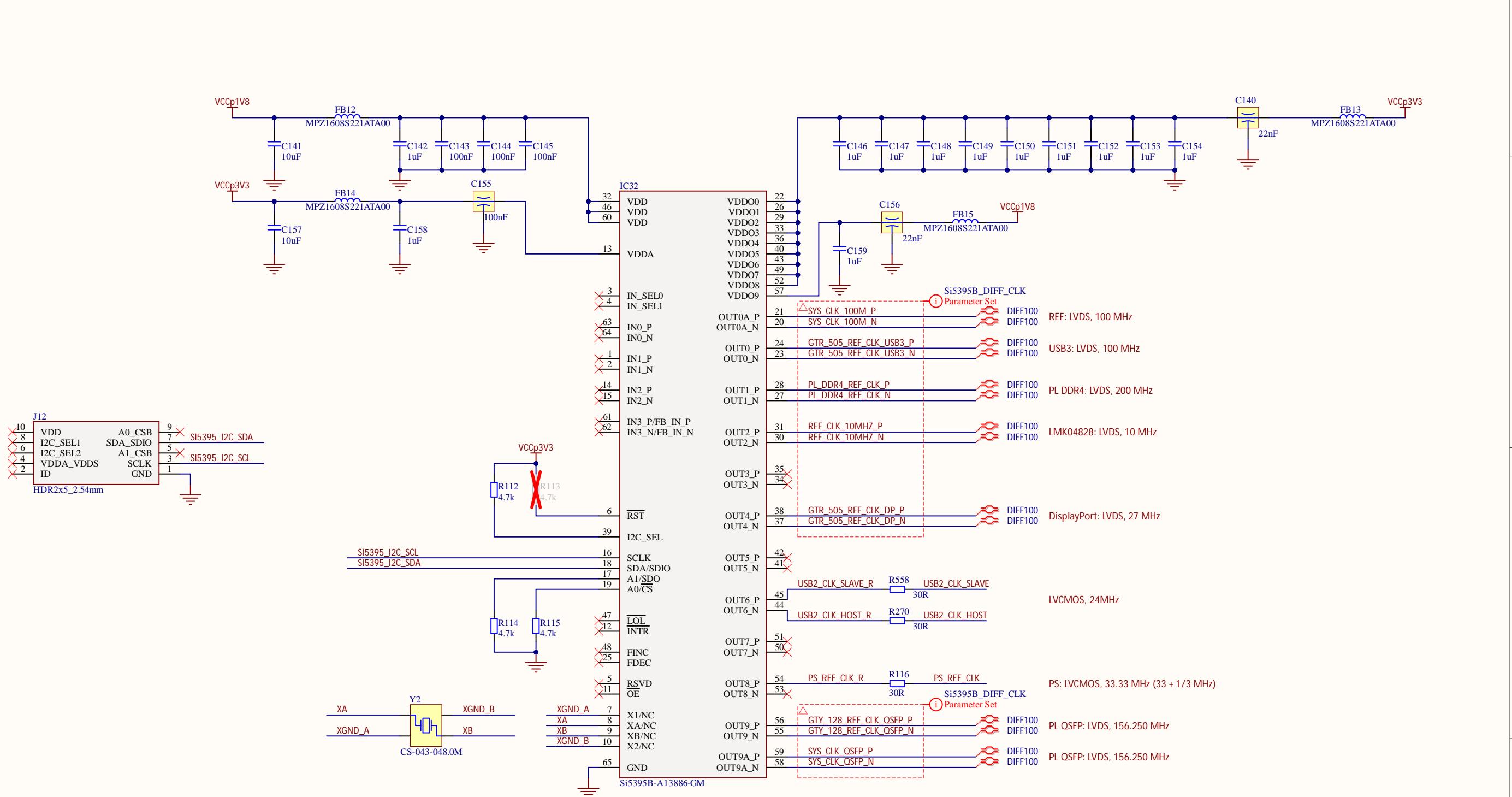
SC1	Screw, Phillips, M2, 6mm	STDF1	SMD Standoff, M2, L:2.5mm
	M2, 6mm	STDF2	SMD Standoff, M2, L:2.5mm
SC2	Screw, Phillips, M2, 6mm	STDF3	SMD Standoff, M2, L:2.5mm
	M2, 6mm	STDF4	SMD Standoff, M2, L:2.5mm
SC3	Screw, Phillips, M2, 6mm		9774025243R
	M2, 6mm		9774025243R
SC4	Screw, Phillips, M2, 6mm		9774025243R
	M2, 6mm		9774025243R



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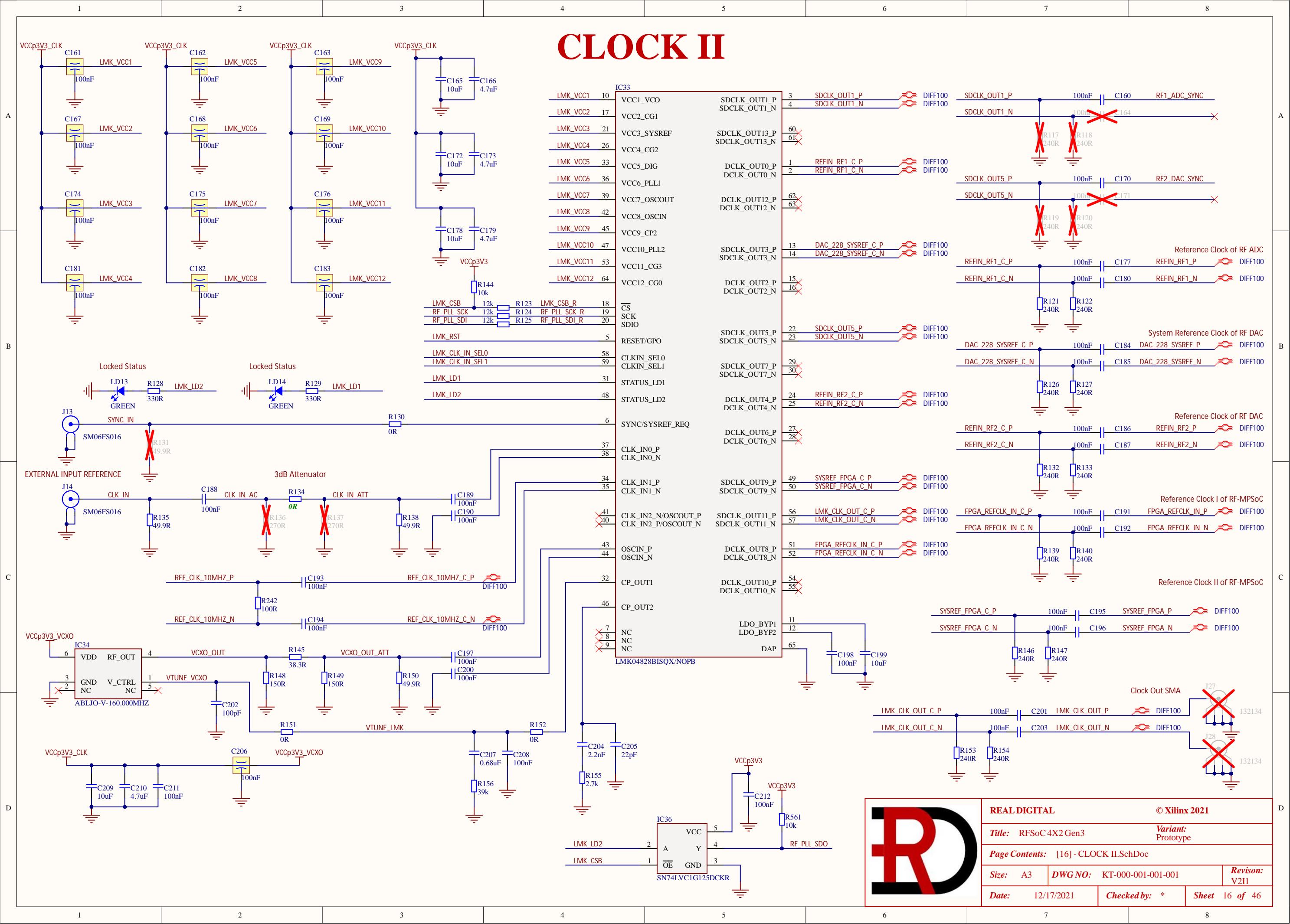
D

CLOCK I: SYS, DDR4, MGT, GTY AND USER

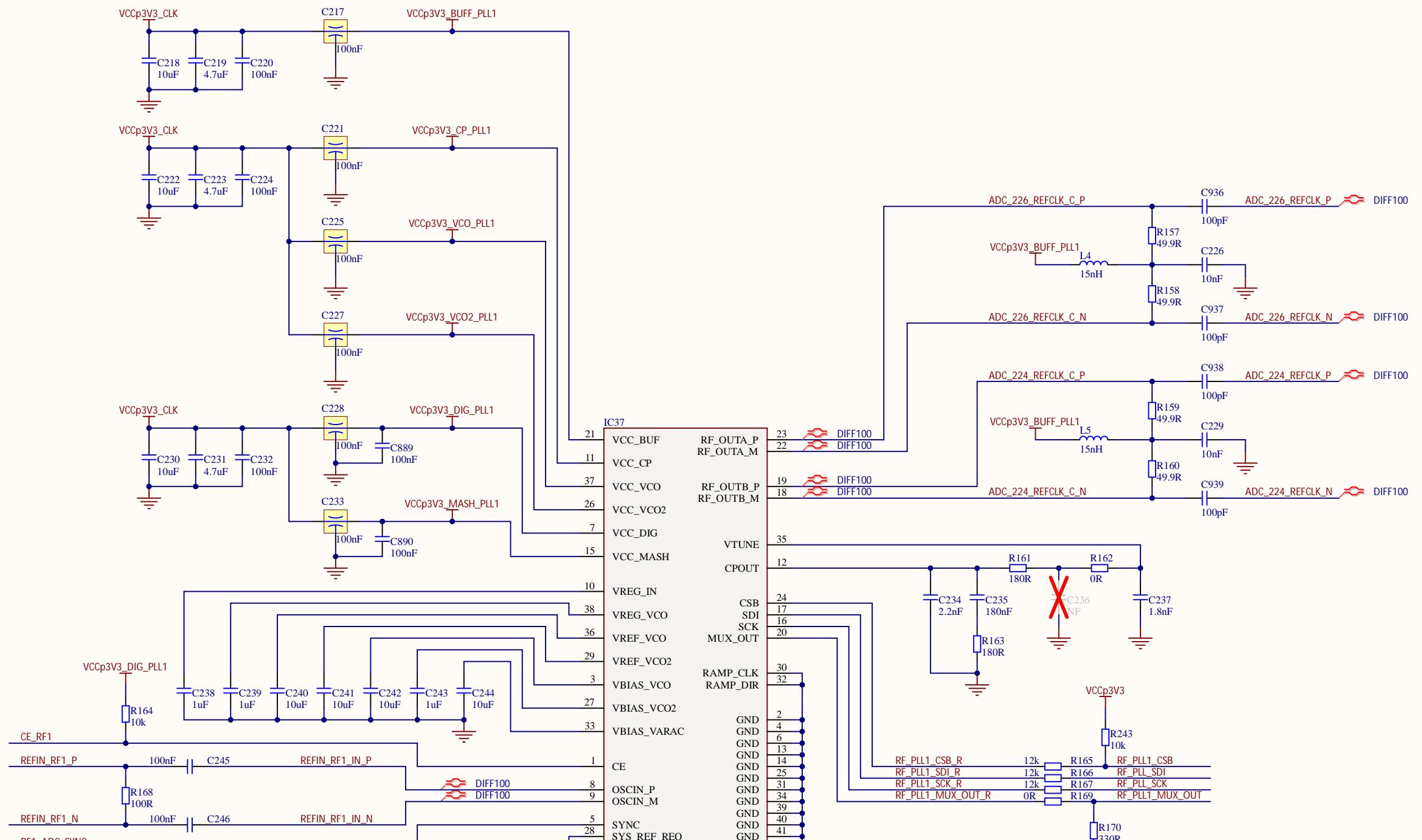


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CLOCK II

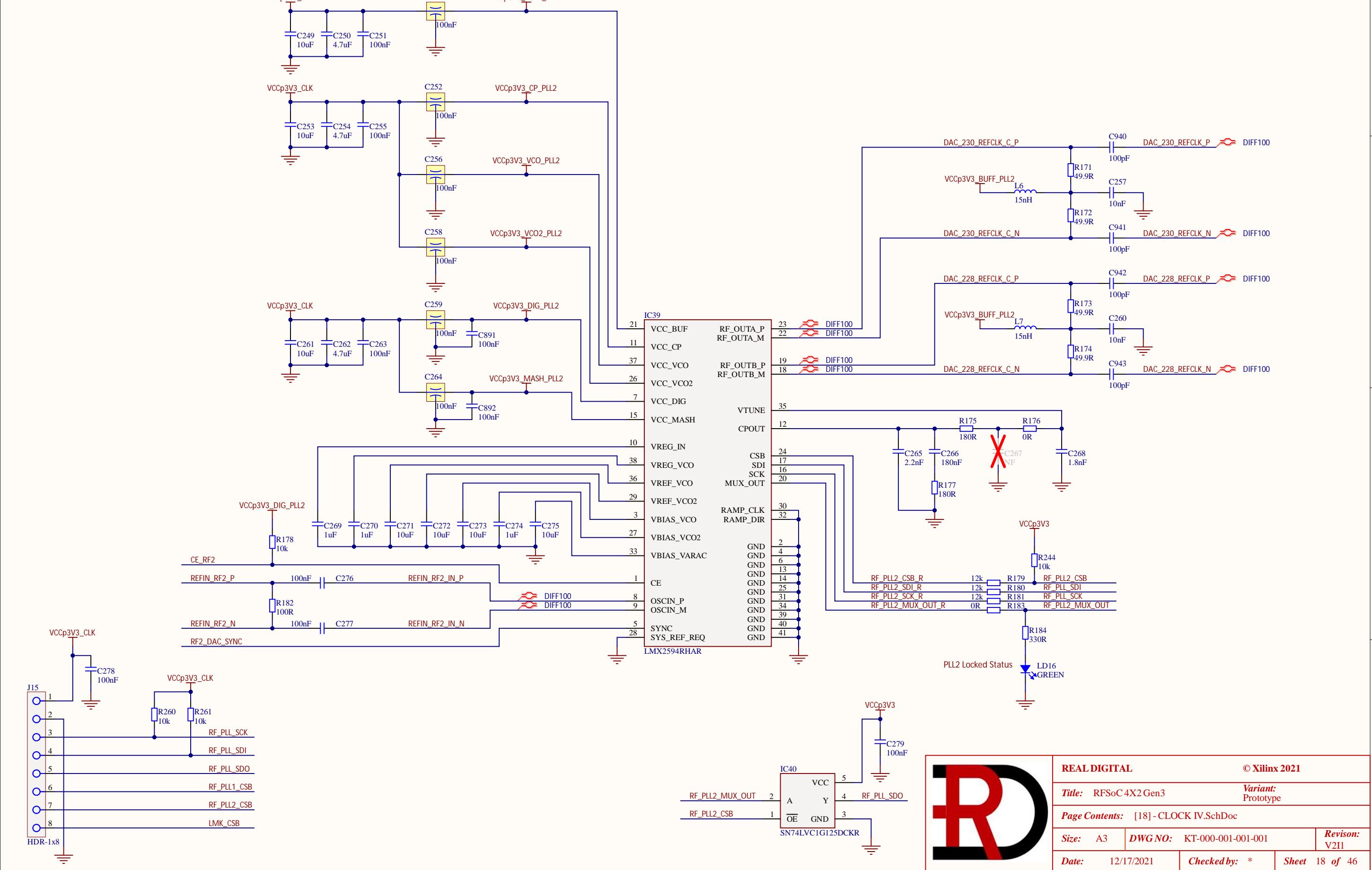


CLOCK III: RF ADC CLOCK

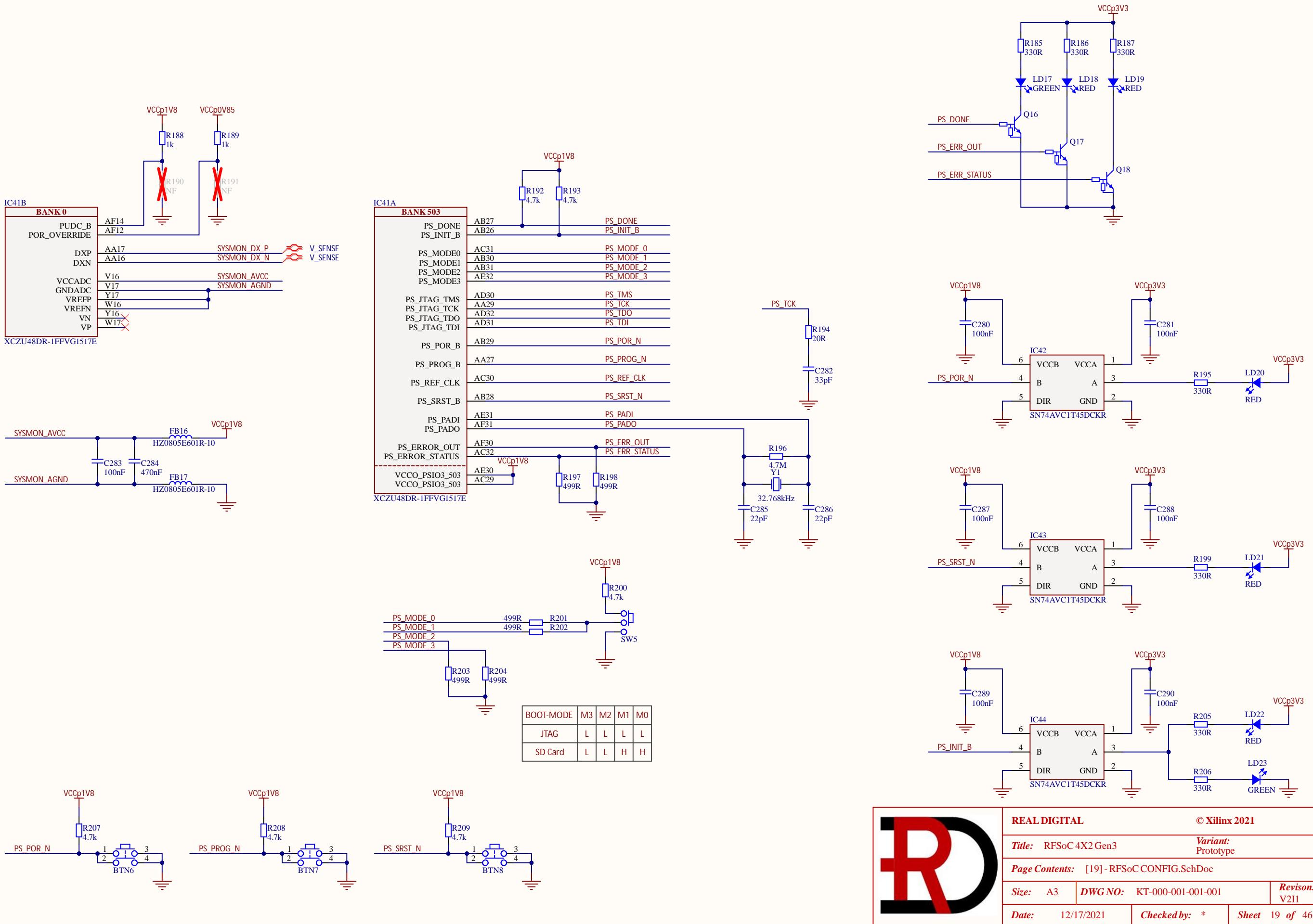


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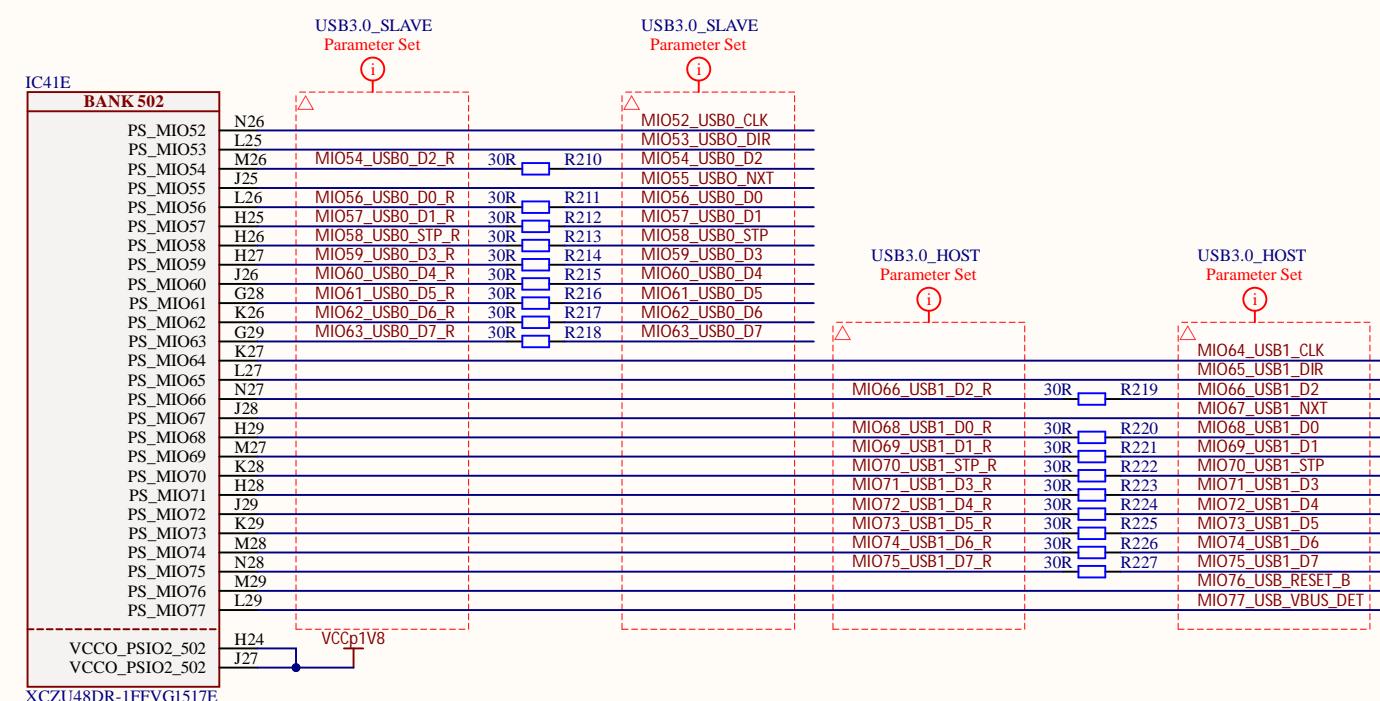
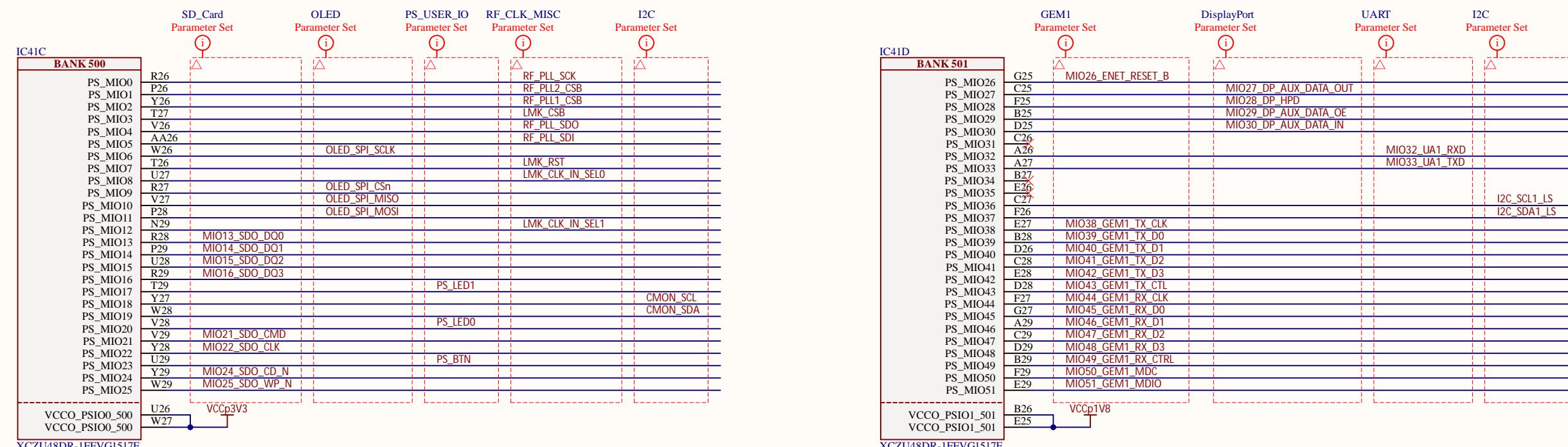
CLOCK IV: RF DAC CLOCK



RFSoC CONFIG

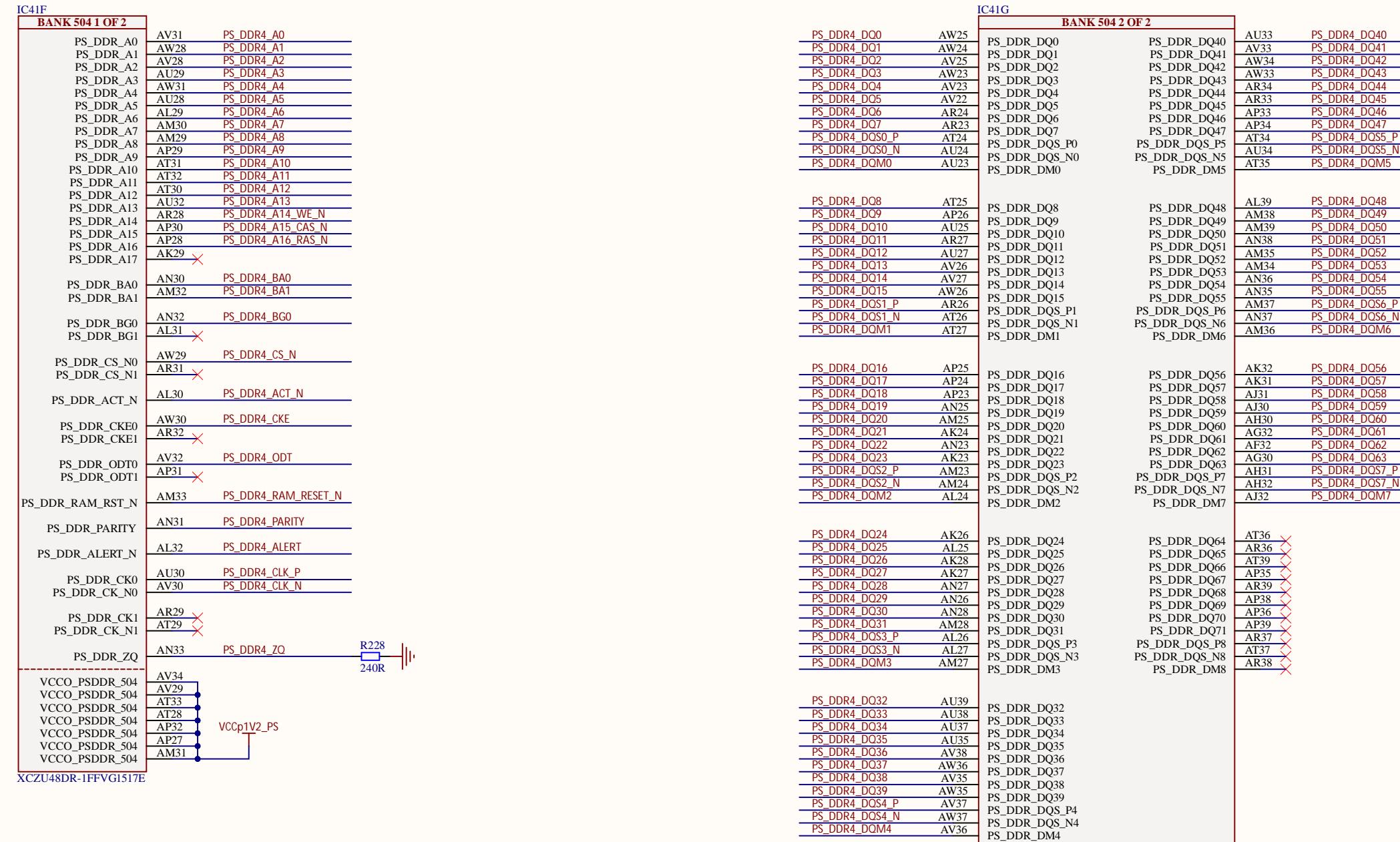


PS: BANKS 500-502

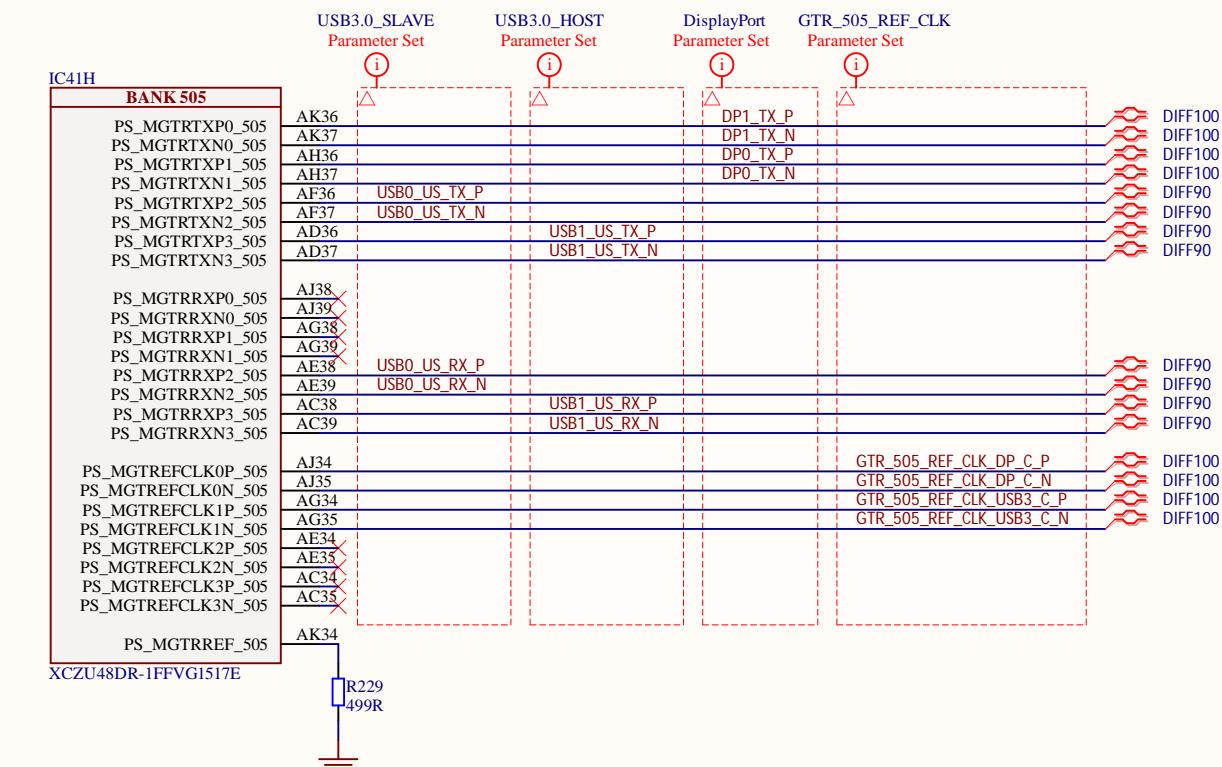


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PS: BANK 504

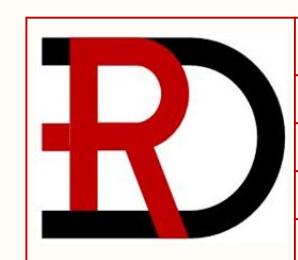


PS: MGT



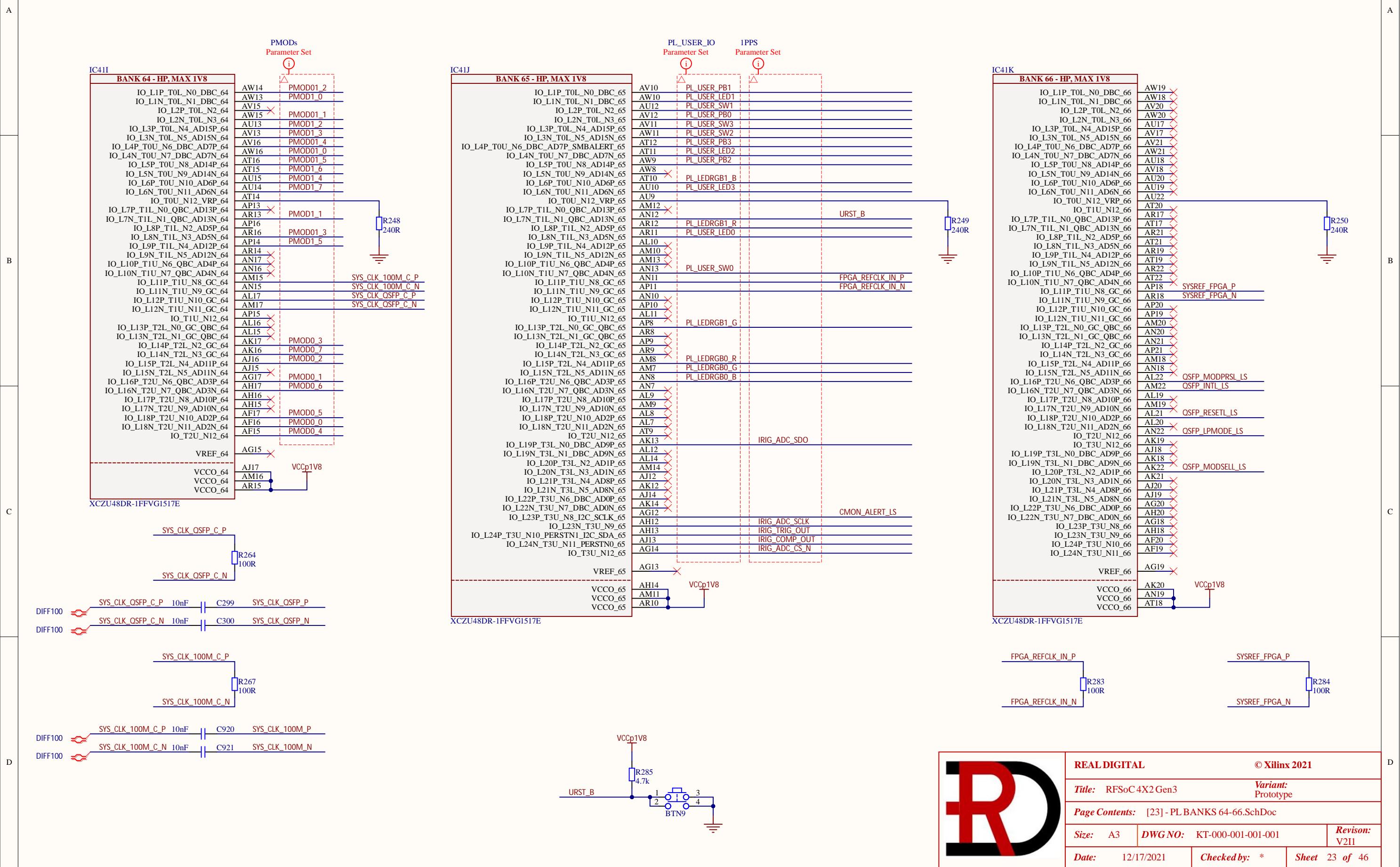
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GTR_505_REF_CLK_USB3_C_P 10nF || C293 GTR_505_REF_CLK_USB3_P
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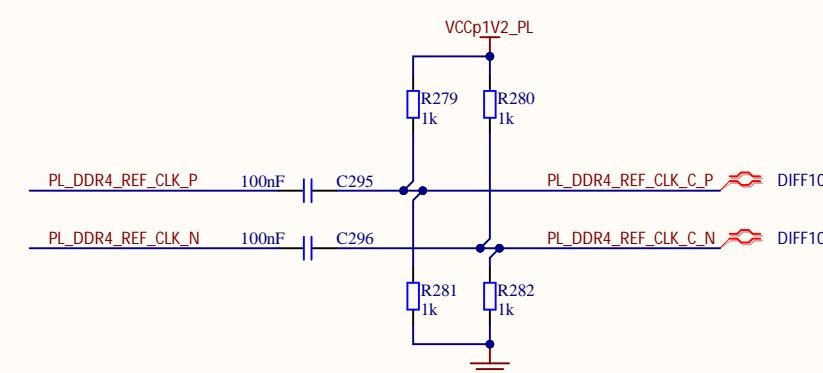
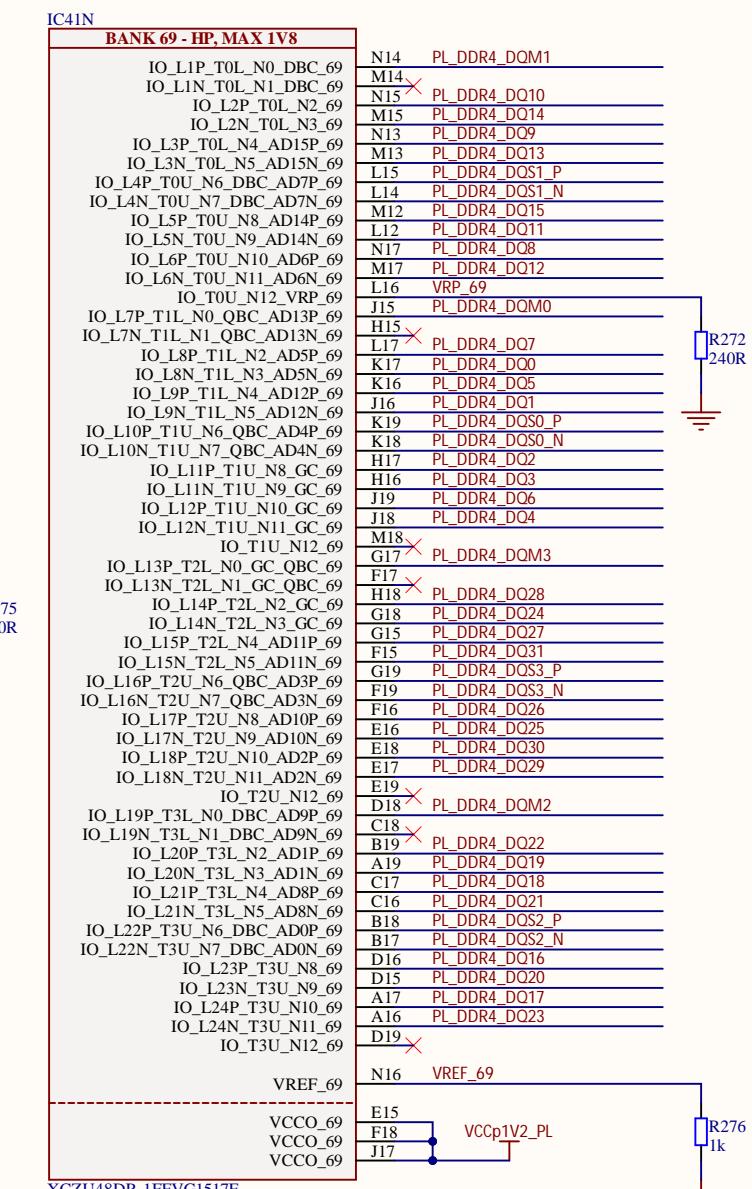
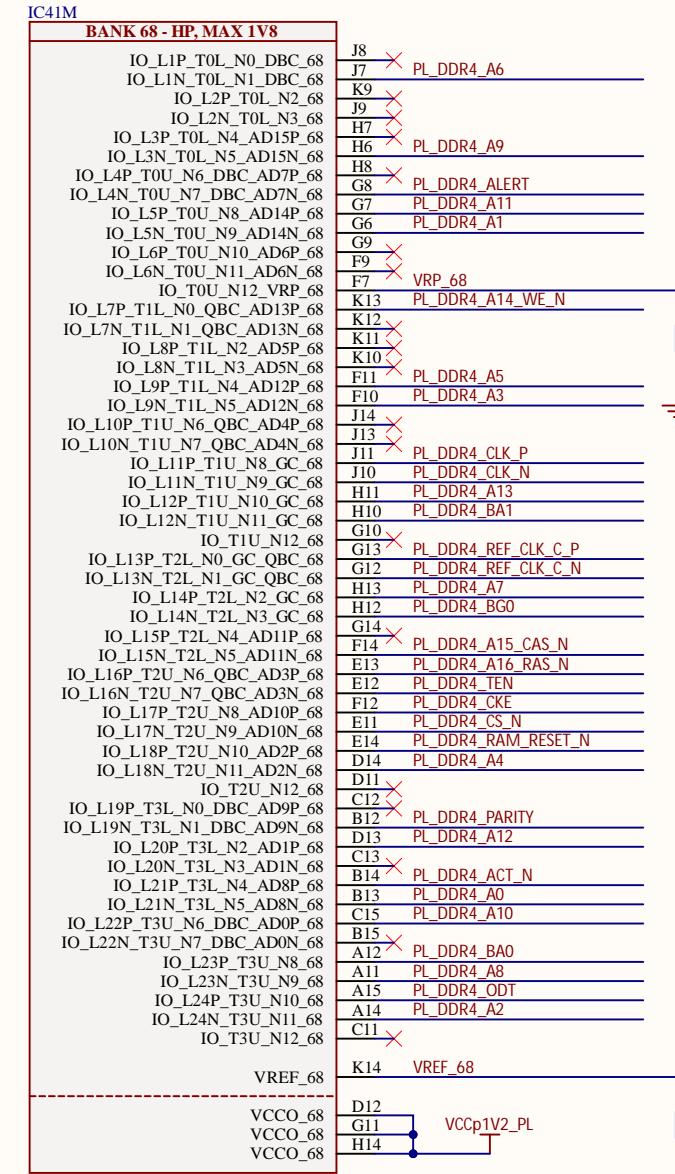
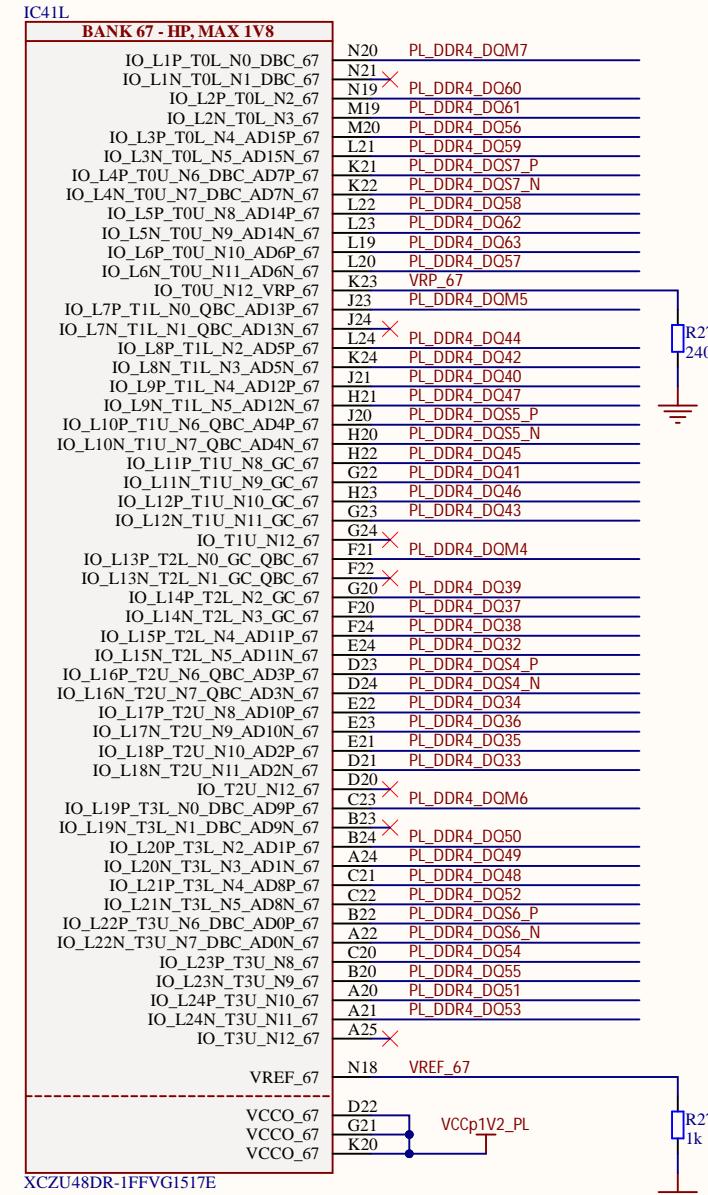
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PL: BANKS 64-66



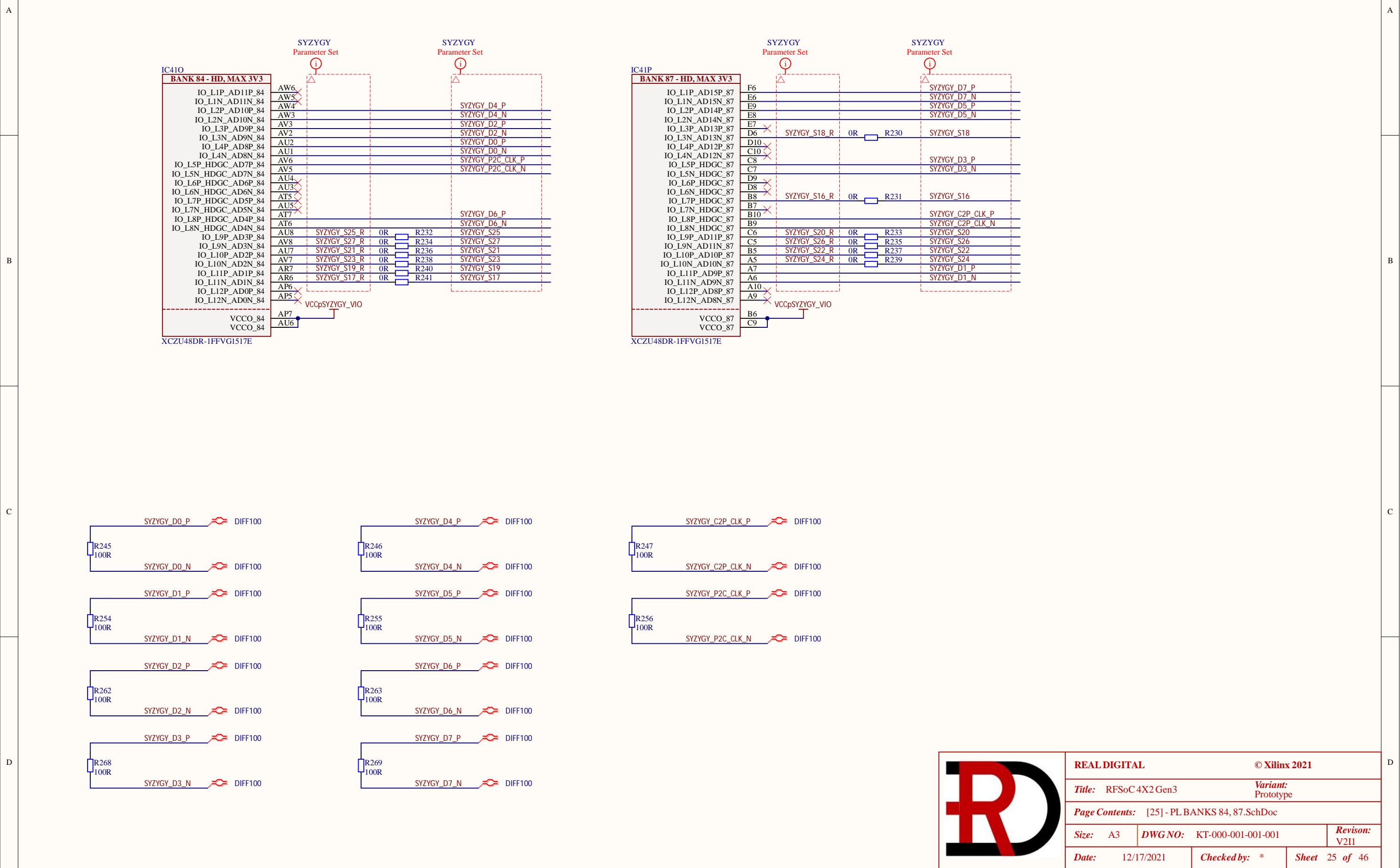
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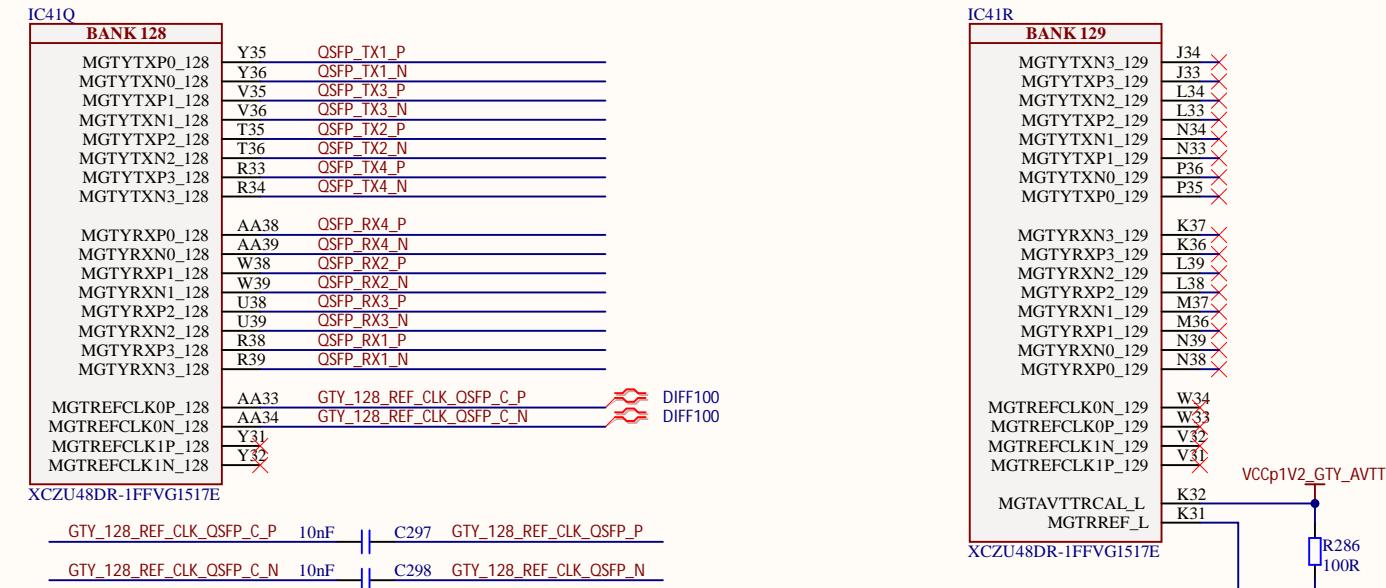
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PL: BANKS 84, 87



PL: GTY

A A

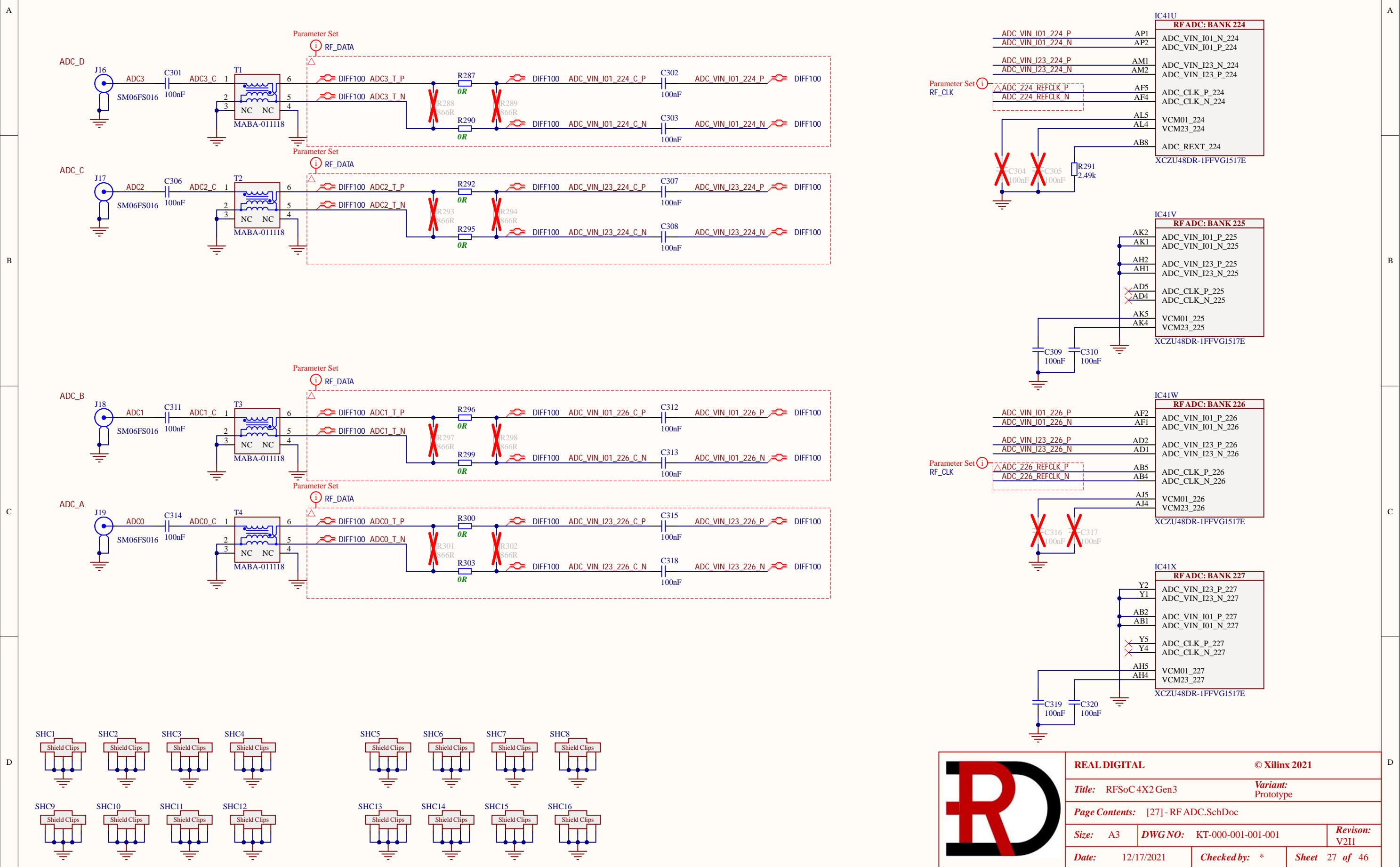


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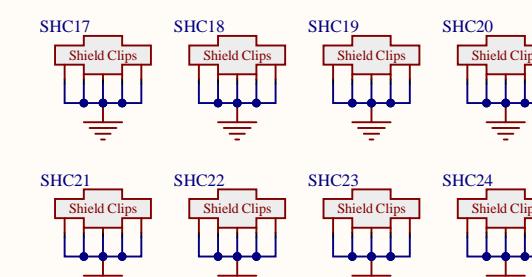
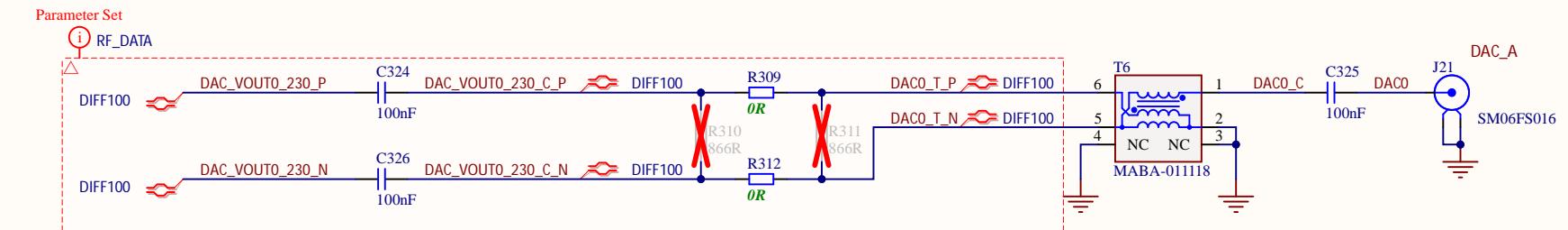
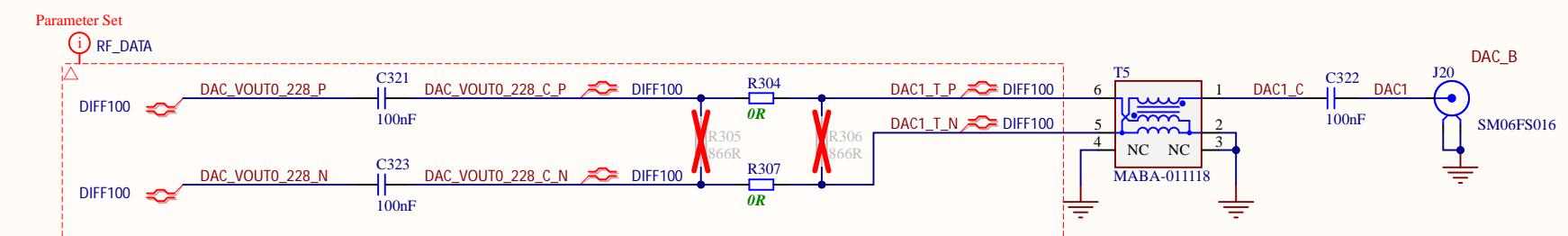
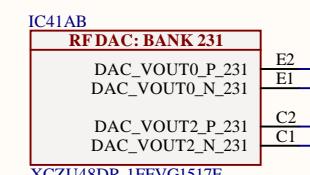
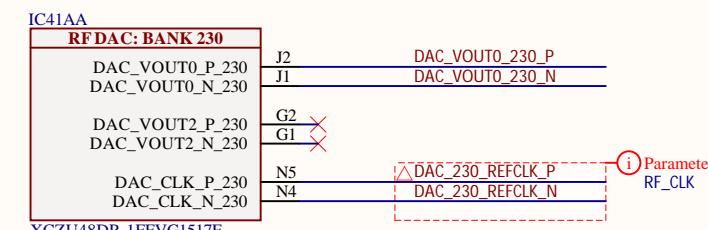
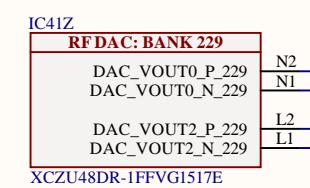
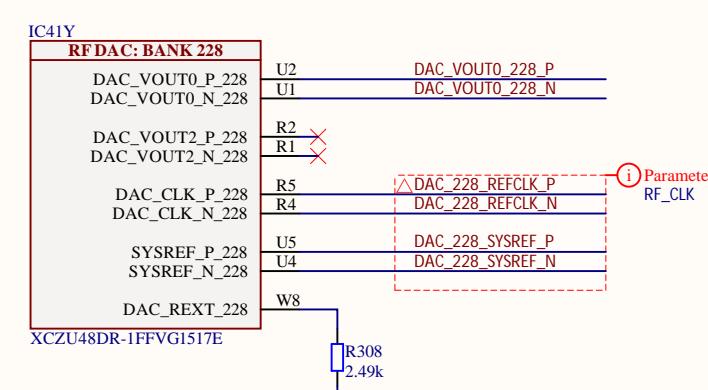


C C

RF ADC

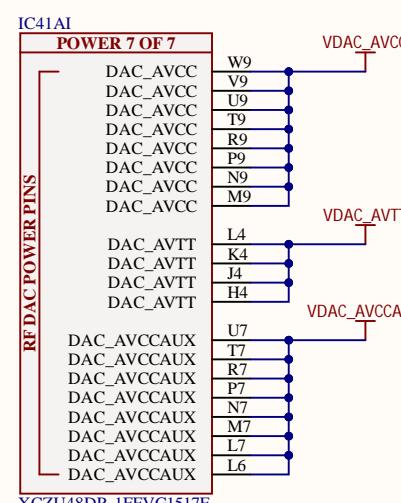
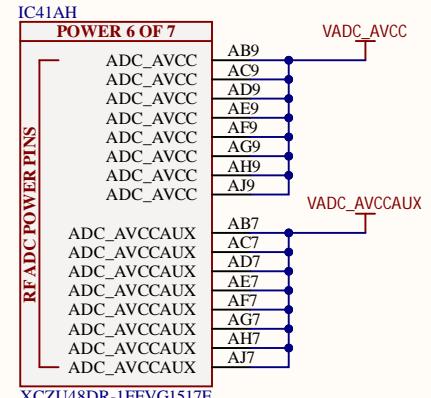
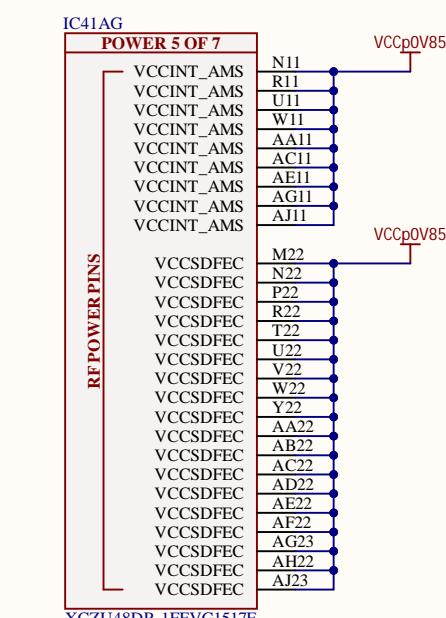
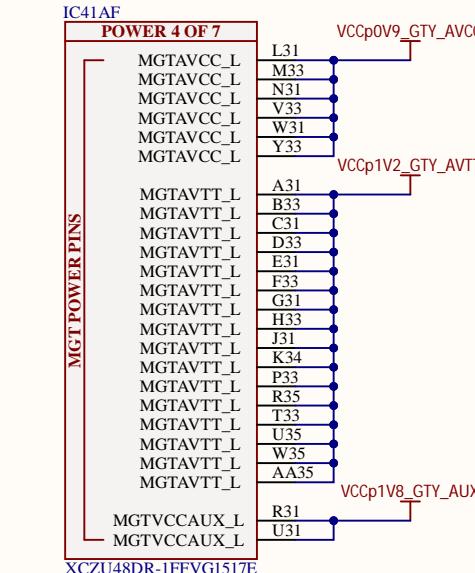
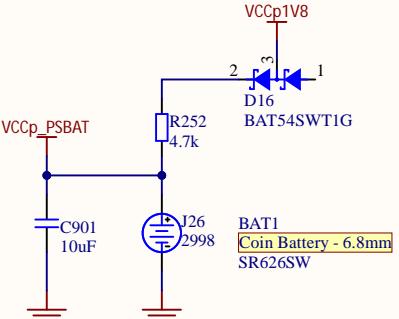
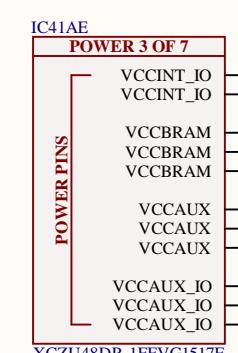
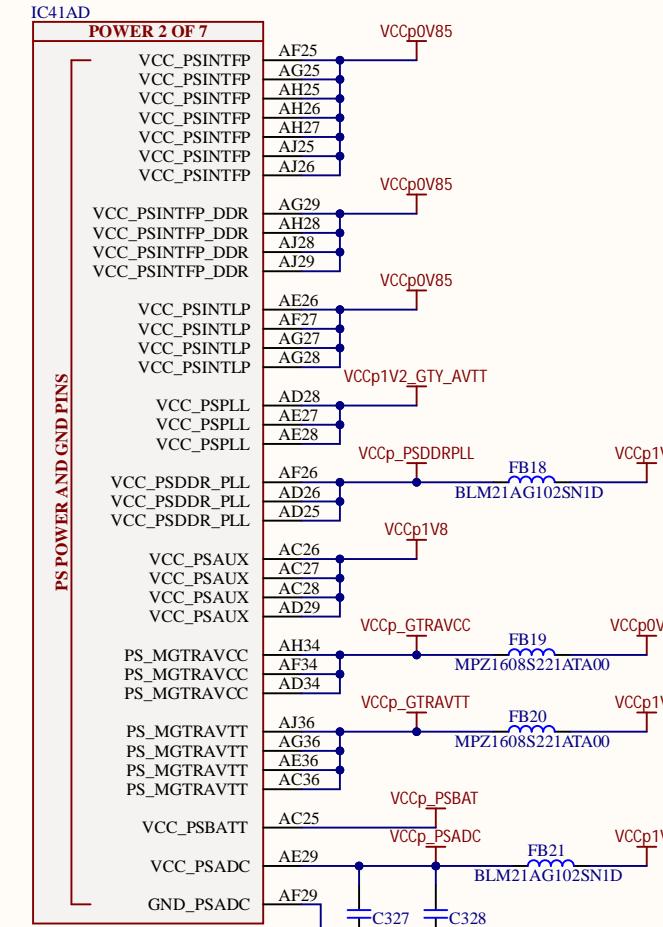
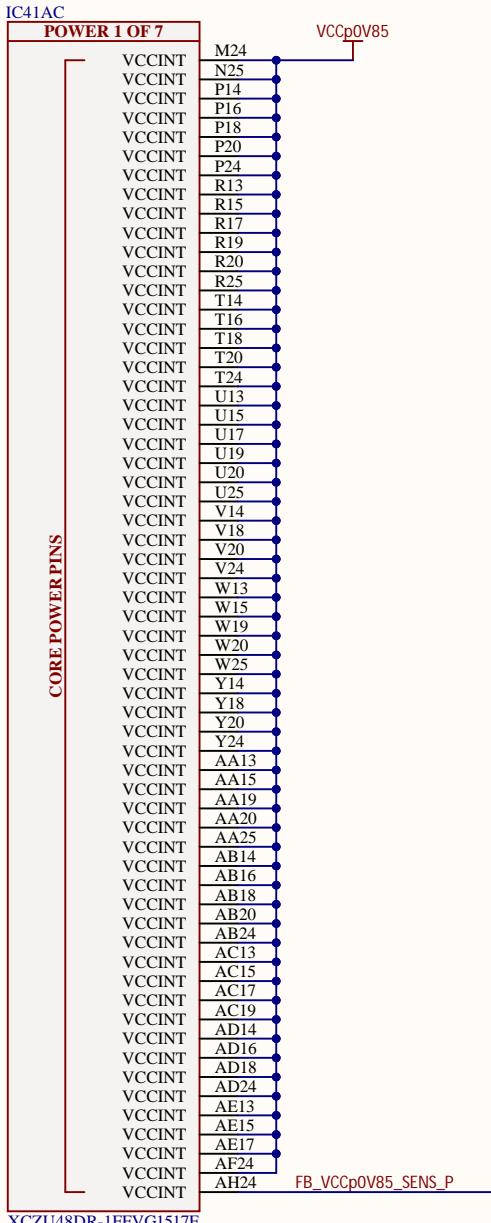


RF DAC



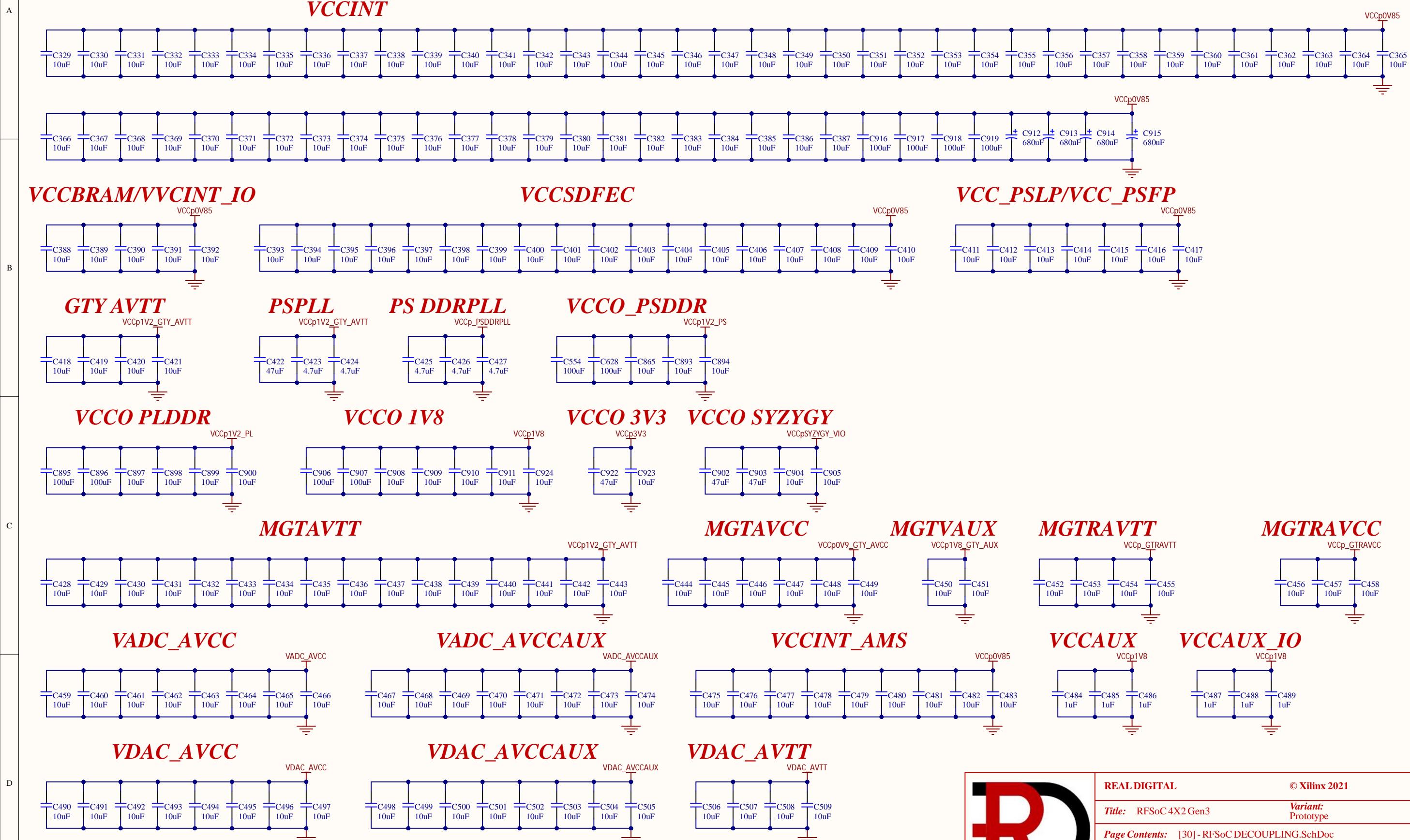
REAL DIGITAL		© Xilinx 2021
Title:	RFSoc 4X2 Gen3	Variant: Prototype
Page Contents:	[28]- RF DAC.SchDoc	
Size:	A3	DWG NO: KT-000-001-001 Revision: V2I1
Date:	12/17/2021	Checked by: *
		Sheet 28 of 46

RFSoC POWER Pins



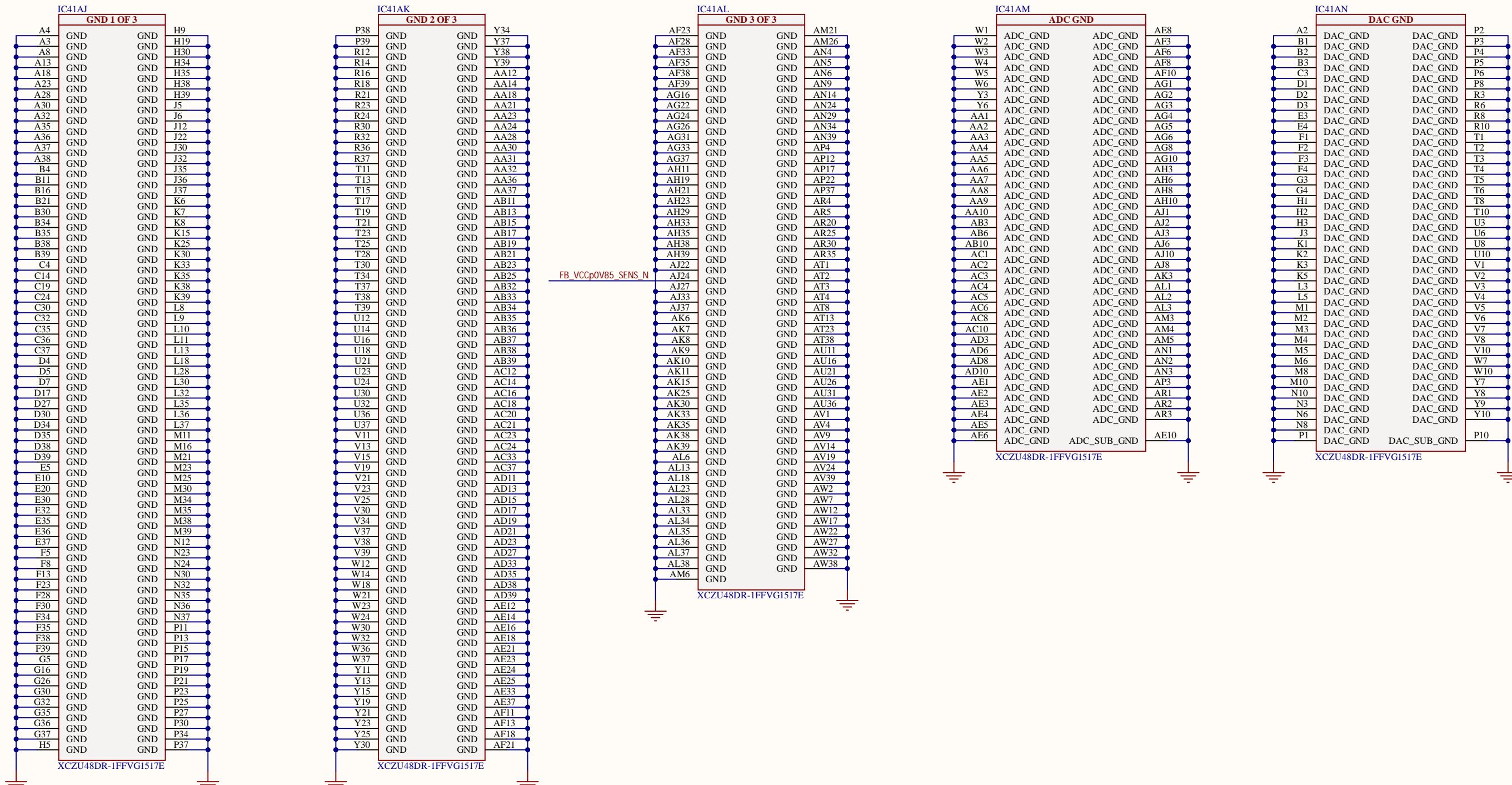
REAL DIGITAL	© Xilinx 2021
Title:	RFSoC 4X2 Gen3
Variant:	Prototype
Page Contents:	[29] - RFSoC POWER Pins.SchDoc
Size:	A3
DWG NO:	KT-000-001-001-001
Revision:	V2II
Date:	12/17/2021
Checked by:	*
Sheet	29 of 46

DECOUPLING



REAL DIGITAL	© Xilinx 2021
Title:	RFSoC 4X2 Gen3
Variant:	Prototype
Page Contents:	[30] - RFSoC DECOUPLING.SchDoc
Size:	A3
DWG NO:	KT-000-001-001-001
Revision:	V2II
Date:	12/17/2021
Checked by:	*
Sheet	30 of 46

RFSoC GND Pins



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Tut - BES - C4V2G - 3

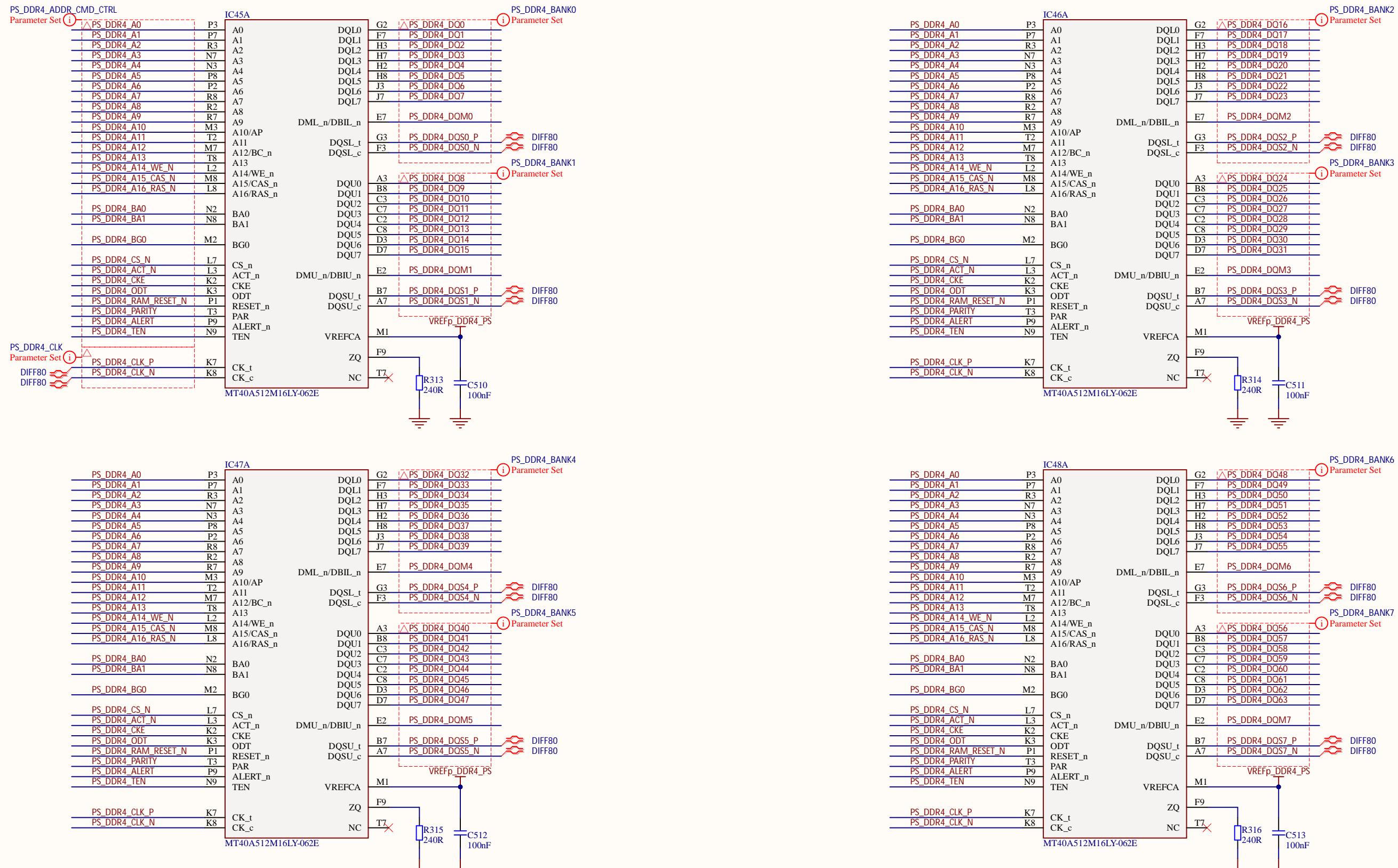
Variant:
Prototype

Page Contents: [31] BESeC GND Pins SchDoc

.SchDoc

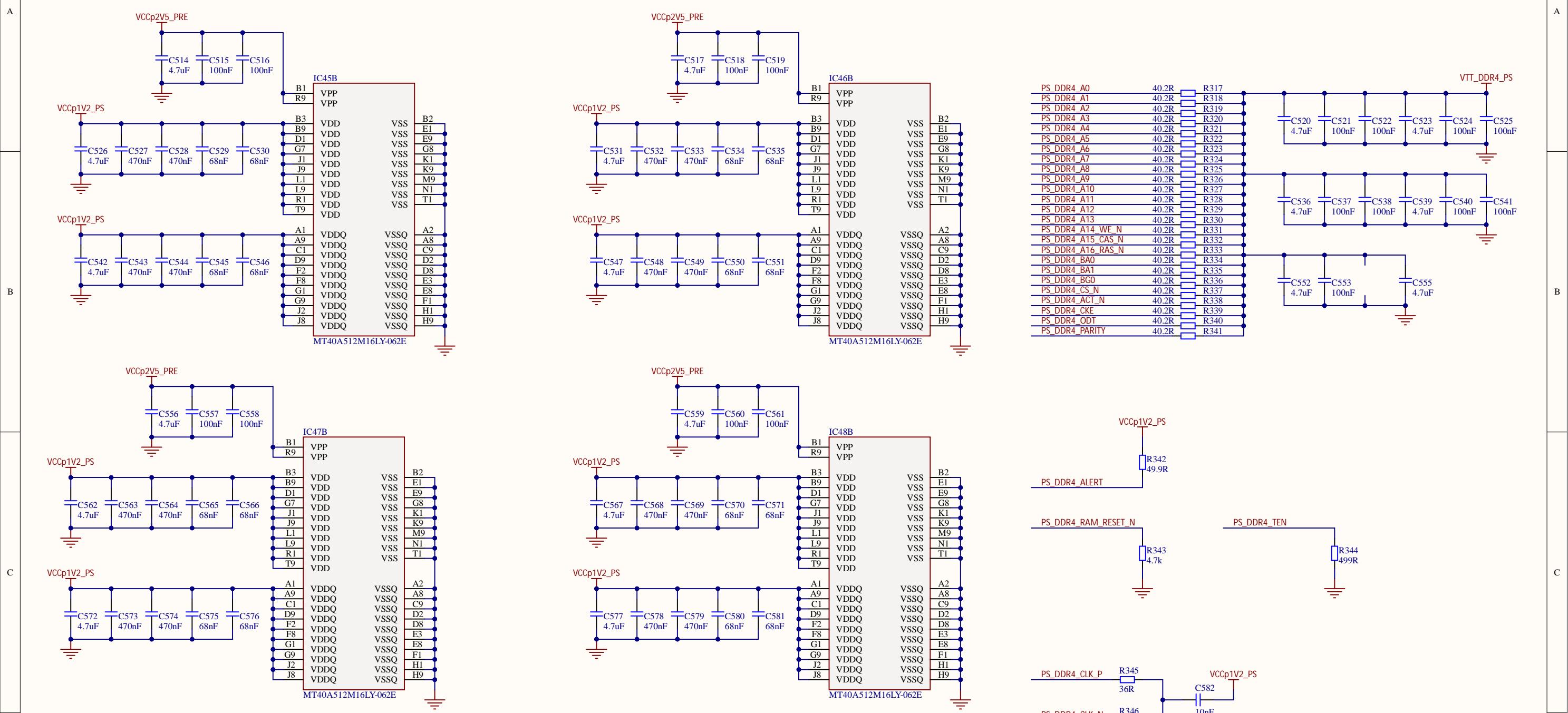
Page 12 of 14 | Last updated: 12/17/2021 | Generated: 12/17/2021 at 10:46 AM | Version: 21.6.46

DDR4 MEMORY PS I



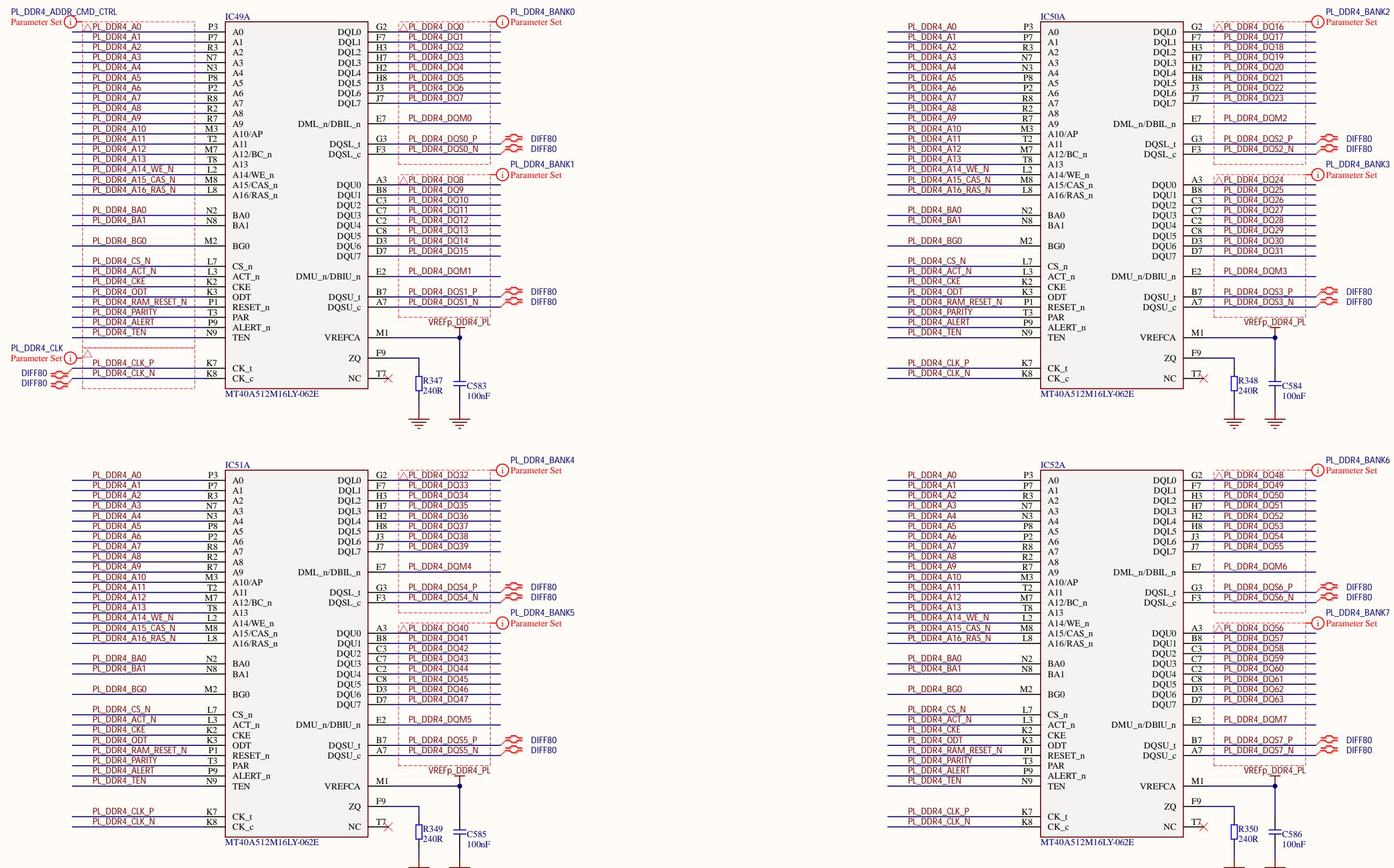
REAL DIGITAL		© Xilinx 2021	
Title:	RFSoc 4X2 Gen3	Variant:	Prototype
Page Contents: [32] - DDR4 MEMORY PS I.SchDoc			
Size: A3	DWG NO: KT-000-001-001-001	Revision:	V2II
Date: 12/17/2021	Checked by: *	Sheet:	32 of 46

DDR4 MEMORY PS II



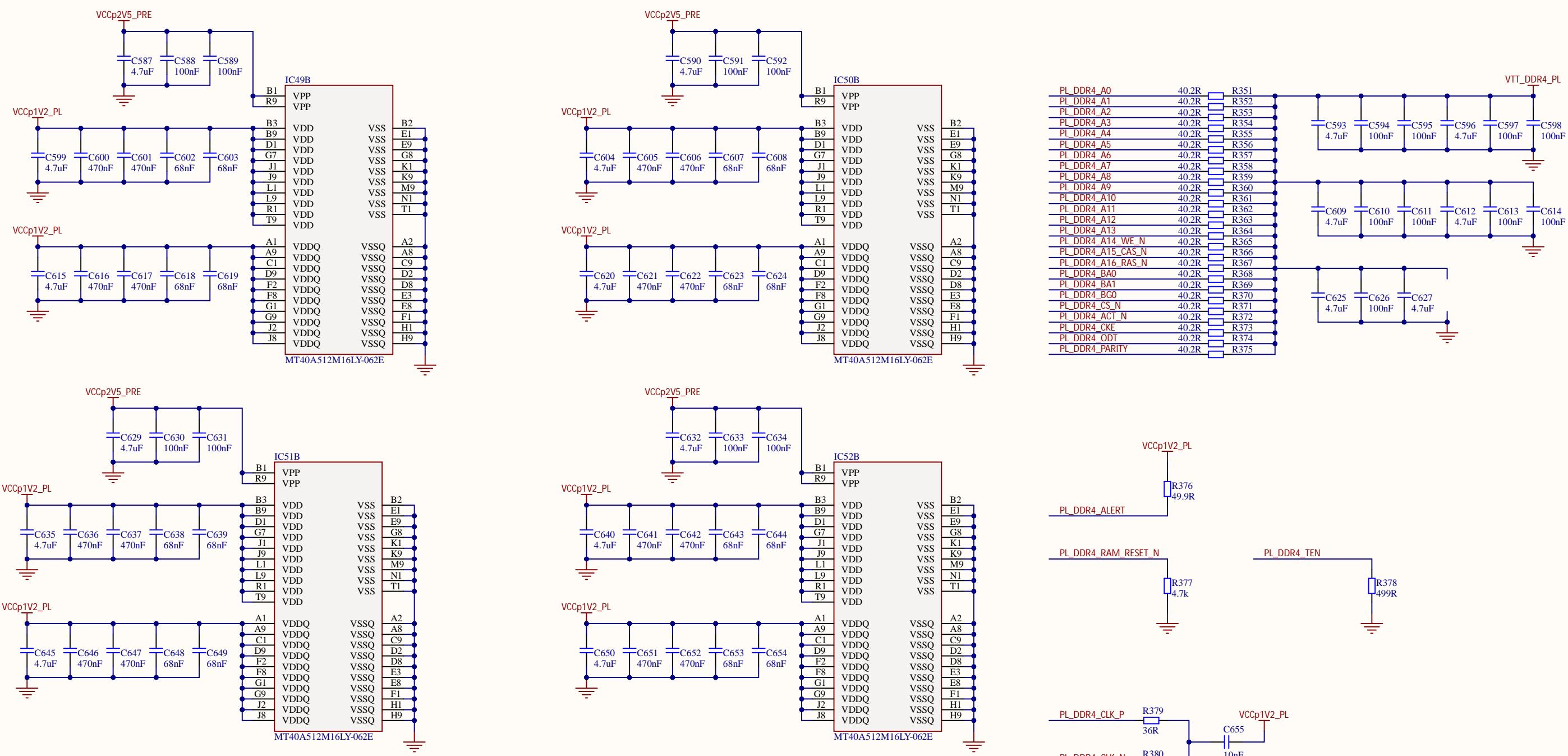
REAL DIGITAL		© Xilinx 2021
Title:	RFSoc 4X2 Gen3	Variant: Prototype
Page Contents:	[33] - DDR4 MEMORY PS II.SchDoc	
Size:	A3	DWG NO: KT-000-001-001-001 V2II
Date:	12/17/2021	Checked by: * Sheet: 33 of 46

DDR4 MEMORY PL I



REAL DIGITAL	© Xilinx 2021
Title: RFSoC 4X2 Gen3	Variant: Prototype
Page Contents: [34] - DDR4 MEMORY PLI.SchDoc	

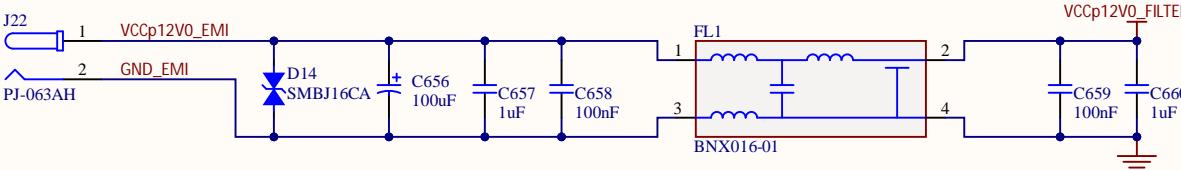
DDR4 MEMORY PL II



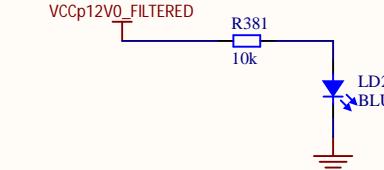
REAL DIGITAL	© Xilinx 2021		
Title: RFSoC 4X2 Gen3	Variant: Prototype		
Page Contents: [35] - DDR4 MEMORY PL II.SchDoc			
Size: A3	DWG NO: KT-000-001-001-001		Revision: V2II
Date: 12/17/2021	Checked by: *	Sheet	35 of 46

POWER INPUT AND FAN CONTROLLER

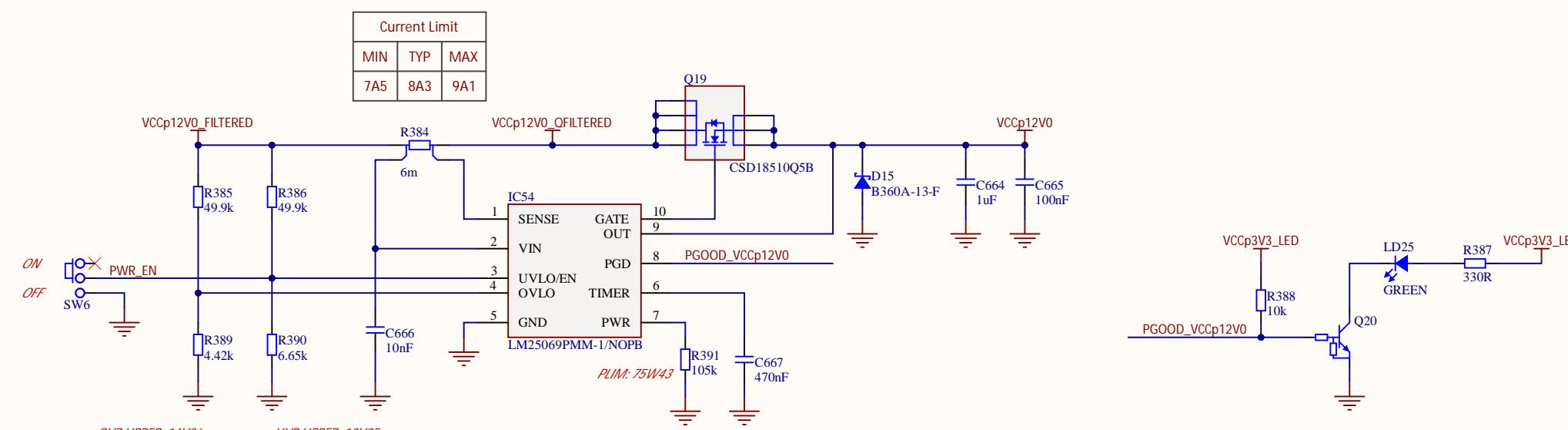
EMI Filter



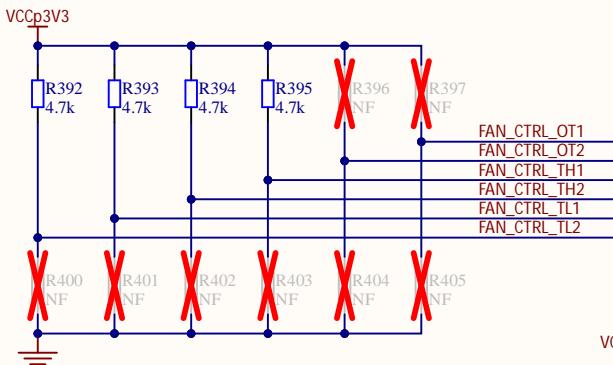
12V0 LED



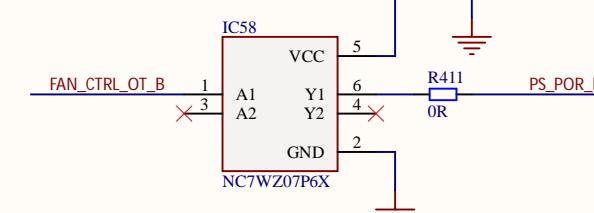
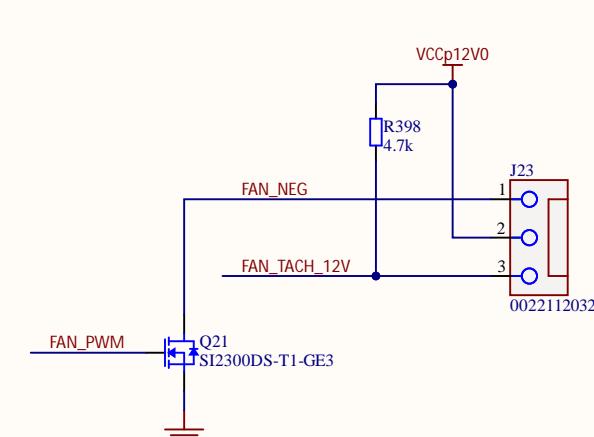
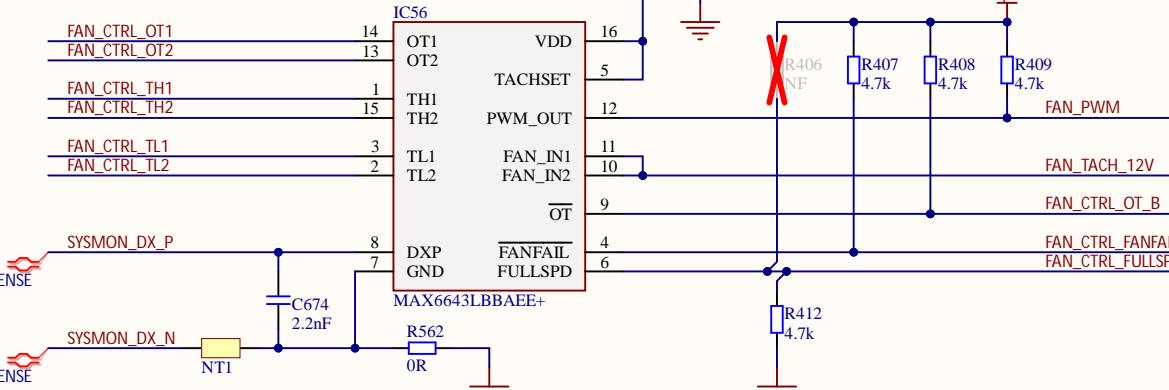
Input Protection (OVP, UVP, ILIM, PLIM)



HS1
Heatsink+Fan
FA+K30B+T725

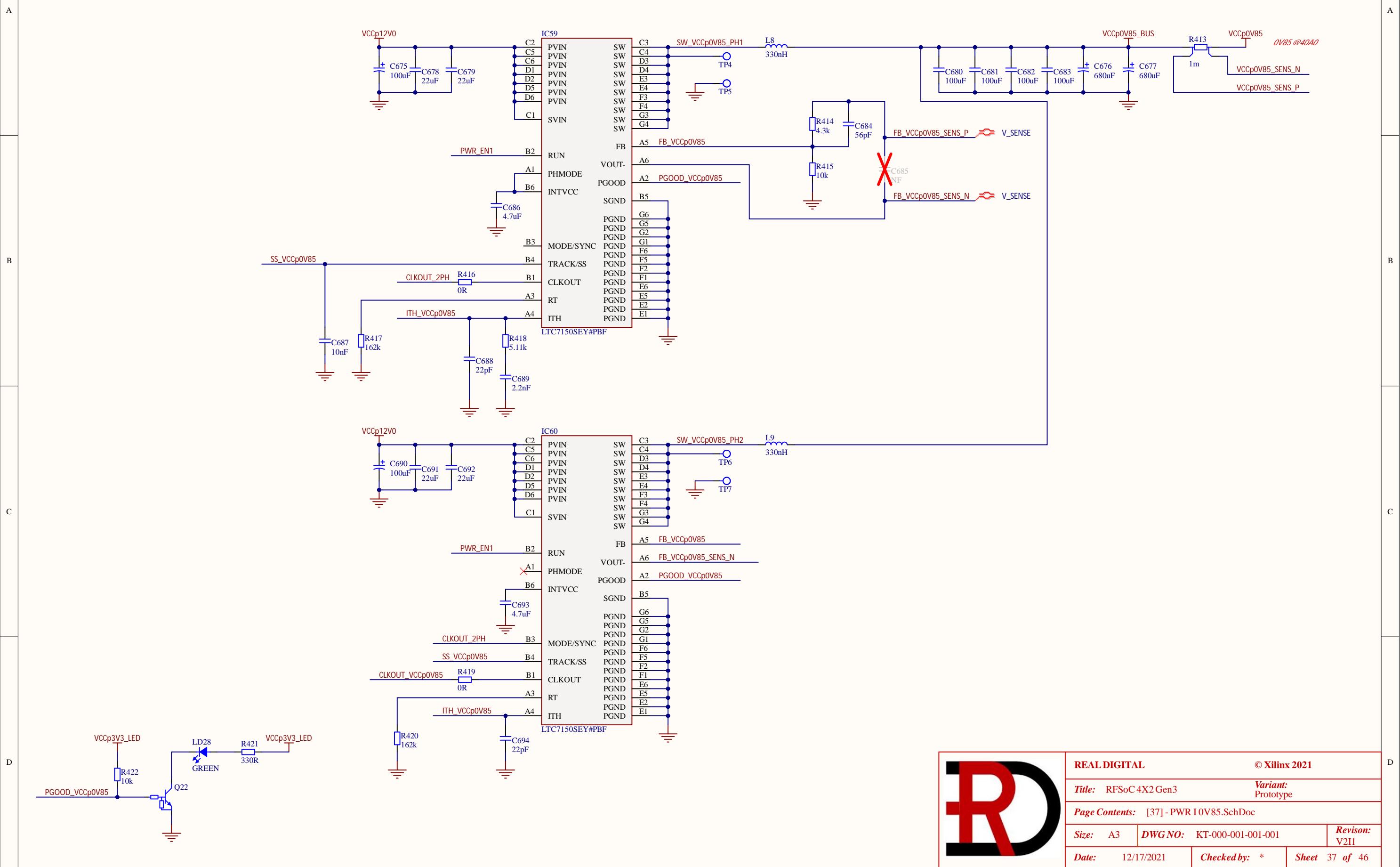


Fan Controller

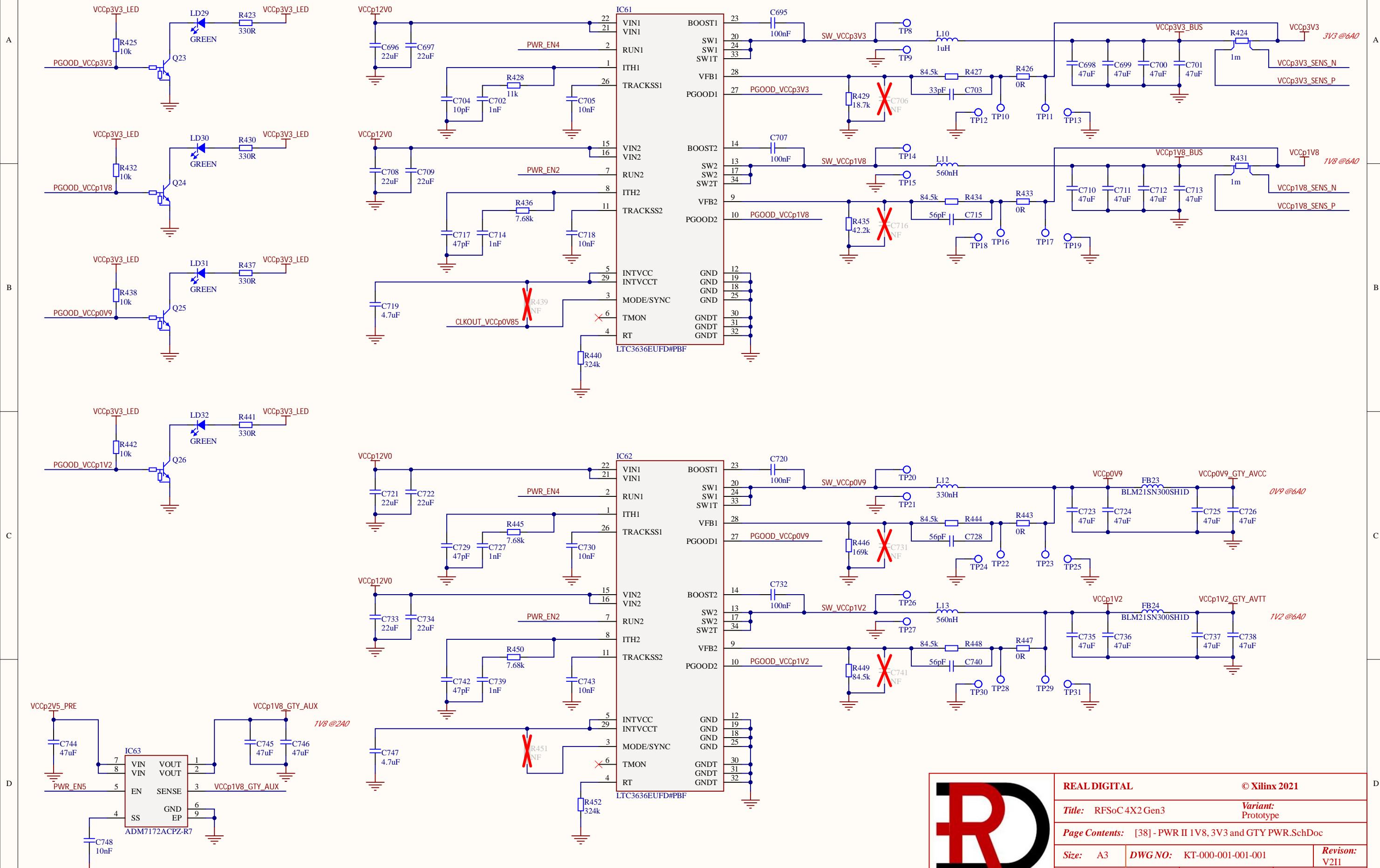


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Title:	RFSoc 4X2 Gen3	Variant: Prototype
Page Contents:	[36] - PWR INPUT AND FAN CONTROLLER.SchDoc	
Size:	A3	DWG NO: KT-000-001-001
Date:	12/17/2021	Checked by: * Sheet 36 of 46
Revision:	V2II	

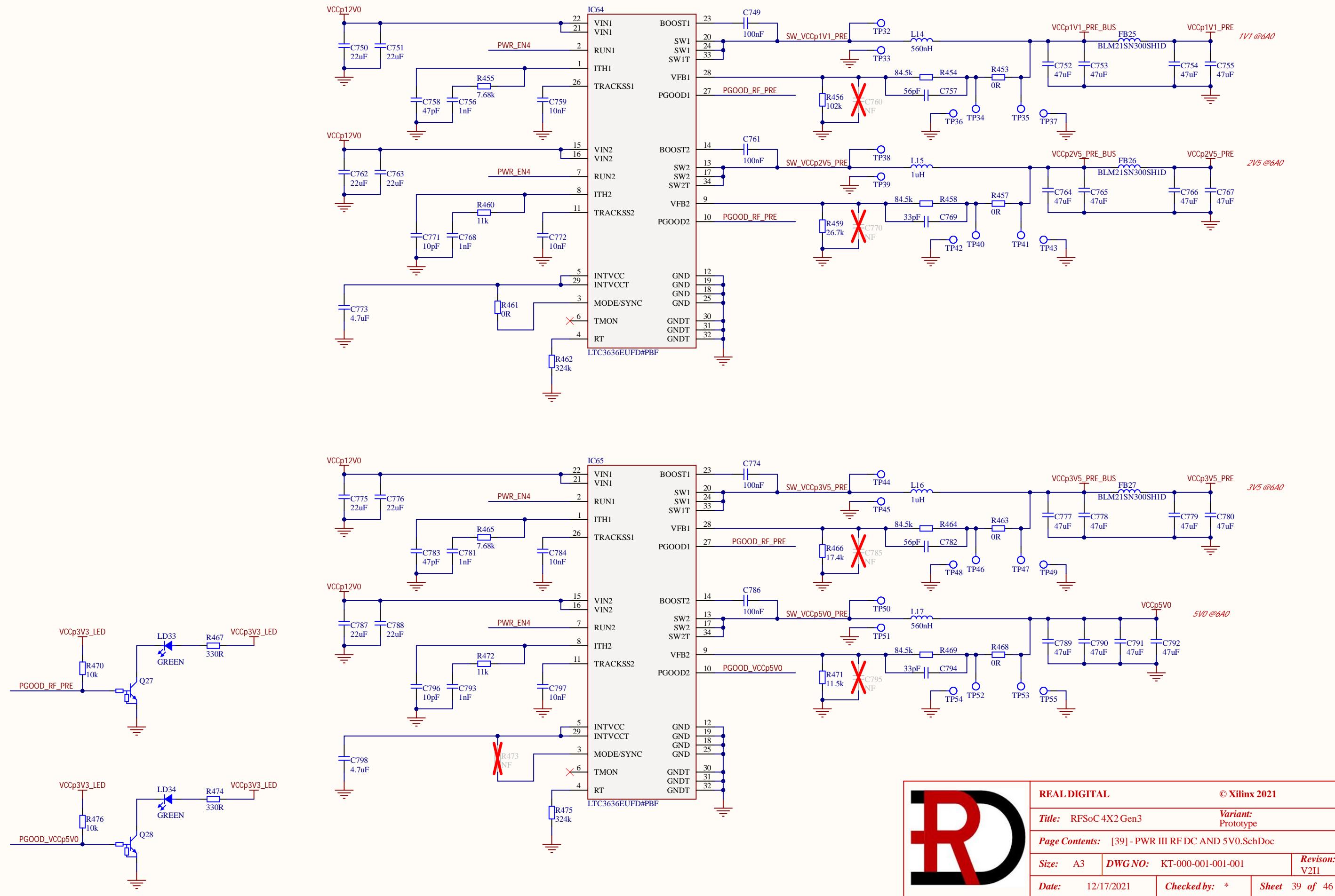
POWER I: VCCp0V85



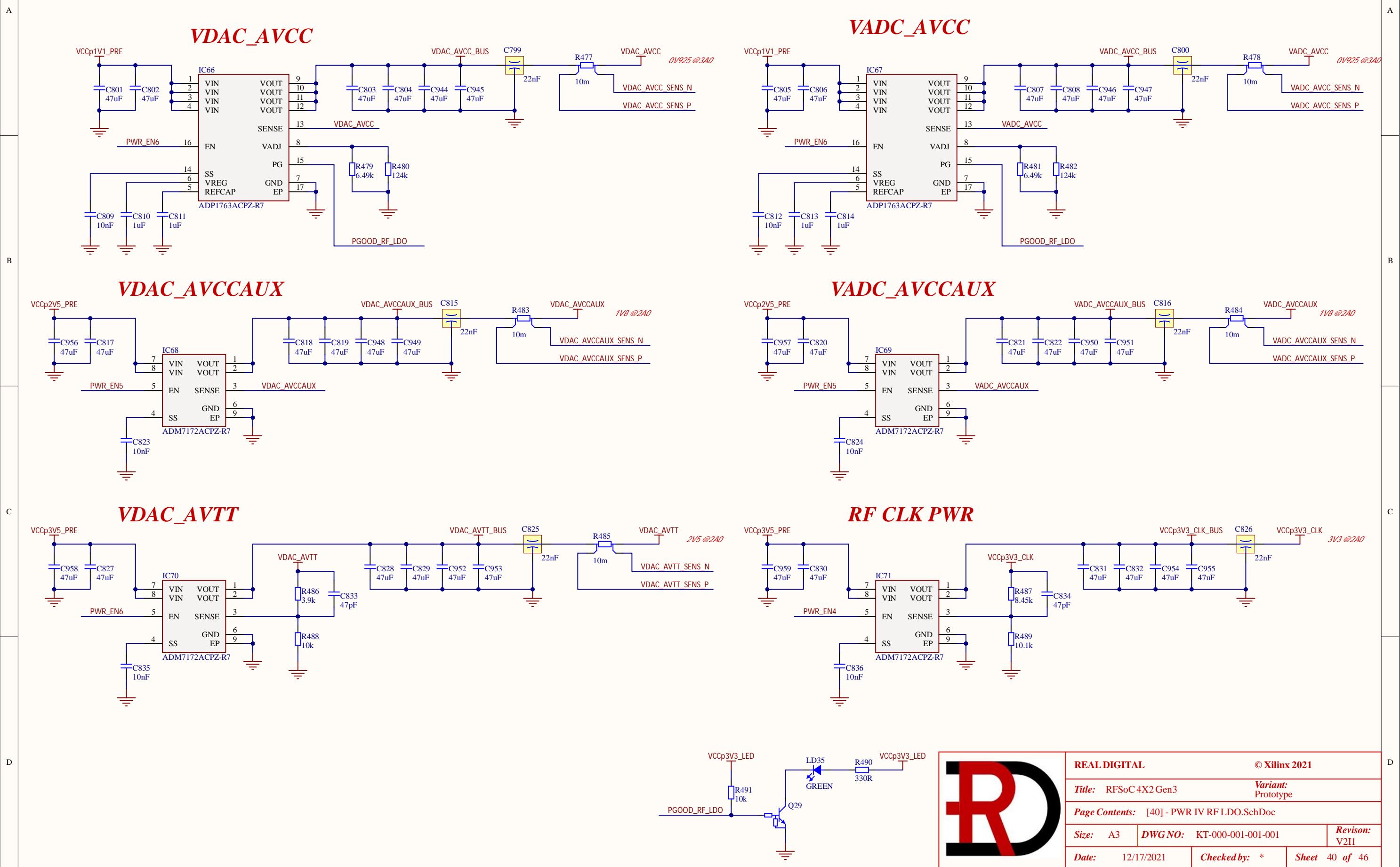
POWER II: VCCp1V8, VCCp3V3 and GTY PWR



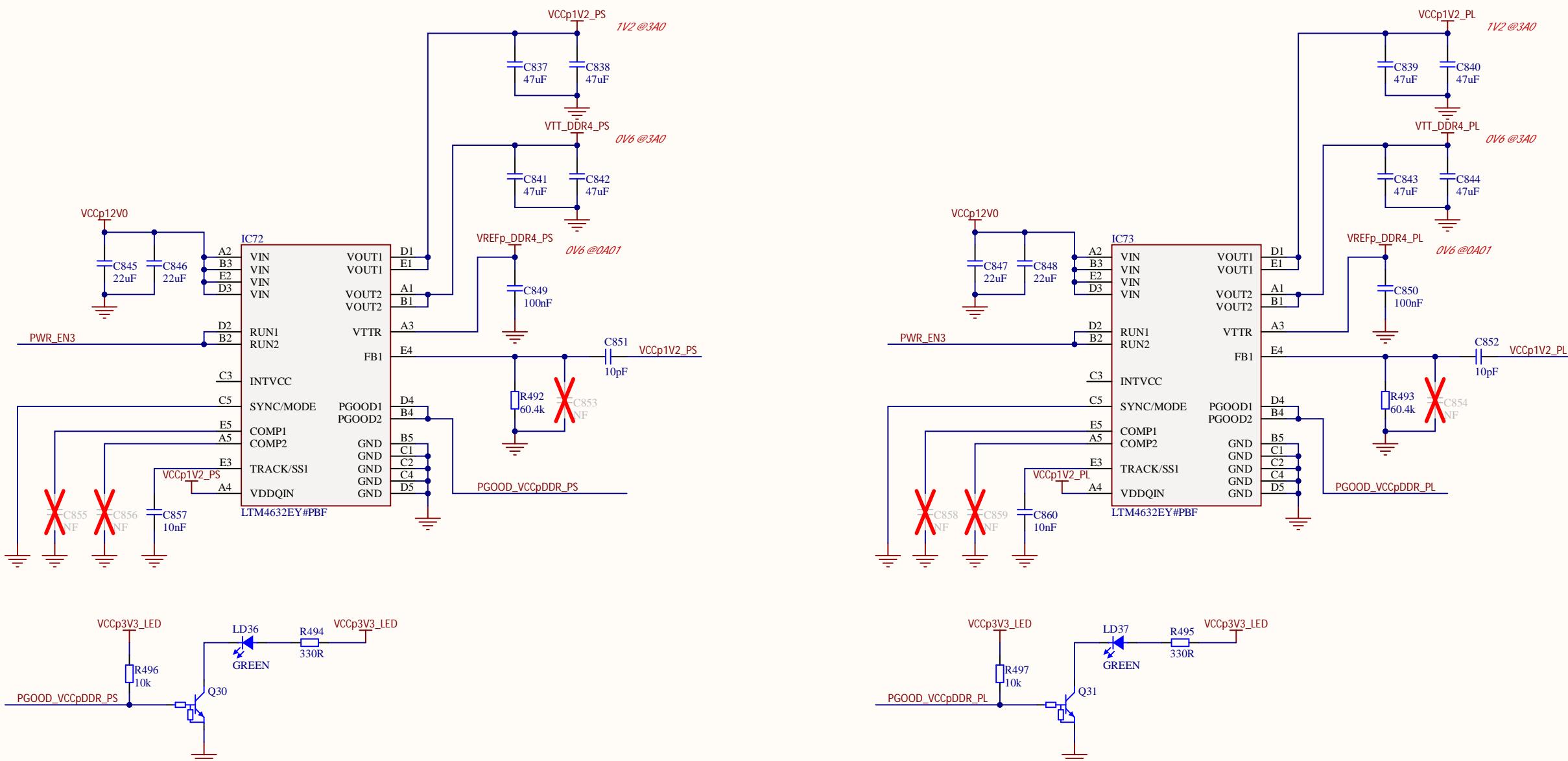
POWER III: RF DC/DC AND 5V0



POWER IV: RF LDO



POWER V: DDR4



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Title: RFSoc 4X2 Gen3

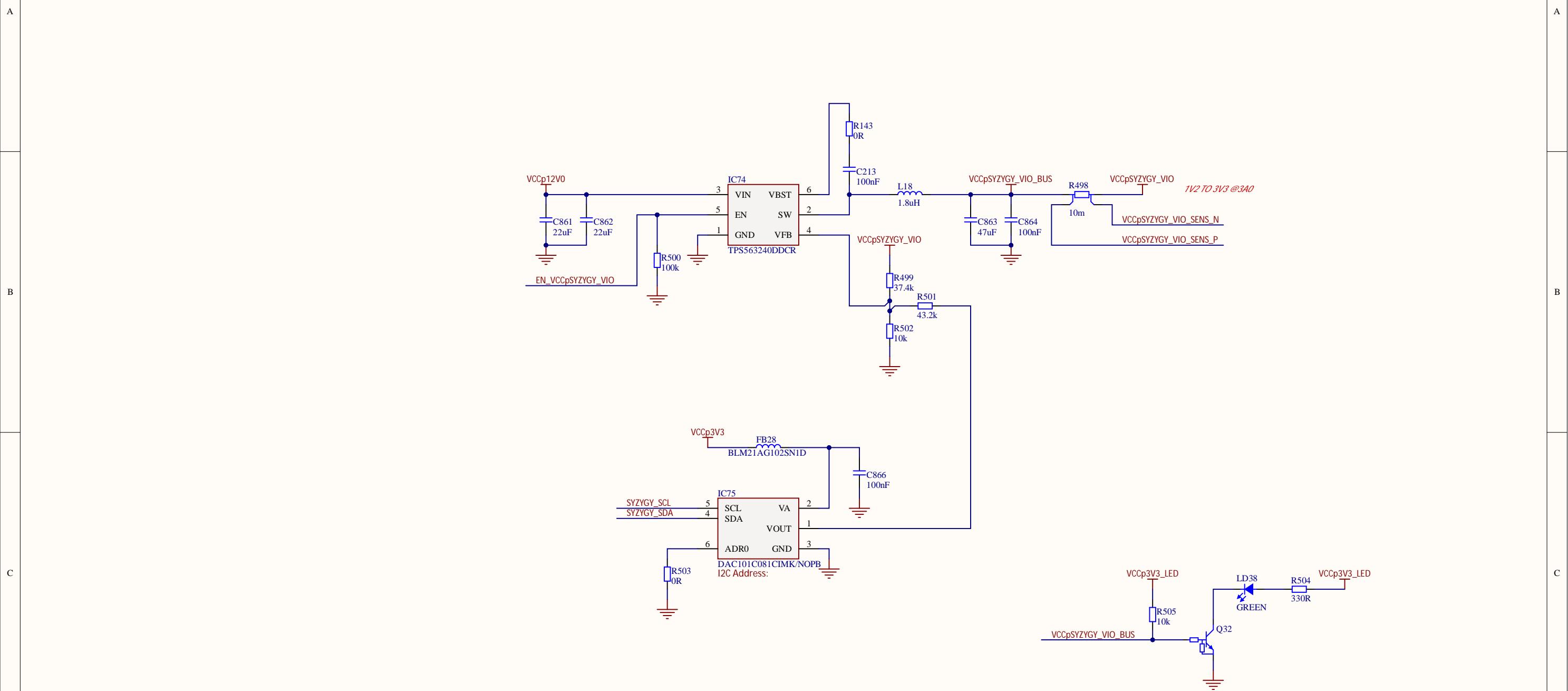
Variant:
Prototype

Page Contents: [41] - PWR V DDR4.SchDoc

Size: A3 DWG NO: KT-000-001-001-001 Revision: V2II

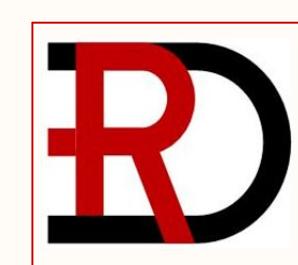
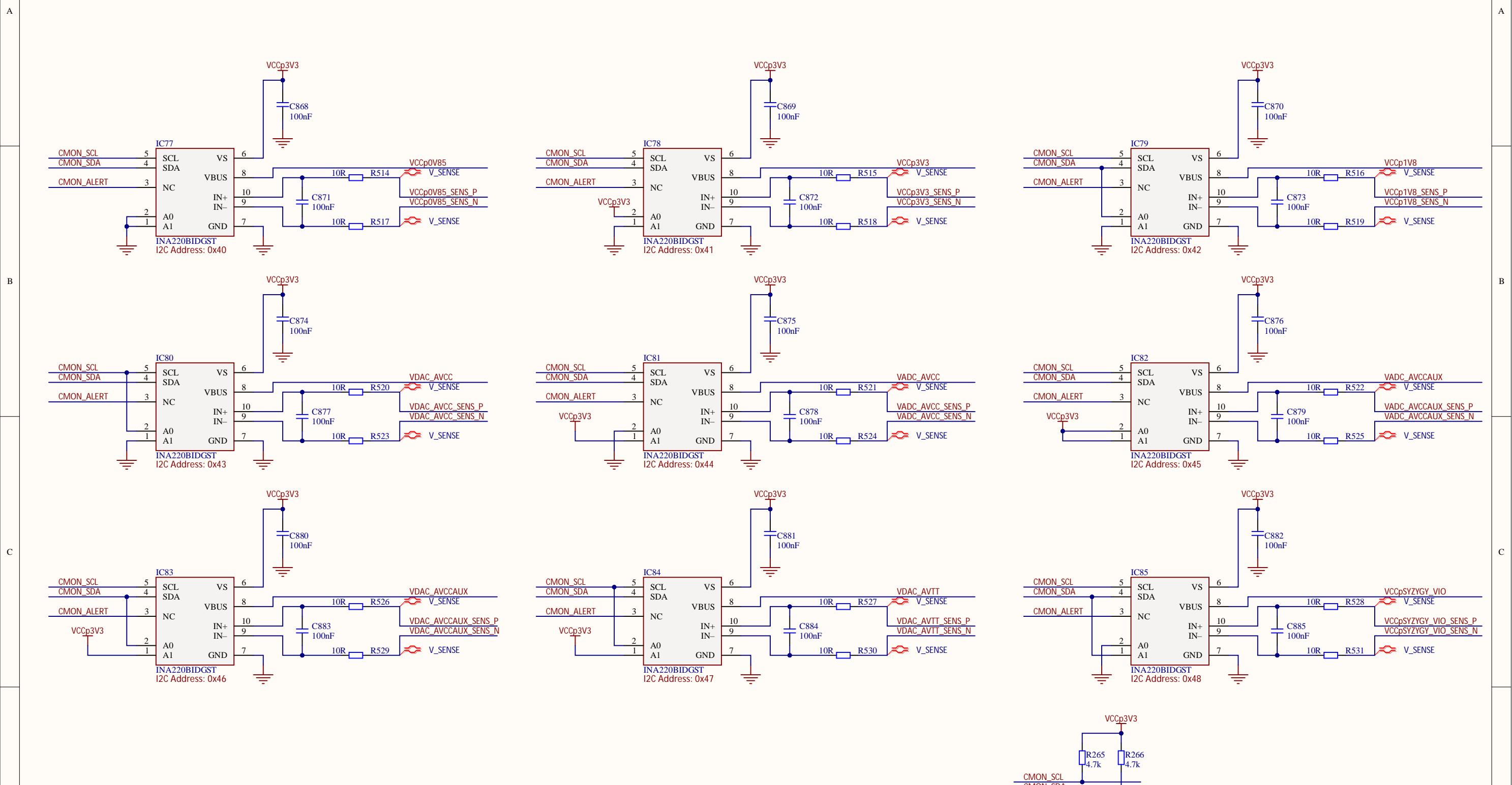
Date: 12/17/2021 Checked by: * Sheet 41 of 46

POWER VI: SYZYGY



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<i>Title:</i>	RFSoC 4X2 Gen3	<i>Variant:</i> Prototype
<i>Page Contents:</i>	[42]- PWR VII SYZYGY.SchDoc	
<i>Size:</i>	A3	<i>DWG NO:</i> KT-000-001-001-001 V2I1
<i>Date:</i>	12/17/2021	<i>Checked by:</i> * <i>Sheet:</i> 42 of 46

CURRENT MONITOR



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Title: RFSoc 4X2 Gen3

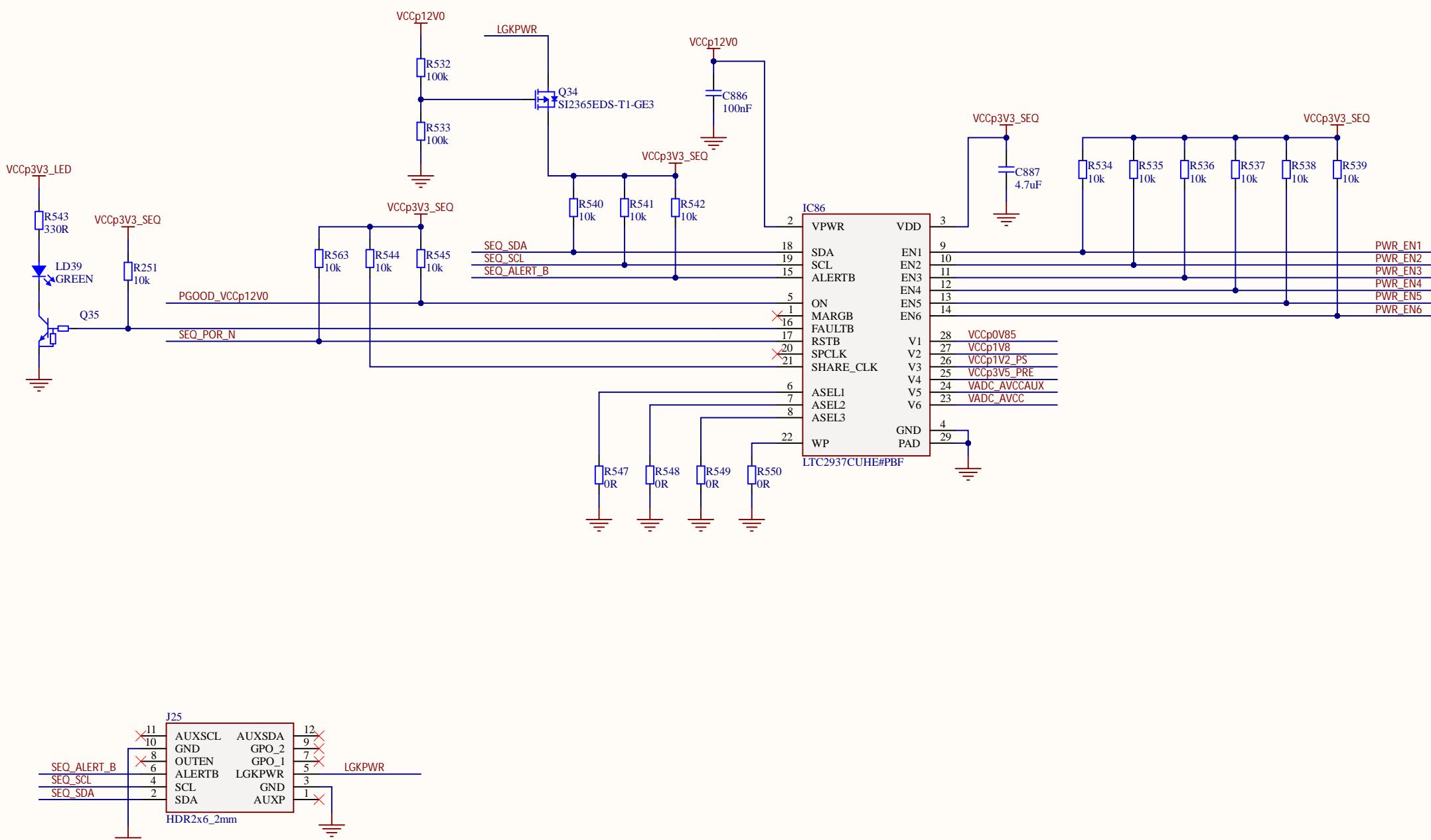
Variant:
Prototype

Page Contents: [43]-CURRENT MONITOR.SchDoc

Size: A3 DWG NO: KT-000-001-001-001 Revision: V2II

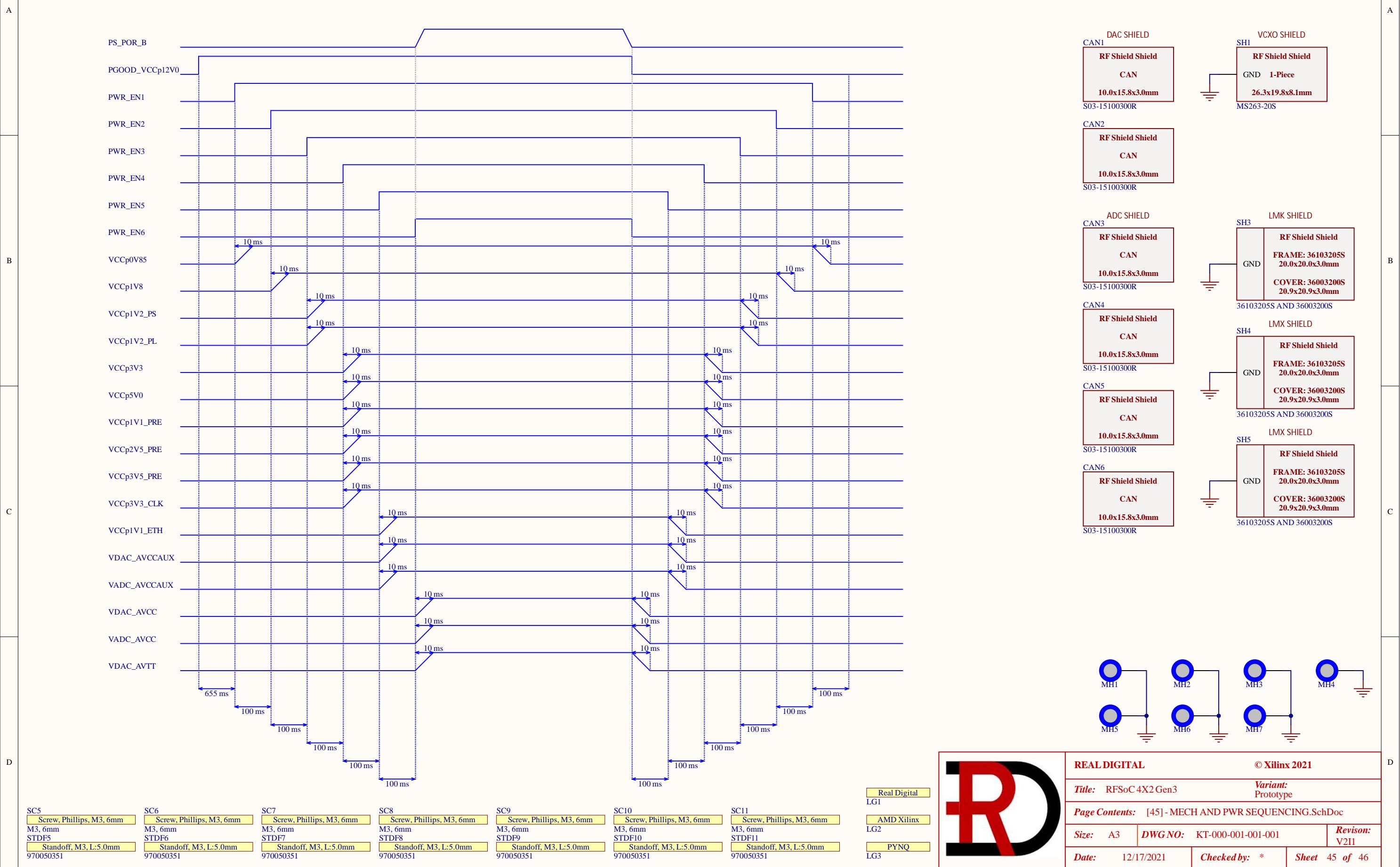
Date: 12/17/2021 Checked by: * Sheet 43 of 46

SEQUENCER



REAL DIGITAL		© Xilinx 2021
Title:	RFSoC 4X2 Gen3	Variant: Prototype
Page Contents: [44]-SEQUENCER.SchDoc		
Size:	A3	DWG NO: KT-000-001-001-001 Revision: V2I1
Date:	12/17/2021	Checked by: * Sheet: 44 of 46

MECHANICAL AND POWER SEQUENCING



DOC: REVISION HISTORY

Schematic:

1. Update Title Block: "CONFIDENTIAL Do not distribute" and "CR 2021 REAL DIGITAL" from all schematic pages
2. Update Cover Page (Sheet 1)
3. Update Block Diagram (Sheet 2)
4. Update Power Diagram (Sheet 3)
5. Remove design notes (Sheet 4, Sheet 18, and Sheet 28)
6. Update POWER SEQUENCING diagram (Sheet 45)

Schematic and PCB

1. Swap MIO33_UA1_RXD and MIO32_UA1_TXD (Sheet 20)
2. Change Sheet 12 name from "SD CARD" to "SD CARD AND EEPROM". Add the EEPROM memory AT24MAC402-MAHM-T connected to the Syzygy I2C bus.
3. Change the status for the resistors connected to SPI_CLK/SMCLK (38) and SPI_DO/SMDAT (39) to "No Load" (Sheet 9, USB5742/2G).
4. Change the status for the capacitors connected to VCM01_224 (AL5), VCM23_224 (AL4), VCM01_226 (AJ5), and VCM23_226 (AJ4) to "NoLoad" (Sheet 27).
5. Rename the net between the power supply sequencer IC86.17 and the OLED display DISP1.8 to be SEQ_POR_N and add a pull-up resistor (10k) to Vccp3v3_SEQ on SEQ_POR_N (Sheet 44).
6. Connect SEQ_POR_N to NVT2008BQ level shifter pin B6 and connect PS_POR_N to NVT2008BQ level shifter pin A6 (Sheet 14).
7. Change the status for the pull-up resistor connected to PS_POR_N to "Load" (Sheet 19).
8. Change DDR4 memory part number from "MT40A512M16JY-083E" to "MT40A512M16LY-062E".

10. Add the AC decoupling capacitors for the RF clocks.
11. Remove the 3dB attenuator for the external input reference clock.

12. Increase the output capacitance for the LDOs (Sheet 40).

13. Silkscreen changes:

- Remove the QR Code;
- Change the Xilinx logo to be AMD_Xilinx;
- Add PYNQ logo;
- Change "USD DEVICE" to "USB DEVICE";
- Add labels for the programming headers: JTAG, SI5395 PROG, SEQ PROG, CLK PROG
- Change DAC0, DAC1, ADC0, ADC1, etc. to DAC_A, DAC_B, ADC_A, ADC_B, etc.

14. Add 200k pull-up resistors connected for the NVT2008BQ "EN" pin, update "VREFB" connection, and add pull-ups on the B side of the level translators. (Sheet 05 - 3 ICs, Sheet 10 - 1 IC, Sheet 14 - 1 IC)

15. Increase the input capacitance for the ADM7172ACPZ-R7 LDOs (Sheet 40).

16. Update the USB3.0 Slave connector schematic symbol and footprint (Sheet 8).

17. Increased the value of the resistors to reduce the brightness of the white and RGB user LEDs

- Change R2, R3, R4, and R5 resistors values from 330R to 1k
- Change R16, R20, R24, and R26 resistors values from 86R6 to 270R
- Change R16, R20, R24, and R26 resistors values from 150R to 470R



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Size:	A3	DWG NO: KT-000-001-001-001 V2II
Date:	12/17/2021	Checked by: * Sheet: 46 of 46