FRAMOS KRIA Documentation

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# Kria KR260

For Xilinx

# Accelerated Applications

For Xilinx

# (SLVS-EC Machine Vision application)

For Xilinx

# Overview

For Xilinx

## Introduction of Accelerated Application

For Xilinx

## Application Features

For Xilinx

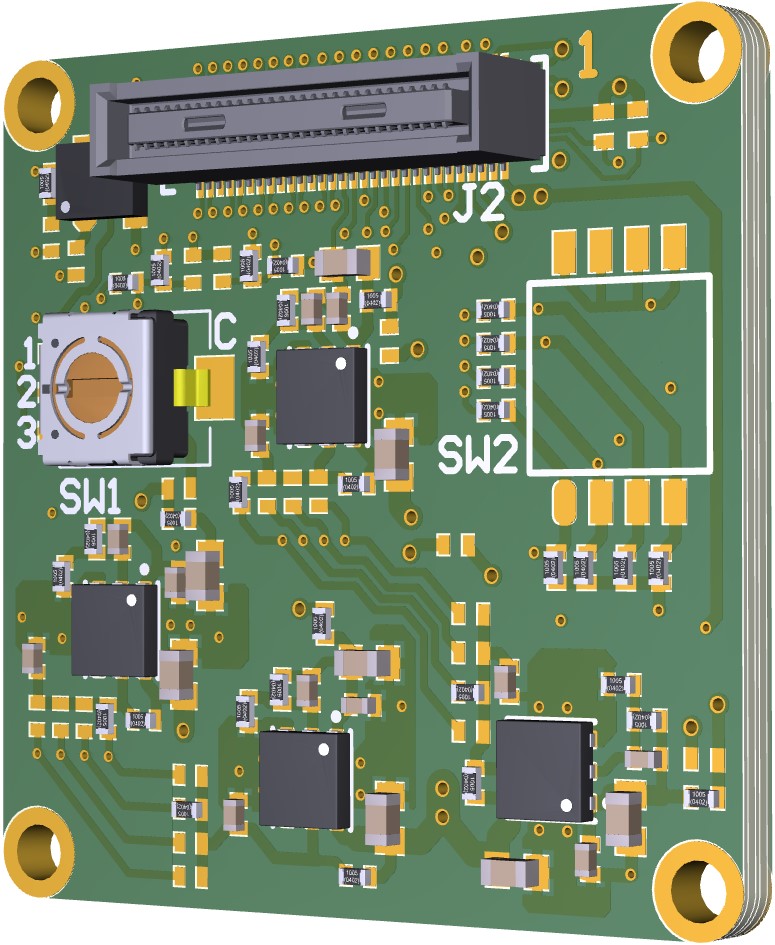
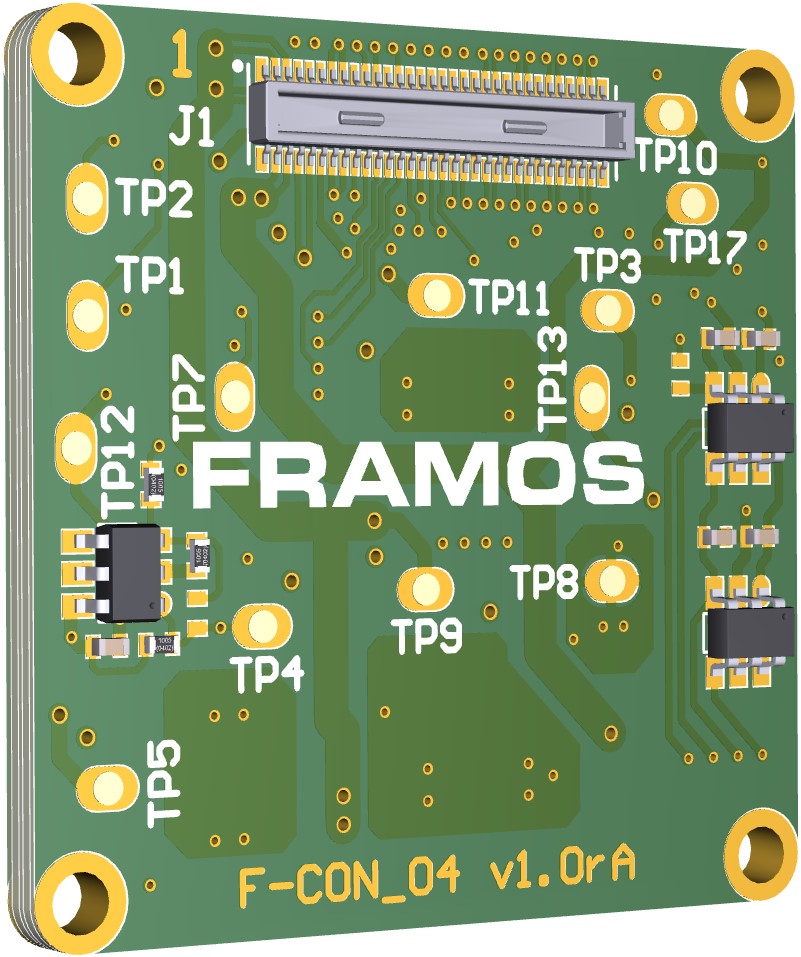
## Overview of Sony IMX547 Sensor

## IMX547 Sensor

The Sony IMX547 is a diagonal 8.8 mm (Type 1/1.8) CMOS active pixel, solid-state image sensor with a square pixel array and 5.10 M effective pixels. This image sensor contains a global shutter with variable charge-integration time and is part of the Pregius S active pixel-type CMOS image sensors. By stacking the signal processing on the back illuminated type CMOS Image Sensor it realizes small chip size and high sensitivity, whilst using the high picture quality global shutter pixel technology of Pregius.

## Overview of FSA Module

The FSA (Framos Sensor Adapter) Connects to the FSM (Framos Sensor Module) allowing with Sub-LVDS, SLVS or SLVS-EC devices.



**PixelMate™ to Xilinx Kria**

**Rear View**

**Top View**

**Connector to FSM (J2)**

**Sensor Clock Source Selection**

Functional Blocks:

* Signal routing
* Voltage generation for image sensor
* Power up sequence for image sensor

A picture containing text, electronics, circuit

Description automatically generated  A picture containing text, electronics, circuit

Description automatically generated

### SW1: Sensor Clock Source Selection

|  |  |
| --- | --- |
| **Pos.** | **Description** |
| **1** | **Clock Provided from FSA (Default)** |
| **2** | **External Clock 1 (MCLK0)** |
| **3** | **External Clock 2 (MCLK1)** |

Table 3: Selection of Sensor Clock Source on FSA-FTx/A-V1

**PixelMate™ - Sub-LVDS, SLVS and SLVS-EC Pinout**

This pinout scheme applies to all sensors that natively output image data using signals according to Sub-LVDS, SLVS or SLVS-EC specification. This layout provides eight data lanes on the connector. Devices with SLVS and SLVS-EC share the same sensor package pins therefore share the same connector pins.

Note: Lane number assignment is applied according to SLVS numbering, which differs in most cases from the SLVS-EC lane numbering. Please refer to image sensor datasheet for correct SLVS-EC numbering.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Pin#** | | **Signal** | **Pin#** | **Signal** |
| **1** | | 3V8 | 2 | 1V8 |
| **3** | | 3V8 | 4 | 1V8 |
| **5** | | V\_ANA | 6 | V\_DIG |
| **7** | | V\_ANA | 8 | V\_DIG |
| **9** | | V\_IF | 10 | V\_AUX |
| **11** | | GND | 12 | GND |
| **13** | | GND | 14 | GND |
| **15** | | SDA | 16 | SCL |
| **17** | | SDO | 18 | XCE |
| **19** | | TOUT0 | 20 | SLAMODE |
| **21** | | TOUT1 | 22 | XMASTER |
| **23** | | TOUT2 | 24 | NC |
| **25** | | NC | 26 | XTRIG |
| **27** | | NC | 28 | XHS |
| **29** | | NC | 30 | XVS |
| **31** | | GND | 32 | GND |
| **33** | | RST | 34 | D\_DATA\_7\_P |
| **35** | | MCLK | 36 | D\_DATA\_7\_N |
| **37** | | GND | 38 | GND |
| **39** | | D\_DATA\_6\_P | 40 | D\_DATA\_5\_P |
| **41** | | D\_DATA\_6\_N | 42 | D\_DATA\_5\_N |
| **43** | | GND | 44 | GND |
| **45** | | D\_DATA\_4\_P | 46 | D\_DATA\_3\_P |
| **47** | | D\_DATA\_4\_N | 48 | D\_DATA\_3\_N |
| **49** | | GND | 50 | GND |
| **51** | | D\_DATA\_2\_P | 52 | D\_DATA\_1\_P |
| **53** | | D\_DATA\_2\_N | 54 | D\_DATA\_1\_N |
| **55** | | GND | 56 | GND |
| **57** | | D\_DATA\_0\_P | 58 | D\_CLK\_0\_P |
| **59** | | D\_DATA\_0\_N | 60 | D\_CLK\_0\_N |
|  | | Common Voltages (from FPA to FSA) | | | | |
|  | | Sensor Specific Voltages (from FSA to FSM) | | | | |
|  | | Sensor Signals | | | | |
|  | | Driving Clock | | | | |
|  | | Data Lines | | | | |

*The table above shows the position of each signal on the 60-pin connector in case the image sensor provides it. For further details, please refer to the image sensor Datasheet.*

Note: The table shows the general signal assignment that applies to all connections using PixelMate**™**.

## Overview of FSM Module

FSM-IMX547

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A close-up of a circuit board  Description automatically generated with medium confidence | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Specification** | | | | | | **Model Name** | **FSM-IMX547 c/m** | | | | | **Image Sensor** | | | | | | Vendor / Name | Sony  IMX547-AAMJ / IMX547-AAQJ | | | | | Shutter Type | CMOS Global Shutter | | | | | Technology / Grade | Pregius S (Gen4) / Industrial | | | | | Chromaticity | Color / Mono | | | | | Optical Format | 1/1.8“ | | | | | Pixel Size | 2.74 x 2.74 µm | | | | | Max. Resolution | 5.1 Mpx / 2448 x 2048 px | | | | | Framerate (max.) | 122 FPS (2-Lane)  65 FPS (1-Lane) | | | | | Bit Depth(s) | 8 / 10 / 12 bit | | | | | **Interface** | | | | | | Data Interface | | | SLVS-EC (1  / 2 Lane) | | | Communication Interface | | | I²C (4-wire serial) | | | Drive Frequency(s) | | | 37.125 / 54 / 74.25 MHz | | | Input Voltages | | | 1.1V, 1.8V, 2.9V, 3.3V | | | Interface Connector | | | Hirose DF40C-60DP-0.4V(51) | | | EEPROM (Sensor ID) | | | Yes | | | **Mechanical** | | | | | | Dimensions (HxWxD) | | | | 28 x 28 | | **Environmental** | | | | | | Operating Temperature | | -30°C to +75°C (function)  -10°C to +60°C (performance) | | | | Storage Temperature | | -40°C to +85°C | | | | Ambient Humidity | | 20% to 95% RH, non condensing | | | |
| Key Benefits & Features:   * 5.1 Mpx Sony CMOS Global Shutter sensor module, ready to embed.   All FSMs are part of a rapid prototyping ecosystem, consisting of:   * Adapters to various processing boards * Design sources for deep embedding * Various accessories and design in services |

## Overview of Framos SLVS-EC IP Core

The SLVS-EC interface standard has emerged as the high-speed interface for image sensors from Sony. It increases throughput to up to 5 Gbit/s per lane at great signal integrity. Engineers developing solutions using Xilinx FPGAs and SoCs can take advantage of FRAMOS’s SLVS-EC RX IP Core, Development Kit, and tested source code examples. Device builders and camera vendors can de-risk the design while reaping the benefits of Sony’s latest high-speed interface.

**Key Benefits & Features**

* Byte-to-pixel conversion for SLVS-EC v1.2 / v2.0
* De-risk integration, reduce time to market
* Reference implementation for evaluation and guidance
* Flexible Lane Support in one IP Core Support for all supported RAW bit-depths
* Error correction and ROI overlap support
* AXI4 communication and control

**Package**

IP Core

* Encrypted RTL (VHDL)
* Source VHDL available
* Simulation Environment (ModelSim)

**Documentation**

* User Manual
* Reference Design Example

Diagram

Description automatically generated

Internal Structure of the SLVS-EC RX IP Core

The SLVS-EC RX IP Core processes the incoming deserialized SLVS-EC packets and outputs the reconstructed pixels on the Output Data Interface. In addition, depending on the core variant, IP Core performs error detection (CRC core variant) or error correction (ECC core variant) on payload data.

### Port Descriptions

The SLVS-EC RX IP Core ports are listed in Table 3, where LANE\_NUM represents the number of lanes.

| Signal | Direction | Width | Description |
| --- | --- | --- | --- |
| data\_clk\_i | Input | 1 | Data clock input |
| rstn\_i | Input | 1 | Active low reset |
| AXI4-Lite | InOut | - | AXI4-Lite slave interface |
| data\_i | Input | 16\*LANE\_NUM | Input parallel data from transceiver |
| rxdatak\_i | Input | 2\*LANE\_NUM | Special character detection input |
| XCVR\_status\_i | Input | 1 | Transceiver status |
| fv\_o | Output | 1 | Frame valid output |
| lv\_o | Output | 1 | Line valid output |
| dv\_o | Output | 1 | Data valid output |
| data\_o | Output | 2\*16\*LANE\_NUM | Parallel pixel data output |
| lnum\_o | Output | 13 | Line number output |
| ebdl\_o | Output | 1 | Embedded valid output |
| did\_o | Output | 4 | Data ID output |
| hit\_o | Output | 3 | Header info type output |
| hinf\_o | Output | 24 | Header information output |
| status\_o | Output | 8 | Core status output |

## Overview of Euresys 10GE Pipeline IP’s

For Euresys

## Performance and Resource Utilization

For ?

# Quick Start

## Test Environment for 10GE

## Application Installation and Execution

## Installation & Sphinx application Usage

## GE application Execution Steps

# Application Architecture

# Software

## 10GE pipeline SW Architecture

# Hardware

## Capture Pipeline HW Architecture

## 10GE Pipeline HW Architecture

# Tutorials

## How to integrate Framos and Euresys Ips

IP Core and reference design guide available from Framos on request.

## How to tune SLVS-EC camera sensor

To be updated by Framos when ready.

# Others

## Debugging steps

## Known issues

# Licensing

## Details on how to get Framos and Euresys IPs license

For more information about how the Framos SLVS-EC RX IP-Core would benefit your next project or want to request the full SLVS-EC IP-Core integration support, please contact the Framos imaging experts at: support@framos.com