基于 Zynq 的 NoC 快速仿真验证平台

An Ultra-fast NoC Simulator based on Zynq

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1. Design Introduction

1.1 Research background

Network-on-Chip (NoC) has become one of the most common interconnection architecture to integrate multi-core system. However, the performance, hardware costs and power consumption of NoC are sensitive to many parameters such as topology, the number and depth of virtual channels (VC), routing algorithms and flow control mechanisms. In order to find the best NoC solution for different applications, a fast and flexible NoC simulator is necessary. In this program, we proposed an ultra-fast NoC simulator based on Zynq, in which the design and simulation parameters, such as the number and depth of VC, the size of packets, topology, inject rate, routing algorithm, etc, are able to be configured by host on PC. We proposed a configurable prototype of standard 5-stage NoC router to replace the model of NoC router to improve the accuracy and simulation speed.

1.2 Application filed

Design and Optimization of NoC

1.3 Scope

This NoC Simulator is suitable for mesh-based NoC. Because the design parameters, which include the number and depth of VC, the size of packets, topology, inject rate, routing algorithm, are configurable. The simulator can be used to evaluate the performance of NoC router, the effectiveness of routing algorithms and NoC mapping results.

2. System construction & Function Description

2.1 Introduction of System

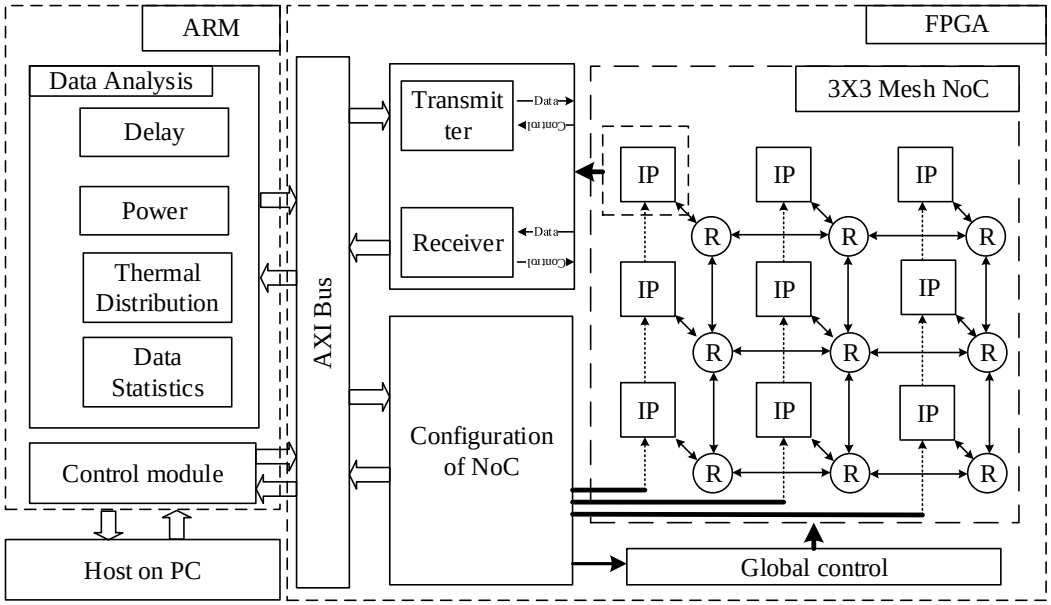


Fig. 1 overall architecture of Ultra-fast NoC Simulator based on Zynq

This simulation platform can be divided into three main components: (1) FPGA side, (2) ARM side, (3) Host on PC. The configuration information. The FPGA side consists of Router microarchitecture, Virtual IP which includes data transmitter and receiver, interconnections between Router microarchitecture and AXI bus between virtual IP and ARM. The ARM side is in charge of gathering statistical data from virtual IP and doing data analysis, which includes delay, power consumption, thermal distribution, etc. It also allocates and sends the configuration information to the routers and virtual IPs on FPGA side. The host on PC is used to control configuration information and show the simulation results.

2.2 Introduction of modules

2.2.1 Router

The NoC router we designed is a standard 5-stage router and configurable switch. For the standard router, we employ On/Off-based wormhole virtual-channel flow control to realize the flow control mechanism. A typical 5-stage router consists of buffer write (BW), route computation (RC), virtual allocation (VA), switch allocation (SA), and switch traversal (ST). The overall architecture is illustrated in Fig.2. In order to simulate different parameters of routers, NoC router has some configurable design parameters. As it can be seen, the router mainly consists of input unit, VC allocator, Table-based routing, Round-robin arbiter and crossbar switch. We employ configurable

Table-based routing to realize suitable routing algorithms for different topology. To reduce the amount of interconnections between routers, On/off flow control is applied to control upstream router to send (on) or not send (off) data. The control bit is on when the number of free buffers in FIFOs rises above the threshold. Furthermore, the number of VCs per port can be configured by up to 8 and the depth of VCs can be configured by up to 16.

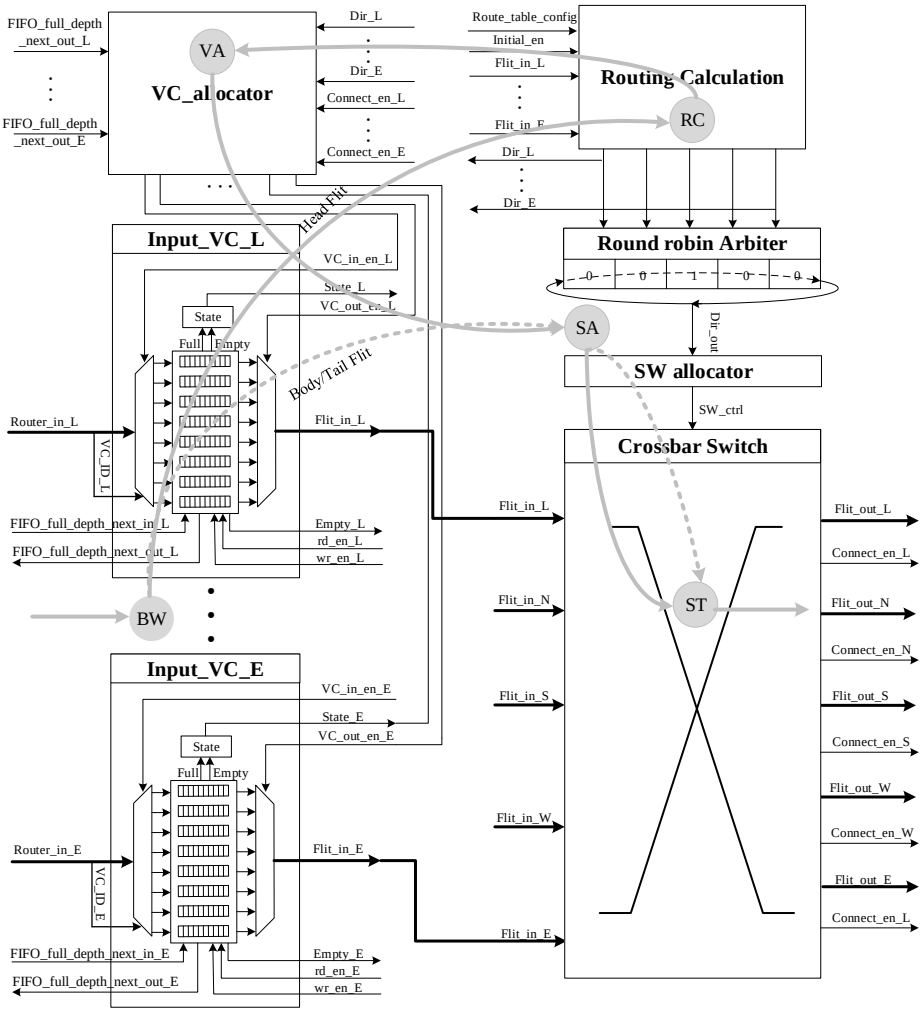


Fig. 2 Architecture of NoC router

2.2.2 Virtual IP

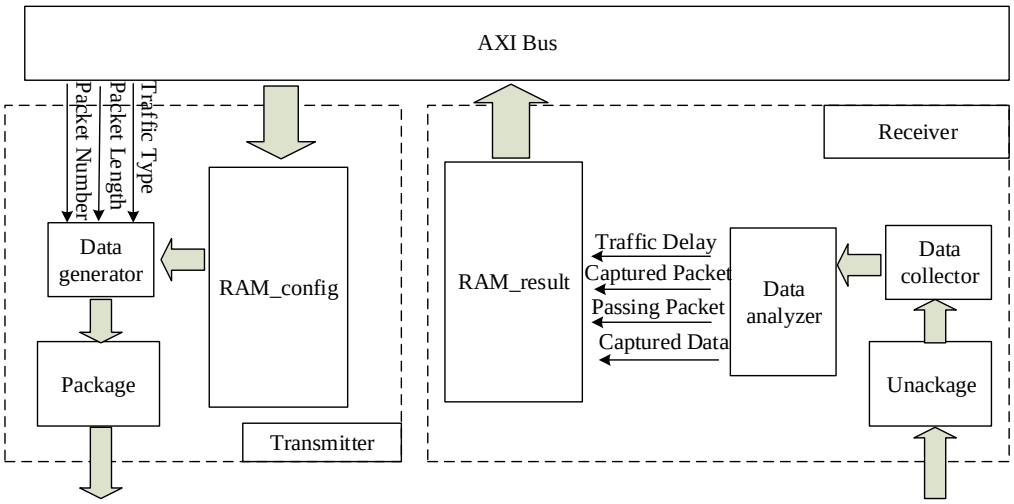


Fig. 3 Diagram of Virtual IP

The virtual IP consists of a data transmitter and a data receiver. The data transmitter consists of data generator, module of data package and a RAM which is used to store configuration information. The function of data transmitter is to generate different type of packets. The data receiver consists of data collector, module of data unpackage, data analyzer and a RAM which is used to store collected information. The function of data receiver is to analyze packets received by routers and collect information which includes communication volume through routers, average packet latency, packets received by routers, etc.

2.2.3. Module of NoC configuration

The function of module of NoC configuration is to configure the length of packets(1-128 flits), the number of packets(1-1024), injection rate(0.1-1flit/noed/clk), and traffic pattern(random, neighbor, bitcomp), ect.

2.2.4. Data analysis

Data analysis which is based on power model, delay model and thermal model, is implemented on the ARM of Zynq. The program on ARM can calculate the power consumption of communication, the average communication delay, and thermal distribution of NoC based on the information collected by virtual IP.

2.2.5. Host on PC

The function of the host on PC is mainly to send the configuration information to Zynq through Uart and show the simulation results graphically.

3. Final Design & Performance Parameters

3.1 Function and performance

To demonstrate NoC simulator's correctness and performance, various scenarios should be considered. We used Xilinx Zynq FPGA to implement a 3X3 mesh NoC to evaluate all configurable parameters. Due to the limitation of FPGA resource, the number of router is reduced to 5. The resource utilization o is shown in Table 1. Fig. 5 and Fig. 6 show the photos of proposed NoC Simulator based on Zynq and simulation results.

(1) NoC emulation on FPGA, which is implemented in Verilog HDL by using Xilinx Vivado,

(2) Program on ARM, which is developed in C by using Xilinx SDK

(3) Host on PC, which is developed in C++ by using Qt which is a cross-platform C++ application development framework, widely used in GUI application development.

Additionally, all modules in FPGA are implemented in AXI-based structure. The final implementation runs at 100 MHz.

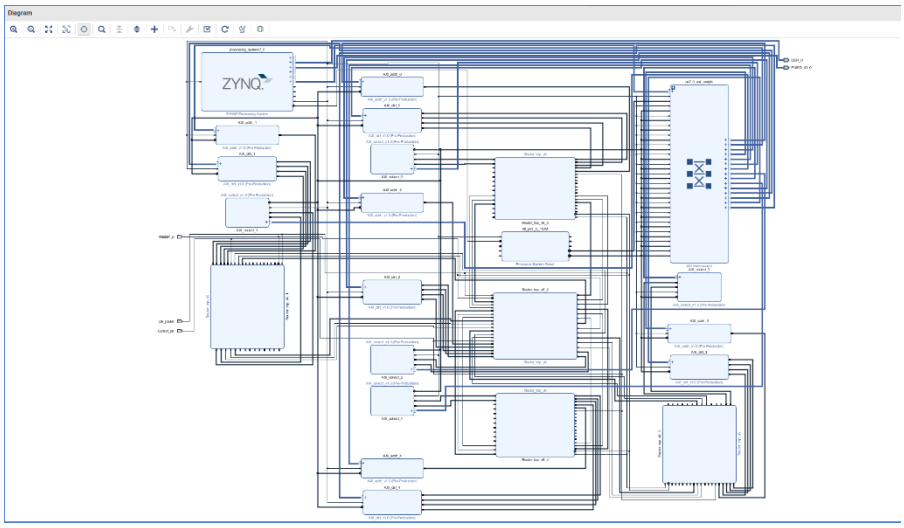


Fig. 4 Diagram of Ultra-fast NoC Simulator based on Zynq

3.2 Power and utilization

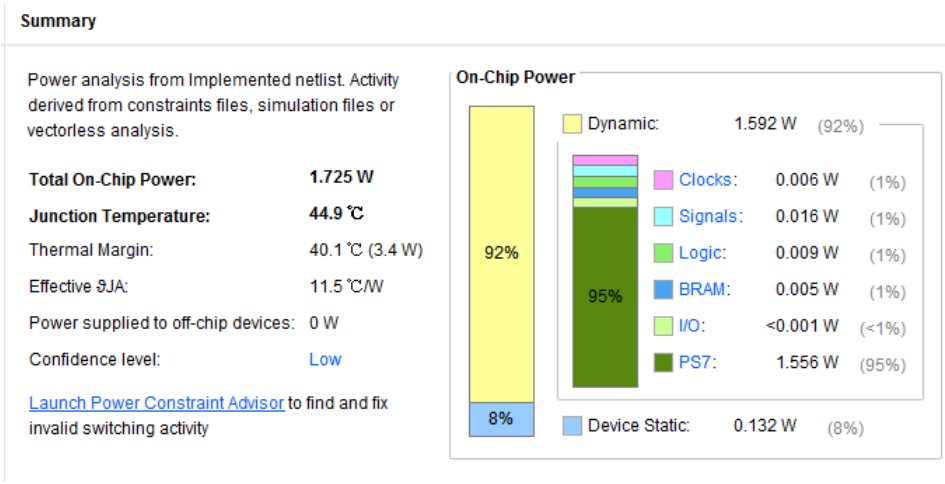
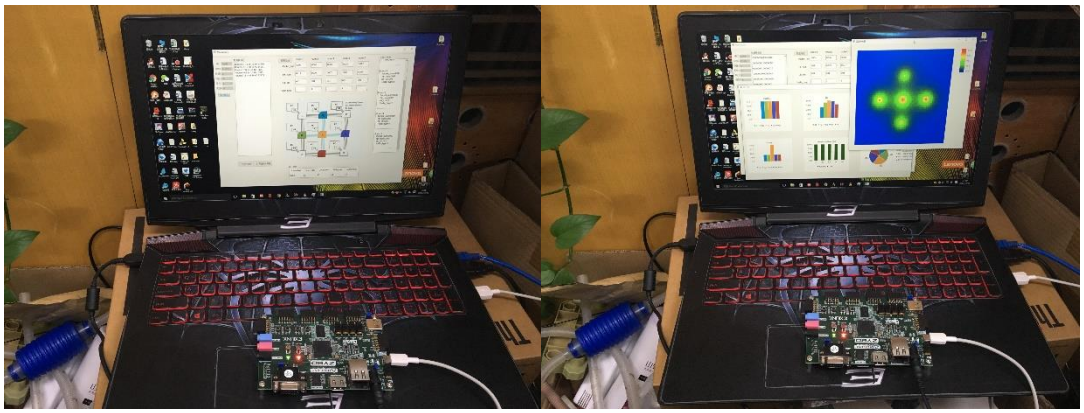


Fig. 5 power analysis of Zynq

Table 1 Utilization of FPGA resource

Resource	Utilization	Available	Utilization%
LUT	14168	17600	80.50
LUTRAM	1907	6000	31.78
FF	14593	35200	41.46
BRAM	48	60	80
IO	3	100	3
BUFG	7	32	21.88



(a) (b)

Fig. 5 Photos of NoC Simulator based on Zynq (a) Configuration interface (b) simulation results

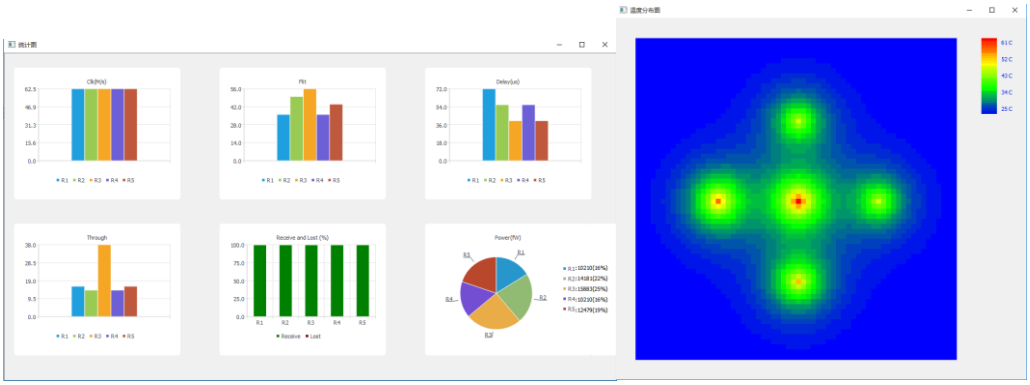


Fig. 6 Simulation results of NoC simulation (a) Simulation results (b)Thermal distribution

4. Conclusion

4.1 Innovation

(1)Apply the combination FPGA and ARM to implement the NoC simulation.

(2) Use configurable prototype of standard 5-stage NoC routers to replace the model of NoC router to improve the accuracy and simulation speed.

(3)Support different topology and routing algorithms by modifying routing table.

(4) Achieve more than 100x speed-up compared to software-based NoC simulators.