IBERO
PUEBLA ®
IDIT

Programable elements I
Interrupts

Interrupt Definition

- **Interrupt request,** signal sent to the processor that temporarily stops a running program and allows a special program, an interrupt handler, to run instead.

```
ISR(TIMER1_OVF_vect)//Interrupt Service Routine
{
        Do Sthg
}
```

Sources

- Timers
- ADC
- Port Pins : INT0, INT1 and INT2
- Analog Comparator
- EEPROM
- UART
- SPI
- TWI or I2C

Vector No.	Program Address[2]	Source	Interrupt Definition
1	$000[1]	RESET	External Pin, Power-on Reset, Brown-out Reset, Watchdog Reset, and JTAG AVR Reset
2	$002	INT0	External Interrupt Request 0
3	$004	INT1	External Interrupt Request 1
4	$006	INT2	External Interrupt Request 2
5	$008	TIMER2 COMP	Timer/Counter2 Compare Match
6	$00A	TIMER2 OVF	Timer/Counter2 Overflow
7	$00C	TIMER1 CAPT	Timer/Counter1 Capture Event
8	$00E	TIMER1 COMPA	Timer/Counter1 Compare Match A
9	$010	TIMER1 COMPB	Timer/Counter1 Compare Match B
10	$012	TIMER1 OVF	Timer/Counter1 Overflow
11	$014	TIMER0 COMP	Timer/Counter0 Compare Match
12	$016	TIMER0 OVF	Timer/Counter0 Overflow
13	$018	SPI, STC	Serial Transfer Complete
14	$01A	USART, RXC	USART, Rx Complete
15	$01C	USART, UDRE	USART Data Register Empty
16	$01E	USART, TXC	USART, Tx Complete
17	$020	ADC	ADC Conversion Complete
18	$022	EE_RDY	EEPROM Ready
19	$024	ANA_COMP	Analog Comparator
20	$026	TWI	Two-wire Serial Interface
21	$028	SPM_RDY	Store Program Memory Ready

Priority

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11	$014	TIMER0 COMP	Timer/Counter0 Compare Match
12	$016	TIMER0 OVF	Timer/Counter0 Overflow
13	$018	SPI, STC	Serial Transfer Complete
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HIGHEST

LOWEST

Interrupt Vectors

Vector Number	Interrupt definition	Vector name
2	External Interrupt Request 0	INT0_vect
3	External Interrupt Request 1	INT1_vect
4	Pin Change Interrupt Request 0	PCINT0_vect
5	Pin Change Interrupt Request 1	PCINT1_vect
6	Pin Change Interrupt Request 2	PCINT2_vect
7	Watchdog Time-out Interrupt	WDT_vect
8	Timer/Counter2 Compare Match A	TIMER2_COMPA_vect
9	Timer/Counter2 Compare Match B	TIMER2_COMPB_vect
10	Timer/Counter2 Overflow	TIMER2_OVF_vect
11	Timer/Counter1 Capture Event	TIMER1_CAPT_vect
12	Timer/Counter1 Compare Match A	TIMER1_COMPA_vect
13	Timer/Counter1 Compare Match B	TIMER1_COMPB_vect
14	Timer/Counter1 Overflow	TIMER1_OVF_vect
15	Timer/Counter0 Compare Match A	TIMER0_COMPA_vect
16	Timer/Counter0 Compare Match B	TIMER0_COMPB_vect
17	Timer/Counter0 Overflow	TIMER0_OVF_vect
18	SPI Serial Transfer Complete	SPI_STC_vect
19	USART Rx Complete	USART_RX_vect
20	USART Data Register Empty	USART_UDRE_vect
21	USART Tx Complete	USART_TX_vect
22	ADC Conversion Complete	ADC_vect
23	EEPROM Ready	EE_READY_vect
24	Analog Comparator	ANALOG_COMP_vect
25	Two-wire Serial Interface	TWI_vect
26	Store Program Memory Read	SPM_READY_vect

Vector Number	Interrupt definition	Vector name
1	External Interrupt Request 0	INT0_vect
2	Pin Change Interrupt Request 0	PCINT0_vect
3	Timer/Counter1 Compare Match A	TIMER1_COMPA_vect
4	Timer/Counter1 Overflow	TIMER1_OVF_vect
5	Timer/Counter0 Overflow	TIMER0_OVF_vect
6	EEPROM Ready	EE_RDY_vect
7	Analog Comparator	ANA_COMP_vect
8	ADC Conversion Complete	ADC_vect
9	Timer/Counter1 Compare Match B	TIMER1_COMPB_vect
10	Timer/Counter0 Compare Match A	TIMER0_COMPA_vect
11	Timer/Counter0 Compare Match B	TIMER0_COMPB_vect
12	Watchdog Time-out	WDT_vect
13	USI Start Condition	USI_START_vect
14	USI Overflow	USI_OVF_vect

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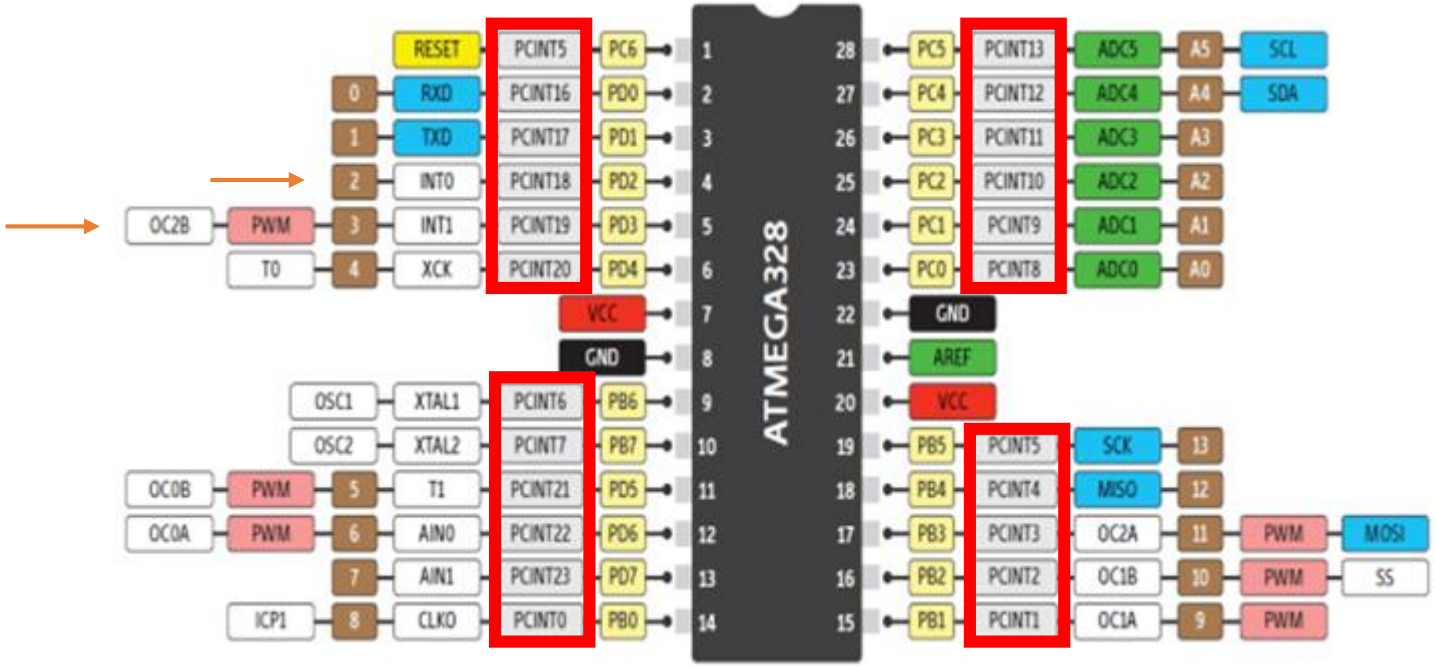
External Interrupts

True Int vs Pin Change Interrupts



PCINTx, Shares ISR
INTx, individual ISR

VectorNo.	Program Address(2)	Source
1	0x0000(1)	RESET
2	0x0002	INT0
3	0x0004	INT1
4	0x0006	PCINT0
5	0x0008	PCINT1
6	0x000A	PCINT2

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Steps to configure the Interrupts:

External Interrupts

1.Set INT1 and INT0 bits in the respective Control Register

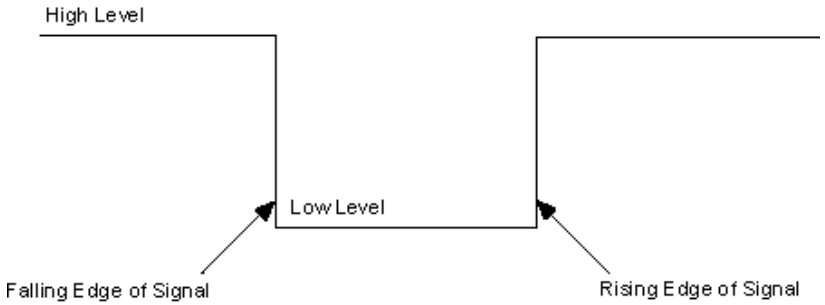
Example for ATMEGA328p

EICRA – External Interrupt Control Register A

The external interrupt control register A contains control bits for interrupt sense control.

Bit	7	6	5	4	3	2	1	0	
(0x69)	–	–	–	–	ISC11	ISC10	ISC01	ISC00	EICRA
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Any logical change on INT1 generates an interrupt request.
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.



On ATTINY

MCUCR – MCU Control Register

The External Interrupt Control Register A contains control bits for interrupt sense control.

Bit	7	6	5	4	3	2	1	0	
0x35	**BODS**	**PUD**	**SE**	**SM1**	**SM0**	**BODSE**	**ISC01**	**ISC00**	**MCUCR**
Read/Write	R	R/W	R/W	R/W	R/W	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

0	0	The low level of INT1 generates an interrupt request.
0	1	Any logical change on INT1 generates an interrupt request.
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

External Interrupts

2. Set the Enable bit in it's correct register

EIMSK – External Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0	
0x1D (0x3D)	–	–	–	–	–	–	INT1	INT0	EIMSK
Read/Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 1 – INT1: External Interrupt Request 1 Enable

Bit 0 – INT0: External Interrupt Request 0 Enable

3. Write the program to follow on interrupt

```
ISR(Intx_vect )
{
        Interrupt Program
}
```

On ATTINY

GIMSK – General Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0	
0x3B	–	INT0	PCIE	–	–	–	–	–	GIMSK
Read/Write	R	R/W	R/W	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

Bit 6 – INT0: External Interrupt Request 0 Enable

Bit 5 – PCIE: Pin Change Interrupt Enable

Example

```
#include <avr/io.h>
#include <avr/interrupt.h>
void int_init()
{
                                                                    //BIT 7 6 5 4 3 2 1 0
        EICRA|= (1 << ISC10)|(1 << ISC11)|(1 << ISC01);//    EICRA: 0 0 0 0 1 1 0 1
        //Int0 on fallin and Int1 on rising
        EIMSK|= (1 << INT1)|(1 << INT0);//Enable interrupt 1 and 0
}
ISR(INT0_vect)
{
        PORTB^=0xFF; //PINS on PORTB ON
}
ISR(INT1_vect)
{
        PORTC^=0xFF; //PINS on PORTB OFF
}
int main(void)
{
   int_init();
   DDRB=0xFF;
   DDRC=0xFF;
   DDRC=0x00; //INT pins as INPUTS
   while (1)
   {}
}
```

PIN Change Interrupts

1. Set the Enable the control register

Example for ATMEGA328p

PCICR – Pin Change Interrupt Control Register

Bit	7	6	5	4	3	2	1	0	
(0x68)	–	–	–	–	–	PCIE2	PCIE1	PCIE0	PCICR
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 2 - PCIE2: Pin Change Interrupt Enable 2
PCINT23..16
Bit 1 – PCIE1: Pin Change Interrupt Enable 1
PCINT14..8
Bit 0 – PCIE0: Pin Change Interrupt Enable 0
PCINT7..0

PIN Change Interrupts

2. Set which pins will act as interruptions

PCMSK2 – Pin Change Mask Register 2

Bit	7	6	5	4	3	2	1	0	
(0x6D)	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	PCMSK2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PCMSK1 – Pin Change Mask Register 1

Bit	7	6	5	4	3	2	1	0	
(0x6C)	–	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	PCMSK1
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PCMSK0 – Pin Change Mask Register 0

Bit	7	6	5	4	3	2	1	0	
(0x6B)	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	PCMSK0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

On ATTINY

PCMSK – Pin Change Mask Register

Bit	7	6	5	4	3	2	1	0	
0x15	–	–	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	PCMSK
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Activity

- Create a code for 2 infinite led cycles which alternate on the use of an interruption on a HIGH signal.

- Create a code which has a led blink at 1 sec intervals, using 4 interrupts when a LOW signal is received make it blink twice at the following intervals:
    - 1. 100 ms
    - 2. 500 ms 3.
    - 1.5 secs
    - 4. 2secs

- Create a code to measure time, when an interrupt is activated save the time passed and light a led the same amount of time passed, with a maximum time of 6 seconds.