| APPLICATION | | REVISIONS | | | APPROVALS | |
|---|---|---|---|---|---|---|
| NEXT ASSY | PROJECT NO. | ECN NO. | REV | DESCRIPTION | DATE | APPROVED |
| | | | | INITIAL SPECS. | 2013/03/28 | HENRY CHEN |
| | | | A | 12V OCP range change to 105% to 125% | 2013/06/28 | HENRY CHEN |
| | | | | Define dc input range | 2013/09/03 | HENRY CHEN |
| | | | | Correct FRU 50~75 bytes | 2013/11/04 | HENRY CHEN |
| | | | | Change 230Vac standby mode efficiency | 2013/11/25 | HENRY CHEN |
| | | | B | Define input power accuracy at 270VDC | 2013/11/26 | HENRY CHEN |
| | | | C | Correct FRU 50~75 bytes | 2014/02/12 | HENRY CHEN |
| | | | D | Re-define standby mode efficiency at 6W | 2014/04/30 | HENRY CHEN |
| | | | | Make sure C32 work when PSU fail | 2014/09/23 | HENRY CHEN |



UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES [MILLIMETERS]. TOLERANCES ARE:

| FRACTIONS | DECIMALS | ANGLES |
|---|---|---|
| ± 1/32 | .XX ± .02 [0.5] | ±1° |
| | .XXX ± .010 [0.25] | |

LITEON

**PS, 1U, 750W, 12V, PS-2751-7H-LF**

| SIZE | DRAWING NO. | REV |
|---|---|---|
| **A** | **PS-2751-7H-LF** | D |

SUPPLEMENTS: EF,PDF

SHEET 1 OF 112

## 1. SCOPE

This document defines the functional requirements up to 750W max output POWER SUPPLY AC-TO-DC MODULE POWER SUPPLY ASSEMBLY developed for LiteON Company, intended for worldwide use in electronic data processing equipment. The power supply module shall contain fan(s) for forced air-cooling. The power supply shall operate with over an AC input voltage range of 90VAC to 264VAC. The power supply module shall be able to accept the valid input voltage from the utility as well as from an uninterruptable power supply. The power supply may be used singly or in redundant configurations up to 6 power supplies. All specifications are applicable under all operating conditions when installed in the End Use system unless otherwise stated.

## 2. REFERENCE DOCUMENTS

### 2.1 APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein. Unless otherwise indicated, the content of this document applies. Undated references refer to the latest revision of the document that is in effect at the time the product is intended to be released.

**TABLE 1 – REFERENCE DOCUMENTS**

| REFERENCE | DESCRIPTION |
|---|---|
| 010-05-C03 | Supplier Management Process Standard Operating Procedure -Corporate |
| 106128 | "Label, Blank, Thermal Print." |
| 106217 | "Specification, SMT Design Guidelines." |
| 106584 | "Procedure, Printing, Label Thermal." |
| 106663 | "Specification, Thru-hole Design Guidelines." |

| REFERENCE | DESCRIPTION |
|---|---|
| 109291 | "Test Specification Packaging of Hewlett Packard (HP) Named Products." |
| 109893 | "Specification, Raw Material, Supplier Packaging/Material Handling." |
| 114971 | "Procedure, IC, Fabrication, Assembly, Packaging and Test Process Change Notification." |
| 130656 | "Procedure, Specification, Packaging Outline, SIMM." |
| 131400 | "Specification, Packaging, Finished Goods Distribution." |
| 137063 | "Specification, Raw Material Supplier, Shipment Bar Codes." |
| 137114 | "Procedure Unitized Load Package Test." |
| 137169 | "Procedure, Country of Origin Encoding." |
| 184968 | "Specification, Test Requirements, Process Materials." |
| 185411 | "Standard Label, Commodity Tracking, OEM Assembly, New." |
| 192192 | "Specification, PCB Fabrication." |
| 441653 | "Label, China, RoHS, ISS" |
| ANSI C63.4 – 2009 | "American National Standard for Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electronic Equipment in the Range of 9 kHz to 40 GHz." American National Standards Institute (ANSI), 2009. |
| Australian Communications & Media Authority | Electromagnetic Compatibility Framework - Information for Suppliers – Residential, Commercial and Light Industry"(and amendments), July 1995, URL: http://www.acma.gov.au |
| C.I.S.P.R. Pub. 22 | "Limits and methods of measurement of radio interference characteristics of information technology equipment." International Special Committee on Radio Interference (C.I.S.P.R.), Fifth Edition, 2005+A1. |
| CCC EMC | "*Regulations for Compulsory Product Certification*," China Certification Center, URL: http://www.cemc.org.cn. |
| CFR 47, Part 15 | "Unintentional Radiators". Title 47 of the Code of Federal Regulations, Part 15, FCC Rules, Radio Frequency Devices, Subpart B. |
| CNS14336 | "Information technology equipment - Safety - General requirements", Bureau of Standard, Metrology and Inspection |
| EN 55022 | "Limits and methods of measurement of radio interference characteristics of information technology equipment." European Committee for Electro technical Standardization (CENELEC), 2006+A1. |
| EN 55024 | "Information technology equipment - Immunity characteristics - Limits and Methods of measurement." European Committee for Electro technical Standardization (CENELEC) 1998 |
| EN 60320-1 | "Appliance Couplers for Household and Similar General Purposes – Part: General Requirements" European Committee for Electro technical Standardization (CENELEC). |
| EN 60950-1:2005 A1: 2010 | "Safety of Information Technology Equipment - Safety - Part 1: General requirements", Second Edition, International Electrotechnical Commission, 2005, including A1:2010 |

| REFERENCE | DESCRIPTION |
|---|---|
| EN 60950-1:2006 A11: 2008 A1: 2009 | "Safety of Information Technology Equipment - Safety - Part 1: General requirements", Second Edition, European Committee for Electrotechnical Standardization (CENELEC), 2006, including A11: 2008 and A1: 2010 |
| EN 61000-3-2:2006 | "Electromagnetic Compatibility (EMC) Part 3-2 Limits - Limits for Harmonics Current Emissions (Equipment input current ≤16A per phase)." International Electrotechnical Commission, 2006. |
| EN61000-3-3/~~A1:2001~~ | "Electromagnetic compatibility (EMC) - Part 3-3 Limits - Limitation of voltage fluctuations and flicker in low-voltage supply systems for equipment with rated current <= 16 A" European Committee for Electrotechnical Standardization (CENELEC), 2008, ~~including Amendment A1, 2001~~ |
| GB4943-2001 | "Safety of Information technology equipment", Standardization Administration of China |
| HP-00011-00 | "General Specification for Environment." |
| IEC 60950-1: 2005 A1: 2010 | "Safety of Information Technology Equipment - Safety - Part 1: General requirements", Second Edition, International Electrotechnical Commission, 2005 including A1:2010 |
| IEC 61000-4 Sections 2 – 6, 11 | "Electromagnetic Compatibility (EMC) – Part 4: Testing and measurement techniques." International Electro technical Commission (IEC). |
| IPC-A-610 | "Specification, Acceptability of Electronic Assemblies." |
| MIL HDBK 217F | "Reliability Prediction of Electronic Equipment." U.S. Military Standard. |
| SMP Reference | "HP Supplier Management Process Reference." HP Document. |
| Taiwan EMC Law | "Commodity EMC Regulation" (Taiwan EMC Law), Bureau of Standards, Metrology, and Inspection under auspices of the Ministry of Economic Affairs, URL:http://www.bsmi.gov.tw . |
| UL 60950-1 CSA C22.2 No. 60950-1-07 | "Safety of Information Technology Equipment including Electrical Business Equipment, First Edition." Underwriters Laboratories, Inc., 2007, Canadian Standards Association, 2007. |
| EN896-00 | ESS Power Supply HALT Procedure and Requirements |
| EN896-01 | ESS HASA Power Supply Requirements with Proof of Screen |

### 2.2 ORDER OF PRECEDENCE

In the event of a conflict between this specification and references cited herein, this specification shall take precedence.

Note: The product (part) and packaging must comply with LiteON, General Specification for the Environment (GSE). These AC Input Modules are to be Lead-Free. Lead in solder for Servers, Storage and Storage Array Systems, Network Infrastructure Equipment for Switching, Signaling, Transmission and Network Management for Telecommunications is not permitted

## 3. GENERAL FUNCTIONAL DESCRIPTION

This specification is for an off-line modular, hot pluggable, N+1,(N=5 max) redundant, power factor corrected, multiple output, CE Mark compliant switching power supply for use in computer systems. The power supply may be used as a non-redundant, single unit. The power supply shall be totally self-contained with internal fan(s) for forced air-cooling.

## 4. ELECTRICAL

### 4.1 AC INPUT

4.1.1 Voltage / Current / Frequency

The power supply shall operate within all specified limits over the ranges as defined in Table 2. The power supply shall be capable of start-up (power-on) with full rated power load at line input as low as 90 VAC.

The power supply internal circuitry shall limit maximum input current to 10A over all rated input and operating ambient conditions. During AC input drop out and recovery condition, input current may exceed 10A for 5 seconds maximum.

**TABLE 2 - INPUT RATINGS**

| PARAMETER | MIN | RATED | MAX |
|---|---|---|---|
| Voltage (Low Line) | 90V | 100V | 132V |
| Voltage (High Line) | 180V | 200-240V | 264V |
| Frequency | 47 Hz | 50 – 60 Hz | 63 Hz |
| Current (Low Line) | | | 8.6A @100VAC* |
| Current (High Line) | | | 4.1A @200VAC* |
| Input Power (Low Line) | | | 840W @115VAC* |
| Input Power (High Line) | | | 812W @230VAC* |
| DC Input Voltage | 192V | 240V | 288V |
| Max DC Input Current | | | 3.6A@240VDC* |

**Note – Current and power ratings are used for reference only. Input currents used for the agency safety label are designated in section 6.6.12.*

4.1.2 Voltage THD

Harmonic voltage distortion of up to 10% THD must not cause the power supply to go out of specified limits. For input voltage types other than sine and/or with distortion greater than 10%, refer to section 4.1.11.

4.1.3 Current THD

The power supply shall incorporate universal input with active power factor correction, which shall reduce line harmonics in accordance with EN61000-3-2 and JEIDA MITI standards. In addition, the power supply shall meet the power factor requirements as specified in Table 3 and 4.

**TABLE 3 –TOTAL HARMONIC DISTORTION (CURRENT)**

| Input Condition(s) | Load Condition(s) | 12VSB Load [A] | 12V Load [A] | Maximum THD [%] |
|---|---|---|---|---|
| 208VAC, 60Hz<br>230VAC, 50-60Hz<br>240VAC, 50-60Hz | ≤5% load | 0 | - | Undefined |
| | >5% - 10% load | 0 | - | 20% |
| | 10% load | 0 | 10% max | 20% |
| | 20% load | 0 | 20% max | 10%* |
| | 30% load | 0 | 30% max | 5%** |
| | >30% load current | 0 | 30% max – 100% max | 5% |

** Between 10% load and 20% load, the THD shall linearly decrease from 20% to 10%.*
*** Between 20% load and 30% load, the THD shall linearly decrease from 10% to 5%.*

Individual harmonic contribution of any fundamental shall not exceed limits as defined in Table 4. In is defined as the RMS value of the current at the 'nth' harmonic. I1 is defined as the RMS value of the first harmonic or the fundamental.

**TABLE 4 – INDIVIDUAL HARMONIC CONTRIBUTION**

| Input Condition(s) | Load Condition(s) | 12VSB Load [A] | 12V Load [A] | $I_n/I_1$ [%] |
|---|---|---|---|---|
| 208VAC, 60Hz<br>230VAC, 50-60Hz<br>240VAC, 50-60Hz | ≤5% load | 0 | - | Undefined |
| | >5% - 10% load | 0 | - | 20% |
| | 10% load | 0 | 10% max | 20%* |
| | 20% load | 0 | 20% max | 10%* |
| | 30% load | 0 | 30% max | 5%** |
| | >30% load current | 0 | | 5% |

** Between 10% load and 20% load, the THD shall linearly decrease from 20% to 10%.*

*** Between 20% load and 30% load, the THD shall linearly decrease from 10% to 5%.*

4.1.4 Power Factor

The power factor shall be equal to or greater than the requirements as defined in Table 5. Power factor measurements shall be performed with source impedance of less than 0.1 Ohm. PFC Guidance: It is expected that the boost converter will operate at the lowest output voltage possible to meet specification for given loading and input conditions.

**TABLE 5 - POWER FACTOR**

| Input Condition(s) | Load Condition(s) | 12VSB Load [A] | 12V Load [A] | Minimum Power Factor |
|---|---|---|---|---|
| 208VAC, 60Hz<br>230VAC, 50-60Hz<br>240VAC, 50-60Hz | 10% load current | 0 | 10%max | 0.94 |
| | 20% load current | 0 | 20%max | 0.96 |
| | 50% load current | 0 | 50%max | 0.98 |
| | 100% load current | 0 | 100%max | 0.98 |

4.1.5 Efficiency

**4.1.5.1 Maximum Power Dissipation: OFF / No Load**

The maximum power supply dissipation for the power supply in an OFF or NO LOAD condition is defined in Table 6.

**TABLE 6 - MAX POWER DISSIPATION FOR NO LOAD/OFF CONDITIONS**

| Input Condition(s) | Load Condition(s) | 12VSB Load [A] | 12V Load [A] | Fan Condition | Max Power Dissipation [W] |
|---|---|---|---|---|---|
| 115VAC<br>230VAC | 1. Standby Power Save Mode | OFF | OFF | OFF | 1 |
| | 2. Standby Mode / No Load | 0 | OFF | MIN RPM | 5 |
| | 3. Output Enabled / No Load | 0 | 0 | MIN RPM | 7 |

**4.1.5.2 Minimum efficiency requirements: Standby Only**

The minimum efficiencies for the power supply in a standby condition are defined in Table 7.

**TABLE 7 - MINIMUM EFFICIENCY FOR STANDBY CONDITIONS**

| Input Condition(s) | Pout [W] | Efficiency [%] |
|---|---|---|
| 115VAC | 6 | 52.0 |
| | 12 | 63.2 |
| | 18 | 66.7 |
| | 24 | 70.6 |
| | 30 | 71.4 |
| 230VAC | 6 | 49.0 |
| | 12 | 63.38 |
| | 18 | 69.38 |
| | 24 | 72.42 |
| | 30 | 74.89 |

#### 4.1.5.3 Minimum efficiency requirements: ON

The minimum efficiency requirements for "ON" conditions (as tested at 25deg C ±3deg) are defined in Table 8.

**TABLE 8 - MINIMUM EFFICIENCY AT LOAD**

| Input Condition(s) | Load Condition(s) | 12VSB Load [A] | 12V Load [A] | Output Watts [W] | Minimum Efficiency [%] |
|---|---|---|---|---|---|
| 115VAC | 10% load current | 0.24 | 6.0 | 75 | 85 |
| | 20% load current | 0.48 | 12.0 | 150 | 89 |
| | 50% load current | 1.20 | 30.0 | 375 | 92 |
| | 100% load current | 2.40 | 60.1 | 750 | 89 |
| 230VAC | 10% load current | 0.24 | 6.0 | 75 | 87 |
| | 20% load current | 0.48 | 12.0 | 150 | 91 |
| | 50% load current | 1.20 | 30.0 | 375 | 94 |
| | 100% load current | 2.40 | 60.1 | 750 | 91 |

4.1.6 AC Inlet Connector

Power supply shall contain an IEC 320 C-14 power inlet. This inlet is rated for a minimum of 10A at 250VAC.

4.1.7 AC Multiple Phase Input Capability

Power supply shall be designed to enable system implementations that use multiple-phase AC input power. In this configuration, not all power supplies in a system are required to be on the same AC input phase.

4.1.8 Range Switching

Power supply shall operate with wide range inputs to accommodate both low and high input ranges without any user intervention or user controls, both at and above rated output power.

4.1.9 Input Leakage Current

Maximum input leakage current at 115V AC, 60Hz shall not exceed 0.5mA.
Maximum input leakage current at 230V AC, 60Hz shall not exceed 1.0mA.

4.1.10 Inrush Current

Inrush current due to EMI filter elements will be limited to 0.2mS in total duration. Maximum current shall be de-rated 50% from the lowest I2t component subjected to the inrush current. AC line inrush current due to power supply turn on shall not exceed 30A peak at all line and load conditions.

Power supply shall meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during hot plug, during any AC dropout condition, over the specified temperature range (Top), and during AC power cycling. The AC power cycling test condition is defined as cycling the AC power off and back on after the power supply has been operating at maximum load and has reached thermal stability. Power supply unit shall meet this inrush current requirement and not be damaged with power input cycling for an indefinite period.

4.1.11 AC Line Dropout

An AC line dropout is the condition when AC input drops below minimum rated input voltage at any phase of the AC line for any length of time. During an AC dropout of one half cycles or less, the power supply shall meet the dynamic voltage regulation limits (Table 16) over 100% of the rated load. An AC line dropout of one half cycles or less shall not cause malfunction of control signals or protection circuits. If the AC dropout time is long enough such that the power supply shuts down, the power supply shall recover safely and meet all turn on requirements. The power supply shall meet the AC dropout requirement over rated AC input voltages, frequencies, and output loading conditions. Any dropout of the AC line shall not cause damage to the power supply. The PSOK signal shall indicate when AC input is valid as defined in Section 4.2.17.3 and Section 4.2.8.

4.1.12 Modified Sine Wave Inputs (UPS)

Some end user systems shall provide AC input power to the power supply via an uninterruptable power supply (UPS). When main AC is lost and the UPS transfers to battery power, the initial transfer shall not exceed the AC line dropout as defined in Section 4.1.11.

The voltage output of the UPS may not reflect a true sine wave. All types of AC presented to the power supply shall be considered valid unless the conditions below are violated:

- Sharp edges or rise times that exceed 2V/us.
- Dead times or 'zero' times in the AC input voltage waveform that exceed 4.5mS. (As measured from +20V to -20V)
- Peak voltages exceeding VACrms*sqrt(2)

When supplied valid AC from the UPS, the power supply shall be able to start and operate within specification. It is acceptable that the supply detects the AC loss and/or abnormal AC and reports PSOK at mid-level. It is not acceptable for the power supply to turn itself OFF or prevent a normal startup due to the perceived AC loss or abnormal AC.

It is recognized that this is an abnormal condition and does not interact with the utility. Therefore for these conditions the power supply is not required to comply with the harmonic current, conducted and ra diated emissions, I2C to UART, power factor, and efficiency requirements in this specification. All other specified parameters apply unless explicitly stated. This UPS section is for design consideration only and is not required to be tested in production of the power supply.

4.1.13 Brownout, Under Voltage

Power supply shall contain protection circuitry such that the application of an input voltage below the minimum specified in Section 4.1.1 shall not cause damage to the power supply unit nor cause failure of the input fuse. In the event of shutdown due to extended brownout, the power supply shall automatically restart after the AC input is within specified limits.

**4.1.13.1 AC Turn Off Requirement**

Power supply shall return to normal power up state after a slow brownout condition. The brownout condition shall be tested with all valid redundant power system configurations using the end use system/s. While the power system is operating at full rated DC load, the AC line voltage shall be reduced from 90VAC/60Hz to 0VAC at a constant rate over a period of 30 minutes. The power shall be then reapplied at 90VAC/60Hz. The PSOK signal shall indicate when AC input is valid as defined in Section 4.2.17.3and Section 4.2.8.

**4.1.13.2 AC Turn On Requirement**

Power supply shall return to normal power up state after a slow brownout or recovery condition. The rate of recovery of the input voltage shall not make any difference to the power supply module. The recovery shall be tested in all valid redundant power system configurations. With the test loads configured for maximum system DC output in resistive mode, the AC line voltage shall be increased from 0VAC to 90VAC/60Hz at a constant rate over 30 minutes. The PSOK signal shall indicate when AC input is valid as defined in Section 4.2.17.3and Section 4.2.8.

4.1.14 Boost Over Voltage

Power supply's boost power factor circuit shall protect against bulk capacitor over-voltage due to boost control circuit or component failure. When a boost over voltage condition is detected, the output 12V shall turn off and remain off until the AC mains power is removed for 30 seconds then reapplied. When a boost over voltage condition is detected, the protection circuit shall guarantee that input to the PFC control circuit remains below minimum operating threshold of the circuit.

***Boost Over voltage guidance:***
The intention of this requirement is to prevent damage to the bulk capacitor. Several boost controllers have built in OVP features that allow the circuit to function in a degraded mode. Operation in this mode must demonstrate that no additional damage occurs. If the built in controller features can be disabled, it is expected that the 12V output shall turn off and remain off until the AC mains power is removed for 30 seconds then reapplied.

4.1.15 Boost Transition Guidance

The power supply shall transition smoothly between boost voltage, frequency, and compensation networks. Boost transitions shall not disrupt the system or cause the power supply to operate outside of specification.

4.1.16 AC Line Fusing

Power supply shall have one line fuse at the AC input. AC line fusing must be acceptable for all safety agency requirements. AC inrush current shall not cause the AC line fuse to open under any conditions. All protection circuits in the power supply shall not cause the AC fuse to open, unless a component in the power supply has failed. This includes DC output overload or shorted output conditions. AC line fusing should make sure the breaker C32 would not become open when power supply unit fail.

4.1.17 Line Transient

Power supply shall operate within specifications under the following conditions:

- Transients as defined in IEC 61000-4-4.
- Transients as defined in IEC 61000-4-5. Up to and including 2 kV limits and phases 0 deg., 90 deg., 180 deg., 270 deg.

4.1.18 Catastrophic Failure Protection

Power supply's circuit design and the components specified in the same shall be such that should a component failure occur, the power supply shall not exhibit the following:

- Flame
- Excessive smoke
- Charred PCB
- Fused PCB Conductor
- Startling noise

4.1.19 Hot Plug Sequencing

The power supply shall be designed such that when operating in redundant configurations, insertion into and removal from the end-system will not interrupt the system operation. During any phase of insertion, start-up, shutdown, or removal, the power supply shall not cause any other like modules in the system to deviate outside of their specifications. Upon application of AC power, the Auxiliary supply shall turn on providing bias power internal to the supply and the 12VSB standby output.

## 4.2 DC OUTPUTS, SIGNAL OUTPUTS, CONTROL INPUTS

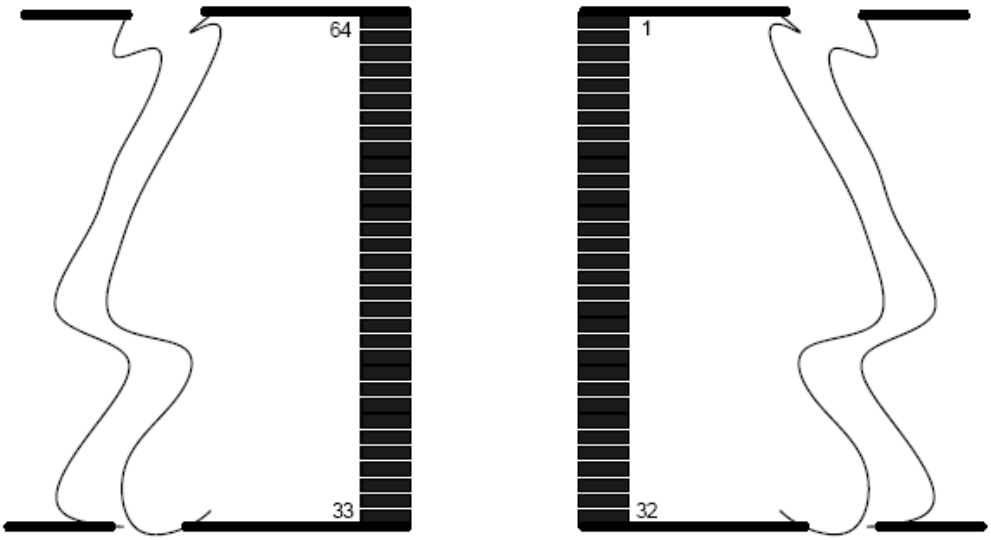
### 4.2.1 Card Edge Output Connector

The output connector shall be a card-edge extension of the PC board internal to the power supply and shall blind mate with a 64 position (32 positions, each side) card edge receptacle. Pin number assignment relates to the card edge finger position as shown in Table 9 and Figure 1. This card-edge shall be dimensioned and located on the power supply as shown in Figure 1. Card edge fingers are dimensioned and numbered according to the details shown in Figure 1. To implement first make last break and last make first break feature, all RTN fingers shall be the longest, Present# finger shall be the shortest, and all other fingers shall be of intermediate length.

**TABLE 9 - PIN NUMBER, FUNCTION, AND DESCRIPTIONS**

| Pin # | Function | Description |
|---|---|---|
| 14-26, 39-51 | RTN | Power and Standby Return |
| 1-13, 52-64 | 12V | 12V Output |
| 37 | 12VSB | 12V Standby Output |
| 38 | PS_INTERRUPT | Power Supply Interrupt signal |
| 36 | PRESENT# | Power Supply Present Signal (shortest pin). |
| 35 | PSOK | Combination of AC input OK and 12V Output OK. |
| 34 | I-MON | 12V load current monitor |
| 33 | PSON# | Power Supply on/off control signal |
| 32 | SCL | Clock |
| 31 | SDA | Data |
| 30 | GND | I2C Signal Ground |
| 29 | ADD0 | Address 0 |
| 28 | ADD1 | Address 1 |
| 27 | ADD2 | Address 2 |

**FIGURE 1 - OUTPUT CONNECTOR**




### 4.2.2 Mating Connectors

Part numbers for the supported mating connectors for this supply are listed in Table 10.

**TABLE 10 - SUPPORTED MATING CONNECTORS**

| TYPE | MANUFACTURER | PART NUMBER |
|---|---|---|
| VERTICAL | TYCO | 1761469 |
| | FCI | 10046971-001LF |
| | FCI | 10111616-00xF |
| RIGHT ANGLE | TYCO | 1761468 |
| | FCI | 10053363-200LF |
| | FCI | 10111743-00xLF |

4.2.3 Output Power

The maximum output power for a single power supply is defined in Table 11. The maximum usable output power shall be derated for configurations with multiple power supplies in parallel. Refer to Section 4.2.9.1 for further definition of N and N+1 load sharing conditions.

**TABLE 11 – MAXIMUM POWER FOR A SINGLE POWER SUPPLY**

| Vin Range | Pmax [W] |
|---|---|
| 90VAC – 108VAC | 750 |
| 108VAC – 132VAC | 750 |
| 180VAC – 264VAC | 750 |

4.2.4 Output Current

The maximum and minimum output currents for each output are defined in Table 12. Refer to Section 4.2.9.1 for further definition of N and N+1 load sharing conditions.

**TABLE 12 – MIN AND MAX OUTPUT CURRENTS (>1 POWER SUPPLIES)**

| Number of Power Supplies in Parallel | 12VSB Min Current [A] | 12VSB Max Current [A] | 12V Min Current [A] | 12V Max Current [A] |
|---|---|---|---|---|
| 1 | 0 | 2.5 | 1* | Pmax/12 |
| 2 | 0 | 2.5 | 1* | 1.8*Pmax/12 |
| 3 | 0 | 2.5 | 1* | 2.7*Pmax/12 |
| 4 | 0 | 2.5 | 1* | 3.6*Pmax/12 |
| 5 | 0 | 2.5 | 1* | 4.5*Pmax/12 |
| 6 | 0 | 2.5 | 1* | 5.4*Pmax/12 |

** The power supply unit shall be capable of operating indefinitely with 0A load on 12V and 12VSB outputs at all line input and operating ambient conditions.*

4.2.5 Output Voltage

**4.2.5.1 Voltage Setpoint**

Minimum, nominal and maximum output voltage set points for 12V and 12VSB are defined in Table 13 along with the load current for adjustment/measurement of the voltage set point. The measurement of the output voltage accuracy is at the PCB mounting pins of the output mating connector in the end use system.

**TABLE 13 - VOLTAGE SET POINT**

| Output | Min [V] | Nominal [V] | Max [V] | Load at Setpoint [A] |
|---|---|---|---|---|
| 12V | 12.27 | 12.30 | 12.33 | 1.0 |
| 12VSB | 11.97 | 12.00 | 12.03 | 0.1 |

#### 4.2.5.2 Remote Sense

Not applicable.

#### 4.2.5.3 Static Regulation / Droop

The 12V and 12VSB outputs shall meet load regulation characteristics of 300mV, ±10% droop from the load at the set point to max load current. These limits do not include the peak-peak ripple/noise specified in Section 4.2.5.4. This load characteristic plus connector resistance shall be used to achieve output load share accuracy.

The droop function for 12V may be disabled through firmware as defined in section 13.

**TABLE 14 –STATIC REGULATION LIMITS**

| OUTPUT | MIN LIMIT [V] | MAX LIMIT [V] |
|---|---|---|
| 12V | 11.97 | 12.33 |
| 12VSB | 11.67 | 12.03 |

#### 4.2.5.4 Ripple/Noise

Ripple and noise shall be measured at the power supply output connector over a bandwidth of 0Hz to 20MHz. Output Ripple and Noise shall not exceed the limits in Table 15. For this measurement, the minimum capacitive load (as specified within Table 19) shall be in parallel with a 10 F tantalum capacitor (minimum 100m ESR) and with a 0.47 F ceramic capacitor placed at the point of measurement.

**TABLE 15 –RIPPLE AND NOISE LIMITS**

| OUTPUT | MAX RIPPLE [mV pk-pk] |
|---|---|
| 12V | 120 |
| 12VSB | 120 |

#### 4.2.5.5 Dynamic Regulation

The 12V and 12VSB output voltages shall remain within limits specified in Table 16 when subject to transient loads as specified in Table 17. The dynamic tolerance includes the static regulation tolerance. Additionally, the following regulation limits shall be met when one out of two units operating in parallel is disabled by way of AC input removal or toggling PSON# signal high. Combined output load of two PS shall be equal to the maximum rating of one PS corresponding to AC input line condition described in Table 11.

**TABLE 16 –DYNAMIC REGULATION LIMITS**

| OUTPUT | MIN [V] | MAX [V] | Condition / Duration |
|---|---|---|---|
| 12V | 11.60 | 12.60 | Normal Operating conditions / At all times |
| 12VSB | 10.80 | 13.20 | |

Load transient repetition rate shall be tested across all possible frequencies (10Hz to 1kHz). This load transient repetition rate is only a test suggestion; LiteON expects the vendor to demonstrate that the supply shall be stable and meet the dynamic response requirements for any possible frequency.

LiteON guidance is that the settling time for all load changes shall be 100uS or less.

**TABLE 17 –OUTPUT TRANSIENT LOAD REQUIREMENTS**

| OUTPUT | STEP LOAD CHANGE | SLEW RATE [A/usec] | MIN CAPACITIVE LOAD [uF] | TEST DESCRIPTION |
|---|---|---|---|---|
| 12V | 50% *minimum static load of 1A)* | ≤ 0.5 | 2,200* | Applies to single and redundant configurations. |
| 12V | 65-130% *10ms pulse duration* | ≤ 0.5 | 2,200* | |
| 12VSB | 100% *(minimum static load of 0A)* | ≤ 0.5 | 270* | |

** Refer to Section 4.2.6*

**TABLE 18 –OUTPUT TRANSIENT LOAD REQUIREMENTS – SPECIAL CONDITIONS**

| OUTPUT | STEP LOAD CHANGE | SLEW RATE [A/usec] | MIN CAPACITIVE LOAD [uF] | TEST DESCRIPTION |
|---|---|---|---|---|
| 12V | 0-70% | ≤ 0.5 | 4,400* | Applies to 1+1 redundant configuration with 1 unit in voltage step-down mode. The 0-70% step change is seen by the unit that is coming out of step-down mode as the active unit is turning OFF or deasserting. |

** Refer to Section 4.2.6*

4.2.6 Capacitive Loading

The power supply (whether single or in parallel configurations) shall be unconditionally stable under all specified operating conditions with the system capacitive load conditions as defined in Table 19. For cases where no system capacitance is present – the power supply shall be unconditionally stable.

**TABLE 19 – SYSTEM CAPACITANCE**

| OUTPUT | MIN | MAX |
|---|---|---|
| 12V | One 2,200uF* per power supply | 22,000uF maximum for any configuration. (1 power supply – 6 power supplies) |
| 12VSB | One 100uF** per power supply. | 1000uF maximum for any configuration (1 power supply – 6 power supplies) |

*System Capacitor Guidance – 12V

The following capacitor families are examples of capacitors that are used in the 2011 common design for the systems using this power supply.

- ZLH family from Rubycon, 16V, 17m ESR (@20degC, 100kHz)
- KZH family from Nippon-Chemicon, 16V, 16m ESR (@20degC, 100kHz)
- UHV family from Nichicon, 16V, 16m ESR (@20degC, 100kHz)

**System Capacitor Guidance – 12VSB

The following capacitor type is used in the 2011 common design for the systems using this power supply.

- SEPC family from Sanyo, 16V, 10m ESR (@20degC, 100kHz)
- Earlier generation systems may have designs with 100uF capacitors and approximate 16mohm ESR each. For this case, the supply shall be stable and fully meet specification.
- There are also conditions in which 12VSB has 0uF on the outputs. For this case – the supply shall be unconditionally stable and ripple limits are extended. (Refer to Ripple/Noise Section).

4.2.7 Startup / Shutdown

All outputs shall rise and fall monotonically. At startup, before PSOK is valid – the maximum load that shall be applied on the outputs is 50% of the maximum current rating for the supply. Refer to the ON/OFF timing specifications for additional information.

NOTE: Single unit turn on and rise time of the 12VSB and 12V shall be controlled such that 12VSB always leads the 12V.

4.2.8 Timing Requirements

Figure 2 and Figure 3 illustrate the timing requirements for single power supply ON/OFF sequence. Figure 4 illustrates the behavior of PSOK for an AC recovery condition. Figure 5 shows the timing requirements associated with the IMON signal.

**FIGURE 2 – SINGLE POWER SUPPLY TIMING FOR AC ON/OFF CYCLE (PSON# LOW)**

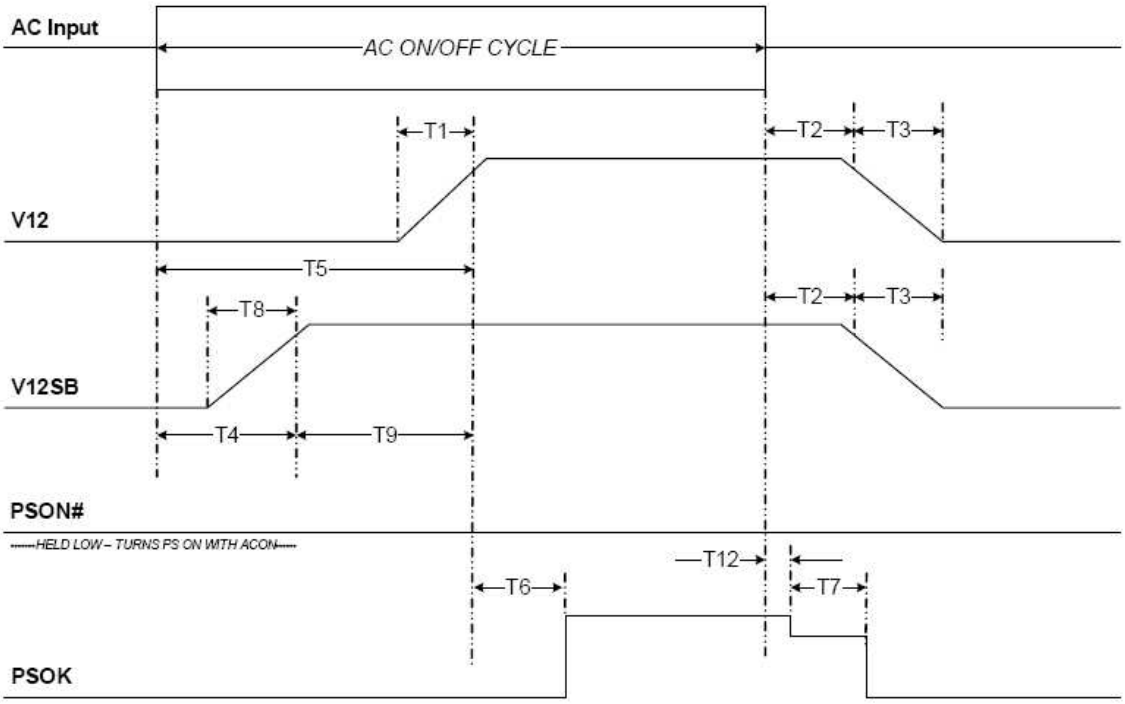
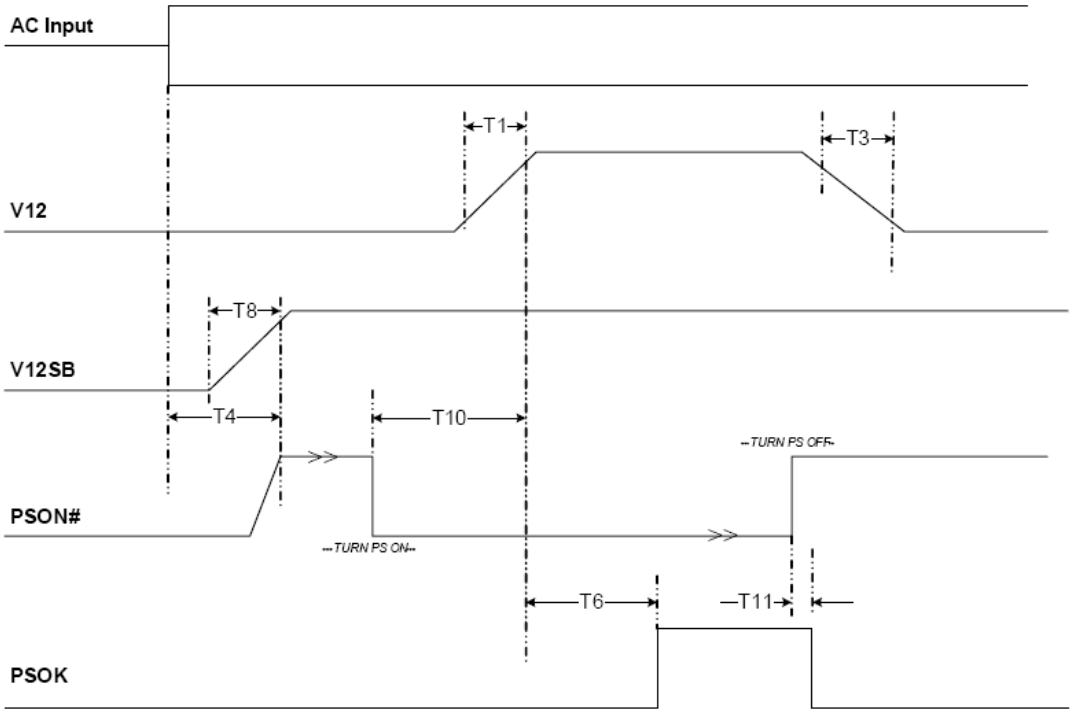
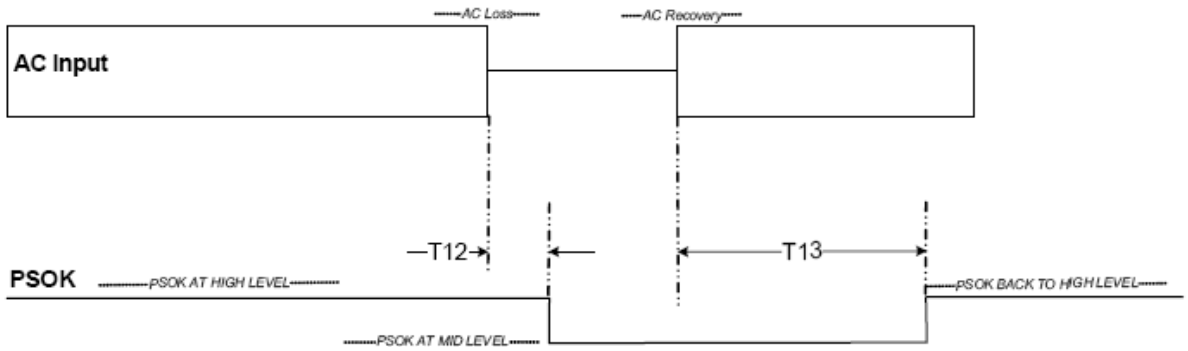



**FIGURE 3 – SINGLE POWER SUPPLY TIMING FOR PSON# CYCLE**



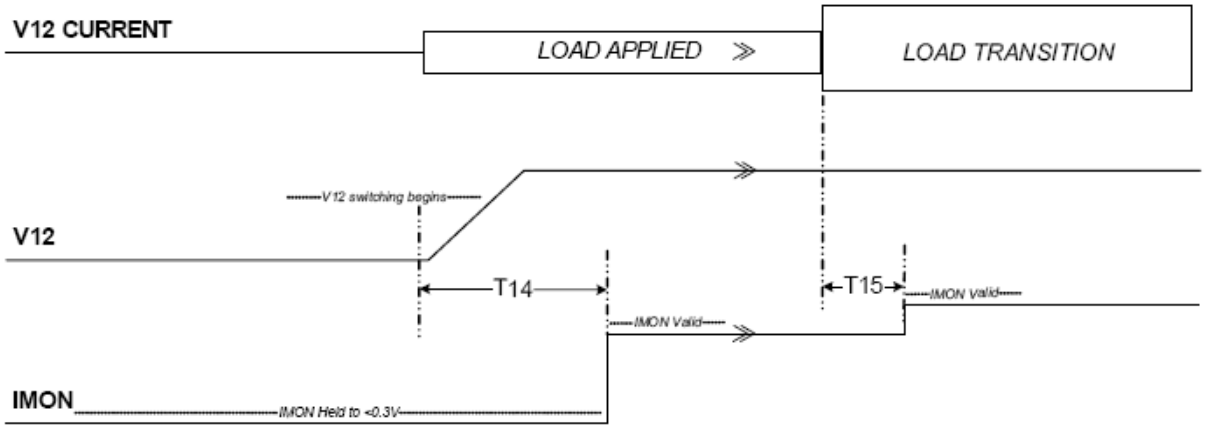

| | | | |
|---|---|---|---|
| Lite-On Technology Corp. | SIZE **A** | **PS-2751-7H-LF** LiteON 750W | REV D |
| | DRAWN | SCALE 1/1 | SHEET 20 OF 112 |

**FIGURE 4 – PSOK TIMING FOR AC LOSS AND RECOVERY**




**(For cases in which PSOK does not go low before AC is recovered)**

**FIGURE 5 – IMON TIMING CHARACTERISTICS**



## TABLE 20 – SINGLE POWER SUPPLY TIMING REQUIREMENTS

| Label | Description | MIN | MAX | UNITS |
|---|---|---|---|---|
| T1* | 12V rise time (10% to 90%) | 10 | 30 | msec |
| T2* | AC input off to 12VSB or 12V 90% of regulation<br>Condition: 100% Pout_max | 10 | | msec |
| T2* | AC input off to 12VSB or 12V 90% of regulation<br>Condition: 50% Pout_max | 20 | | msec |
| T2* | AC input off to 12VSB or 12V 90% of regulation<br>Condition: 25% Pout_max | 30 | | msec |
| T2* | AC input off to 12VSB or 12V 90% of regulation<br>Condition: 12.5% Pout_max | 40 | | msec |
| T3* | All outputs falling from 90% regulation to < 0.3V with respect to common return (12V@1A, 12VSB@0.1A). | | 500 | msec |
| T4* | AC input on to 12VSB at 90% of final value after AC has been removed for more than 5 seconds. | 800 | 1300 | msec |
| T5* | AC input on to 12V at 90% of final value with PSON# asserted low after AC has been removed for more than 5 seconds. | 1000 | 1500 | msec |
| T6* | 12V at 90% of final value to PSOK high. | 50 | 100 | msec |
| T7* | PSOK Mid level to PSOK low | 6 | | msec |
| T8* | 12VSB rise time (10% to 90%) | 10 | 30 | msec |
| T9* | 12VSB in regulation to 12V at 90% of final value at AC turn on with PSON# low. | 50 | 300 | msec |
| T10* | PSON# low to 12V at 90% of final value when AC has been present for more than 5 seconds. | 10 | 30 | msec |
| T11* | Delay from PSON# high to PSOK low. | | 50 | msec |
| T12* | Delay from AC input OFF or Not Valid to PSOK mid level. | 0 | 4 | msec |
| T13* | PSOK Recovery for conditions in which AC loss is detected AND AC is restored before PSOK transitions low. | | 100 | msec |
| T14* | Delay from time 12V output begins switching till time Imon reports a valid reading.<br><br>IMON shall be held to <0.3V until this time has expired. | $T1_{min}$ + 10mS | $T1_{max}$ + 20mS | msec |
| T15* | Delay from output current transition to valid I-monitor signal change | | 500 | usec |

*Note – All timing requirements apply to full range of input voltages as specified in Section 4.1

4.2.9 Load Sharing

#### 4.2.9.1 12V Output Load Sharing

The 12V output shall load share with up to 6 power supplies in parallel using the droop current share method. For cases where the nominal 12V current per PS is >50% of the maximum current capability of a single supply, the 12V main outputs of the power supplies shall current share within ±10% of the nominal current per PS. For all conditions, should reverse current exist in parallel conditions, the power supply shall not be damaged or shut off unexpectedly. Provided these conditions are met – no supply will exceed the maximum output power for a single power supply.

**TABLE 21 – REDUNDANT 12V LOAD SHARING (N+1)**

| # PS in Parallel [N+1] | Max System Load [Imax] | Nominal current per PS [Inom] | PS1 Current | PS2 Current | PS3 Current | PS4 Current | PS5 Current | PS6 Current |
|---|---|---|---|---|---|---|---|---|
| 2 | 6.25A[c] | Inom = System Load / # PS | Inom ±10%* | Inom ±10%* | N/A | N/A | N/A | N/A |
| 3 | 112.5A[c] | | Inom ±10%* | Inom ±10%* | Inom ±10%* | N/A | N/A | N/A |
| 4 | 168.8A | | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* | N/A | N/A |
| 5 | 225A | | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* | N/A |
| 6 | 281.3A[c] | | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* |

** ±10% valid only when Inom is > 50% of max current for a single supply*

**TABLE 22 – NON REDUNDANT 12V LOAD SHARING (N)**

| # PS in Parallel [N] | Max System Load [Imax] | Nominal current per PS [Inom] | PS1 Current | PS2 Current | PS3 Current | PS4 Current | PS5 Current | PS6 Current |
|---|---|---|---|---|---|---|---|---|
| 2 | 112.5A | Inom = System Load / # PS | Inom ±10%* | Inom ±10%* | N/A | N/A | N/A | N/A |
| 3 | 168.8A | | Inom ±10%* | Inom ±10%* | Inom ±10%* | N/A | N/A | N/A |
| 4 | 225A[c] | | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* | N/A | N/A |
| 5 | 281.3A[c] | | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* | N/A |
| 6 | 337.5A[c] | | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* | Inom ±10%* |

** ±10% valid only when Inom is > 50% of max current for a single supply*

#### 4.2.9.2 12VVSB Output Load Sharing

The 12VSB output shall load utilize the droop current share method as defined in Section 4.2.5.3.

For configurations of two power supplies in parallel and a system load >1.25A, the two power supplies shall current share their 12VSB outputs within ±50% of the nominal current per PS. For configurations greater than 2 power supplies, the supplies are not required to accurately current share. The total system current on the 12VSB Is limited to 2.5A regardless of number of supplies and therefore no supply shall be overburdened. For all conditions, should reverse current exist in parallel conditions, the power supply shall not be damaged or shut off unexpectedly.

**TABLE 23 – 12VSB LOAD SHARING**

| # PS in Parallel [N+1] | Max System Load [Imax] | Nominal current per PS [Inom] | PS1 Current | PS2 Current | PS3 Current | PS4 Current | PS5 Current | PS6 Current |
|---|---|---|---|---|---|---|---|---|
| 2 | 2.5A | Inom = System Load / # PS | Inom ±50%* | Inom ±50%* | N/A | N/A | N/A | N/A |
| 3 | 2.5A | | ≤2.5A | ≤2.5A | ≤2.5A | N/A | N/A | N/A |
| 4 | 2.5A | | ≤2.5A | ≤2.5A | ≤2.5A | ≤2.5A | N/A | N/A |
| 5 | 2.5A | | ≤2.5A | ≤2.5A | ≤2.5A | ≤2.5A | ≤2.5A | N/A |
| 6 | 2.5A | | ≤2.5A | ≤2.5A | ≤2.5A | ≤2.5A | ≤2.5A | ≤2.5A |

** ±50% valid only when Inom is > 1.25A*

4.2.10 Load Monitoring (IMON)

Power supplies shall provide an analog output (IMON) representing 12V output load current. This signal may be monitored by the system to determine total load demand on the 12V output. I-Monitor signal provides both the load sharing function (as a feedback for output regulation droop function) and 12V output current information. Signal characteristic is defined below in Table 24. Additional timing requirements may be located in the timing definitions (Section 4.2.8)

- Signal noise when measured at the mating connector end of the card edge shall be less than 250mV peak to peak at 20 MHz bandwidth.
- Signal noise when measured in the end use system shall be designed to be less than 500mV peak to peak at 250 MHz bandwidth.

**TABLE 24 - I-MONITOR OUTPUT CHARACTERISTIC**

| Item | Description | Min | Nominal | Max | Units |
|---|---|---|---|---|---|
| $V_{share}$; $I_{out}$= 75A | Voltage of load monitor bus. | 3.88 | 4.00 | 4.12 | V |
| $V_{share}$; $I_{out}$= 62.5A | Voltage of load monitor bus. | 3.23 | 3.33 | 3.43 | V |
| $V_{share}$; $I_{out}$= 37.5A | Voltage of load monitor bus. | 1.94 | 2.00 | 2.06 | V |
| $V_{share}$; $I_{out}$= 15A | Voltage of load monitor bus. | 0.76 | 0.8 | 0.84 | V |
| $V_{share}$; $I_{out}$= 3.75A | Voltage of load monitor bus. | 0.16 | 0.2 | 0.24 | V |
| $V_{share}$; $I_{out}$= 0A | Voltage of load monitor bus. | -0.2 | 0 | 0.2 | V |
| $\Delta V_{share}/\Delta I_{out}$ ; $I_{out}$>0.5A | Slope of load monitor bus voltage with changing load. | | 4 / $I_{outmax}$ | | V / A |
| $I_{share}$ sink; $V_{share}$=4V | Amount of current the load monitor bus output from each power supply sinks. | | | 0.25 | mA |
| $I_{share}$ source; $V_{share}$=4V | Amount of current the load monitor bus output from each power supply sources. | 2.0 | | | mA |
| $T_{repsonse}$ | Delay from output current transition to I-monitor signal change | | | 500 | usec |

4.2.11 Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. The microprocessor and its I2C communication bus is expected to continue operating under a fault protection condition. 12VSB output shall remain powered on if the failure does not involve this output. When a protection circuit shuts down the power supply, green LED shall change to unlighted status and the PSOK signal shall be asserted LOW. If the power supply latches off due to a protection circuit tripping, AC input or PSON# signal toggle shall release latch condition and the power supply shall attempt to provide output power to the load. Minimum time delay for the toggle function shall be AC input OFF for 15sec, PSON# cycle HIGH for 1sec.

Power to Micro controller circuitry associated with I2C communication to the system shall be logic OR between power supply internal source and system side 12VSB.

#### 4.2.11.1 12VSB Over Current Protection

The power supply shall provide limited output current to the load for protecting the power supply from damage under indefinite over load conditions. 12VSB over current protection shall be hiccup (output re-try at a constant interval). A sustained overload shall not latch off 12VSB output. 12VSB over current limit level shall be maintained for a period of 100 msec. minimum and 500 msec. maximum.

**TABLE 25 – 12VSB OVER CURRENT PROTECTION (HARDWARE LIMIT)**

| OUTPUT | MINIMUM OVER CURRENT LIMIT | MAXIMUM OVER CURRENT LIMIT | Response Time | Type |
|---|---|---|---|---|
| 12VSB | 3.5A | 5A | 100mS – 500mS | Constant Current, Hiccup |

#### 4.2.11.2 12V Over Current Protection

The power supply shall provide limited output current to the load for protecting the power supply from damage under indefinite over load conditions. 12V over current protection shall be constant current type. Maximum short circuit current is limited only by the output load impedance and output voltage level during the short circuit. It is expected that the supply will self protect for any load over the maximum over current trip point. Over current limit level shall be maintained for a period of 100ms minimum and 200ms maximum. During the overcurrent event – it is not required to meet regulation limits. After this time the power supply shall latch off. The latch shall be cleared by toggling PSON# signal or by an AC input re-cycle.

**TABLE 26 – 12V OVERCURRENT PROTECTION**

| OUTPUT | MINIMUM OVER CURRENT LIMIT | MAXIMUM OVER CURRENT LIMIT | Response Time | Type |
|---|---|---|---|---|
| 12V | 105% of Imax | 125% of Imax | 100mS – 200mS | Constant Current, Latch |

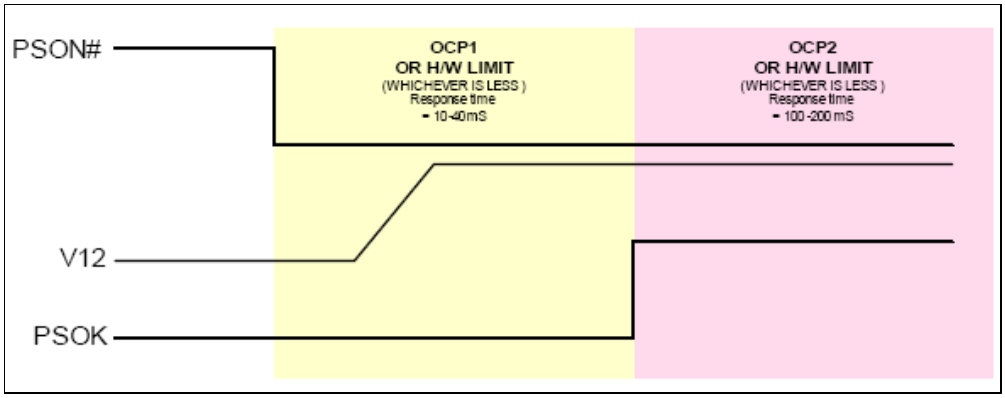
#### 4.2.11.3 12V Programmable Current Limit

In addition to the 12V current limit, there exists in the firmware an ability to write system specific current limits for the main output into register locations (register 0x5A and register 0x5C) through I2C commands. These software limits (OCP1 and OCP2) shall always be less than or equal to the hardware current limit. The basic functionality of the OCP limits and the hardware limit is shown in the following figure. Refer to section 12.4.3 for the register definitions.

OCP1 is the startup current limit. This condition is ONLY valid for the case where PSON# has transitioned from high to low and PSOK is low. The fault response time for OCP1 shall be 10mS minimum and 40mS maximum. If at the end of the OCP1 time delay the current still exceeds OCP1, the main output shall latch off. (A latch off condition can only be reset by an AC cycle, PSON# toggle, or a standby overcurrent).

OCP2 is the steady state current limit. It shall always be less than or equal to the hardware limit of the power supply. PSON# must be low and PSOK must be high for this limit to be valid. The fault response time for OCP2 is the same as for the Hardware current limit: 100ms minimum and 200mS maximum. If at the end of the OCP1 time delay the current still exceeds OCP2 limits or the Hardware limit (whichever is less), the main output system shall latch off. (A latch off condition can only be reset by an AC cycle, PSON# toggle, or a standby overcurrent).

**FIGURE 6 – 12V CURRENT LIMIT TIMING (HARDWARE AND SOFTWARE)**



#### 4.2.11.4 12VSB Overvoltage Protection

Power supply over voltage protection shall be locally sensed. Power supply shall shutdown in a retry hiccup mode upon an over voltage condition on the 12VSB output. This latch shall be cleared by toggling the PSON# signal or by an AC input re-cycle. Table 27 contains the minimum and maximum output voltage levels for this condition. Output levels shall be measured at the pins of card edge receptacle with minimum and maximum output loads.

**TABLE 27 – 12VSB OVERVOLTAGELIMITS**

| OUTPUT | MAXIMUM VOLTAGE LIMITS [V] |
|---|---|
| 12VSB | 13.6 --- 15.0 |

#### 4.2.11.5 12V Overvoltage Protection

Power supply over voltage protection shall be locally sensed. Power supply shall shutdown in a latch off mode upon an over voltage condition on 12V output. This latch shall be cleared by toggling the PSON# signal or by an AC input re-cycle. Table 27 contains the minimum and maximum output voltage levels for this condition. Output levels shall be measured at the pins of card edge receptacle with minimum and maximum output loads.

**TABLE 28 – OUTPUT OVERVOLTAGE LIMITS**

| OUTPUT | MAXIMUM VOLTAGE LIMITS [V] |
|---|---|
| 12V | 13.6 --- 15.0 |

#### 4.2.11.6 Internal Fan Fault Protection

See section 4.2.15 for description of protection from faulted fan(s).

#### 4.2.11.7 Over Temperature Protection

The power supply shall be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature which could cause internal part failures. In an over temperature condition the PS shall shutdown. The 12VSB shall not shutdown during an OTP condition on the main outputs. When the temperature drops to within safe operating limit for internal parts, the power supply shall restore power automatically. The OTP circuit shall incorporate built in hysteresis such that the power supply does not oscillate on and off due to temperature recovering condition. The power supply shall alert the system of the OTP condition via the power supply PSOK signal changing to a low state and the green LED changing to an unlighted condition.

### 4.2.12 12VSB Shutdown

12VSB is a standby 12V rail that can be ON as long as input to the unit is within operating range per section 4.1.1 and output current is within rating per section 4.2.3. This rail may be disabled to enter standby power supply shutdown mode when the system writes to SF6 in the PS Control register.

**Standby power supply shutdown circuitry requirements:**

- Must be able to disable all converters.
- Must maintain intelligence from 12VSB bus while all converters are disabled.
- Must be able to successfully bring the converters back online.
- When exiting this mode ensure that Bit D of the PS Control register is set to 0.
- Must not enter this mode unless all of the following occur:
  - There is no 12V on the main output.
  - The power supply is in standby.
  - Bit D in the PS Control register is set to 1 by the system.

- Must re-enable all converters when any of the following occur:
  - Bit D of the PS Control register is set to 0 by the system.
  - PSON transitions to logic low.
  - 12VSB falls below 10.8V
  - 12V is detected on the 12V output.
  - The secondary microcontroller loses its input voltage.
- When exiting this mode ensure that Bit D of the PS Control register is set to 0.

4.2.13 Hot Swap Requirement

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltage (including 12VSB) shall remain within the limits specified in Table 16 with the capacitive load specified in Table 19. Hot swap test shall be conducted when the system is operating under both static and dynamic conditions. Power supply unit can be hot swapped by the following methods:

1. AC inlet on the exterior face of the power supply (opposite the DC connector). Extraction: The AC power is disconnected from the power supply then the power supply is removed from the system. Insertion: The power supply is inserted into the system without the AC power applied then the AC power is applied.
2. Server management turning on the hot swapped power supply. Extraction: Server management turns off only one of the power supplies via the PSON# signal then the power supply is removed from the system. Insertion: Power supply is inserted into the system, server management looks for power supply, depending upon the state of the system (on or off), the system then turns on the power supply via the PSON# signal or goes to standby mode operation.
3. AC inlet on the exterior face of the power supply (opposite the DC connector). Extraction: The power supply is removed from the system with the AC power still applied to the power supply and the power supply ON. Insertion: Power supply is inserted into the system with the AC power applied, power supply shall turn on when docked into the system.

Many variations of the above are possible. Supplies need to be compatible with these different variations. In general, a failed (off by internal latch or external control) supply may be removed, then replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply may get turned on by plugging AC into the external face, or by system management recognizing an inserted supply and explicitly turning it on.

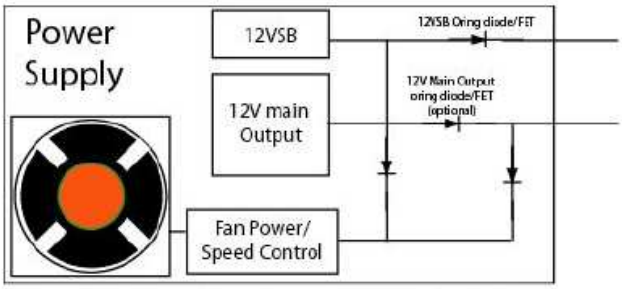
4.2.14 Output Isolation/Or ing Diode

Not applicable.

4.2.15 Internal Cooling Fans

Power supply shall use 40mm x 40mm high-speed 12V input fan, see Section 10. Fan shall be powered from system side 12V output. Power supply internal 12VSB power shall be diode OR connected as a source for fan operation in standby only condition. Operating conditions like power supply removal, insertion, fan turn-on, turn-off, fault conditions like fan open circuit or fan short circuit shall not cause system side 12V output or 12VSB to deviate outside dynamic regulation limits. Fan fault protection circuits are not required.

**FIGURE 7 - FAN POWER DIAGRAM**




Fan(s) is (are) powered from internal 12VSB diode or'ed with 12V main output common bus as shown above

4.2.16 Fan Speed Control

In standby mode power supply fan may operate at minimum speed to maintain component reliability at all load, line and ambient conditions.

When 12V output is enabled, power supply fan shall operate at minimum achievable fan speed. Power supply shall contain fan speed control circuits to vary the speed so that the critical component temperatures do not exceed safe operating levels. A scheme where the fan's speed is constantly adjusted to maintain critical component's temperature under reliable operating threshold is the required method. Three temperature sensors are required. Sensors are to be located on a critical primary component, a critical secondary component, and at the air inlet to the supply. Refer to firmware requirements as defined in section 12.

Fans shall be powered from voltage source inside the power supply and from system side voltage source.

- In redundant mode, 12V main power available, the fan(s) in the power supply without input AC shall operate at minimum speed, 1500 ±500 RPM, to avoid re-circulation of hot air through it.
- When the power supply is in standby mode, and no 12V main power is present, the fan shall operate at minimum speed.
- If the supply enters power saver mode, 12VSB off, the fan shall be OFF.

When the ambient power supply temperature is greater than 55 ±5C, the power supply shall increase the fan speed. The ambient power supply temperature hysteresis for fan closed control is to be ±5 degree. The power supply shall increase the fan speed linearly to regulate the ambient power supply temperature to prevent, or delay, an over temperature shutdown.

Power supply design shall employ PWM control technique to vary fan speed for maintaining hot spot components within reliable limits.

4.2.17 Other Control and Indicator Functions

The following sections define the input and output signals from the power supply. Signals that can be defined as Active Low true use the following convention: signal# = Active Low.

#### 4.2.17.1 PSON#

PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the 12V power rail. When this signal is not pulled low by the system, or left open, the 12V output is turned off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to the Section 4.2.8 for timing specifications. When in off or standby condition, the 12V output shall be less than 50mV with respect to output return.

- Signal noise when measured at the mating connector end of the card edge shall be less than 250mV peak to peak at 20 MHz bandwidth.
- Signal noise when measured in the end use system shall be designed to be less than 500mV peak to peak at 250 MHz bandwidth.

**TABLE 29 - PSON# SIGNAL CHARACTERISTIC**

| **SIGNAL TYPE** | **Accepts an open collector/drain input from the system. Pull-up internal to the power supply.** | |
|---|---|---|
| $PSON^{\#}$ = Low | ON | |
| $PSON^{\#}$ = Open | OFF (Not installed in system) | |
| $PSON^{\#}$ = High | OFF | |
| | MIN | MAX |
| Logic level low (power supply ON) | 0V | 0.8V |
| Logic level high (power supply OFF) | 2.0V | 3.30V +5% |
| Source current, Vpson = low | | 1mA |
| Signal rise and fall time | | 200usec |

#### 4.2.17.2 PRESENT# (Power Supply Present Indicator)

PRESENT# signal is used to sense the number of power supplies in the system (operational or not) and provide hot plug insertion and removal functionality by controlling main outputs during hot plug insertion and removal by employing following circuitry. When the unit is not connected to the system, fast shut down signal in the power supply does not allow main outputs to be turned ON. Similarly when the unit is removed from the system the fast shut down signal quickly turns OFF main outputs and discharges output capacitors. This signal shall be the shortest gold finger pin on the card edge to allow for last make, first break configuration.

- Signal noise when measured at the mating connector end of the card edge shall be less than 250mV peak to peak at 20 MHz bandwidth.
- Signal noise when measured in the end use system shall be designed to be less than 500mV peak to peak at 250 MHz bandwidth.

**FIGURE 8 – PRESENT# INDICATOR ARCHITECTURE**

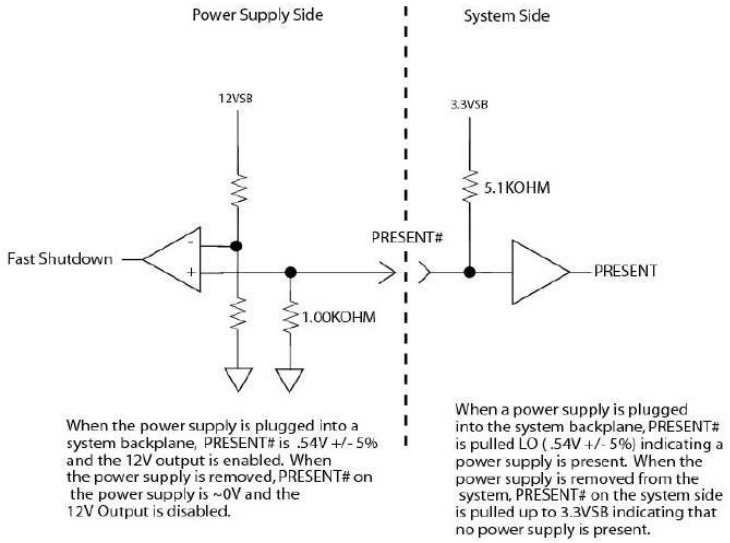



**TABLE 30 - PRESENT# SIGNAL CHARACTERISTICS**

| SIGNAL TYPE | Output From Power Supply, Pull-Up To 3.3VSB with 5.1k in System. | |
|---|---|---|
| PRESENT# = Low | Present | |
| PRESENT# = High | Not Present | |
| | MIN | MAX |
| Logic level low voltage | 0V | 0.6V |
| Logic level high voltage, Isink=50µA | 1.0V | 3.30V +5% |
| 12V Output enable threshold | 350mV | |
| 12V output disable threshold | 150mV | 250mV |
| Sink current, PRESENT# = low | | 1 mA |
| Signal transition time. Transition is defined as period during system insertion or removal as the Present pin makes or breaks contact with a powered system. | | 200usec |

#### 4.2.17.3 PSOK (Output OK Indicator)

PSOK is a combined indicator of AC input and 12V DC output conditions. This is a three level signal to indicate different stages as follows.

- AC not OK and DC not OK – Signal status shall be LOW (<0.6V).
- AC OK and DC not OK – Signal status shall be LOW (<0.6V).
- AC OK and DC OK – Signal status shall be HIGH (> 3.0V).
- AC not OK and DC OK – Signal status shall be Mid Level (Between 2V and 2.5V).
- DC OK threshold is defined as when the 12V output is greater than 11.5V.
- DC not OK threshold is defined as when the 12V output is less than 11.4V and greater than 11.3V.
- AC line input shall be sensed on the utility side of the input fuse.
- AC OK shall be defined as when the AC is present (as sensed by the utility side of the fuse) ~and~ the input conditions are valid (Section 4.1.1)
- AC NOT OK shall be defined as when either AC is not present (as sensed by the utility side of the fuse) ~OR~ the input conditions are not valid (Section 4.1.1)

To achieve desired results microcontroller circuits and other signal related logic shall be wire or'ed between internally generated Vcc and 12VSB output.

- Signal noise when measured at the mating connector end of the card edge shall be less than 250mV peak to peak at 20 MHz bandwidth.
- Signal noise when measured in the end use system shall be designed to be less than 500mV peak to peak at 250 MHz bandwidth.

When operating two power supplies in parallel, PS OK signal detection and control function shall be designed such that an internal failure of the power supply (e.g. controller, driver, primary component etc) shall cause the signal to switch from HIGH to LOW. There shall be a specific detection circuit to manage PS OK signal level when a power supply unit is turned on into an existing 12V bus and turned off from an existing 12V bus or by an internal failure. This requirement also applies to 2 power supplies connected in parallel and one of the power supplies is put into Low Output Voltage Mode through I2C register 0x3A (Vout Step Down Mode – System Type 5 or Special Function 5).

**TABLE 31 - PSOK SIGNAL CHARACTERISTICS**

| SIGNAL TYPE | Output from power supply. Powered from12VSB output common to the system. | |
|---|---|---|
| PSOK = High | PS Good | |
| PSOK = Low | PS Not Good | |
| PSOK = Mid | AC Bad, DC Good | |
| | MIN | MAX |
| Logic level low voltage | 0V | 0.6V |
| Logic level mid voltage | 2.0V | 2.5V |
| Logic level high voltage | 3.0V | 3.30V +5% |
| Sink current, PSOK = low | | 1mA |
| Source current, PSOK = mid | | 200uA |
| Source current, PSOK = high | | 1mA |
| Signal rise and fall time | | 200µsec |

#### 4.2.17.4 I2C DATA and CLOCK

Two pins at the power supply connector are allocated for the I2C serial clock (SCL) and serial data (SDA) signals. Both pins are bi-directional and are used to form the serial I2C bus. I2C data and clock signals shall be used to communicate power supply status with the end use system as defined in Section 12.

**Hardware requirements:**

- Internal Connection: SCL and SDA shall each be pulled up internally within the power supply with a 20k resistor. The power for the I2C clock and data lines internal to the power supply shall be 5.0V and generated from the system side of the 12VSB. This configuration allows a system with available redundant standby power to be able to access the uC on a power supply in which the input power has been removed.) Capacitance on each signal internal to the Power Supply shall be less than 150pF.
- System Side Connection SCL and SDA shall also be pulled up externally by the system with 3k – 10K resistors. SCL and SDA on the system side shall be pulled up to a 5Vsb rail also generated from the 12VSB. If the system I2C bus voltage is not 5.0V, then the system shall implement level shifting / isolation circuits between the PS side and the system side of the bus.

**Measurement Requirements:**

- Signal noise when measured at the I2C device (e.g. EEPROM, microcontroller etc.) shall be less than 80% peak to peak of the device rating 20 MHz bandwidth.
- Signal noise when measured at the mating connector end of the card edge shall be less than 250mV peak to peak at 20 MHz bandwidth. Signal noise when measured in the end use system shall be designed to be less than 500mV peak to peak at 250 MHz bandwidth.

#### 4.2.17.5 PS_INTERRUPT Tab

One pin at the power supply connector is allocated for the I2C interrupt open drain signal. Signal behavior in response to certain operating condition changes in the power supply shall meet firmware requirements as defined in the firmware section of this document.

**Hardware Requirements:**

- Internal Connection: Open Drain Signal
- System Side Connection: PS_INTERRUPT shall be pulled up external to the supply to a maximum voltage of 5V. The max sink current shall be 5mA.

**Measurement Requirements:**

- Signal noise when measured at the mating connector end of the card edge shall be less than 80% peak to peak of the device rating 20 MHz bandwidth.
- Signal noise when measured at the mating connector end of the card edge shall be less than 250mV peak to peak at 20 MHz bandwidth.
- Signal noise when measured in the end use system shall be designed to be less than 500mV peak to peak at 250 MHz bandwidth.

### 4.2.17.6 PS ADDRESS LINES

A0, A1, A2 Address pins A0, A1 and A2 are used by end use system to allocate unit address to a power supply in particular slot position as defined in the firmware section of this document.

**Hardware requirements:**

- Internal Connection: A0, A1, and A2 shall each be pulled up internally within the power supply with a 10k resistor. The power for the I2C clock and data lines internal to the power supply shall be 5.0V and generated from the system side of the 12VSB. This configuration allows a system with available redundant standby power to be able to access the uC on a power supply in which the input power has been removed.)

- System Connection: A0, A1, and A2 on the system side may be left floating or pulled down. If pulled down, the pull down resistor shall be a 300 resistor.

**Measurement Requirements:**

- Signal noise when measured at the I2C device (e.g. EEPROM, microcontroller etc.) shall be less than 80% peak to peak of the device rating 20 MHz bandwidth.

- Signal noise when measured at the mating connector end of the card edge shall be less than 250mV peak to peak at 20 MHz bandwidth.

- Signal noise when measured in the end use system shall be designed to be less than 500mV peak to peak at 250 MHz bandwidth.

## 5. ENVIRONMENTAL REQUIREMENTS

All materials in the product must not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) in excess of the limits specified in the RoHS Compliance Specification Addendum to the LiteON General Specification for the Environment (GSE). Upon retirement of the RoHS Compliance Specification Addendum, RoHS material restrictions will be specified directly in the GSE.

### 5.1 TEMPERATURE

5.1.1 Operating

5 to 50 C (End use system maximum ambient of 35 C, internal system temperature rise of 15 C, resulting in 50 C maximum ambient power supply temperature.)

5.1.2 Non-operating

-40 to 85 C

### 5.2 COOLING

Power supply shall meet the requirements of this specification when installed in the intended system.

### 5.3 HUMIDITY

5 to 95% relative humidity, non-condensing, both operating and non-operating

### 5.4 ALTITUDE

5.4.1 Operating

5,000 feet above sea level with no derating. The maximum ambient power supply temperature shall be linearly derated from 50 C at 5,000 feet above sea level to 40 C at 10,000 feet above sea level.

5.4.2 Non-operating

50,000 feet above sea level

### 5.5 MECHANICAL SHOCK

5.5.1 Fixturing

The power supply subassembly may be rigidly clamped directly to the shock equipment surface.

5.5.2 Operating

Half sine wave shock - 5 G, 11 ms duration, half sine wave shock in each direction of 3 mutually perpendicular axes. There shall be one shock input in each direction of 3 mutually perpendicular axes for a total of six shock inputs.

5.5.3 Non-operating

- Half sine wave shock - 140 G, 2 ms duration, half sine wave shock in each direction of 3 mutually perpendicular axes. There shall be one shock input in each direction of 3 mutually perpendicular axes for a total of six shock inputs.
- Square wave shock - 40 G, 166 in/sec velocity change, square wave shock in each direction of three mutually perpendicular axes. There shall be one shock input in each direction of 3 mutually perpendicular axes for a total of six shock inputs.

## 5.6 VIBRATION

5.6.1 Fixturing

The power supply subassembly may be rigidly clamped directly to the vibration equipment surface.

5.6.2 Operating

- Sinusoidal Vibration - 0.25 G zero-to-peak, 10 to 500 Hz, 0.25 oct/min in each of three mutually perpendicular axes. The test duration shall be one sweep from 10 to 500 to 10 Hz in each of 3 mutually perpendicular axes.
- Random Vibration - 0.002 G2/Hz, 10 to 500 Hz, nominal 1.0 Grms in each of 3 mutually perpendicular axes. The test duration shall be one hour/axis for a total test duration of three hours.

5.6.3 Non-Operating

- Sinusoidal Vibration - 0.75 G zero-to-peak, 10 to 500 Hz, 0.5 oct/min. The test duration shall be one sweep from 10 to 500 to 10 Hz in each of 3 mutually perpendicular axes.
- Random Vibration - 0.008 G2/Hz, 10 to 500 Hz, nominal 2.0 Grms in each of 3 mutually perpendicular axes. The test duration shall be one hour/axis for a total test duration of three hours.

## 5.7 PACKAGED VIBRATION AND SHOCK

5.7.1 Shipping Package Vibration (Palletized)

The palletized material shall meet the requirements specified in LiteON. For bulk shipments of printed circuit boards, the packaging shall be designed to protect against damage or loss during shipment or movement within LiteON. Package design criteria are covered in LiteON. Package performance shall be verified using LiteON. Labeling requirements are covered in LiteON, ref. Figures 4 and 5.

5.7.2 Shipping Package Vibration (Individual)

The individual packages shall meet the requirements of LiteON. When shipping a completed option kit, Package design criteria are covered by LiteON. Package performance shall be verified using LiteON. Labeling requirements are outlined in the Bill of Material and covered in detail within LiteON.

## 5.8 ELECTROSTATIC DISCHARGE (ESD)

The power supply shall withstand the following ESD conditions at any point on the power supply enclosure.

- ±15 kV air discharge with no abnormal operation or damage to power supply
- Transients as defined in IEC 801-2
- The storage capacitance shall be 150 pF and the discharge resistance shall be 330 ohms. The power supply shall meet all discharge requirements for the CE Mark designation.

## 6. AGENCY APPROVALS

### 6.1 PRODUCT SAFETY REQUIREMENTS AND APPROVALS

The OEM Power Supply Module shall be approved/licensed/certified as specified below. Copies of ALL approval licenses for the OEM Power Supply Module shall be provided to the Product Safety Group as part of the final OEM Power Supply Module qualification. The OEM Power Supply Module shall pass all applicable safety tests in the end product at the intended load and operating environment (see special considerations below). Besides the required outside Regulatory qualification for the end product with the OEM Power Supply Module, the Product Safety Group reserves the right to conduct all applicable component level Safety tests and evaluations on the OEM Power Supply Module. Samples and information from the OEM Supplier will be requested in order to support this evaluation.

Unless otherwise agreed, the OEM Power Supply shall be certified with all Regulatory Agencies under trademark as a regulatory model. The Power Supply Module nameplate label will contain LITEON company trademark/name and REGULATORY MODEL NUMBER (RMN) HSTNS–XXXX. If no RMN is assigned, the manufacturer's certified model number shall appear. In general, the power supply certifications shall be in the name of the OEM supplier using name or logo as approved trademark identifier. If Co-Licensing is necessary. Co-Licenses can be avoided in most cases by providing the appropriately registered Regulatory File/Project No. under the Approval marks.

**Power supplies with Fans**: If the power supply contains a fan, it should be subjected to the testing in subclasses 2.1.1 and 4.2.5 in IEC 60950/EN 60950/UL 60950/C22.2 No 60950. The agency test reports shall include this testing as part of the evaluation.

The information continued in this section is/was the criteria and approvals anticipated at the time of release of this document. This information may not be current. It is suggested that for current information, LiteON Product Safety Group be contacted.

**EN 60950 (IEC 60950):** The OEM Power Supply Module shall comply with all applicable requirements of EN 60950-1 and IEC 60950-1. The OEM Power Supply Module shall also comply with the applicable requirements of each of the IEC based 60950 based national or regional standards identified below:

**CB SCHEME CERTIFICATION:** The manufacturer of the OEM Power Supply Module shall obtain a CB Test Certificate and CB Test Report from a National Certification Body. The Certificate and Report shall be valid for and state conformity with IEC 60950-1 and EN 60950-1. The report should also include an evaluation of all the country specific deviations (not just the Group deviations). The CB Test Certificate shall contain LiteON's trademark/name LiteON authorized Series number or the manufacturer's model number.

**NA APPROVAL:** The OEM Power Supply Module shall be certified as a component ITE power supply by Underwriters Laboratories Inc. (Recognized Component) or Canadian Standards Association in accordance with UL/CSA 60950-1. The nameplate shall include the Supplier's UL Recognition mark or CSA Mark for both the US and Canada. The Supplier's UL or CSA file number (EXXXXXX or LRXXXXX) and any other required factory identification. All output circuits shall be SELV for external interconnection and operator accessibility. The supplier shall provide a copy of the agency report showing any "conditions of acceptability" that must be considered for the end product application.

**EUROPEAN SAFETY APPROVAL:** The OEM Power Supply Module shall be certified by at least one European Notified Body to the requirements of EN60950-1 and all European country deviations. The Safety Mark issued by that body shall appear on the nameplate label. Typical notified body agencies are TUV, VDE, Nemko, SEMKO, DEMKO, and Fimko.

**CHINA APPROVAL:** The OEM power supply shall be approved by China National Import & export Commodities Inspection Corp. in accordance with and shall comply with GB4943-2001 (IEC 60950-1). The CCC Safety mark shall appear on the product nameplate label as well as the factory name (may be in Chinese).

**TAIWAN:** The product shall be certified for safety by BSMI Taiwan in accordance with Chinese National Standard (CNS) 14336 (IEC60950). The product label shall contain the BSMI ID number. The BSMI certificate must include the LiteON regulatory model number, if applicable.

## 6.2 EMC REQUIREMENTS AND APPROVALS

### 6.2.1 RF Emissions

The information contained in this section is/was the criteria and approvals anticipated at the time of release of this document. This information may not be current. It is suggested that for current information, LiteON EMC Services group be contacted.

If the power supply will not be marketed as an option, only the CISPR REQUIREMENTS and CE REQUIREMENTS sections are applicable. Otherwise, based upon the intended marketing and use of the product, the power supply shall comply with:

**FCC APPROVAL:** All administrative and performance requirements for CFR 47, Part 15 class B using the C.I.S.P.R. Publication 22 limits and the ANSI C63.4 procedures. Radiated emission testing shall be performed at 10 meters. Conducted emission testing shall be performed at the rated line voltages. This device, when tested as part of a system defined by LiteON Company, shall not increase the emissive level of that system to a level greater than 3 dB below the C.I.S.P.R. Publication 22 limits. Testing shall be performed using LiteON Company labeled/manufactured peripherals. The manufacturer shall obtain a Grant of Equipment Authorization from the FCC. The manufacturer shall supply the appropriate information to the user in the user's manual. The product label shall contain the FCC ID and the appropriate statement. As an alternative, the manufacturer shall perform the Declaration of Conformity authorization (e.g., using ~~MVLAP/A2LA~~ accredited laboratories acceptable to the FCC]. The manufacturer shall supply the appropriate information to the user in the user's manual. The manufacturer shall supply the Declaration of Conformity to LiteON. The product label shall contain the FCC.

**C.I.S.P.R. REQUIREMENTS:** All administrative and performance requirements for C.I.S.P.R. Publication 22 Class B. Radiated emission testing shall be performed at 10 meters. Conducted emission testing shall be performed at the rated line voltages. This device, when tested as part of a system defined by LiteON Company, shall not increase the emissive level of that system to a level greater than 3 dB below the Class B limits. Testing shall be performed using LiteON Company labeled/manufactured peripherals.

**AUSTRALIAN ACMA APPROVAL:** All administrative and performance requirements for AS/NZS CISPR22, Class B in accordance with the Electromagnetic Compatibility Framework Information for Suppliers document, July 1995 and URL: http://www.acma.gov.au. The product label shall contain the C-Tick logo and the manufacturer's Supplier Code. Use of an agent is required.

**TAIWAN BSMI APPROVAL:** All administrative and performance requirements for the BSMI Taiwan "Commodity EMC Regulation" in accordance with Chinese National Standard (CNS)13438, (CISPR22), Class B. The product label shall contain the BSMI ID number. The BSMI certificate must include both the LiteON series number and the marketing name. URL: http://www.bsmi.gov.tw

**CHINA CCC APPROVAL:** administrative and performance requirements for the CQC China "Related Regulations of Detailed Rules and Procedures for Implementing the Safety License System of Import Commodities" in accordance with Standard GB9254 (CISPR 22), Class B and URL: http://www.ciq.gov.cn/cqcchina/www/index-e.htm. The product label shall contain the CCC logo. The CCC certificate must include both LiteON series number and the marketing name.

**KOREA KCC APPROVAL:** All administrative and performance requirements for the KCC Korea "EMC Registration Regulation" Class B and URL: http://www.rra.go.kr/ . The product label shall contain the KCC registration number, the KCC certificate applicant name, and, if different, the KCC certificate manufacturer name.

All EMC testing/submissions shall be performed using the most recent operating systems software appropriate for the product (e.g., Windows 7), LiteON Company labeled/manufactured peripherals, the defined test systems (contact EMC Services), and a continuous scrolling 'H' pattern.

6.2.2 Harmonic Current Emissions

IEC 61000-3-2 –Power supplies with input power draw exceeding 600W shall comply with the class A limits for harmonic current emissions in IEC 61000-3-2 when tested under all conditions of end product load. The OEM shall provide LiteON's Agency group with a copy of the test report showing all harmonic current measurements and the calculated limits based on the measured input power for each loading condition.

6.2.3 Voltage Fluctuations Flicker Requirements

IEC 61000-3-3 – The power supply shall comply with the applicable limits for voltage fluctuations and flicker in IEC 61000-33 when tested under all conditions of varying load exhibited by the intended LiteON server for which the power supply is to be used. The OEM shall provide LiteON Agency group with a copy of the test report showing all applicable measurements.

## 6.3 CE MARK REQUIREMENTS

The power supply shall comply with all of the performance requirements for placing the CE Marking on the product in accordance with the EMC Directive [2006/95/EC] with its amendments, and the Low Voltage Directive [2006/95/EC] with its amendments. Specifically, the product shall comply with the following requirements and associated test parameters:

**TABLE 32 – CE MARK REQUIREMENTS AND PARAMETERS**

| REQUIREMENT | PARAMETERS |
|---|---|
| Electrical Product Safety requirements | EN 60950-1 |
| Harmonic distortion compliance requirements | EN 61000-3-2 |
| Line voltage fluctuation and flicker requirements | EN 61000-3-3 |
| EMC emissions compliance requirement | EN 55022 (CISPR 22 - Class B at 10 meters) |
| Immunity compliance requirements | EN 55024 consisting of:<br>• IEC 61000-4-2: 1995 Electrostatic Discharge, [4kV contact, 8kV air discharge]<br>• IEC 61000-4-3: 1995 RF Fields, [3V/m; 80 - 1000 MHz; 80% modulated at distance of 3 meters.<br>• IEC 61000-4-4: 1995 Elec. Fast Transients [± 1kV on AC power port for 1 minute; ±0.5kV on signal/control lines]<br>• IEC 61000-4-5: 1995 Surge, [± 1kV line to line/±2kV line to earth on AC power port;±0.5kV for outdoor cables] |

| | |
|---|---|
| | • IEC 61000-4-6:1996 Conducted RF, [3V; 0.15-80MHz; 80% modulated]<br>• IEC 61000-4-11:1994 Voltage variations, [>95% dip,0.5 period; 30% dip, 25 periods;>95%reduction, 250 periods] |

For the purposes of compliance with EN 55024, the product when tested with the intended system, shall not cause a halt of the operation of software applications (Does not apply to 30% and 95% dips tests). Voltages and currents shall remain within the specified parameters contained elsewhere in this document. Test setups shall be in accordance with EN 55022, namely complete systems with all ports appropriately terminated into a peripheral.

- The manufacturer shall place the CE Mark on the label.
- Manufacturer's Declaration of Conformity - A D of C accompanied by a complete Technical Data file containing all associated Test Reports shall be provided to the LiteON EMC Services and Product Safety groups prior to first revenueable product shipment.

## 6.4 AGENCY ACCEPTANCE TESTING

Acceptance testing will be performed by LiteON. Test samples for acceptance testing will be retained by LiteON. Copies of all submissions documents and resulting approvals will be supplied to LiteON Product Safety and EMC Services representatives prior to first valuable product shipment.

## 6.5 PRODUCTION LINE TESTS

### 6.5.1 Production Line Test Compliance

As part of end product Production Line Tests, LiteON reserves the right to conduct the Hipot and Ground Bond Tests with the associated test parameters as noted below on the Power Supply Module production. Failure to comply with the LiteON end product Hipot or Ground Bond tests when conducted at LiteON is considered unacceptable and a justification for rejection. In addition to meeting the minimum UL/CSA/TUV production line tests, the OEM Power Supply Module manufacturer may opt to change the production parameters provided the OEM accepts responsibility for conformance with the LiteON Production Test parameters.

### 6.5.2 Production Line Hipot Test

One hundred percent (100%) of the OEM Power Supply Module shall comply with the minimum Production Line Hipot (High Potential) Test as noted below. The test shall be applied between the PRIMARY (AC LINE and NEUTRAL) and EARTH GROUND (CHASSIS/INPUT RECEPTACLE GROUND TERMINAL):

**TABLE 33 - PRODUCTION LINE HIPOT**

| PARAMETERS | SETTING |
|---|---|
| VOLTAGE | 2150 Vdc Minimum |
| TRIP CURRENT SENSITIVITY | 600 Microamperes Maximum |
| VOLTAGE RAMP TIME | 500 V/Second ramp Minimum |
| DWELL TIME | 1 Second Minimum |
| BREAKDOWN ARC DETECTION | 10 Microseconds Maximum |

### 6.5.3 Production Line Ground Bond Test

One hundred percent (100%) of the OEM Power Supply Module shall comply with the minimum Production Line Ground Bond Test as noted below. The test shall be applied between the GROUNDED SHEET METAL CHASSIS and the INPUT RECEPTACLE EARTH GROUND TERMINAL.

**TABLE 34 - PRODUCTION GROUND BOND**

| PARAMETERS | SETTING |
|---|---|
| OUTPUT CURRENT | 25 Amperes Minimum |
| OUTPUT VOLTAGE | 2.5 Vac or Vdc Minimum |
| TRIP RESISTANCE SENSITIVITY | 0.1 Ohms Maximum |

## 6.6 AGENCY COMPONENT REQUIREMENTS

6.6.1 Printed Wiring Boards

All printed wiring boards shall be Underwriter Laboratories Inc. Recognized Component rated 94V-1 or less flammable and shall be so marked. The maximum board surface temperature shall not exceed its UL temperature rating under any normal operating condition (130 C). Use of solder build-up on traces as a method of increasing current/energy capacity shall be approved by each of the Agencies identified in Section 6.

6.6.2 Wiring

All internal and external wiring shall be UL Recognized Component Appliance Wiring Material (AVLV2), and CSA Certified "Appliance Wiring Material" (AWM). Primary circuit wire shall be minimum rated 300V, 105°C, while the secondary SELV shall be rated at min. 30V, 80°C.

6.6.3 AC Line Fuse

An AC Line Fuse shall be used. The device shall be provided in a clip fuse holder or provided with "press-on" pigtail leads for soldering to the PWB. The PWB shall be marked with the fuse voltage and current.

6.6.4 AC Receptacle

The Inlet receptacle shall comply with EN 60320 and be Certified, Recognized or approved by CSA, UL, VDE and one of the Nordic Agencies (NEMKO, SEMKO, FIMKO, DEMKO). It shall be rated min. 10A, 250V. Each appliance inlet pin shall be able to withstand a 15 lb. force applied perpendicularly to its axis; the force shall be applied within 1.5 mm of the tip of the pin without breaking.

6.6.5 Voltage Select Switch

If used, the Voltage Select Switch shall be Certified, Recognized, or Approved by CSA, UL, VDE, and one of the NORDIC Agencies (NEMKO, SEMKO, FIMKO, or DEMKO).

6.6.6 Hot Plug Connectors

If the power supply is intended for hot plugging (disconnecting under load), the connector must be approved/tested for this at the max. rated load of the supply. This fact must be noted in the agency test report (e.g. conditions of acceptability).

6.6.7 Enclosure

Any surface of the power supply enclosure that will serve as an external surface of the end product must comply with the mechanical strength tests in 4.2.1, 4.2.4, and 4.2.5 of IEC 60950-1. All openings on the power supply enclosure must comply with the accessibility requirements of 2.1.1.1 of IEC 60950-1. These facts must be noted in the agency test report (e.g. conditions of acceptability).

6.6.8 Plastic Parts

Any plastic parts forming part of the overall assembly shall be considered part of the power supply and shall be covered by the respective agency test reports. Parts external to the overall power supply enclosure shall be flame rated min. HB in accordance with IEC 60950-1. Parts forming part of the overall power supply enclosure shall be flame rated 5V in accordance with IEC 60950-1.

6.6.9 Approved Vendor List

The OEM's Approved Vendor List (AVL) of Critical Components shall be sent to the LiteON Safety Group prior to approval.

6.6.10 Clearances

The typical end product is intended for operation at up to 3000 m above sea level. Unless otherwise specified, the clearances according to section 2.10.3.1 of IEC 60950-1 shall be evaluated for this operating altitude. The end product is intended for use in a pollution degree 2 environment with a mains transient rating of 2500V.

6.6.11 Optocouplers

In the end product application, the measured temperatures of all pri-sec isolating photo-couplers shall not exceed the rated limit for the component when tested under all conditions of allowable room operating ambient temperature. This limit applies during abnormal operation and fault testing of the end product as well. Note – Unless otherwise specified in the component certifications, the default rating for photo-couplers is 100 C. Typical end product abnormal conditions include max load operating with blocked front vents; blocked rear vents and stalled fans.

6.6.12 Electrical Rating

In most cases, the marked electrical rating of the power supply will be a significant factor in the electrical rating of the end product. Where multiple suppliers exist for a specific model power supply, the electrical rating must be the same for all models.

The following values for the electrical rating on the main label shall be:

- 100-240V ~ 50-60 Hz 9-4.5A

Any exceptions to this must be verified and approved by the product safety certification engineers responsible for the end product.

## 7. RELIABILITY

### 7.1 DEMONSTRATED MEAN TIME BETWEEN FAILURES

The power supply shall have a demonstrated MTBF of greater than 500,000 hours, when operated under the following conditions:

7.1.1 Input Voltage

120 VAC.

7.1.2 Output Load

Rated full load.

7.1.3 Ambient Temperature

50 C maximum ambient temperature to the power supply.

### 7.2 LIFE EXPECTANCY

The power supply shall have a field failure rate of less than 1% per 4000 hrs within the first 100,000 hours of operation.

### 7.3 SEMICONDUCTOR TEMPERATURE

Maximum semiconductor junction temperature shall not exceed 125 C or 25 C below the rated vendor's maximum rating whichever is less under any specified operation.

## 8. COMPONENT REQUIREMENTS

### 8.1 PRINTED WIRING BOARDS

8.1.1 Design and Fabrication of PCBs

The power supply printed circuit board shall meet the requirements specified within LiteON. The PCB layout and design shall meet the requirements specified within LiteON Layout Guideline. Electric field intensity between adjacent tracks shall not exceed 25V/0.001in.

8.1.2 Solder Mask

Solder mask shall be provided on all primary and secondary traces with spacing less than 2 mm.

8.1.3 Contamination

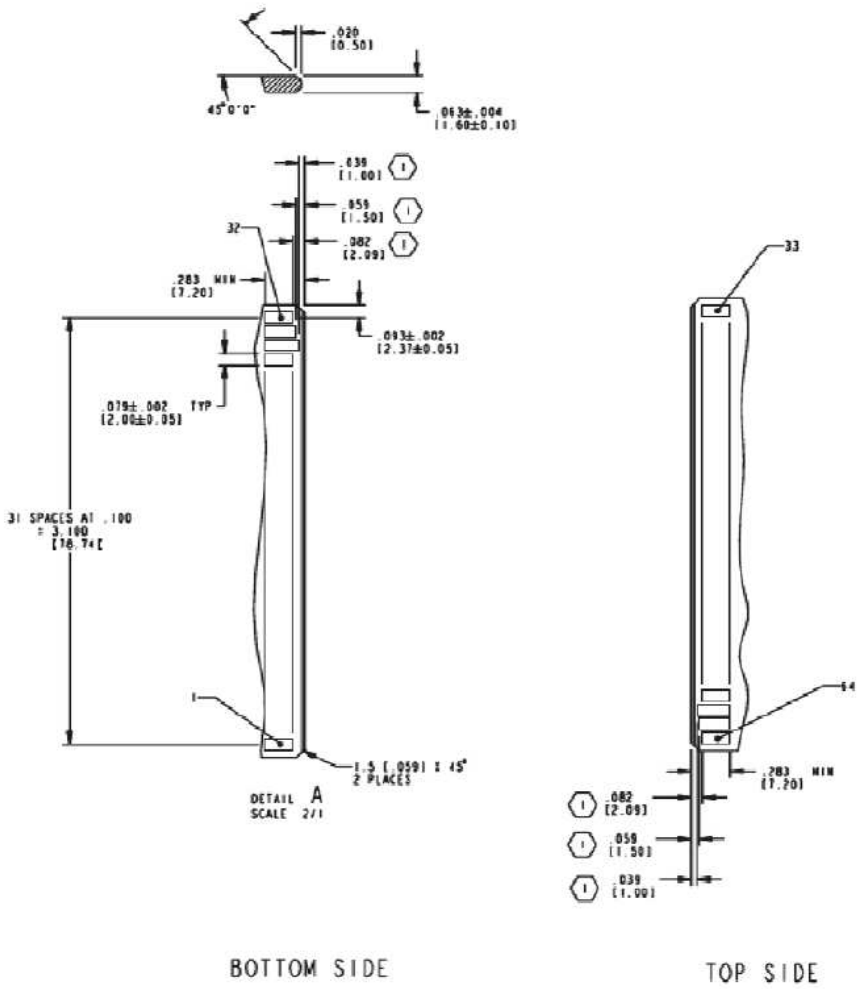
Bare PCB testing shall use Ion Chromatography to determine the halide analysis of residues on PC boards, using high temp (180 F for 1 hour) soak in 18.2 M water. Those limits are 5 ug/in2 chloride and 10 ug/in2 bromide.

PCA from no-clean process shall use Ion Chromatography to determine the type and concentration of acids in flux residues on PC boards after assembly process and environmental exposures, using high temp (180 F for 1 hour) soak in 18.2 M water. Those limits are 5 ug/in2 chloride and 10 ug/in2 bromide. Additionally, the no-clean processes meet the requirements specified within LiteON.

8.1.4 Card Edge and Gold Finger Contacts

Power supply main board shall extend beyond power supply case and form card edge finger connections to mate with a 64 position (32 positions, each side). PCB card edge shall incorporate Gold plated contact fingers. The plating requirements are as defined within LiteON, which specifies a minimum of 30 micro-inches of Gold over a minimum of 100 micro-inches of Nickel. Card edge and fingers shall be free of contaminants such as solder flux or solder, and shall be free of voids or defects in the plating. Critical dimensions for card edge are shown below. *Note: Specified gold finger lengths can be used at the vendor option along the edge connector.*

**FIGURE 9- CARD EDGE CONNECTOR**




8.1.5 Safety

All printed wiring boards shall be Underwriter Laboratories, Inc. Recognized Component rated 94V-1 or less flammable and shall be so marked. The maximum board surface temperature shall not exceed its UL rating under any normal operating condition.

## 8.2 WIRING

All internal and external wiring shall be rated minimum 105 C and UL Recognized Component Appliance Wiring Material (AVLV2), and CSA certified “Appliance Wiring Material” (AWM). Wire shall be rated minimum 300 V.

## 8.3 COMPONENT QUALIFICATION

All components shall be qualified to mutually agreed upon specifications as to their acceptability. No changes can occur without prior written permission from LiteON Company. All requests for changes must be evaluated and approved in writing by LiteON Company. Such requests should be forwarded to the designated LiteON procurement engineer.

## 9. QUALITY ASSURANCE AND RELIABILITY PROVISIONS

### 9.1 RESPONSIBILITY FOR INSPECTION

Unless otherwise specified in the contract or purchase order, the supplier shall be responsible for performing inspections and tests that ensure the product meets all the requirements of this document A Quality Plan and Process Management Plan will be completed and agreed on between the supplier and LiteON prior to release of product to LiteON procurement.

### 9.2 LOT ACCEPTANCE

Lots furnished to this specification shall be capable of passing a sampling inspection plan as defined by LiteON Procurement Engineering and approved by the supplier. Failing lots may be returned to the supplier or subject to other dispositions.

Supplier will perform a LiteON acceptable Out of Box Audit (OBA) inspection on all LiteON products, as they are ready to ship. The audit will be performed per an agreed on inspection plan and may include visual, packing, packaging, mechanical and dimensional inspections, and functional testing. Supplier shall notify LiteON within twenty-four hours of any OBA failure. Data and results of this OBA shall be provided to LiteON at regular agreed upon intervals.

### 9.3 CHANGE NOTIFICATION

Deviations from this specification are not permitted without specific written authorization from LiteON Procurement.

The Supplier must notify LiteON of any significant changes to the manufacturing process, manufacturing site, product, test or critical components at least 60 days prior to the implementation of the change.

Significant changes include but are not limited to the following:

- Changes affecting Form, Fit, or Functionality of the product
- Changes in the manufacturing site/location
- Changes in supplier's critical assembly/test process
- Changes in critical components or suppliers of critical components
- Changes for the purpose of continuous improvement and achieving quality goals

### 9.4 PRODUCT RELIABILITY

#### 9.4.1 MTBF

The calculated and/or demonstrated MTBF of the product shall be provided to LiteON Design and Procurement Engineering prior to final product approval. The product shall function for minimum 8,760 power-on hours per year and the unit shall have a service life of five years. MTBF should be calculated using Telcordia SR332 (Bellcore TR332) method 1 case 3 (assuming Ground Benign controlled environment and 25 deg. C.)

#### 9.4.2 HALT/HASS

Supplier shall perform a LiteON approved HALT as reference in document EN896-00 and HASA-POS per document EN896-01 on the product and provide test results prior to final product approval. LiteON Design and Procurement Engineering must approve any changes or modifications to the test protocol, product or the manufacturing process following the final HALT test.

LiteON may require additional HALT or HASA testing depending on any product or manufacturing process changes or modifications.

9.4.3 Sustaining Reliability Plan

The supplier shall have a LiteON approved Ongoing Reliability Test (ORT) and mutually agreed upon ongoing Highly Accelerated Stress Audit (HASA) based on EN896-01 in place prior to product release to LiteON Procurement. The supplier shall perform an Ongoing Reliability Test (ORT) and mutually agreed upon ongoing Highly Accelerated Stress Audit (HASA) based on EN896-01 throughout the life of the product. The ORT plan and calculation format shall be reviewed and approved by LiteON Reliability Engineering prior to first shipment of production level product. Data and results of this test shall be provided to LiteON at regular agreed upon intervals. LiteON Reliability Engineering reserves the right, at their discretion, to conduct tests it deems necessary to verify the reliability of the product.

9.4.4 Annualized Return Rate and Annualized Failure Rate (ARR and AFR)

**9.4.4.1 Data**

ARR and AFR data shall be provided to LiteON Procurement Engineering at regular agreed upon intervals.

**9.4.4.2 ARR/ARF Calculations**

ARR = Number of returned LiteON units in warranty / total number units shipped to LiteON in past 36 months x 100 x 12

AFR = Number of returned LiteON units in warranty minus number of NDF/ total number units shipped to LiteON in past 36 months x 100 x 12 10.

**9.4.4.3 ARR/AFR Goals**

LiteON Procurement Engineering at the start of a program will provide ARR/AFR goals. Goals may be adjusted or modified on a regular basis, typically quarterly.

**9.4.4.4 ARR/AFR Goals Exceeded**

If the ARR/AFR rate exceeds the goal limits the supplier must inform LiteON within two (2) working days. A written corrective action plan (8D) must be submitted to LiteON within ten (10) working days. LiteON reserves the option to stop or continue production until containment and/or corrective action is in place. The above requirements for corrective action also apply if independent LiteON calculations, based upon actual quantities shipped and returned, show that the ARR/AFR have been exceeded. In addition if LiteON receives data that indicates field failures have significantly increased, even though ARR or AFR rates do not reflect that rise, LiteON still reserves the right to stop production until containment and/or corrective action is in place.

In the event the ARR/AFR goals are exceeded LiteON reserves the right to implement a field recall of product. During a recall, production will stop until containment and/or corrective action is in place. Any cost incurred as a result of the recall will be obligated per the contractual agreement.

## 10. MECHANICAL OVERVIEW

The mechanical design shall meet LiteON requirements specified within this section.

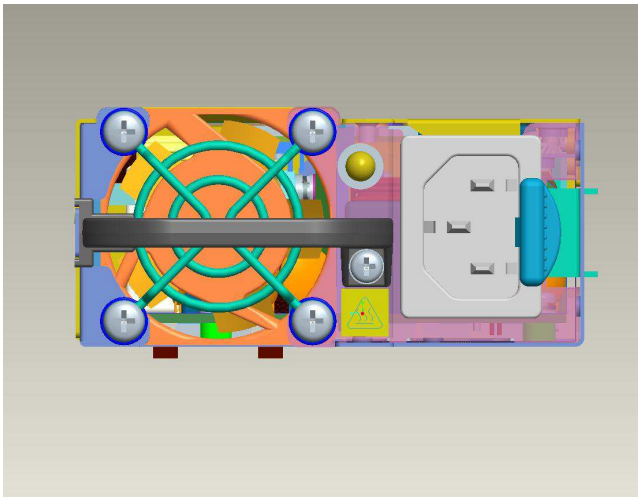
### 10.1 DIMENSIONS

The mechanical configuration of the power supply, with critical dimensions for fit within the end application, is shown in Figure 11. PS shall measure 1.515” (H) x 3.4” (W) x 7.5” (L) excluding card edge connector. Height of chassis shall be 1.515” at all places except fan location where the height shall be 1.595”. Refer to the mechanical drawing.

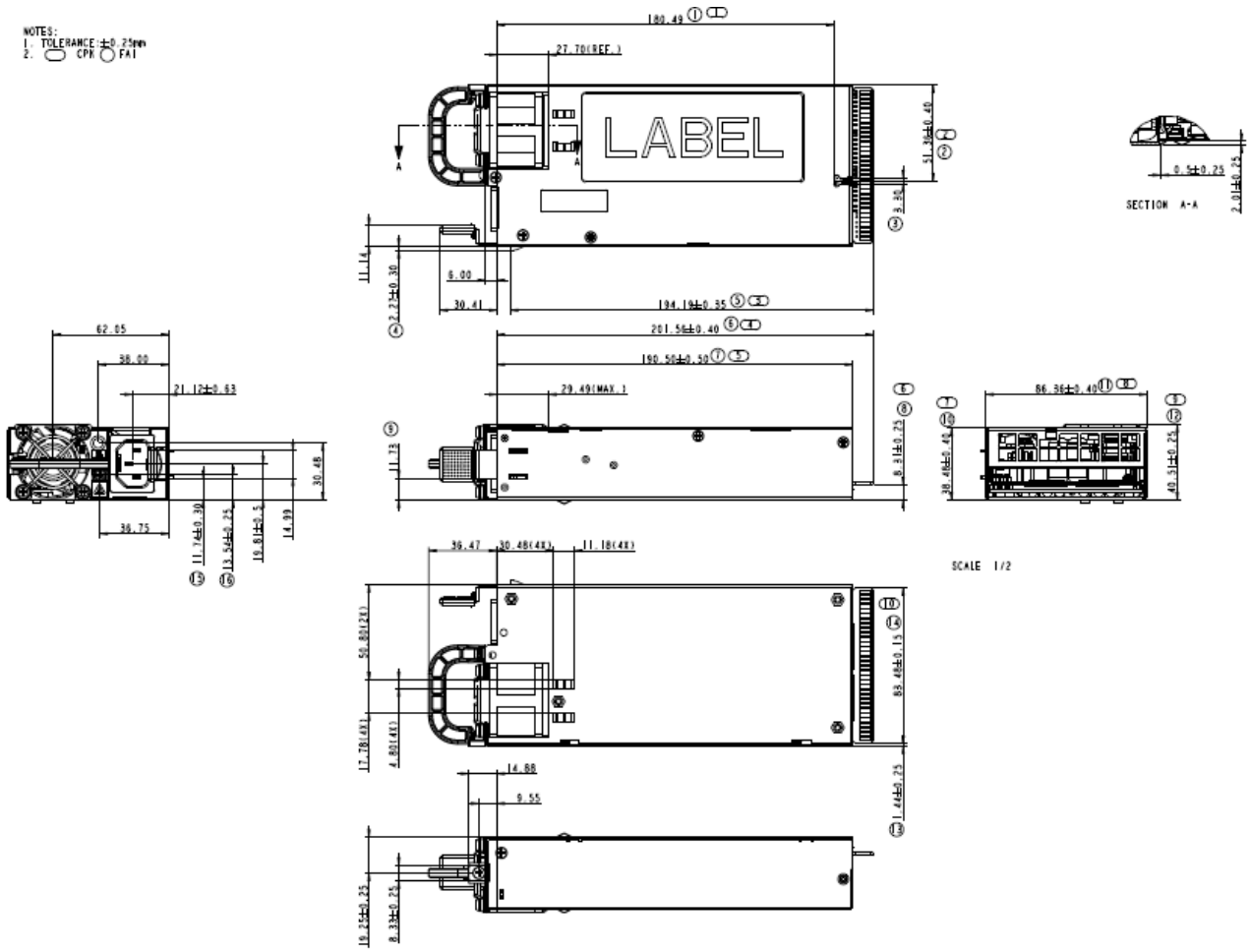
### 10.2 FRONT VIEW

The following figure shows the general placement of the fan labels and fan grill.

**FIGURE 10 - POWER SUPPLY FAN ORIENTATION**



## FIGURE 11 - MECHANICAL




| | | | | |
|---|---|---|---|---|
| Lite-On Technology Corp. | SIZE A | PS-2751-7H-LF<br>LiteON 750W | | REV D |
| | DRAWN | SCALE 1/1 | SHEET 49 OF 112 | |

### 10.3 AC INLET, EXTERIOR FACE

The AC inlet shall be located on the exterior face of the power supply. This is the face of the power supply that will be accessible when the power supply is installed in a system. Figure 11 shows the location of this connector.

### 10.4 LED INDICATOR

There shall be a green POWER LED (PWR) on the AC inlet side of the power supply that will behave per firmware as defined in section 12. When lit, the LED indicates either of the following conditions are true:

- Valid AC is applied, 12VSB is within regulation limits, and 12V output is within regulation limits.
- Valid AC is applied to the PS and 12VSB is within regulation limits (for blade systems only)

The LED and its location shall meet ESD requirements required for the power supply. The LED shall be securely mounted in such a way that incidental pressure on the LED will not cause it to become displaced.

### 10.5 CHASSIS AND CHASSIS FINISH

Power supply enclosure chassis shall be hot-dipped galvanized steel to match system chassis and shall have sufficient metal thickness to meet safety agency requirements per Section 6.6.7.

### 10.6 POWER SUPPLY FAN, LOCATION AND ORIENTATION

Power supply shall contain one internal 40mm high-speed fan sufficient to cool the power supply and provide some additional system cooling and ventilation. The fan shall be located as shown in Figure 10. The fan shall be oriented to intake system air on the power supply card edge end (output connector) and exhaust air out of the exterior face (AC inlet) end.

### 10.7 SYSTEM AIRFLOW GUIDANCE

The end system shall provide adequate airflow to the power supply. Recommended air flow is a minimum of 10CFM with no more than 1" pressure drop.

### 10.8 ACOUSTIC REQUIREMENT

Fan noise as measured from one meter distance from the power supply shall meet the limits defined in Table 35.

**TABLE 35 –ACOUSTIC LIMITS**

| Load Condition | PS Ambient Temperature [°C] | Typical [dBA] | Maximum [dBA] |
|---|---|---|---|
| Full Output Rated Load | 25 | 55 | 60 |
| | 35 | 57 | 62 |
| | 50 | 61 | 65 |
| Half Output Rated Load | 25 | 42 | 45 |
| | 35 | 50 | 55 |
| | 50 | 57 | 67 |

The test setup shall be as follows: The PS is a desktop module with bystander locations only. The PS is to be placed on a table 26 to 34 inches high with the position of four- (4) bystander microphones. The microphones will be one meter away, centered on each side, 1.5 meters high, as measured from the floor, and placed at a 30 down angle. The A-weighted (100 -10 kHz) sound pressure must be measured at the four- (4) bystander positions. Sound pressure is a measurement of the total noise at the specified microphone location in the room.

## 10.9 MATERIALS

All polymeric parts within the enclosure shall be molded from Underwriters Laboratories, Inc. “Recognized” QMFZ2 polymeric material minimally rated 94 V-2.

## 10.10 WEIGHT

Completed power supply assembly shall weigh 3 pounds maximum (For reference only).

## 10.11 PACKAGING AND LABELING

Packing shall be sufficient to protect the product against loss or damage during shipment from the manufacturer to the destination. The shipping, packaging, and labeling shall meet the requirements of LiteON. LiteON defines the preferred shipping label requirements.

The method of shipment shall be agreed upon between sender and recipient. The product shall be clearly identified and packed according to prevailing regulations. It is the responsibility of the shipper to take all reasonable precautions to ensure the product arrives undamaged and on time.

## 10.12 PALLETIZATION AND SHIPPING

A 42” x 48” pallet will be used. A 40” x 48” pallet will be used for Europe. Palletization, labeling and shipping requirements shall be in accordance to LiteON.

## 11. FRU SPECIFICATIONS

Power supply unit shall contain internal EEPROM device accessible through I2C communication. Unit FRU data shall be accessible with the input AC not connected as long as the unit is connected to system backplane which is providing 12VSB power. The following tables describe the FRU data to be stored in power supply EEPROM by vendor.

### 11.1 FRU -DATE

**Table 36 - POWER SUPPLY FRU CONTENTS:**

| OFFSET | VALUE | DEFINITION |
|---|---|---|
| (BYTES) | (DECIMAL) | (REMARKS) |
| 0 to 7 | | **Common Header, 8 Bytes** |
| 0 to 7 | 001 | Format Version Number |
| | 000 | Internal Use Area Offset |
| | 000 | Chassis Info Area Offset |
| | 001 | Board Info Area Offset |
| | 005 | Product Info Area Offset |
| | 014 | Multi Record Area Offset |
| | 000 | PAD (reserved) Default value is 0. |
| | 235 | Zero Check Sum |
| 8 to 39 | | **Board Info Area, 32 Bytes** |
| 8 | 001 | **Format Version Number** |
| 9 | 004 | **Board Info Area Length** |
| 10 | 025 | **Language (English)** |
| 11 to 13 | **032** | Number of minutes from 1/1/96 to build date. LSB first (little endian). Shall be calculated at the time of manufacturing. Default date is 05/28/07. Default date shall indicate that the Mfg. date was not programmed correctly by the power supply vendor. |
| | **132** | |
| | **091** | |
| 14 | 192 | Board Manufacture type/length [8-bit ASCII / 00h] |
| 15 | 192 | Board Product Name type/length [8-bit ASCII /00h] |
| 16 | 192 | Board Serial Number type/length [8-bit ASCII / 00h] |
| 17 | 202 | Product Spare Part Number type/length [8-bit ASCII/0Ah] |
| 18 to 27 | 057 | Specified 10-Byte Sequence<br>Product Spare Part Number: “999999-001”<br>In Decimal = 057, 057, 057, 057, 057, 057, 045, 048, 048, 049<br>In Hex = 39H, 39H, 39H, 39H, 39H, 39H, 2DH, 30H, 30H, 31H |
| | 057 | |
| | 057 | |
| | 057 | |
| | 057 | |
| | 057 | |
| | 045 | |
| | 048 | |
| | 048 | |
| | 049 | |
| 28 | 200 | FRU File ID type/length [8-bit ASCII / 8] (Used as FRU version) |
| 29 to 36 | 048 | FRU File ID: “04/21/11" |

## Table 36 - POWER SUPPLY FRU CONTENTS:

| OFFSET | VALUE | DEFINITION |
|---|---|---|
| (BYTES) | (DECIMAL) | (REMARKS) |
| | 052 | |
| | 047 | |
| | 050 | |
| | 049 | |
| | 047 | |
| | 049 | |
| | 049 | |
| 37 | 193 | End Tag |
| 38 | 000 | PAD |
| 39 | 181 | Zero checksum<br>Shall be calculated at the time of manufacturing.<br>Default value is 209 or D3h. Default value shall indicate that the Mfg.<br>Date was not programmed correctly by the power supply vendor. |
| 40 to 111 | | **Product Info Area, 72 Bytes** |
| 40 | 001 | **Product Info Area Format version** |
| 41 | 009 | **Product Info Area Length** in multiples of 8 Bytes |
| 42 | 025 | **Language** (English) |
| 43 | 197 | **Manufacturer Name** Type/Length (0C5H) = Type “ASCII+LATIN1” 5 Bytes. |
| | 076 | Manufacturer Name 5 byte sequence |
| | 084 | Company Name: LTEON |
| 44 to 48 | 069 | In Decimal = 076, 084, 069, 079, 078 |
| | 079 | In Hex = 4CH, 54H, 45H, 4FH, 4EH |
| | 078 | Vendor specific information |
| 49 | 218 | **Product Name** Type/Length (DAH) = Type “ASCII+LATIN1” 26 Bytes. |
| | 076 | |
| | 084 | |
| | 069 | |
| | 079 | |
| | 078 | |
| | 032 | |
| | 055 | |
| | 053 | |
| | 048 | |
| | 087 | |
| | 032 | 26 Byte sequence |
| | 080 | Product Name : “LTEON 750W PLATINUM PS “ |
| 50 to 75 | 076 | In Decimal = 076, 084, 069, 079, 078, 032, 055, 053, 048, 087, 032, 080, 076, 065, 084, 073, 078, 085, 077, 032, 080, 083, 032, 032, 032, 032 |
| | 065 | In Hex = 4CH, 54H, 45H, 4FH, 4EH, 20H, 37H, 35H, 30H, 57H, 20H, 50H, 4CH, 41H, 54H, 49H, 4EH, 55H, 4DH, 20H, 50H, 53H, 20H, 20H, 20H, 20H |
| | 084 | |
| | 073 | |
| | 078 | |
| | 085 | |
| | 077 | |
| | 032 | |
| | 080 | |
| | 083 | |
| | 032 | |
| | 032 | |
| | 032 | |

## Table 36 - POWER SUPPLY FRU CONTENTS:

| OFFSET | VALUE | DEFINITION |
|---|---|---|
| (BYTES) | (DECIMAL) | (REMARKS) |
| | 032 | |
| 76 | 202 | **Product Option Kit Number** Type/Length (0CAH) = Type “ASCII+LATIN1” 10 Bytes. |
| 77 to 86 | 057<br>057<br>057<br>057<br>057<br>057<br>045<br>066<br>050<br>049 | Specified 10-Byte Sequence<br>Product Option Kit Number: “999999-B21”<br>In Decimal = 057, 057, 057, 057, 057, 057, 045, 066, 050, 049<br>In Hex = 39H, 39H, 39H, 39H, 39H, 39H, 2DH, 42H, 32H, 31H |
| 87 | 194 | **Supplier Revision Counter -** Type/Length (0C2H) = Type “ASCII+LATIN1” 2 Bytes.<br>Production level start at “01”. |
| 88 to 89 | 048<br>049 | Specified 2-Byte Sequence<br>Production level start at “01”<br>In Decimal = 048, 049<br>In Hex = 30H, 31H |
| 90 | 206 | **Product Serial Number** Type/Length (0CEH) = Type “ASCII+LATIN1”<br>14 Bytes. |
| 91 | 054 | Commodity Code, “6” for Power Supply<br>In Decimal = 054<br>In Hex = 36H |
| 92 to 95 | 088<br>088<br>088<br>088 | AAAA: Assembly Code,<br>“XXXX”<br>In Decimal = 088,088, 088, 088<br>In Hex = 58H,58H, 58H, 58H<br>Vendor specific information |
| 96 to 97 | 048<br>065 | RR: Revision Level,<br>Specified 2-Byte Sequence<br>Production level start at “0A”<br>In Decimal = 048, 065<br>In Hex = 30H, 41H |
| 98 to 99 | **XXX**<br>**XXX** | **YY: Year of Mfg.**<br>“13”→2013, “14”→2014<br>2 Byte Sequence for week Code<br>Shall be calculated at the time of manufacturing. |
| 100 to 101 | **XXX**<br>**XXX** | **WW: Week of Mfg.**<br>2 Byte Sequence for week Code<br>Shall be calculated at the time of manufacturing. |
| 102 to 104 | **XXX**<br>**XXX**<br>**XXX** | **Unique Sequence Identifier**<br>Specified 3 Bytes Sequence for Serial Number<br>Shall be added at the time of manufacturing. |
| 105 | 000 | **Asset Tag** Default Value is 0 |
| 106 | 000 | **FRU File ID type/Length [not used]** |
| 107 | 193 | **End Tag**<br>In Decimal: 193<br>In Hex: 0C1H |
| 108 to 110 | 000<br>000 | PAD |

## Table 36 - POWER SUPPLY FRU CONTENTS:

| OFFSET | VALUE | DEFINITION |
|---|---|---|
| (BYTES) | (DECIMAL) | (REMARKS) |
| | 000 | |
| 111 | **XXX** | Zero Check Sum Shall be calculated at the time of manufacturing. |
| 112 to 199 | | **Multi Record Area, 88 Bytes** |
| 112 to 116 | | Power Supply Record Header |
| 112 to116 | 000 | Record type = 00 for Power supply |
| | 002 | End of List /Record Format Version Number |
| | 024 | Record Length of Power Supply Record |
| | **018** | Record CHECKSUM of Power Supply Record (Zero CHECKSUM) |
| | **212** | Header CHECKSUM of Power Supply Record Header (Zero CHECKSUM) |
| 117 to 140 | | **Power Supply Record** |
| 117 to 118 | 238 | Overall Capacity of the Power Supply, 750W = 02EEH<br>2 Bytes Sequence<br>In Decimal = 238, 002<br>In Hex =EEH, 02H |
| | 002 | |
| 119 to 120 | 132 | Peak VA, 900W = 0384H<br>2 Bytes Sequence<br>In Decimal = 132, 003<br>In Hex = 84H, 03H |
| | 003 | |
| 121 | 030 | Inrush Current, A<br>In Decimal = 030<br>In Hex = 1EH |
| 122 | 005 | Inrush Interval, 5ms<br>In Decimal = 005<br>In Hex = 05H |
| 123 to 124 | 040 | Low End Input Voltage Range 1(10mV), 9000= 2328H<br>2 Bytes Sequence<br>In Decimal = 040, 035<br>In Hex = 28H, 23H |
| | 035 | |
| 125 to 126 | 144 | High End Input Voltage Range 1(10mV), 13200= 3390H<br>2 Bytes Sequence<br>In Decimal = 144, 051<br>In Hex = 90H, 33H |
| | 051 | |
| 127 to 128 | 080 | Low End Input Voltage Range 2(10mV), 18000= 4650H<br>2 Bytes Sequence<br>In Decimal = 080, 070<br>In Hex = 50H, 46H |
| | 070 | |
| 129 to 130 | 032 | High End Input Voltage Range 2(10mV), 26400= 6720H<br>2 Bytes Sequence<br>In Decimal = 032, 103<br>In Hex = 20H, 67H |
| | 103 | |
| 131 | 047 | Low End Input Frequency Range, 47Hz = 2FH |
| 132 | 063 | High End Input Frequency Range, 63Hz = 3FH |
| 133 | 010 | AC Dropout Tolerance in ms, 10mS= 0AH |
| 134 | 026 | Binary Flags, 1 indicates function supported and a 0 indicates function not supported.<br>Bits 7-5: RESERVED, WRITE AS 000B<br>Bit 4: Tachometer Pulses Per Rotation / Predictive Fail Polarity BIT = 1<br>Bit 3: Hot Swap / Redundancy Support BIT = 1<br>Bit 2: Autos witch Support BIT = 0<br>Bit 1: Power Factor Correction Support BIT = 1<br>Bit 0: Predictive Fail Support BIT = 0 |

## Table 36 - POWER SUPPLY FRU CONTENTS:

| OFFSET | VALUE | DEFINITION |
|---|---|---|
| (BYTES) | (DECIMAL) | (REMARKS) |
| | | In Decimal = 026<br>In Hex = 1AH |
| 135 to 136 | 132<br>019 | Peak Wattage Capacity and Holdup Time, **900W = 0384H**;<br>1 hundreds of milliseconds = 01H<br>Bits 15-12: Holdup Time in Seconds 01 *100 msec = 01H<br>Bits 11- 0: Peak Capacity in Watts **900W = 0384H**<br>2 Bytes sequence:<br>In Decimal: 132, 019<br>In Hex: **84H, 13H** |
| 137 to 139 | 000<br>000<br>000 | **Combined Wattage,** None.<br>Byte 1: 000 = 00H<br>Bits 7-4: 0000B<br>Bits 3-0: 0000B<br>Byte 2 and Byte 3: 00H, 00H<br>3 Bytes Sequence<br>In Decimal = 000, 000, 000<br>In Hex = 00H, 00H, 00H |
| 140 | 000 | **Predictive Fail Tachometer Lower Threshold,** Not Applicable.<br>Predictive Failure is not Supported. |
| 141 to 145 | | **12V DC Output Record Header** |
| 141 to 145 | 001 | Record type = 01 for DC Output Record |
| | 002 | End of List /Record Format Version Number for 12V DC Output Record |
| | 013 | Record Length of 12V DC Output Record |
| | 083 | Record CHECKSUM of 12V DC Output Record (Zero CHECKSUM) |
| | 157 | Header CHECKSUM of 12V DC Output Record Header (Zero CHECKSUM) |
| 146 to 158 | | **12V Output Record** |
| 146 | 001 | **Output Information,** 001 = 01H<br>Bit 7: Standby Information = 0B<br>Bits 6-4: Reserved, Write as 000B<br>Bits 3-0: Output Number10 = 001B<br>In Decimal: 001<br>In Hex: 01H |
| 147 to 148 | 206<br>004 | Nominal Voltage (10mV), 1230 = 04CEH<br>2 Bytes Sequence<br>In Decimal: 206, 004<br>In Hex: CEH, 04H |
| 149 to 150 | 136<br>004 | Maximum Negative Voltage Deviation (10mV), 1160 = 0488H<br>2 Bytes Sequence<br>In Decimal: 136, 004<br>In Hex: 88H, 04H |
| 151 to 152 | 236<br>004 | Maximum Positive Voltage Deviation (10mV), 1260 = 04ECH<br>2 Bytes Sequence<br>In Decimal: 236, 004<br>In Hex: ECH, 04H |
| 153 to 154 | 120<br>000 | Ripple and Noise pk-pk 10Hz to 30 MHz (mV), 120 = 0078H<br>2 Bytes Sequence<br>In Decimal: 120, 000<br>In Hex: 78H, 00H |
| 155 to 156 | 100 | Minimum Current Draw (10mA; 1/10 IPMI spec value), 100 = 0064H |

## Table 36 - POWER SUPPLY FRU CONTENTS:

| OFFSET | VALUE | DEFINITION |
|---|---|---|
| (BYTES) | (DECIMAL) | (REMARKS) |
| | 000 | 2 Bytes Sequence<br>In Decimal: 100, 000<br>In Hex: 64H, 00H |
| 157 to 158 | 106<br>024 | Maximum Current Draw (10mA; 1/10 IPMI spec value), 6250 = 1868H<br>2 Bytes Sequence<br>In Decimal: 106, 024<br>In Hex: 6AH, 18H |
| 159 to 163 | | **12Vsb Output Record Header** |
| 159 to 163 | 001 | Record type = 01 for DC Output Record |
| | 002 | End of List /Record Format Version Number for 12Vsb Output Record |
| | 013 | Record Length of 12Vsb Output Record |
| | **239** | Record CHECKSUM of 12Vsb Output Record (Zero CHECKSUM) |
| | **001** | Header CHECKSUM of 12Vsb Output Record Header (Zero CHECKSUM) |
| 164 to 176 | | **12Vsb Output Record** |
| 164 | 130 | **Output Information,** 130 = 82H<br>Bit 7: Standby Information = 1B<br>Bits 6-4: Reserved, Write as 000B<br>Bits 3-0: Output Number 2 = 010B |
| 165 to 166 | 176<br>004 | Nominal Voltage (10mV), 1200 = 04B0H<br>2 Bytes Sequence<br>In Decimal: 176, 004<br>In Hex: B0H, 04H |
| 167 to 168 | 056<br>004 | Maximum Negative Voltage Deviation (10mV), 1080 = 0438H<br>2 Bytes Sequence<br>In Decimal: 056, 004<br>In Hex: 38H, 04H |
| 169 to 170 | 040<br>005 | Maximum Positive Voltage Deviation (10mV), 1320 = 0528H<br>2 Bytes Sequence<br>In Decimal: 040, 005<br>In Hex: 28H, 05H |
| 171 to 172 | 120<br>000 | Ripple and Noise pk-pk 10Hz to 30 MHz (mV), 120 = 0078H<br>2 Bytes Sequence<br>In Decimal: 120, 000<br>In Hex: 78H, 00H |
| 173 to 174 | 000<br>000 | Minimum Current Draw (10mA; 1/10 IPMI spec value), 0 = 0000H<br>2 Bytes Sequence<br>In Decimal: 000, 000<br>In Hex: 00H, 00H |
| 175 to 176 | 250<br>000 | Maximum Current Draw (10mA; 1/10 IPMI spec value), 250 = 00FAH<br>2 Bytes Sequence<br>In Decimal: 250, 000<br>In Hex: FAH, 00H |
| 177 to 181 | | **OEM Record Header** |
| 177 to 181 | 208 | Record type = 208 for PS OEM Record |
| | 130 | End of List /Record Format Version Number for OEM Record |
| | 018 | Record Length of OEM Record |
| | 095 | Record CHECKSUM of OEM Record (Zero CHECKSUM) |
| | 061 | Header CHECKSUM of OEM Record Header (Zero CHECKSUM) |

## Table 36 - POWER SUPPLY FRU CONTENTS:

| OFFSET | VALUE | DEFINITION |
|---|---|---|
| (BYTES) | (DECIMAL) | (REMARKS) |
| 182 to 199 | | **OEM Record** |
| 182 to 184 | 011<br>000<br>000 | OEM ID, ID is 11 (LSB first)<br>3 Bytes Sequence<br>In Decimal: 011, 000, 000<br>In Hex: 0BH, 00H, 00H |
| 185 | 003 | **Multi Record Sub-Type:** 03<br>Power Supply Low Line Characteristics, PS feature Set, and PS Identifier. |
| 186 to 187 | 238<br>002 | Low Line Overall Capacity of the Power Supply, 750W =02EEH<br>2 Bytes Sequence<br>In Decimal = 238, 002<br>In Hex = EEH, 02H |
| 188 to 189 | 132<br>019 | Low Line Peak Wattage Capacity and Holdup Time, 900W = 0384H;<br>1 hundreds of milliseconds = 01H<br>Bits 15-12: Holdup Time in Seconds 1 *100 msec = 01H<br>Bits 11- 0: Peak Capacity in Watts 960 = 0383H<br>2 Bytes sequence:<br>In Decimal: 132, 019<br>In Hex: 84H, 13H |
| 190 | 128 | PS Feature Class: 128<br>In Decimal: 128<br>In Hex: 80H |
| 191 | 141 | PS Identifier:<br>Input (Bit 7): 1b ( 0b for DC input, 1b for AC input)<br>PS ID (Bits 6 - 0): 0001101b<br>In Decimal: 141<br>In Hex: 8DH |
| 192 to 197 | 000<br>000<br>000<br>000<br>000<br>000 | Reserved. Default Value is 0. |
| 198 to 199 | 000<br>000 | Reserved. Default Value is 0. |
| 200 to 204 | | **PS Diagnostic Record Header** |
| 200 to 204 | 208 | Record type = 208 for PS Diagnostic Record |
| | 002 | End of List /Record Format Version Number for PS Diagnostic Record |
| | 051 | Record Length of PS Diagnostic Record |
| | **176** | Record CHECKSUM of PS Diagnostic Record (Zero CHECKSUM) |
| | **075** | Header CHECKSUM of PS Diagnostic Record Header (Zero CHECKSUM) |
| 205 to 255 | | **PS Diagnostic Record** |
| 205 to 208 | 000<br>000<br>000<br>000 | ID Number |
| 209 to 224 | 000<br>000<br>000 | Serial Number |

## Table 36 - POWER SUPPLY FRU CONTENTS:

| OFFSET | VALUE | DEFINITION |
|---|---|---|
| (BYTES) | (DECIMAL) | (REMARKS) |
| | 000 | |
| | 000 | |
| | 000 | |
| | 000 | |
| | 000 | |
| | 000 | |
| | 000 | |
| | 000 | |
| | 000 | |
| | 000 | |
| | 000 | |
| | 000 | |
| | 000 | |
| 225 | 000 | Total Runtime LSB |
| 226 | 000 | Total Runtime Byte #2 |
| 227 | 000 | Total Runtime MSB |
| 228 | 000 | PS Status LSB |
| 229 | 000 | PS Status MSB |
| 230 | 000 | Shutdown Event LSB |
| 231 | 000 | Shutdown Event MSB |
| 232 | 000 | Warning Event LSB |
| 233 | 000 | Warning Event MSB |
| 234 | 000 | Input Voltage LSB |
| 235 | 000 | Input Voltage MSB |
| 236 | 000 | Input Current LSB |
| 237 | 000 | Input Current MSB |
| 238 | 000 | Output Voltage LSB |
| 239 | 000 | Output Voltage MSB |
| 240 | 000 | Output Current LSB |
| 241 | 000 | Output Current MSB |
| 242 | 000 | T1 Temperature LSB |
| 243 | 000 | T1 Temperature MSB |
| 244 | 000 | T2 Temperature LSB |
| 245 | 000 | T2 Temperature MSB |
| 246 | 000 | F1 Speed LSB |
| 247 | 000 | F1 Speed MSB |
| 248 | 000 | Peak Input Current LSB |
| 249 | 000 | Peak Input Current MSB |
| 250 | 000 | Peak Output Current LSB |
| 251 | 000 | Peak Output Current MSB |
| 252 | 000 | PS Control LSB |
| 253 | 000 | PS Control MSB |
| 254 | 000 | PAD |
| 255 | 080 | ASCII "P" = Programmed at factory |

## 12. FIRMWARE SPECIFICATIONS

This section contains power supply to system interface protocol, control, monitoring and reporting requirements of power supply operation through I2C data and I2C clock signals.

Power supply design shall comply with the requirements of communication, monitoring, reporting and control specifications in the document.

### 12.1 HARDWARE / FIRMWARE INTERFACE

#### 12.1.1 I2C & FRU

The power supply shall include a microcontroller (uC) for power monitoring functionality, a 256 bytes EEPROM for Event Log, and a second 256 bytes EEPROM for FRU. The power supply can use an EEPROM internal to the microcontroller for Event Log but it must use an external EEPROM device for FRU. Both the microcontroller and the FRU EEPROM shall use an I2C bus to communicate with the system. In the absence of an EEPROM internal to the microcontroller the power supply can use an external EEPROM for Event Log but such EEPROM must be on a separate i2c bus and connected only to the microcontroller. The Event Log must always be accessed via the assigned registers in the microcontroller.

Two pins at the power supply connector are allocated for the I2C Serial Clock (SCL) signal and the Serial Data (SDA) signal. Both pins are bi-directional and are used to form a serial I2C bus. Pins A0, A1, and A2 are also allocated at the power supply connector for selecting the I2C address of communication devices inside the power supply. For hardware requirements for the I2C pins, refer to section 4.2.17.4.

The address capability of the power supply is shown in Table 36.

**TABLE 37- POWER SUPPLY I2C DEVICE ADDRESS CAPABILITY**

| PDB address pins A2/A1/A0 | 0/0/0 | 0/0/1 | 0/1/0 | 0/1/1 | 1/0/0 | 1/0/1 | 1/1/0 | 1/1/1 |
|---|---|---|---|---|---|---|---|---|
| Power Supply FRU device (EEPROM) | 0xA0 | 0xA2 | 0xA4 | 0xA6 | 0xA8 | 0xAA | 0xAC | 0xAE |
| Power Supply Monitoring/Control device (microcontroller) | 0xB0 | 0xB2 | 0xB4 | 0xB6 | 0xB8 | 0xBA | 0xBC | 0xBE |
| Power Supply UART Communication | 0X90 | 0X92 | 0X94 | 0X96 | 0X98 | 0X9A | 0X9C | 0X9E |

#### 12.1.2 UC FLASH Programming Interface

All microcontrollers in the power supply with flash memory shall be capable of off-line programming and checksum verification. The power supply shall at a minimum contain a connector header to which an external programming device can perform the following:

Read the uC flash memory in HEX data
Calculate a checksum value for the HEX data
Program the uC flash memory with new HEX data

The PS vendor shall provide LiteON with the necessary equipment and instructions to perform these tasks.

### 12.1.3 UC FLASH CHECKSUM

A checksum value shall be calculated for each microcontroller with flash memory inside the power supply. The checksum value shall:
Be at least 4 digits in length (e.g. 0xFFFF)
Be constant value for each unique power supply revision.
For example All Rev 01 power supplies have checksum 0x1234.

## 12.2 FIRMWARE PROTOCOL

An I2C Master device shall accesses the uC over an I2C interface using standard I2C transfer semantics. The uC shall always be an I2C slave. The I2C Master is permitted to operate the I2C clock (SCL) up to 100 kHz (10 µs minimum period). The uC is permitted to extend any clock period by holding the clock in the low state. An I2C Master device shall not send a communication sequence more often than once within any 80msec period.

The uC firmware UA shall have a 2 seconds timeout for the completion of a single I2C transaction. It shall start a 2 second timer when it receives a start condition. If a stop is not received within 2 seconds then the timer should time out and the UA shall reset its I2C interface and be ready for next I2C transaction from the system. Under no circumstances the UA shall hold the I2C bus (SCL or SDA) longer than 2 second. Upon receiving a Stop condition the UA shall abort the current I2C communication and be ready for the next communication.

The UA supports three operations for register set access: a write operation, read operation and a command operation. All operations include two transfers, one write transfer followed by one read transfer. These operations are described in the following sections.

In the following sections, figures showing I2C transfers use the following abbreviations:

**TABLE 38 – I2C ABBREVIATIONS**

| ABBREVIATION | DESCRIPTION |
|---|---|
| S | Start condition |
| Address | Device address (most significant seven bits of the address byte) |
| R/W | Read or Write designation bit (LSB of the device address) |
| REG | Data value in a write transfer that defines the register that I2c Master intends to write (in this transfer) or read (in the next transfer) |
| Data*n* | Data being read from the target or written to the target |
| A, A* | Acknowledge and negative acknowledge, either by the slave for writes or by the master for reads. (The $I^2C$ protocol requires the master to "negative acknowledge" the last byte of a read transfer. This causes the slave to release the data signal so the master can signal the stop condition.) |
| CHKSUM | Check sum |
| N | Not acknowledge, either by the slave for writes or by the master for reads |
| P | Stop condition |

In these figures, dark shaded areas indicate times when the master is driving the data bit, SDA, and light areas indicate times when the slave is driving the data bit.

### 12.2.1 Checksum

The checksum for any group of bytes is the two's complement of the sum of the bytes. Therefore, the sum of the bytes and the checksum is 0, modulo 100h. The checksum calculation includes the I2C slave address (except in the 2nd Read Checksum, CHKSUMr) and all the data bytes.

The I2C Master shall always verify the checksum after a read operation or a write operation. If the checksum indicates a communication failure, then the standard practice

shall be for the I2C Master to retry the operation up to 3 times before reporting a communication failure.

12.2.2 Write Operations

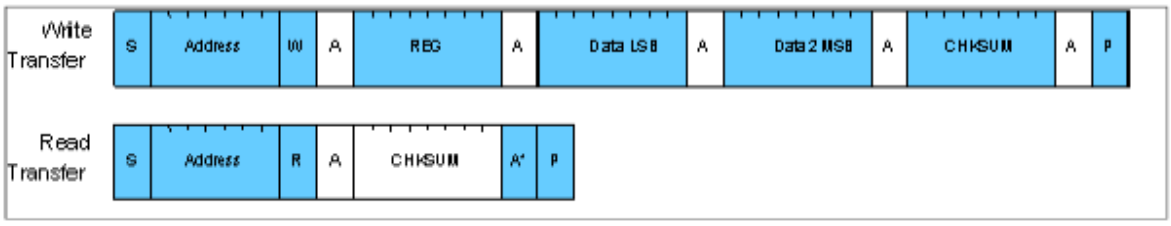
Write operations to the uC are comprised of a write transfer followed by a read transfer. Repeated start operation is not supported.

The write transfer of a write operation always contains exactly four data bytes. The first data byte of the write transfer specifies the uC register location to be accessed. The next two bytes are the data to be written to the register (LSB first). The fourth data byte is the checksum for the preceding three bytes and the I2C slave address. If the uC register location is received as 0x5E, the operation shall be interpreted as a command operation.

The read transfer for a write operation always contains exactly one data byte. It provides I2C Master with a confirmation that the write transfer was received without error by the uC. If the write transfer was completed without error to the uC, the uC drives exactly the checksum of the write transfer as the single data byte of the read transfer. If the uC detected a checksum error during the write transfer, it drives the binary inverse of the checksum (as received by the uC) as the single data byte of the read transfer. If the uC detects an error on a write transfer of a write operation, it discards the data and does not update the specified register. If I2C Master detects an error on the read transfer of a write operation, it repeats the entire write operation.

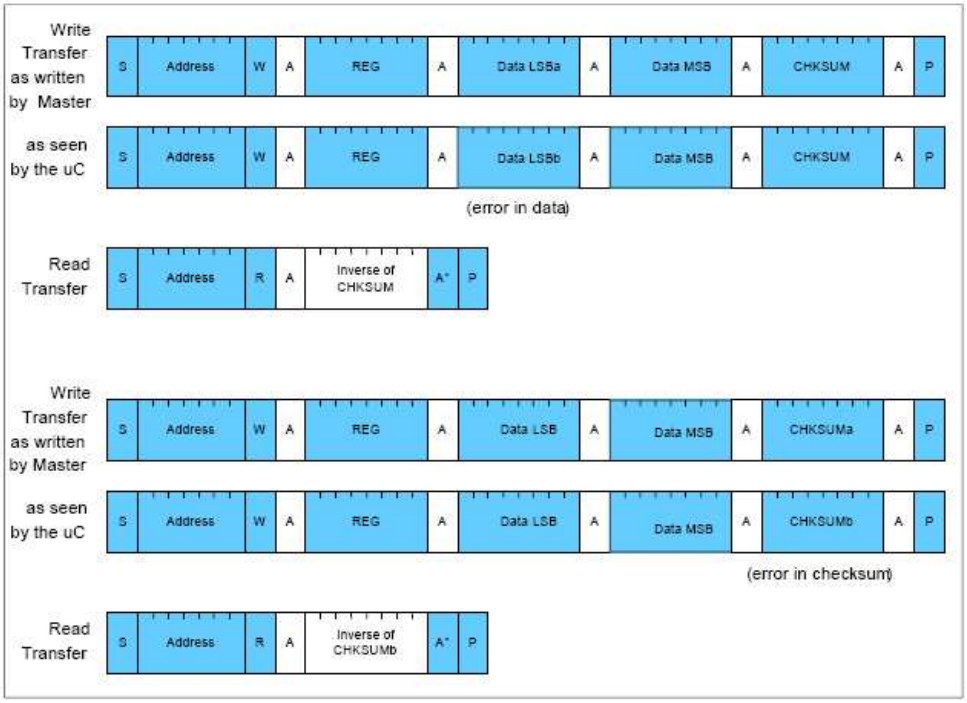
A typical write operation is shown in the figure below. In this example, Reg designates the register location being written. Data LSB designates the least significant byte of the data written to the uC register. Data MSB designates the most significant byte of the data written to the uC register. CHKSUM is the checksum for Address, REG, Data LSB, and Data MSB. In this example, the uC received the write data without an error and indicated this by sending the same checksum (CHKSUM) back to I2C Master during the read transfer.

**FIGURE 12 - TYPICAL WRITE OPERATION TO THE UC, NO ERROR**




The figure below shows two write error cases. In first case, an error occurs during transmission of Data LSB such that the uC receives a value other than the value sent by I2C Master. In this case, the uC detects the error when it calculates the checksum and indicates the error by sending the inverse of CHKSUM. In the second case, the error actually occurs in the CHKSUM byte. In this case, I2C Master transmitted a checksum value of CHKSUMa, but an error occurred on the bus, which caused the uC to read CHKSUMb as the checksum. The uC indicates the error by inverting the checksum, as it detected it, and using this as the data for the read transfer.

**FIGURE 13 - TYPICAL WRITE OPERATION TO THE UC, ERROR ON WRITE TRANSFER**




12.2.3 Read Operations

Read operations to the uC are comprised of two transfers, a write transfer followed by a read transfer.

Repeated start operation between transfers is not supported.

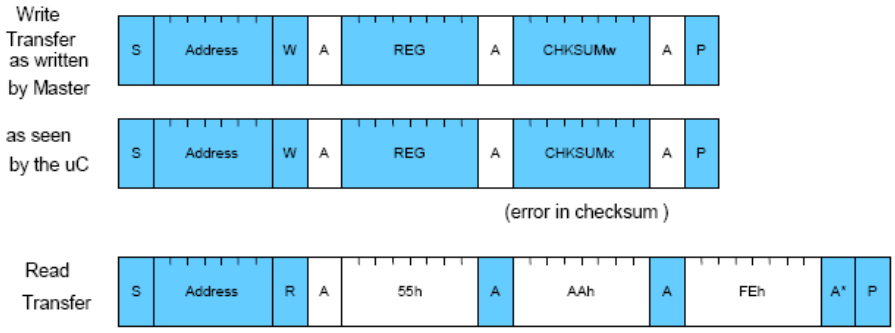
The write transfer of a read operation always contains exactly two data bytes. The first data byte of the write transfer specifies the uC register location to be accessed. The next byte is the checksum for the preceding byte and the I2C slave address. The read transfer for a read operation always contains exactly three data bytes. It provides I2C Master with a confirmation that the write of the register location was received without error by the uC and provides the requested read data. If the write transfer was completed without error by the uC, the uC provides the request read data (LSB first). The third byte is the checksum for the preceding two bytes, as described in Section 12.3.1. If the uC detected a checksum error during the write transfer, it drives 0x55, 0xAA, 0xFE as the three data bytes of the read transfer.

A typical read operation is shown in the figure below. In this example, REG in the one-byte write transfer designates the register location. CHKSUMw is the checksum for REG and Address. Data LSB designates the least significant data byte read from the uC register location REG. Data MSB designates the most significant data byte read from the uC register location REG. CHKSUMr is the checksum for Data LSB and Data MSB.

**FIGURE 14 - TYPICAL READ OPERATION FROM THE UC, NO ERROR**


The figure below shows the case in which the uC detects a checksum error in the write transfer. In this case, I2C Master transmitted a checksum value of CHKSUMw, but an error occurred on the bus, which caused the uC to read CHKSUMx as the checksum. The uC indicates the error by sending the pattern, 0x55, 0xAA, 0xFE, as the data for the read transfer. The read transfer would have been the same if the error had occurred in the REG byte rather than the CHKSUM byte. If the error was in the Address byte then a different device with that slave address would receive the data sent by the master in the write part of the read operation. If the slave uses this protocol then it would respond by sending the pattern, 0x55, 0xAA, 0xFE as described above. If a device at that address is not present then the master will not get and acknowledgement from the slave.

**FIGURE 15 - TYPICAL READ OPERATION FROM THE UC, ERROR ON WRITE TRANSFER**




12.2.4 Command Operations

Command operations to the uC are comprised of two transfers, a write transfer followed by a read transfer.

Repeated start operation between transfers is not supported.

The write transfer of a command operation contains command and data bytes. The first data byte of the write transfer specifies the uC register location 0x5E which indicates the following data bytes should be interpreted by the specified command operation. The command operation is indicated by the 2nd data byte of the write transfer. The intermediate data bytes contain the data to be processed. The final byte is the checksum for the preceding bytes and the i2C slave address.

The read transfer for a command operation always contains an odd number of data bytes. It provides I2C Master with a confirmation that the command operation was received without error by the uC and provides the requested read data if applicable. If the command operation was completed without error by the uC, the uC provides response according to the definition of the command process. If the uC detects a checksum error during the write transfer, it drives 0xFA as all data bytes requested by the master.

Typical command operation is shown in the figures below. In this example, REG in the one-byte write transfer designates the register location. CHKSUMw is the checksum for REG and Address. Data LSB designates the least significant data byte read from the uC

register location REG. Data MSB designates the most significant data byte read from the uC register location REG. CHKSUMr is the checksum for Data LSB and Data MSB.

**FIGURE 16 - TYPICAL COMMAND OPERATION TO THE UC, NO ERROR**

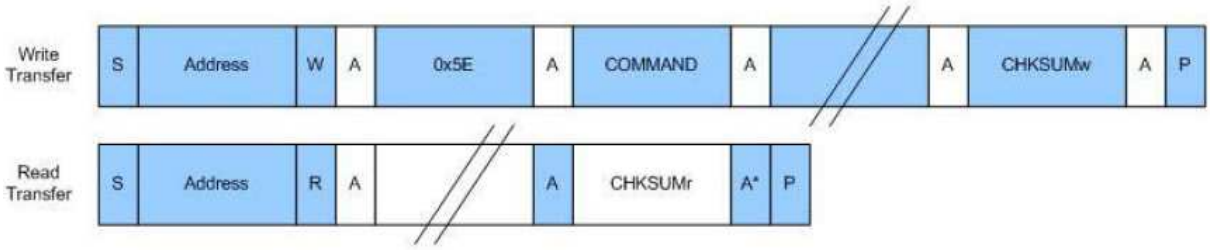
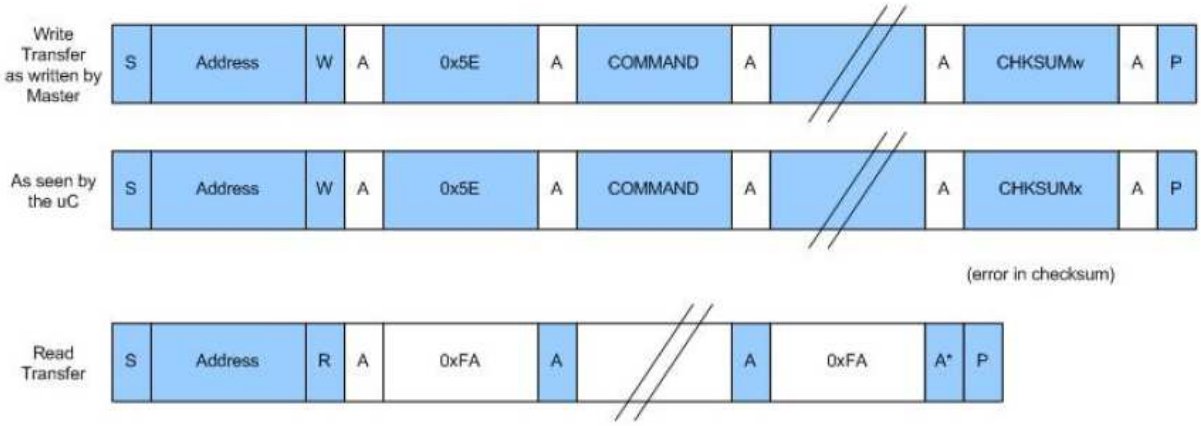



**FIGURE 17 - TYPICAL COMMAND OPERATION TO THE UC, ERROR ON WRITE TRANSFER**




## 12.3 CODE STRUCTURE

12.3.1 Initialization

### 12.3.1.1 Register Set

The uC shall have a set of registers described in the table below. The register set includes some reserved read only registers that are not used at this time. The reserved registers if read shall return a value of 0x0000. The reserved bits of all the registers shall also be read only and shall return zero when read. The registers are all 16-bits wide. The even address of the register shall store the LSB of the data and odd address shall store the MSB of the data. Read and write to odd number registers shall return a value of 0x0000. Only read and write to even number registers shall respond with the register data. Registers must be shadowed during update so that accessing the register via I2C in the middle of an update does not yield to LSB and MSB from two different updates. Registers providing sensor data must ensure that the data supplied is derived from a single analog to digital conversion and not skewed so as the MSB and the LSB come from two different conversions or events. If the analog to digital conversion has an accuracy of less than 16-bits, say 8 or 10 bits, the value must be stored at the correct scaling in the

required 16-bit format. Signed 2-byte data is returned in 2's compliment format. The data is returned in Little Endian format – LSB sent first, followed by MSB.

The power monitoring and reporting part of the firmware shall be referred as User Application (UA) in this document.

**TABLE 39 - MICROCONTROLLER REGISTERS**

| Register Name | Register Address | Bit(s) Name | Bit(s) Number | Access | Default Value |
|---|---|---|---|---|---|
| uC Info | 0x00 | Reserved | 0-3 | RO | |
| | | uC Type | 4-7 | | |
| | | Minor Firmware Revision | 8-B | | |
| | | Major Firmware Revision | C-F | | |
| PS Status | 0x02 | Output DCOK | 0 | RO | |
| | | Input OK | 1 | | |
| | | PSON | 2 | | |
| | | Vendor ID | 3-5 | | |
| | | Fan1 Override | 6 | | |
| | | Fan2 Override | 7 | | |
| | | Input Range | 8-A | | |
| | | Reserved | B-F | | |
| Shutdown Event | 0x04 | Failure | 0 | RO | |
| | | Over Voltage | 1 | | |
| | | Over Current | 2 | | |
| | | Over Temperature | 3 | | |
| | | Input Loss | 4 | | |
| | | Reserved | 5 | | |
| | | Fan1 Failure | 6 | | |
| | | Fan2 Failure | 7 | | |
| | | OTP Inlet | 8 | | |
| | | OTP Internal 1 | 9 | | |
| | | OTP Internal 2 | A | | |
| | | OCP1 | B | | |
| | | OCP2 | C | | |
| | | Reserved | D-F | | |
| Warning Event | 0x06 | Vin High Warning | 0 | RO | |
| | | Vin Low Warning | 1 | | |
| | | Vout High Warning | 2 | | |
| | | Vout Low Warning | 3 | | |
| | | Inlet Temp High Warning | 4 | | |
| | | Internal Temp High Warning | 5 | | |
| | | Vaux High Warning | 6 | | |
| | | Vaux Low Warning | 7 | | |
| | | Iout High Warning | 8 | | |
| | | Reserved | 9-F | | |
| Input Voltage | 0x08 | | | RO | |
| Input Current | 0x0A | | | RO | |
| Input Power | 0x0C | | | RO | |
| Output Voltage | 0x0E | | | RO | |
| Output Current | 0x10 | | | RO | |
| Output Power | 0x12 | | | RO | |
| Aux Voltage | 0x14 | | | RO | 0x0000 |
| Aux Current | 0x16 | | | RO | 0x0000 |

**TABLE 39 - MICROCONTROLLER REGISTERS**

| Register Name | Register Address | Bit(s) Name | Bit(s) Number | Access | Default Value |
|---|---|---|---|---|---|
| Aux Power | 0x18 | | | RO | 0x0000 |
| Inlet Temperature (T1) | 0x1A | | | RO | |
| Internal Temperature (T2) | 0x1C | | | RO | |
| Fan1 Speed | 0x1E | | | RO | |
| Fan2 Speed | 0x20 | Reserved | | RO | 0x0000 |
| Inlet Temp Monitor | 0x22 | | | RO | |
| Internal Temp 1 Monitor | 0x24 | | | RO | |
| Internal Temp 2 Monitor | 0x26 | | | RO | |
| Fan 1 Monitor | 0x28 | | | RO | |
| Capability | 0x2A | | | RO | |
| Average Input Power Accumulator LSW | 0x2C | | | RO | |
| Average Input Power Accumulator MSW | 0x2E | | | RO | |
| Average Input Power Count | 0x30 | | | RW | |
| Maximum ½ Second Average Input Power | 0x32 | | | RW | |
| Maximum ½ Second Average Input Current | 0x34 | | | RW | |
| Peak Output Current | 0x36 | | | RW | |
| Peak Aux Current | 0x38 | | | RW | 0x0000 |
| PS Control | 0x3A | System Type | 0-2 | RW | 0x0000 |
| | | Shutdown Event Interrupt Mask | 3 | | |
| | | Warning Event Interrupt Mask | 4 | | |
| | | Interrupt | 5 | | |
| | | Fan1 System Control | 6 | | |
| | | Fan2 System Control | 7 | | |
| | | SF1 – LED ON in SB | 8 | | |
| | | SF2 – Fan Fault Disabled | 9 | | |
| | | SF3 – Vout Step Up | A | | |
| | | SF4 – Vout Adjustable | B | | |
| | | SF5 – Vout Step Down | C | | |
| | | SF6 – SB Power Save | D | | |
| | | Reserved | E-F | | |
| Fan1 Control | 0x3C | | | RW | 0x0000 |
| Fan2 Control | 0x3E | Reserved | | RW | 0x0000 |
| Fan1 Min Speed | 0x40 | | | RW | 0x0000 |
| Fan2 Min Speed | 0x42 | Reserved | | RW | 0x0000 |
| Input Voltage Min Warning | 0x44 | | | RW | 0x0A00 |
| Input Voltage Max Warning | 0x46 | | | RW | 0x21C0 |
| Output Voltage Min Warning | 0x48 | | | RW | 0x0B00 |
| Output Voltage Max Warning | 0x4A | | | RW | 0x0D00 |
| Aux Voltage Min Warning | 0x4C | (Reserved for future development) | | RW | 0x0000 |
| Aux Voltage Max Warning | 0x4E | (Reserved for future development) | | RW | 0x0000 |
| Inlet Temperature Warning | 0x50 | | | RW | 0x0C80 |
| Internal Temperature Warning | 0x52 | | | RW | 0x1900 |
| Event Log Write | 0x54 | Event Log Offset | 0-7 | RW | 0x0000 |
| | | Event Log Data | 8-F | | |
| Event Log Read | 0x56 | Event Log Offset | 0-7 | RW | 0x0000 |
| | | 0x00 during Write / Event Log Data during read | 8-F | | |
| Output Voltage Set | 0x58 | | | RW | 0x3133 |
| Over Current Set point 1 | 0x5A | | | RW | 0x2300 |
| Over Current Set point 2 | 0x5C | | | RW | 0x2300 |
| Command Operation | 0x5E | | | RO | 0x0000 |

**TABLE 39 - MICROCONTROLLER REGISTERS**

| Register Name | Register Address | Bit(s) Name | Bit(s) Number | Access | Default Value |
|---|---|---|---|---|---|
| Image Status | 0x60 | Image ID | 0-1 | RO | |
| | | Checksum OK | 2-3 | | |
| | | Command Status | 4 | | |
| | | Reserved | 5-F | | |
| Main Image Revision | 0x62 | Minor FW Revision Number | 0-7 | RO | |
| | | Major FW Revision Number | 8-F | | |
| Main Image Checksum | 0x64 | | | RO | |
| Staged Image Revision | 0x66 | Minor FW Revision Number | 0-7 | RO | |
| | | Major FW Revision Number | 8-F | | |
| Staged Image Checksum | 0x68 | | | RO | |
| Reserved | 0x6A – 0xEE | | | RO | 0x0000 |
| Blackbox Read Register 0 | 0xF0 | Corresponds to 0x00 – 0x1E | | RO | 0xE3FE |
| Blackbox Read Register 1 | 0xF2 | Corresponds to 0x20 – 0x3E | | RO | 0x2E00 |
| Blackbox Read Register 2 | 0xF4 | Corresponds to 0x40 – 0x5E | | RO | 0x6000 |
| Blackbox Read Register 3 | 0xF6 | Corresponds to 0x60 – 0x7E | | RO | 0x0007 |
| Blackbox Read Register 4 | 0xF8 | Corresponds to 0x80 – 0x9E | | RO | 0x0000 |
| Blackbox Read Register 5 | 0xFA | Corresponds to 0xA0 – 0xBE | | RO | 0x0000 |
| Blackbox Read Register 6 | 0xFC | Corresponds to 0xC0 – 0xDE | | RO | 0x0000 |
| Blackbox Read Register 7 | 0xFE | Corresponds to 0xE0 – 0xFE | | RO | 0x0000 |

## 12.4 REGISTERS

### 12.4.1 Static

#### 12.4.1.1 uC Information (Register 0x00)

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | | | | | 0 | 0 | 0 | 0 |
| Definition | uC Type | | | | RESERVED | | | |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | | | | | | | | |
| Definition | Major Firmware Revision | | | | Minor Firmware Revision | | | |

| Bits | Description |
|---|---|
| F - C | Major Firmware Revision. This revision number shall be updated for Spec Update or PSU revision as specified . At time of product release, the firmware revision shall be set to 2.0. |
| B - 8 | Minor Firmware Revision. This revision number shall be updated for every new code revision by the PS Vendor after product release. Updated code after product release must be approved through the standard SCR process. |
| 7 – 4 | uC Type. These bits indicate the type of uC used. The uC type is assigned for each microcontroller vendor used.<br>0000b = Microchip;<br>0001b = STmicroelectronics;<br>0010b = FreeScale;<br>0011b = Texas Instruments;<br>0100b – Silicon Labs<br>All other bit combinations are reserved. If uC from other vendors are used then new code will be assigned for those vendors . |
| 3 - 0 | Reserved bits. Must return zero when read. |

#### 12.4.1.2 Capability (Register 0x2A)

The Capability register (0x2A) shall indicate which system types and special functions are capable on the power supply. The capability (and default values) shall be indicated by the applicable power supply specification.

| PS Control | Bit(s) | Requirement |
|---|---|---|
| System Type | 0-2 | Types 0,1,2,4,5 Required |
| Shutdown Event Interrupt Mask | 3 | Required |
| Warning Event Interrupt Mask | 4 | Required |
| Interrupt | 5 | Required |
| Fan1 System Control | 6 | Required |
| Fan2 System Control | 7 | Not Required |
| SF1 – LED ON in SB | 8 | Required |
| SF2 – Fan Fault Disabled | 9 | Required |
| SF3 – Vout Step Up | A | Not Required |
| SF4 – Vout Adjustable | B | Required |
| SF5 – Vout Step Down | C | Required |
| SF6 – SB Power Save | D | Required |
| Blackbox Register Set | E | Required |
| Reserved | F | Reserved |

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Access** | **RO** | **RO** | **RO** | **RO** | **RO** | **RO** | **RO** | **RO** |
| Default Value | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| Definition | SYSTEM TYPE 7 | SYSTEM TYPE 6 | SYSTEM TYPE 5 | SYSTEM TYPE 4 | SYSTEM TYPE 3 | SYSTEM TYPE 2 | SYSTEM TYPE1 | SYSTEM TYPE 0 |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| Definition | RESERVED | Blackbox | SF6 | SF5 | SF4 | SF3 | SF2 | SF1 |

| Bits | Description |
|---|---|
| F - E | Reserved bits. Reserved bits are read only and shall return 0 when read. |
| D - 8 | SF6 - SF0: Special Function Capability<br>0b = Special Function IS NOT capable on this power supply<br>1b = Special Function IS capable on this power supply |
| 7 - 0 | System Type 7 - 0: System Type Capability<br>0b = System Type IS NOT capable on this power supply<br>1b = System Type IS capable on this power supply |

#### 12.4.1.3 Blackbox Read Register 0 (Register 0xF0)

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| Definition | Reg. 0x0E | Reg. 0x0C | Reg. 0x0A | Reg. 0x08 | Reg. 0x06 | Reg. 0x04 | Reg. 0x02 | Reg. 0x00 |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| Definition | Reg. 0x1E | Reg. 0x1C | Reg. 0x1A | Reg. 0x18 | Reg. 0x16 | Reg. 0x14 | Reg. 0x12 | Reg. 0x10 |

| Bits | Description |
|---|---|
| F - 0 | Blackbox Read Register<br>0b = Blackbox should NOT read this register.<br>1b = Blackbox should read this register. |

#### 12.4.1.4 Blackbox Read Register 1 (Register 0xF2)

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Reg. 0x2E | Reg. 0x2C | Reg. 0x2A | Reg. 0x28 | Reg. 0x26 | Reg. 0x24 | Reg. 0x22 | Reg. 0x20 |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| Definition | Reg. 0x3E | Reg. 0x3C | Reg. 0x3A | Reg. 0x38 | Reg. 0x36 | Reg. 0x34 | Reg. 0x32 | Reg. 0x30 |

| Bits | Description |
|---|---|
| F - 0 | Blackbox Read Register<br>0b = Blackbox should NOT read this register.<br>1b = Blackbox should read this register. |

#### 12.4.1.5 Blackbox Read Register 2 (Register 0xF4)

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Reg. 0x4E | Reg. 0x4C | Reg. 0x4A | Reg. 0x48 | Reg. 0x46 | Reg. 0x44 | Reg. 0x42 | Reg. 0x40 |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Definition | Reg. | Reg. | Reg. | Reg. | Reg. | Reg. | Reg. | Reg. |

| | 0x5E | 0x5C | 0x5A | 0x58 | 0x56 | 0x54 | 0x52 | 0x50 |
|---|---|---|---|---|---|---|---|---|
| **Bits** | **Description** | | | | | | | |
| F - 0 | Blackbox Read Register<br>0b = Blackbox should NOT read this register.<br>1b = Blackbox should read this register. | | | | | | | |

#### 12.4.1.6 Blackbox Read Register 3 (Register 0xF6)

| **Bit #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Definition | Reg. 0x6E | Reg. 0x6C | Reg. 0x6A | Reg. 0x68 | Reg. 0x66 | Reg. 0x64 | Reg. 0x62 | Reg. 0x60 |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Reg. 0x7E | Reg. 0x7C | Reg. 0x7A | Reg. 0x78 | Reg. 0x76 | Reg. 0x74 | Reg. 0x72 | Reg. 0x70 |
| **Bits** | **Description** | | | | | | | |
| F - 0 | Blackbox Read Register<br>0b = Blackbox should NOT read this register.<br>1b = Blackbox should read this register. | | | | | | | |

#### 12.4.1.7 Blackbox Read Register 4 (Register 0xF8)

| **Bit #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Reg. 0x8E | Reg. 0x8C | Reg. 0x8A | Reg. 0x88 | Reg. 0x86 | Reg. 0x84 | Reg. 0x82 | Reg. 0x80 |
| Bit # | F | E | D | C | B | A | 9 | 8 |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Reg. 0x9E | Reg. 0x9C | Reg. 0x9A | Reg. 0x98 | Reg. 0x96 | Reg. 0x94 | Reg. 0x92 | Reg. 0x90 |
| **Bits** | **Description** | | | | | | | |
| F - 0 | Blackbox Read Register<br>0b = Blackbox should NOT read this register.<br>1b = Blackbox should read this register. | | | | | | | |

#### 12.4.1.8 Blackbox Read Register 5 (Register 0xFA)

| **Bit #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Reg. 0xAE | Reg. 0xAC | Reg. 0xAA | Reg. 0xA8 | Reg. 0xA6 | Reg. 0xA4 | Reg. 0xA2 | Reg. 0xA0 |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Definition | Reg. 0xBE | Reg. 0xBC | Reg. 0xBA | Reg. 0xB8 | Reg. 0xB6 | Reg. 0xB4 | Reg. 0xB2 | Reg. 0xB0 |
|---|---|---|---|---|---|---|---|---|
| **Bits** | **Description** | | | | | | | |
| F - 0 | Blackbox Read Register<br>0b = Blackbox should NOT read this register.<br>1b = Blackbox should read this register. | | | | | | | |

#### 12.4.1.9 Blackbox Read Register 6 (Register 0xFC)

| **Bit #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Reg. 0xCE | Reg. 0xCC | Reg. 0xCA | Reg. 0xC8 | Reg. 0xC6 | Reg. 0xC4 | Reg. 0xC2 | Reg. 0xC0 |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Reg. 0xDE | Reg. 0xDC | Reg. 0xDA | Reg. 0xD8 | Reg. 0xD6 | Reg. 0xD4 | Reg. 0xD2 | Reg. 0xD0 |
| **Bits** | **Description** | | | | | | | |
| F - 0 | Blackbox Read Register<br>0b = Blackbox should NOT read this register.<br>1b = Blackbox should read this register. | | | | | | | |

#### 12.4.1.10 Blackbox Read Register 7 (Register 0xFE)

| **Bit #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Reg. 0xEE | Reg. 0xEC | Reg. 0xEA | Reg. 0xE8 | Reg. 0xE6 | Reg. 0xE4 | Reg. 0xE2 | Reg. 0xE0 |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | RESERVED | | | | | | | |
| **Bits** | **Description** | | | | | | | |
| F - 8 | Reserved bits. Must return zero when read. | | | | | | | |
| 7 - 0 | Blackbox Read Register<br>0b = Blackbox should NOT read this register.<br>1b = Blackbox should read this register. | | | | | | | |

12.4.2 Status

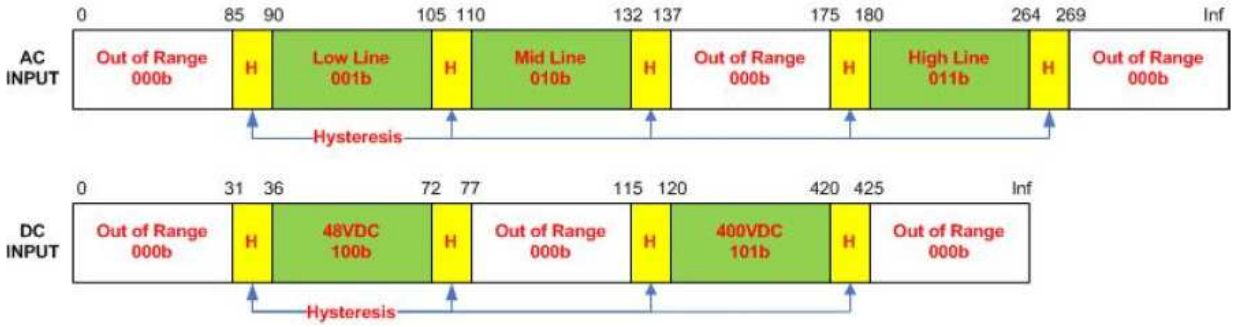
### 12.4.2.1 PS Status (Register 0x02)

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | | | | | | | |
| Definition | Fan2 Override | Fan1 Override | Vendor ID | | | PSON | Input OK | Output DCOK |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | | | |
| Definition | RESERVED | | | | | INPUT RANGE | | |

| Bits | Description |
|---|---|
| F - B | Reserved bits. Must return zero when read. |
| A – 8 | Input Range.<br>• 000b = Input Voltage out of range;<br>• 001b = Low Line. Input Voltage 90VAC to 108VAC;<br>• 010b = Mid Line. Input Voltage 109VAC to 132VAC;<br>• 011b = High Line. Input Voltage 180VAC to 264VAC;<br>• 100b = 48VDC, Input Voltage is 36VDC to 72VDC;<br>• 101b = 420VDC, Input Voltage is 120VDC to 420VDC;<br>• All other bit combinations are reserved.<br>See input range diagram below for explanation, hysteresis, etc. |
| 7 | Fan2 Override – not required<br>• 0b = If Fan2 Speed is set by the external system via Fan2 Control register then that has not been overridden by the PS internal Fan Control.<br>• 1b = Fan2 Speed set by the external system via Fan2 Control register has been overridden by the PS internal Fan Control.<br><br>This bit shall be cleared when the external system relinquishes the fan speed control by clearing the Fan2 System Control bit in the PS Control Register or when the Fan2 Speed set by the external system via Fan2 Control Register is higher than the Fan2 Speed required by power supply's internal Fan control. If Fan2 is not available then this bit is read only and shall always return zero when read. |
| 6 | Fan1 Override.<br>• 0b = If Fan1 Speed is set by the external system via Fan1 Control register then that has not been overridden by the PS internal Fan Control.<br>• 1b = Fan1 Speed set by the external system via Fan1 Control register has been overridden by the PS internal Fan Control.<br><br>This bit shall be cleared when the external system relinquishes the fan speed control by clearing the Fan1 System Control bit in the PS Control Register or when the Fan1 Speed set by the external system via Fan1 Control Register is higher than the Fan1 Speed required by power supply's internal Fan control. |
| 5 - 3 | Vendor ID.<br>• 010b = LiteOn;<br>• All other bit combinations are reserved |
| 2 | PSON - PSON bit shall indicate the status of the PSON pin.<br>• 0b = PSON signal is in standby position.<br>• 1b = PSON is asserted to turn the PS ON. |

| | |
|---|---|
| 1 | Input OK. Input can be AC or DC. The Input OK bit shall indicate if the input, AC or DC, is OK. \<br>• 0b = Input to the PS is not OK.<br>• 1b = Input to the PS is OK. |
| 0 | Output DCOK. The Output DCOK bit of this register shall indicate that the PS DC (12V Main) output is OK.<br>• 0b = Main DC output of the PS is not OK.<br>• 1b = Main DC output of the PS is OK. |

**FIGURE 18 - INPUT RANGE DIAGRAM**




Input voltage other than above specified range shall return a value of 000b to indicate that the Input Voltage is out of Range. Hysteresis shall be used so that the Input Range Code and the Input OK bit does not toggle when the input voltage is close to the input range limits

12.4.3 Control

The User Application (UA) shall allow limited external control of the PS via PS Control Register.

#### 12.4.3.1 PS Control (Register 0x3A)

PS Control register, address 0x3A, describes common features that can be enabled by the host system. For this power supply, the required features are listed below:

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RW | RW | RW | RW | RW | RW | RW |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Fan2 System Control | Fan1 System Control | Interrupt | Warning Event Mask | Shutdown Event Mask | System Type | | |

| Bit # | F | E | D | C | B | A | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RW | RW | RW | RW | RW | RW |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | RESERVED | | SF6 | SF5 | SF4 | SF3 | SF2 | SF1 |

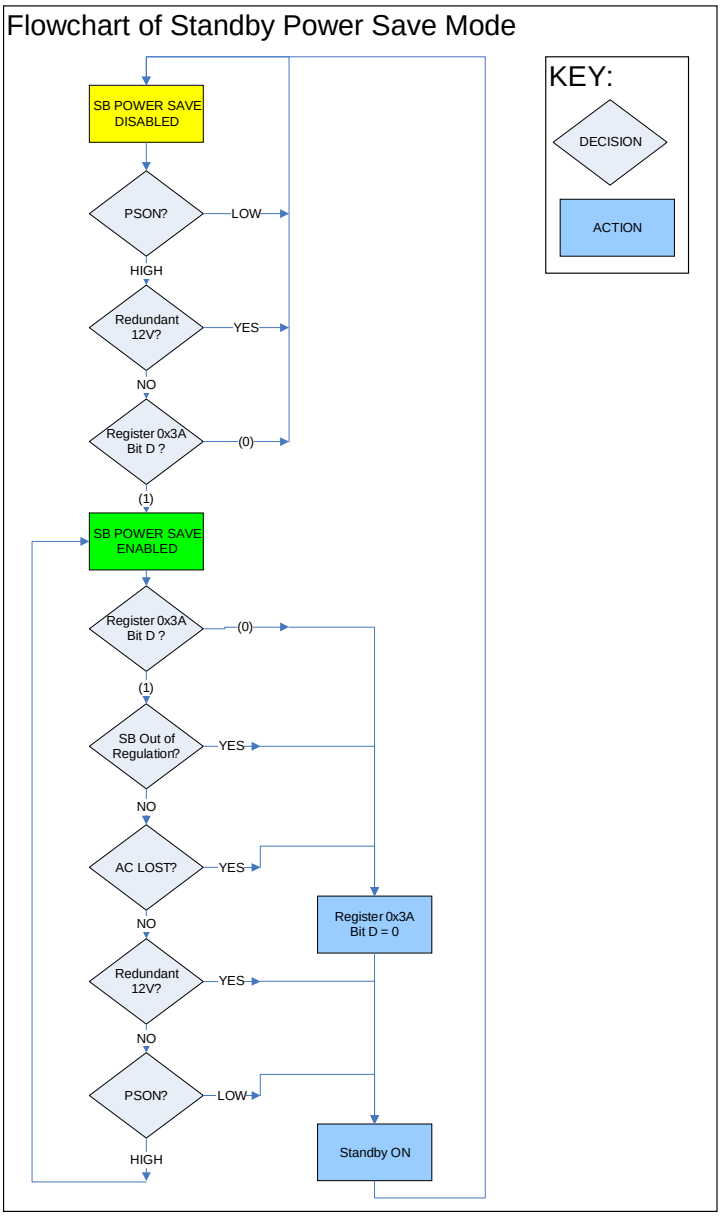
| Bits | Description |
|---|---|
| F - E | Reserved bits. Reserved bits are read only and shall return 0 when read. |

| Bits | Description |
|---|---|
| D | SF6 (Special Function 6): Standby Power Save<br>• 0b = Standby Power Save Disabled<br>• 1b = Standby Power Save Enabled<br>To enable Standby Power Save mode, ALL of the following conditions must occur:<br>• PSON is high (output disabled)<br>• 12V main output voltage is detected OFF (from any supply in parallel).<br>• SF6 bit is set high (1b)<br>To disable Standby Power Save mode, ANY of the following conditions can occur:<br>• PSON is low (output enabled)*<br>• 12V main output is detected ON (from any supply in parallel)*<br>• SF6 bit is reset low (0b)**<br>• Standby output is detected out of regulation low**<br>• Input power is removed from all supplies**<br>* In conditions 1 & 2 the supply shall disable standby save mode AND bit D shall remain high (1b).<br>** In conditions 3, 4, & 5 the supply shall disable standby save mode AND bit D shall be RESET low (0b).<br>*** PS shall ignore this setting if this feature is not supported by the power supply."<br><br>Refer to figure below for flowchart / explanation. |
| C | SF5 (Special Function 5): Vout Step Down<br>• 0b = Vout Step Down Disabled<br>• 1b = Vout Step Down Enabled<br>If SF5 bit is set, the PS output voltage shall be set to 12.05V ±30mV (across the entire output load range) and disable the droop share mode.<br>*** PS shall ignore this setting if this feature is not supported by the power supply." |
| B | SF4 (Special Function 4): Adjustable Vout – required<br>• 0b = Adjustable Vout Disabled<br>• 1b = Adjustable Vout Enabled<br>If SF4 bit is set, the PS output voltage shall be set to the voltage indicated by the Output Voltage Set Register (Register 0x58) and disable the droop share mode.<br>*** PS shall ignore this setting if this feature is not supported by the power supply." |
| A | SF3 (Special Function 3): Vout Step Up– not required<br>• 0b = Vout Step up Disabled<br>• 1b = Vout Step up Enabled<br>If SF3 bit is set, the PS output voltage shall be set to 12.40V ±40mV (at 1A output load).<br>*** PS shall ignore this setting if this feature is not supported by the power supply." |
| 9 | SF2 (Special Function 2): Fan Fault Disabled<br>• 0b = Fan Fault Enabled<br>• 1b = Fan Fault Disabled<br>If SF2 bit is set, the PS shall continue to operate even when the PS fan(s) have failed. If a Fan fails then the appropriate Fan Fail bit must be set but the PS Failure bit must not be set as long as the PS is operating normally without the FAN and the Output DCOK is OK. If another shutdown event occurs after a fan failure, then the PS shall shutdown and report both events to the shutdown event register and event log.<br>** PS shall ignore this setting if this feature is not supported by the power supply." |
| 8 | SF1 (Special Function 1): LED ON in SB<br>• 0b = LED OFF in SB<br>• 1b = LED ON in SB<br>If SF1 bit is set, the PS LED shall be ON even when the PS is put to standby via PSON signal and the Input to the PS is OK. However, the PS LED shall turn OFF if the PS has failed (failure bit = 1 in the shutdown event register).<br>** PS shall ignore this setting if this feature is not supported by the power supply." |
| 7 | Fan2 System Control. – not required<br>• 0b = External system does not want to control Fan2.<br>• 1b = External system is controlling Fan2 or wants to control Fan2.<br>This bit shall be set when external system writes a non-zero value to Fan2 Control register.<br>Clearing this bit shall clear the content of the Fan2 Control register and relinquish system control of Fan2 to PS. External system cannot set this bit and writing a 1b to this bit shall be ignored.<br>If Fan2 is not available then this bit is read only and shall always return 0b when read. |

| Bits | Description |
|---|---|
| 6 | Fan1 System Control.<br>• 0b = External system does not want to control Fan1.<br>• 1b = External system is controlling Fan1 or wants to control Fan1.<br>This bit shall be set when external system writes a non-zero value to Fan1 Control register. Clearing this bit shall clear the content of the Fan1 Control register and relinquish system control of Fan1 to PS. External system cannot set this bit and writing a 1b to this bit shall be ignored. |
| 5 | Interrupt bit.<br>• 0b = PS has not generated an interrupt.<br>• 1b = PS has generated and interrupt.<br>External system cannot set this bit and writing a 1b to this bit shall be ignored. This bit can be cleared by external system. Toggling the PSON, or cycling input voltage shall also clear this bit. Clearing this bit shall set the PSI2cInterrupt pin HIGH. |
| 4 | Warning Event Mask.<br>• 0b = PS shall not generate an interrupt when a Warning Event occurs.<br>• 1b = PS shall generate an interrupt when a Warning Event occurs. |
| 3 | Shutdown Event Mask.<br>• 0b = PS shall not generate an interrupt when a Shutdown Event occurs.<br>• 1b = PS shall generate an interrupt when a Shutdown Event occurs. |

| Bits | Description |
|---|---|
| 2 - 0 | System Type.<br>• 000b = ML/DL Systems. PS LED shall be off when the PS is put to standby via PSON signal or when the PS has failed. PS LED shall be lit when the Output DCOK is OK.<br>• 001b = Blade System. PS LED shall be ON even when the PS is put to standby via PSON signal and the Input to the PS is OK. However, the PS LED shall turn OFF if the PS has failed (failure bit = 1). When system type is changed to Blade system, PS shall update Min Fan Speed Register to 9000 RPMs.<br>• 010b = Redundant Fan Systems. PS function shall be identical to bit combination 000b (ML/DL systems) but the PS shall continue to operate even when the PS fan(s) have failed. If a Fan fails then the appropriate Fan Fail bit must be set but the PS Failure bit must not be set as long as the PS is operating normally without the FAN and the Output DCOK is OK. If another shutdown event occurs after a fan failure, then the PS shall shutdown and report both events (except input loss) to the shutdown event register and event log.<br>• 011b = Vout Step Up System. – not required. PS function shall be identical to bit combination 000b (ML/DL systems) but the PS output voltage shall be set to 12.40V ±40mV (at 1A output load) if this feature is supported by the PS. PS shall ignore this setting if this feature is not supported by the power supply.<br>• 100b = Adjustable Vout Systems – required. PS function shall be identical to bit combination 000b (ML/DL systems) but the PS output voltage shall be set to the voltage indicated by the Output Voltage Set Register (Register 0x58) and disable the droop share mode if this feature is supported by the PS. PS shall ignore this setting if this feature is not supported by the power supply.<br>• 101b = Vout Step Down System. PS function shall be identical to bit combination 000b (ML/DL systems) but the PS output voltage shall be set to 12.05V ±30mV (across the entire load range) and disable the droop share mode if this feature is supported by the PS. PS shall ignore this setting if this feature is not supported by the power supply.<br><br>All other bit combinations are reserved and writing these combinations shall be ignored. All system types and special function registers shall respond independently in an OR'd configuration. For example, if system type is 101 (vout step down) OR SF5 bit is 1, OR both, then the system shall respond as vout step down system. If multiple output voltage adjustments are indicated by a combination of special functions and/or system types, then the power supply shall respond in the following order: (1) SF4 / System Type 4 , (2) SF5 / System Type 5, (3) SF3 / System Type 3.<br><br>When the System Type is set to 001b, PS LED shall be lit as soon as Aux power is available and Input is OK. Otherwise, the PS LED shall be lit when the PSON is enabled and the Output DCOK is asserted. When the system type is set to 010b the UA shall disable the power supply fan fault shutdown. In that case when the PS fan fails the PS shall continue to operate normally, shall not de-assert the PSOK signal, and shall not set the Failure bit but must set the fan failure bit in the Shutdown Event Register. When the system type is set to 011b the UA shall set the output voltage to 12.45V if that feature is supported by the PS. When the system type is set to 100b the UA shall set the output voltage set by the Output Voltage Set register if that feature is supported by the PS. If the system type was set to Vout Step Up or Adjustable Vout System and is reverted back to a System type without those supports then the output voltage shall fall back to the nominal voltage of the power supply. If a system type is set but is not supported by the PS then the UA shall ignore that setting. If the Shutdown Event Mask bit is set by the external system and any of the bits in the Shutdown Event Register is set then the UA shall generate an interrupt via PsI2cInterrupt line. If the Warning Event Mask bit is set by the external system and any of the bits in the Warning Event Register is set then the UA shall generate an interrupt via PsI2cInterrupt line.<br><br>Fan1 System Control bit shall be set by the UA when the Fan1 Speed is set by the external system via Fan1 Control Register. When the external system clears this bit the UA shall clear the Fan1 Control Register and control the Fan1 fan speed internally. If a second Fan is present in the PS then Fan2 System Control shall represent fan Fan2 and shall be set and cleared similarly. |

**FIGURE 19 -FLOW CHART OF LiteON STANDBY POWER SAVE MODE**



#### 12.4.3.2 Output Voltage Set (Register 0x58)

User Application (UA) shall set the PS output voltage to the voltage set by this register, only when the system type bits in the PS Control Register is set to 100b (Adjustable Vout System.) The default value of this Register shall be 12.30V. The output voltage shall be set in 1/1024 volts as a 16-bit binary numbers (each least significant bit represents 1/1024 V). For output load conditions 10% of max load current, the minimum resolution of the output voltage sensor shall be 20mV with an accuracy of ±1% or better. For load conditions >10% of max load current, the minimum resolution of the output voltage sensor shall be 3mV with an accuracy of ±1% or better. This value of this register shall be limited by the PS Vout droop regulation limits (12.3V to 12V over full load). If external system sets a voltage higher than 12.3V then the UA shall limit it to 12.3V and if it sets a voltage lower than 12.0V then the UA shall limit it to 12.0V.

#### 12.4.3.3 Over Current Protection Set point 1 (Register 0x5A)

OCP Set Point = HW over-current threshold as defined in 4 (not-adjustable)

OCP2 Register = SW over-current threshold (effective ONLY lower than HW)

User Application (UA) shall allow adjustment of the over-current protection (OCP) for the main output by writing to an OCP register. The OCP register may only disable the output when a value is written lower than the default hardware OCP set point (which may exist anywhere between 120%-140% of output load). The OCP register shall default to the hardware maximum OCP set point (140% of output load). The OCP1 timer shall be set to 10-40mS max. Refer to Section 4 for additional information.

If the PSON# signal has transitioned from high to low, the PSOK signal is low, the output current exceeds the OCP1 register, AND the OCP1 timer has expired, then the output shall latch off and report the over-current condition in the shutdown event register.

This register shall provide the over current protection (OCP) limit for the 12V output. The OCP register shall be written in 1/64 amps as a 2's complement 16-bit binary numbers (each least significant bit represents 1/64 A).

| **Bit #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
|---|---|---|---|---|---|---|---|---|
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Default Value | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| Definition | OCP Set point 1 LSB | | | | | | | |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Default Value | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| Definition | OCP Set point 1 MSB | | | | | | | |

#### 12.4.3.4 Over Current Protection Set point 2 (Register 0x5C)

OCP Set Point = HW over-current threshold as defined in 4 (not-adjustable)

OCP1 Register = SW over-current threshold (effective ONLY lower than HW)

User Application (UA) shall allow adjustment of the over-current protection (OCP) for the main output by writing to an OCP register. The OCP register may only disable the output when a value is written lower than the default hardware OCP set point (which may exist anywhere between 120%-140% of output load). The OCP register shall default to the hardware maximum OCP set point (140% of output load). The OCP2 timer shall be set to 100-200mS max. Refer to Section 4 for additional information.

If the PSON# signal has transitioned from high to low, the PSOK signal is low, the output current exceeds the OCP2 register, AND the OCP2 timer has expired, then the output shall latch off and report the over-current condition in the shutdown event register.

This register shall provide the over current protection (OCP) limit for the 12V output. The OCP register shall be written in 1/64 amps as a 2's complement 16-bit binary numbers (each least significant bit represents 1/64 A).

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Default Value | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| Definition | OCP Set point 1 LSB | | | | | | | |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Default Value | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| Definition | OCP Set point 1 MSB | | | | | | | |

12.4.4 Shutdown

#### 12.4.4.1 Shutdown Event (Register 0x04)

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Fan2 Failure | Fan1 Failure | Reserve | Input Loss | OT | OC | OV | Failure |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | RESERVED | | | OCP2 | OCP1 | OT Internal 2 | OT Internal 1 | OT Inlet |

| Bits | Description |
|---|---|
| F - D | Reserved bits. Reserved bits are read only and shall return 0 when read. |
| C | OCP2<br>• 0b = PS is operating normally.<br>• 1b = PS has shutdown due to over current protection software limit OCP2<br><br>If this bit is set then it shall be cleared when any of the following occur:<br>• PSON transitions from disabled to enabled<br>• Input OK transitions from enabled to disabled<br>• Standby output voltage drops out of regulation |
| B | OCP1<br>• 0b = PS is operating normally.<br>• 1b = PS has shutdown due to over current protection software limit OCP1<br><br>If this bit is set then it shall be cleared when any of the following occur:<br>• PSON transitions from disabled to enabled<br>• Input OK transitions from enabled to disabled<br>• Standby output voltage drops out of regulation |
| A | Over Temperature Internal 2.<br>• 0b = PS is operating normally.<br>• 1b = PS has shutdown due to over temperature condition on Internal sensor #2.<br>If this bit is set then it shall be cleared when the over temperature condition is cleared. |
| 9 | Over Temperature Internal 1.<br>• 0b = PS is operating normally.<br>• 1b = PS has shutdown due to over temperature condition on Internal sensor #1.<br>If this bit is set then it shall be cleared when the over temperature condition is cleared. |
| 8 | Over Temperature Inlet.<br>• 0b = PS is operating normally.<br>• 1b = PS has shutdown due to over temperature condition on inlet sensor.<br>If this bit is set then it shall be cleared when the over temperature condition is cleared. |
| 7 | Fan2 Failure – not required<br>• 0b = Fan2 is OK.<br>• 1b = PS latched off due to Fan2 failure.<br>If this bit is set then it shall be cleared when any of the following occur:<br>• PSON transitions from disabled to enabled<br>• Input OK transitions from enabled to disabled<br>• Standby output voltage drops out of regulation<br>If Fan2 is not available then this bit is read only and shall always return 0b when read. |

| | |
|---|---|
| 6 | Fan1 Failure.<br>• 0b = Fan1 is OK.<br>• 1b = PS latched off due to Fan1 failure.<br>If this bit is set then it shall be cleared when any of the following occur:<br>• PSON transitions from disabled to enabled<br>• Input OK transitions from enabled to disabled<br>• Standby output voltage drops out of regulation |
| 5 | Reserved bit. Must return zero when read. |
| 4 | Input Loss. Input can be AC or DC.<br>• 0b = PS input is present.<br>• 1b = PS input is not present. |
| 3 | Over Temperature.<br>• 0b = PS is operating normally.<br>• 1b = PS has shutdown due to over temperature condition on any temp sensor.<br>If this bit is set then it shall be cleared when the over temperature condition is cleared. |
| 2 | Over Current.<br>• 0b = PS is operating normally.<br>• 1b = PS latched off due to an over current condition (hardware limit or software limit)<br><br>If this bit is set then it shall be cleared when any of the following occur:<br>• PSON transitions from disabled to enabled<br>• Input OK transitions from enabled to disabled<br>• Standby output voltage drops out of regulation |
| 1 | Over Voltage.<br>• 0b = PS is operating normally.<br>• 1b = PS latched off due to an over voltage condition.<br>If this bit is set then it shall be cleared when any of the following occur:<br>• PSON transitions from disabled to enabled<br>• Input OK transitions from enabled to disabled<br>• Standby output voltage drops out of regulation |
| 0 | Failure. This bit indicates a general PS failure.<br>• 0b = PS is operating normally.<br>• 1b = PS has failed. PS Input is OK, PSON is ON, and Output DCOK is not OK.<br>When this bit gets set it will initiate an event log write if the previous event was not same as the present event. If this bit is set then it shall be cleared when any of the following occur:<br>• PSON transitions from disabled to enabled<br>• Input OK transitions from enabled to disabled<br>• Standby output voltage drops out of regulation |

12.4.5 Warning

The user application (UA) shall check the PS input voltage, output voltage and temperature against t he warning levels set by the external system and set the appropriate warning bits in the warning event register. It shall set the Vin high warning, Vout high warning, Vaux high warning, inlet temp (T1) high warning, and internal temp (T2) high warning bits when the sensor data exceeds the set warning limits of the respective sensors. It shall set the Vin low warning, Vout low warning, and Vaux low warning when the sensor data falls below the respective sensor's regulation limits. Inlet temperature (T1) and internal temperature (T2) warning bits shall be cleared when the respective sensor data is 5 Deg. C below the set warning limit. Temp high warnings (T1 & T2) are always valid. Vin and Vaux high & low warnings are valid only when the input OK status bit is set. Vout high & low warnings are valid only when the output DCOK status bit is set. Adequate hysteresis shall be used to prevent the reported status from toggling.

**TABLE 40 - DEFAULT INPUT VOLTAGE WARNING SET POINTS**

| PS Input | Input Voltage Min Warning Set (1) | Input Voltage Min Warning Clear (0) | Input Voltage Max Warning Clear (0) | Input Voltage Max Warning Set (1) |
|---|---|---|---|---|
| AC | 80 VAC | < or = 89 VAC | > or = 265 VAC | 270 VAC |
| 48V DC | 30 VDC | < or = 35 VDC | > or = 73 VDC | 75 VDC |
| 400V DC | 100 VDC | < or = 119 VDC | > or = 421 VDC | 450 VDC |

**12.4.5.1 Warning Event (Register 0x06)**

| **Bit #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | Vaux Low | Vaux High | Internal Temp High | Inlet Temp High | Vout Low | Vout High | Vin Low | Vin High |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | RESERVED | | | | | | | Iout high |

| **Bits** | **Description** |
|---|---|
| F - 9 | Reserved bits. Must return zero when read. |
| 8 | Iout High Warning.<br>• 0b = Output current is lower than or equal to 100% of max spec.<br>• 1b = Output current is higher than 100% of max spec.<br><br>This bit shall be reset when:<br>• Output current is reduced lower than 95% of max spec.<br>• Output DCOK status bit is reset low |
| 7 | Vaux Low Warning. – not required<br>• 0b = Vaux voltage is higher than level set by the Aux Voltage Min Warning register.<br>• 1b = Vaux voltage is lower than the level set by the Aux Voltage Min Warning register.<br>This bit is valid only when InputOK status bit is set. If this bit is set then it shall be cleared when Aux Voltage is within regulation limit.<br><br>If Vaux sensor is not available then this bit shall always return 0b when read. |

| | |
|---|---|
| 6 | Vaux High Warning. – not required<br>• 0b = Vaux voltage is lower than level set by the Aux Voltage Max Warning register.<br>• 1b = Vaux voltage is higher than the level set by the Aux Voltage Max Warning register.<br>This bit is valid only when InputOK status bit is set. If this bit is set then it shall be cleared when Aux Voltage is within regulation limit.<br><br>If Vaux sensor is not available then this bit shall always return 0b when read. |
| 5 | Internal Temp High Warning.<br>• 0b = Internal temperature is lower than level set by the Internal Temperature Warning register.<br>• 1b = Internal temperature is higher than level set by the Internal Temperature Warning register.<br><br>If this bit is set then it shall be cleared when internal temperature is 5C lower than the temperature set by the Internal Temperature Warning register. |
| 4 | Inlet Temp High Warning.<br>• 0b = Inlet temperature is lower than level set by the Inlet Temperature Warning register.<br>• 1b = Inlet temperature is higher than level set by the Inlet Temperature Warning register.<br><br>If this bit is set then it shall be cleared when inlet temperature is 5C lower than the temperature set by the Inlet Temperature Warning register. |
| 3 | Vout Low Warning.<br>• 0b = Output voltage is higher than level set by the Output Voltage Min Warning register.<br>• 1b = Output voltage is lower than the level set by the Output Voltage Min Warning register.<br><br>This bit is valid only when Output DCOK status bit is set. If this bit is set then it shall be cleared when Output Voltage is within regulation limit and higher than the level set by the Output Voltage Min Warning register. |
| 2 | Vout High Warning.<br>• 0b = Output voltage is lower than level set by the Output Voltage Max Warning register.<br>• 1b = Output voltage is higher than the level set by the Output Voltage Max Warning register.<br><br>This bit is valid only when Output DCOK status bit is set. If this bit is set then it shall be cleared when Output Voltage is within regulation limit and lower than the level set by the Output Voltage Max Warning register. |
| 1 | Vin Low Warning.<br>• 0b = Input voltage is higher than level set by the Input Voltage Min Warning register.<br>• 1b = Input voltage is lower than the level set by the Input Voltage Min Warning register.<br><br>This bit is valid only when InputOK status bit is set. See the table below for set and clear thresholds. |
| 0 | Vin High Warning.<br>• 0b = Input voltage is lower than level set by the Input Voltage Max Warning register.<br>• 1b = Input voltage is higher than the level set by the Input Voltage Max Warning register.<br><br>This bit is valid only when InputOK status bit is set. See the table below for set and clear thresholds. |

#### 12.4.5.2 Input Voltage Min Warning (Register 0x44)

The UA shall generate an input voltage warning by setting the Vin Low Warning bit in the Warning Event Register when the input voltage is below the value set in the Input Voltage Min Warning Register.

External system shall be capable of setting the Input Voltage Min Warning level by writing to this register. If it writes an Input Voltage Min Warning level within 8V or higher than the Input Voltage Max Warning level then the UA shall set the Input Voltage Min Warning 8V (1 Least Significant Bit of Most significant Byte) lower than the Input Voltage Max Warning level.

#### 12.4.5.3 Input Voltage Max Warning (Register 0x46)

The UA shall generate an input voltage warning by setting the Vin High Warning bit in the Warning Event Register when the input voltage is above the value set in the Input Voltage Max Warning Register.

External system shall be capable of setting the Input Voltage Max Warning level by writing to this register. If it writes an Input Voltage Max Warning level within 8V or lower than the Input Voltage Min Warning level then the UA shall set the Input Voltage Max Warning 8V (1 Least Significant Bit of Most significant Byte) higher than the Input Voltage Min Warning level.

#### 12.4.5.4 Output Voltage Min Warning (Register 0x48)

The Vout Low Warning bit in the Warning Event Register shall be set when the output voltage is below the value set in the Output Voltage Min Warning Register. The default value of Output Voltage Min Warning Register is 11.0V.

The warning shall be cleared when the output voltage is within regulation limits. External system shall be capable of setting the Output Voltage Min warning level by writing to this register. If it writes an Output Voltage Min Warning level within 1V of or higher than the Output Voltage Max Warning level then the UA shall set the Output Voltage Min Warning 1V (1 Least Significant Bit of Most significant Byte) lower than the Output Voltage Max Warning level.

#### 12.4.5.5 Output Voltage Max Warning (Register 0x4A)

The Vout High Warning bit in the Warning Event Register shall be set when the output voltage is above the value set in the Output Voltage Max Warning Register. The default value of Output Voltage Max Warning Register is 13.0V.

The warning shall be cleared when the output voltage is within regulation limits. External system shall be capable of setting the Output Voltage Max warning level by writing to this register. If it writes an Output Voltage Max Warning level within 1V of or lower than the Output Voltage Min Warning level then the UA shall set the Output Voltage Max Warning 1V (1 Least Significant Bit of Most significant Byte) higher than the Output Voltage Min Warning level.

#### 12.4.5.6 Aux Voltage Min Warning (Register 0x4C) – Not Required

The Vaux Low Warning bit in the Warning Event Register shall be set when the aux voltage is below the value set in the Aux Voltage Min Warning Register. If aux voltage sensor is not available then a write to this register shall be ignored, the default value of this register shall be 0x0000 and shall always return the default value when read.

The warning shall be cleared when the aux voltage is within regulation limits. External system shall be capable of setting the Aux Voltage Min warning level by writing to this register. If it writes an Aux Voltage Min Warning level within 1V of or higher than the Aux Voltage Max Warning level then the UA shall set the Aux Voltage Min Warning 1V (1 Least Significant Bit of Most significant Byte) lower than the Aux Voltage Max Warning level.

#### 12.4.5.7 Aux Voltage Max Warning (Register 0x4E) – Not Required

The Vaux High Warning bit in the Warning Event Register shall be set when the aux voltage is above the value set in the Aux Voltage Max Warning Register. If aux voltage sensor is not available then a write to this register shall be ignored, the default value of this register shall be 0x0000 and shall always return the default value when read.

The warning shall be cleared when the aux voltage is within regulation limits. External system shall be capable of setting the Aux Voltage Max warning level by writing to this register. If it writes an Aux Voltage Max Warning level within 1V of or lower than the Aux Voltage Min Warning level then the UA shall set the Aux Voltage Max Warning 1V (1 Least Significant Bit of Most significant Byte) higher than the Aux Voltage Min Warning level.

#### 12.4.5.8 Inlet Temperature Warning (Register 0x50)

The Inlet Temp High Warning bit in the Warning Event Register shall be set when the inlet temperature is above the value set in this Register. The default value of inlet temperature warning shall be 50C. When the inlet temperature is greater than 50C, the power supply shall increase the fan speed linearly to regulate the inlet temperature to prevent, or delay, an over temperature shutdown.

The warning shall be cleared when the inlet temperature is 5C below the value set in this register. External system shall be capable of setting the warning levels by writing to this Registers.

#### 12.4.5.9 Internal Temperature Warning (Register 0x52)

The Internal Temp High Warning bit in the Warning Event Register shall be set when the internal temperature is above the value set in this Register. The default value of internal temperature warning shall be 100C.

The warning shall be cleared when the internal temperature is 5C below the value set in this register. External system shall be capable of setting the warning levels by writing to this Registers.

### 12.4.6 Input

#### 12.4.6.1 Input Voltage (Register 0x08)

The User Application (UA) shall monitor and report the input voltage to the power supply via Input Voltage Register. The input voltage shall be reported in 1/32 volts RMS as a 2's complement 16-bit binary numbers (each least significant bit represents 1/32 VRMS). The minimum resolution of the input voltage sensor shall be 1.4V with a reporting accuracy of ±5% or better. The UA shall update this value at least once every 250msec. The UA shall respond to a step change within 1 second, after which the new data shall be within the accuracy requirements.

#### 12.4.6.2 Input Current (Register 0x0A)

The User Application (UA) shall monitor and report the input current to the power supply via Input Current Register. The input current shall be reported in 1/64 amps as a 2's complement 16-bit binary numbers (each least significant bit represents 1/64 A). The minimum resolution of the input current sensor shall be 50mA. The UA shall update this value at least once every 250msec. The UA shall respond to a step change within 1 second, after which the new data shall be within the accuracy requirements. The minimum input current reported shall be 0.25A. Input current reporting accuracy shall be:

**TABLE 41 – F/W INPUT CURRENT ACCURACY**

| Input ≤ 0.25A | 0.25A < input ≤ 1A | 1A<input ≤ 3A | Input > 3A |
|---|---|---|---|
| Out of range<br>Report 0.25A | ±0.05A | 5% | 3% |

#### 12.4.6.3 Input Power (Register 0x0C)

The User Application (UA) shall monitor and report the total input power of the power supply. The RMS input power shall be reported in Watts, (W) via Input Power Register. The UA shall update this value at least once every 250msec. The UA shall respond to a step change within 1 second, after which the new data shall be within the accuracy requirements

The reported input power shall be greater than the reported output power for any condition of output power greater than 36W (3A on 12V).

The reported input power shall be capable of reporting down to 20W of input power.

**TABLE 42 – F/W INPUT POWER ACCURACY**

| Input Power <20W | 20W≤ Input Power ≤100W | Input power > 100W |
|---|---|---|
| Out of range<br>Report a constant value | ±5W* | ±5%* |

** When calibrated at 115VAC and 230VAC and 270VDC(at 12Vsb/1A).*

#### 12.4.6.4 Average Input Power Accumulator and Counter

The UA shall have a 32bit accumulator of average input power every 0.5 sec, (±10%, 450ms-550ms). Every 0.5 seconds, it shall measure the average input power over the preceding 0.5 second to the accuracy specified for register 0x0C and accumulate that half second average power in the Average Input Power Accumulator LSW and Average Input Power Accumulator MSW. Each time the Average Input Power Count register is read, the uC stores a snap shot of the internal average input power accumulator that corresponds to this count, and makes that snap shot available in the externally visible Average Input Power Accumulator registers. When the Average-Power Accumulator registers are read, the values are those associated with the most recent reading of the Average Input Power Count register, regardless of the delay between reading those registers. If the Average Input Power Count register is read again before reading the Average Input Power Accumulator registers, the uC takes a new snap shot of the internal average power accumulator.

#### 12.4.6.5 Average Input Power Accumulator LSW (Register 0x2C)

This register shall hold the Least Significant Word of the Average Input Power Accumulator.

#### 12.4.6.6 Average Input Power Accumulator MSW (Register 0x2E)

This register shall hold the Most Significant Word of the Average Input Power Accumulator.

#### 12.4.6.7 Average Input Power Count (Register 0x30)

This register shall maintain a 16 bit count of the average input power added to the Average Input Power Accumulator Register. When the Average Input Power Count reaches its limit (0xFFFF) the UA shall stop accumulating the Average Input Power in the Average Input Power Accumulator Register and stop incrementing the Average Input Power Count Register and retain the values in both the registers until the Average Input Power Count Register is cleared by the external system. When the external system clears the Average Input Power Count Register, by writing 0x0000 to this register OR when input is Not OK (PS Status register, bit 1 = 0), the UA shall clear the Average Input Power Accumulator Register and start a new accumulation and count.

#### 12.4.6.8 Maximum ½ Second Average Input Power (Register 0x32)

The User Application (UA) shall monitor and report the maximum ½ second input power as the maximum 1/2 sec average power value added to the Average Input Power Accumulator since the Maximum ½ Second Input Power Register was cleared. The aximum ½ second average input power reporting shall be active after Input OK signal is asserted. External system can clear this register and start a new maximum ½ second average input power calculation by writing 0x0000 to this Register OR when input is Not OK (PS Status register, bit 1 = 0). Writing a value other than 0x0000 to this register shall be ignored.

#### 12.4.6.9 Maximum ½ Second Average Input Current (Register 0x34)

The User Application (UA) shall monitor and report the maximum 1/2-second average input current of the power supply via Peak Input Current Register The maximum ½ second average input current shall be reported in 1/64 amps as a 2's complement 16-bit binary number (each least significant bit represents 1/64 A). The minimum resolution and accuracy shall be same as the input current reporting. The maximum ½ second average input current reporting shall be active after InputOK signal is asserted. External system can clear this register and start a new peak input current calculation by writing 0x0000 to this Register OR when input is Not OK (PS Status register, bit 1 = 0). Writing a value other than 0x0000 to this register shall be ignored.

### 12.4.7 Main Output

#### 12.4.7.1 Output Voltage (Register 0x0E)

This Register shall provide the measured output voltage of the 12V main output. The output voltage shall be reported in 1/256 volts as a 2's complement 16-bit binary numbers (each least significant bit represents 1/256 V). The minimum resolution of the output voltage sensor shall be 60mV with and accuracy of ±2% or better. 13.4.7.2 Output Current (Register 0x10) This register shall provide the measured 12V output current. The output current shall be reported in 1/64 amps as a 2's complement 16-bit binary numbers (each least significant bit represents 1/64 A). The minimum resolution of the output current sensor shall be 500mA. The minimum output current reported shall be 3A. Output current reporting accuracy shall be:

**TABLE 43 – F/W OUTPUT CURRENT REPORTING ACCURACY**

| <=3A | 3<output<6A | 6A<output<10A | 10A<output<30A | 30A<=output |
|---|---|---|---|---|
| Undefined | ±50% | ±15% | ±10% | ±5% |

#### 12.4.7.3 Output Power (Register 0x12)

This register shall provide the total output power of the 12V main output. The output power shall be reported in watts.

Reported output power shall not exceed the reported input power for any condition of output power greater than 36W (3A on 12V).

The reported output power shall be capable of reporting output power down to 36W (3A) output power.

#### 12.4.7.4 Peak Output Current (Register 0x36)

This register shall store the peak output current of the 12V main output. The peak output current shall be reported in 1/64 amps as a 2's complement 16-bit binary numbers (each least significant bit represents 1/64 A). The minimum resolution and accuracy shall be same as the output current reporting. The Peak Output Current shall be active after PSOK signal is asserted. External system can clear this register and start a new peak output current calculation by writing a 0x0000 to this Register OR when output is Not OK (PS Status register, bit 0= 0)." Writing a value other than 0x0000 to this register shall be ignored.

### 12.4.8 Temperature

The User Application (UA) shall monitor the inlet air temperature of the power supply and two internal hotspot temperatures.

#### 12.4.8.1 Inlet Temperature (T1) (Register 0x1A)

This register shall provide the inlet air temperature coming into the power supply. The temperature sensor data shall be reported in 1/64 °C as a 2's complement 16-bit binary numbers (each least significant bit represents 1/64 °C). The minimum resolution of the inlet temperature shall be 1.5 °C with an accuracy of ± 5 °C. The inlet temperature accuracy requirement shall be applied only above the nominal inlet operating temp of 25 °C and when the supply has reached thermal equilibrium.

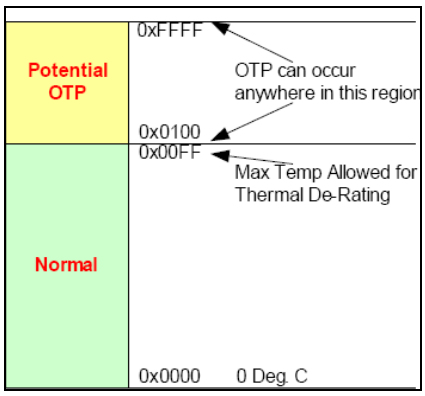
#### 12.4.8.2 Internal Temperature (T2) (Register 0x1C)

This register shall provide the maximum temperature of the two internal hotspot temperatures inside of the power supply. The temperature sensor data shall be reported in 1/64 °C as a 2's complement 16-bit binary numbers (each least significant bit represents 1/64 °C). The minimum resolution of the internal temperature shall be 1.5 °C with an accuracy of ± 5 °C. The location of the hotspot shall be determined by individual power supply vendor. The internal temperature accuracy requirement shall be applied only above the nominal inlet operating temp of 25 °C and when the supply has reached thermal equilibrium.

#### 12.4.8.3 Inlet Temperature Monitor (Register 0x22)

This register shall provide the percentage of the inlet temperature sensor compared to the maximum allowed temperature to maintain all component thermal derating.

**FIGURE 20 - TEMPERATURE MONITOR DIAGRAM**




The monitor data shall be reported in 1/256 percent as a 2's complement 16-bit binary numbers (each least significant bit represents 1/256 percent. Above the 0x0100 level, the temp sensor causes the fan to increase speed to prevent an over-temperature protection event.

#### 12.4.8.4 Internal Temperature Monitor 1 (Register 0x24)

This register shall provide the percentage of the primary internal temperature sensor compared to the maximum allowed temperature to maintain all component thermal derating.

The monitor data shall be reported in 1/256 percent as a 2's complement 16-bit binary numbers (each least significant bit represents 1/256 percent). At 0x0100 and above, the power supply is allowed to shut down due to an over-temperature protection. At the 0x0100 level, the fan shall begin increasing speed to prevent an over-temperature protection event.

#### 12.4.8.5 Internal Temperature Monitor 2 (Register 0x26)

This register shall provide the percentage of the secondary internal temperature sensor compared to the maximum allowed temperature to maintain all component thermal derating.

The monitor data shall be reported in 1/256 percent as a 2's complement 16-bit binary numbers (each least significant bit represents 1/256 percent). At 0x0100 and above, the power supply is allowed to shut down due to an over-temperature protection. At the 0x0100 level, the fan shall begin increasing speed to prevent an over-temperature protection event.

### 12.4.9 Fan

The User Application (UA) shall monitor the fan tachometer signals and report the fan speeds in RPM. It shall be capable of controlling the fan speeds set by the external system.

#### 12.4.9.1 Fan1 Speed (Register 0x1E)

This register shall provide the measured Fan1 speed. Fan1 speed shall be reported in rpm with an accuracy of ± 5% or better. The minimum resolution of the reported fan speed shall be 200 rpm.

#### 12.4.9.2 Fan2 Speed (Register 0x20) – not required

This register shall provide the measured Fan2 speed. Fan2 speed shall be reported in rpm with an accuracy of ± 5% or better. The minimum resolution of the reported fan speed shall be 200 rpm. If Fan2 is not available then the default value of this register shall be 0x0000 and shall always return the default value when read.

#### 12.4.9.3 Fan1 Control (Register 0x3C)

If the external system wants to control the Fan1 speed then it can write the desired fan RPM to this Register. Writing a value of 0x0000 to this register shall be ignored. The UA shall set the Fan1 System Control bit in the PS Control Register to indicate that the system has written the fan speed to the Fan1 Control Register. If the external system no longer wishes to control the Fan1 speed then it shall clear the Fan1 System Control bit in the PS Control Register and the UA shall clear the Fan1 Control Register and control the Fan1 speed internally. The fan speed control must be set immediately (>100 RPM/sec) to implement the fan speed set by the external system. The UA can override the fan speed set by the external system and increase the fan speed to meet power supply thermal requirement but it is not allowed to set the fan speed lower than the speed set by the external system. If the UA overrides the fan speed it shall indicate that by setting fan override bit in the PS Status register.

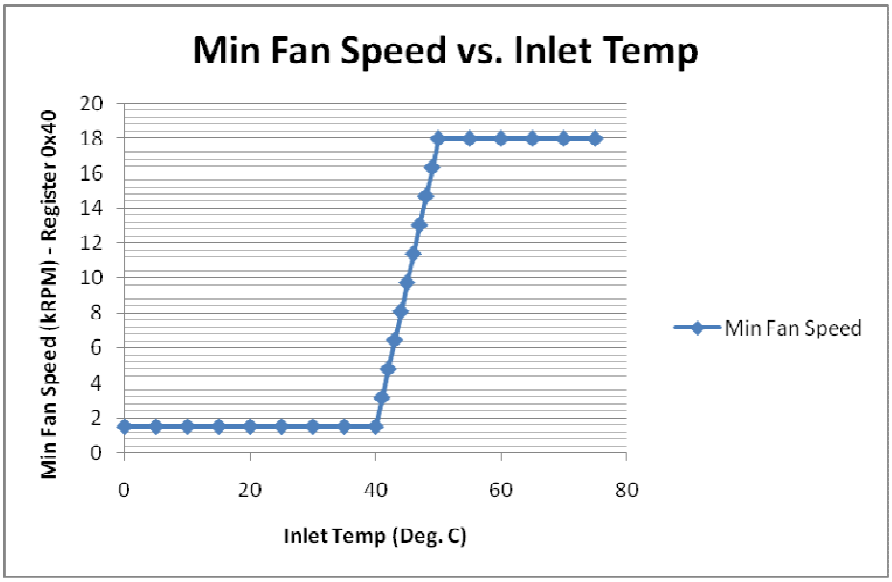
#### 12.4.9.4 Fan2 Control (Register 0x3E) – not required

If the external system wants to control the Fan2 speed then it can write the desired fan RPM to this Register. Writing a value of 0x0000 to this register shall be ignored. The UA shall set the Fan2 System Control bit in the PS Control Register to indicate that the system has written the fan speed to the Fan2 Control Register. If the external system no longer wishes to control the Fan2 speed then it shall clear the Fan2 System Control bit in the PS Control Register and the UA shall clear the Fan2 Control Register and control the Fan2 speed internally. The fan speed control must be set immediately (>100 RPM/sec) to implement the fan speed set by the external system. The UA can override the fan speed set by the external system and increase the fan speed to meet power supply thermal requirement but it is not allowed to set the fan speed lower than the speed set by the external system. If the UA overrides the fan speed it shall indicate that by setting fan override bit in the PS Status register. If Fan2 is not available then a write to this register shall be ignored and the default value of this register shall be 0x0000 and shall always return the default value when read.

#### 12.4.9.5 Fan1 Min Speed (Register 0x40)

External system can set Fan1 Min Speed via this register. The default value of this register shall be 0x05DC. The UA shall not set the Fan1 speed lower that the speed set by this register in any condition.

**FIGURE 21 - MIN FAN SPEED VS. INLET TEMP**



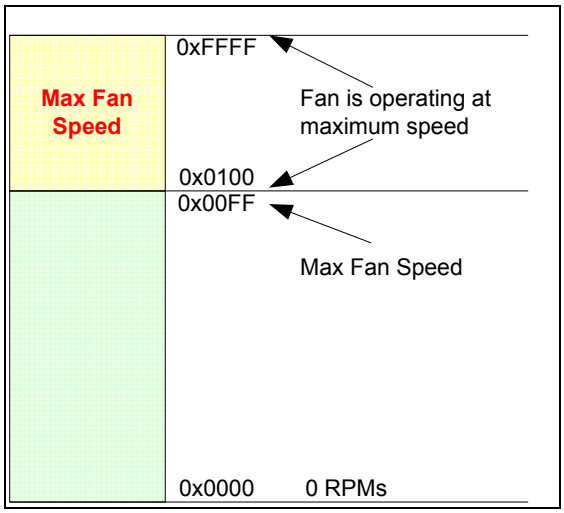

#### 12.4.9.6 Fan2 Min Speed (Register 0x42) – not required

External system can set Fan2 Min Speed via this register. The default value of this register shall be 0x0000. The UA shall not set the Fan2 speed lower that the speed set by this register in any condition. If Fan2 is not available then a write to this register shall be ignored and the default value of this register shall be 0x0000 and shall always return the default value when read.

#### 12.4.9.7 Fan Speed Monitor 1 (Register 0x28)

This register shall provide the percentage of the fan speed compared to the maximum available fan speed.

**FIGURE 22 - POWER SUPPLY FAN MONITOR DIAGRAM**




The monitor data shall be reported in 1/256 percent as a 2's complement 16-bit binary numbers (each least significant bit represents 1/256 percent). At 0x0100 and above, the power supply fan is operating at the maximum duty cycle.

12.4.10 Interrupt

**12.4.10.1 Description**

The UA shall generate an interrupt on the PsI2cInterrupt line if any of the bits on the Shutdown Event Register or the Warning Event Register is set and the respective mask bits are set in the PS Control Register. It shall set the Interrupt bit in the PS Control Register after generating the interrupt. The PsI2cInterrupt shall be an active low open drain signal and appropriate pull up resistor must be provided on the system side. This signal shall be set high when the system clears the Interrupt bit in the PS Control register OR when the system resets from a failure condition as described in the shutdown event register.

12.4.11 Event Log

The PS shall have an Event Log EEPROM of 256 bytes. User Application (UA) shall provide the external system read and write access to the Event Log via Event Log Read and Event Log Write Register using the same I2C protocol described in section 12 of this document.

**12.4.11.1 Event Log Write Register (Register 0x54)**

External system shall be capable of writing to the Event Log EEPROM indirectly via this register. External system must write 2 bytes to this Register to write to the Event Log. The first byte (LSB of the Event Log Write Register) shall be the offset of the Event Log to be written and the second byte (MSB of the Event Log Write Register) shall be the data to be written. On completion of the write to this register the UA shall transfer the data to the Event Log.

| **Bit #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
|---|---|---|---|---|---|---|---|---|
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | EVENT LOG OFFSET | | | | | | | |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |

| Access | RW | RW | RW | RW | RW | RW | RW | RW |
|---|---|---|---|---|---|---|---|---|
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | EVENT LOG DATA | | | | | | | |

| Bits | Description |
|---|---|
| F - 8 | Event log offset. |
| 7 - 0 | Event Log Data |

#### 12.4.11.2 Event Log Read Register (Register 0x56)

External system shall be capable of reading to the Event Log EEPROM indirectly via this register. External system must write 2 bytes to this Register first to read from the Event Log. The first byte (LSB of the Event Log Read Register) shall be the offset of the Event Log to be read and the second byte (MSB of the Event Log Read Register) shall be 0x00 for this transfer. On completion of the write to this register the UA shall read the data from the Event Log offset and store it in the MSB of the Event Log Read Register.

The external system shall then read the Event Log Read Register and receive the Event Log data from the MSB that read.

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | EVENT LOG OFFSET | | | | | | | |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | EVENT LOG DATA | | | | | | | |

| Bits | Description |
|---|---|
| F - 8 | Event log offset. |
| 7 - 0 | Event Log Data |

#### 12.4.11.3 Persistent Peak Event Log Offsets (0-24)

The persistent peak register offsets shall communicate maximum reported readings. The User Application (UA) shall update the persistent peak register offsets as necessary to maintain the peak values. The register offsets shall be both read and write accessible. For each offset - the register shall be cleared (data set to 0x00) after all manufacturing tests are completed and before the power supply is shipped.

- Peak Input Voltage (offsets 0-1) - maximum reported input voltage.
- Peak Input Current (offsets 2-3) - maximum reported input current.
- Peak Input Power (offsets 4-5)- maximum reported input power.
- Peak Output Voltage (offsets 6-7) - maximum reported output voltage.
- Peak Output Current (offsets 8-9) - maximum reported output current.
- Peak Output Power (offsets 10-11)- maximum reported output power.
- Peak Inlet Temp (offsets 12-13) - maximum reported inlet temperature.
- Peak Internal Temp (offsets 14-15)- maximum reported internal temperature
- Peak Fan Speed (offsets 16-17) -maximum reported fan speed.
- Reserved (offsets 18-24) - RESERVED.

#### 12.4.11.4 Run Time Counter

The User Application (UA) shall maintain a total runtime counter. The runtime counter shall keep count of number of minutes the power supply has been operating. The power supply shall be considered operating when the Output DCOK signal is high. The UA shall update the runtime counter in the Event Log EEPROM once every 24 hours or when the event log is updated due to an event.

#### 12.4.11.5 Calibration

The User Application (UA) shall allow calibration information to be stored in designated registers of the Event Log. The offset 0x1C shall be designated as the key and the offsets 0x20 to 0x2D shall hold the calibration data. The UA shall only allow write commands to calibration offsets if the key matches the specified value 0x4B. If the key matches the specified value 0x4B, then the UA shall also allow data to be written in the event log for all read-only registers. This shall be used to allow the manufacturer to clear the event log after production testing and before shipping the supply. The UA shall reset the key offset to 0x00 at every power-on reset condition of the microcontroller. If production calibration is not utilized, the calibration registers shall be set to zero.

Note: The calibration data registers (offset 32 – 45) shall be accessible only when the calibration key is written.

#### 12.4.11.6 Event Log Update

User Application (UA) shall maintain a circular log of the last 7 events by saving the registers specified in this section. When the event log update starts the UA shall set the event update flag by writing a 1 to the event update flag in the Event Log EEPROM. Every event shall start with an event number followed by 3 bytes of time stamp. The total runtime at the time of the event shall be the time stamp. The total runtime counter in the Event Log EEPROM must be updated before the time is stamped. The PS Status, Shutdown Event, Warning Event, Input Voltage, Input Current, Output Voltage, Output Current, T1 Temp, T2 Temp, F1 Speed, Peak Input Current, Peak Output Current, and PS Control registers shall be stored in the event log (LSB first). UA shall update the event log when the power supply has failed (Failure bit in the Shutdown Event Register has been set) and the previous event was not same as the current event. It shall update the runtime counter every time an event happens whether that event is written to the event log or not. When there are more than 7 events then the 8th event shall overwrite the 1st event. The 9th event shall overwrite the 2nd event and so on. After writing the event log the total event count and the next event location shall be updated. Finally the event update flag shall be cleared to indicate that the entire event was written successfully.

**Table 44 - Power Supply event log**

| Access | Offset (Dec) | Data (Dec) | Description |
|---|---|---|---|
| RW | 0 | 0 | Peak Input Voltage LSB |
| RW | 1 | 0 | Peak Input Voltage MSB |
| RW | 2 | 0 | Peak Input Current LSB |
| RW | 3 | 0 | Peak Input Current MSB |
| RW | 4 | 0 | Peak Input Power LSB |
| RW | 5 | 0 | Peak Input Power MSB |
| RW | 6 | 0 | Peak Output Voltage LSB |
| RW | 7 | 0 | Peak Output Voltage MSB |
| RW | 8 | 0 | Peak Output Current LSB |
| RW | 9 | 0 | Peak Output Current MSB |
| RW | 10 | 0 | Peak Output Power LSB |

**Table 44 - Power Supply event log**

| Access | Offset (Dec) | Data (Dec) | Description |
|---|---|---|---|
| RW | 11 | 0 | Peak Output Power MSB |
| RW | 12 | 0 | Peak Inlet Temp LSB |
| RW | 13 | 0 | Peak Inlet Temp MSB |
| RW | 14 | 0 | Peak Internal Temp LSB |
| RW | 15 | 0 | Peak Internal Temp MSB |
| RW | 16 | 0 | Peak Fan Speed LSB |
| RW | 17 | 0 | Peak Fan Speed MSB |
| RW | 18 | 0 | RESERVED |
| RW | 19 | 0 | |
| RW | 20 | 0 | |
| RW | 21 | 0 | |
| RW | 22 | 0 | |
| RW | 23 | 0 | |
| RW | 24 | 0 | |
| RO | 25 | 0 | Total Runtime LSB |
| RO | 26 | 0 | Total Runtime Byte #2 |
| RO | 27 | 0 | Total Runtime MSB |
| RW | 28 | 0 | Calibration Key |
| RO | 29 | 0 | Event update Flag |
| RO | 30 | 0 | Total Event count |
| RO | 31 | 46 | Next Event Location |
| RO | 32 | 0 | Calibration Data |
| RO | 33 | 0 | Calibration Data |
| RO | 34 | 0 | Calibration Data |
| RO | 35 | 0 | Calibration Data |
| RO | 36 | 0 | Calibration Data |
| RO | 37 | 0 | Calibration Data |
| RO | 38 | 0 | Calibration Data |
| RO | 39 | 0 | Calibration Data |
| RO | 40 | 0 | Calibration Data |
| RO | 41 | 0 | Calibration Data |
| RO | 42 | 0 | Calibration Data |
| RO | 43 | 0 | Calibration Data |
| RO | 44 | 0 | Calibration Data |
| RO | 45 | 0 | Calibration Data |
| RO | 46 | 0 | Event # |
| RO | 47 | 0 | Runtime LSB |
| RO | 48 | 0 | Runtime Byte #2 |
| RO | 49 | 0 | Runtime MSB |
| RO | 50 | 0 | PS Status LSB |
| RO | 51 | 0 | PS Status MSB |
| RO | 52 | 0 | Shutdown Event LSB |
| RO | 53 | 0 | Shutdown Event MSB |
| RO | 54 | 0 | Warning Event LSB |
| RO | 55 | 0 | Warning Event MSB |
| RO | 56 | 0 | Input Voltage LSB |
| RO | 57 | 0 | Input Voltage MSB |
| RO | 58 | 0 | Input Current LSB |
| RO | 59 | 0 | Input Current MSB |

**Table 44 - Power Supply event log**

| Access | Offset (Dec) | Data (Dec) | Description |
|---|---|---|---|
| RO | 60 | 0 | Output Voltage LSB |
| RO | 61 | 0 | Output Voltage MSB |
| RO | 62 | 0 | Output Current LSB |
| RO | 63 | 0 | Output Current MSB |
| RO | 64 | 0 | T1 Temperature LSB |
| RO | 65 | 0 | T1 Temperature MSB |
| RO | 66 | 0 | T2 Temperature LSB |
| RO | 67 | 0 | T2 Temperature MSB |
| RO | 68 | 0 | F1 Speed LSB |
| RO | 69 | 0 | F1 Speed MSB |
| RO | 70 | 0 | Peak Input Current LSB |
| RO | 71 | 0 | Peak Input Current MSB |
| RO | 72 | 0 | Peak Output Current LSB |
| RO | 73 | 0 | Peak Output Current MSB |
| RO | 74 | 0 | PS Control LSB |
| RO | 75 | 0 | PS Control MSB |
| RO | 76 | 0 | Event # |
| RO | 77 | 0 | Runtime LSB |
| RO | 78 | 0 | Runtime Byte #2 |
| RO | 79 | 0 | Runtime MSB |
| RO | 80 | 0 | PS Status LSB |
| RO | 81 | 0 | PS Status MSB |
| RO | 82 | 0 | Shutdown Event LSB |
| RO | 83 | 0 | Shutdown Event MSB |
| RO | 84 | 0 | Warning Event LSB |
| RO | 85 | 0 | Warning Event MSB |
| RO | 86 | 0 | Input Voltage LSB |
| RO | 87 | 0 | Input Voltage MSB |
| RO | 88 | 0 | Input Current LSB |
| RO | 89 | 0 | Input Current MSB |
| RO | 90 | 0 | Output Voltage LSB |
| RO | 91 | 0 | Output Voltage MSB |
| RO | 92 | 0 | Output Current LSB |
| RO | 93 | 0 | Output Current MSB |
| RO | 94 | 0 | T1 Temperature LSB |
| RO | 95 | 0 | T1 Temperature MSB |
| RO | 96 | 0 | T2 Temperature LSB |
| RO | 97 | 0 | T2 Temperature MSB |
| RO | 98 | 0 | F1 Speed LSB |
| RO | 99 | 0 | F1 Speed MSB |
| RO | 100 | 0 | Peak Input Current LSB |
| RO | 101 | 0 | Peak Input Current MSB |
| RO | 102 | 0 | Peak Output Current LSB |
| RO | 103 | 0 | Peak Output Current MSB |
| RO | 104 | 0 | PS Control LSB |
| RO | 105 | 0 | PS Control MSB |
| RO | 106 | 0 | Event # |
| RO | 107 | 0 | Runtime LSB |
| RO | 108 | 0 | Runtime Byte #2 |

**Table 44 - Power Supply event log**

| Access | Offset (Dec) | Data (Dec) | Description |
|---|---|---|---|
| RO | 109 | 0 | Runtime MSB |
| RO | 110 | 0 | PS Status LSB |
| RO | 111 | 0 | PS Status MSB |
| RO | 112 | 0 | Shutdown Event LSB |
| RO | 113 | 0 | Shutdown Event MSB |
| RO | 114 | 0 | Warning Event LSB |
| RO | 115 | 0 | Warning Event MSB |
| RO | 116 | 0 | Input Voltage LSB |
| RO | 117 | 0 | Input Voltage MSB |
| RO | 118 | 0 | Input Current LSB |
| RO | 119 | 0 | Input Current MSB |
| RO | 120 | 0 | Output Voltage LSB |
| RO | 121 | 0 | Output Voltage MSB |
| RO | 122 | 0 | Output Current LSB |
| RO | 123 | 0 | Output Current MSB |
| RO | 124 | 0 | T1 Temperature LSB |
| RO | 125 | 0 | T1 Temperature MSB |
| RO | 126 | 0 | T2 Temperature LSB |
| RO | 127 | 0 | T2 Temperature MSB |
| RO | 128 | 0 | F1 Speed LSB |
| RO | 129 | 0 | F1 Speed MSB |
| RO | 130 | 0 | Peak Input Current LSB |
| RO | 131 | 0 | Peak Input Current MSB |
| RO | 132 | 0 | Peak Output Current LSB |
| RO | 133 | 0 | Peak Output Current MSB |
| RO | 134 | 0 | PS Control LSB |
| RO | 135 | 0 | PS Control MSB |
| RO | 136 | 0 | Event # |
| RO | 137 | 0 | Runtime LSB |
| RO | 138 | 0 | Runtime Byte #2 |
| RO | 139 | 0 | Runtime MSB |
| RO | 140 | 0 | PS Status LSB |
| RO | 141 | 0 | PS Status MSB |
| RO | 142 | 0 | Shutdown Event LSB |
| RO | 143 | 0 | Shutdown Event MSB |
| RO | 144 | 0 | Warning Event LSB |
| RO | 145 | 0 | Warning Event MSB |
| RO | 146 | 0 | Input Voltage LSB |
| RO | 147 | 0 | Input Voltage MSB |
| RO | 148 | 0 | Input Current LSB |
| RO | 149 | 0 | Input Current MSB |
| RO | 150 | 0 | Output Voltage LSB |
| RO | 151 | 0 | Output Voltage MSB |
| RO | 152 | 0 | Output Current LSB |
| RO | 153 | 0 | Output Current MSB |
| RO | 154 | 0 | T1 Temperature LSB |
| RO | 155 | 0 | T1 Temperature MSB |
| RO | 156 | 0 | T2 Temperature LSB |
| RO | 157 | 0 | T2 Temperature MSB |

**Table 44 - Power Supply event log**

| Access | Offset (Dec) | Data (Dec) | Description |
|---|---|---|---|
| RO | 158 | 0 | F1 Speed LSB |
| RO | 159 | 0 | F1 Speed MSB |
| RO | 160 | 0 | Peak Input Current LSB |
| RO | 161 | 0 | Peak Input Current MSB |
| RO | 162 | 0 | Peak Output Current LSB |
| RO | 163 | 0 | Peak Output Current MSB |
| RO | 164 | 0 | PS Control LSB |
| RO | 165 | 0 | PS Control MSB |
| RO | 166 | 0 | Event # |
| RO | 167 | 0 | Runtime LSB |
| RO | 168 | 0 | Runtime Byte #2 |
| RO | 169 | 0 | Runtime MSB |
| RO | 170 | 0 | PS Status LSB |
| RO | 171 | 0 | PS Status MSB |
| RO | 172 | 0 | Shutdown Event LSB |
| RO | 173 | 0 | Shutdown Event MSB |
| RO | 174 | 0 | Warning Event LSB |
| RO | 175 | 0 | Warning Event MSB |
| RO | 176 | 0 | Input Voltage LSB |
| RO | 177 | 0 | Input Voltage MSB |
| RO | 178 | 0 | Input Current LSB |
| RO | 179 | 0 | Input Current MSB |
| RO | 180 | 0 | Output Voltage LSB |
| RO | 181 | 0 | Output Voltage MSB |
| RO | 182 | 0 | Output Current LSB |
| RO | 183 | 0 | Output Current MSB |
| RO | 184 | 0 | T1 Temperature LSB |
| RO | 185 | 0 | T1 Temperature MSB |
| RO | 186 | 0 | T2 Temperature LSB |
| RO | 187 | 0 | T2 Temperature MSB |
| RO | 188 | 0 | F1 Speed LSB |
| RO | 189 | 0 | F1 Speed MSB |
| RO | 190 | 0 | Peak Input Current LSB |
| RO | 191 | 0 | Peak Input Current MSB |
| RO | 192 | 0 | Peak Output Current LSB |
| RO | 193 | 0 | Peak Output Current MSB |
| RO | 194 | 0 | PS Control LSB |
| RO | 195 | 0 | PS Control MSB |
| RO | 196 | 0 | Event # |
| RO | 197 | 0 | Runtime LSB |
| RO | 198 | 0 | Runtime Byte #2 |
| RO | 199 | 0 | Runtime MSB |
| RO | 200 | 0 | PS Status LSB |
| RO | 201 | 0 | PS Status MSB |
| RO | 202 | 0 | Shutdown Event LSB |
| RO | 203 | 0 | Shutdown Event MSB |
| RO | 204 | 0 | Warning Event LSB |
| RO | 205 | 0 | Warning Event MSB |
| RO | 206 | 0 | Input Voltage LSB |

**Table 44 - Power Supply event log**

| Access | Offset (Dec) | Data (Dec) | Description |
|---|---|---|---|
| RO | 207 | 0 | Input Voltage MSB |
| RO | 208 | 0 | Input Current LSB |
| RO | 209 | 0 | Input Current MSB |
| RO | 210 | 0 | Output Voltage LSB |
| RO | 211 | 0 | Output Voltage MSB |
| RO | 212 | 0 | Output Current LSB |
| RO | 213 | 0 | Output Current MSB |
| RO | 214 | 0 | T1 Temperature LSB |
| RO | 215 | 0 | T1 Temperature MSB |
| RO | 216 | 0 | T2 Temperature LSB |
| RO | 217 | 0 | T2 Temperature MSB |
| RO | 218 | 0 | F1 Speed LSB |
| RO | 219 | 0 | F1 Speed MSB |
| RO | 220 | 0 | Peak Input Current LSB |
| RO | 221 | 0 | Peak Input Current MSB |
| RO | 222 | 0 | Peak Output Current LSB |
| RO | 223 | 0 | Peak Output Current MSB |
| RO | 224 | 0 | PS Control LSB |
| RO | 225 | 0 | PS Control MSB |
| RO | 226 | 0 | Event # |
| RO | 227 | 0 | Runtime LSB |
| RO | 228 | 0 | Runtime Byte #2 |
| RO | 229 | 0 | Runtime MSB |
| RO | 230 | 0 | PS Status LSB |
| RO | 231 | 0 | PS Status MSB |
| RO | 232 | 0 | Shutdown Event LSB |
| RO | 233 | 0 | Shutdown Event MSB |
| RO | 234 | 0 | Warning Event LSB |
| RO | 235 | 0 | Warning Event MSB |
| RO | 236 | 0 | Input Voltage LSB |
| RO | 237 | 0 | Input Voltage MSB |
| RO | 238 | 0 | Input Current LSB |
| RO | 239 | 0 | Input Current MSB |
| RO | 240 | 0 | Output Voltage LSB |
| RO | 241 | 0 | Output Voltage MSB |
| RO | 242 | 0 | Output Current LSB |
| RO | 243 | 0 | Output Current MSB |
| RO | 244 | 0 | T1 Temperature LSB |
| RO | 245 | 0 | T1 Temperature MSB |
| RO | 246 | 0 | T2 Temperature LSB |
| RO | 247 | 0 | T2 Temperature MSB |
| RO | 248 | 0 | F1 Speed LSB |
| RO | 249 | 0 | F1 Speed MSB |
| RO | 250 | 0 | Peak Input Current LSB |
| RO | 251 | 0 | Peak Input Current MSB |
| RO | 252 | 0 | Peak Output Current LSB |
| RO | 253 | 0 | Peak Output Current MSB |
| RO | 254 | 0 | PS Control LSB |
| RO | 255 | 0 | PS Control MSB |

12.4.12 Commands

The User Application (UA) shall allow additional functionality via PS Command Register.

### 12.4.12.1 PS Command (Register 0x5E)

PS Command register, address 0x5E, describes additional commands that can be accessed by the host system. These commands utilize the Firmware Command Protocol defined in section 12.2.4. For this power supply, the required features are listed below:

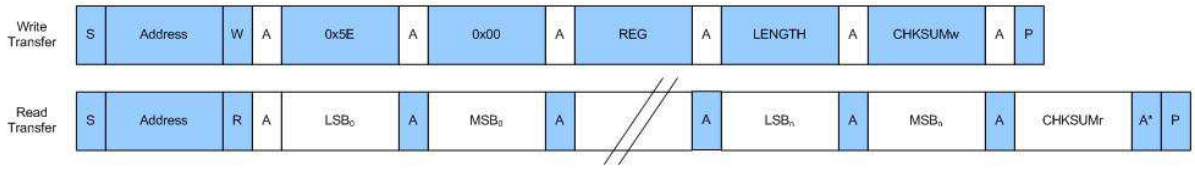
**0x00 – Consecutive Read Command**

The consecutive read command shall allow the system to read multiple registers in a single i2c transaction. The system shall specify a starting register and a length of registers to read. The length shall be less than or equal to 15. The power supply shall respond with an error where all bytes are equal to 0xFA if an error occurs. Some possible error cases are listed below. Register access shall follow standard procedures for accessing undefined or odd register addresses. On a successful command receipt, the power supply shall respond with the requested register words, LSB followed by MSB, for the starting register and the following consecutive registers, up to the total number of requested registers. The final byte of the read transfer shall be the checksum for all preceding data bytes (LSB0 to MSBn).

**Possible error cases:**

- Length equal to 0 (Expected response: 1 word 0xFAFA data)
- Length greater than 15 (Expected response: 15 words 0xFAFA data)
- Too few/many arguments
- Start address plus Length is greater than 0xFF
- Invalid checksum

**FIGURE 23 – TYPICAL CONSECUTIVE READ COMMAND**



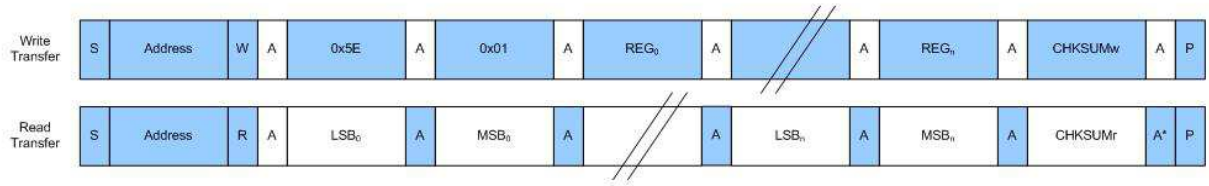

**0x01 – Custom Read Command**

The custom read command shall allow the system to read multiple registers in a single i2c transaction. The system shall specify a list of registers desired. The list shall include less than or equal to 15 registers. The power supply shall respond with an error where all bytes are equal to 0xFA if an error occurs. Some possible error cases are listed below. Register access shall follow standard procedures for accessing undefined or odd register addresses. On a successful command receipt, the power supply shall respond with the requested register words as LSB followed by MSB for each register in the specified order. The final byte of the read transfer shall be the checksum for all preceding data bytes (LSB0 to MSBn).

**Possible error cases:**

- Fewer than 1 registers requested (Expected response: 1 word 0xFAFA data)
- Greater than 15 registers requested (Expected response: 15 words 0xFAFA data)
- Invalid checksum

**FIGURE 24 – TYPICAL CUSTOM READ COMMAND**



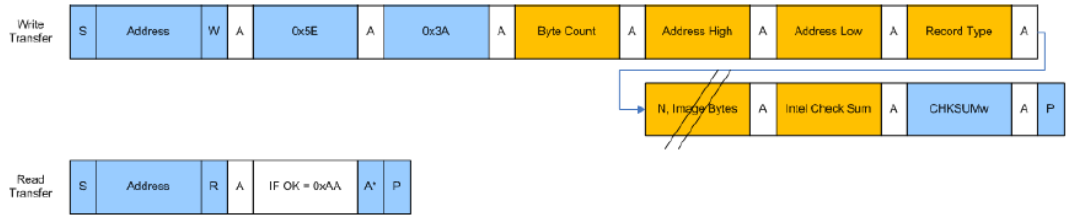

**0x02-0x39 – Reserved**

Commands 0x02 to 0x39 are reserved and undefined. Undefined commands shall respond with an error where all bytes are equal to 0x55.

**0x3A – Receive Staged Image Command**

The Receive Staged Image Command will be used to write a new main firmware image from the system to be staged in the power supply. This command shall be unlocked via the Bootloader Command (0xFF). When locked, the power supply should respond with an error code of 0xFA. The default state upon boot up shall be locked. When unlocked, the system shall send the new image as a single line of the Intel HEX format including the byte count, address, record type, data, and checksum. If a valid line of code is received (as indicated by both the Intel and LiteON checksums), the power supply shall respond with data 0xAA. If any byte is invalid or the Intel or LiteON checksums do not match the expected values, a failure shall be indicated by 0xFA as data. Any other value shall indicate an unknown error occurred. Refer to Section 13 for additional information on the bootloader function.

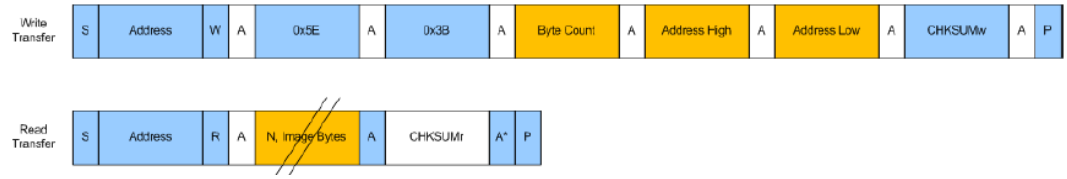
**FIGURE 25 – TYPICAL RECEIVE STAGED IMAGE COMMAND**




**0x3B – Transmit Staged Image Command**

The Transmit Staged Image Command will be used to read a staged main firmware image from the power supply to the system. The system shall write a byte length and an address. The power supply shall then return the requested bytes stored for the requested memory address. Data shall be returned corresponding to the same address as received via command 0x3A. If the requested byte count is greater than 16 (0x10) or the checksum does not match the expected value, a failure shall be indicated by 0xFA as data. Any other value shall indicate an unknown error occurred. Refer to Section 13 for additional information on the bootloader function.

**FIGURE 26 – TYPICAL TRANSMIT STAGED IMAGE COMMAND**



**0x3C – Initiate Bootload Command**

The Initiate Bootload Command shall be used to initiate the bootload process from the external staged firmware image. This command shall be unlocked via the Bootloader Command (0xFF). When locked, the power supply should respond with an error code of 0xFA. The default state upon boot shall be locked. When unlocked, the system shall send a two byte data sequence equal to 0x4850. If the system sends the correct data, the micro shall indicate success (0x31 as DATA) and then transition to the boot image, initiate the flash process from the external staged main image, and boot into the new image. If an error occurs in the flash process and the new main image does not pass the vendor specified checks, the micro shall start up in the backup image. If the specified two byte data sequence does not match, then the micro shall indicate failure (0x55 as DATA) and NOT transition to the boot image.

**0x3D – Verify Staged Image Command**

The Verify Staged Image Command shall be used to verify the staged main image checksum using vendor specific algorithms. Upon receipt of a successful verify command, the power supply shall indicate success (0x31 as DATA) and immediately change the status of the checksum OK bits in register 0x60 to indicate the verification was requested and not yet completed. If an error occurs in the transmission, then the micro shall indicate failure (0x55 as DATA) and not change the status of the checksum OK bits. Once the verification is completed, the micro shall update the checksum OK bits to indicate the status of the staged main image.

**0x3E-0xDF – Reserved**

Commands 0x3E to 0xDF are reserved and undefined. Undefined commands shall respond with an error containing two bytes of 0x55 data.

**0xE0-0xEF – Vendor Commands**

Commands 0xE0 to 0xEF are reserved for vendor specific definitions. These commands shall be used for passive purposes of returning data and shall not modify the operation of the power supply in any way. The response to these commands is not defined for use by the system. Removal of these commands at production is not required. The vendor shall provide detailed documentation to LiteON for any command used. All unused commands shall be considered reserved and shall respond with an error containing two bytes of 0x55 data.

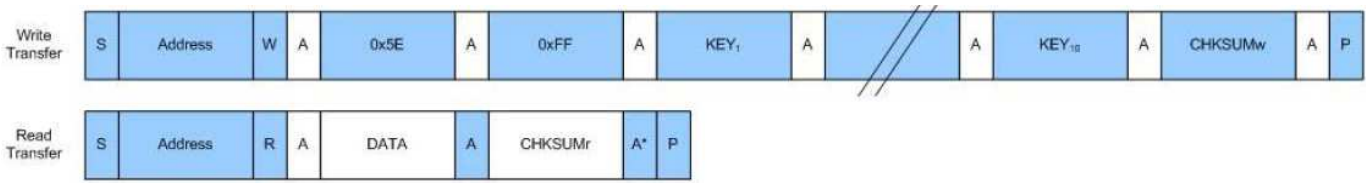
**0xF0-0xFE – Reserved Commands**

0xF0 to 0xFE are reserved and undefined. Undefined commands shall respond with an error containing two bytes of 0x55 data.

**0xFF – Bootloader Unlock Command**

The bootloader command shall allow the system to unlock commands 0x3A and 0x3C. The system shall send a key consisting of 6 data bytes. The key data bytes shall contain reference information for what type of code is being sent by the system. Key bytes shall be pre-defined by the microcontroller. See the key definition and further information on the bootloader in section 13. If the system sends a matching set of key bytes to the micro, then it shall indicate success (0x31 as DATA) and commands 0x3A and 0x3C shall be unlocked. If ANY of the key bytes do not match, then the micro shall indicate failure (0x55 as DATA) and commands 0x3A and 0x3C shall be locked.

**FIGURE 27 – TYPICAL BOOTLOADER COMMAND**




## 13. BOOTLOADER

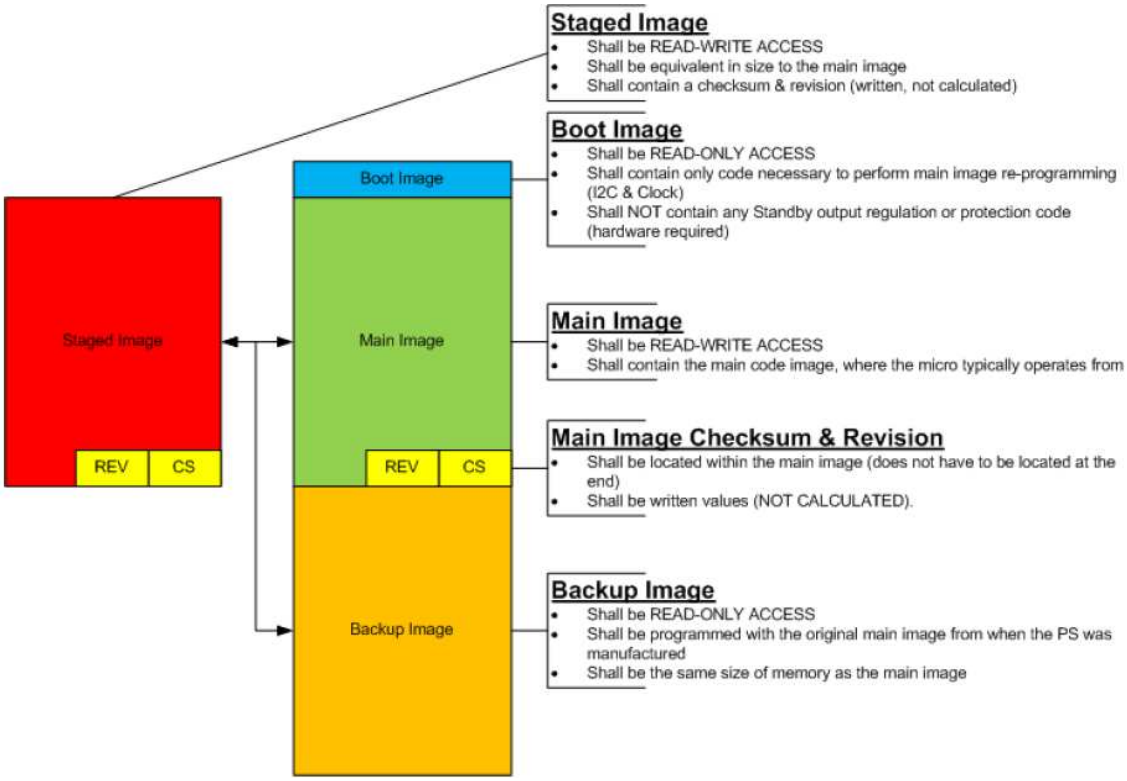
This section contains microcontroller bootloader to system interface protocol requirements through I2C data and I2C clock signals.

### 13.1 BLOCK DIAGRAM

13.1.1 Memory Map

#### 13.1.1.1 Overview

**FIGURE 28 – MICROCONTROLLER MEMORY MAP**




13.1.2 Boot Image

The boot image shall be read-only access. It shall contain only the code necessary to perform main image re-programming. It shall NOT contain any code required for the standby output regulation or protection functions. The standby output must be capable of operation, control, and protection without the assistance of the microcontroller and must remain within regulation requirements throughout the bootload process.

The boot image shall automatically initiate re-programming of the main image with new code stored in the staged image. The boot image shall be capable of managing the flash process while responding to I2C transactions. The boot image shall implement appropriate protections to ensure the flash process can be performed successfully.

The boot image shall contain pointers to the main and staged image checksums and revisions. It shall continuously provide access to the checksums and revisions in the respective checksum and revision registers. It shall NOT continuously calculate or verify the checksums.

Upon completion of the flash process, the boot image shall contain a vendor specific algorithm to determine the calculated checksum of the new main image. The calculated checksum shall then be compared to the main image checksum. If the result of this verification is passed, it shall automatically switch to the main image; otherwise it shall automatically switch to the backup image.

13.1.3 Main Image

The main image shall be read-write access. It shall contain the main code image that is the primary location in which the micro attempts to operate. It shall not include any references from the backup image or the boot image. It shall contain the commands necessary to switch to the boot image, including disabling the main output. It shall NOT contain commands to switch to the backup image.

The main image shall contain a checksum within its memory space. The main image checksum shall uniquely identify the main FW image. The main image shall contain a major and minor FW revision register. This register shall be incremented whenever a new main image is released. At product release, the FW revision shall be 0x0100.

13.1.4 Backup Image

The backup image shall be read-only access. It shall contain the backup code image that is the secondary location that the micro attempts to operate ONLY when the main image is not valid. It shall not include any references from the main image or the boot image. It shall contain the commands necessary to switch to the boot image, including disabling the main output. It shall NOT contain commands to switch directly to the main image.

The backup image shall be identical to the main image at the time of production. The backup image shall be identical in memory size to the main image.

13.1.5 Staged Image

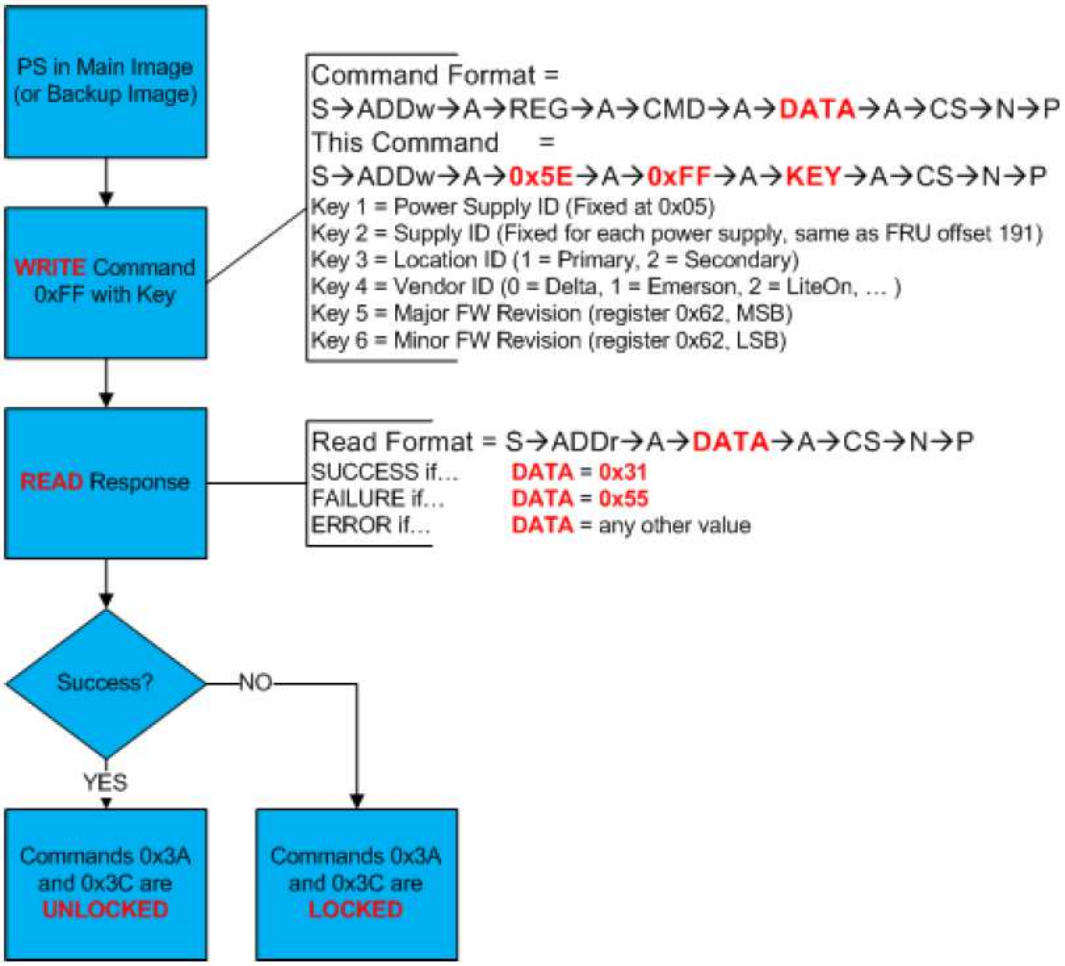
The staged image shall be an external EEPROM with read-write access ONLY accessible through the main or backup image. The staged image shall be identical in memory size to the main image.

The staged image shall contain a checksum and revision within its memory space. The staged image checksum and revision shall uniquely identify the staged FW image.

## 13.2 PROTOCOLS

### 13.2.1 Unlock Protocol

**FIGURE 29 – UNLOCK BOOTLOADER COMMANDS**




If the micro is in the main or backup image, it shall contain a command that unlocks the bootloader commands and allows new code to be staged in an external memory device and enables the transition to the boot image. The command register (0x5E) shall contain the command 0xFF which is followed by 6 “KEY” data bytes. The KEY data bytes shall contain reference information for what type of code is being sent by the system. Key bytes shall be pre-defined by the microcontroller. If the system sends a matching set of key bytes to the micro, then it shall indicate success (0x31) and unlock the remaining bootloader commands and update the command status (bit 4 of image status register 0x60). If ANY of the key bytes do not match, then the micro shall indicate failure (0x55) and NOT unlock the bootloader commands. The bootloader commands shall expire and return to a locked state after a successful Initiate Bootload command is received or after 30 minutes have elapsed.

The 1st key byte shall be the PS ID. This value shall be fixed at 0x05.

The 2nd key byte shall be the Supply ID. This shall correspond to data at offset 191 of the FRU EEPROM, indicating the type of power supply. This value shall be fixed for each power supply.

The 3rd key byte shall be the Location ID. This shall identify the location of the micro within the power supply. Data 0x01 shall indicate the primary side, data 0x02 shall indicate the secondary side, and all other values shall be reserved.

The 4th key byte shall be the Vendor ID. This shall correspond to data at bits 5-3 of the PS Status Register (0x02), indicating the vendor of the power supply.

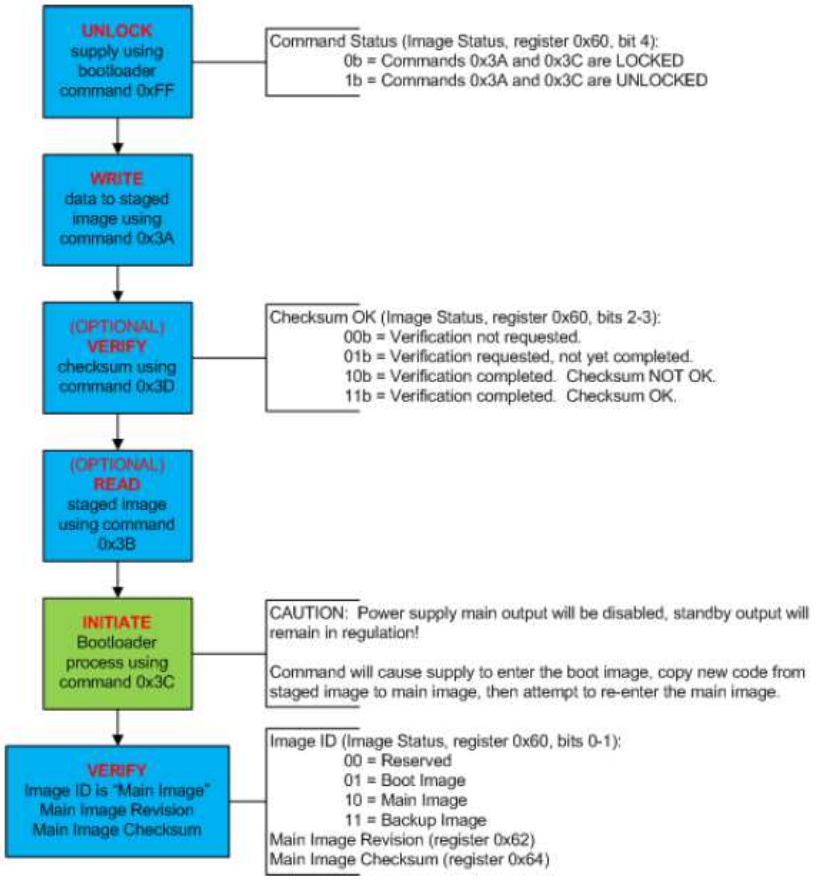
- **0x02 = LiteOn;**
- All other values are reserved

The 5th key byte shall be the Major FW Revision Number. This shall correspond to data at bits 8-F of the Main Image Revision register (0x62), indicating the Major FW revision of the power supply.

The 6th key byte shall be the Minor FW Revision Number. This shall correspond to data at bits 0-7 of the Main Image Revision register (0x62), indicating the Minor FW revision of the power supply.

### 13.2.2 Bootloader Protocol

**FIGURE 30 – BOOTLOADER PROTOCOL FLOWCHART**



To initiate the bootloader process, the system must unlock commands 0x3A and 0x3C as described in section 13.2.1. Once unlocked, the system can write a new firmware image to the power supply via the Receive Staged Image Command described in section 12.4.12.1. The system may also optionally verify the staged image checksum via the Verify Staged Image Command (0x3D) or read back the staged image via the Transmit Staged Image Command (0x3B), also described in section 12.4.12.1.

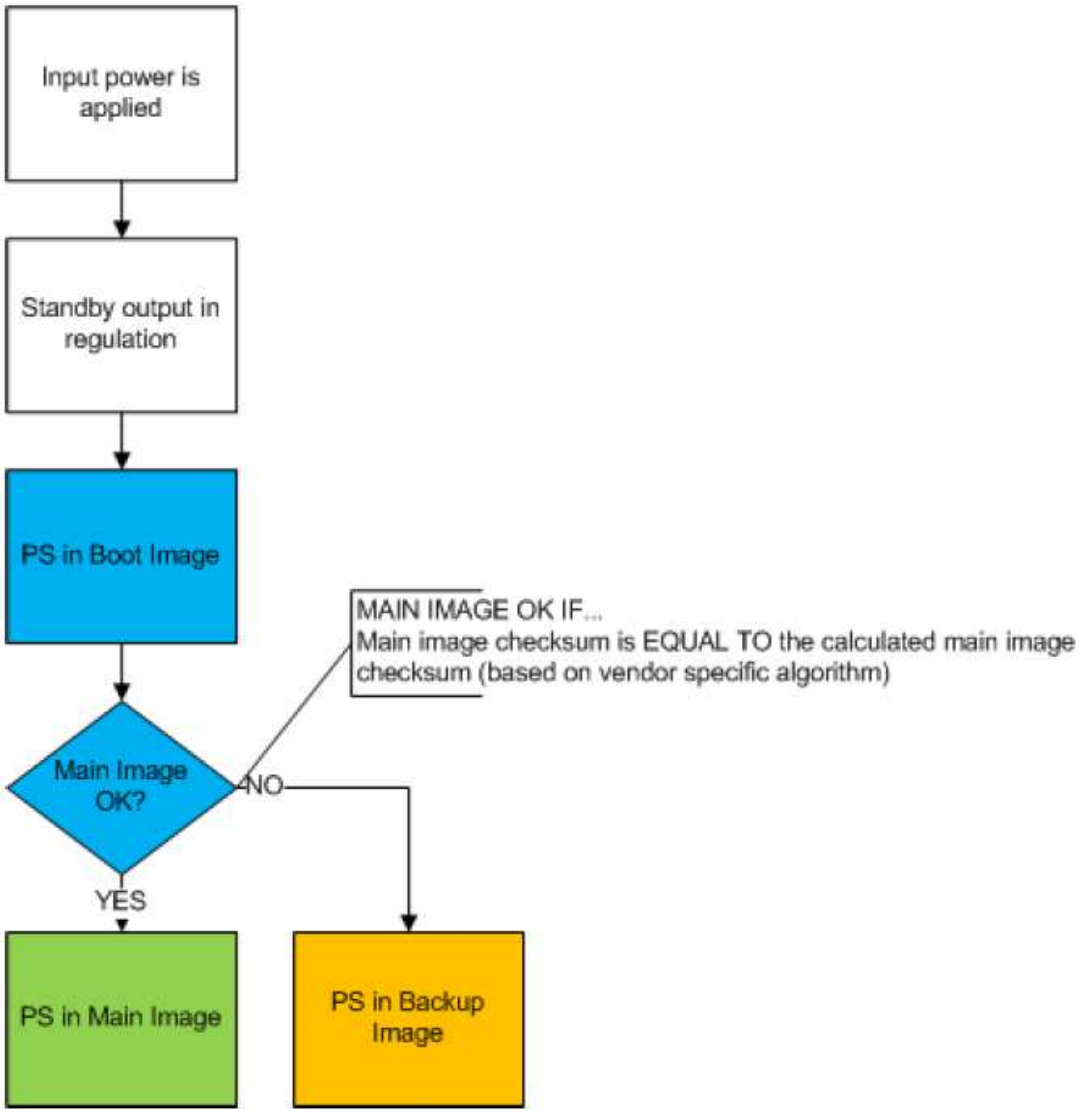
The system will send command 0x3C, the Initiate Bootload Command, to begin the reflashing process. The system shall read the response from the power supply, after which the power supply will shut down its main output and transition to the boot image. The standby output must remain within regulation requirements. The power supply shall then automatically initiate the re-programming process, replacing the current main image with the staged image. Once the main image has been fully re-programmed, the power supply shall verify the new main image and transition into the main image if the verification passes. If the main image verification fails, the power supply shall transition to the backup image.

The system shall verify that the bootloader process was successful by comparing the Image ID bits of the Image Status register and Main Image Revision and Checksum registers to the expected values. If the Image ID bits indicate that the power supply is operating in the Main Image and the Main Image Revision and Checksum registers match the expected values, the process was successful. If the Image ID bits indicate that the power supply is operating in the Backup Image or the Main Image Revision and Checksum registers do not match the expected values, the process was unsuccessful and the system must begin the process again. If the Image ID bits indicate that the power supply is operating in the Boot Image, the process has not yet completed.

*NOTE: IF THE POWER SUPPLY HAS BEEN IN THE BOOT IMAGE FOR 10 MINUTES, IT SHALL AUTOMATICALLY START VERIFICATION OF THE MAIN IMAGE AND SWITCH TO THE MAIN IMAGE OR BACKUP IMAGE ACCORDINGLY.

13.2.3 Startup Protocol

**FIGURE 31 – STARTUP FLOWCHART**




At startup, the power supply shall default to the boot image and immediately process the main image. The main image checksum shall uniquely identify the main FW image. The boot image may also perform additional vendor specific algorithms to validate the main image. If BOTH the checksum and vendor specific algorithms pass, then the micro shall switch to the main image. If EITHER the checksum or the vendor specific algorithms fail, then the micro shall switch to the backup image.

## 13.3 REGISTER SET

### 13.3.1 Register Set

**TABLE 45 – MICROCONTROLLER REGISTERS**

| Register Name | Register Address | Description | Bit(s) Number | Access | Default Value |
|---|---|---|---|---|---|
| RESERVED | 0x00 – 0x5E | | | RO | 0x0000 |
| Image Status | 0x60 | Image ID | 0 – 1 | RO | |
| | | Checksum OK | 2 – 3 | | |
| | | Command Status | 4 | | |
| | | Reserved | 5 – F | | |
| Main Image Revision | 0x62 | Minor FW Revision Number | 0 – 7 | RO | |
| | | Major FW Revision Number | 8 – F | | |
| Main Image Checksum | 0x64 | | | RO | |
| Staged Image Revision | 0x66 | Minor FW Revision Number | 0 – 7 | RO | |
| | | Major FW Revision Number | 8 – F | | |
| Staged Image Checksum | 0x68 | | | RO | |
| RESERVED | 0x6A – 0xFE | | | RO | 0x0000 |

### 13.3.2 Register Definitions

#### 13.3.2.1 Image Status (Register 0x60) <AVAILABLE IN ALL IMAGES>

This register shall indicate which image the micro is operating and the status of the staged image checksum.

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | | | | | |
| Definition | RESERVED | | | CMD STATUS | CHECKSUM OK | | Image ID | |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Definition | RESERVED | | | | | | | |

| Bits | Description |
|---|---|
| F – 5 | Reserved bits. Must return zero when read. |
| 4 | Command Status<br>• 0b = Commands 0x3A and 0x3C locked.<br>• 1b = Commands 0x3A and 0x3C unlocked. |
| 3 - 2 | Checksum OK<br>• 00b = Verification not requested.<br>• 01b = Verification requested, not yet completed.<br>• 10b = Verification completed. Checksum NOT OK.<br>• 11b = Verification completed. Checksum OK.<br><br>These bits shall indicate the status of the staged image checksum and shall be reset when<br>• System attempts to write new code via Receive Staged Image Command, OR<br>• Micro attempts to switch from boot image to main image, OR<br>• Verify command is sent from the host system, OR<br>• Input power is removed. |

| Bits | Description |
|---|---|
| 1 – 0 | Image ID<br>• 00 = Reserved<br>• 01 = Boot Image<br>• 10 = Main Image<br>• 11 = Backup Image<br><br>This bit shall indicate which image is micro is currently operating from. |

#### 13.3.2.2 Main Image Revision (Register 0x62) <AVAILABLE IN ALL IMAGES>

This register shall indicate the main image revision. The MSB shall correlate to the major FW revision. The LSB shall correlate to the minor FW revision, and shall be incremented by the PS vendor upon release. At production release, the FW revision shall begin at 0x0100 (rev 1.0). The main image revision values of 0x0000 and 0xFFFF are invalid. The Main Image Revision shall be a static value written as part of the code image.

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | | | | | | | | |
| Definition | Minor FW Revision | | | | | | | |
| **Bit #** | **F** | **E** | **D** | **C** | **B** | **A** | **9** | **8** |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | | | | | | | | |
| Definition | Major FW Revision | | | | | | | |

| Bits | Description |
|---|---|
| F – 8 | Major FW Revision. This revision shall correlate to the FW revision of the main image. |
| 7 – 0 | Minor FW Revision. This revision shall correlate to the FW revision of the main image. |

#### 13.3.2.3 Main Image Checksum (Register 0x64) <AVAILABLE IN ALL IMAGES>

This register shall indicate the main image checksum. The main image checksum shall uniquely identify the main FW image. To prevent issues with default micro image values, the main image checksum values of 0x0000 and 0xFFFF are invalid. If the vendor compiles the main image and observes an invalid checksum, they shall update the code with an offset to prevent this occurrence. The location of the checksum in the main image and the algorithm to verify the checksum shall be vendor specific. The Main Image Checksum shall be a static value written as part of the code image.

#### 13.3.2.4 Staged Image Revision (Register 0x66) <AVAILABLE IN ALL IMAGES>

This register shall indicate the staged image revision. The MSB shall correlate to the major FW revision. The LSB shall correlate to the minor FW revision. The Staged Image Revision shall be a static value written as part of the code image.

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Default Value | | | | | | | | |
| Definition | Minor FW Revision | | | | | | | |

| Bit # | F | E | D | C | B | A | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access | R O | RO | RO | RO | RO | RO | RO | RO |
| Default Value | | | | | | | | |
| Definition | Major FW Revision | | | | | | | |

| Bits | Description |
|---|---|
| F – 8 | Major FW Revision. This revision shall correlate to the FW revision of the main image. |
| 7 – 0 | Minor FW Revision. This revision shall correlate to the FW revision of the main image. |

#### 13.3.2.5 Staged Image Checksum (Register 0x68) <AVAILABLE IN ALL IMAGES>

This register shall indicate the staged image checksum which shall uniquely identify the staged FW image. The Staged Image Checksum shall be a static value written as part of the code image.