SIMON FRASER UNIVERSITY
School of Mechatronic Systems Engineering
MSE 352 Digital Logic and Microcontrollers
Quiz IV (**Time 15 minutes**) – Fall 2015

Student Full Name:_____

Student Number :_____

Trace the following assembly program and state the values **(in hex)** of the core registers R0, R1 and R2 when any of their contents change.

R0	R1	R2

LDR	Load
BL	Long branch with link
MOV	Move
ORR	Logical OR
CMP	Compare
BEQ	Branch if Equal
LSL	Logical Shift Left
LSR	Logical Shift Right
ORR	Logical OR
AND	Logical AND
B	Branch

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```
1        .thumb
2        .text
3        .align  2
4
5        .global main
6
7  main: .asmfunc
8
9      LDR R0, FIFTHSEC                ; R0 = FIFTHSEC (delay 0.2 second)
10     BL  delay                       ; delay at least (3*R0) cycles
11
12     MOV R0, #0x3B
13     MOV R1, #0x00
14     MOV R2, #0x00
15     AND R1,R0,#0x55
16     LSL R1,R1,#1
17     AND R2,R0,#0xAA
18     LSR R2,R2,#1
19     ORR R0,R1,R2
20     MOV R1, #0x00
21     MOV R2, #0x00
22     AND R1,R0,#0x33
23     LSL R1,R1,#2
24     AND R2,R0,#0xCC
25     LSR R2,R2,#2
26     ORR R0,R1,R2
27     MOV R1, #0x00
28     MOV R2, #0x00
29     AND R1,R0,#0x0F
30     LSL R1,R1,#4
31     AND R2,R0,#0xF0
32     LSR R2,R2,#4
33     ORR R0,R1,R2
34
35 loop
36     B   loop
37     .endasmfunc
38
39 ;------------delay------------
40 ; Delay function for testing, which delays about 3*count cycles.
41 ; Input: R0  count
42 ; Output: none
43 ONESEC              .field 5333333,32      ; approximately 1s delay at ~16 MHz clock
44 QUARTERSEC         .field 1333333,32      ; approximately 0.25s delay at ~16 MHz clock
45 FIFTHSEC           .field 1066666,32      ; approximately 0.2s delay at ~16 MHz clock
46 delay:  .asmfunc
47     SUBS R0, R0, #1                 ; R0 = R0 - 1 (count = count - 1)
48     BNE delay                       ; if count (R0) != 0, skip to 'delay'
49     BX  LR                          ; return
50     .endasmfunc
51
52 .end
```