MSE 352: Digital Logic and Microcontrollers

Chapter 4
Combinational Logic

Mohammad Narimani
School of Mechatronic Systems Engineering
Simon Fraser University

Introduction

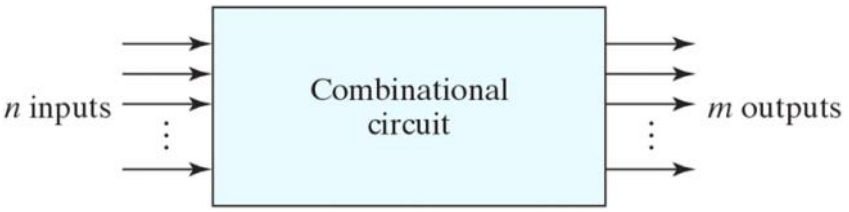
September 25, 2018 3:12 PM

Combinational Logic:

Logic circuits for digital systems are categorized as :

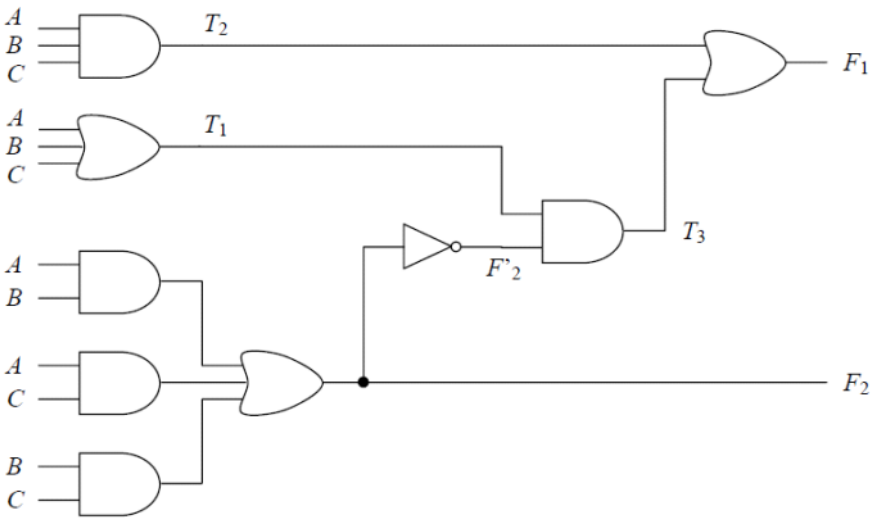
A combinational circuit consists of logic gates whose outputs at any time are determined from only the …

A sequential circuits employ storage elements in addition to logic gates. Their outputs are a function of the …



The diagram of a combinational circuit has logic gates with no feedback paths or memory elements.

As an example, consider the following combinational circuit with 3 inputs and 2 outputs ($n = 3, m = 2$):



Design Procedure

September 25, 2018 3:35 PM

The design of combinational circuits starts from the specification of the design objective and then creating Boolean functions than can be realized using logic gates including in the following steps:

1. From a circuit specifications, determine the required number of inputs and outputs and assign a symbol to each.

2. Derive the truth table that defines the required relationship between inputs and outputs.

3. Obtain the simplified Boolean functions for each output as a function of the input variables.

4. Draw the logic diagram and verify the correctness of the design (manually or by simulation).

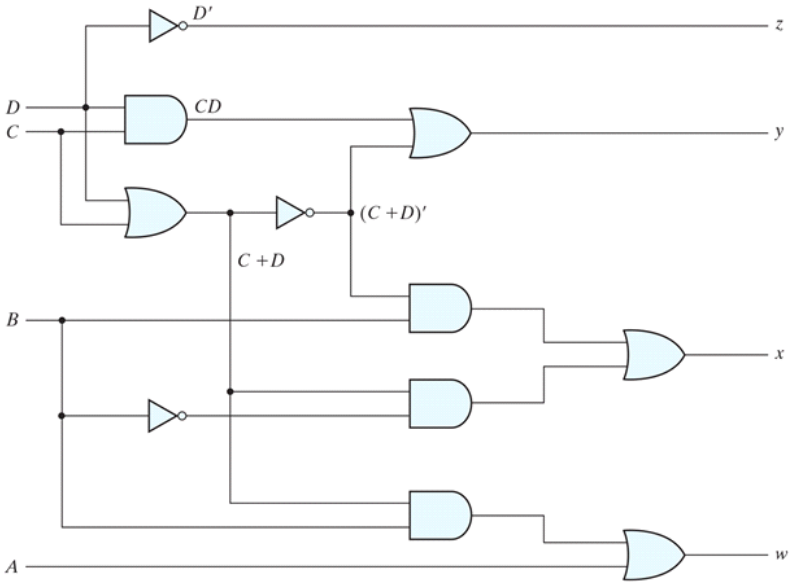
Design Procedure- Cont'd

September 25, 2018 3:47 PM

Example: Convert a BCD code to Excess-3 code

Input BCD				Output Excess-3 Code			
A_3	A_2	A_1	A_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Truth Table for Code Conversion Example


D′
z
D
C
CD
y
(C + D)′
C + D
B
x
A
w

Binary Adder–Subtractor

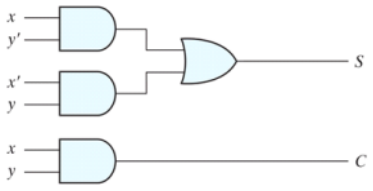
September 25, 2018 3:49 PM

A binary adder–subtractor is a combinational circuit that performs the arithmetic operations of addition and subtraction with binary numbers.

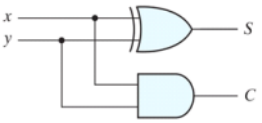
This circuit is developed using a hierarchical design.

Half Adder:

x	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



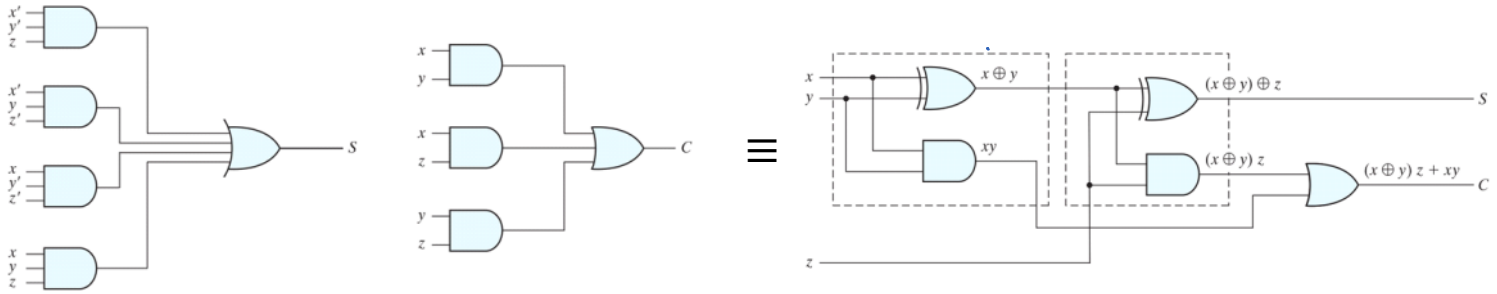
(a) $S = xy' + x'y$
$C = xy$



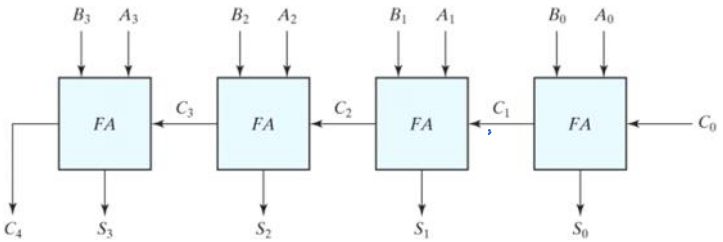
(b) $S = x \oplus y$
$C = xy$

Full Adder:

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



4-bit Full Adder:



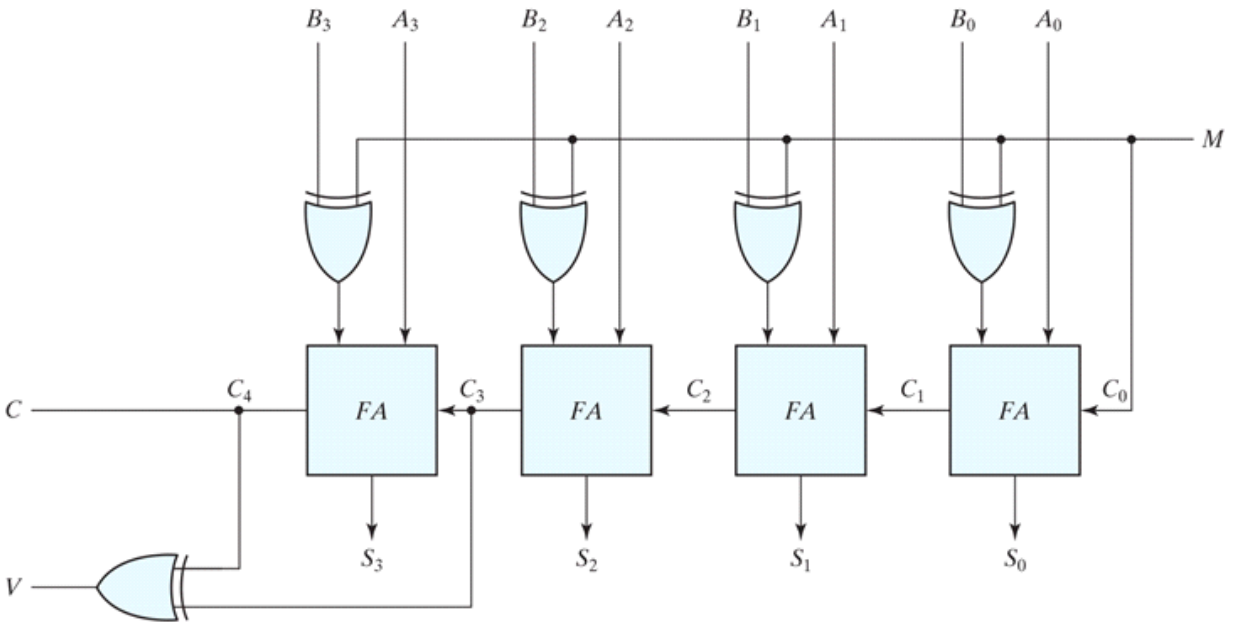
Subscript *i*:	**3**	**2**	**1**	**0**	
Input carry	0	1	1	0	C_i
Augend	1	0	1	1	A_i
Addend	0	0	1	1	B_i
Sum	1	1	1	0	S_i
Output carry	0	0	1	1	C_{i+1}

Binary Adder–Subtractor - Cont'd

September 25, 2018 4:00 PM

Binary Subtractor:

- The subtraction $A - B$ can be done by taking the 2's complement of B and adding it to A.
- The 2's complement can be obtained by taking the 1's complement and adding 1 to the least significant pair of bits.
- The 1's complement can be implemented with inverters, and a 1 can be added to the sum through the input carry



Other Combinational Circuits

Thursday, September 27, 2018 12:42 PM

- BCD Adder
- Binary Multiplier
- Magnitude Comparator

Decoders

Thursday, September 27, 2018 12:47 PM

In digital systems, discrete quantities are represented by binary codes.
For example, with 3 bits one can show maximum 8 discrete values.

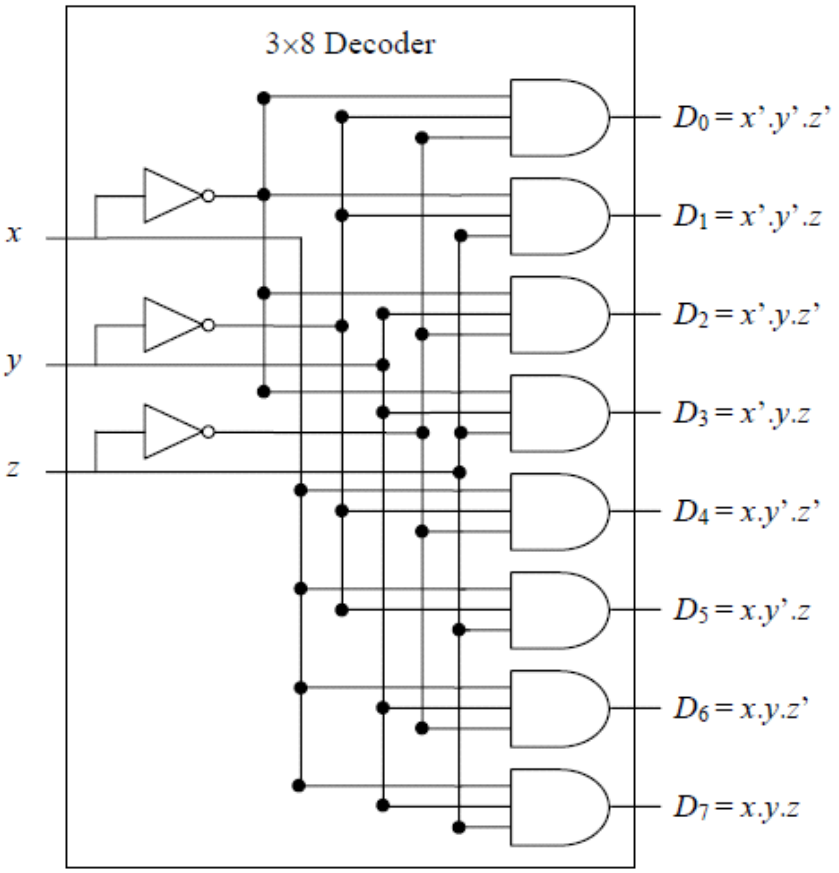
- Decoder circuits are used to decode encoded information.

- A decoder is a combinational circuit that has n inputs and a maximum of 2^n outputs.

- The truth table for a 3-to-8-line decoder is as follows:

Inputs			Outputs							
x	y	z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

- The logic circuit for this decoder is shown in the following figure, where each output represents one of the minterms.


3×8 Decoder
x
y
z
D0 = x'.y'.z'
D1 = x'.y'.z
D2 = x'.y.z'
D3 = x'.y.z
D4 = x.y'.z'
D5 = x.y'.z
D6 = x.y.z'
D7 = x.y.z

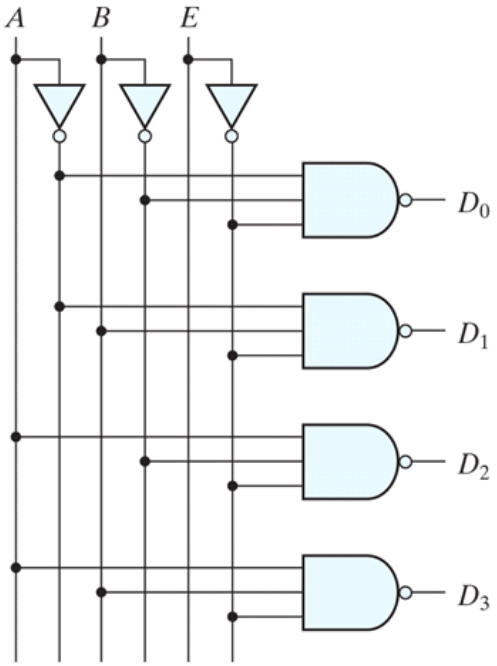
Decoders -Cont'd

Thursday, September 27, 2018 1:14 PM

Implementation of Decoders with NAND gates and enable input:

- Some decoders are constructed with NAND gates. In this case a decoder generates complemented outputs.

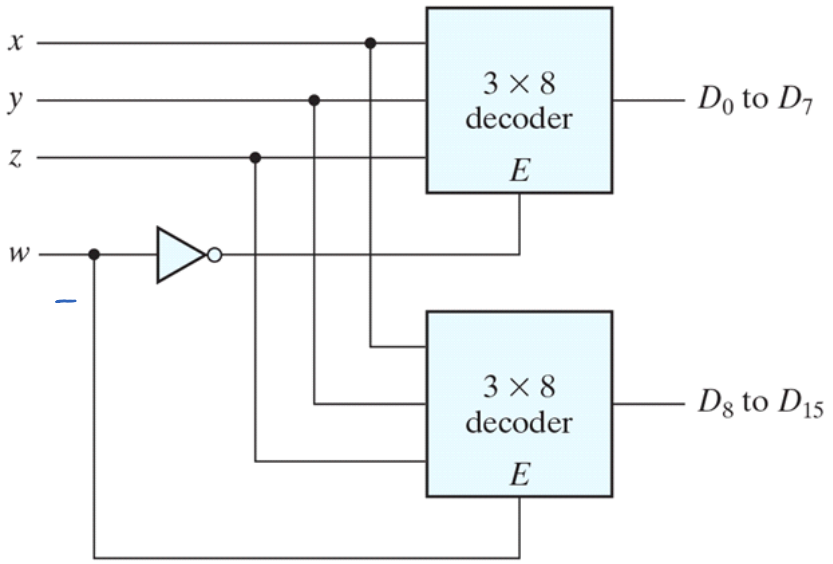
- To control the operation of the circuit (decoder), an "enable inputs" are often used in the decoders



E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

- One can connect multiple decoders with enable lines to build a decoder with a greater number of outputs.

- For example, two 3-to-8-line decoders with enable lines can be connected to construct a 4-to-16-line decoder as follows:



Combinational Logic Implementation

Thursday, September 27, 2018 1:43 PM

Any combinational circuit with n inputs and m outputs can be implemented with an n-to-2^n line decoder and m OR gates.

How?

1- A decoder with n inputs provides 2^n minterms (outputs), where each of them is associated with a unique pattern of input bits.

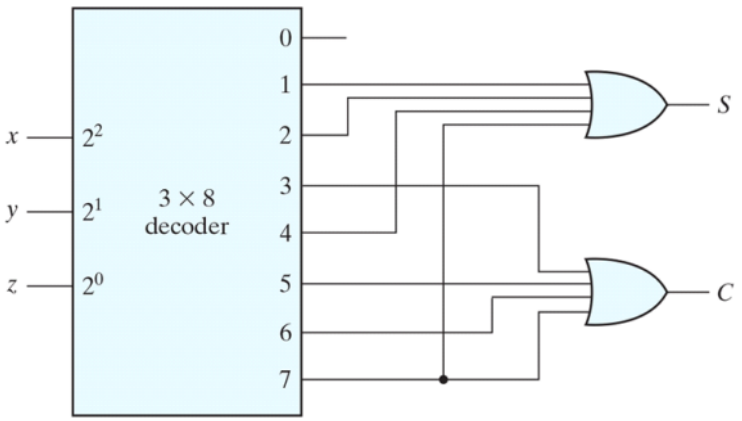
2- We learned in Chapter 3 that any Boolean function can be expressed in sum-of-minterms form.

3- Using an OR gate which combines the minterms which contribute to build a Boolean function, a hardware implementation of the function can be realized.

Example: A full adder can be implemented as follows:

$S(x, y, z) = \sum(1,2,4,7)$

$C(x, y, z) = \sum(3,5,6,7)$ =>



Encoders

Thursday, September 27, 2018 3:36 PM

- An encoder's operation is the inverse operation of a decoder.

- For example, an octal-to-binary encoder is given below:

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Truth Table of an Octal-to-Binary Encoder

The corresponding Boolean expressions are:

$$x = D_4 + D_5 + D_6 + D_7$$

$$y = D_2 + D_3 + D_6 + D_7$$

$$z = D_1 + D_3 + D_5 + D_7$$

Priority Encoder:

- In case more than one input is turned on simultaneously, an input priority must be established to guarantee that only one input is encoded.

Inputs				Outputs		
D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Truth Table of a Priority Encoder

- What is V?

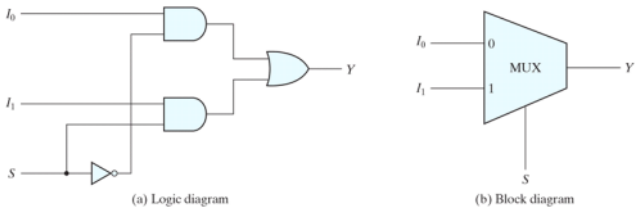
Multiplexer

Thursday, September 27, 2018 1:32 PM

A multiplexer or a *data selector* is a combinational circuit that chooses one of the signals connected to its input pins and reproduces the signal on this input at the output terminal.

Example:

A Two-to-one-line multiplexer is as follows:

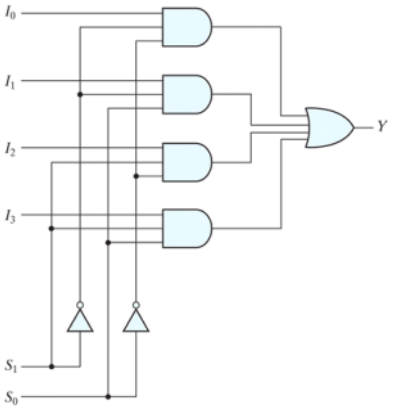


(a) Logic diagram (b) Block diagram

- I_0 and I_1 are the input lines, S is the selection line, and Y is the output.

Example:

A Four-to-one-line multiplexer is as follows:

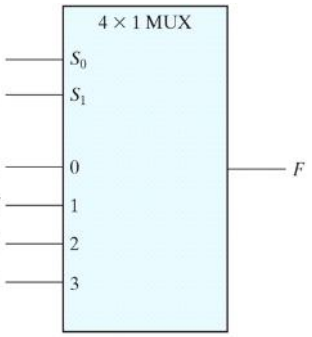


(a) Logic diagram

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(b) Function table

=>



Multiplexer - Cont'd

Thursday, September 27, 2018 4:23 PM

Implementation of a Boolean function using MUX:

- A multiplexer can be used to implement any Boolean function.

- The first $n-1$ variables will be used as selection inputs and the remaining variable together with its complement, 1, and 0 will be used to build data inputs.

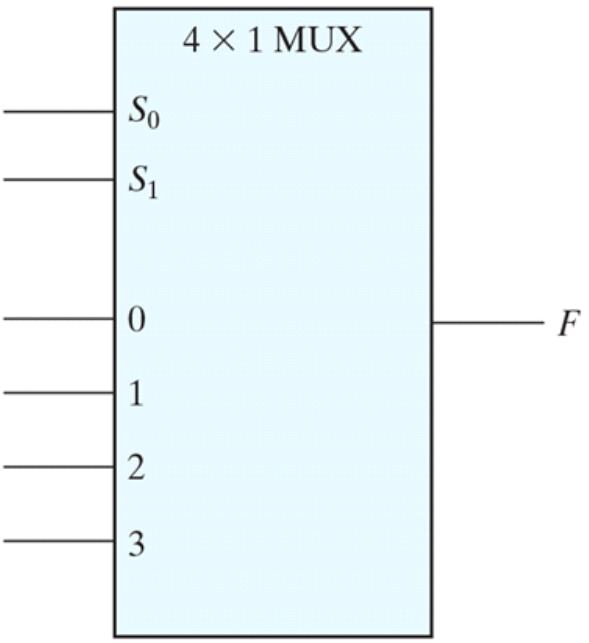
- Draw the corresponding truth table and for each pair of rows (2^{n-1} pair of rows) in the truth table, try to see if the corresponding function values are equal to 0, 1, the remaining variable in the input columns, or its complement.

Example:

Implement the following Boolean function using a 4×1 MUX.

$F(x, y, z) = \sum(1,2,6,7)$

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



Example:

Implement the following Boolean function using a proper MUX.

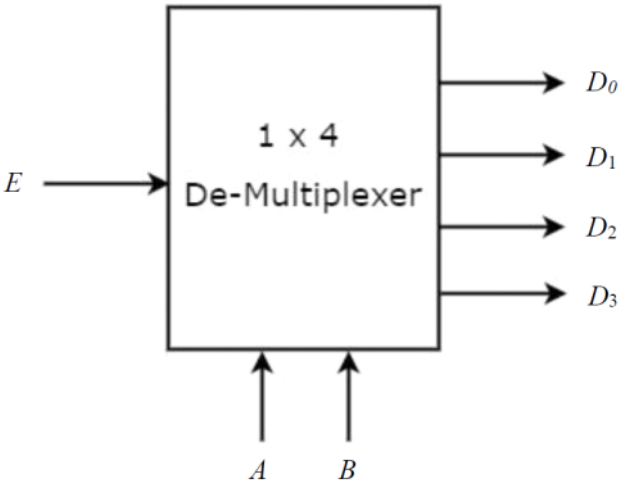
$F(w, x, y, z) = \sum(1,3,4,11,12,13,14,15)$

Demultiplexer

Thursday, September 27, 2018 4:46 PM

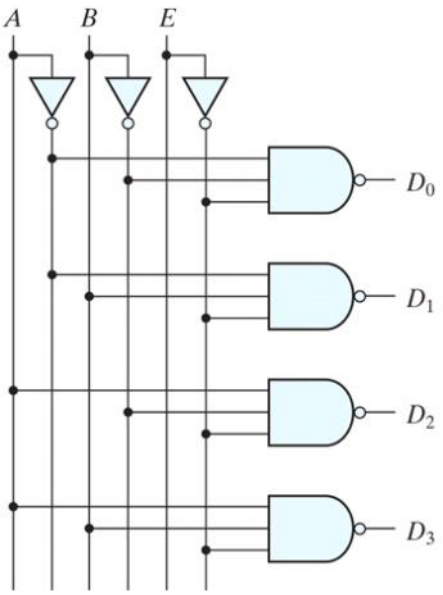
- A demultiplexer is a circuit that receives information from a single line and directs it to one of 2^n possible output lines.

- The selection of a specific output is controlled by the bit combination of n selection lines.



- Because decoder and demultiplexer operations are obtained from the same circuit, a decoder with an enable input is referred to as a decoder – demultiplexer

.



E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Three-state buffer

Thursday, September 27, 2018 4:49 PM

A digital circuits that exhibit three states.

- Two of the states are signals equivalent to logic 1 and logic 0 as in a conventional gate.

- The third state is a high-impedance state in which the logic behaves like an open circuit. As a result, the circuit connected to the output of the three-state gate is not affected by the inputs to the gate.