

# ELC 2137 Lab #3: Adders

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## Summary

To complete the Adders lab students were required to build and design logical circuits given the required outputs. In order to minimize both human and hardware error, it is imperative that students draw out each circuit with corresponding gates, LED's, GND, Voltage, and correct current flow through each path. By doing this student's are able to visualize the logical side of the circuits as well as catch any future mistakes that might occur throughout the lab. Once a diagram has been built, students were responsible for fulfilling a circuit with the desired outcome. By the end of the lab, students should be able to complete a functioning Full Adder, Two-Bit Adder, Half-Bit Adder on both papers and on a circuit board.

## Q&A

1. Which gates could we use for combining the carry bits?

Based on the truth table, a OR gate needs to be used for the carry bits. Only one carry needs to be true, the out carry will be true. It is an OR gate. The first and second carry are not true at same time, so an XOR gate is also fine.

2. Which one should we use and why?

A OR gate should be used in the lab, but XOR gate is also fine. In the lab, 7486 chip is used. The chip has four XOR gates. The carry1 and carry 2 are not true at the same time. It is true when one of the carry is true, so using a XOR will be identical as using OR gate.

## Results

In this section, put your simulation waveforms, results tables, pictures of hardware, and any other required items. According to the table above,

Table 1: 2-bit adder truth table

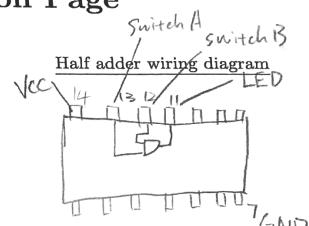
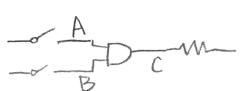
Cin	A	B	C1	C2	S1	S2	Cout	S
0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	1	0	1
0	1	0	0	0	1	1	0	1
0	1	1	1	0	0	0	1	0
1	0	0	0	0	0	1	0	1
1	0	1	0	1	1	0	1	0
1	1	0	0	1	1	0	1	0
1	1	1	1	0	0	1	1	1

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### Circuit Demonstration Page

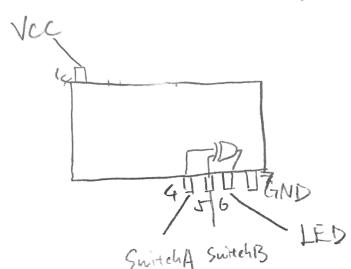
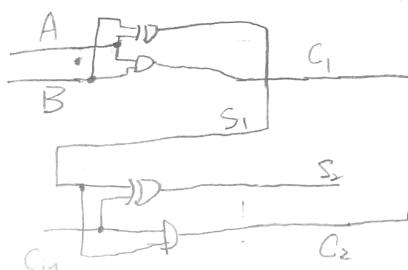
Half adder schematic



Half adder:

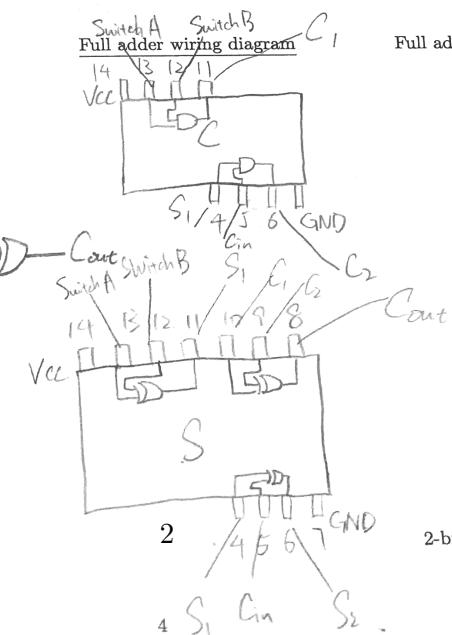
<u>BD</u>			
A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Full adder schematic



Full adder:

<u>DD</u>			
C <sub>1</sub>			
A	B	C <sub>in</sub>	C <sub>out</sub>
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



2-bit adder:

<u>BB</u>							
A <sub>1</sub>	B <sub>1</sub>	A <sub>0</sub>	B <sub>0</sub>	C <sub>in</sub>	C <sub>out</sub>	S <sub>1</sub>	S <sub>2</sub>
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	1	0	0	0	0	1	0
0	1	0	1	0	0	1	1
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	1	0	0	1	1	0	0
1	1	0	1	1	1	1	1
1	1	1	0	0	1	1	1
1	1	1	1	1	1	1	1

## Circuits

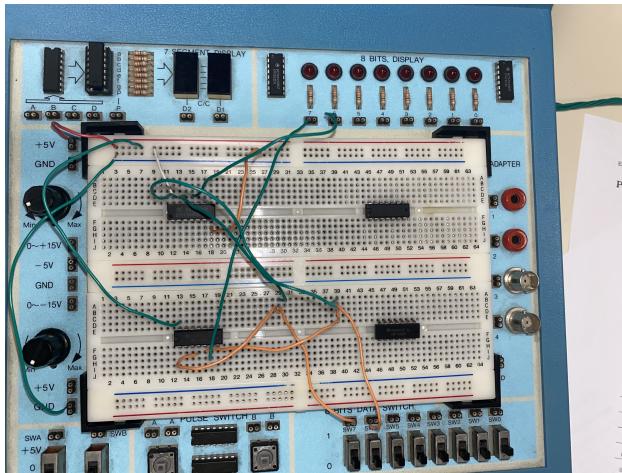


Figure 1: This is the half adder.

There is a lack of the full adder pictures, but the left half of the 2-bit adder is full adder circuit.

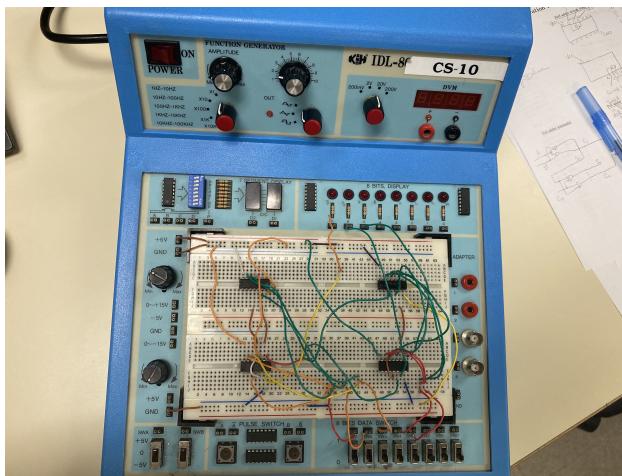


Figure 2: This is the 2-bit adder.

## Conclusion