Xingquan Li

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Dr.~Xingquan Li is an associate researcher at Pengcheng Laboratory (PCL). He received the Ph.D degree from Fuzhou University in 2018. His research interesting includes EDA and AI for EDA. His team has developed an Open-source infrastructure of EDA (iEDA). He has published over 50 papers in journals and conferences such as TCAD, TC, TVLSI, TODAES, DAC, ICCAD, DATE, ICCD, ASP-DAC, ISPD and has filed 13 invention patents. He has achieved first-place award from ICCAD@CAD Contest three times in 2017, 2018, and 2022. In 2020, he was honored with the Operational Research Application Award from the Chinese Operations Research Society. In 2023, he received the Best Paper Award from ISEDA.

Research Interest

- ☞ Electronic Design Automation (EDA), AI for EDA
- ☞ Machine Learning Optimization algorithm (ML-OPT)

Work Experience

- ➢ Associate Researcher, PhD supervisor, Pengcheng Laboratory, Department of Circuit and Systems, 2022.07- 2024.06
- ➢ Visiting Scholar, Pengcheng Laboratory, 2020.08-2022.07
- ➢ Associate Professor, Minnan Normal University, School of Mathematics and Statistics, 2019.07- 2024.06
- ➢ Lecturer, Minnan Normal University, School of Mathematics and Statistics, 2018.11-2019.07
- ➢ Teaching Assistant, Fuzhou University, Discrete Mathematics and Theor1etical Computer Research Center, 2015.10-2018.06

Educational Background

- ✧ Visiting Scholar, Pengcheng Laboratory, 2020.08-2022.07
  Research Subject: Open-source EDA platform, Co-supervisor: Prof. Yungang Bao
- ✧ Ph.D, Fuzhou University, Applied Mathematics, 2013.09-2018.06
  Doctoral Thesis: Research on map decomposition in integrated circuit manufacturing design, Excellent doctoral dissertation in Fujian Province, Advisor: Prof. Wenxing Zhu
- ✧ Bachelor Degree, Fuzhou University, Applied Mathematics, 2009.09-2013.06

Research Projects

- ➢ Ministry of Industry and Information Technology, 2023 Software Platform Open-source Digital Design Software Public Technology Service and Innovation Platform project, Open-source Digital Chip Design Automation Public Technology Service and Innovation Platform, No. 000645-23ZB0719/01, 2023-2025, Sub-project director

- Major Key Project of Pengcheng Laboratory, The key technology and basic design software of efficient computing network fusion chip, project No. PCL2023A03, 2023-2025, Sub-project director (intelligent P/EDA tool and technologies), project leader: Hanming Wu
- Major Key Project of Pengcheng Laboratory, Intelligent Core chip Design and core software of Network Communication, Project No. PCL2021A08, 2021-2023, participant, project leader: Shaohua Yu
- National Natural Science Foundation of China (Youth) Project, VLSI mixed-cell-high standard cell placement algorithm research for advanced process, project No. 61907024, 2019-2022, Host
- Natural Science Foundation of Fujian Province, VLSI mixed-cell-high standard cell placement algorithm research for advanced process, project No. 2020J05161, 2020-2023, Host

Representative Achievements

1) **Open-source EDA infrastructure and toolchain —— iEDA**

   iEDA is an Open-source EDA platform that can support the design from Netlist-to-GDS at 28nm process million gate chip. Including: 1) EDA infrastructure (such as database, file parser, GUI interaction system, evaluator and optimizer; 2) 11 EDA tools. iEDA is Open-source (https://github.com/OSCC-Project/iEDA). The results were published at the ISEDA conference and received the Best Paper Award.

2) **Intelligent EDA framework and package——AiEDA**

   AiEDA aims at building an intelligent EDA framework system and toolkit for AI for EDA field. It includes: 1) Labeled data system (supports data generation and feature extraction); 2) EDA tool interaction (supports two sets of commercial and Open-source EDA tools); 3) Supports EDA feature data analysis; 4) Supports AI + EDA model training and inference. This system has been used to train intelligent macro unit layout tasks, achieving better indicators than commercial tools on some chips.

3) **Open-source chip design flow——iFlow**

   This project built an Open-source iFlow (https://gitee.com/oscc-project/iFlow), supporting most Open-source tools, multiple process libraries and all chip designs. iFlow is used for 3 times tape-out: 1. February 2022 (700,000, 110nm process), returned in October, debugged in January 2023. 2. August 2022 (1.5 million door CPU chip, 110nm process), test successful. 3. January 2023 (1.5 million door CPU chip, 28nm process).

4) **The 3D chip design placement**

   Based on the study of the key technologies of digital chip design, considering complex factors. This work won the global first place in ICCAD @ Contest (2022 CAD Contest @ ICCAD, 3D Placement with D2D Vertical Connections, IEEE, ACM). The competition's solution has significant reference value for EDA practice and is crucial for improving 3D chip design quality.

Selected Papers

1. **Xingquan Li**, Ziran Zhu and Wenxing Zhu*, “Discrete relaxation method for triple patterning lithography layout decomposition,” *IEEE Transactions on Computers (TC)*, vol. 66, no. 2, pp. 285–298 (2017). **(CCF-A)**

2. **Xingquan Li** and Wenxing Zhu*, “Two-Stage Layout Decomposition for Hybrid E-Beam and Triple Patterning Lithography,” *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 23, no. 1 (2017). **(CCF-B)**

3. **Xingquan Li**, Jianli Chen and Wenxing Zhu*, “Discrete Relaxation Method for Contact Layer Decomposition of DSA with Triple Patterning,” *Integration, the VLSI Journal*, vol. 61, no. 1, pp. 77-87 (2018). **(CCF-C)**

4. Ye Huang, **Xinquan Li**, Wenxing Zhu and Jianli Chen*, “Cut Redistribution and DSA Template Assignment for Unidirectional Design,” In *Proceedings of ASICON (ASICON)*, 2017.

5. **Xingquan Li**, Bei Yu, Jiaojiao Ou, Jianli Chen, David Z. Pan and Wenxing Zhu*, “Graph Based Redundant Via Insertion and Guiding Template Assignment for DSA-MP,” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI),* vol. 26, no. 11, pp. 2504-2517, (2018). **(CCF-B)**

6. Jianli Chen, Peng Yang, Ye Huang, **Xingquan Li**, Wenxing Zhu and Yao-Wen Chang*, “Mixed-Cell-Height Placement with Minimum-Implant-Area Constraints,” In *Proceedings of IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, 2018**. (CCF-B)**

7. Ziran Zhu, **Xingquan Li**, Yuhang Chen, Zhipeng Huang, Jianli Chen, Wenxing Zhu and Yao-wen Chang*, “Technology and Region Constraints-Aware Multi-Deck Standard Cell Legalization,” In *Proceedings of IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, 2018**. (CCF-B)**

8. Hao Geng, Haoyu Yang, Bei Yu*, **Xingquan Li** and Xuan Zeng, “Sparse VLSI Layout Feature Extraction: A Dictionary Learning Approach (Invited),” In *Proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2018. **(CCF-C)**

9. **Xingquan Li**, Bei Yu, Jianli Chen and Wenxing Zhu*, “A Local Optimal Method on DSA Guiding Template Assignment with Redundant/Dummy Via Insertion,” In *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2019**. (CCF-C)**

10. **Xingquan Li**, Jianli Chen, Yuhang Chen, Ziran Zhu, Wenxing Zhu* and Yao-Wen Chang, “Analytical Mixed-Cell-Height Legalization Considering Average and Maximum Movement Minimization,” In *Proceedings of ACM International Symposium on Physical Design (ISPD),* 2019**. (CCF-C)**

11. **Xingquan Li***, Bei Yu, Jianli Chen, and Wenxing Zhu, “DSA Guiding Template Assignment with Multiple Redundant Via and Dummy Via Insertion”， *Integration, the VLSI Journal*, 2019. **(CCF-C)**

12. **Xingquan Li*,** Cong Cao, and Tao Zhang, "Block Diagonal Dominance Based Dynamic Programming for Detecting Community", *The Journal of Supercomputing (SC),* 2020. **(CCF-C)**

13. Tingshen Lan, **Xingquan Li,** Jianli Chen, Jun Yu, Lei He, Senhua Dong, Wenxing Zhu, Yao-Wen Chang*, Timing-Aware Fill Insertions with Design-Rule and Density Constraints, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 1-8, 2020. **(CCF-B)**

14. **Xingquan Li***, Jiangkao Li, Hongxi Wu, Yeh-Cheng Chen, "Discrete relaxation method for hybrid e-beam and triple patterning lithography layout decomposition" *Journal of Ambient Intelligence and Humanized Computing (AIHC)*, 2021. **(SCI)**

15. **Xingquan Li***, Hongxi Wu, "Toward graph classification on structure property using adaptive motif based on graph convolutional network", *The Journal of Supercomputing (SC)*, 2021. **(CCF-C)**

16. Zhipeng Huang, **Xingquan Li**, Wenxing Zhu*. Optimization models and algorithms for placement of very large scale integrated circuits [J/OL]. *Operations Research Transactions*, 2021, 25(3).

17. Xiqiong Bai, Ziran Zhu, Pingping Li, Jianli Chen, Tingshen Lan, **Xingquan Li,** Jun Yu, Wenxing Zhu, Yao-Wen Chang*, Timing-aware fill insertions with design-rule and density constraints, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2021. **(CCF-A)**

18. Zhiyuan Yan, Biwei Xie, **Xingquan Li**, Yugang Bao*, Exploiting Architecture Advances For Sparse Solvers In Circuit Simulation, *IEEE/ACM Design, Automation and Test in Europe Conference (DATE)*, 2022. (**CCF-B**)

19. Shengkun Wu, Biwei Xie, **Xingquan Li*** ， An Adaptive Partition Strategy of Galerkin Boundary Element Method for Capacitance Extraction， in *Proceedings of the 28th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2023. **(CCF-C)**

20. **Xingquan Li**, Simin Tao, Zengrong Huang, Shijian Chen, Zhisheng Zeng, Liwei Ni, Zhipeng Huang, Chunan Zhuang, Hongxi Wu, Weiguo Li, Xueyan Zhao, He Liu, Shuaiying Long, Wei He, Bojun Liu, Sifeng Gan, Zihao Yu, Tong Liu, Yuchi Miao, Zhiyuan Yan, Hao Wang, Jie Zhao, Yifan Li, Ruizhi Liu, Xiaoze Lin, Bo Yang, Zhen Xue, Zonglin Yang, Zhenggang Wu, Jiangkao Li, Yuezuo Liu, Ming Peng, Yihang Qiu, Wenrui Wu, Zheqing Shao, Kai Mo, Jikang Liu, Yuyao Liang, Mingzhe Zhang, Zhuang Ma, Xiang Cong, Daxiang Huang, Guojie Luo, Huawei Li, Haihua Shen, Mingyu Chen, Dongbo Bu, Wenxing Zhu, Ye Cai, Xiaoming Xiong, Ying Jiang, Yi Heng, Peng Zhang, Biwei Xie*, Yungang Bao*. "**iEDA:** An Open-source Intelligent Physical Implementation Toolkit and Library", *in proceedings of IEEE International Symposium of EDA (ISEDA)*, 2023. **(Best Paper Award)**

21. He Liu, Shengkun Wu, Simin Tao, Biwei Xie, **Xingquan Li***, and Ge Li. "Accurate Timing Path Delay Learning using Feature Enhancer with Effective Capacitance", *in proceedings of IEEE International Symposium of EDA (ISEDA)*, 2023.

22. Liwei Ni, Zonglin Yang, Jiaxi Zhang, Changhong Feng, Jianhua Liu, Guojie Luo, Huawei Li, Biwei Xie and **Xingquan Li***. "MEC: An Open-source Fine-grained Mapping Equivalence Checking Tool for FPGA", *in proceedings of IEEE International Symposium of EDA (ISEDA)*, 2023.

23. Jie Zhao, Biwei Xie and **Xingquan Li***. "Weight Uncertainty in Transformer Network for the Traveling Salesman Problem", *in proceedings of IEEE International Symposium of EDA (ISEDA)*, 2023.

24. Cong Cao*, Fan Liu, Juan Cheng, Menglin Kong, Muzhou Hou, Ruichen Li, **Xingquan Li**, Landslide Surface Displacement Prediction Based on VSXC-LSTM Algorithm, *in proceedings of ENNS International Conference on Artificial Neural Networks (ICANN)*, 2023. **(CCF-C)**

25. Menglin Kong, Shaojie Zhao, Juan Cheng, **Xingquan Li**, Ri Su, Muzhou Hou, Cong Cao*, FaFCNN: A General Disease Classification Framework Based on Feature Fusion Neural Networks, *in proceedings of IEEE International Conference on Systems, Man, and Cybernetics (SMC)*, 2023. **(CCF-C)**

26. Xueyan Zhao, Shijian Chen, Yihang Qiu, Jiangkao Li, Zhipeng Huang*, Biwei Xie, **Xingquan Li*** and Yungang Bao, iPL-3D: A Novel Bilevel Programming Model for Die-to-Die Placement, *In Proceedings of IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, 2023. **(CCF-B)**

27. Fuxing Huang, Duanxiang Liu, **Xingquan Li,** Bei Yu and Wenxing Zhu*, Handling Orientation and Aspect Ratio of Modules in Electrostatics-based Large Scale Fixed-Outline Floorplanning, *In Proceedings of IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, 2023. **(CCF-B)**

28. Liwei Ni, Zonglin Yang, Jiaxi Zhang, Junfeng Liu, Huawei Li, Biwei Xie and **Xingquan Li*,** "Adaptive Reconvergence-driven AIG Rewriting via Strategy Learning", *In Proceedings of IEEE International Conference on Computer Design (ICCD),* 2023. **(CCF-B)**

29. Junfeng Liu, Liwei Ni, **Xingquan Li**, Min Zhou, Lei Chen, Xing Li, Qinghua Zhao and Shuai Ma*, "AiMap: Learning to Improve Technology Mapping for ASICs via Delay Prediction", *In Proceedings of IEEE International Conference on Computer Design (ICCD),* 2023. **(CCF-B)**

30. Ping Zhang, Pengju Yao, **Xingquan Li,** Bei Yu, and Wenxing Zhu*, "V-GR: 3D Global Routing with Via Minimization and Multi-Strategy Rip-up and Rerouting" in *Proceedings of the 28th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2024. **(CCF-C)**

31. **Xingquan Li**, Simin Tao, Shijian Chen, Zhisheng Zeng, Zhipeng Huang, Hongxi Wu, Weiguo Li, Zengrong Huang, Liwei Ni, Xueyan Zhao, He Liu, Shuaiying Long, Ruizhi Liu, Xiaoze Lin, Bo Yang, Fuxing Huang, Zonglin Yang, Yihang Qiu, Zheqing Shao, Jikang Liu, Yuyao Liang, Biwei Xie, Yungang Bao and Bei Yu*, iPD: An Open-source intelligent Physical Design Tool Chain (invited), in *Proceedings of the 28th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2024. **(CCF-C)**

32. **Xingquan Li,** Zengrong Huang, Simin Tao, Zhipeng Huang, Chunan Zhuang, Hao Wang,

Yifan Li, Yihang Qiu, Guojie Luo, Huawei Li, Haihua Shen, Mingyu Chen, Dongbo Bu, Wenxing Zhu, Ye Cai, Xiaoming Xiong, Ying Jiang, Yi Heng, Peng Zhang, Bei Yu, Biwei Xie*, Yungang Bao*, iEDA: An Open-source infrastructure of EDA (invited), in *Proceedings of the 28th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2024. **(CCF-C)**

33. W Zheng, M Kong, R Li, L Xiong, **Xingquan Li**, M Hou, C Cao*, A novel automatic detection and classification algorithm for elderly cognitive impairment using CSVM, Biomedical Signal Processing and Control 93, 106195, 2024. **(CCF-C)**
34. M Kong, R Li, J Wang, **Xingquan Li**, S Jin, W Xie, M Hou, C Cao*, CFTNet: a robust credit card fraud detection model enhanced by counterfactual data augmentation, Neural Computing and Applications, 1-17, 2024. **(CCF-C)**
35. Ye Cai, Yuyao Liang, Zhipeng Luo, Biwei Xie, **Xingquan Li***, PCT-Cap: Point Cloud Transformer for Accurate 3D Capacitance Extraction, *in proceedings of IEEE International Symposium of EDA (ISEDA)*, 2024.
36. Ye Cai, Zonglin Yang, Liwei Ni, Biwei Xie, **Xingquan Li***, Enhancing ASIC Technology Mapping via Parallel Supergate Computing, *in proceedings of IEEE International Symposium of EDA (ISEDA)*, 2024.
37. Zhipeng Huang, Zengrong Huang, Simin Tao, Shijian Chen, Zhisheng Zeng, Liwei Ni, Chunan Zhuang, Weiguo Li, Xueyan Zhao, He Liu, Biwei Xie, and **Xingquan Li***, AiEDA: An Open-source AI-native EDA Library, *in proceedings of IEEE International Symposium of EDA (ISEDA)*, 2024.
38. Ye Cai, Zonglin Yang, Liwei Ni, Junfeng Liu, Biwei Xie, and **Xingquan Li***, Parallel AIG Refactoring via Conflict Breaking, in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, 2024. **(CCF-C)**
39. He Liu, Simin Tao, Zhipeng Huang, Biwei Xie, **Xingquan Li*** and Ge Li, Instance-level Timing Learning and Prediction at Placement using Res-UNet Network, in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, 2024. **(CCF-C)**
40. Zhisheng Zeng; Jikang Liu; Zhipeng Huang; Ye Cai; Biwei Xie; Yungang Bao; **Xingquan Li***, Net Resource Allocation: A Desirable Initial Routing Step, in *Proceedings of Design Automation Conference (DAC)*, San Francisco CA USA, 2024. **(CCF-A)**
41. Weiguo Li; Zhipeng Huang; Bei Yu; Wenxing Zhu; **Xingquan Li***, Toward Controllable Hierarchical Clock Tree Synthesis with Skew-Latency-Load Tree， in *Proceedings of Design Automation Conference (DAC)*, San Francisco CA USA, 2024. **(CCF-A)**

Academic Reports

- "Mixed-Cell-Height Placement with Minimum-Implant-Area Constraints", the 10th China Fault Tolerance and Testing Committee, Harbin, 2018.
- “A Local Optimal Method on DSA Guiding Template Assignment with Redundant/Dummy Via Insertion ”， ASP-DAC , 2019，Tokyo, Japan，2019.

- “Analytical Mixed-Cell-Height Legalization Considering Average and Maximum Movement Minimization”, ISPD, San Francisco, CA, USA, 2019.
- "Open-source EDA Design Practices", CCF-YOCSEF, Shenyang, 2021.
- "Graph algorithm problem in EDA", Sun Yat-sen University, Guangzhou, 2021.
- "Open-source EDA Problems and EDA Tool Design", OSEDA Forum, Shanghai, 2022.
- "2022 ICCAD Contest: 3D Placement with D2D Vertical Connections", University of Science and Technology of China, Hefei, 2022.
- "2022 ICCAD Contest: 3D Placement with D2D Vertical Connections", EDA^2 Physical Implementation Sub-committee, Online, 2022.
- "EDA Introduction", School of Mathematics, Chinese Academy of Sciences, Beijing, 2023.
- "Introduction to iEDA Work", Central South University, Changsha, 2023.
- “iEDA: An Open-source Intelligent Physical Implementation Toolkit and Library”， International Symposium of EDA (ISEDA)，2023.
- "Open-source intelligent EDA Platform (iEDA)", Sun Yat-sen University, Shenzhen, 2023.
- "Intelligent EDA System", Beijing University of Posts and Telecommunications, Beijing, 2023.
- "Open-source iEDA Platform", EDA^2 Physical Implementation Sub-committee, Online, 2023.
- "Open-source EDA Promoting Academic Competition", ISIC, Nanjing, 2023.
- "EDA Platform and Machine Learning", ISIC, Nanjing, 2023.
- "iEDA Tutorial", iEDA, Online, 2023.
- "Intelligent EDA Platform and its Application", the second Xiamen Open-source Chip Industry Promotion Forum, 2023.
- "EDA Software Design and Algorithms", the 3rd China RISC-V Summit, Beijing, 2023.
- "AiEDA: Intelligent EDA Framework", the 4th CCF-DAC, Beijing, 2023.
- "Open-source EDA Platform and Tool Chain", 8th ICICM, Nanjing, 2023.
- "AiEDA: Intelligent EDA Framework and Its Applications", Computer Conference 2023 CNCC, Shenyang, 2023.
- AiEDA: An Open-source AI-native EDA library, ISEDA 2024 invited speaker, 2024.

Conference Organization

- Open-source EDA Design: Netlist- -to-GDS, National Laboratory, 2021
- Open-source Intelligent EDA Tools and Its Key Technologies, Open-source Intelligent EDA Brainstorming, 2022
- Annual Meeting of iEDA Work Summary, National Laboratory, 2022
- iEDA Tutorial (Phase 1-5), iEDA Community Lecture Series, 2023.
- The first Greater Bay Area EDA Symposium, Pengcheng Lab, 2023.
- The 2nd Open-source EDA (OSEDA) Seminar, the 3rd China RISC-V Summit, 2023.
- Open-source Chip Technology Ecology Forum, 3rd China RISC-V Summit, 2023.
- Open-source Digital EDA Tools and Models Forum, 4th CCF-DAC, Beijing, 2023.
- iEDA Tutorial, 2th ISEDA, Xian, 2024.
- Open-source Intelligent EDA Tools and Models Forum, 2th CCF-Chip, Shanghai, 2024.

Academic Awards

- ISEDA Best Paper Award, 2023
- CCF-DAC Best Paper Award Candidate, 2023
- 2022 CAD Contest @ ICCAD, 3D Placement with D2D Vertical Connections, First Place.
- Science and Technology Award of Chinese Operations Research Society—Operations Research Application Award, 2020
- The Third Prize of Excellent Paper of Fujian Province, 2020
- Fujian Province Excellent Doctoral Dissertation (3/51), 2019
- ICCAD 2018 @ CAD Contest on Timing Aware Fill Insertion Global, First Place, 2018.
- ICCAD 2017 @ CAD Contest on Multi-Deck Standard Cell Legalization, First Place (first time in mainland of China), 2017
- National Scholarship, 2017

Academic Service

- IEEE/ACM/EDA^2 Member
- CCF Member
  - Council member of CCF Integrated Circuit Design Committee,
- ORSC Member
  - Council member of Algorithm Software and Application Branch of China Operations Research Society,
  - Council member of Intelligent Optimization Branch of China Operations Research Society
- Contest chair of China EDA Elite Challenge, 2022/2023/2024
- Open Atomic Open-source Software Competition expert, 2023
- TCAD, TVLSI, Integration, ICCAD, ASP-DAC, SASIMI, Supercomputing, JCST Reviewer
- ISEDA TPC，2023
- Xiamen Open-source Chip Industry Promotion Association technical Expert Committee of the first technical expert, 2023.08-2025.08