

Tutorial 7

iEDA: An Open-source Physical Design EDA Infrastructure and Toolchain

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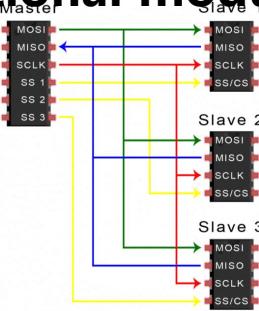
iEDA Tutorial Agenda

- **Part 0:** iEDA Overview (**Xingquan Li**)
- **Part 1:** iEDA Infrastructure (**Zengrong Huang/Xingquan Li**)
- **Part 2:** iPL: Placement Tool and Its Technologies (**Shijian Chen**)
- **Part 3:** iCTS: Clock Tree Synthesis Tool and Its Technologies (**Weiguo Li**)
- **Part 4:** iRT: Routing Tool and Its Technologies (**Zhisheng Zeng**)
- **Part 5:** iSTA: Static Timing Analysis Tool and Its Technologies (**He Liu**)
- **Part 6:** iPA: Power Analysis Tool and Its Technologies (**Simin Tao**)

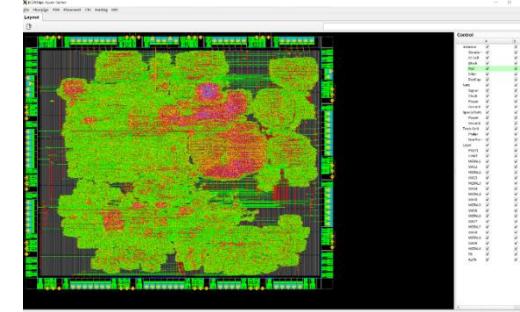
- 01 **Background**
- 02 **iEDA**

Chip Design Elements

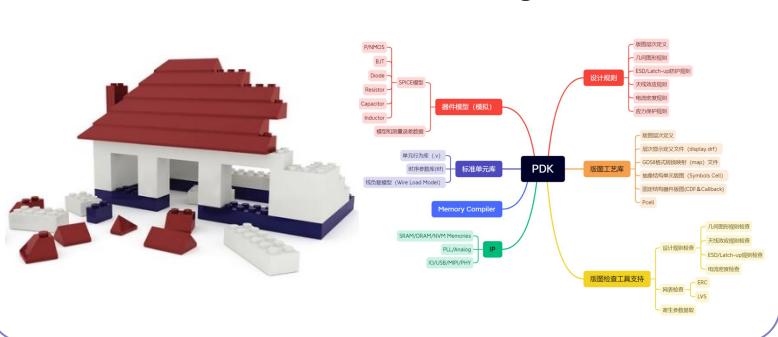
**IP: Intellectual Property
Functional module**



**EDA: Electronic design
automation software (tool)**



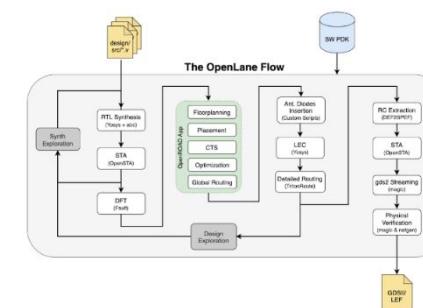
**PDK: Process design
kits from foundry**



Flow



**Flow: Chip design flow
config and script**



Open-source RTL, PDK and Flow

Open-source RTL

Accelerator	Analog	Connectivity	CPU	FPGA	Memory	System
aes/aes_core	AMS_KGD	aib	OpenXiangShan	FABulous	core_axi_cache	Beagle_SDR_GPS
ara	open-pmic	aib-protocols	a2i	fabric_team	HuanCun	bsg_manycore
FFTGenerator	Analog Basic Blocks/LDO	core_ddr3_controller	black-parrot	OpenFPGA	openram	cep
fpu		HDMI	Cores-SweRV	prga	lake	esp
garnet		i2c		core-v-verif		hero
gplgpu		litedram		cva6		litex
core_jpeg		liteeth		cv32e40p		openFASOC
vortex		litepice		ibex		openpiton
VeriGPU		litescope		microwatt		opentitan
tvm-vta		pymtl3-net		neorv32		openwifi-hw
...		verilog-ethernet		picorv32		pulp
		ravenoc		rocket-chip		pulpissimo
		verilog-uart		serv		
				snitch		
			boom			
			Low-RISC			
			OpenXuantie - OpenC910 Core			
			ysyx			

Open-source PDK

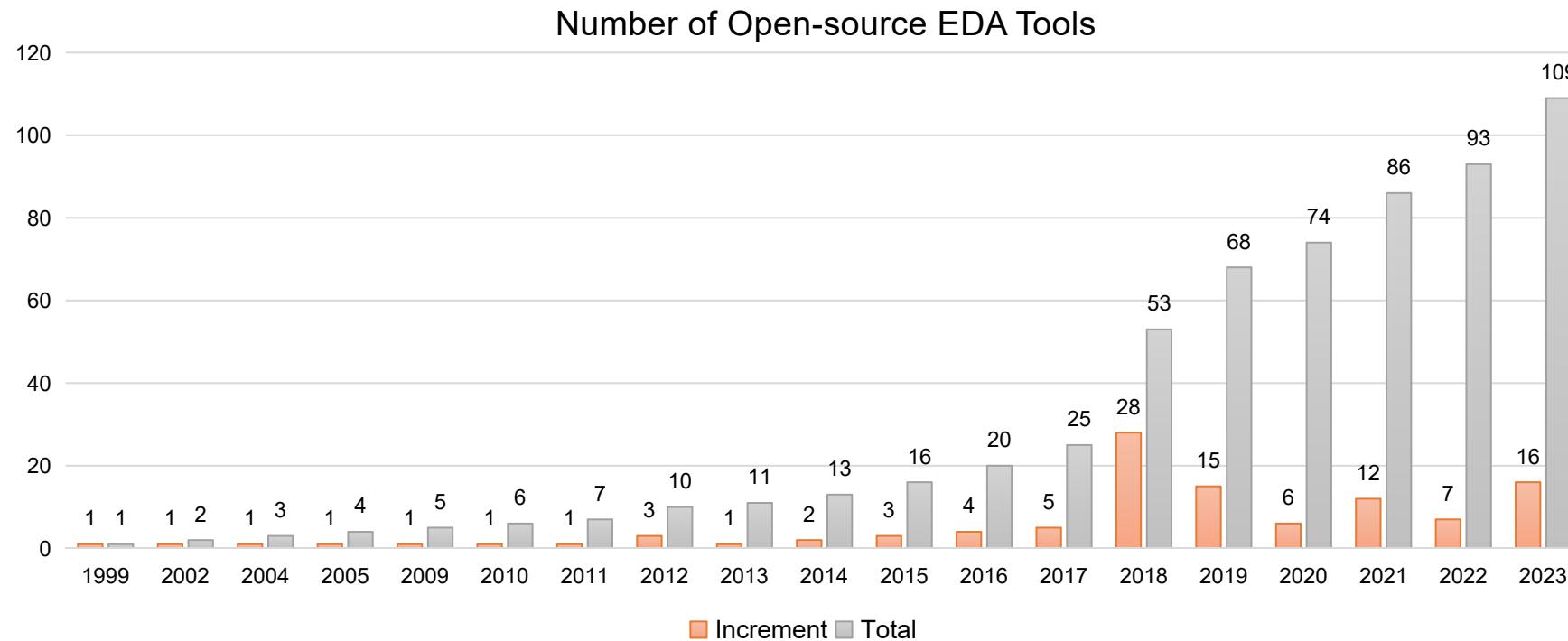
PDK name	Process node	Foundary	Institution
Sky130	130nm	Skywater	Google/Efabless
Sky90	90nm	Skywater	Google/Efabless
gf180	180nm	GlobalFoundries	Google/Efabless
NanGate45	45nm	Fake	Si2
Asap7	7nm	Fake	ARM Ltd

Open-source Flow

Flow	Function	Contributor Institution
Qflow	RTL-GDS	Efabless
VSDFLOW	RTL-GDS	VLSI System Design
OpenRoad	RTL-GDS	UCSD
OpenLane	RTL-GDS	Efabless/UCSD
Ophidian	Netlist-GDS	UFSC
Rsyn	Physical Synthesis	FURG
SiliconCompiler	RTL-GDS	Zero ASIC
SymbiFlow	FPGA design flow	F4PGA
iFlow	RTL-GDS	PCL/ICT/BOSC/...

Increasing Open-source EDA Tools

- Open-souce in EDA may be a tendency



Open-source EDA Tools

Design Module	Design Step	Some Open-source Tools						iEDA
HLS	HLS	LegUp	GAUT	PandA	FCUDA	XLS		
	Logic Simulation	Verilator/iVerilog	GHDL	FreeHDL	TkGate			
	Circuit Simulation	NGSpice	mixedsim	GnuCap	Qucs	XICE		
	Debug							
Logic Synthesis	Logic Synthesis	Yosys	ABC	EPFL-LS-Lib	LLDHL	UNIVR	iLS	
	Tech Map	ABC					iMap	
DFT	DFT	Fault						
	Formal							
Physical Design	Partition	PartitionMgr	METIS	KaHyPar	MPPart		iNO	
	Floorplan	OpenRoad TritonMacroPlacer	OpenRoad	Parquest			iFP	
	PDN	OpenPDN					iPDN	
	Placement	RePlace OpenDP	DreamPlace	Graywolf	Capo		iPL	
	CTS	TritonCTS					iCTS	
	Timing OPT	TritonSizer	Gate-Sizing				iTO	
	Routing	FastRoute TritonRoute	CUGR Dr.CU	Qrouter	NTHU-Route	BoxRouter/FGR/ORGE	iRT	
	ECO	OpenRoad-eco					iECO	
	STA	OpenSTA	OpenTimer				iSTA	
	RCX	OpenRCX	SPEF-Extractor				iRCX	
Signoff	Power	OpenRoad-pp					iPA	
	IR Drop	PDNSim	IREDGe				iIR	
	DRC	Klayout	Magic				iDRC	
	Antenna	OpenRoad-ant						
Physical Verification	LVS	Netgen						
	MPL							
	RET/ILT							
	Mask Generation							

A Promising Open-source Precedent

- **OpenROAD: No Humans, 24 Hours**
- **Efabless-OpenLane: RTL2GDS Digital Flow**

OpenROAD: No Humans, 24 Hours

- **FOCUS:** Ease of use and runtime
- **Directly attack the crises of design and innovation**
 - **Schedule barrier:** **RTL-to-GDS** in 24 hours
 - **Expertise barrier:** No-human-in-loop, **tapeout GDS**
 - **Cost barrier:** Open source (and, runs in 24 hours)
- **Unleash system innovation and design innovation**
- **Enable tool customization to system, application needs**

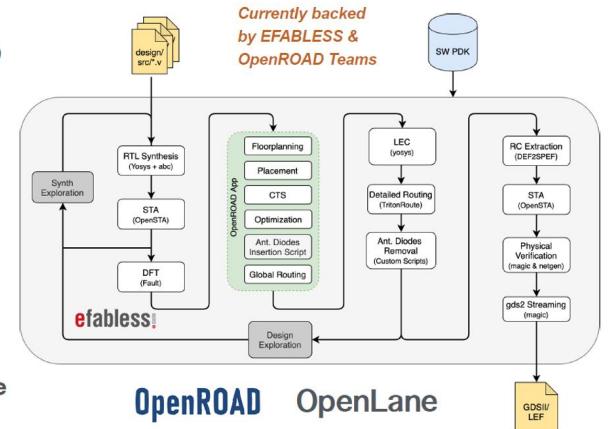


Efabless: OpenLane

DIGITAL COMPILER-LIKE RTL2GDS

OpenLane is a no-human in the loop RTL to GDS compiler built around OpenROAD that works like a **GNU software compiler with trade-offs in area and performance.**

It opens the door for software developers to generate hardware representation without the need for details. That's at least a **1000X** more potential designers!



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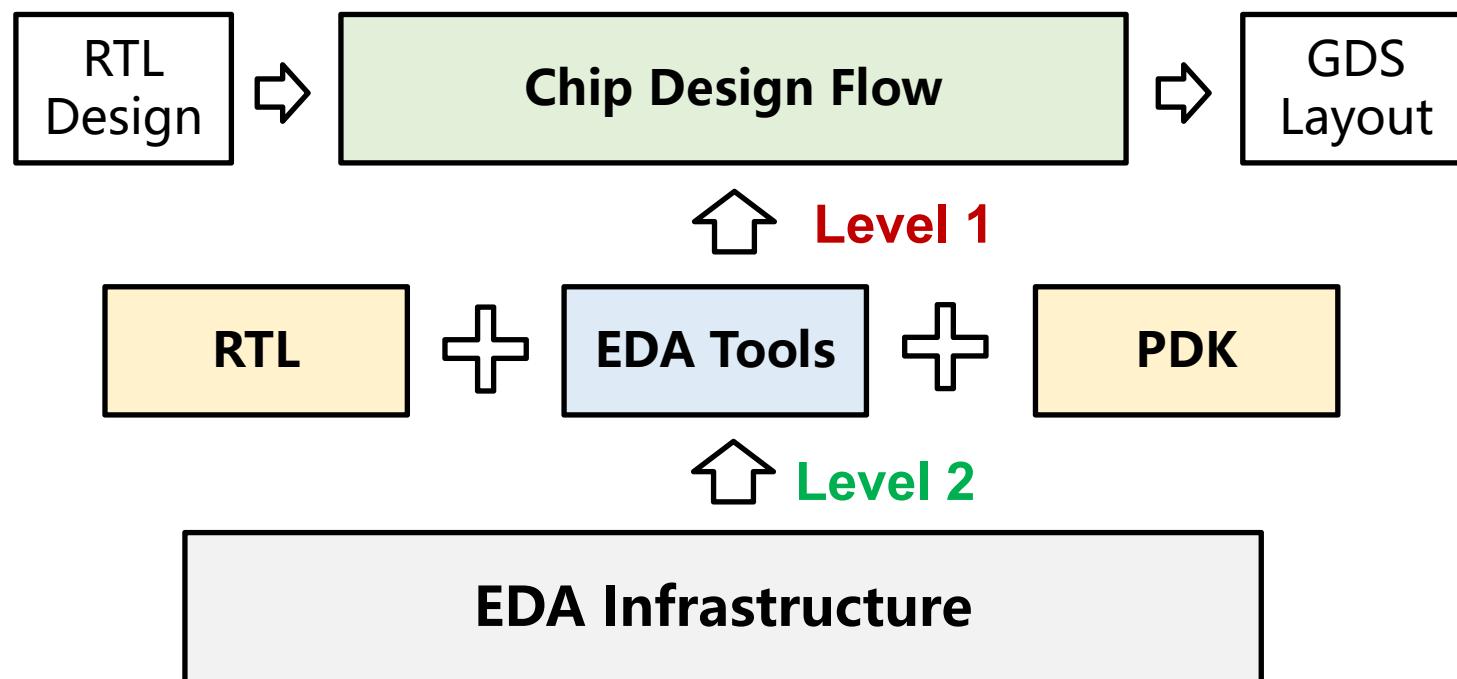
Mohamed Kassem, Efabless



From “Andrew B. Kahng, The OpenROAD Project: Today and Beyond, 2022”

We Need Infrastructure

- **Level 1:** Open-source tools, RTLs, PDKs support chip design
- **Level 2:** Open-source Infrastructure supports EDA development



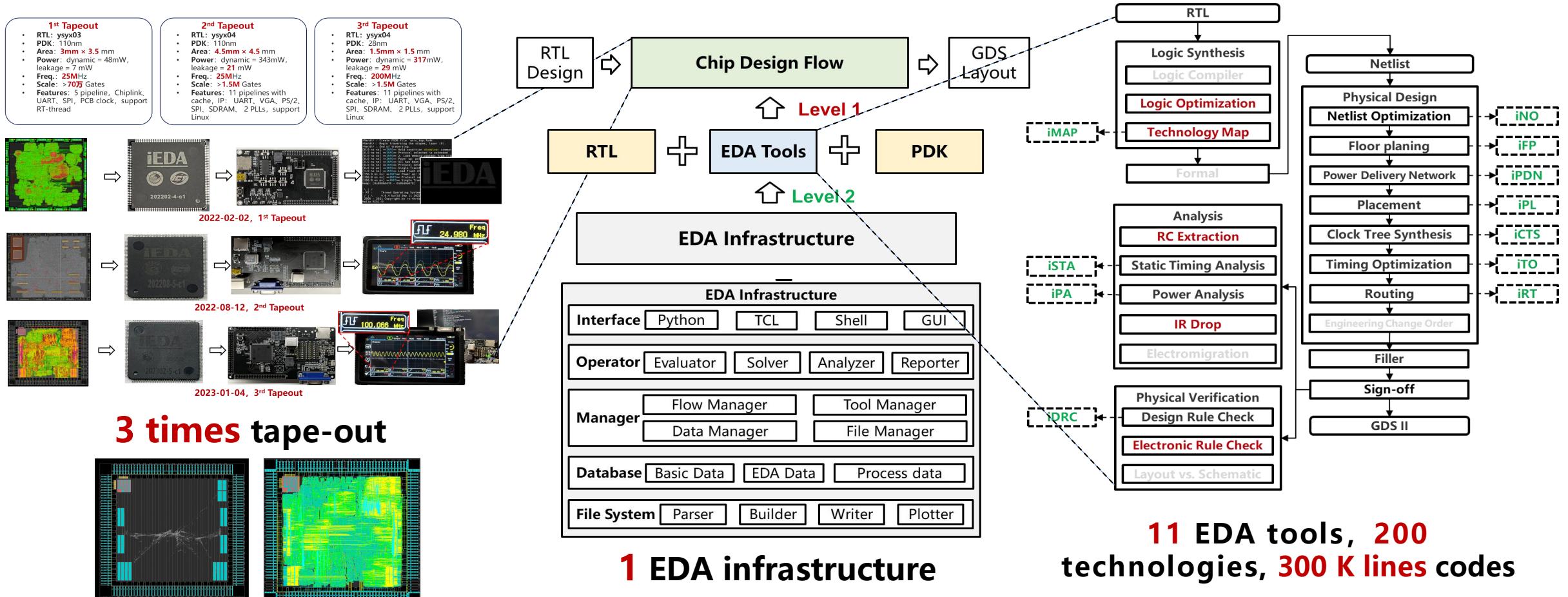
Our Motivation

- **Open-source EDA situation**
 - Only support **one algorithmic** approach, **no algorithm can perform best for any case.**
 - **Challenges in reliability, extendibility, easy-to-use.**
 - **We should provide a EDA tool R&D platform.**
 - This projects are developed and maintained **by some professors and students.**
- **The motivation of iEDA**
 - **Attract** diverse **academic disciplines**, and **bridge** the **gap** between **industry** and **academia**
 - **Support various algorithmic** solutions, and **provide long-term support.**
 - **iEDA is the set of EDA tools and algorithm sets**

- 01 **Background**
- 02 **iEDA**

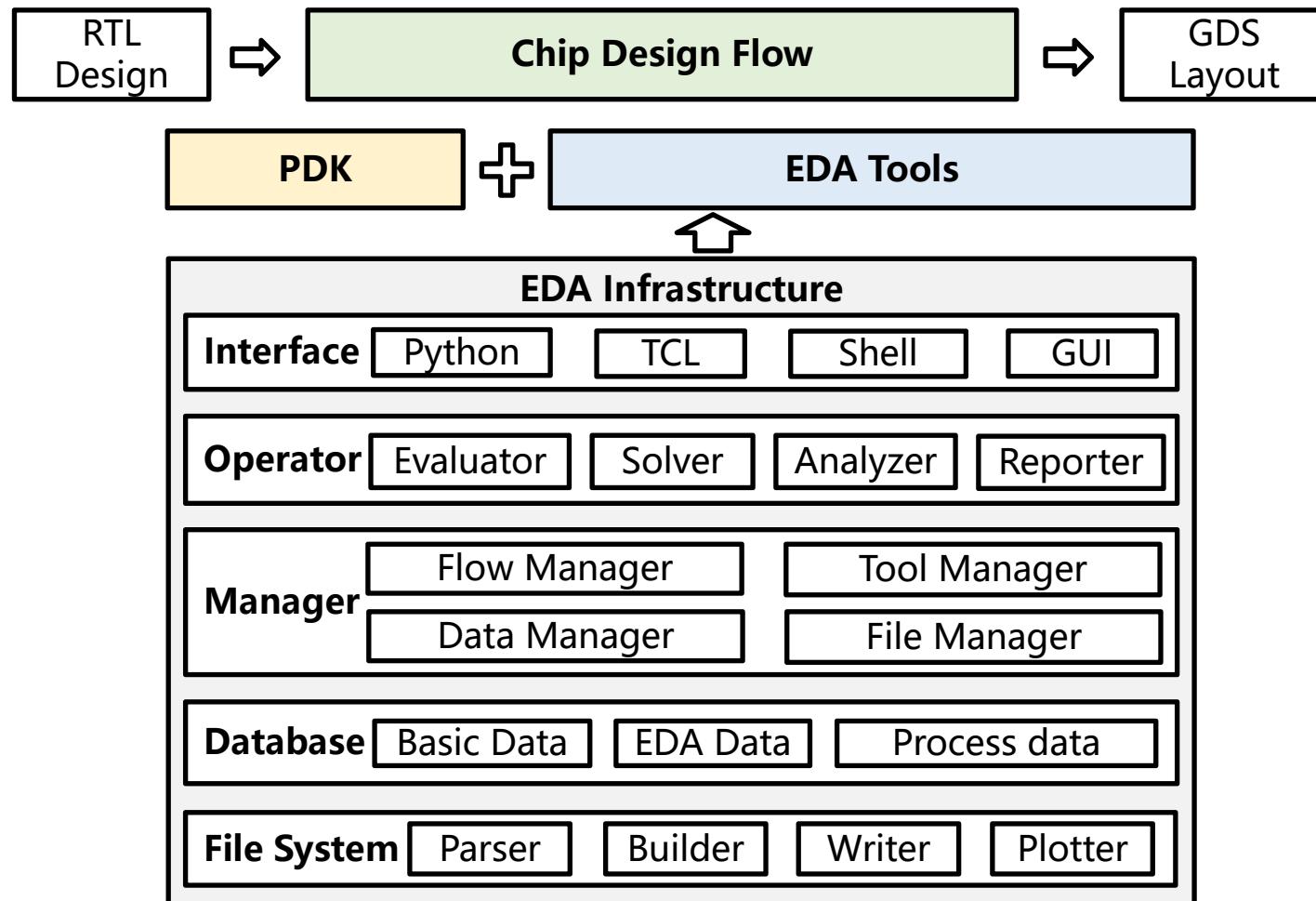
iEDA Overview

- EDA Infrastructure, EDA Tools, 3 times tape-out design by iEDA
 - Level 1: Open-source EDA, RTL, PDK, supporting chip design;
 - Level 2: Open-source Infrastructure supports EDA development and research

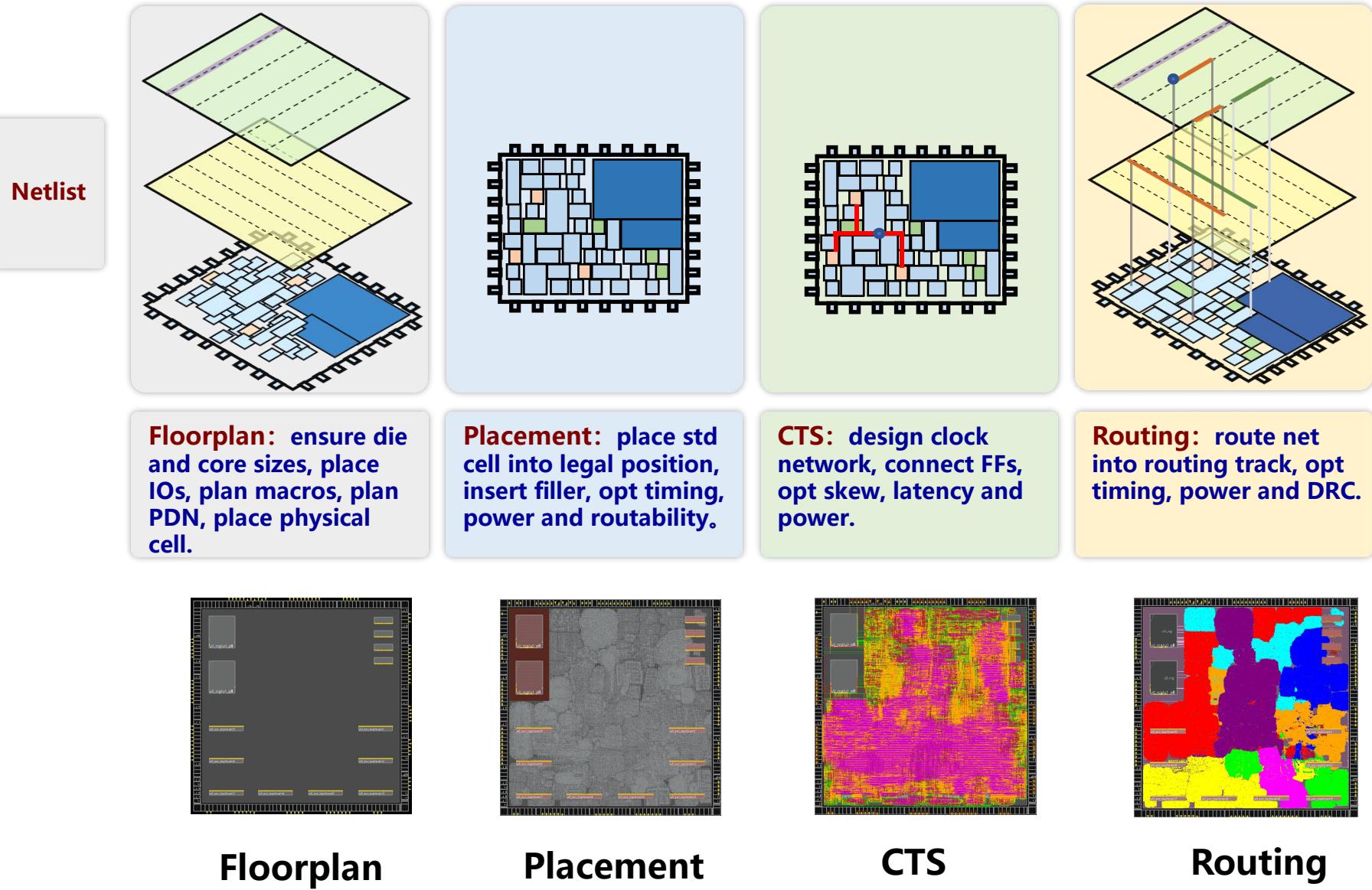
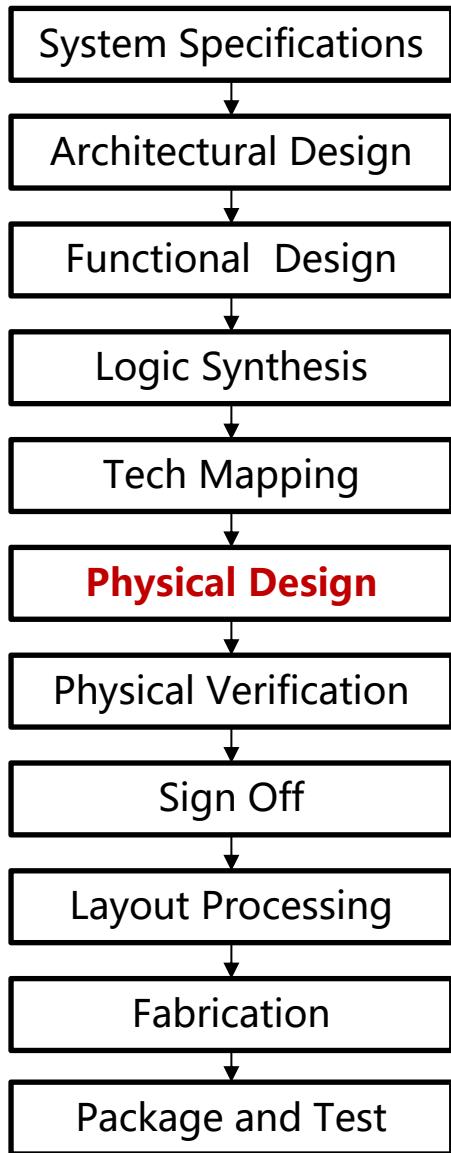


iEDA: Infrastructure

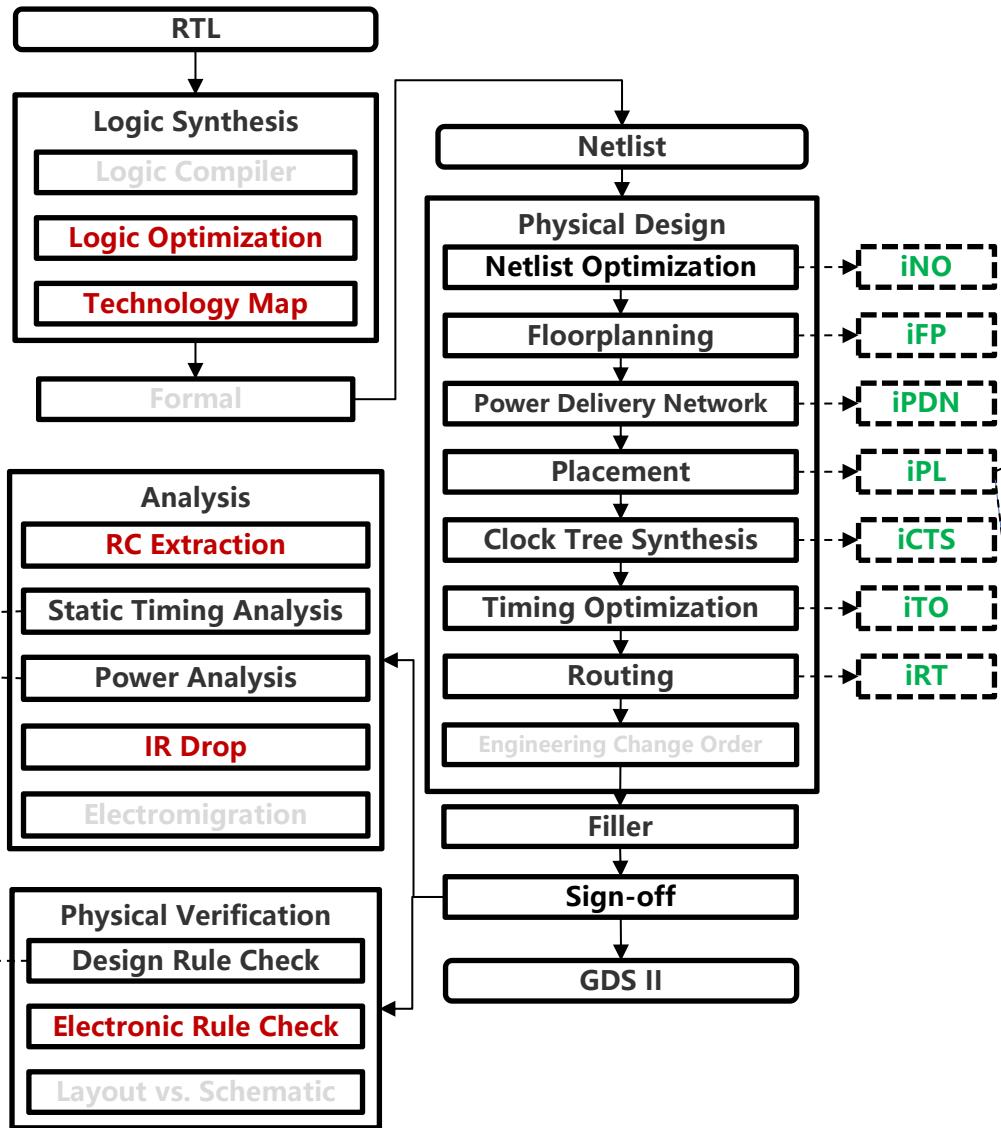
- File System
- Database
- Manager
- Operator
- Interface
- Utility
- Some perf tools



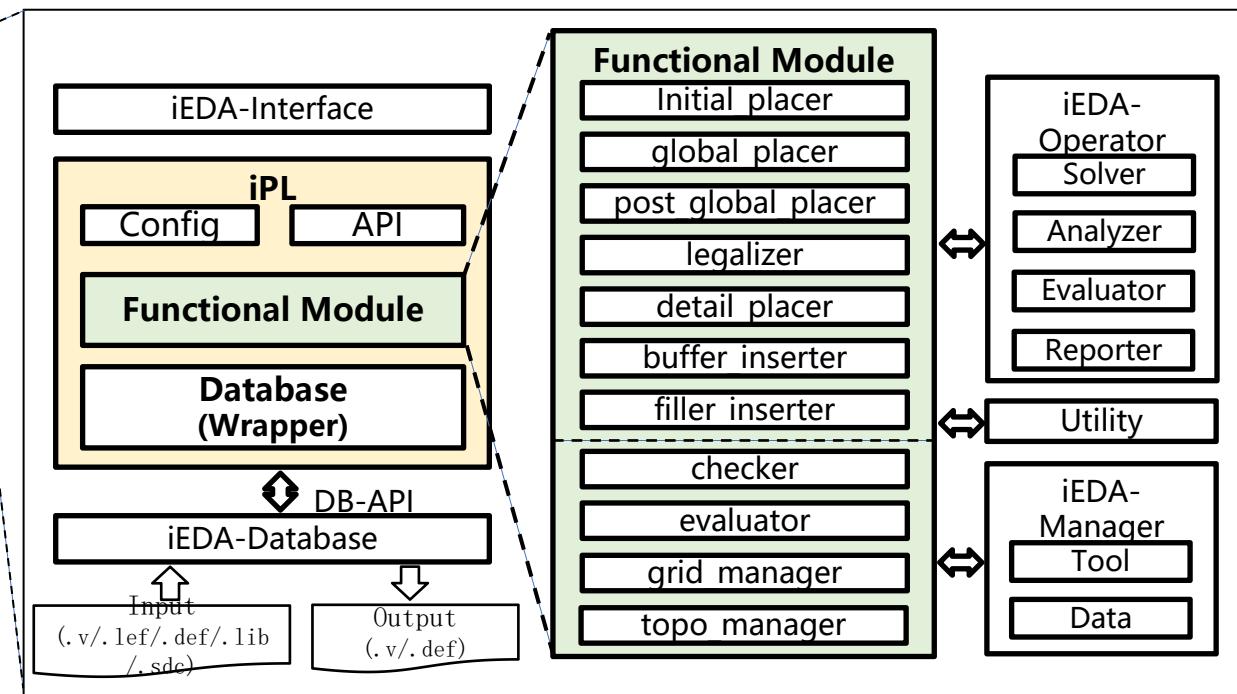
Physical Design



iEDA: Physical Design Toolchain

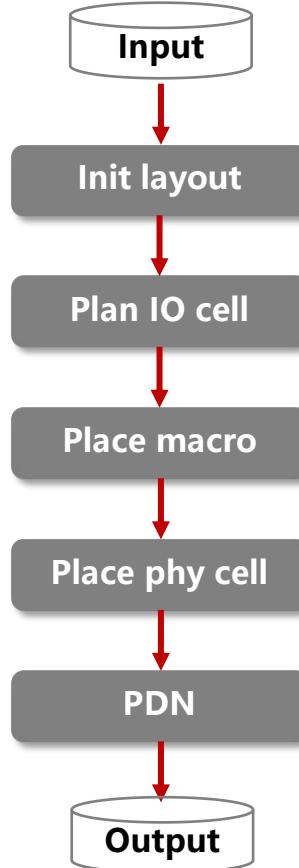


- **Netlist-to-GDS II**
 - 11 tools, and other 5 tools are R&Ding.
 - Design, Analysis, Verification
- **Design Concept:**
 - Unified framework, deconstructed and merged
 - multi-lingual interface, hot-pluggable modules.

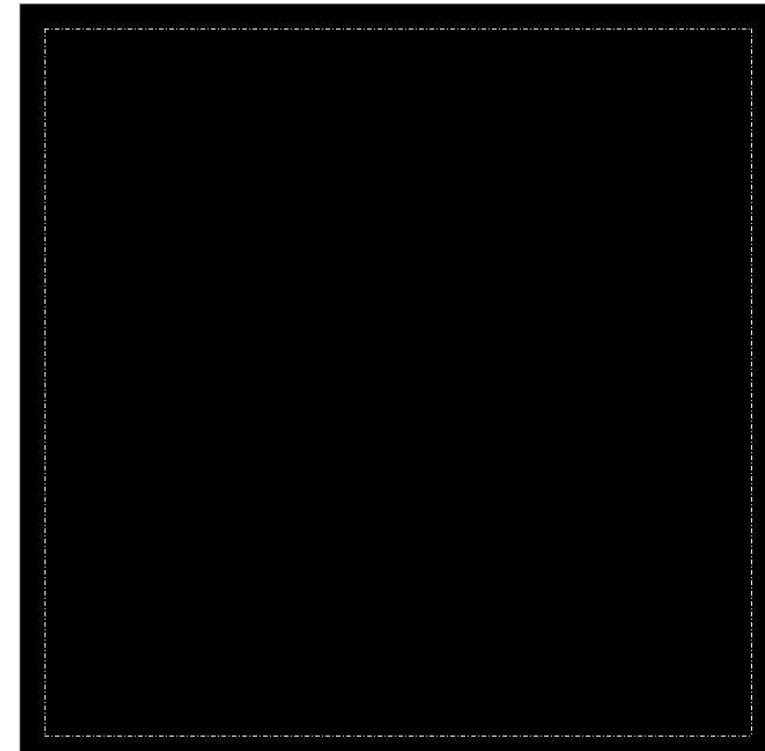
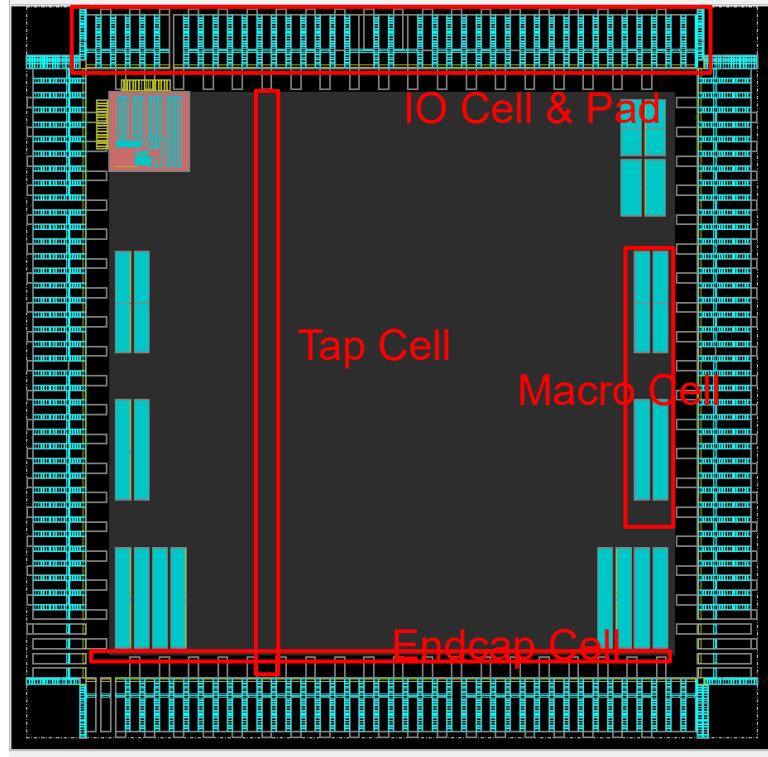


Floorplan (iFP) & Power Delivery Network (iPDN)

Flow

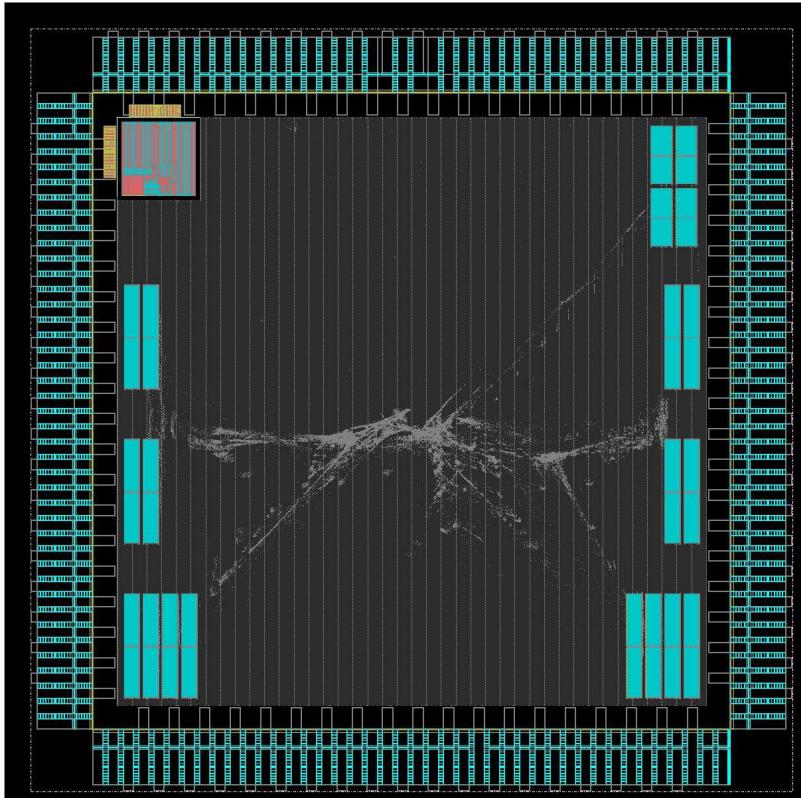
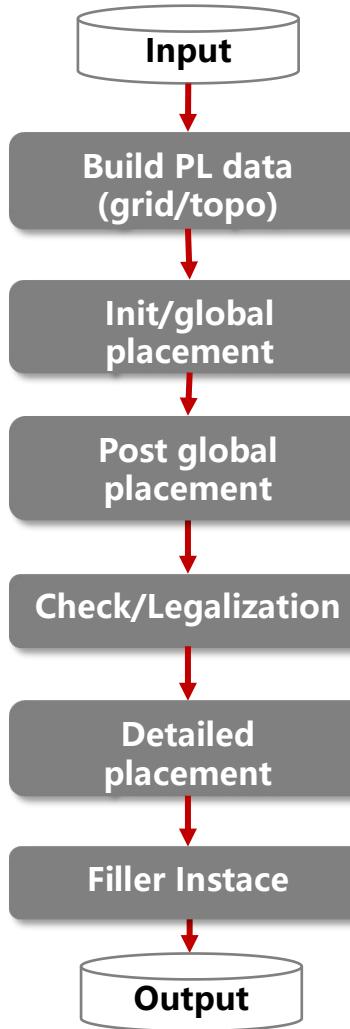


Key Metrics	Data
DIE Area	$1.5 \times 1.5 \text{ mm}^2$
DIE Utili	0.166554
Core Area	$1.16 \times 1.15 \text{ cm}^2$
Core Utili	0.279541
#IO Pin	110
#Instance	297504
#Net	311869
Pin	pin (≥ 32) = 2893
PDN	M1, M2, M7, M8, M9, AP



Placement (iPL)

Flow



■ Min Wirelength Model

$$\begin{aligned} & \min_{\boldsymbol{v}} W(\boldsymbol{v}) \\ & \text{s.t. } \rho_b(\boldsymbol{v}) \leq \rho_0, \quad \forall b \in B \end{aligned}$$

where \boldsymbol{v} is cell location, $W(\boldsymbol{v})$ is wirelength, $\rho_b(\boldsymbol{v})$ is the area density in $b \in B$, ρ_0 is density threshold.

$$\boldsymbol{W}(\boldsymbol{v}) \left\{ \begin{array}{l} HPWL_{ex}(\boldsymbol{v}) = \max_{i,j \in e} |x_i - x_j| \\ LSE_{ex} = \gamma \left(\ln \left(\sum_{i \in e} \exp \left(\frac{x_i}{\gamma} \right) \right) + \ln \left(\sum_{i \in e} \exp \left(\frac{-x_i}{\gamma} \right) \right) \right) \end{array} \right.$$

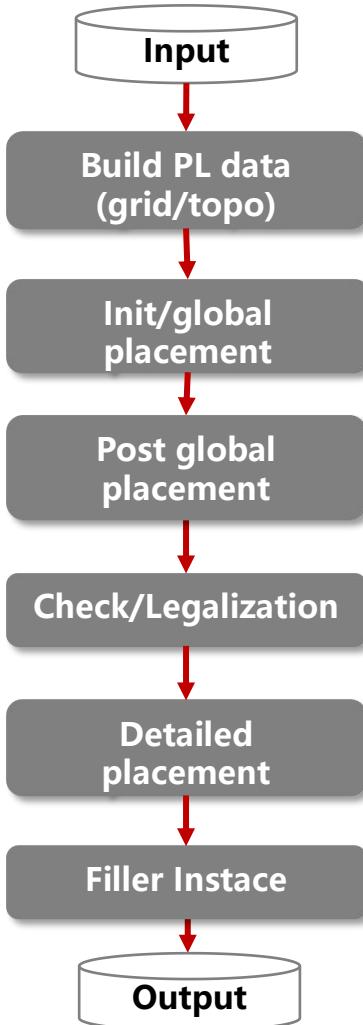
$$\boldsymbol{\rho}_b(\boldsymbol{v}) \left\{ \begin{array}{l} D(\boldsymbol{v}) = \frac{1}{2} \sum_{v \in V} D_i(x, y) = \frac{1}{2} \sum_{v \in V} q_i \psi_i(x, y) \\ \begin{cases} \nabla \cdot \nabla \psi(x, y) = -\rho(x, y), \\ \hat{\mathbf{n}} \cdot \psi(x, y) = \mathbf{0}, \quad (x, y) \in \partial R \\ \iint_R \rho(x, y) = \iint_R \psi(x, y) = 0. \end{cases} \end{array} \right.$$

$$\min_{\boldsymbol{v}} f(\boldsymbol{v}) = W(\boldsymbol{v}) + \lambda \sum_{\forall b \in B} \boldsymbol{\rho}_b(\boldsymbol{v})$$

- Nesterov Method or Conjugate Gradient

Placement (iPL)

Flow



Key parameter config	
Input	iFP.def, iFP.v
output	iPL_result.def, iPL.v
is_max_length_opt	Whether to enable max wirelength optimization
max_length_constraint	set max wirelength constraint
is_timing_aware_mode	Whether to enable timing opt
ignore_net_degree	ignore net whose pin number > k
num_threads	set number of CPU thread
[BUFFER] max_buffer_num	Set the number of using max buffer
[BUFFER] buffer_type	Set available buffer name
[GP-Wirelength] min_wirelength_force_bar	Control wirelength range
[GP-Density] target_density	Set target density
[GP-Density] bin_cnt_x	Set the number of horizontal Bin
[GP-Density] bin_cnt_y	Set the number of vertical Bin
[LG] global_right_padding	Set instance spacing (/site)
[DP] global_right_padding	Set instance spacing (/site)
[Filler] min_filler_width	Set min width of filler (/site)

Basic Summary

```

summary_report.txt X
scripts > sky130 > result > pl > report > summary_report.txt
1 Generate the report at 2023-08-15T15:10:33
2 +-----+-----+
3 | Base Info | Value |
4 +-----+-----+
5 | Design | gcd |
6 | Utilization | 0.098599 |
7 | Site Num | 78 * 542 |
8 | Instances Count | 795 |
9 | - Macro Count | 0 |
10 | - StdCell Count | 795 |
11 | -- FlipFlop Count | 34 |
12 | -- Clock Buffer Count | 0 |
13 | -- Normal Logic Count | 761 |
14 | Nets Count | 675 |
15 | - Signal Net Count | 674 |
16 | - Clock Net Count | 1 |
17 | - Reset Net Count | 0 |
18 | - Other Net Count | 0 |
19 +-----+-----+
20
21 +-----+-----+
22 | Violation Info | Value |
23 +-----+-----+
24 | Core Range Violated Count | 0 |
25 | Row/Site Alignment Violated Count | 0 |
26 | Power Alignment Violated Count | 0 |
27 | Overlap Violated Count | 0 |
28 +-----+-----+
29
30 +-----+-----+
31 | Wirelength Info | Value |
32 +-----+-----+
33 | Total HPWL | 14402289 |
34 | Max HPWL | 328905 |
35 | Total STWL | 15057480 |
36 | Max STWL | 512025 |
37 | LongNet HPWL (Exceed 1000000) Count | 0 |
38 +-----+-----+
39
40 +-----+-----+
41 | Bin Density Info | Value |
42 +-----+-----+
43 | Peak BinDensity | 1.000000 |
44 +-----+-----+
45
46 +-----+-----+-----+-----+
47 | Clock Timing Info | Early WNS | Early TNS | Late WNS | Late TNS |
48 +-----+-----+-----+-----+
49 | core_clock | 0.000000 | 0.000000 | -0.194720 | -2.818471 |
50 +-----+-----+-----+-----+
51
52 +-----+-----+
53 | Congestion Info | | |
54 +-----+-----+
55 | Average Congestion of Edges | 0.537355 |
56 | Total Overflow | 53.000000 |
57 | Maximal Overflow | 18.000000 |
58 +-----+-----+

```

The basic summary report provides a high-level overview of the design and placement statistics. It includes information on base info, design utilization, site counts, macro and stdcell counts, flipflop and clock buffer counts, normal logic counts, and net counts. It also tracks violation counts for core range, row/site alignment, and power alignment, as well as overflow metrics for congestion and timing.

Design rule violation violation_detail_report.txt

Wirelength
wl_detail_report.txt

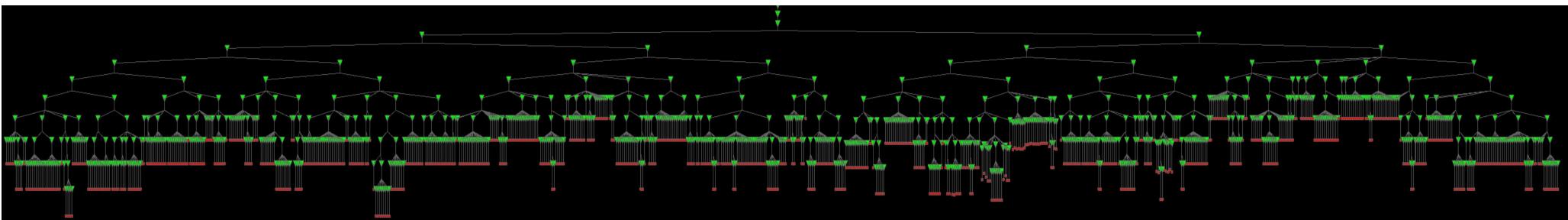
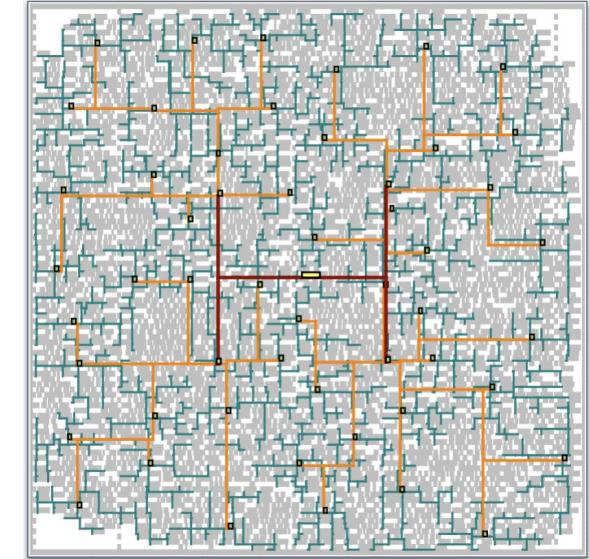
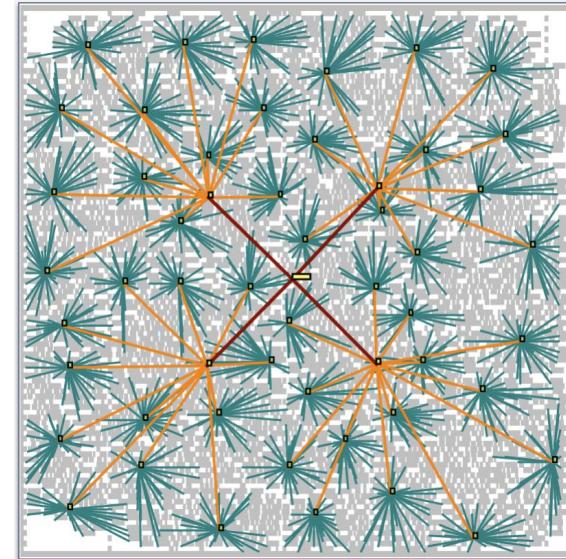
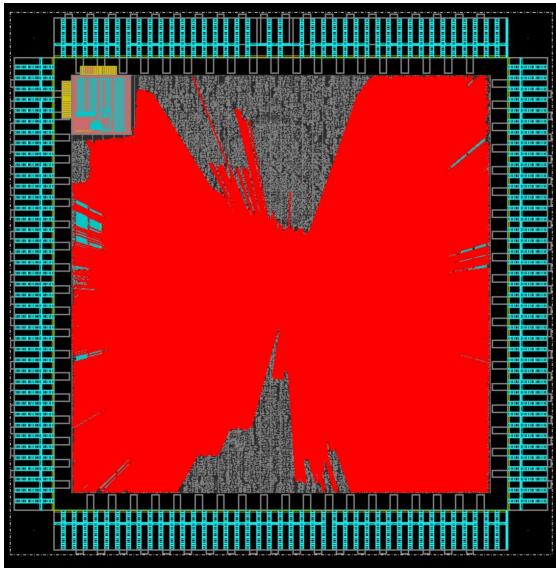
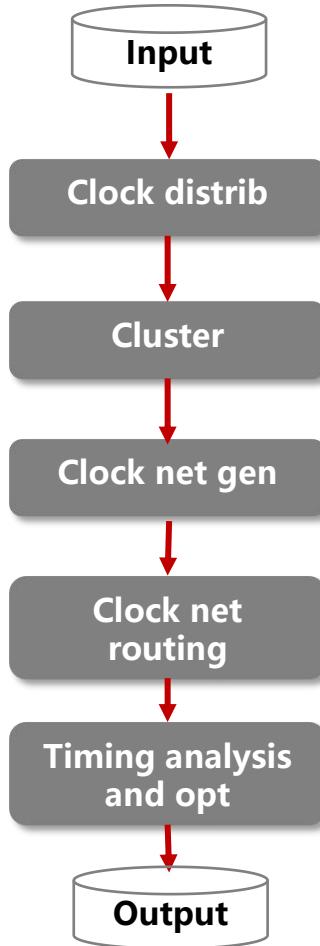
Instance density

Timing

Congestion

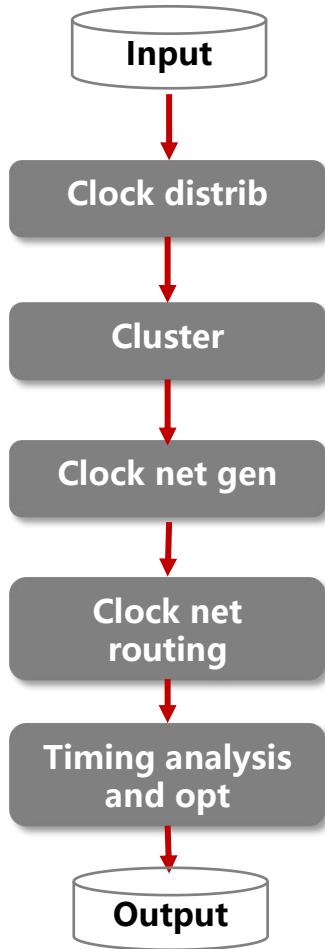
Clock Tree Synthesis (iCTS)

Flow



Clock Tree Synthesis (iCTS)

Flow



Timing

- Latency (max delay)
- Skew

Level	Inst Num	Min Skew	Max Skew	Avg Skew	Violation
1	1210	6.62388e-05	0.0145301	0.00105275	0
2	204	0.000406356	0.0278176	0.00972537	0
3	80	0.0042316	0.0411625	0.0190886	0
4	41	0.00690457	0.0566811	0.0323446	0
5	22	0.0261657	0.0760005	0.0524973	0
6	13	0.0261657	0.0799602	0.0623044	0
7	7	0.0261657	0.08	0.0669329	0
8	4	0.0603809	0.08	0.0743834	0
9	2	0.0799208	0.08	0.0799604	0
10	1	0.08	0.08	0.08	0

Level	Inst Num	Min Delay	Max Delay	Avg Delay	Violation
1	1210	0.000237424	0.0432362	0.00143337	None
2	204	0.0518461	0.0983796	0.0688073	None
3	80	0.119261	0.174637	0.145464	None
4	41	0.187633	0.255905	0.219663	None
5	22	0.250207	0.319777	0.294133	None
6	13	0.324988	0.400232	0.365337	None
7	7	0.405067	0.452041	0.435055	None
8	4	0.500763	0.549897	0.522962	None
9	2	0.573994	0.578742	0.576368	None
10	1	0.608399	0.608399	0.608399	None

Power

- Buffering
- Wirelength

Type	Wire Length
Top	161.021
Trunk	2255.200
Leaf	9267.600
Total	11683.821
Max net length	232.360

Type	HP Wire Length
Top	161.021
Trunk	1347.840
Leaf	3871.380
Total	5380.241
Max net length	161.021

Name	Type	Inst	Inst Area
		Count	(um ²)
CKBD12BWP35P140	Buffer	45	96.39
CKBD16BWP35P140	Buffer	8	22.176
CKBD20BWP35P140	Buffer	12	40.824
CKBD24BWP35P140	Buffer	63	254.016
CKBD4BWP35P140	Buffer	1082	954.324
CKBD6BWP35P140	Buffer	1129	1280.29
CKBD8BWP35P140	Buffer	81	122.472

Violation

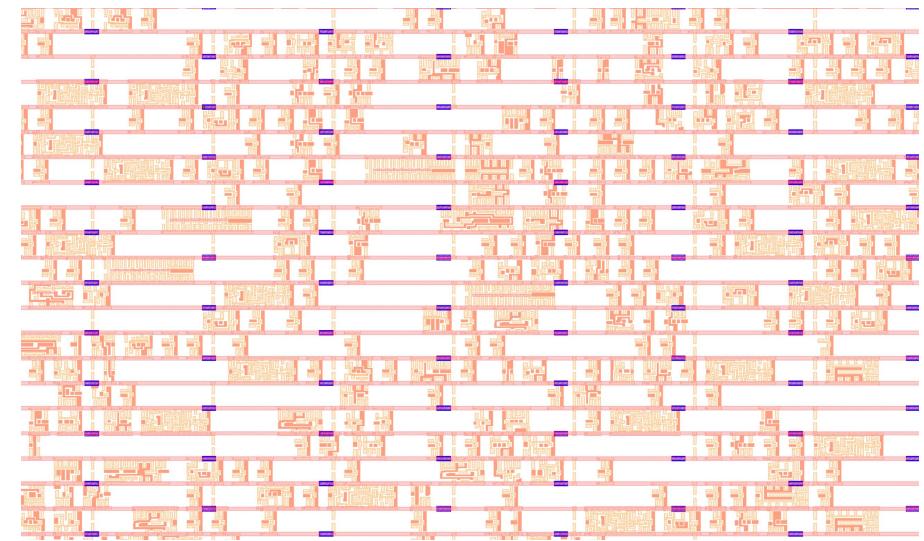
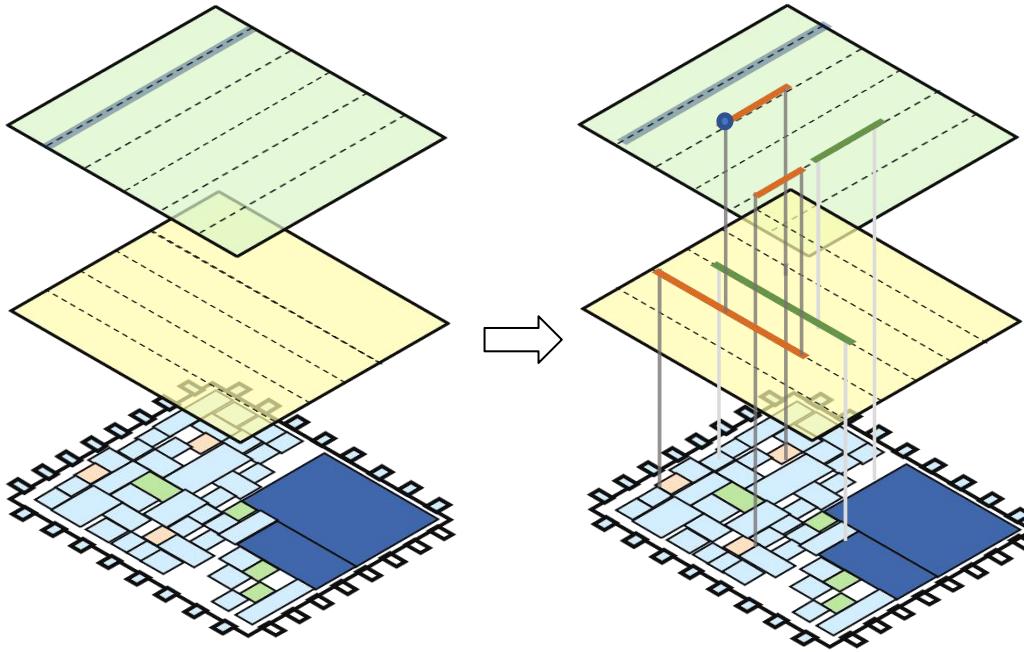
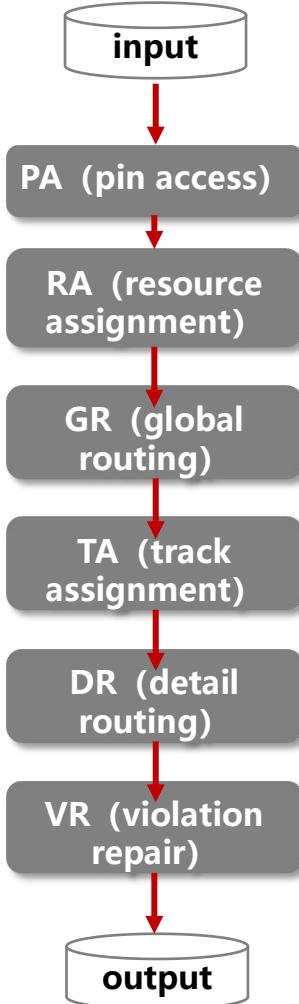
- Fanout
- Capacitance
- Slew (transition)

Level	Inst Num	Min Slew	Max Slew	Avg Slew	Violation
1	1210	0.0355823	0.0881141	0.0564704	970
2	204	0.0342527	0.0938317	0.0559007	134
3	80	0.0148774	0.103097	0.0581444	45
4	41	0.00736284	0.102664	0.0516092	20
5	22	0.0175251	0.103516	0.0535373	9
6	13	0.0116574	0.0884235	0.0402797	4
7	7	0.00706415	0.101609	0.0506611	3
8	4	0.015983	0.0220045	0.0188449	0
9	2	0.0259563	0.0286678	0.027312	0
10	1	0	2.22507e-388	0	0

Net / InstPin	NextRuntime	TranTime	TranJack	CellPort	Remark	
sdram.clk_o	0.800e/0.800f	1.583e/1.494f	-0.783e/-0.694f	CKED024BWP35P140/I	R	
sdram.clk_o_15397_buf:I	0.800e/0.800f	1.537e/1.446f	-0.737e/-0.646f	INVD1BWP40P140LV/TZN	R	
u0_soc_top/u0_sdram_axi_u_core/U300:ZN	0.800e/0.800f	5.000e/5.000f	5.704e/5.598f	-0.784e/-4.558f	PDXOEDG_V_G/XOUT	R
u0_clk_xout	0.800e/0.800f	5.000e/5.000f	5.704e/9.598f	-0.784e/-4.558f	PDXOEDG_V_G/XOUT	R
u1_clk_xout	0.800e/0.800f	5.000e/5.000f	5.704e/9.598f	-0.784e/-4.558f	PDXOEDG_V_G/XOUT	R
clk_hs_peri	0.800e/0.800f	0.850e/0.880f	-0.050e/-0.080f	CKED024BWP35P140/I	R	
clk_hs_peri_11489_buf:I	0.800e/0.800f	0.850e/0.880f	-0.050e/-0.080f	CKED024BWP35P140/I	R	
u0_rcg/u0_p1_clk	0.267e/0.267f	0.139e/0.138f	0.078e/0.078f	CKRXZD4BWP40P140LV/T11	R	
u0_rcg/u0_p1_clk	0.267e/0.267f	0.000e/0.000f	0.267e/0.267f	PLTS28HMLAINT/FOUTPOSTDIV	R	
u0_rcg/u0_p1_clk	0.267e/0.267f	0.000e/0.000f	0.267e/0.267f	PLTS28HMLAINT/FOUTPOSTDIV	R	
clk_core	0.800e/0.800f	0.522e/0.533f	0.278e/0.267f	CKED04BWP35P140/I	R	
clk_core_1724_buf:I	0.800e/0.800f	0.522e/0.533f	0.278e/0.267f	CKED04BWP35P140/I	R	
clk_hs_peri	0.800e/0.800f	0.519e/0.568f	0.281e/0.232f	INVD1BWP40P140LV/T/I	R	
u0_soc_top/u0_sdram_axi_u_core/U300:I	0.800e/0.800f	0.437e/0.437f	0.080e/0.056f	BUFOBWP30P140LV/T/I	R	
fanout_buf_40:I	0.437e/0.437f	0.080e/0.056f	0.339e/0.381f	BUFOBWP30P140LV/T/I	R	

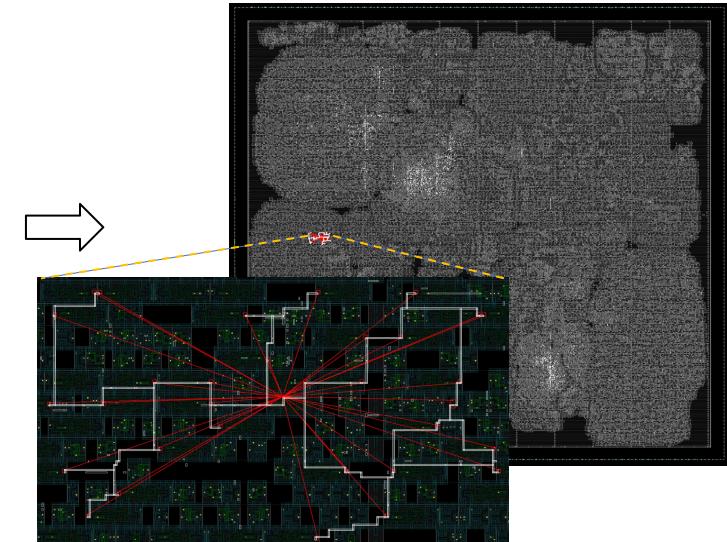
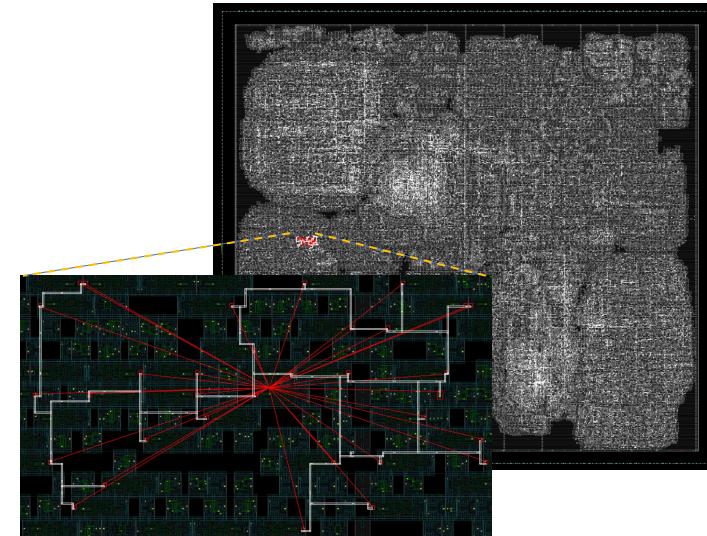
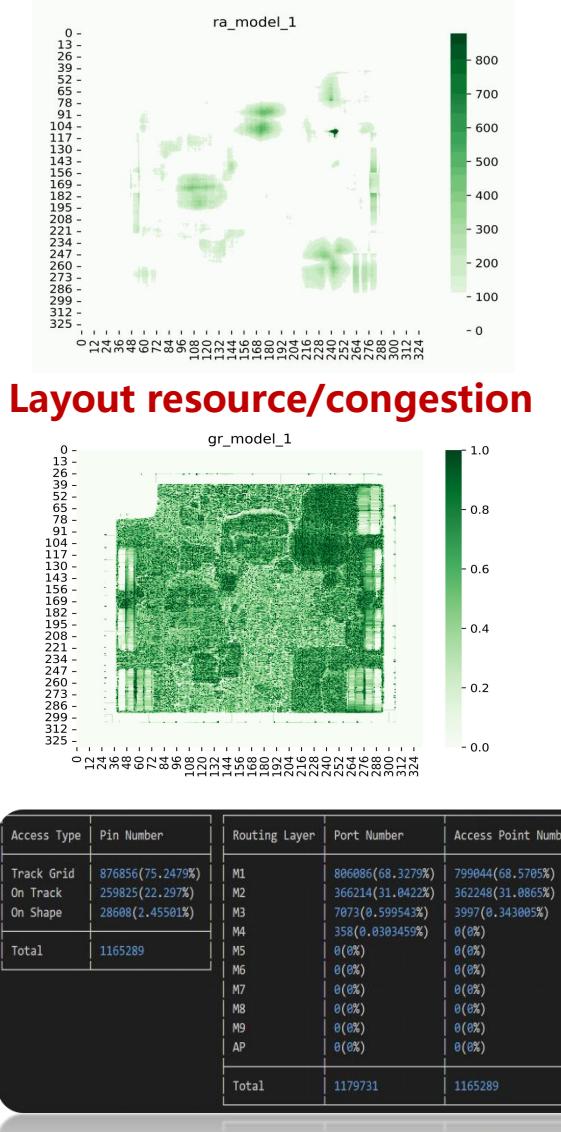
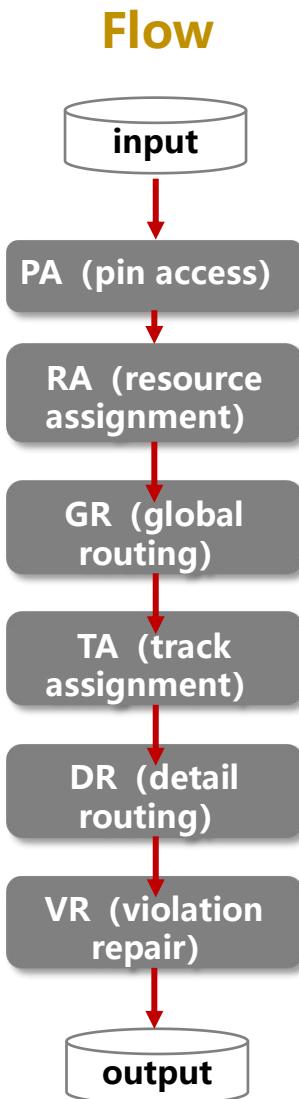
Routing (iRT)

Flow



- **Optimization metrics:** wirelength, timing, congestion, DRC
- **Optimization operations:** Global routing: Track allocation: Detailed routing
- **Routing algorithms:** Pattern routing, A* routing, Steiner tree, Non-linear programming, Integer programming

Routing (iRT)



Access Type	Pin Number	Routing Layer	Port Number	Access Point Number
Track Grid	876856(75.2479%)	M1	806086(68.3279%)	799044(68.5705%)
On Track	259825(22.297%)	M2	366214(31.0422%)	362248(31.8865%)
On Shape	28608(2.45501%)	M3	7073(0.599543%)	3997(0.343005%)
	Total 1165289	M4	358(0.038345%)	0(0%)
		M5	0(0%)	0(0%)
		M6	0(0%)	0(0%)
		M7	0(0%)	0(0%)
		M8	0(0%)	0(0%)
		M9	0(0%)	0(0%)
		AP	0(0%)	0(0%)
		Total	1179731	1165289

Routing Layer	Wire Length / um	Cut Layer	Via Number	Resource Overflow	GCell Number	Access Overflow	GCell Number
M1	9774(0.117785%)	C0	0(0%)	[0,0,1)	921387(83.1%)	[0,0,1)	1.78338e+06(80.4%)
	846292(10.1985%)	VIA1	595417(30.6475%)	[0,1,0,2)	57544(5.19%)	[0,1,0,2)	108739(4.9%)
M2	1.98405e+06(23.9095%)	VIA2	682833(35.147%)	[0,2,0,3)	51492(4.64%)	[0,2,0,3)	79939(3.6%)
M3	1.78748e+06(21.5406%)	VIA3	400386(20.6088%)	[0,3,0,4)	40084(3.61%)	[0,3,0,4)	90020(4.06%)
M4	1.29642e+06(15.6229%)	VIA4	135600(6.97965%)	[0,4,0,5)	21944(1.98%)	[0,4,0,5)	56112(2.53%)
M5	1.41202e+06(17.016%)	VIA5	89437(4.60353%)	[0,5,0,6)	10780(0.972%)	[0,5,0,6)	36741(1.66%)
M6	960890(11.5795%)	VIA6	38709(1.99244%)	[0,6,0,7)	4140(0.373%)	[0,6,0,7)	30046(1.35%)
M7	539.92(0.00650648%)	VIA7	262(0.0134857%)	[0,7,0,8)	1223(0.11%)	[0,7,0,8)	12155(0.548%)
M8	720(0.00867659%)	VIA8	148(0.0076179%)	[0,8,0,9)	222(0.02%)	[0,8,0,9)	8771(0.395%)
M9				[0,9,1]	74(0.00667%)	[0,9,1]	11881(0.536%)
AP				Total	1942792	Total	2217780

Pin Access

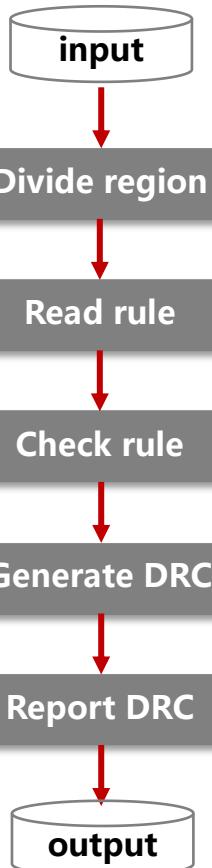
Wirelength and via

DRC Summary	
DRC Type	Number
Cut Different Layer Spacing	433141
Cut EOL Spacing	197803
Cut Enclosure	152168
Cut EnclosureEdge	0
Cut Spacing	358281
Metal Corner Filling Spacing	10443
Metal EOL Spacing	869415
Metal JagToJog Spacing	0
Metal Notch Spacing	733497
Metal Parallel Run Length Spacing	864355
Metal Short	1745445
MinHole	1260
MinStep	670823
Minimal Area	1248072

Design rule check

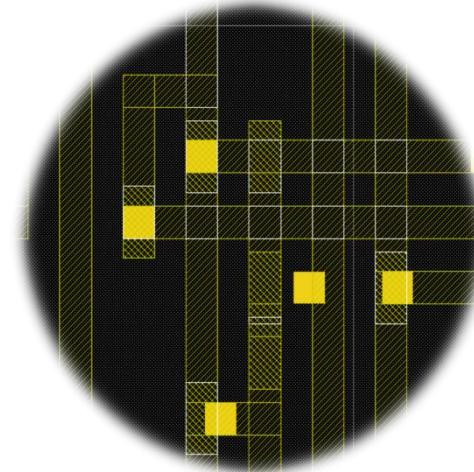
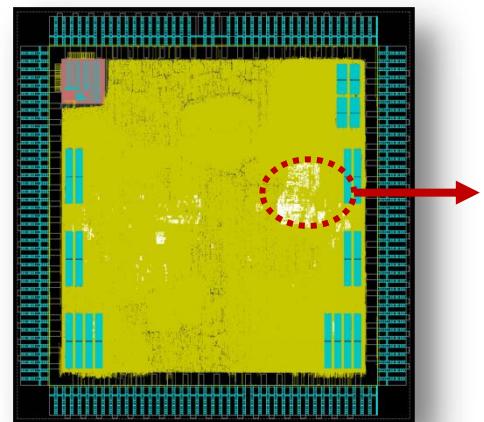
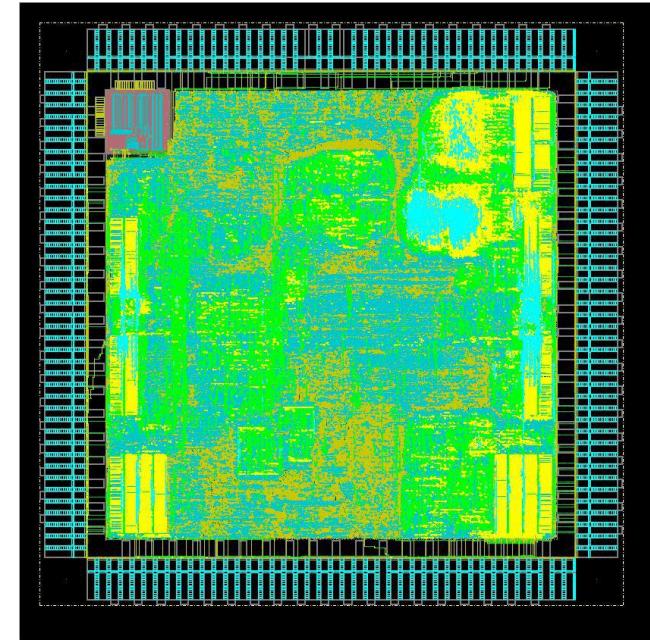
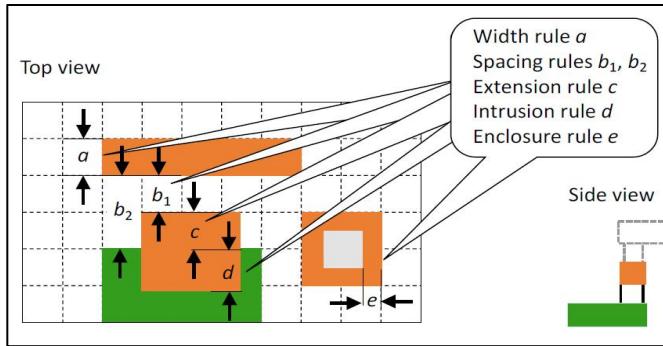
Design Rule Check (iDRC)

Flow



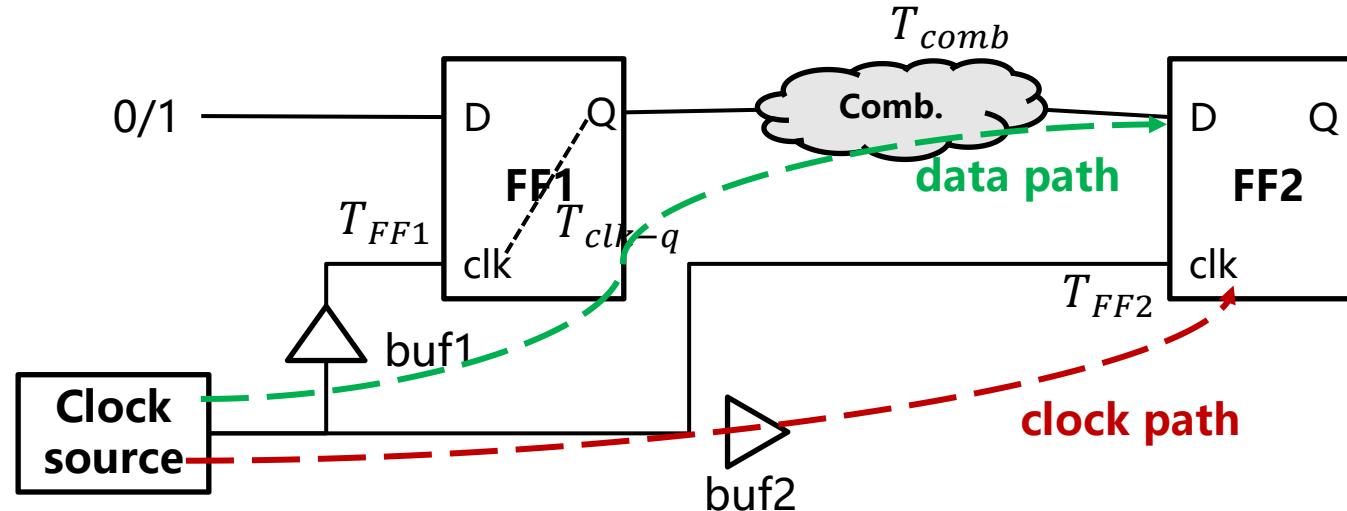
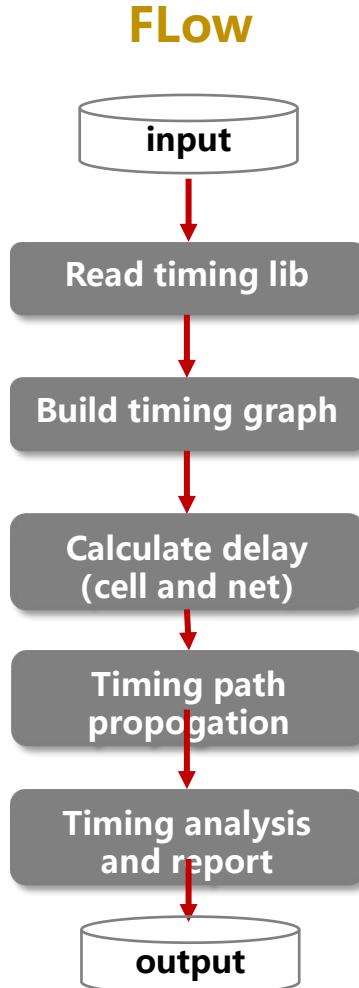
Support DRC Rules:

- Cut Different Layer Spacing
- Cut EOL Spacing
- Cut Enclosure
- Cut Enclosure Edge
- Cut Spacing
- Metal Corner Filling Spacing
- Metal EOL Spacing
- Metal JogToJog Spacing
- Metal Notch Spacing
- Metal Parallel Run Length Spacing
- Metal Short
- MinHole
- MinStep
- Minimal Area



**DRC
Visualization**

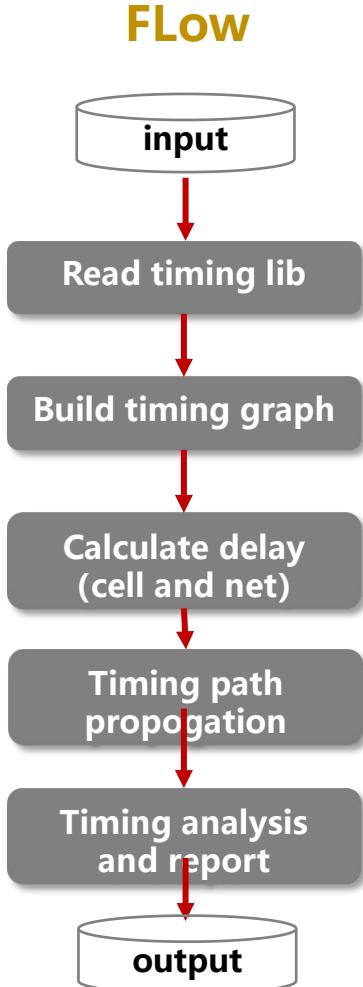
Static Timing Analysis (iSTA)



$$T_{FF1} + T_{clk-q} + T_{comb} + T_{setup} - T_{FF2} - T = T_{slack}^{late} \geq 0 \quad \text{Setup Constraint}$$

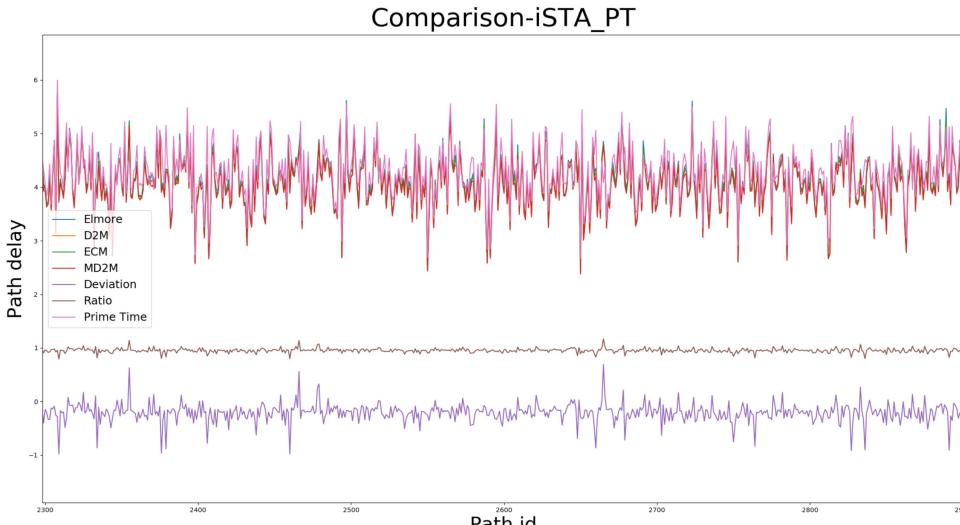
$$T_{FF1} + T_{clk-q} + T_{comb} - T_{hold} - T_{FF2} = T_{slack}^{early} \geq 0 \quad \text{Hold Constraint}$$

Static Timing Analysis (iSTA)



Feature
Support hierarchy netlist and def
Basic setup/hold analysis
Support NLDM/Elmore
Support CCS model
Support high-level net delay model
Support sdf mark
OCV
AOCV
POCV
Consider IRDrop analysis on multi-voltage domain
Hierarchy analysis
Crosstalk analysis
clock gate analysis
Latch analysis

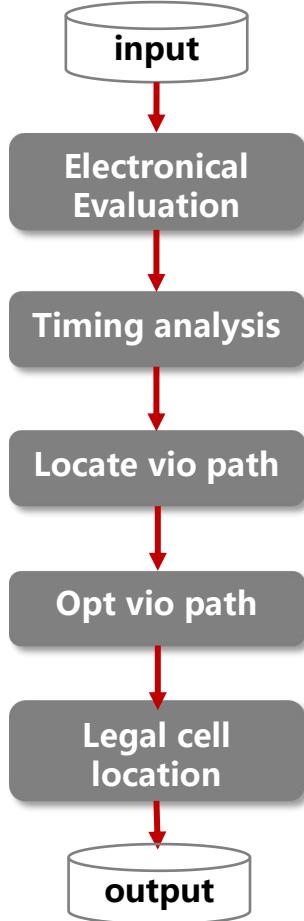
Point	Fanout	Capacitance	Resistance	Transition	Delta Delay	Derate	Incr	Path
u1_clk:XC (PDXOEDG_V_G)						1.000	0.000	0.000r
sys_clk_100m (clock net)	1	0.002	0.000	0.000	0.000	1.000	0.000	0.000r
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)	1	0.002	0.000	0.000	0.000	1.000	0.000	0.000r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)	1	0.002	0.000	0.006	0.000	0.885	0.011	0.011r
sys_clk_100m_buf (clock net)	2	0.001	0.000	0.006	0.000	1.000	0.000	0.011r
u0_rcg/u1_lv1_ckmux2hdv4:IO (CKMUX2D4BWP40P140LVT)	2	0.006	0.000	0.018	0.000	0.885	0.032	0.043r
u0_rcg/u1_lv1_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)	5	0.001	0.000	0.018	0.000	1.000	0.000	0.043r
u0_rcg/mux_core_clk (clock net)	5	0.001	0.000	0.018	0.000	0.885	0.021	0.064r
u0_rcg/mux_core_clk_0_buf:I (CKBD4BWP35P140)	17	0.008	0.000	0.015	0.000	1.000	0.000	0.043r
u0_rcg/mux_core_clk_0_buf:Z (CKBD4BWP35P140)	17	0.000	0.000	0.015	0.000	0.885	0.064	0.064r
u0_rcg/mux_core_clk_0_(clock net)	17	0.001	0.000	0.009	0.000	1.000	0.000	0.109r
u0_rcg/mux_core_clk_div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)	1	0.001	0.000	0.009	0.000	1.000	0.000	0.109r
clock CLK_u1_clk_XC (rise edge)						0	0	0
clock network delay (propagated)						0.064	0.064	0.064
u0_rcg/mux_core_clk_div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)	1	0.000	0.000	0.015	0.000	1.000	0.000	0.064r
u0_rcg/mux_core_clk_div3/gt_en1_reg:Q (DFSNQD1BWP40P140LVT)	1	0.001	0.000	0.009	0.000	0.820	0.045	0.109r
u0_rcg/mux_core_clk_div3/gt_en1_(net)	1	0.001	0.000	0.009	0.000	1.000	0.000	0.109r
u0_rcg/mux_core_clk_div3/U_G1:E (CKLNQD4BWP40P140LVT)	1	0.001	0.000	0.009	0.000	1.000	0.000	0.109r
u1_clk:XC (PDXOEDG_V_G)						1.000	0.000	0.000r
sys_clk_100m (clock net)	1	0.002	0.000	0.000	0.000	1.000	0.000	0.000r
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)	1	0.002	0.000	0.006	0.000	1.039	0.013	0.013r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)	1	0.002	0.000	0.006	0.000	1.039	0.038	0.051r
sys_clk_100m_buf (clock net)	2	0.001	0.000	0.006	0.000	1.000	0.000	0.013r
u0_rcg/u1_lv1_ckmux2hdv4:IO (CKMUX2D4BWP40P140LVT)	2	0.006	0.000	0.018	0.000	1.039	0.038	0.051r
u0_rcg/u1_lv1_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)	5	0.001	0.000	0.018	0.000	1.000	0.025	0.076r
u0_rcg/mux_core_clk (clock net)	5	0.001	0.000	0.015	0.000	1.000	0.000	0.076r
u0_rcg/mux_core_clk_0_buf:I (CKBD4BWP35P140)	17	0.008	0.000	0.009	0.000	NA	0.000	0.076r
u0_rcg/mux_core_clk_0_buf:Z (CKBD4BWP35P140)	17	0.000	0.000	0.009	0.000	NA	0.000	0.076r
u0_rcg/mux_core_clk_div3/gt_en1_(net)	17	0.001	0.000	0.009	0.000	NA	0.000	0.076r
clock CLK_u1_clk_XC (rise edge)						0	0	0
clock network delay (propagated)						0.076	0.076	0.076
library hold time						0.000	0.000	0.076
clock reconvergence pessimism						-0.011	0.064	0.045
data require time							0.064	
data arrival time							0.109	
slack (MET)							0.045	



pt/ista ratio	value
mean	1.11
variance	0.00095
median	1.107
maximum	1.5404
minimum	0.9035

Timing Optimization (iTO)

Flow



Key parameter config	
Input	iPL.def, iCTS.def
output	iTO_setup_result.def, iTO_hold_reslut.def
setup_slack_margin	setup slack value
hold_slack_margin	hold slack value
max_buffer_percent	Area ratio of inserted buffer
max_utilization	Core utilization
DRV_insert_buffers	Available buffer for optimizing DRV
setup_inser_t_buffers	Available buffer for optimizing setup
hold_insert_buffers	Available buffer for optimizing hold
number_passes_allowed_decreasing_slack	The number of times that WNS is allowed continuously decrease when opt setup
rebuffer_max_fanout	For setup, a wire network is not optimized for buffer insertion when its fanout exceeds this value
split_load_min_fanout	For setup, fanout is reduced by inserting a buffer when fanout is greater than this value

DRV report

```

path
Worst Slack: -5.88383
Found 3 slew violations.
Found 11 capacitance violations.
Found 0 fanout violations.
Found 0 long wires.
Before ViolationFix | slew_vio: 3 cap_vio: 11 fanout_vio: 0 length_vio: 0
The 1th check
After ViolationFix | slew_vio: 3 cap_vio: 0 fanout_vio: 0 length_vio: 0
The 2th check
After ViolationFix | slew_vio: 0 cap_vio: 0 fanout_vio: 0 length_vio: 0
DRV_net_3
Inserted 11 buffers in 12 nets.
Resized 0 instances.
  
```

Setup report

```

Inserted 10 hold buffers.

Worst Hold Path Launch : u0_soc_top/u0_sdram_axi/u_core/sample_data0_q_reg_8:CP
Worst Hold Path Capture: u0_soc_top/u0_sdram_axi/u_core/sample_data_q_reg_8:CP

The 1-th timing check.
worst hold slack: -1.28225
Unable to repair all hold violations. There are still 16 endpoints with hold violation.
Max utilization reached.
  
```

Clock Group	Hold TNS	Hold WNS
CLK_chiplink_tx_clk	0	0
CLK_clk_hs_peri	-185.768	-1.27825
CLK_div2_core	-2006.7	-0.106129
CLK_div2_hs_peri	-216.759	-0.028571
CLK_div3_hs_peri	-72.5124	-0.028571
CLK_div4_core	-1304.1	-0.106129
CLK_div4_hs_peri	-185.768	-1.27825
CLK_div4_peri	-231.408	-0.042802
CLK_sdram_clk_o	0	0
CLK_spi_clk	0	0
CLK_spi_clk_out	0	0
CLK_u0_chiplink_rx_clk_pad_PAD	-89.8732	-0.028408
CLK_u0_clk_XC	-2987.42	-0.106129
CLK_u0_pll_FOUTPOSTDIV	-8546.64	-0.106129
CLK_u1_clk_XC	-2755.16	-0.106129

Clock Group	Hold TNS	Hold WNS
CLK_chiplink_tx_clk	0	0
CLK_clk_hs_peri	0	0
CLK_div2_core	0	0
CLK_div2_hs_peri	0	0
CLK_div3_hs_peri	0	0
CLK_div4_core	0	0
CLK_div4_hs_peri	0	0
CLK_div4_peri	0	0
CLK_sdram_clk_o	0	0
CLK_spi_clk	0	0
CLK_spi_clk_out	0	0
CLK_u0_chiplink_rx_clk_pad_PAD	0	0
CLK_u0_clk_XC	0	0
CLK_u0_pll_FOUTPOSTDIV	0	0
CLK_u1_clk_XC	0	0

Hold report

- Fix timing design rule violation
 - Max cap/Max slew/Max wirelength/Max fanout
- Fix hold time
- Fix setup time
- Cell sizing
- Buffer Insertion
- Load Insertion
- Buffer/load location

Power Analysis (iPA)

Flow



input

Read timing lib

Build power graph

**Data mark
Calculate Toggle**

Toggle and SP Propagation

Calculate and report power



API	Description
buildGraph	Build iPW graph data structure
readVCD	Parse the VCD file
buildSeqGraph	Build timing subgraph
checkPipelineLoop	Detect PipeLine loop
levelizeSeqGraph	Grade timing subgraph
propagateToggleSP	Propagate Toggle and SP data on the graph
calcLeakagePower	Calculate the leakage power
calcInternalPower	Calculate internal power
calcSwitchPower	Calculate switching power
analyzeGroupPower	Analyze power data
reportPower	Output power report

cases	iPA total power	Innovus total power	deviation
aes_cipher_top	22.22mW	23.74mW	6.4%
gcd	0.38mW	0.37mW	3.6%
uart	0.51mW	0.49mW	3.9%

Generate the report at 2023-05-06T09:54:06

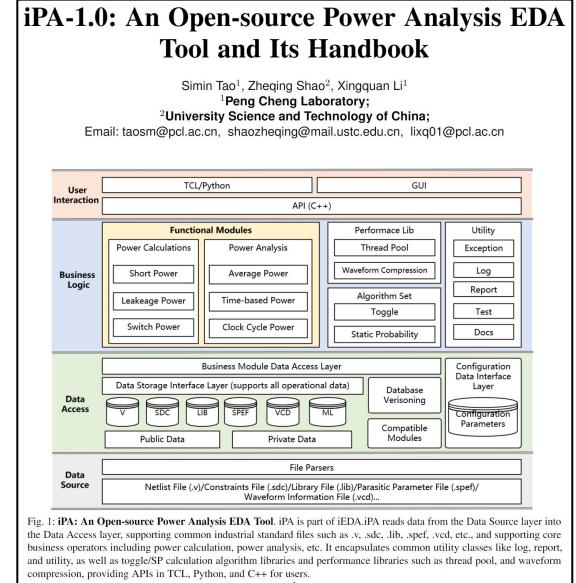
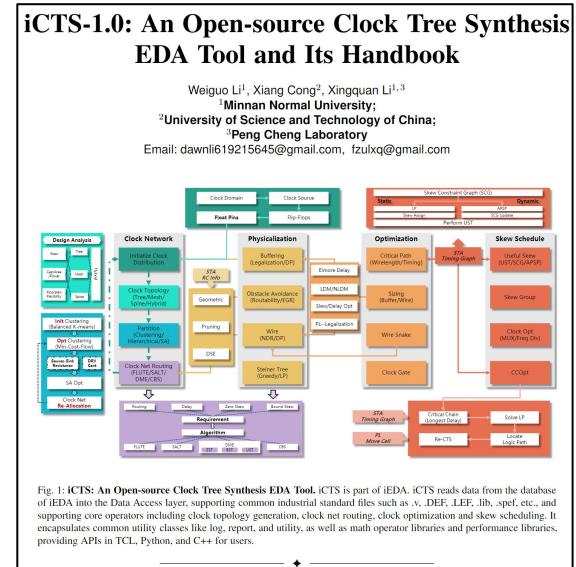
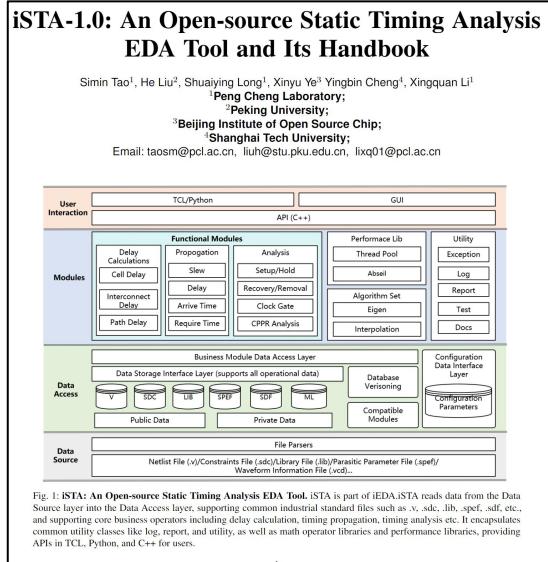
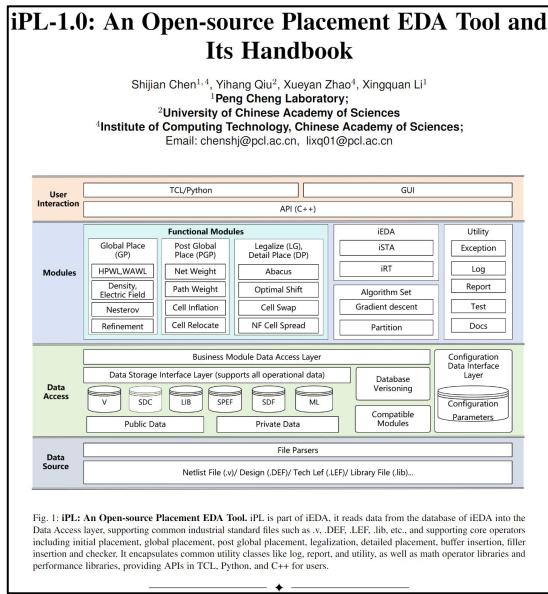
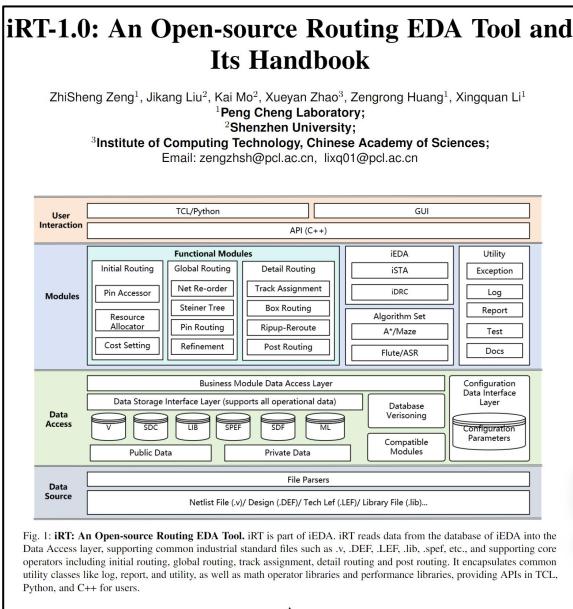
Report : Averaged Power

Power Group	Internal Power	Switch Power	Leakage Power	Total Power (%)
combinational	1.064e-07	5.063e-09	3.079e-08	1.422e-07 (27.595%)
sequential	2.862e-07	7.337e-09	7.963e-08	3.732e-07 (72.405%)
Net Switch Power == 1.240e-08 (2.406%)				
Cell Internal Power == 3.926e-07 (76.173%)				
Cell Leakage Power == 1.104e-07 (21.422%)				
Total Power == 5.154e-07				

- Evaluate power before / during / after the physical design process
- Average model
- Timing window (coming soon)
- VCD parser
- Report/API

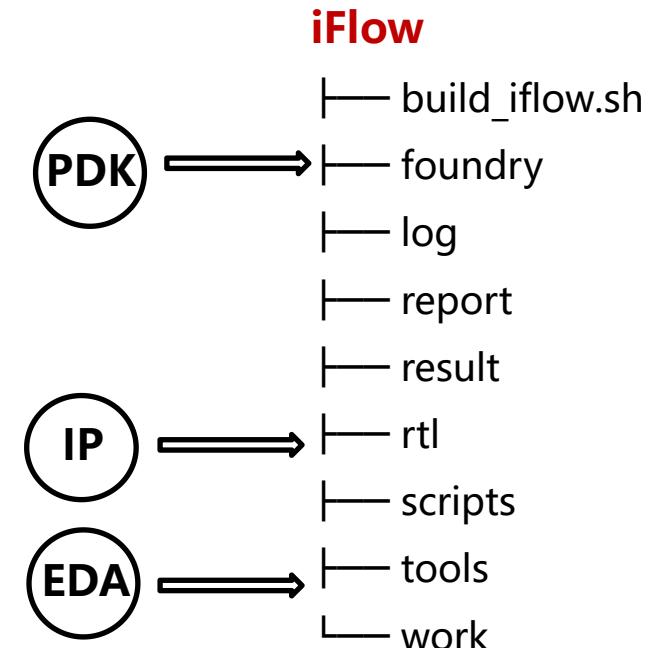
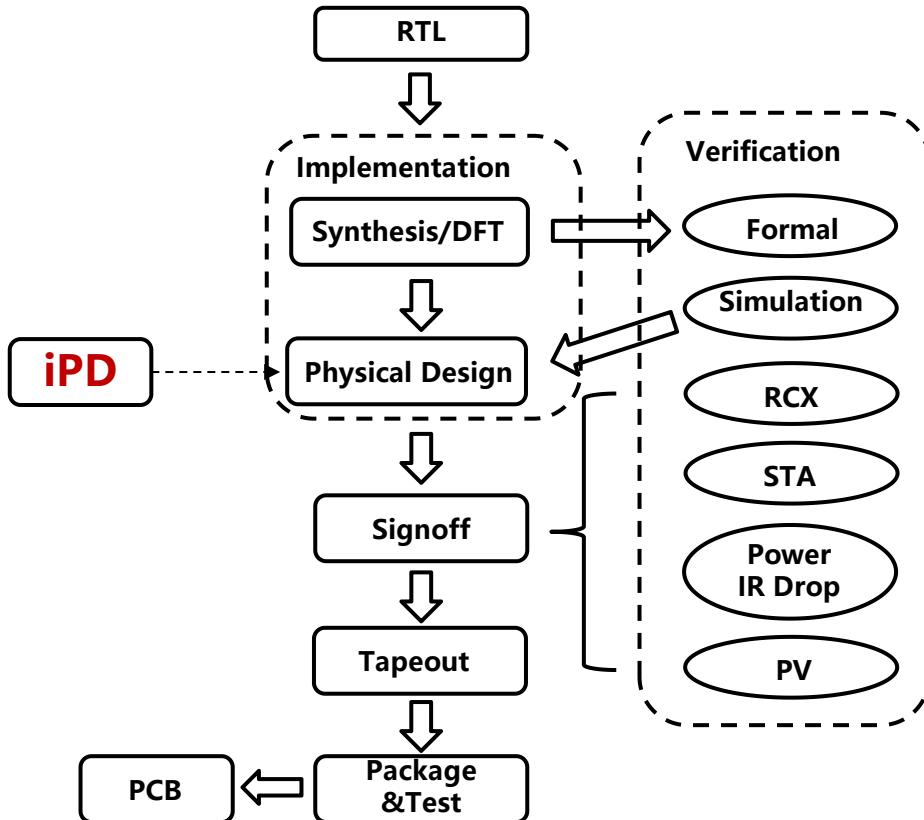
Handbooks (Arxiv)

- Knowledge and Technology
- system
- comprehensive
- new
- practical
- software



iFlow: A Chip Design Flow

- iFlow: supporting different EDA tools, PDKs, designs



Chip design flow

Open-source Count

- **Netlist-to-GDS II**
 - **11 tools, and other 5 tools are R&Ding.**
 - **Design, Analysis, Verification**
- **Repo**
 - EDA infrastructure and physical design
 - Starred: $238+138=376$
 - Fork: $53+21=74$
- **Number of Codes**
 - **>0.3M lines**
 - **exclude 3rd party and history**
- **Contributors**
 - Total: 80 contributors

The screenshot shows the Gitee repository page for the project `OSCC / iEDA`. The repository has 2,111 commits, 3 branches, and 0 tags. It includes sections for Readme, View license, Activity, Custom properties, 238 stars, 3 watching, 21 forks, Report repository, Releases (No releases published), Packages (No packages published), Contributors (25), and Languages (C++ 88.8%, Verilog 4.4%).

Code

- !14 Fix: iT0 generates the wrong result path (e400704 - last week)
- init repo of OSCC/iEDA (.gitee)
- feature:support IR rust and C operation (cmake)
- finish iPL Timing-driven placement (docs)
- refactor: intergrate eval tcl commands (scripts)
- Fix: Wrong Output Path (src)
- !1 update230508 (.clang-format)
- !1 update230508 (.clang-tidy)
- update dockerfile (.dockerignore)
- feature:support build liberty rust data (.gitignore)
- update src/third_party/mt-kahypar submodule. (.gitmodules)
- feature:add rust cmake (CMakeLists.txt)
- update dockerfile (Dockerfile)
- fix typo from LICENSE (LICENSE)
- Merge branch 'master' of gitee.com:oscc-project/iEDA into ... (README-CN.md)
- Merge branch 'master' of gitee.com:oscc-project/iEDA into ... (README.md)
- Merge branch 'master' of gitee.com:oscc-project/iEDA into ... (build.sh)

Contributors 25

Languages

- C++ 88.8%
- Verilog 4.4%

Community

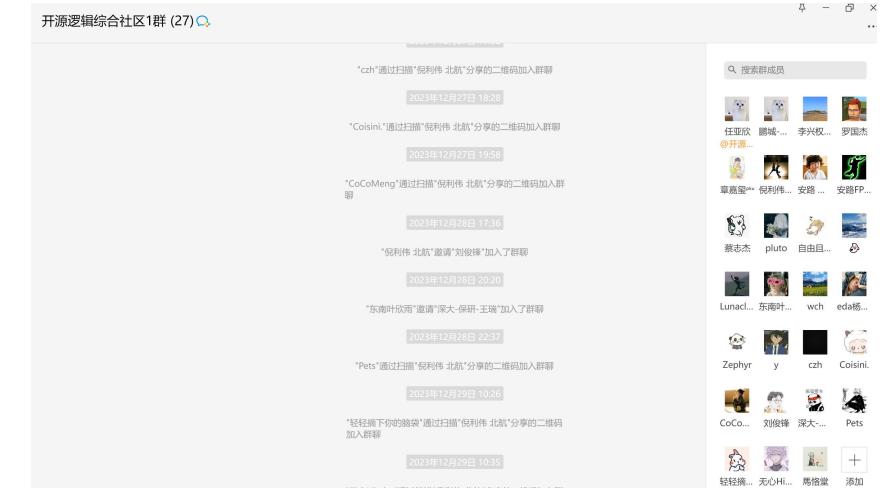
- User

- Wechat Group
 - ~1000 Peoples



- Contributor

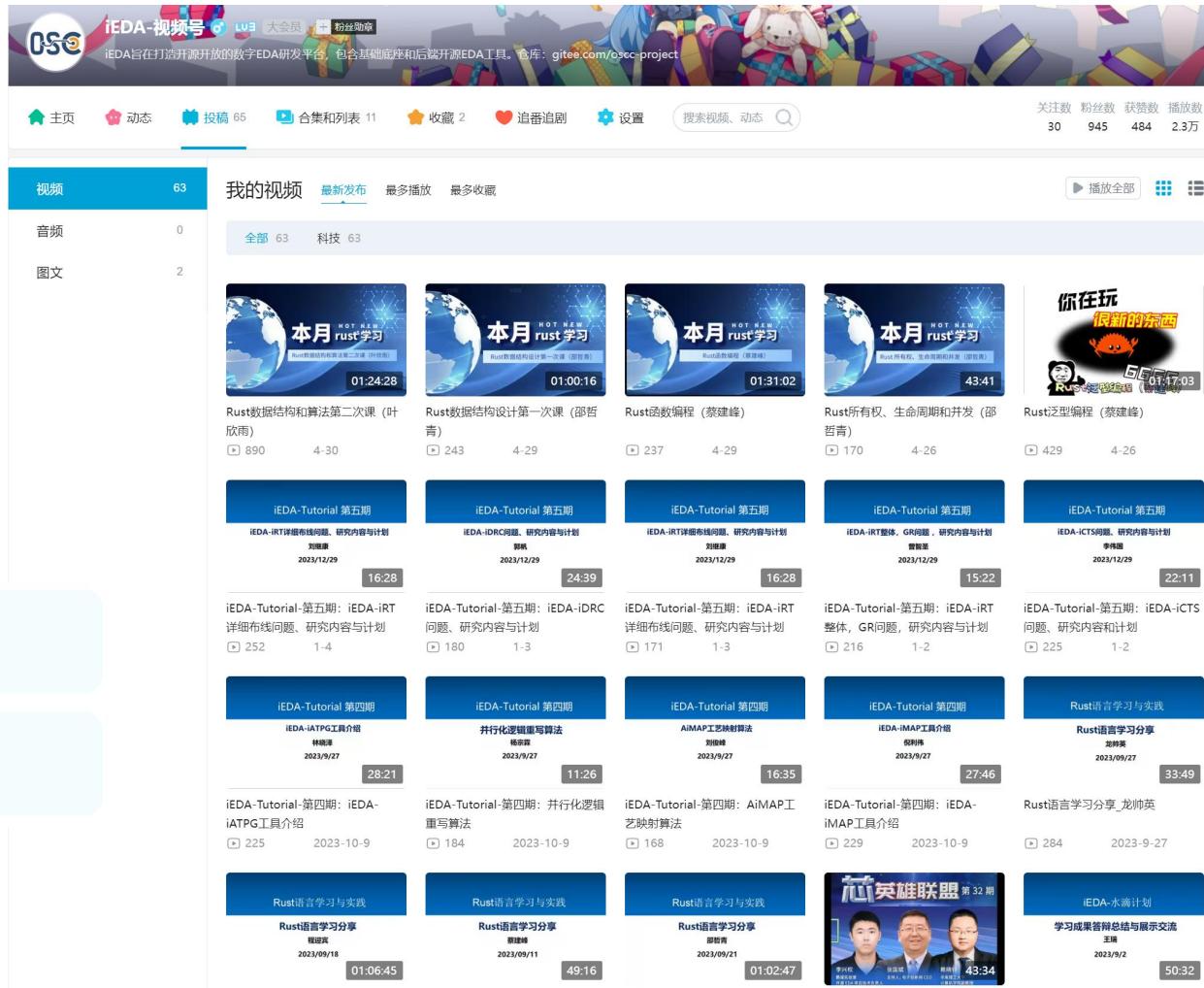
- Logic Synthesis Community ;
 - Committee: ICT, Anlogic、PKU、PCL、BUPT、CUHK、Giga-da、Ninecore
 - Community: 27 contributors



Lecture Videos (Bilibili)

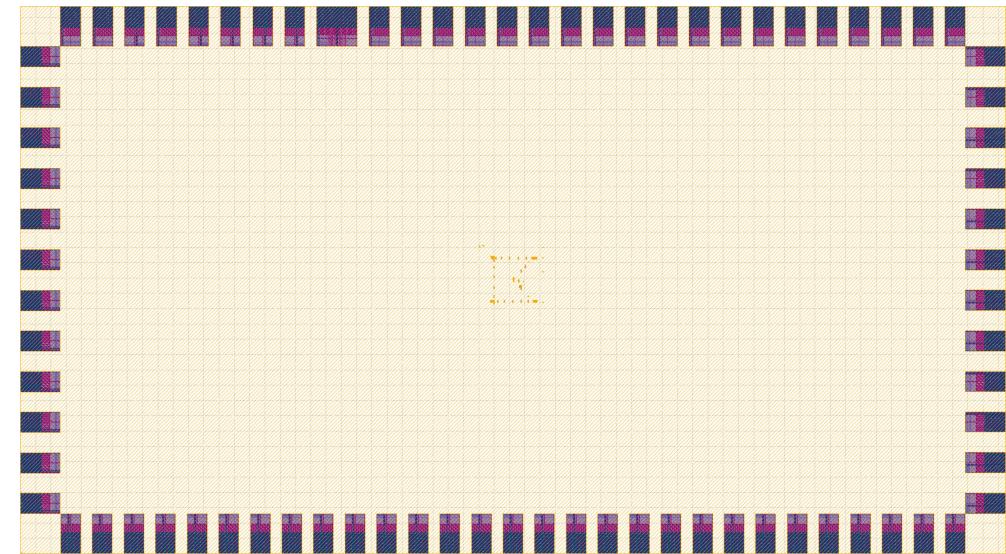
• Lecture Videos

- Basic EDA Knowledge,
- Frontiers in EDA Lectures,
- iEDA Development Process and Tools,
- Chip Design Using iEDA Tools,
- Related EDA Technologies.



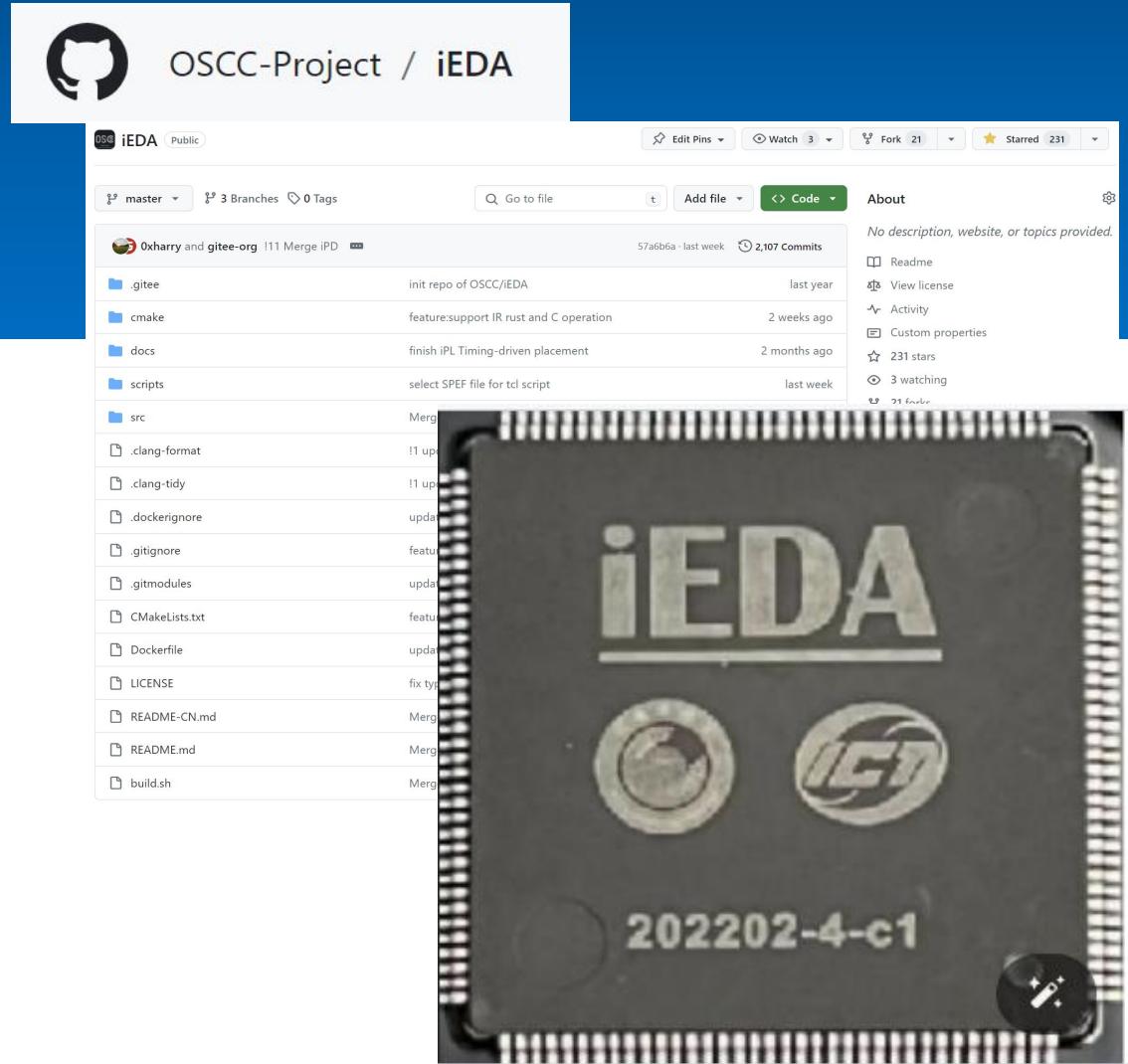
iEDA Objective

- **iEDA Objective**
 - EDA Infrastructure
 - Explore new and efficient EDA R&D method
 - High quality and performance EDA tool
- **Open-source: (Gitee/Github)**
 - Gitee: <https://gitee.com/oscc-project/iEDA>
 - GitHub: <https://github.com/OSCC-Project/iEDA>
 - Gitlink: <gitlink.org.cn/OSchip/iEDA>
 - OpenI: <openipcl.ac.cn/OSCC/iEDA>
- **ISEDA 2023 Best Paper Award**
 - iEDA: An Open-source Intelligent Physical Implementation Toolkit and Library, ISEDA, 2023.



iEDA Tutorial Agenda

- **Part 0:** iEDA Overview (**Xingquan Li**)
- **Part 1:** iEDA Infrastructure (**Zengrong Huang**)
- **Part 2:** iPL: Placement Tool and Its Technology (**Shijian Chen**)
- **Part 3:** iCTS: Clock Tree Synthesis Tool and Its Technologies (**Weiguo Li**)
- **Part 4:** iRT: Routing Tool and Its Technologies (**Zhisheng Zeng**)
- **Part 5:** iSTA: Static Timing Analysis Tool and Its Technologies (**Simin Tao/He Liu**)
- **Part 6:** iPA: Power Analysis Tool and Its Technologies (**Siming Tao**)



Thanks

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