ECE 340: Semiconductor Electronics
Section B

Lecture1: Introduction

Wenjuan Zhu

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Fall 2015 • Section B: MWF 10am • ECEB 2015

- **Three lecture/discussion meetings per week**
- **Five sections in parallel: same syllabus, homeworks, exams**
- **Grade = 10% HW, 15% Quiz (3x5%), 40% Midterm (2x20%), 35% Final**

- **Exams:**
  - **Midterm I: Thursday, October 8th (tentative)**
  - **Midterm II: Thursday, November 5th, (tentative)**
  - **Final exam: to be announced**
- **Quizzes: 3x, 10~15 min., unannounced, must be taken in assigned section**
- **Homework: assigned on Friday, need to be turned in at the beginning of the next Friday class**

- **Solutions, other resources on web sites: http://courses.ece.illinois.edu/ece340**
- **Lecture notes: https://wiki.cites.illinois.edu/wiki/display/ece340bfa15/**

- **Prof. Wenjuan Zhu, OH Tuesday 4-5pm, MNTL 3258**
- **Please take advantage of all instructor and TA office hours**
- **Please read Syllabus handout**

- For absence and any logistic issues, please contact course director **Prof. John Dallesasse** in advance.
- For homework grading related issues, contact TA **Ben Kesler**.
- For Compass issues, contact TA **Ardy Winoto**.
- For technical questions, please ask the instructors or TAs in the office hour. (Please do not use emails).

Absence Policy

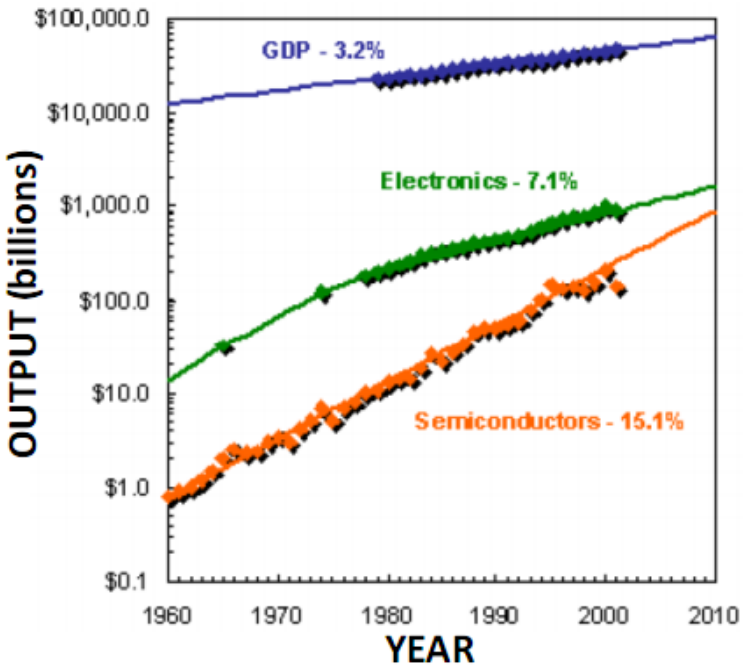
- Any absence for a job interview that requires travel, student athlete related absences, or specific university-related events must be pre-arranged with the course director.
- No excused absences are given for homework – students must make arrangements to have this turned in for them if they will be out for an approved reason on the day that homework is due.
- If the student is absent due to illness, an excused absence will only be given if they are excused by the Dean of Students. They should be aware that the Dean's office is applying a stricter policy with regard to absences due to illness.

Introduction

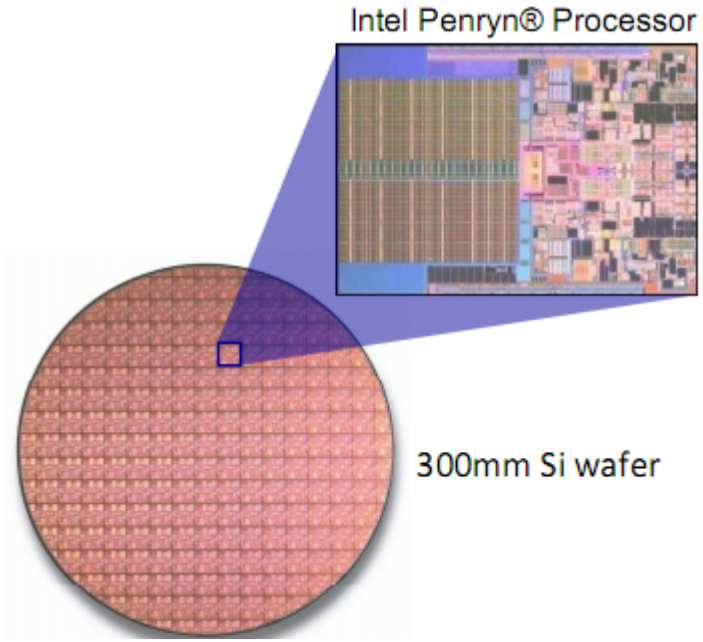
- Questions, questions…

  Why “semiconductors”? Why “electronics”? Why are we here?

- **IC technology advancement over the past 40+ years has had dramatic impact on the way we live, work, and play.**

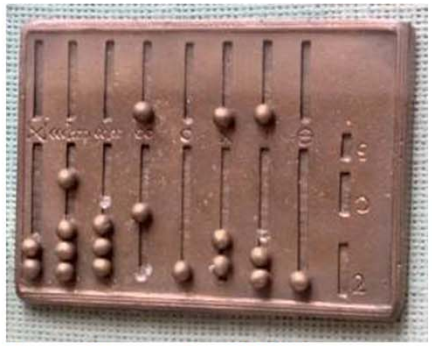


- What's at the heart of all?
  - Semiconductor devices: the brain of all electronics

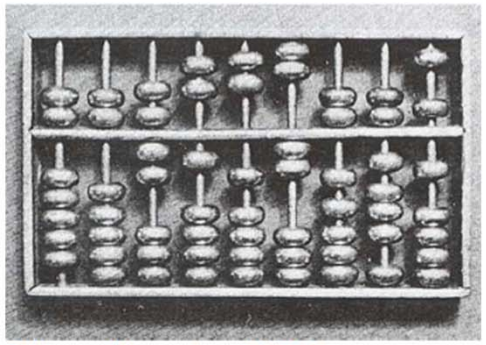


Historical Context

- The abacus, ancient digital memory

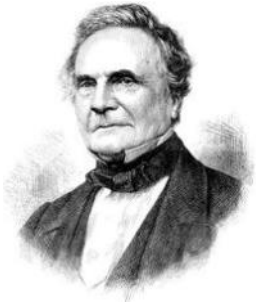


Roman Abacus (ca. 200BC)

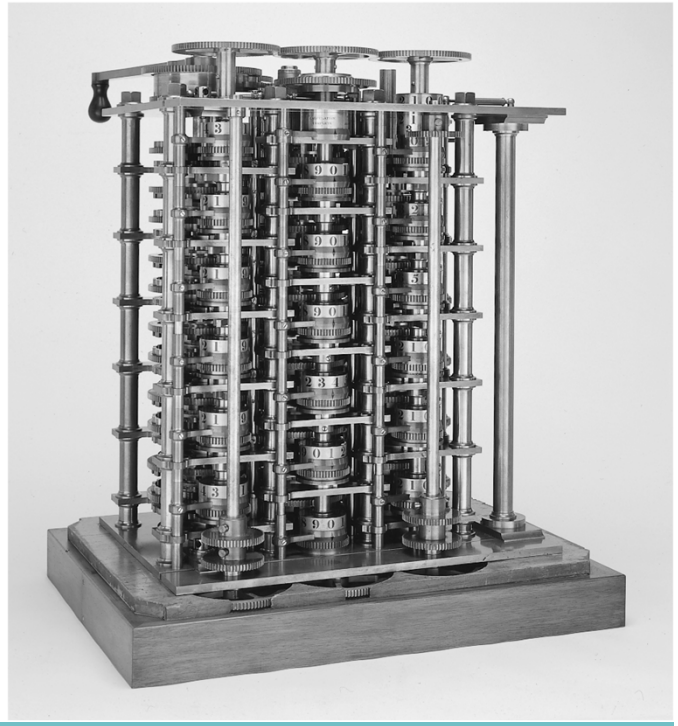


Chinese Abacus (ca. 190AD)

  - Information represented in digital form
  - Each rod is a decimal digit (units, tens, etc.)
  - A bead is a memory device, not a logic gate
- An early mechanical computer
  - The Babbage difference engine, 1832
  - 25,000 parts

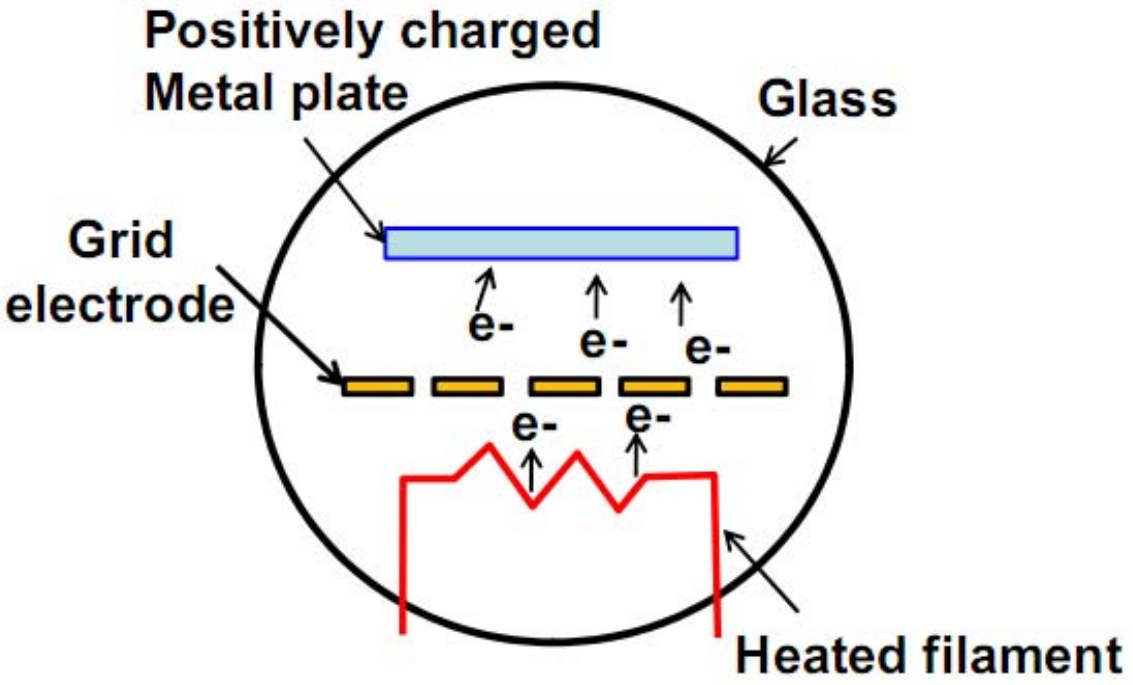


Charles Babbage (Wikipedia)



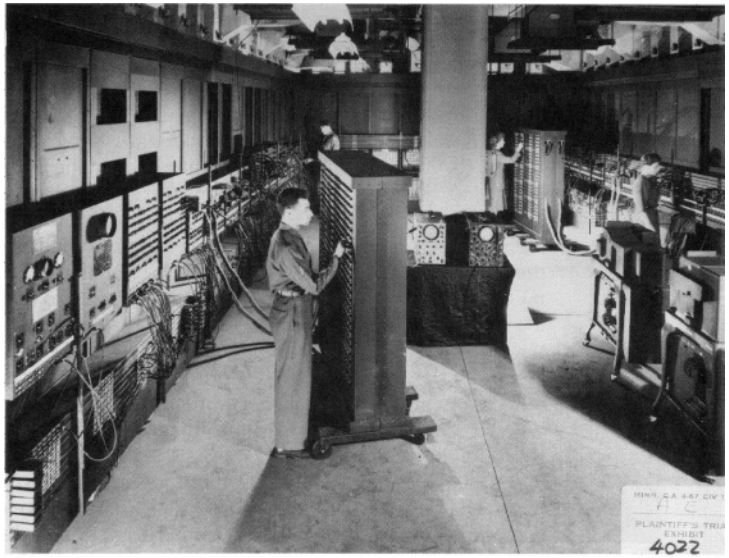
History: vacuum tube

- Thomas Edison invented light bulb in 1879
- Lee DeForest invented vacuum tube triode to amplify weak signals in 1907. He put a third electrode between the filament and plate to control the electron flow



History: vacuum tube computer

- ENIAC: The first electronic computer (1946)
  - 30 tons, including ~20,000 vacuum tubes, relays
  - Punch card inputs, ~5 kHz speed
  - It failed ~every five days

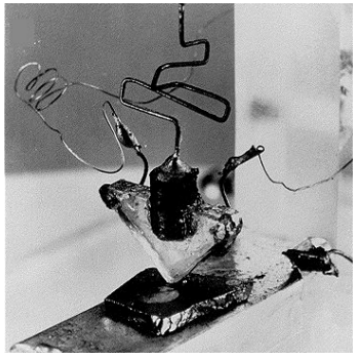


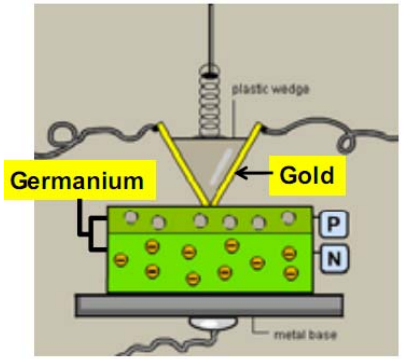
Note: ILLIAC @ UIUC
5 tons, 2800 vacuum tubes
64k memory (1952)

Sources: Wikipedia, http://www.pbs.org/transistor

History: transistor

- The first transistor was invented in 1947 at Bells Labs by Brattain, Bardeen, and Shockley





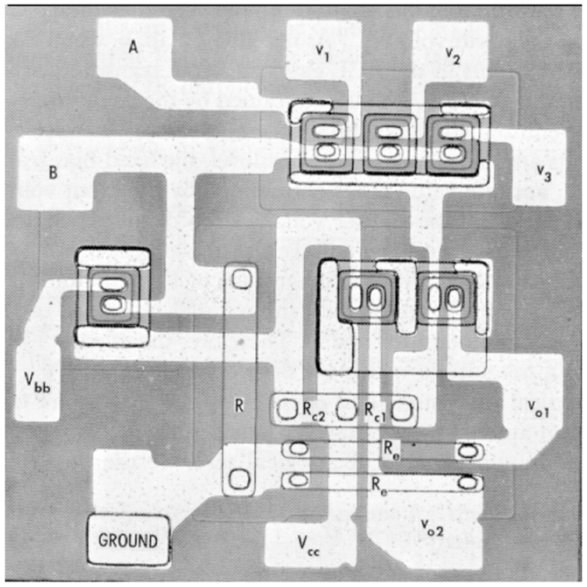
ECE & Physics faculty member at University of Illinois (1952-1991)

Nobel prize 1956 – Transistor

Nobel prize 1972 – Theory of Superconductivity

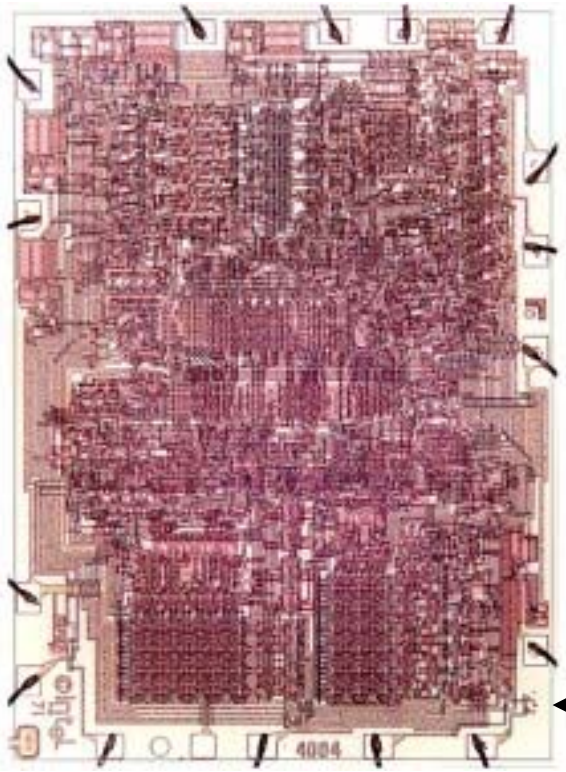
History: integrated circuit

- **The first Integrated circuits was fabricated in 1950s. All transistors and metal interconnects were fabricated on the same piece of silicon substrate**



Jack Kilby

BSEE University of Illinois



- The first microprocessor, Intel 4004 (1971)
- 2250 transistors, 740 kHz operation

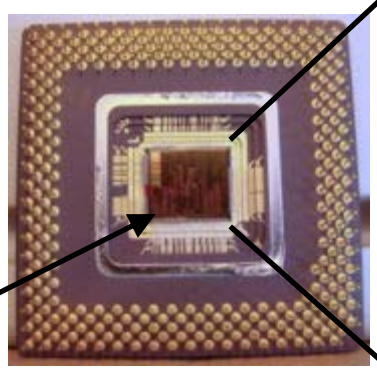
← F.F. = Federico Faggin (designer)

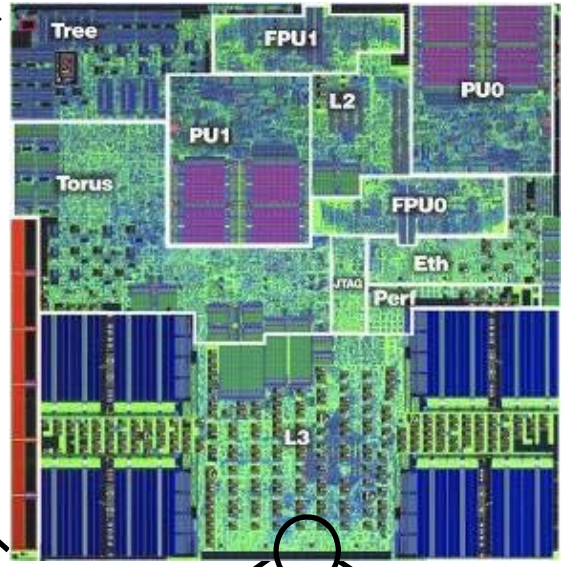
- Comparable computational power with ENIAC
- Built on 2” and then 3” wafers (vs. 12” today)
- 10 μm line widths (vs. 28-45 nm today), 4-bit bus width
- Used in… the Busicom Calculator:
- See http://www.intel4004.com

Followed by 8008 (8-bit), 8080, 8086
Then 80286, 80386, 80486 = i486 (1989, 0.8 μm lines)
Pentium, II, III, Itanium, IV, Celeron, Core 2 Duo, Atom…

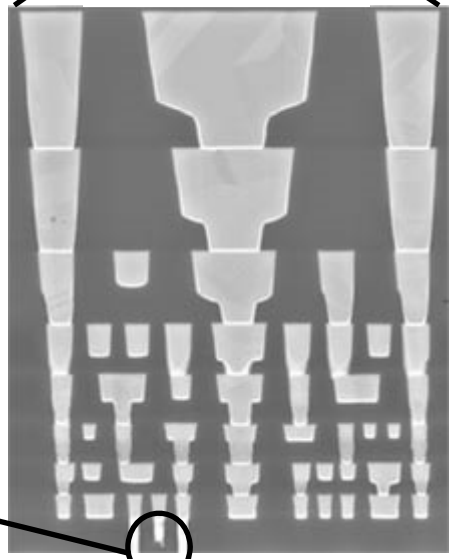
Take the cover off a microprocessor.

Packaged die

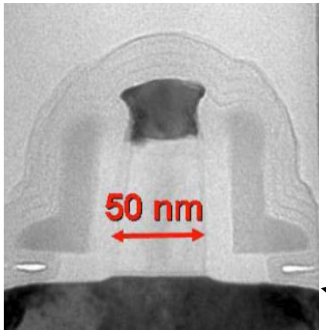




Cross-section



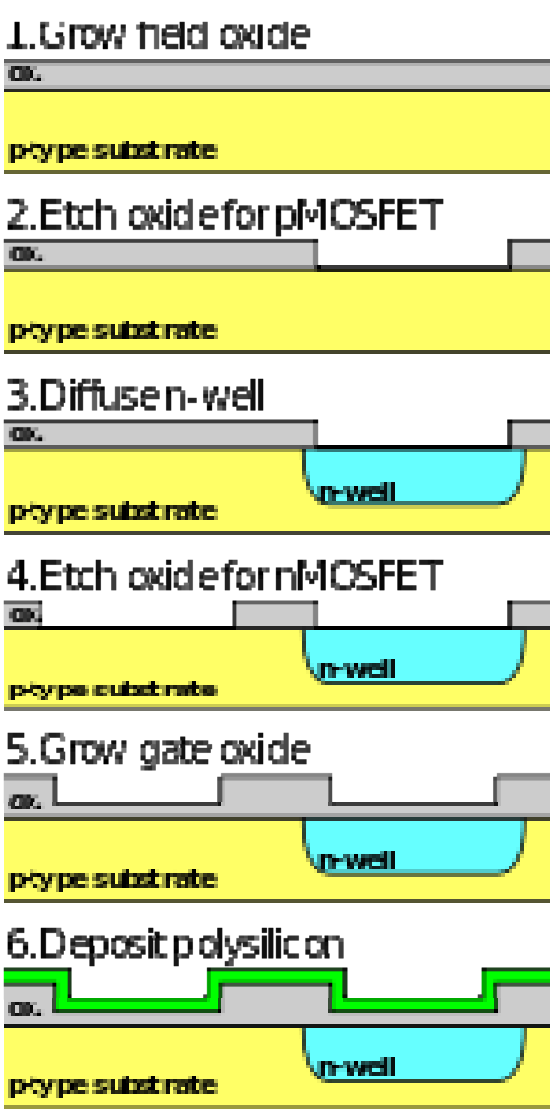
Single transistor

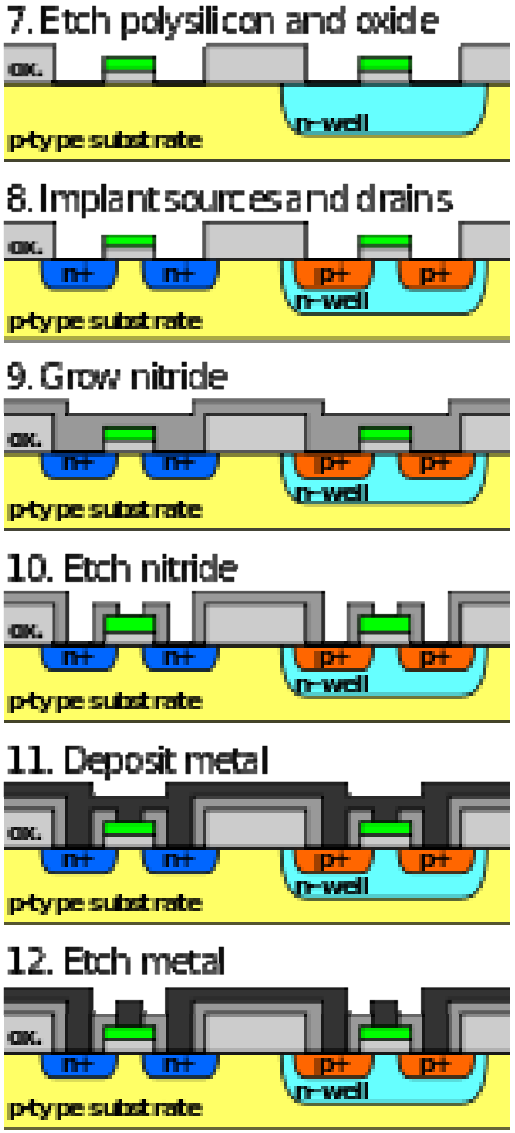


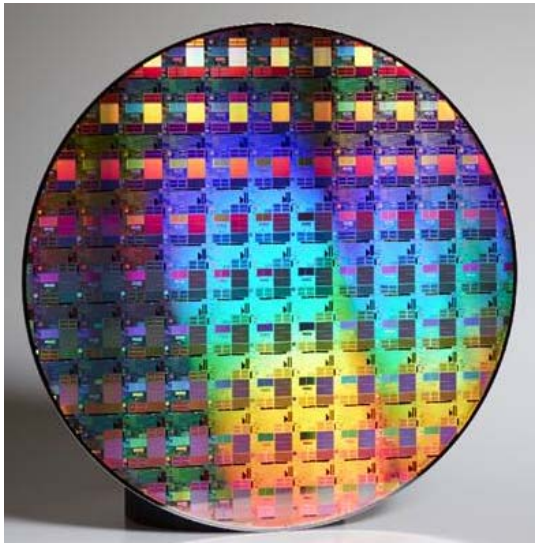
Full wafer (100s of dies)

modern wafers: 200-300 mm diameter (8-12 inches)

CMOS Front-end-of-line process flow

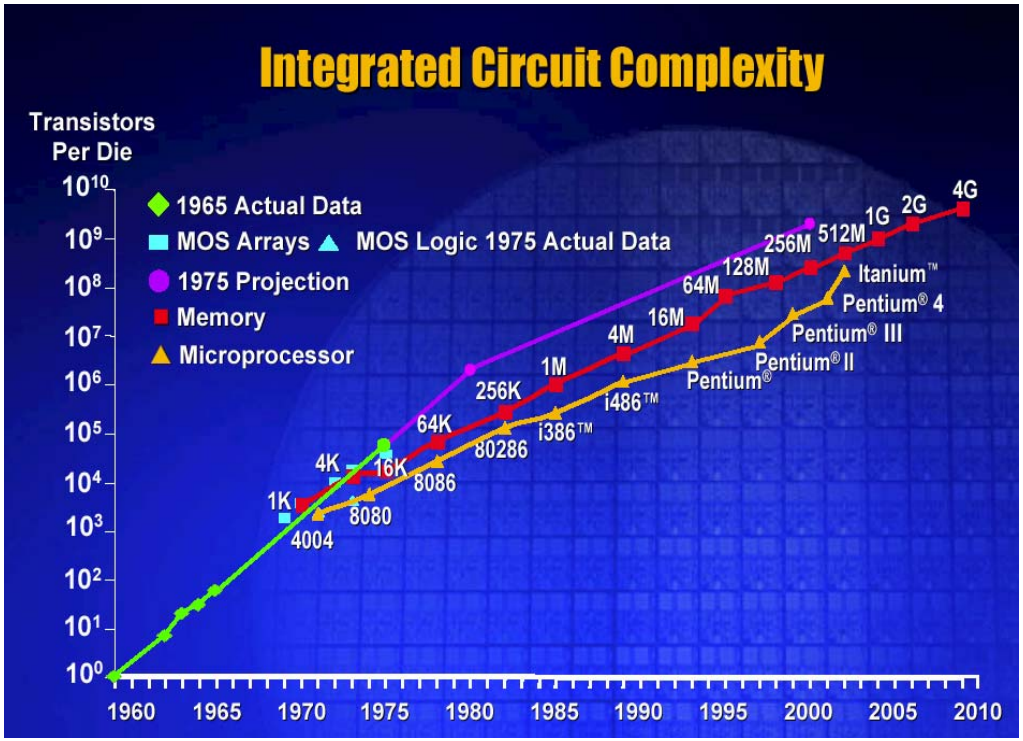




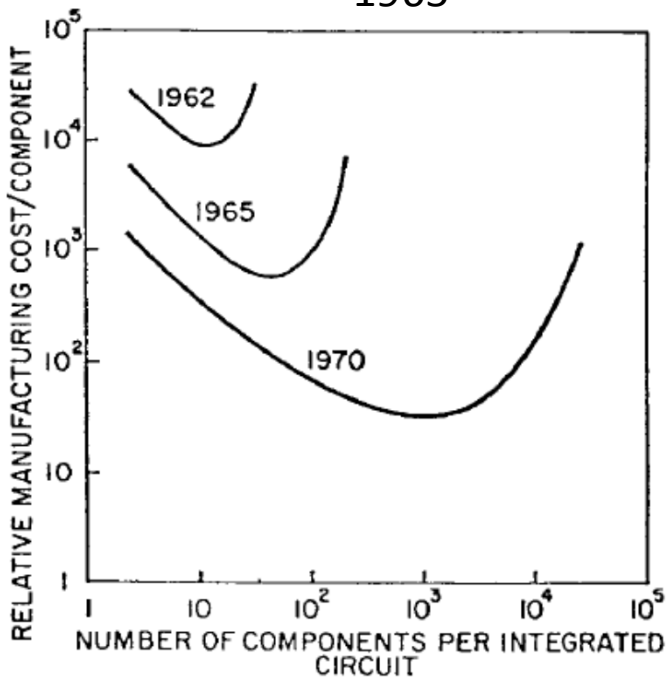


Gordon Moore's "Law"

~ doubling circuit density every 1.5-2 years



1965

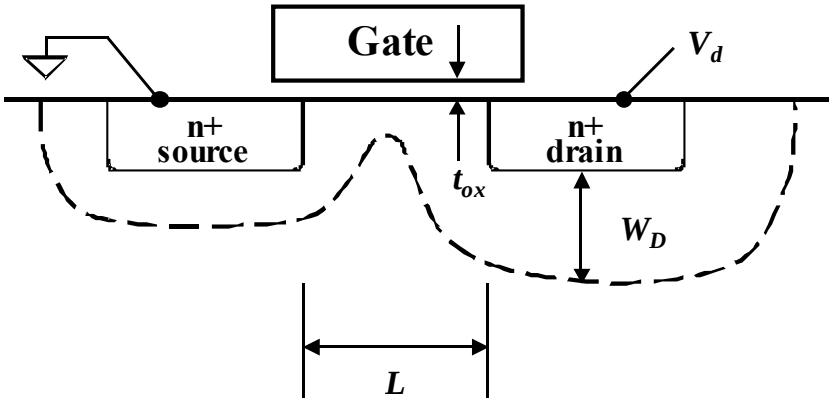


- Approximately 10^{18} transistors were produced in 2011.
- Roughly 50 transistors for every ant in the world

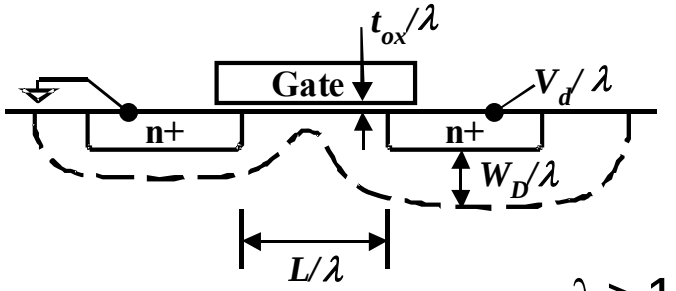
Source: http://www.intel.com

Device Scaling

Original Device



Scaled Device



$\lambda > 1$

Constant field scaling:

Device dimensions	$1/\lambda$
Voltage	$1/\lambda$
Gate Delay Time per device	$1/\lambda$
Power Dissipation per device	$1/\lambda^2$

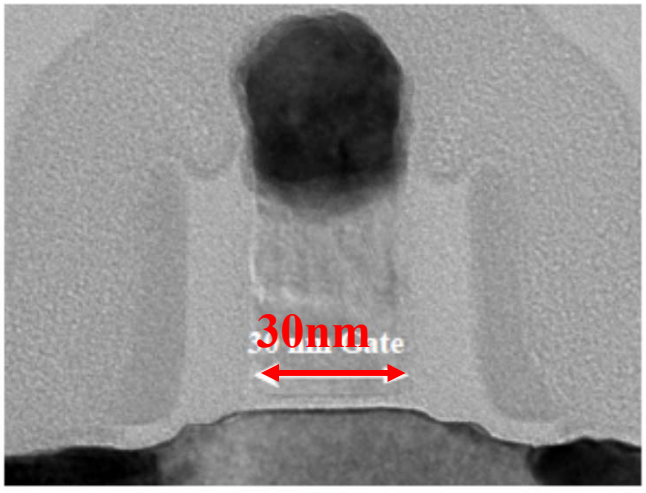
⇨ **Higher density**

⇨ **Higher speed**

⇨ **Less power consumption**

CMOS scaling and technology nodes

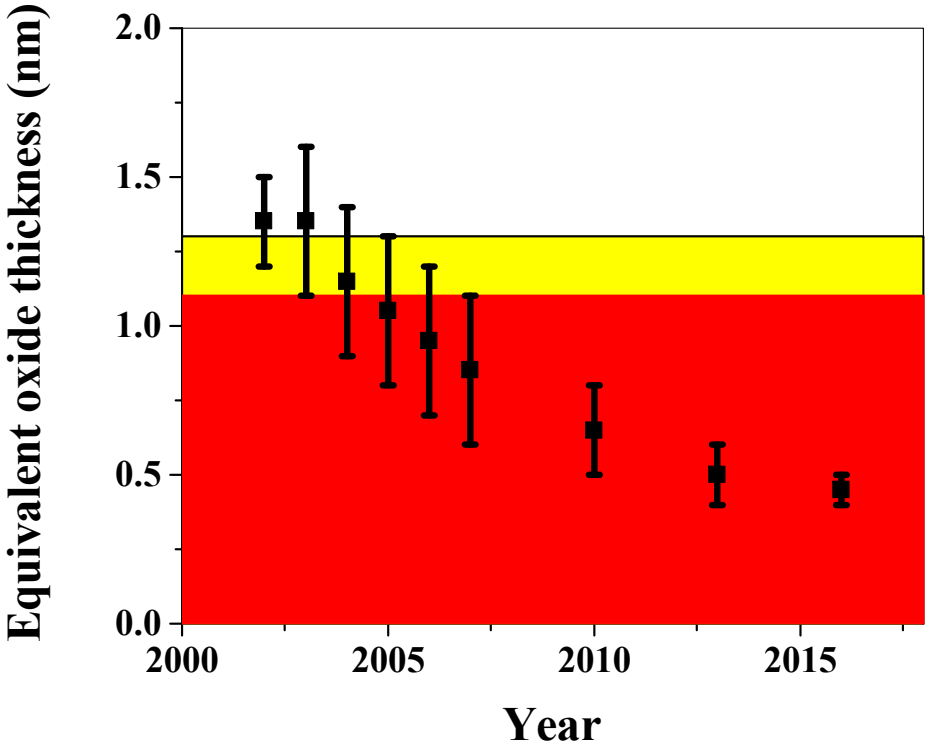
- Why scaling?
  - higher density/lower cost, higher performance, lower power.
- How?
  - Well, that is a long story



IBM "65 nm" technology

10 µm – 1971
6 µm – 1974
3 µm – 1977
1.5 µm – 1982
1 µm – 1985
800 nm – 1989
600 nm – 1994
350 nm – 1995
250 nm – 1997
180 nm – 1999
130 nm – 2001
90 nm – 2004
65 nm – 2006
45 nm – 2008
32 nm – 2010
22 nm – 2012
14 nm – 2014
10 nm – *2016-2017*
7 nm – *2017-2018*
5 nm – *2020-2021*

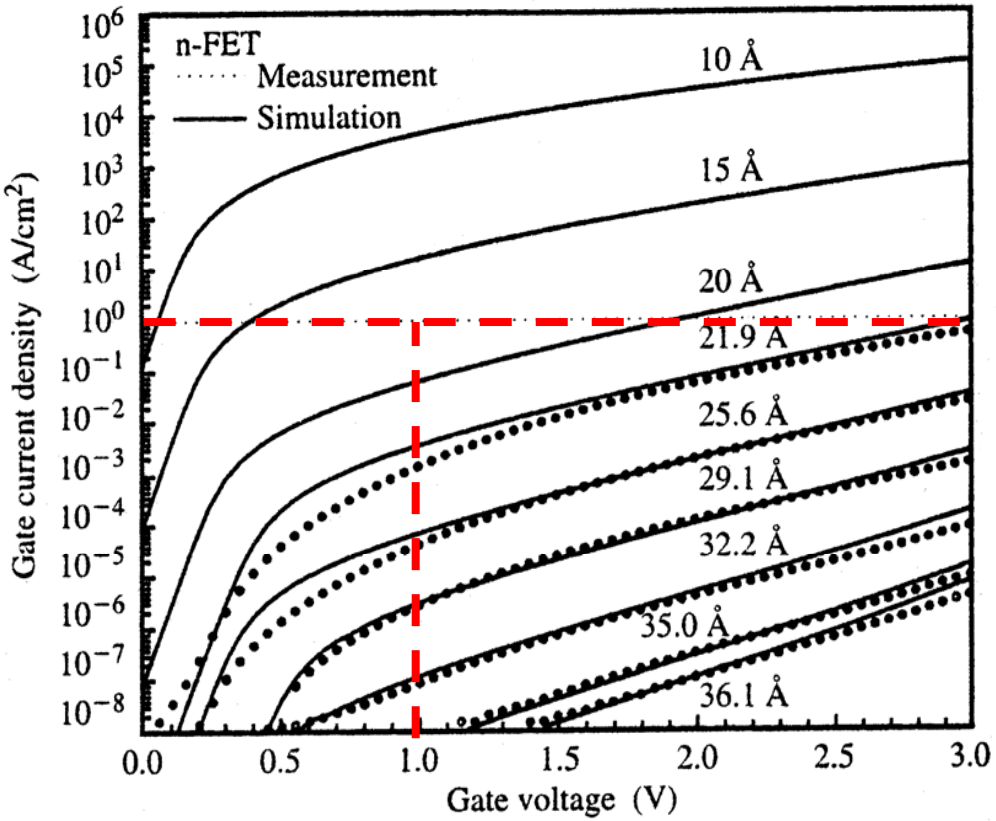
Scaling of gate dielectrics



- Gate dielectric scales down to maintain the gate control on the channel.
- 1.1nm oxide only contains ~3 monolayers of SiO_2 atoms
- Continued scaling of SiO_2 is facing severe challenges.

ITRS 2002, for high performance logic technology

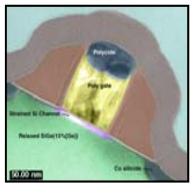
Limitation for silicon oxide scaling



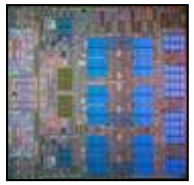
- For 1A/cm^2 @1V requirement, the ultimate scaling limit of SiO_2 will be ~ 1.8nm.

More “Moore”?

SOI



Strained Silicon

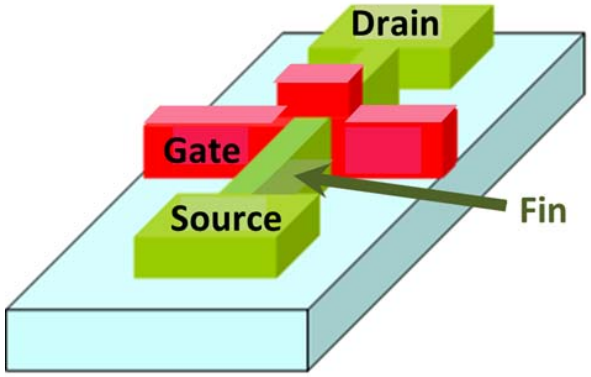


Dual Core

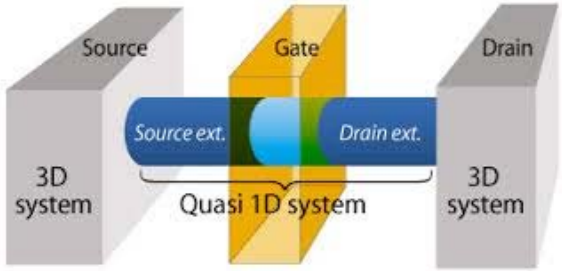
Immersion

High-k

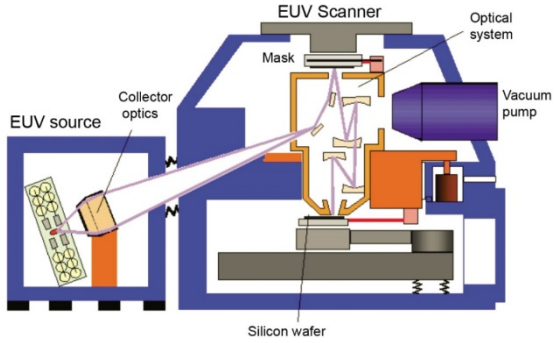
3D Chip Stacking



FinFET



Silicon nanowire



EUV

Scaling limit

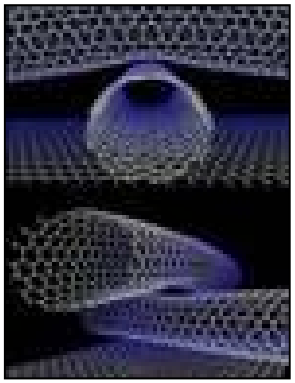
Approaching a "Red Brick Wall"

Challenges/Opportunities for Semiconductor R&D

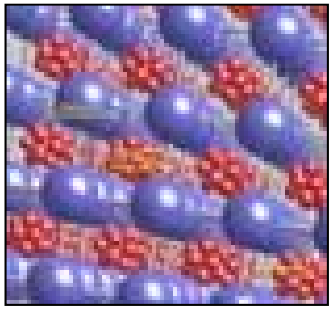
Year of Production:	1999	2002	2005	2008	2011	2014
DRAM Half-Pitch [nm]:	180	130	100	70	50	35
Overlay Accuracy [nm]:	65	45	35	25	20	15
MPU Gate Length [nm]:	140	85-90	65	45	30-32	20-22
CD Control [nm]:	14	9	6	4	3	2
T_{ox} (equivalent) [nm]:	1.9-2.5	1.5-1.9	1.0-1.5	0.8-1.2	0.6-0.8	0.5-0.6
Junction Depth [nm]:	42-70	25-43	20-33	16-26	11-19	8-13
Metal Cladding [nm]:	17	13	10	0	0	0
Inter-Metal Dielectric K:	3.5-4.0	2.7-3.5	1.6-2.2	1.5	<1.5	<1.5

*2001 ITRS roadmap

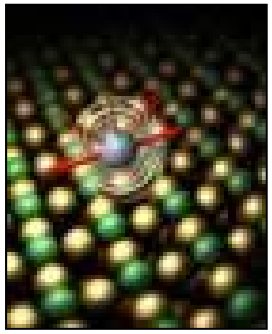
Beyond “Moore”



Carbon Nanotube Transistors

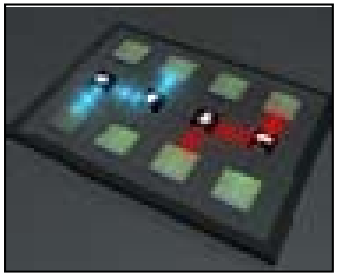


Self Assembly

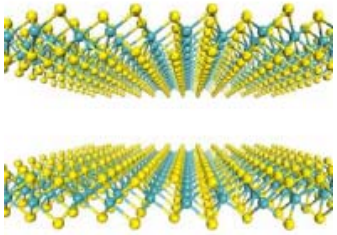


Atomic Storage

spintronics

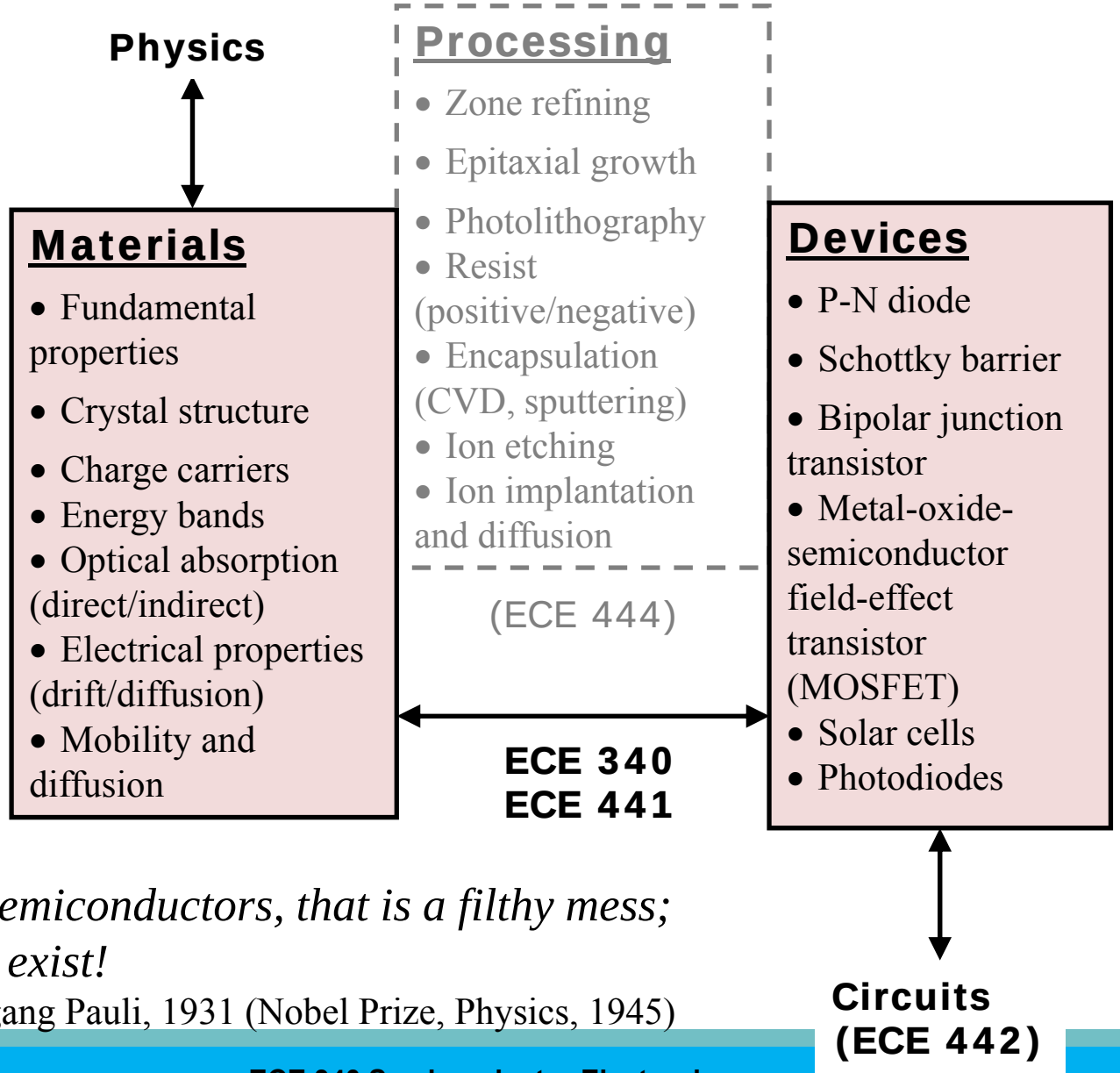


Nanophotonic Switch



2D materials

- What do we learn in ECE 340? (and later in ECE 441)



One shouldn't work on semiconductors, that is a filthy mess; who knows if they really exist!

Wolfgang Pauli, 1931 (Nobel Prize, Physics, 1945)

- Let's have a journey together in "Semiconductor Devices".
- Buckle up! It is going to be a rough ride.

Thank you!

LINKS

- INTRO VIDEO:

http://www.youtube.com/watch?v=cdqiP0aR1-Q