ECE 340 # Homework Assignment #10 **Fall 2015**

DUE: FRIDAY,NOVEMBER 20, 2015

Print your **name** and **NetID** legibly. Follow the guidelines and format given in the syllabus. Staple multiple pages. Show all units. Homework must be turned in at the **beginning** of class and any late homework assignments will not be accepted. Please contact the course director, Professor Dallesasse, should any issues with late homework arise.

1. MOS CAPACITORS

(A). Consider an ideal (ignore work function difference) Si MOS capacitor with acceptor doping of $N_a = 2 \times 10^{16}$ cm^{-3} and an oxide thickness of 200 nm. Find the threshold voltage of this device. Note that $q\chi_{Si} = 4.05$ eV.

(B). Given that the device has a copper gate metal ($\Phi_m = 4.6$ V), find the threshold of this device.

(C). Find the maximum depletion width of this device as well as the minimum capacitance.

(D). Sketch the low frequency C vs. V_G curve for this device being sure to note the flatband voltage, the threshold voltage, and the minimum capacitance.

(E). Repeat parts (b)-(d) for an MOS with donor doping of 1×10^{16} cm^{-3} and the same gate metal.

2. MOSFET OUTPUT CHARACTERISTICS

An n-channel MOSFET is designed with a silicon dioxide thickness of 12 nm. Assuming the channel mobility is $\mu_n = 1000$ cm^{2}V^{-1}s^{-1}, the channel length is 15 μm, the channel width is 150 μm, and the acceptor concentration is $N_a = 4 \times 10^{16}$ cm^{-3}, find the threshold voltage of the device. It is feasible to assume the gate work function is negligible. Create a plot of the drain current versus drain voltage for various gate voltages (at least 4) above threshold. [NOTE: Please use plotting software and do not simply sketch the plots.]

3. MOSFET CHARACTERISTICS CONT'D

Consider an n-MOSFET with a metal gate and an Al_2O_3 gate insulator (assume $k = \varepsilon_{in}/\varepsilon_0 \approx 10$) of thickness d = 5 nm. The threshold voltage of this device is found to be V_T = 0.3 V and the flat band voltage is 0 V. A schematic of this device is shown in Fig. 3.1.

(A). First, assuming that the source and drain terminals are both grounded and a voltage is applied only to the gate, draw the low frequency $C - V_{GS}$ curve of the device. Be sure to label key values and regions of operation and also calculate and label the maximum capacitance C_{max}.

(B). Now sketch the high frequency curve for this device. Is it similar or different from the low frequency curve in part (a)? Why or why not?

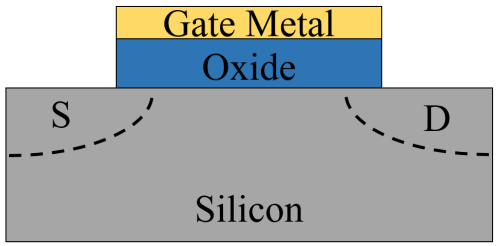

Figure 3.1: MOSFET Schematic

(C). A voltage is now applied to the source and drain. The measured $I-V$ characteristics are shown in Fig. 3.2 for two gate voltages. Assuming the device parameters given in this problem, find the second applied voltage V_{GS2}.

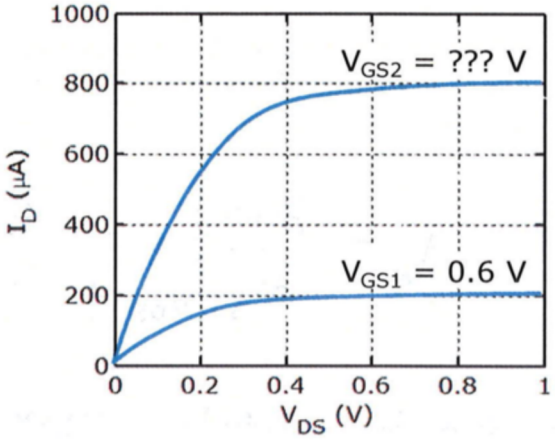

Figure 3.2: MOSFET I_D vs. V_{DS} Characteristic

(D). Sketch the I_D vs. V_{GS} curve of the same device when $V_{DS} = 0.4$ V. Be sure to indicate numerically the voltage transition points between the off-state, saturation, and the linear regime.

(E). Consider the bias point where $V_{GS} = V_{DS} = 1.3$ V. Find the transductance g_m if $Z/L = 15$ and the mobility is $\mu = 500$ cm^{2}V^{-1}s^{-1}.

4. Integrated Circuits

(A). Figure 9-24 in the text depicts a logic inverter using an n-MOSFET. Paying particular attention to the differences in operation, draw a diagram for a similar inverter using a p-MOSFET. Given that these designs only require one MOSFET to function, why are CMOS designs favored for integrated circuits?

(B). Refer to the CMOS inverter depicted in Figure 9-25. Assumer that the two MOSFETs have the same insulator capacitances. Derive the expression for the input voltage at the transition region (V_m), where both transistors are saturated. From your result, find the condition for this voltage to occur at $V_{in} = V_{DD}/2$. Comment on the design issues that this may cause.