ECE 340: Semiconductor Electronics

Chapter 6: Field-effect transistors

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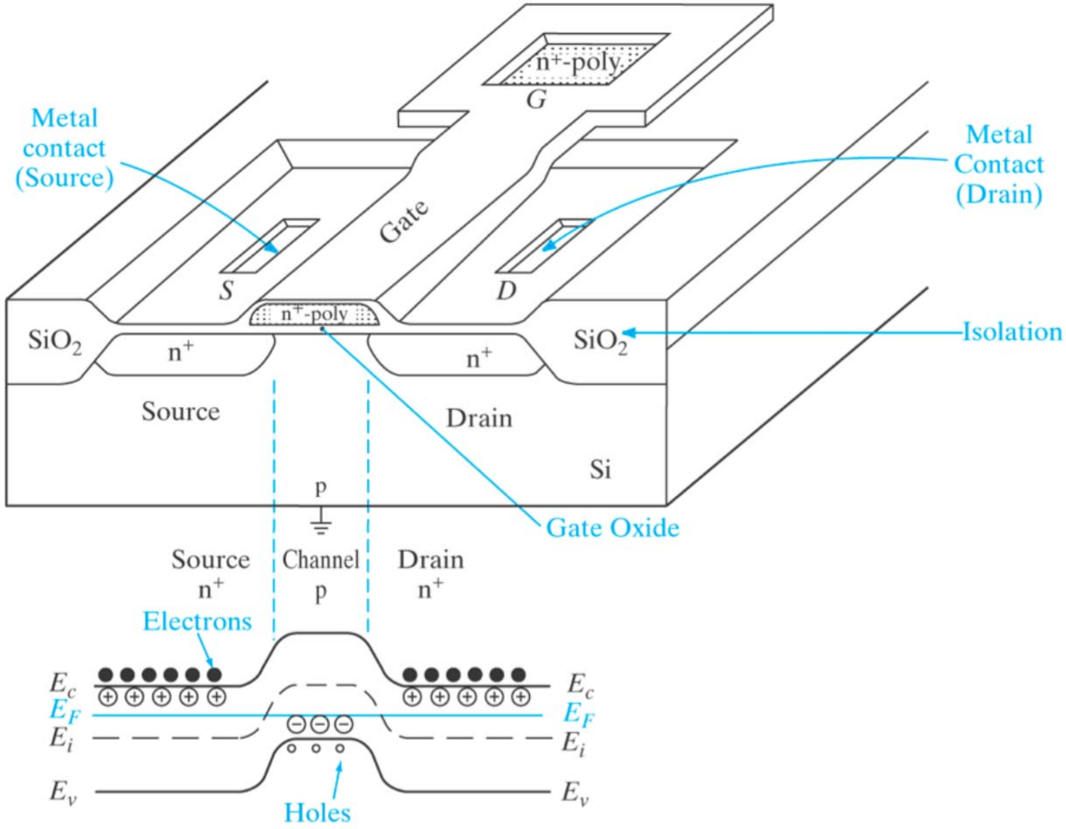
Outline

- Metal-insulator-semiconductor FET
  - Basic operation and fabrication
  - Ideal MOS capacitor
  - Effects of real surfaces
  - Threshold voltage
  - The MOS field-effect transistor
  - Substrate bias effect

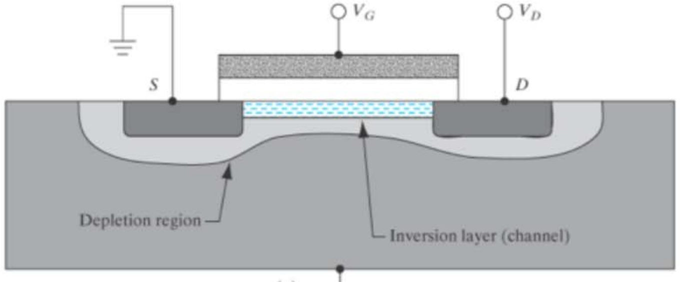
MOSFET structure and band diagram



- Channel current is controlled by a voltage applied at a gate electrode
- A positive voltage applied to the gate induces positive charge in the metal of the gate
- In the semiconductor, negative charges are induced in response to the positive charge on the gate
- The induced electrons are mobile and form a conductive channel
- Threshold Voltage V_T: voltage required to induce a conductive channel ("normally off" device)

MOSFET at various operating conditions

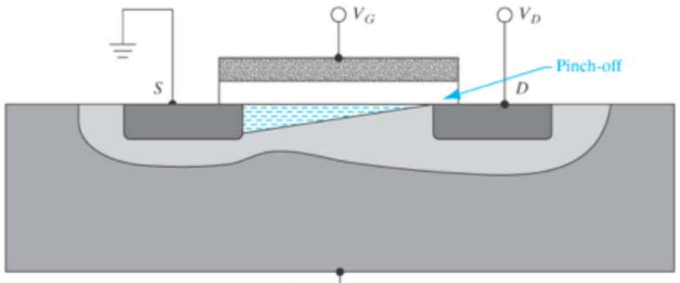
Linear region



(a)

- At small drain bias V_D, channel is a gate controlled resistor

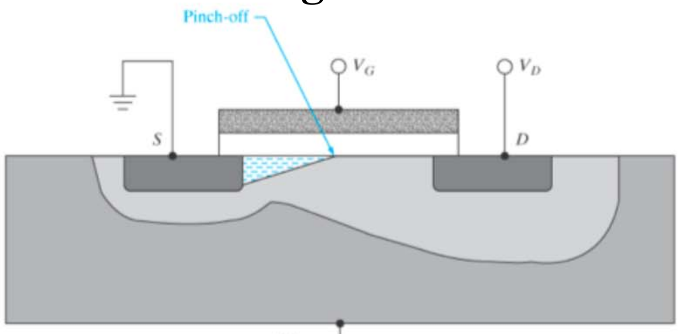
Onset of saturation at pinch-off



(b)

- When $V_D = V_G - V_{T,}$ the channel is pinched off

Strong saturation

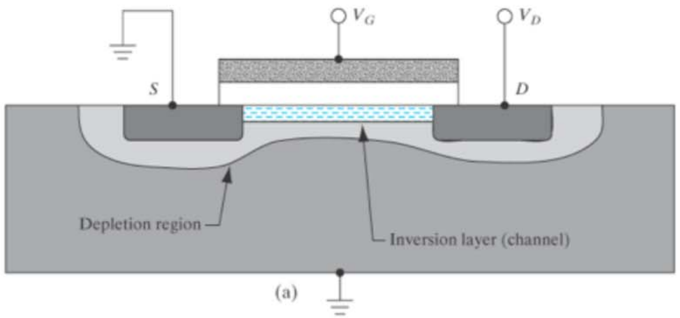


(c)

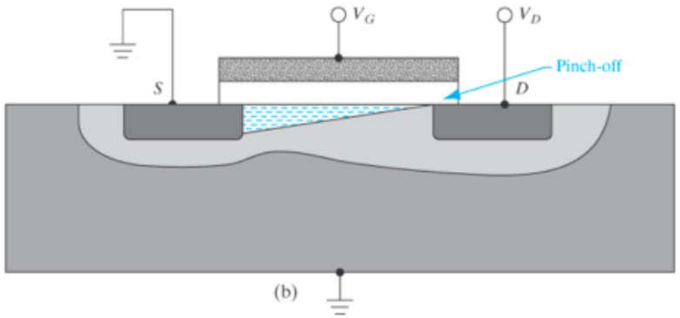
- When $V_D > V_G - V_{T,}$ the pinch off point move more into the channel

MOSFET at various operating conditions

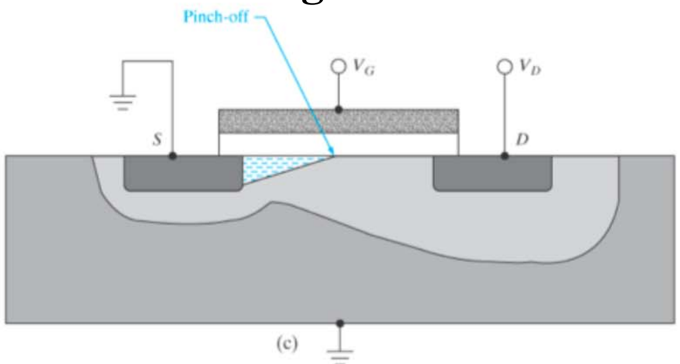
Linear region

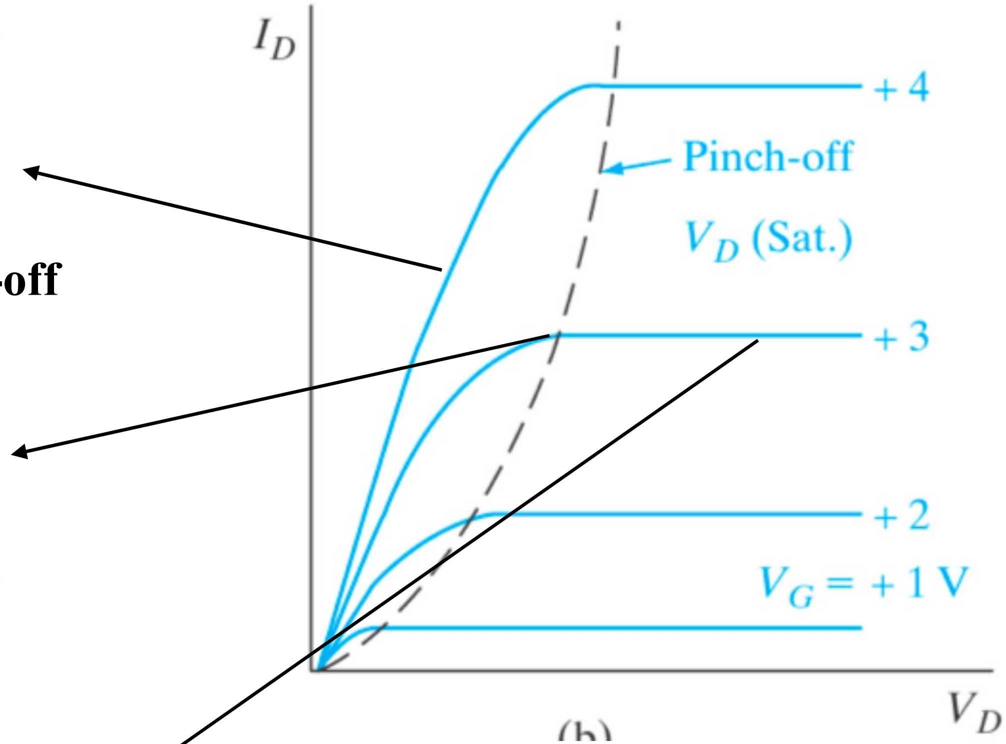


Onset of saturation at pinch-off



Strong saturation





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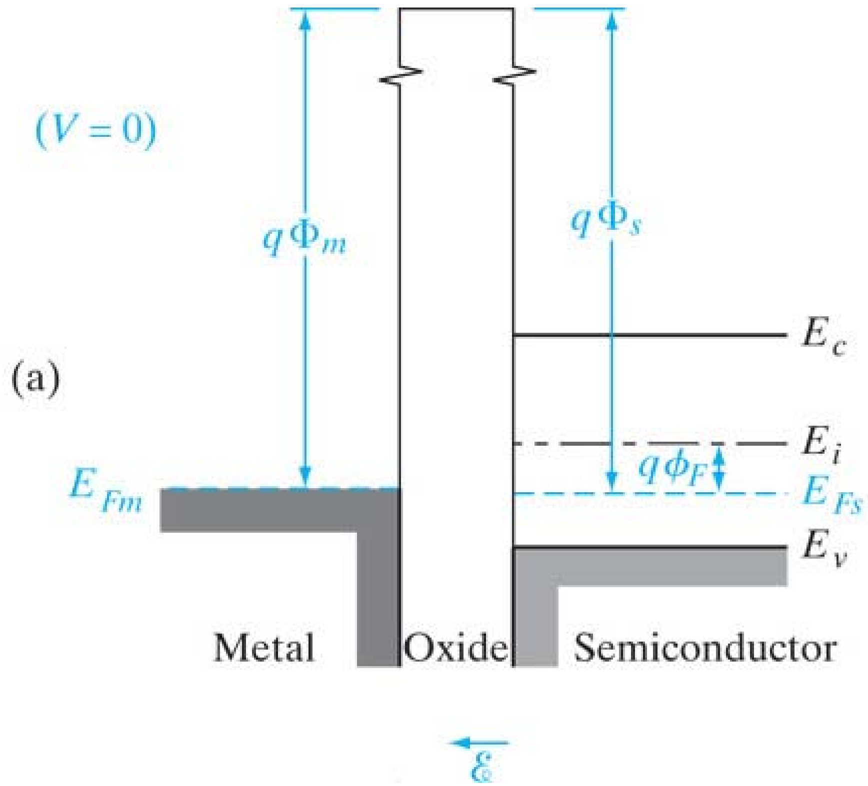
Ideal MOS capacitor at equilibrium

"Ideal": $\phi_m = \phi_s$ and no other defect or trap charges



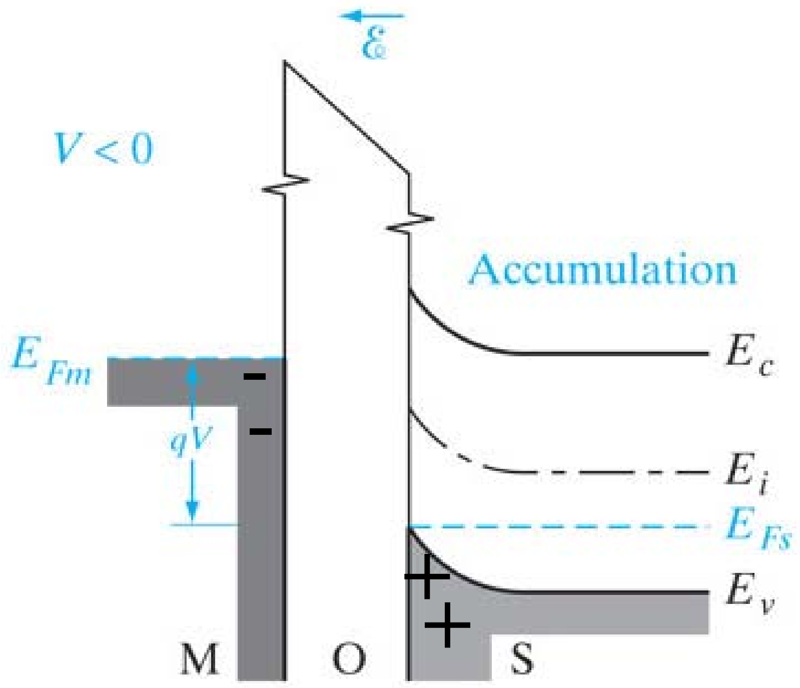
No gate bias;
No band bending.

$$\phi_F = (E_i - E_F)/q$$

- At equilibrium, Fermi level line up, no band bending

Ideal MOS structure at accumulation

Positive voltage on p-substrate (similar to forward bias in pn junction)

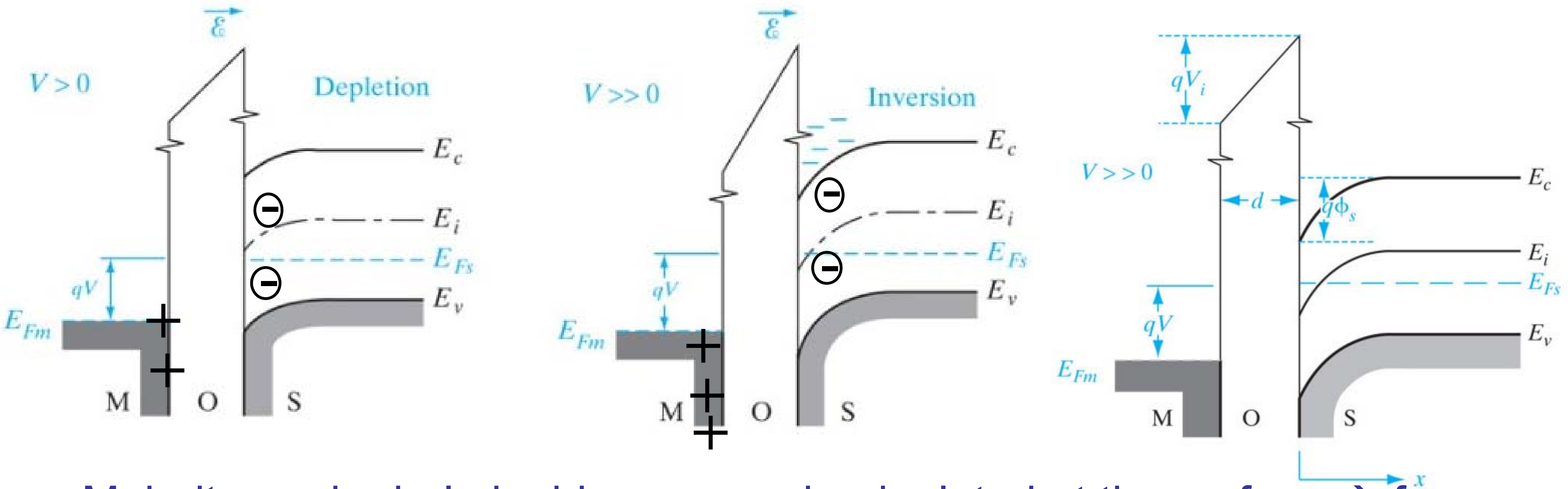


- Majority carrier hole accumulated at the surface

Ideal MOS structure at depletion and inversion

Negative voltage on p-substrate (similar to reverse bias in pn junction)

Depletion **Inversion** **Strong inversion**



- Majority carrier hole is driven away, i.e depleted at the surface → form depletion region
- Minority carrier is attracted to the surface:

When $n \geq n_i$ ($\phi_s = \phi_F$): inversion

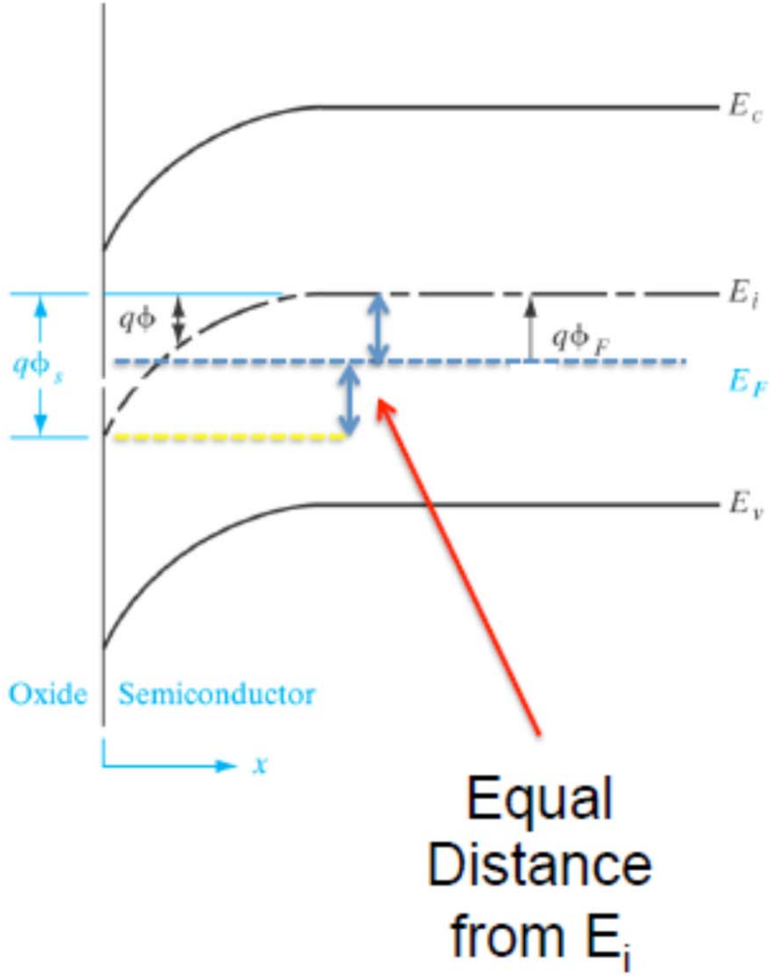
When $n \geq p_o$ ($\phi_s = 2\phi_F$): strong inversion

MOS channel: strong inversion

- In the case where Φ_s has moved past the intrinsic level by an amount Φ_F the material is as n-type as it was p-type and is in "strong inversion"

Strong Inversion:

$$\phi_s(inv.) = 2\phi_F = 2\frac{kT}{q}\ln\frac{N_a}{n_i}$$



Carrier Concentration

- **For electrons:**

At neutral region:

$$n_0 = n_i e^{(E_F - E_i)/kT} = n_i e^{-q\Phi_F/kT}$$

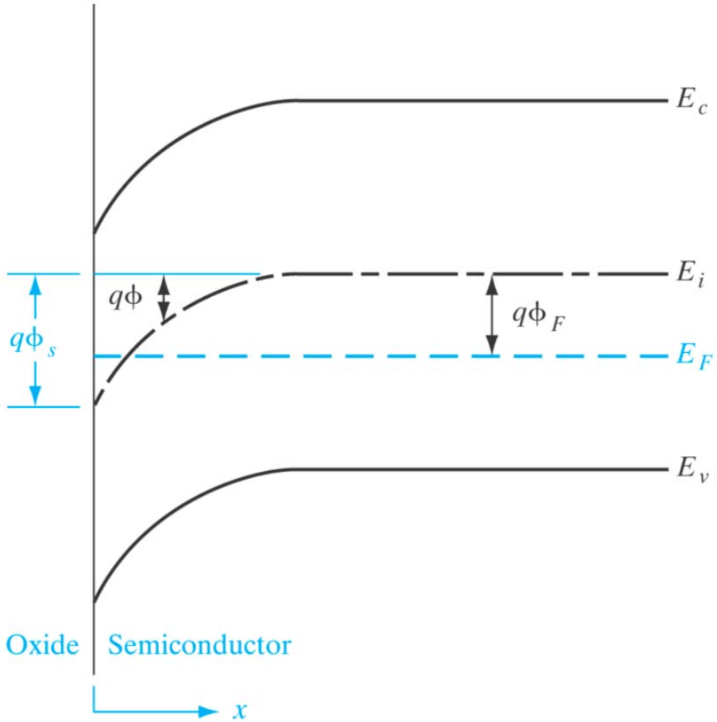
At any position x:

$$n = n_i e^{-q(\Phi_F - \Phi)/kT} = n_0 e^{q\Phi/kT}$$

- **For holes:**

$$p_0 = n_i e^{q\Phi_F/kT}$$

$$p = p_0 e^{q\Phi/kT}$$



Solving for electric field and band bending

- Poisson's equation:

$$\frac{\partial^2 \boldsymbol{\phi}}{dx^2} = \frac{d\mathcal{E}(x)}{dx} = \frac{q}{\epsilon_s}(p - n + N_d^+ - N_a^-)$$

- Electric field:

$$\mathcal{E} = \frac{\sqrt{2}kT}{qL_D}\left[\left(e^{-q\boldsymbol{\phi}/kT} + \frac{q\boldsymbol{\phi}}{kT} - 1\right) + \frac{n_0}{p_o}\left(e^{q\boldsymbol{\phi}/kT} - \frac{q\boldsymbol{\phi}}{kT} - 1\right)\right]^{1/2}$$

- Surface electric field (x=0, $\boldsymbol{\phi} = \boldsymbol{\phi_s}$):

$$\mathcal{E}_s = \frac{\sqrt{2}kT}{qL_D}\left[\left(e^{-q\boldsymbol{\phi_s}/kT} + \frac{q\boldsymbol{\phi_s}}{kT} - 1\right) + \frac{n_0}{p_o}\left(e^{q\boldsymbol{\phi_s}/kT} - \frac{q\boldsymbol{\phi_s}}{kT} - 1\right)\right]^{1/2}$$

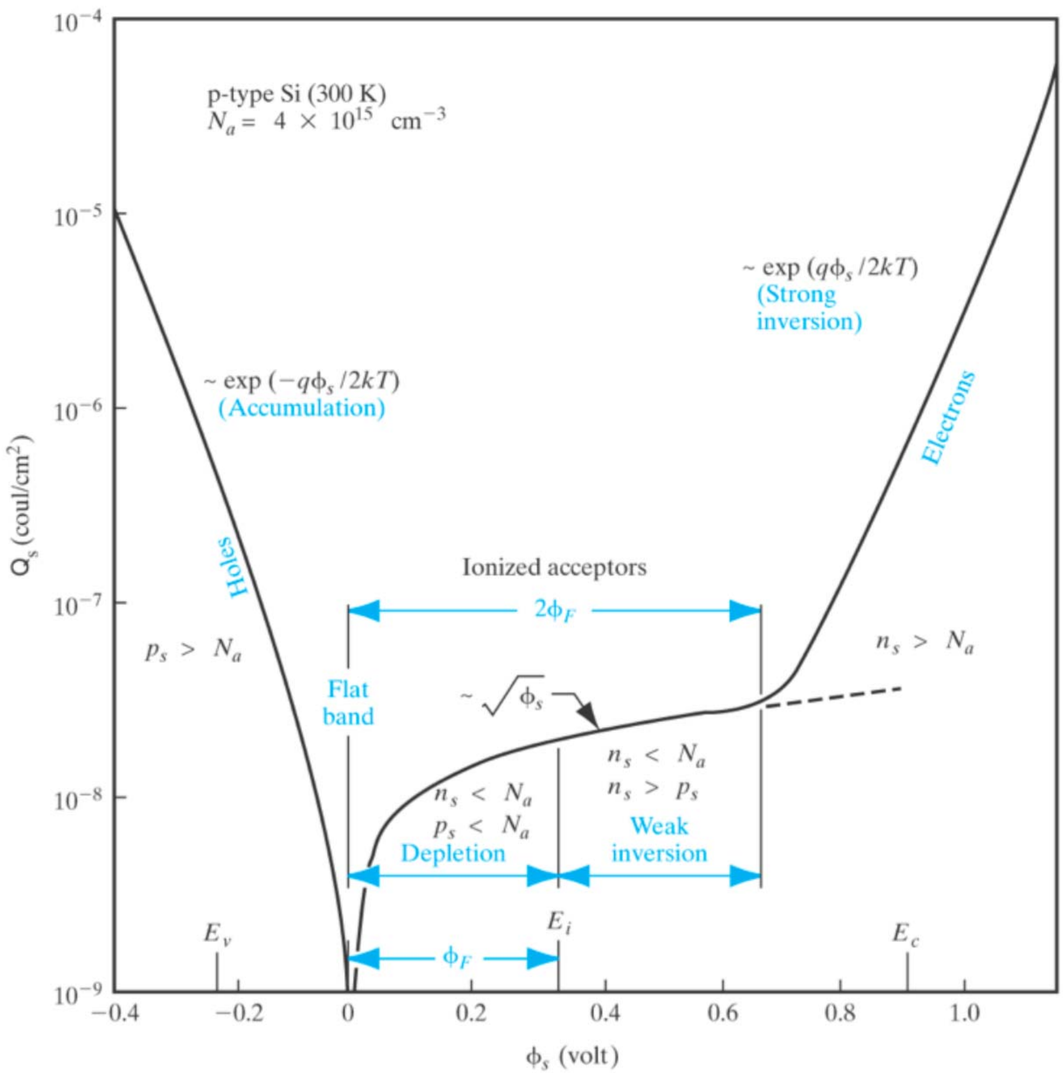
Where $L_D = \sqrt{\frac{\epsilon_s kT}{q^2 p_o}}$ Debye screening length

Space-charge density vs surface potential

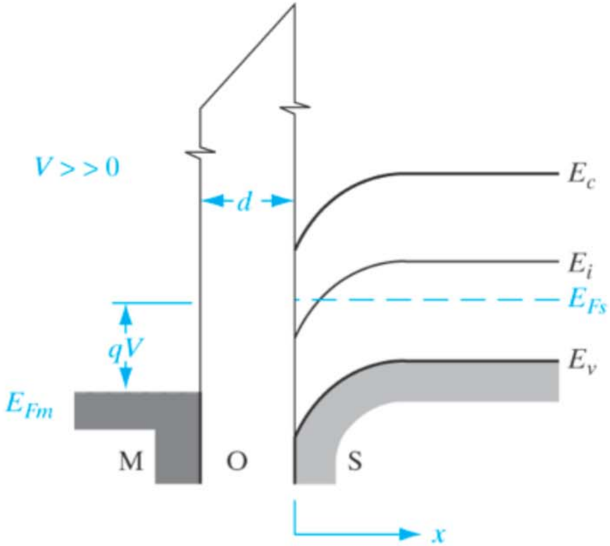
- Space charge density

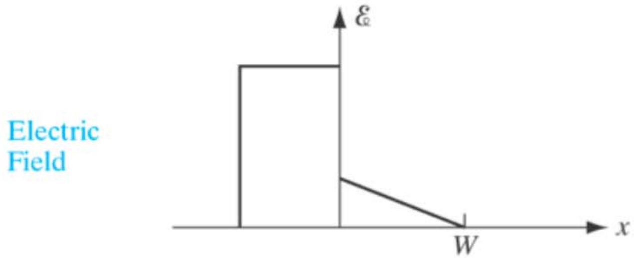
$$Q_s = -\epsilon_s \mathcal{E}_s$$

- When the surface potential is zero, the net space charge is zero
- When the surface potential is negative, majority carriers (holes) are attracted to the surface forming an accumulation layer
- When the surface potential is positive, initially a depletion region forms (space charge), and then an inversion layer with mobile electrons

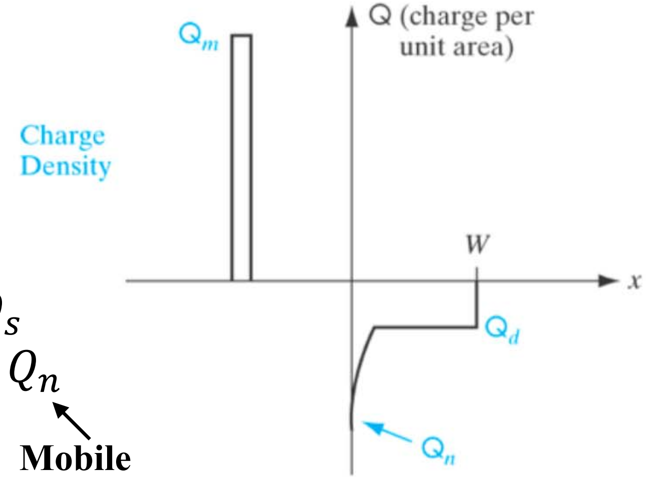


Charge density, field and potential at inversion





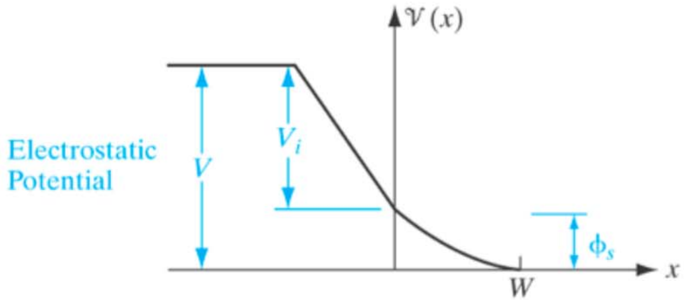
$$\mathcal{E}_{ox} = \frac{\epsilon_s}{\epsilon_{ox}} \mathcal{E}_s$$



$$Q_m = -Q_s$$
$$= qN_d W - Q_n$$

Depletion charge

Mobile inversion region charge



$$V = V_i + \boldsymbol{\phi_s}$$

$$\boldsymbol{V_i = \frac{-Q_s d}{\epsilon_i} = \frac{-Q_s}{C_i}}$$

Depletion width and depletion capacitance

MOS capacitor

$$\boldsymbol{W}=\left[\frac{2\epsilon_s\phi_s}{qN_a}\right]^{1/2}$$

n+--p junction

$$\boldsymbol{W}=\left[\frac{2\epsilon_s(V_0-V_a)}{qN_a}\right]^{1/2}$$

depletion capacitance $$\boldsymbol{C_d}=\frac{\boldsymbol{\epsilon_s}}{\boldsymbol{W}}$$

depletion charge $$Q_d=-qN_aW$$

Threshold voltage

- **Unlike pn junction, minority carrier can pile up at the surface, since insulator block its way to diffuse to metal.**
- **When $n \geq p_o$ ($\phi_s = 2\phi_F$, strong inversion, $n \geq N_a$), further increase in voltage result in stronger inversion rather than more depletion.**
- Maximum depletion width:

$$\Rightarrow \quad \boxed{W_m = \left[\frac{4\epsilon_s \phi_F}{qN_a}\right]^{1/2}}$$

- The maximum depletion charge:

$$Q_{d\_m} = -qN_a W_m$$

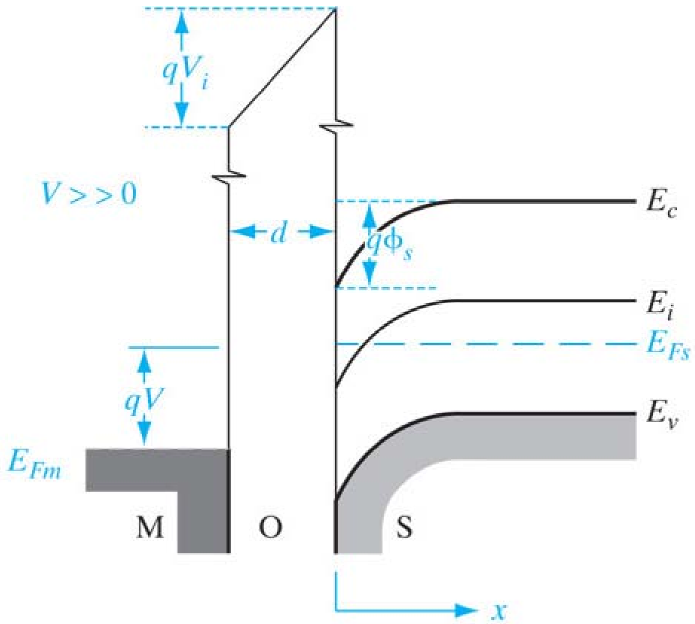
- Threshold voltage:

$$\boxed{V_T = -\frac{Q_{d\_m}}{C_i} + 2\phi_F}$$

Ideal case

Voltage drop on insulator

Voltage drop on semiconductor



MOS capacitance

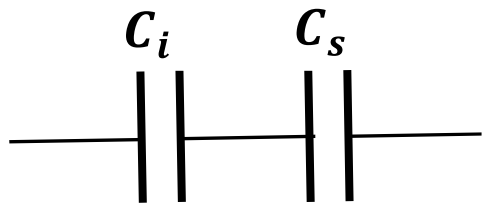
- Total MOS capacitance:

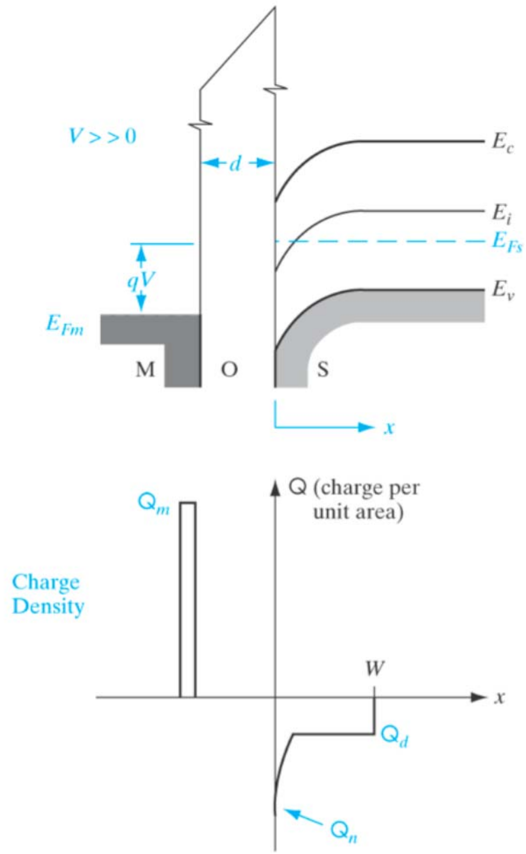
$$\frac{1}{C} = \frac{1}{C_i} + \frac{1}{C_s}$$

Insulator capacitance

Semiconductor capacitance

$$C_i = \frac{\epsilon_i}{d} \qquad C_s = \frac{dQ_s}{d\phi_s}$$



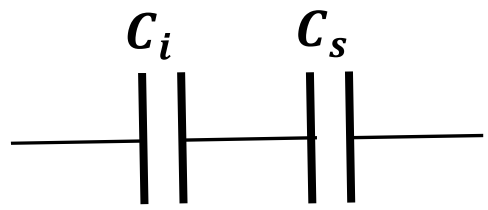


Insulator capacitance

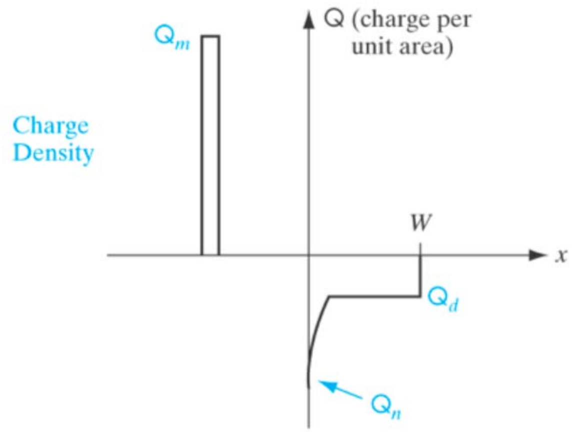
$$C_i = \frac{\epsilon_i}{d}$$

Permittivity of the insulator

Oxide thickness

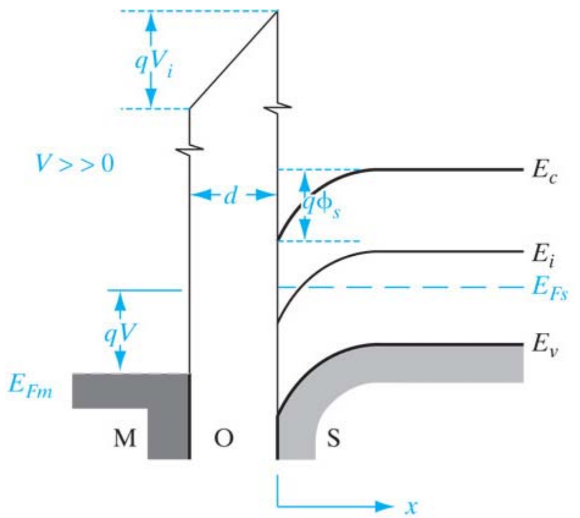


The relative permittivity (ϵ_r or k): is dielectric permittivity expressed as a ratio relative to the permittivity of vacuum



$$\epsilon_r = \frac{\epsilon_i}{\epsilon_0}$$

vacuum permittivity $\epsilon_0 = 8.85 \times 10^{-12}$ F/m



SiO_2 relative permittivity: 3.9

High-k dielectric: insulators with relative permittivity higher than SiO_2 (3.9)

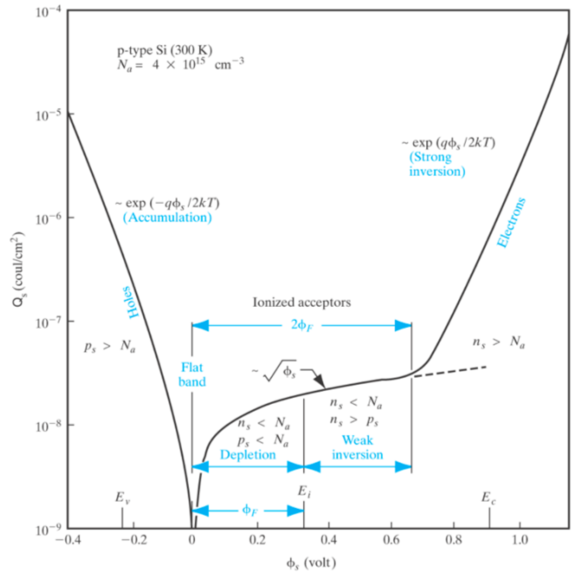
Semiconductor capacitance at accumulation

- Semiconductor capacitance is very high due to the steep slope of $\boldsymbol{Q_s}$ vs $\boldsymbol{\phi_s}$ plot:

$$\boldsymbol{C_s = \frac{dQ_s}{d\phi_s} = \frac{dQ_p}{d\phi_s}}$$

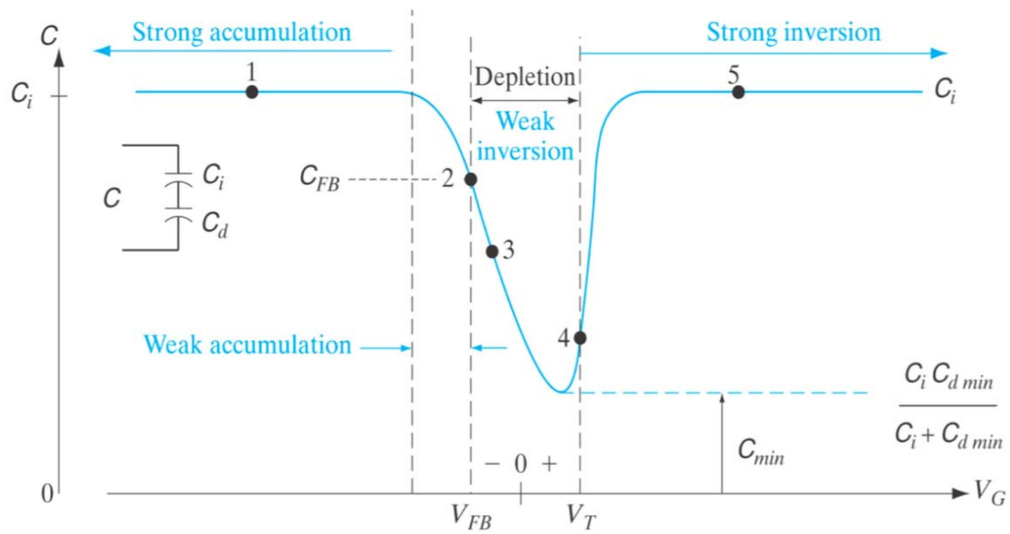
$$\boldsymbol{Q_p} = \frac{\sqrt{2}kT\boldsymbol{\epsilon_s}}{qL_D}\left(e^{-q\boldsymbol{\phi_s}/kT}\right)^{1/2}$$

$\boldsymbol{C_s}$ is very large, >> $\boldsymbol{C_i}$



- Total capacitance:

$$\boldsymbol{C \approx C_i}$$



Semiconductor capacitance at depletion

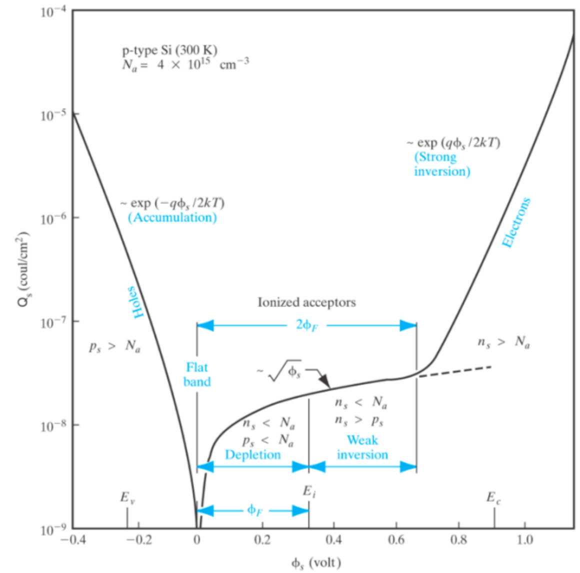
- Depletion capacitance:

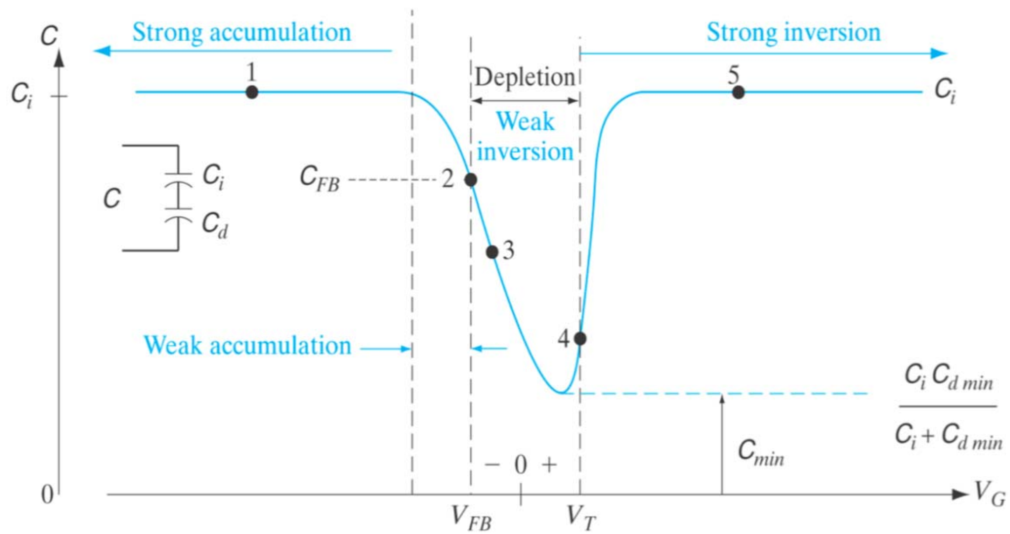
$$C_d = \frac{\epsilon_s}{W}$$

$$W \uparrow \rightarrow C_d \downarrow$$

- Total capacitance:

$$C = \frac{1}{\frac{1}{C_i} + \frac{1}{C_d}} = \frac{C_i C_d}{C_i + C_d}$$





Semiconductor capacitance at inversion

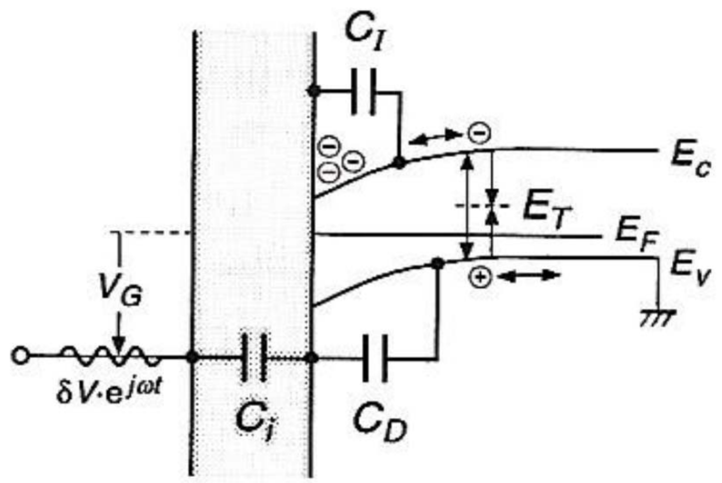
- Depletion capacitance reach maximum

$$\boldsymbol{C_d = \frac{\epsilon_s}{W_m}}$$

- Inversion carrier capacitance is very large:

$$\boldsymbol{C_I = \frac{dQ_n}{d\phi_s}}$$

$$\boldsymbol{Q_n} \approx \frac{\sqrt{2}kT\epsilon_s}{qL_D}\left(e^{q\phi_s/kT}\right)^{1/2}$$



Semiconductor capacitance at inversion

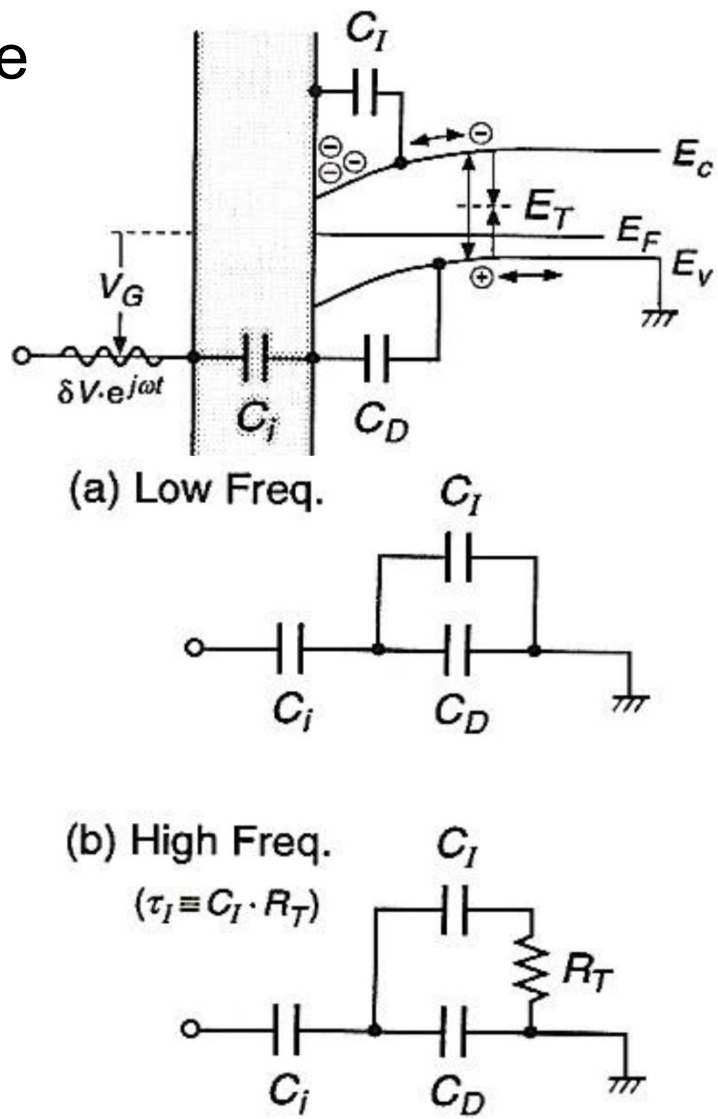
- At low frequency, total capacitance is

$$C = \frac{1}{\frac{1}{C_i} + \frac{1}{C_d + C_I}} \approx C_i$$

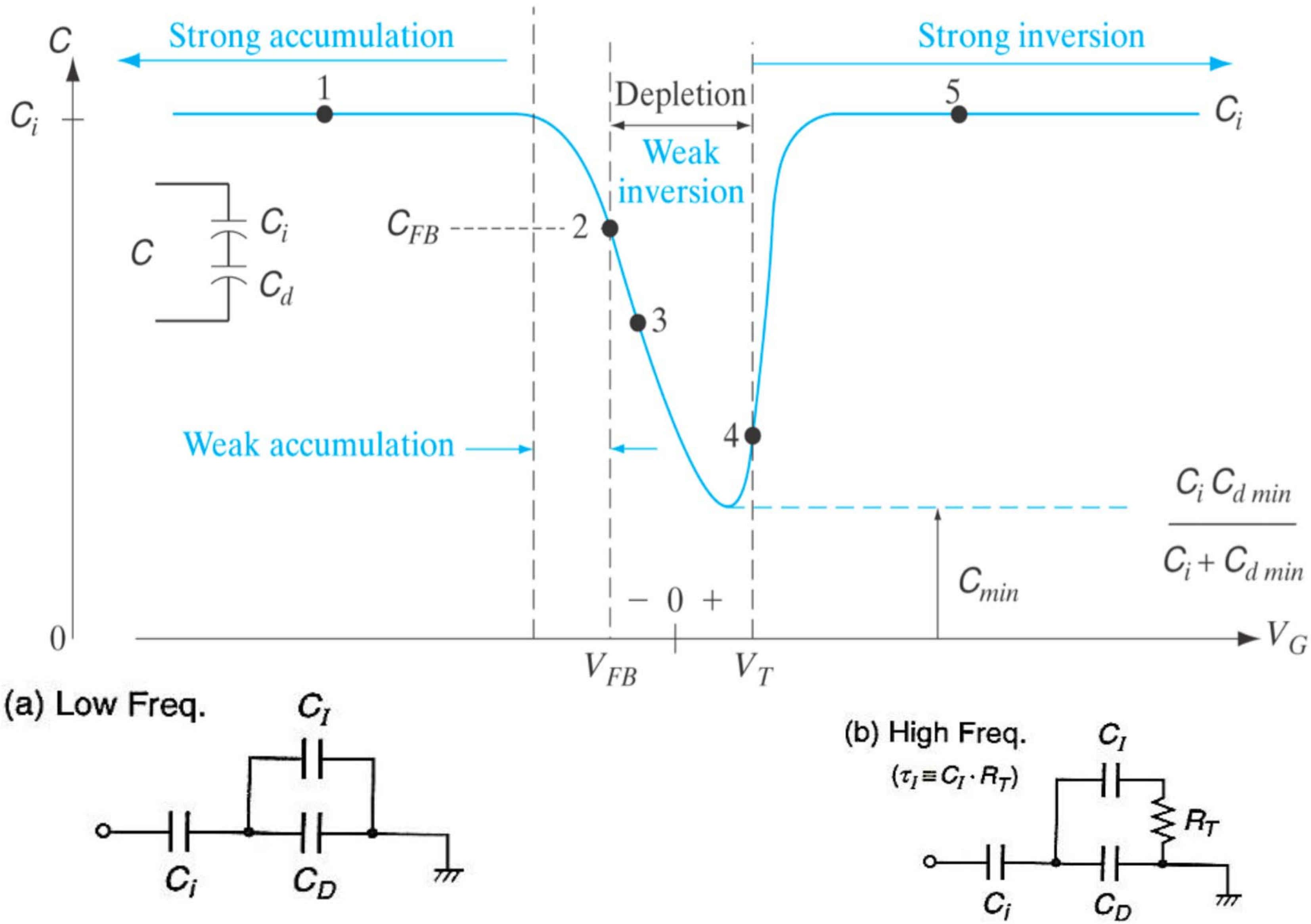
C_I is very large

- High frequency, minority carrier can not follow ac signal, total capacitance is:

$$C = \frac{1}{\frac{1}{C_i} + \frac{1}{C_d}} = \frac{C_i C_d}{C_i + C_d}$$



MOS capacitance



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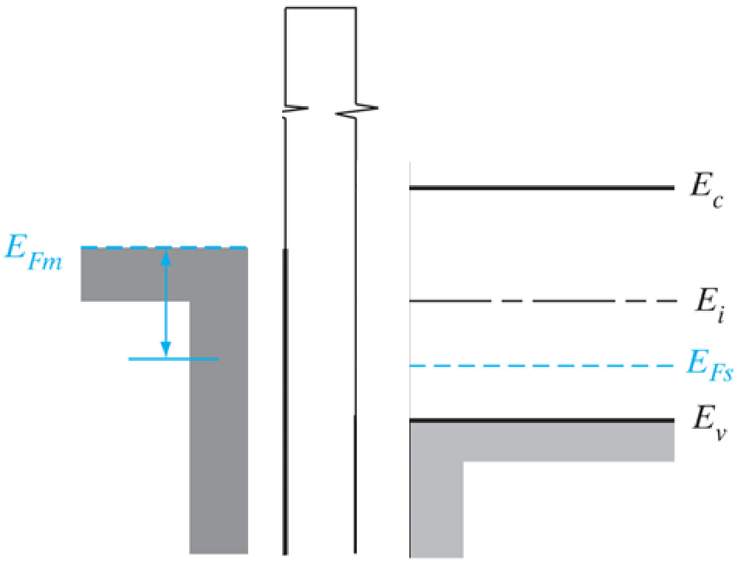
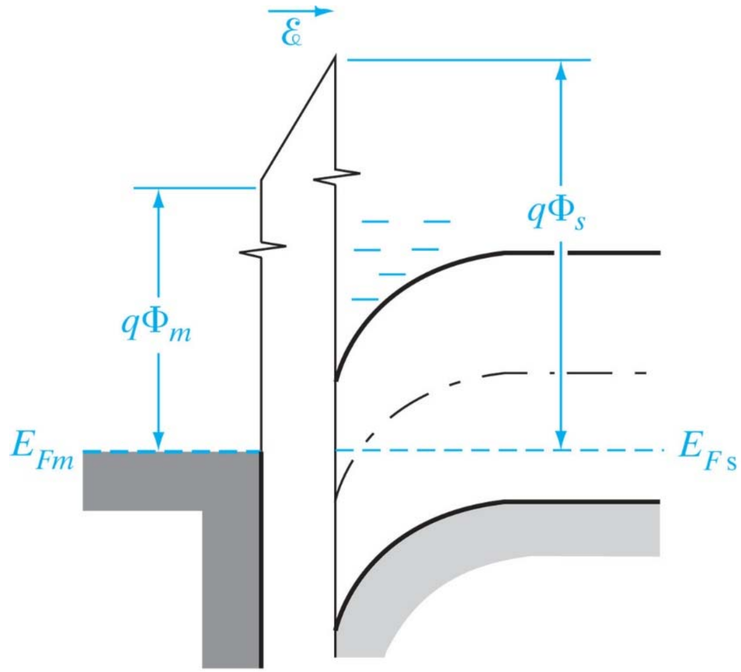
Non-ideal MOS capacitor $\phi_m \neq \phi_s$

Before contact



$\phi_m \neq \phi_s$

After contact, at equilibrium

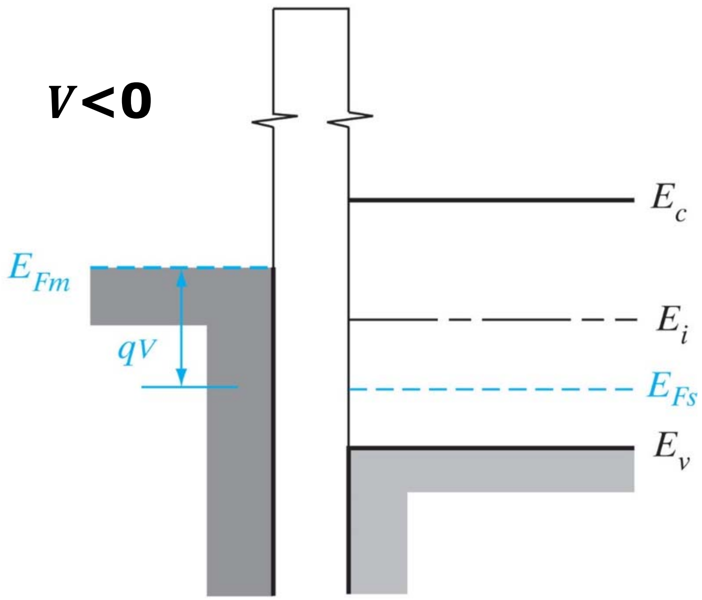


(a) Equilibrium
$V = 0$

- After contact, electron transfer from metal to semiconductor
- Fermi level alignment → band bending

Flat band voltage

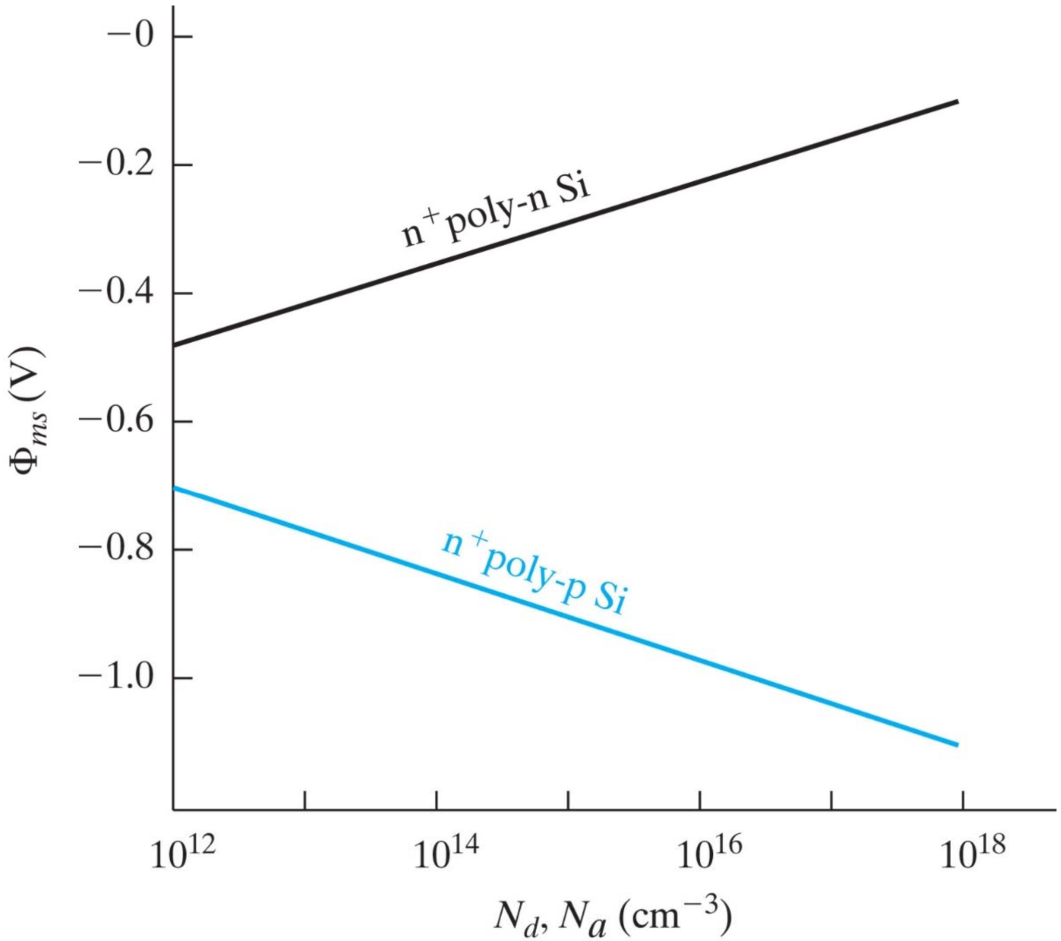
- Flat band voltage: the voltage to bring the MOS back to flat energy band (no bending)

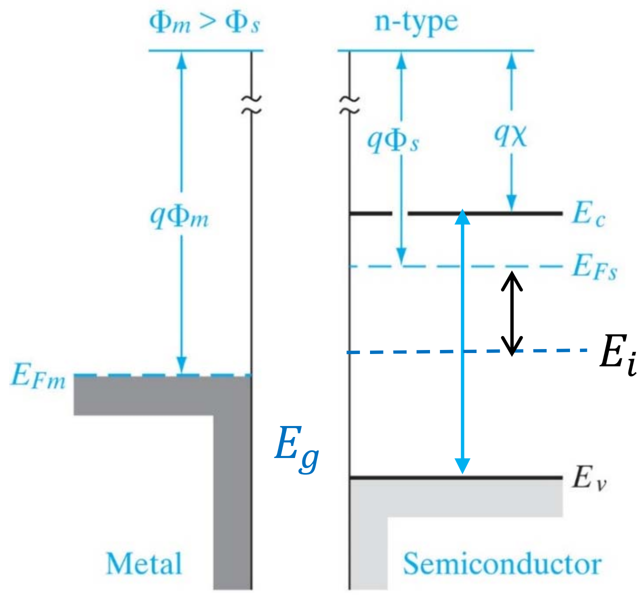


(b) Flat band
$V = V_{FB} = \Phi_{ms}$

$$V_{FB} = \phi_{ms} = \phi_m - \phi_s$$

Effect of doping on work function difference $\boldsymbol{\phi_{ms}}$





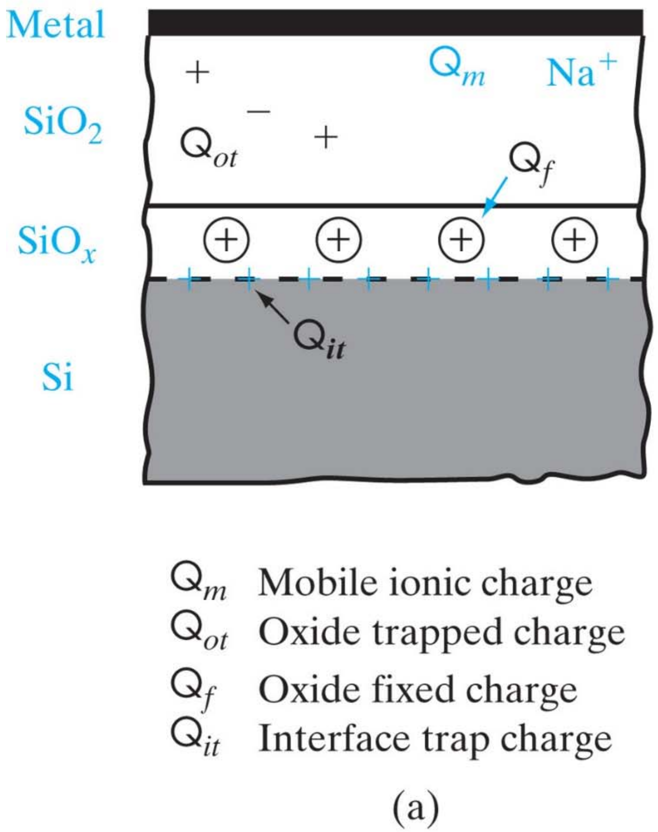
$$E_F - E_i = kT\,ln\left(\frac{N_d}{N_i}\right)$$

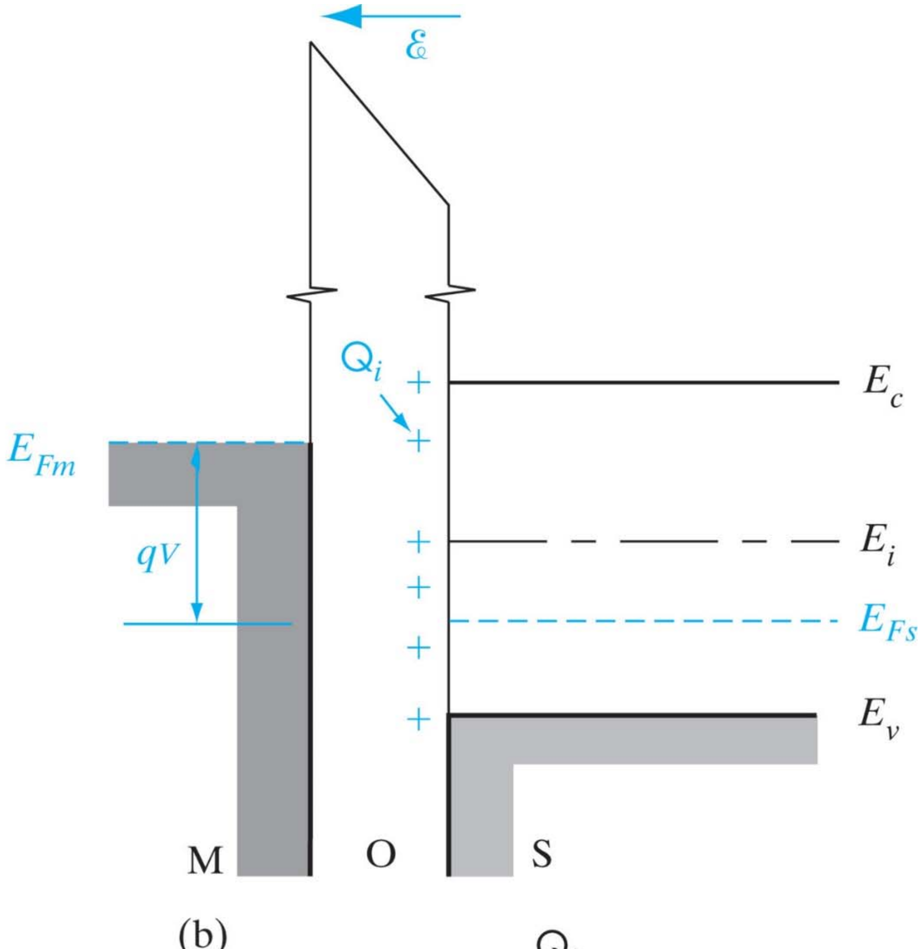
$$\Longrightarrow \quad \boldsymbol{\phi_s} = \chi + \frac{E_g}{2q} - \frac{kT}{q} ln\left(\frac{N_d}{N_i}\right)$$

$$\Longrightarrow \quad \boldsymbol{\phi_{ms}} = \boldsymbol{\phi_m} - \boldsymbol{\phi_s} = \boldsymbol{\phi_m} - \chi - \frac{E_g}{2q} + \frac{kT}{q} ln\left(\frac{N_d}{N_i}\right)$$

$$N_d \uparrow \rightarrow \boldsymbol{\phi_{ms}} \uparrow$$

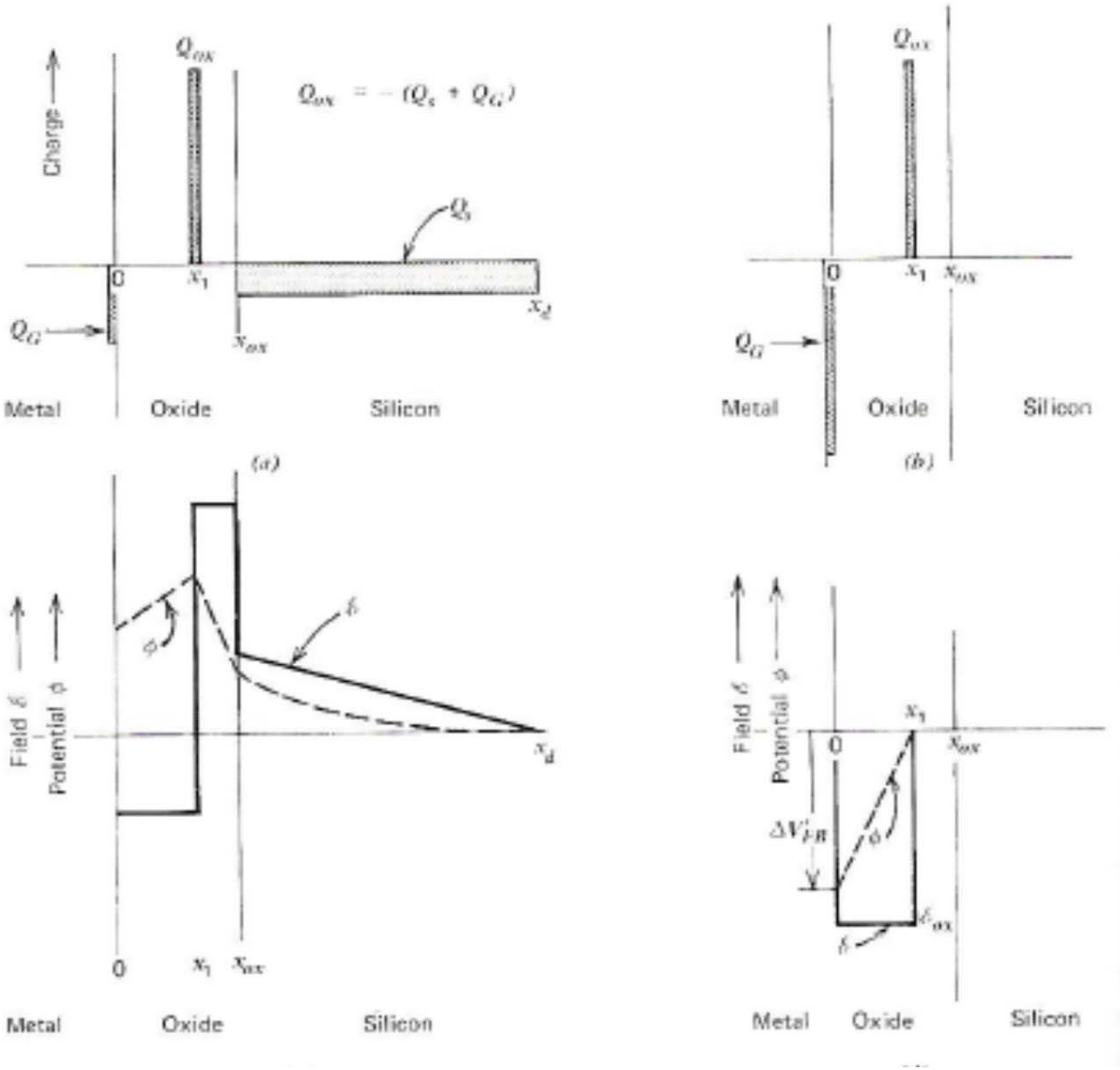
Effect of charges in the oxide on flatband voltage





$$V = V_{FB} = -\frac{Q_i}{C_i}$$

Effect of oxide charge on MOS system



$$\mathcal{E}_{ox} = -\frac{Q_{ox}}{\epsilon_{ox}} \qquad 0 < x < x_1$$

$$\Delta V_{FB} = x_1 \mathcal{E}_{ox} = -\frac{x_1 Q_{ox}}{\epsilon_{ox}}$$

$$\Delta V_{FB} = -\frac{x_1 Q_{ox}}{C_{ox} x_{ox}}$$

If $\quad x_1 = x_{ox}$

$$\Delta V_{FB} = -\frac{Q_{ox}}{C_{ox}}$$

Combine 2 factors in real surfaces

Work function difference

$$V_{FB} = \phi_{ms}$$

Oxide charge

$$V_{FB} = -\frac{Q_i}{C_i}$$

$$V_{FB} = \phi_{ms} - \frac{Q_i}{C_i}$$

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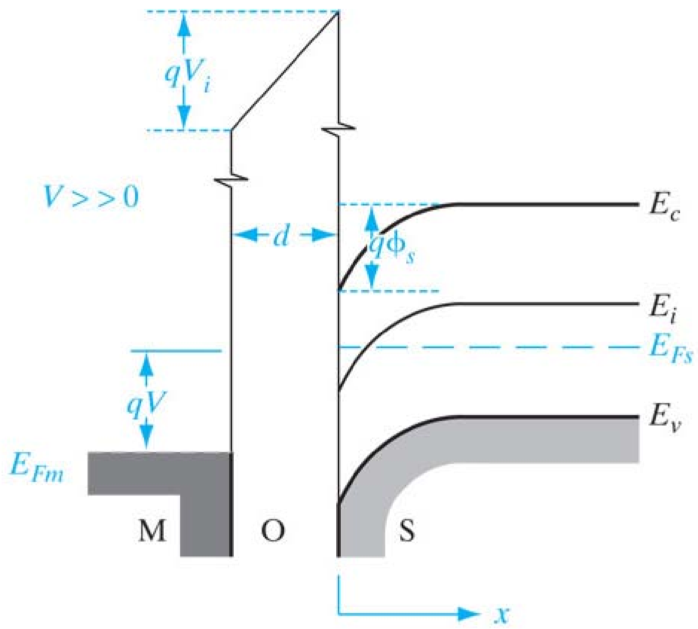
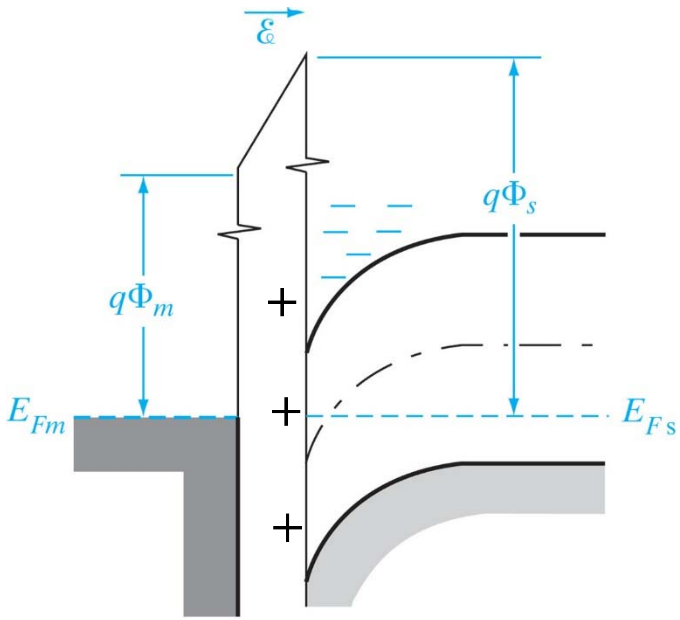
Threshold voltage

$\phi_m = \phi_s$ and no oxide charge



$$\boxed{V_T = -\frac{Q_{d\_m}}{C_i} + 2\phi_F}$$

$\phi_m \neq \phi_s$ and oxide charge exist



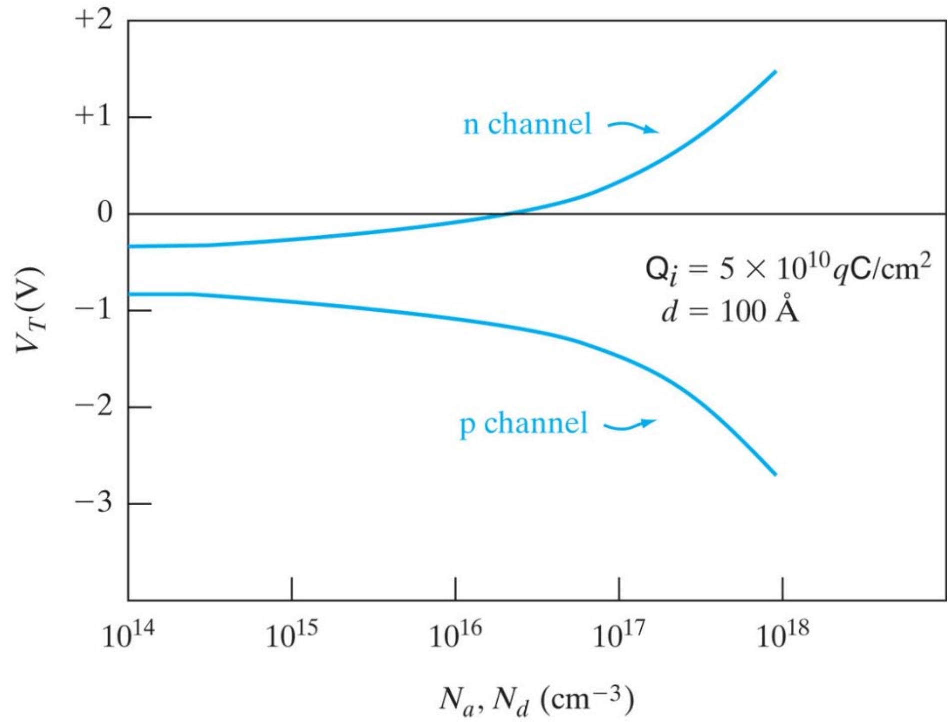
$$V_{FB} = \phi_{ms} - \frac{Q_i}{C_i}$$

$$\boxed{V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{d\_m}}{C_i} + 2\phi_F}$$

Threshold voltage

$$V_T = \boldsymbol{\phi_{ms}} \quad - \frac{\boldsymbol{Q_i}}{\boldsymbol{C_i}} \quad - \frac{Q_{dm}}{C_i} \quad + 2\boldsymbol{\phi_F}$$

	$-\frac{Q_i}{C_i}$	$-\frac{Q_{dm}}{C_i}$	$+2\phi_F$
	(-)	(+) n channel	(+) n channel
		(-) p channel	(-) p channel



p channel:

$$\phi_F \downarrow = (E_i - E_F)/q = \frac{kT}{q} ln\left(\frac{N_i}{N_d \uparrow}\right)$$

$$Q_{d\_m} \uparrow = 2\sqrt{q\epsilon_s N_d \uparrow \boldsymbol{\phi_F}}$$

- n-channel: p substrate
- p-channel : n substrate

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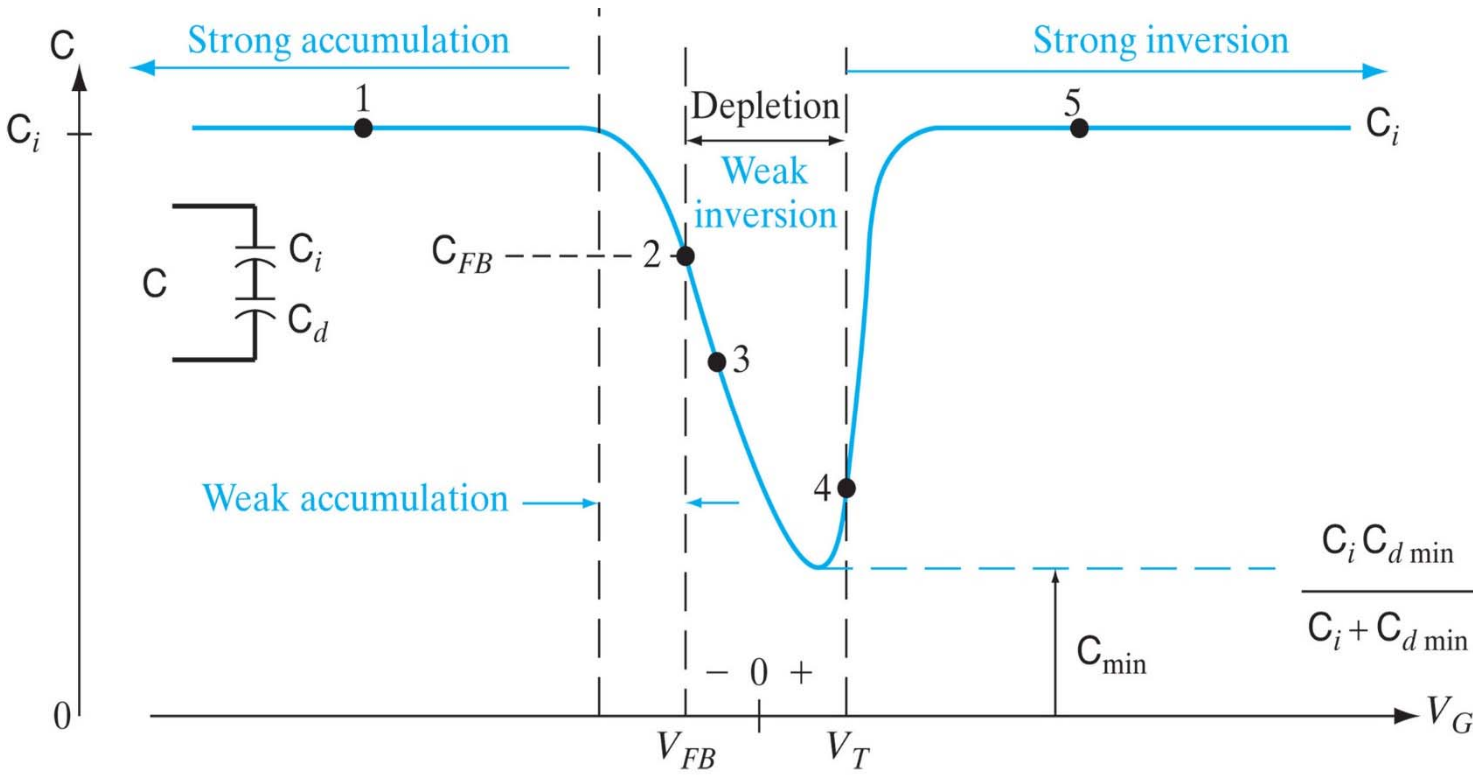
  - Substrate bias effect

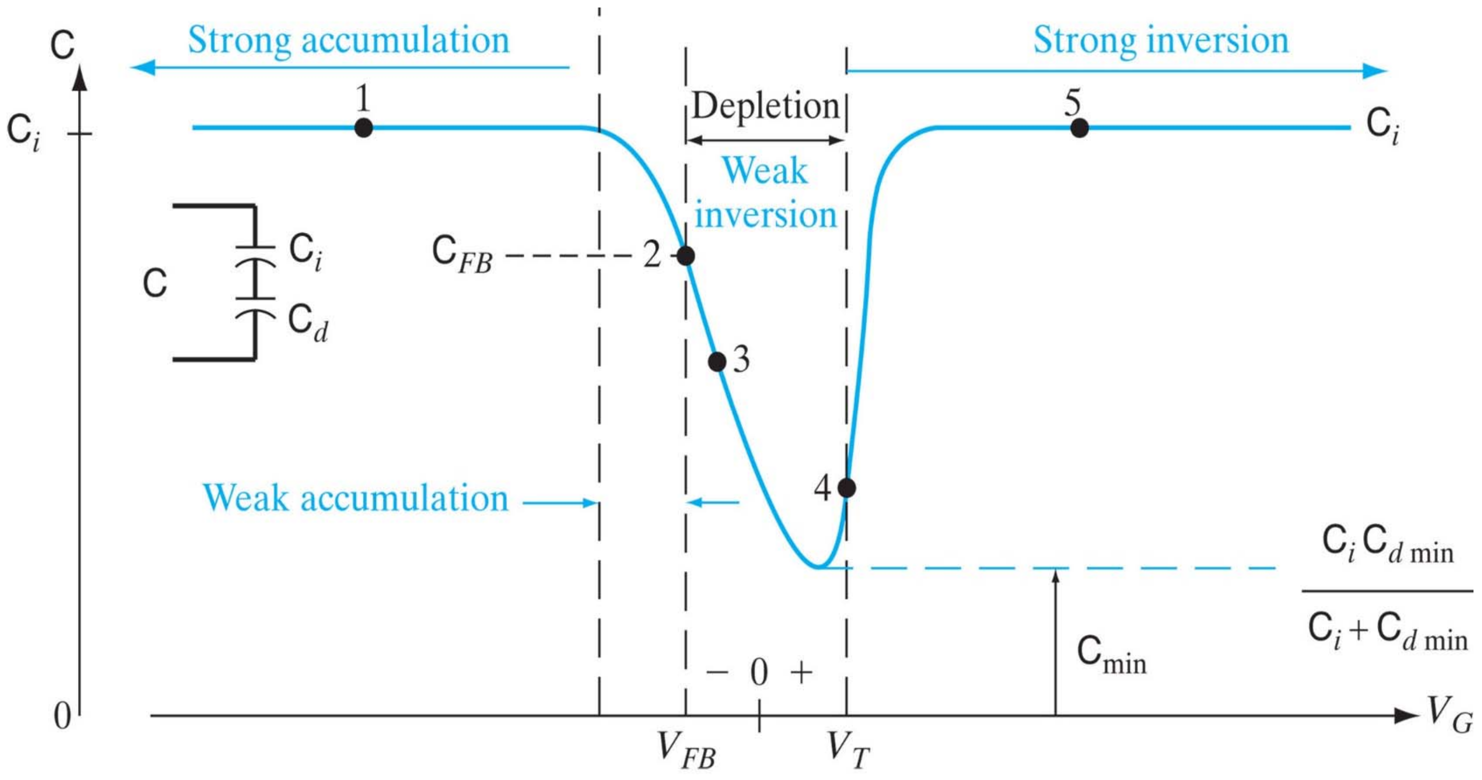
CV analysis: what information can we get from CV measurement?



(1) Insulator thickness, from

$$C_i = \frac{\epsilon_i}{d}$$

CV analysis: what information can we get from CV measurement?



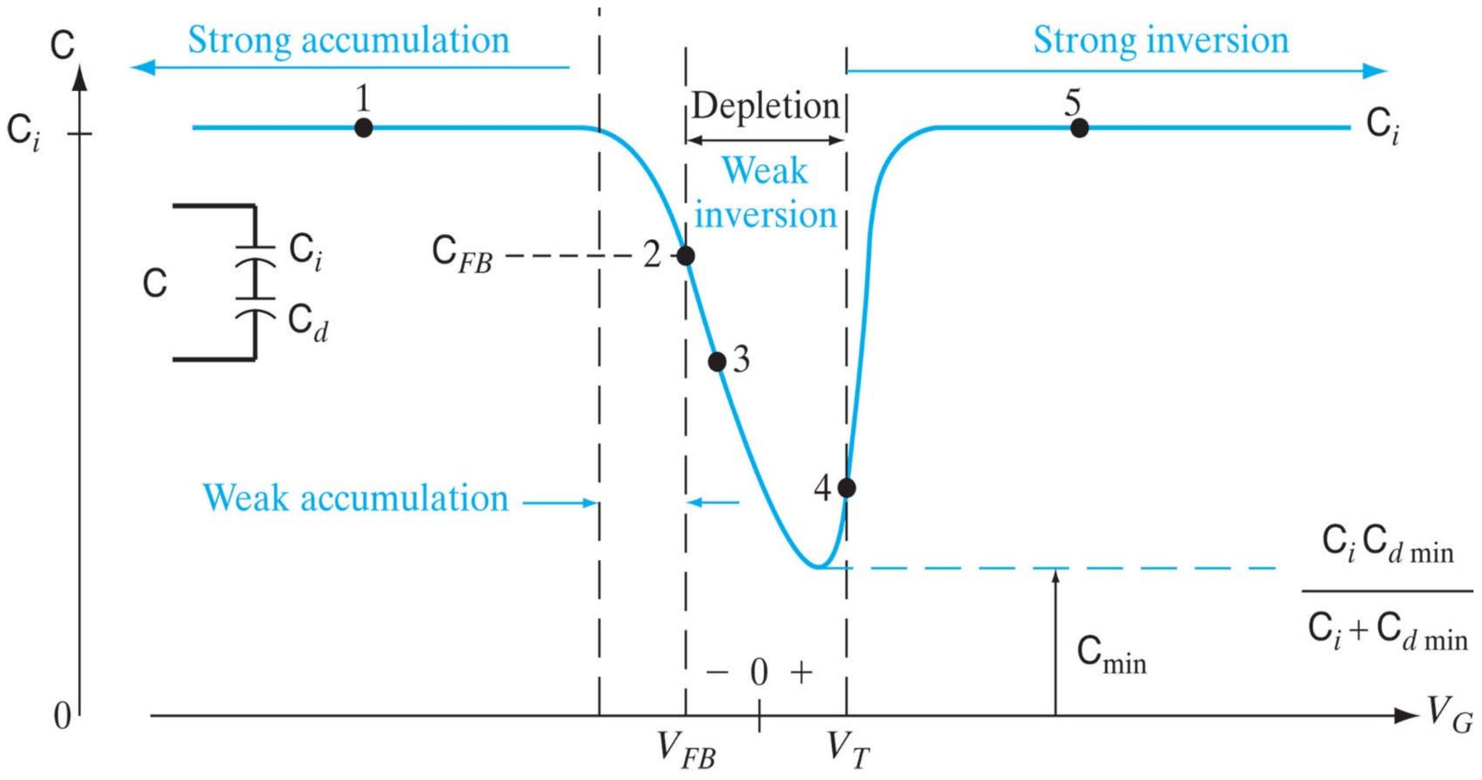
(2) Maximum depletion width, from

$$C_{dmin} = \frac{\epsilon_s}{W_m} \qquad C_{dmin} = \left(\frac{1}{C_{min}} - \frac{1}{C_i}\right)^{-1}$$

(3) Doping, from

$$W_m = 2\sqrt{\frac{\epsilon_s kT ln(N_a/N_i)}{q^2 N_a}}$$

CV analysis: what information can we get from CV measurement?



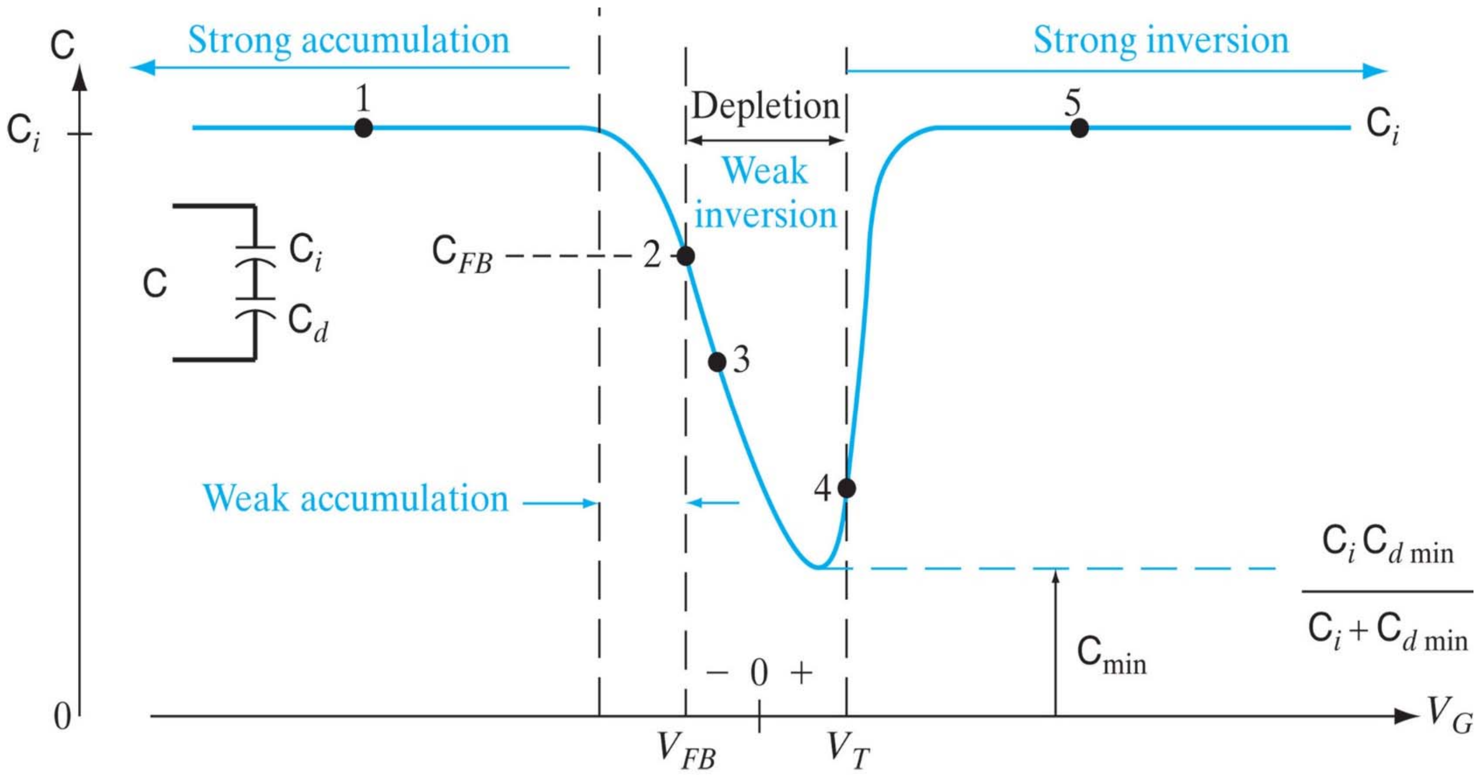
(4) Flatband capacitance

$$C_{debye} = \frac{\epsilon_s}{L_D} \qquad L_D = \sqrt{\frac{\epsilon_s kT}{q^2 N_a}}$$

$$C_{FB} = \left(\frac{C_i C_{debye}}{C_i + C_{debye}} \right)$$

(5) Flatband voltage V_{FB}, from CV plot

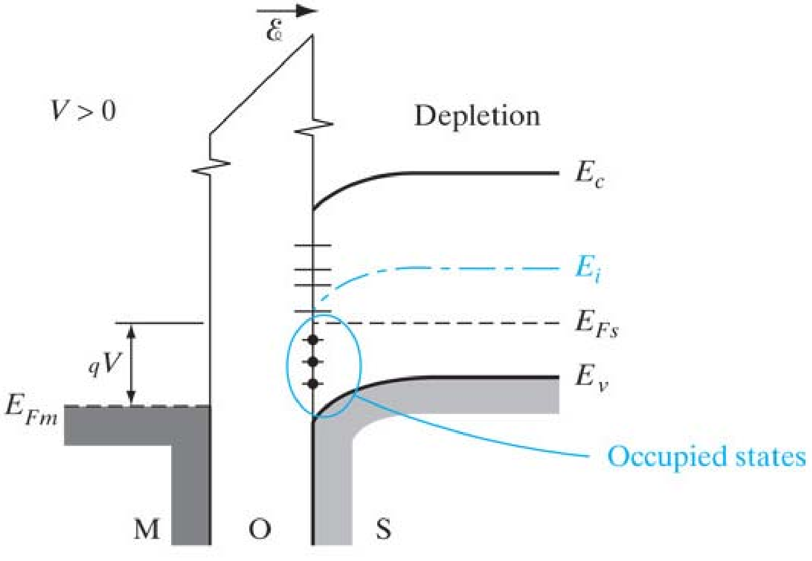
CV analysis: what information can we get from CV measurement?



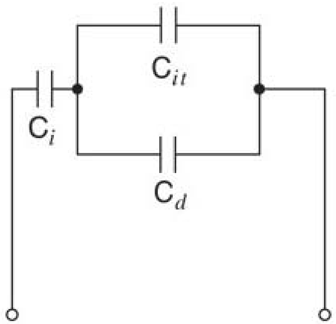
(6) Threshold voltage

$$V_T = \boldsymbol{V_{FB}} - \frac{Q_{d\_m}}{C_i} + 2\boldsymbol{\phi_F}$$

Interface trap

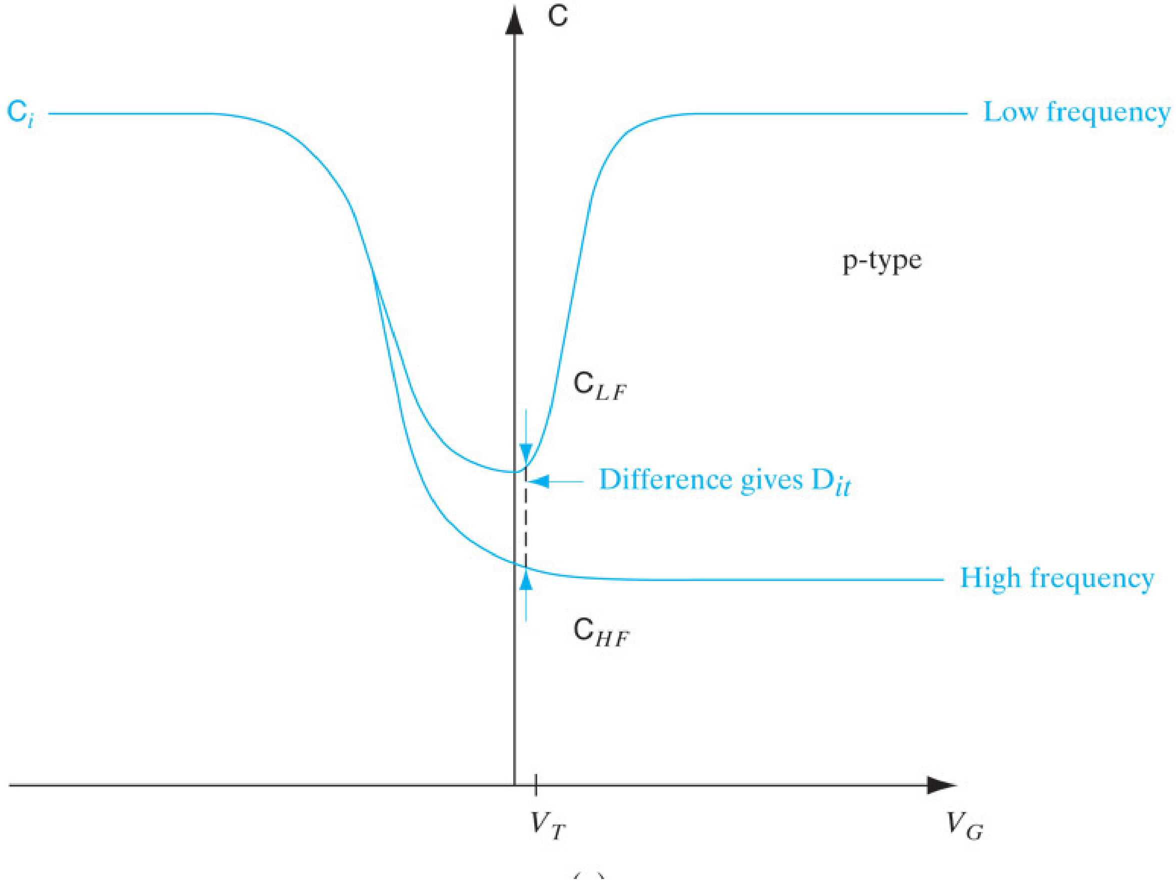


(b)



- when the interface state is below the Fermi level, it tends to trap an electron; When the interface state is above the Fermi level, it tends to give up its trapped electrons;
- This charge storage results in interface trap capacitance, which is in parallel with depletion capacitance
- The interface state can keep pace with low frequencies, not the extremely high frequencies.

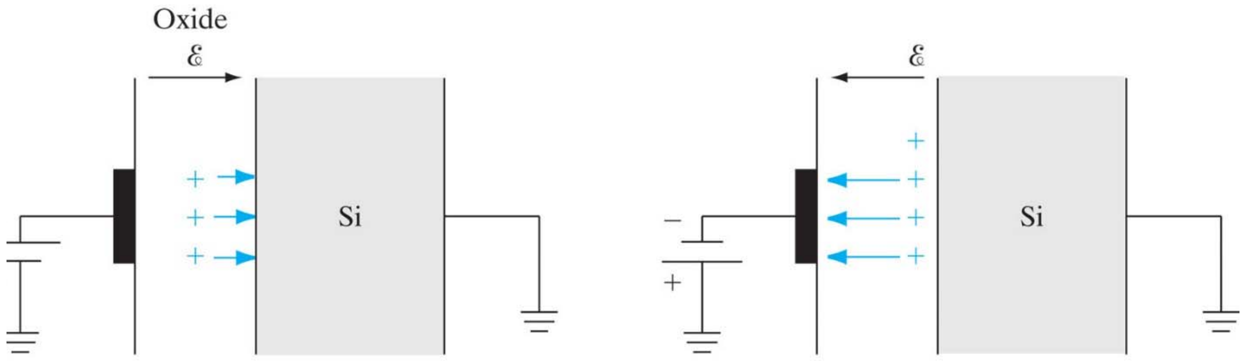
CV analysis: what information can we get from CV measurement?



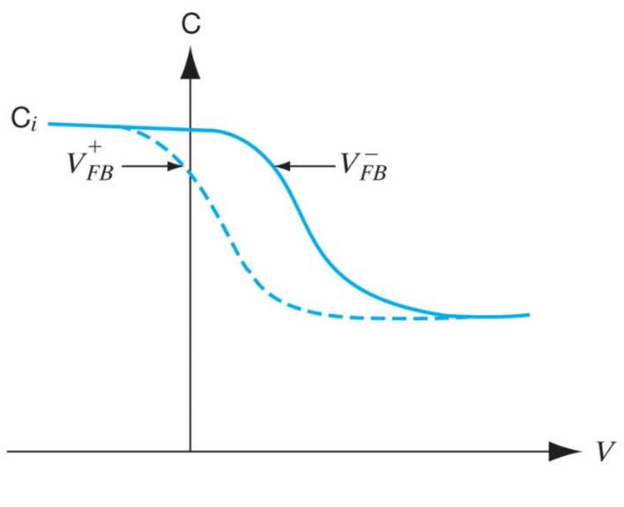
(7) Interface state density, from

$$D_{it} = \frac{1}{q}\left(\frac{C_i C_{LF}}{C_i - C_{LF}} - \frac{C_i C_{HF}}{C_i - C_{HF}}\right)$$

Mobile ion



(a)



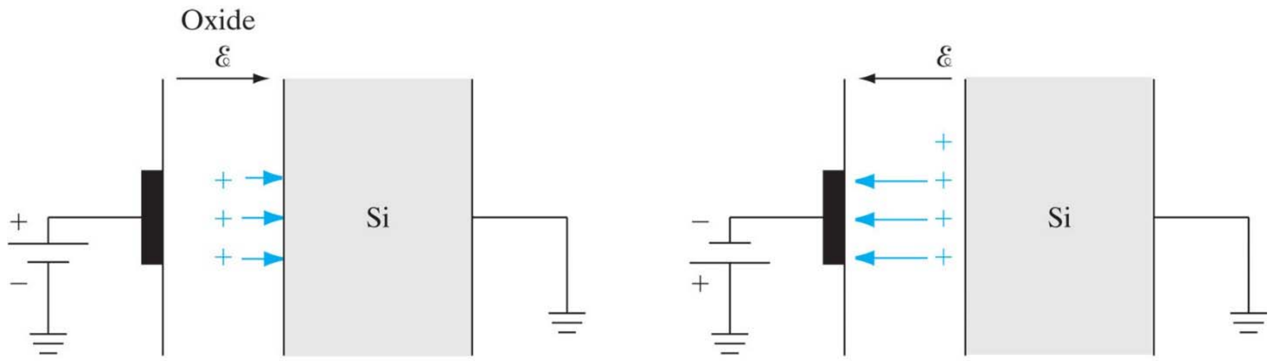
(b)

Flatband voltage shift due to mobile ion is :

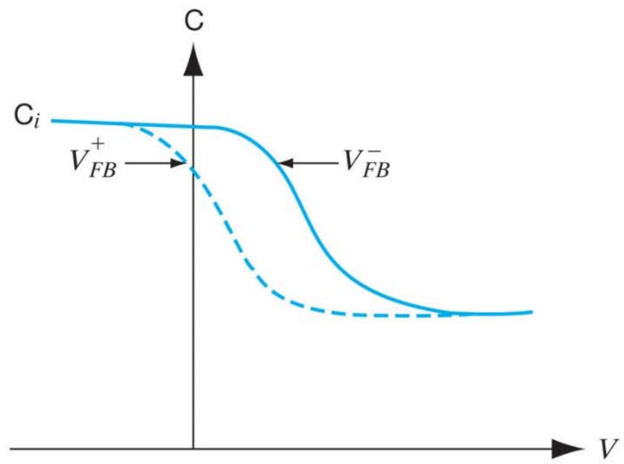
$$\Delta V_{FB} = -\frac{Q_i}{C_i} = -\frac{Q_i}{\epsilon_i}d$$

- When the mobile charge is at oxide/silicon interface $d = d_{ox}$, ΔV_{FB} is largest.
- When the mobile charge is located at metal/oxide interface d=0, ΔV_{FB}=0

CV analysis: what information can we get from CV measurement?



(a)



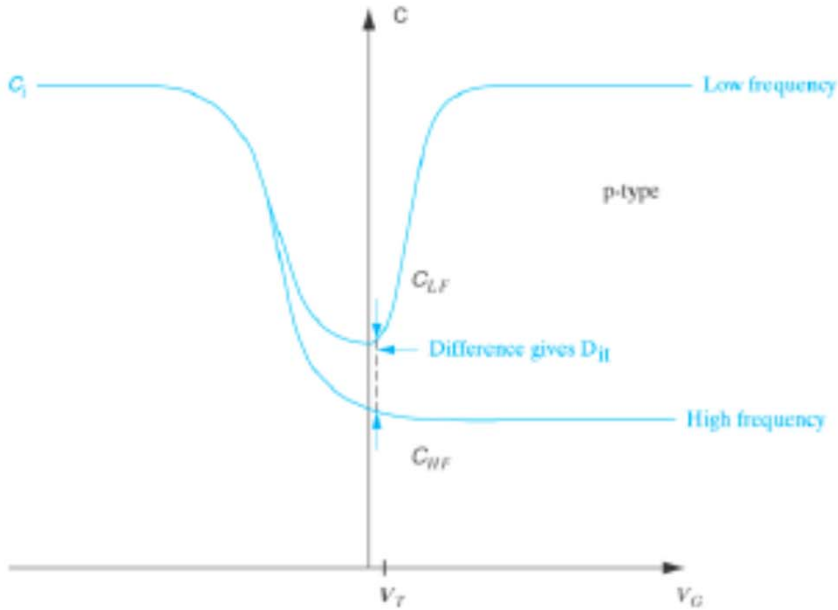
(b)

(8) Mobile ion density, from

$$Q_m = C_i(V_{FB}^{-} - V_{FB}^{+})$$

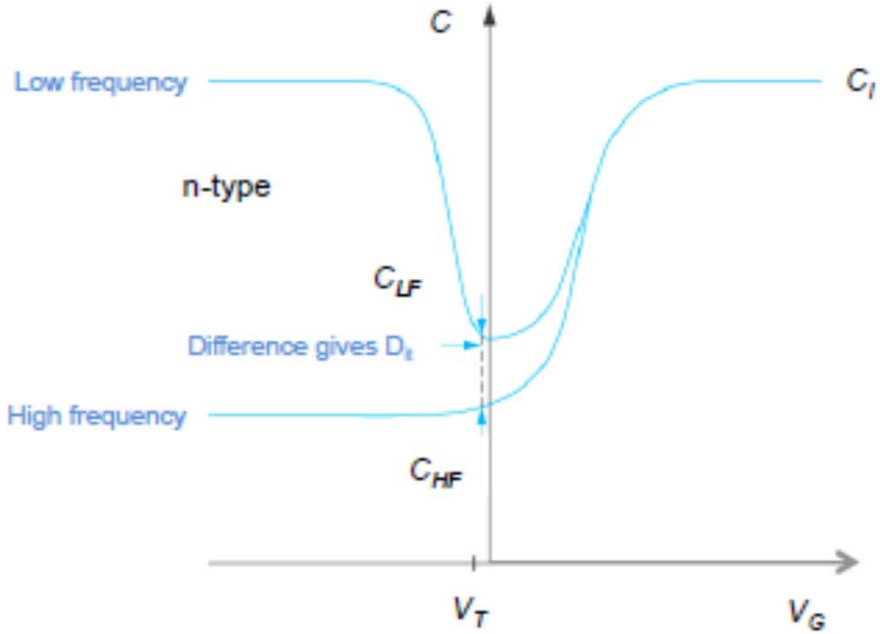
Substrate type

p-Type Substrate (Well)



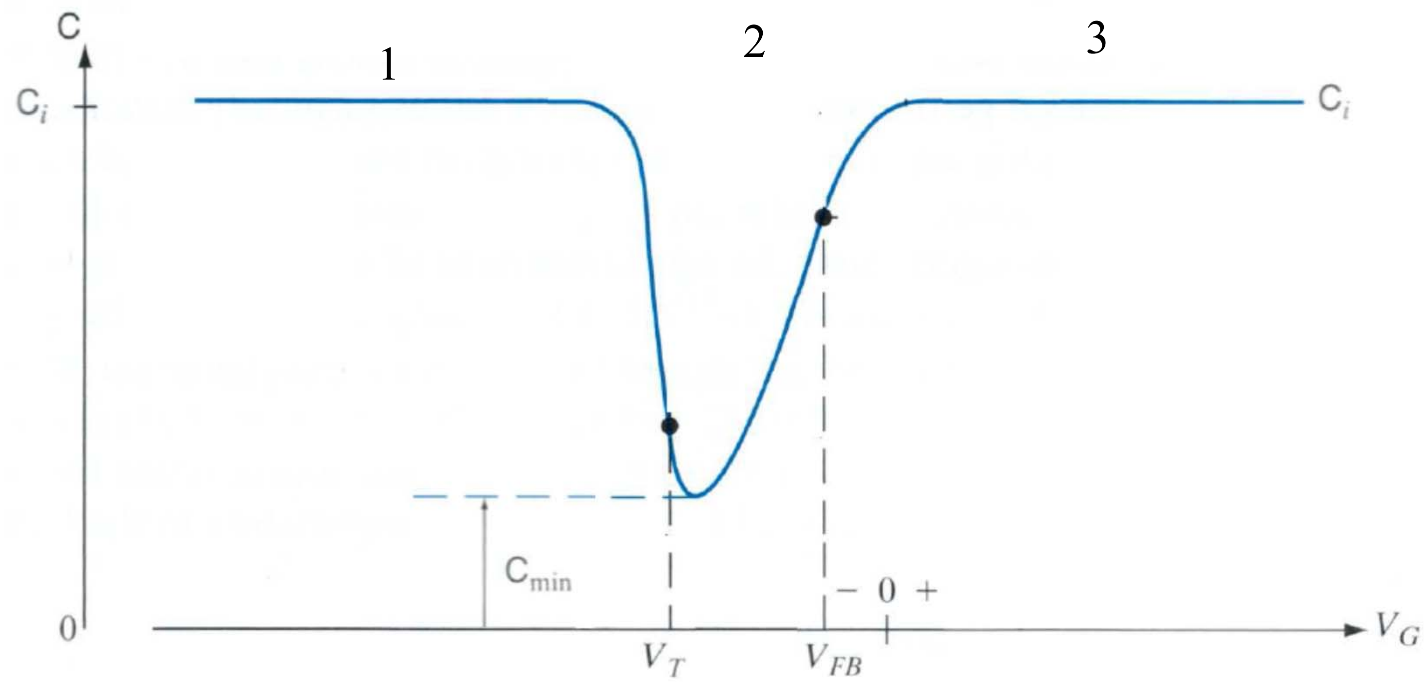
n-Channel Device

n-Type Substrate (Well)



p-Channel Device

Exercise:



Q:

- **Is this n type or p type substrate? What is the channel type?**
- **What is the region in 1, 2, 3? (accumulation, depletion, inversion etc)**
- **Is this a high-frequency or low frequency CV?**
- **What is the high frequency CV looks like?**

Outline

- Metal-insulator-semiconductor FET
  - Basic operation and fabrication
  - Ideal MOS capacitor
  - Effects of real surfaces
  - Threshold voltage
  - MOS capacitance-voltage analysis
  - The MOS field-effect transistor
  - Substrate bias effect

Gate voltage and charge

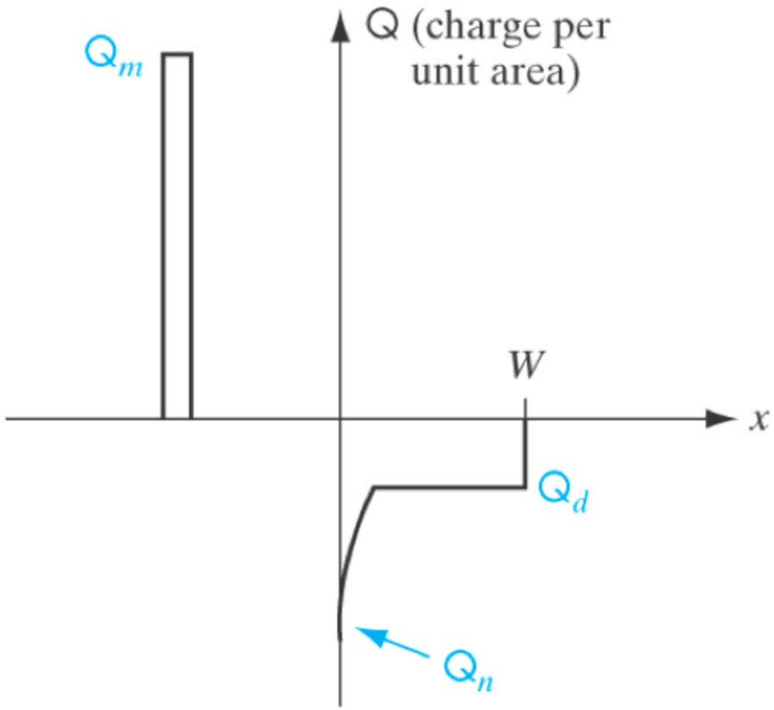
When V_D=0:

$$V_G = V_{FB} - \frac{Q_s}{C_i} + \phi_s$$

Voltage to achieve flatband

Voltage Due to Charge Across Insulator

Potential Across Semiconductor



$$Q_s = Q_d + Q_n$$

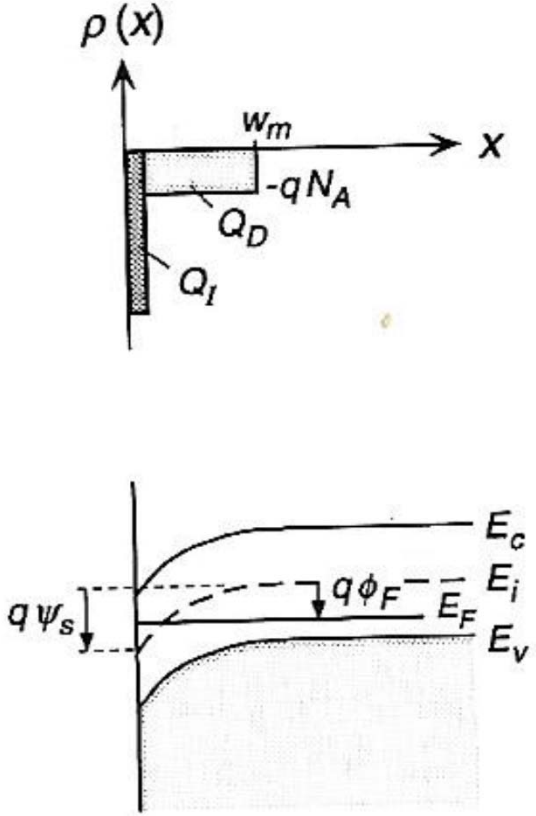
$$Q_n = -C_i\left[V_G - \left(V_{FB} - \frac{Q_d}{C_i} + \phi_s\right)\right]$$

Above Threshold ($V_G > V_T$):

$$Q_n = -C_i(V_G - V_T)$$

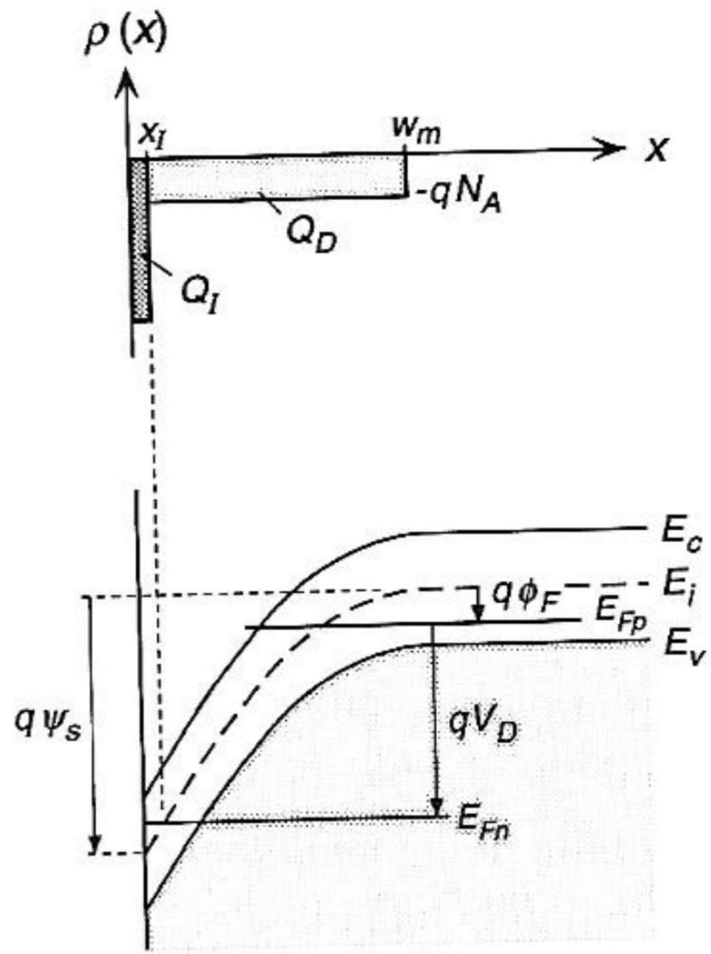
Effect of Drain bias

$V_D = 0$



$$Q_n = -C_i\left(V_G - V_{FB} - 2\phi_F - \frac{1}{C_i}\sqrt{2q\epsilon_s N_a 2\phi_F}\right)$$

$V_D \neq 0$



$$Q_n = -C_i\left(V_G - V_{FB} - 2\phi_F - V_x - \frac{1}{C_i}\sqrt{2q\epsilon_s N_a(2\phi_F + V_x}\right)$$

Charge with applied drain voltage

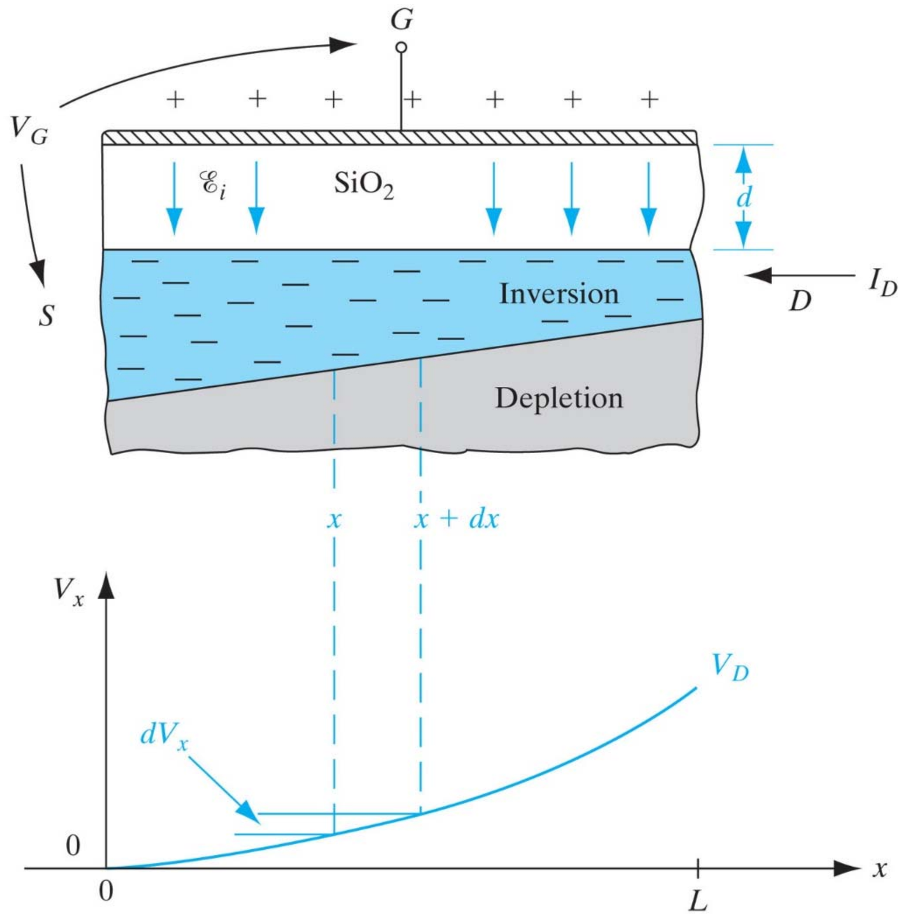
When $V_D \neq 0$, there is any voltage rise V_x from the source at any point x in channel, if neglecting the variation in Q_d:

$$Q_n = -C_i(V_G - V_T - V_x)$$

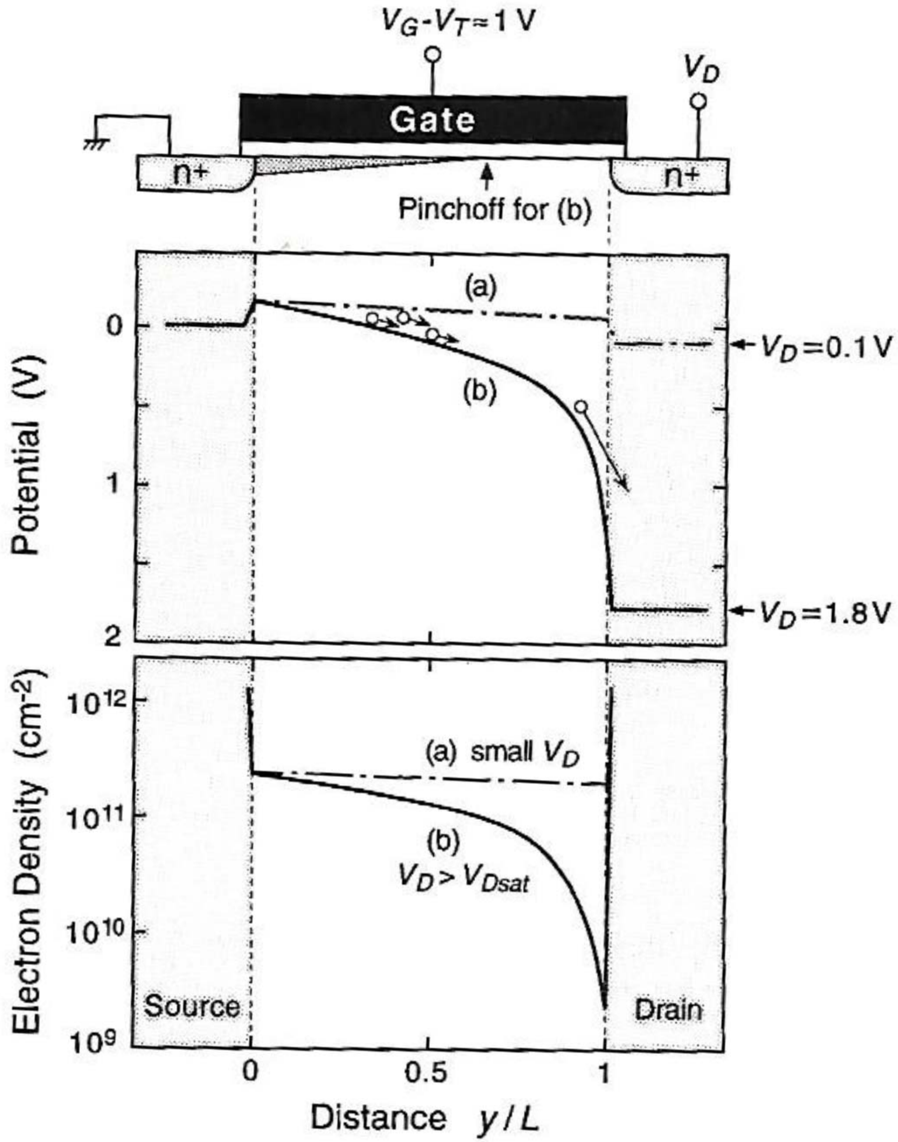
$$I_D = \overline{\mu_n} W |Q_n(x)| \frac{dV_x}{dx}$$

$$\boxed{I_D = \frac{\overline{\mu_n} W C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]}$$

Define $\mathbf{k_N} = \dfrac{\overline{\mu_n}\mathbf{WC_i}}{\mathbf{L}}$



Potential and electron density distribution



(a) Linear regions

(b) Saturation regions

Output characteristics: linear region

- Linear region $V_D<(V_G - V_T)$

$$\boxed{I_D = \frac{\overline{\mu_n} W C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]}$$

If $V_D<<(V_G - V_T)$

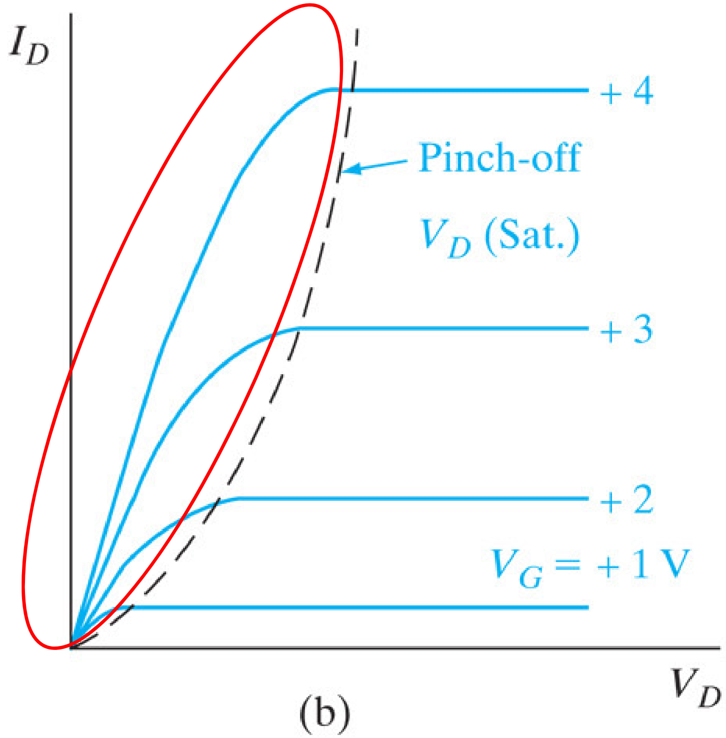
$$\boxed{I_D = \frac{\overline{\mu_n} W C_i}{L}(V_G - V_T)V_D}$$

Conductance of the channel

$$g_D = \frac{\partial I_D}{\partial V_D} \cong \frac{W}{L}\overline{\mu_n} C_i (V_G - V_T)$$

Transconductance

$$g_m = \frac{\partial I_D}{\partial V_G} \cong \frac{W}{L}\overline{\mu_n} C_i V_D$$



Output characteristics: saturation region

- Saturation condition $V_D \cong (V_G - V_T)$

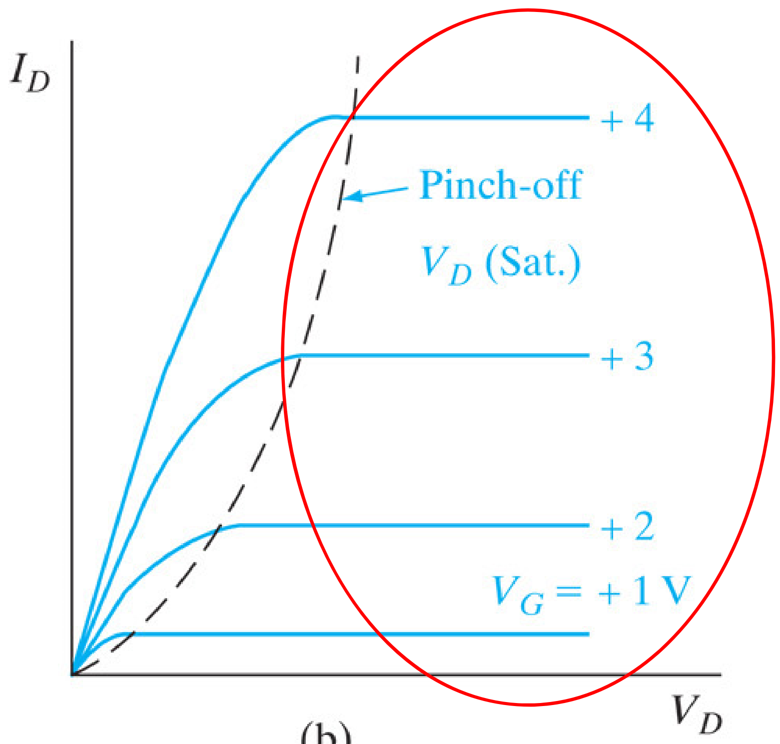
$$I_D(sat.) = \frac{W}{2L}\overline{\mu_n}C_i(V_G - V_T)^2 = \frac{W}{2L}\overline{\mu_n}C_i V_D^2(sat.)$$

Conductance of the channel

$$g_D = \frac{\partial I_D}{\partial V_D} \cong 0$$

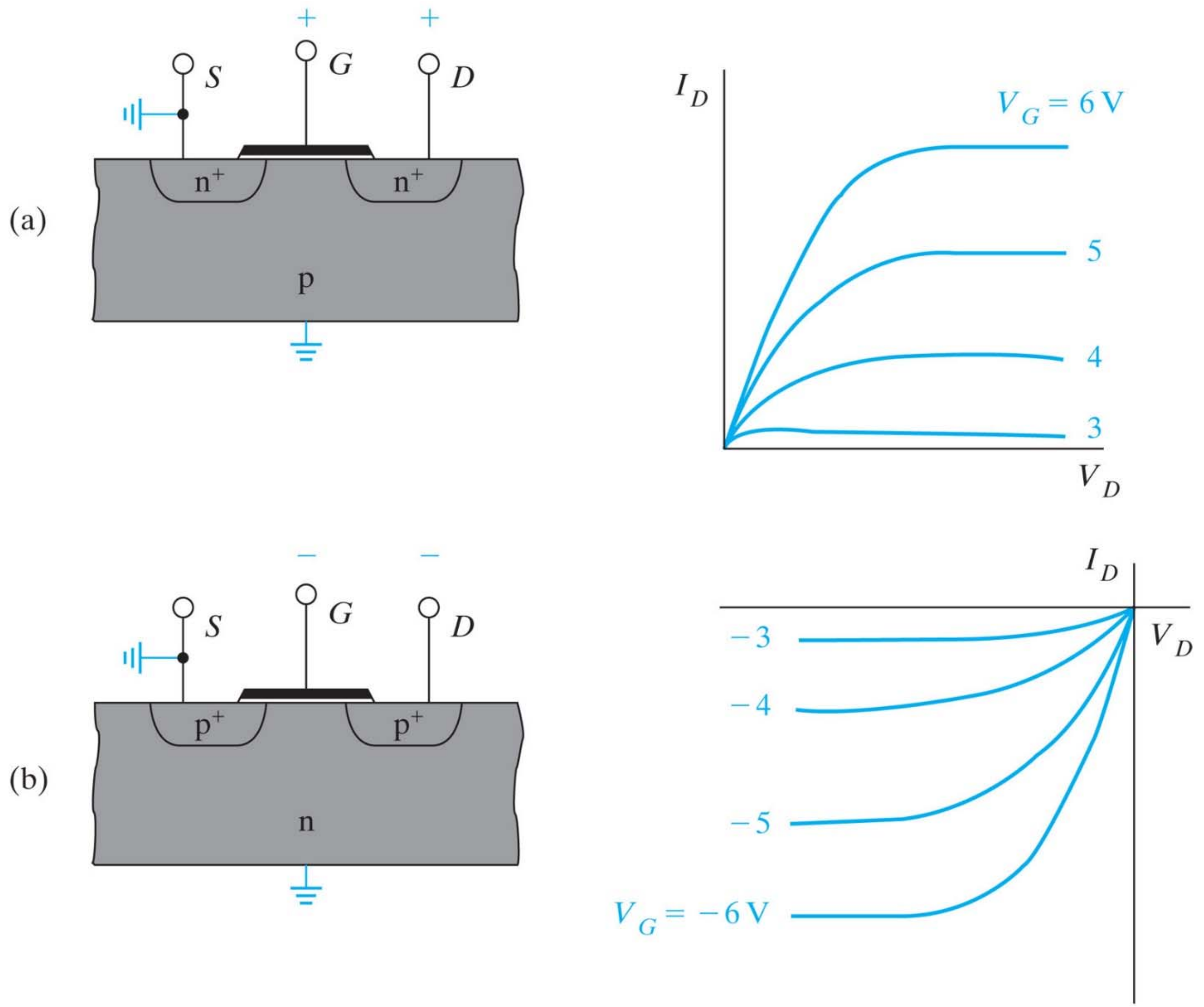
Transconductance

$$g_m(\text{sat.}) = \frac{\partial I_D(sat.)}{\partial V_G} \cong \frac{W}{L}\overline{\mu_n}C_i(V_G - V_T)$$



(b)

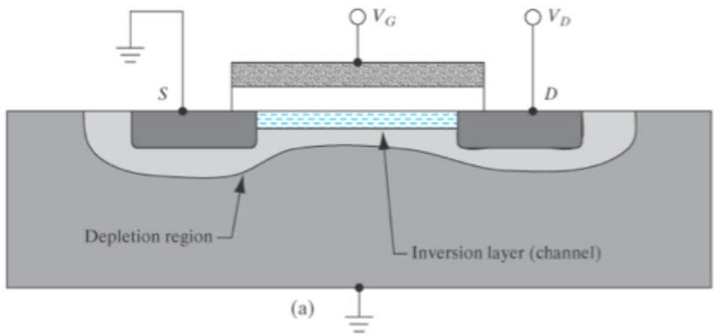
Output characteristics

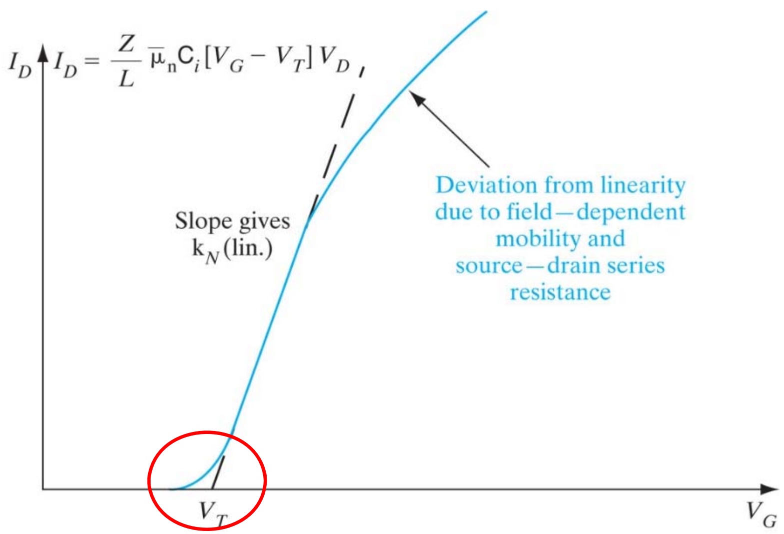


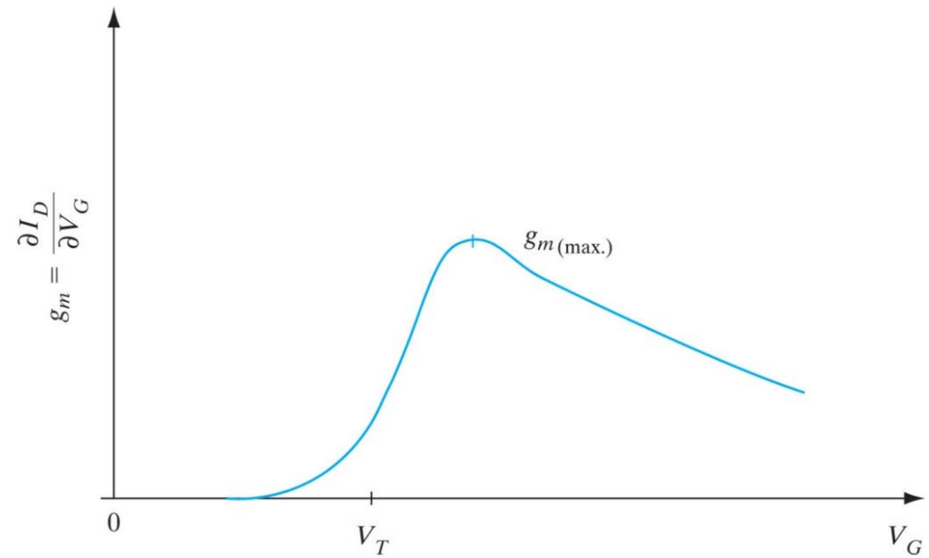
n-MOSFET

p-MOSFET

Transfer characteristics: linear region

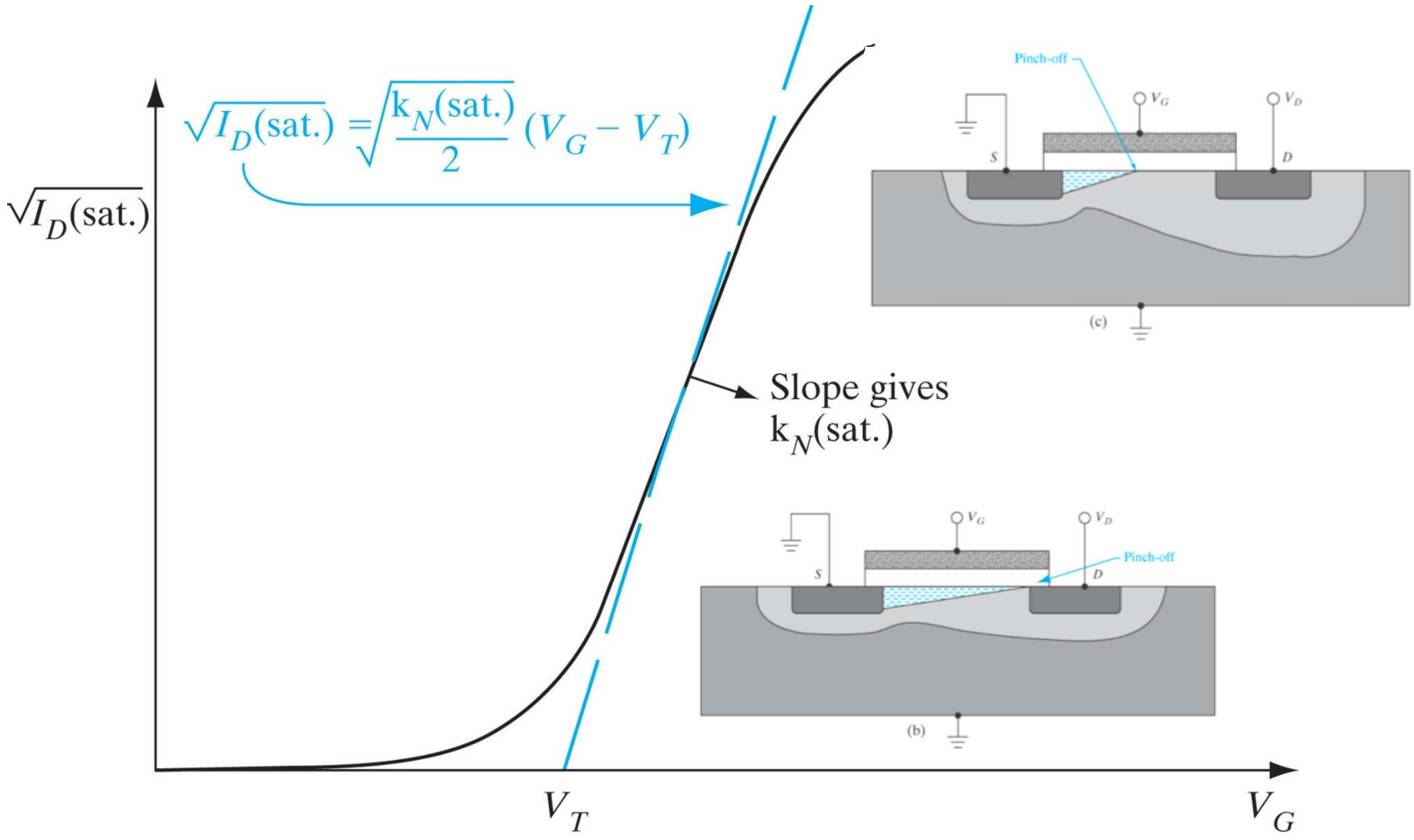






$\boldsymbol{Q_n = -C_i(V_G - V_T)}$ is not valid near $\boldsymbol{V_G = V_T}$

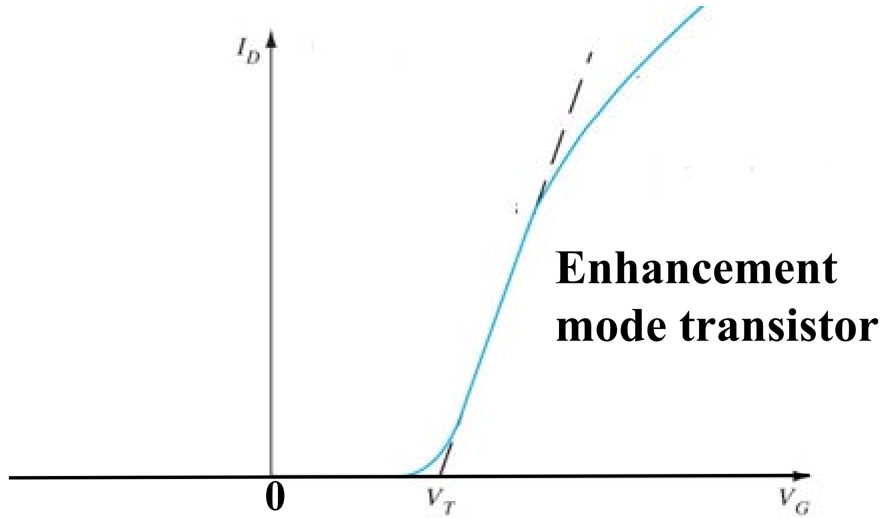
Transfer characteristics: Saturation region

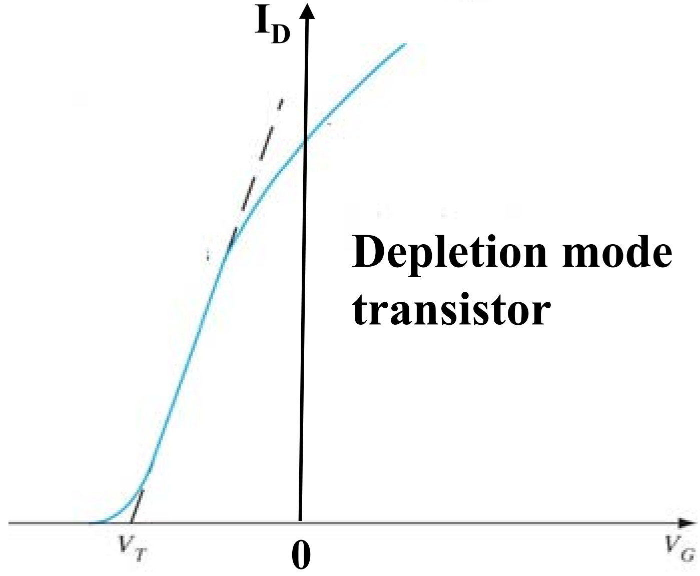


MOSFET type

- n-MOSFET: p substrate
- p-MOSFET: n substrate

- Enhancement mode transistor: normally off,
  - nMOSFET V_T>0, or pMOSFET V_T <0
- Depletion mode transistor: normally on
  - nMOSFET V_T <0, or pMOSFET V_T >0





Exercise: MOSFET

Consider an enhancement-mode Si n-MOSFET with a length of L= 1 μm, width of W = 20 μm, a silicon oxide (ε_{SiO2}=0.35x10^{-12}F/cm) thickness of t_{OX}=40 nm, and a threshold voltage V_T=1 V. The drain-source voltage V_{DS}=5 V and the gate voltage V_{GS}=3 V. Assume zero substrate bias and a mobility of 300 cm^2/V·s.

Q:

1.what kind of device is this? (Majority carrier or minority carrier)

2. What is the type of substrate? (n, p or intrinsic)

3. Assume Silicon and Aluminum gate metal work functions of Φ_{SI} ~ 5 eV & Φ_{Al} =4 eV. What type of bias we need to apply to achieve flat band condition? (+, - or no bias)

4. Which operation mode/region is this device in? (linear or saturation)

5. Calculate the drain current (ID).

Exercise: MOSFET, solution

Consider an enhancement-mode Si n-MOSFET with a length of L= 1 μm, width of W = 20 μm, a silicon oxide (ε_{SiO2}=0.35x10^{-12}F/cm) thickness of t_{OX}=40 nm, and a threshold voltage V_T=1 V. The drain-source voltage V_{DS}=5 V and the gate voltage V_{GS}=3 V. Assume zero substrate bias and a mobility of 300 cm^2/V·s.

Q:

1.what kind of device is this? (Majority carrier or <u>minority carrier</u>)

2. What is the type of substrate? (n, <u>p</u> or intrinsic)

3. Assume Silicon and Aluminum gate metal work functions of Φ_{SI} ~ 5 eV & Φ_{Al} =4 eV. What type of bias we need to apply to achieve flat band condition? (positive, <u>negative</u>, or no bias)

4. Which operation mode/region is this device in? (linear or <u>saturation</u>)

5. Calculate the drain current (I_D).

$$\boxed{I_D(sat.) = \frac{W}{2L}\overline{\mu_n}C_iV_D^2(sat.)}$$

$$C_i = \frac{\varepsilon_{SiO2}}{t_{ox}}$$

Outline

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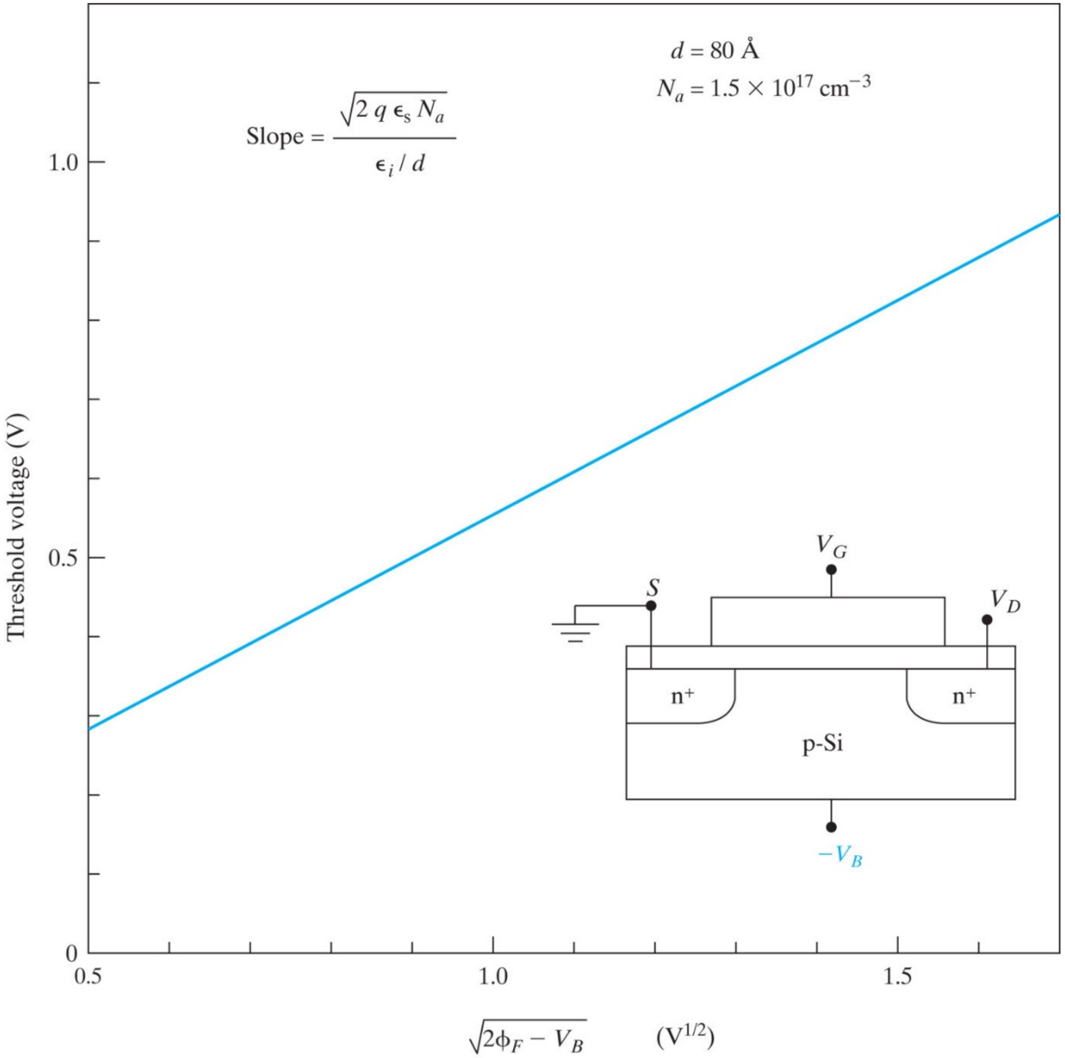
Substrate bias effect



When a reverse bias is applied between substrate and the source, the depletion region is widen and the depletion charge is changes to:

$$Q'_d = 2\epsilon_s q N_a (2\phi_F - V_B)^{1/2}$$

The change in threshold voltage due to substrate bias is:

$$\Delta V_T = \frac{\sqrt{2\epsilon_s q N_a}}{C_i}\left[(2\phi_F - V_B)^{1/2} - (2\phi_F)^{1/2}\right]$$