1. MOS CAPACITORS

(A). First, we find

$$\phi_F = \frac{kT}{q}\ln\frac{N_a}{n_i} = 0.365 \text{ eV} \tag{1.1}$$

The depletion charge is given as

$$Q_d = -\sqrt{2qN_a\varepsilon_s 2\phi_F} = -6.99\times10^{-8} \text{ C} \tag{1.2}$$

And the insulator capacitance is given as

$$C_i = \frac{\varepsilon_i}{d} = 1.73\times10^{-8} \text{ F/cm}^2 \tag{1.3}$$

Therefore, in the ideal case where the metal work function is negligible,

$$V_T = -\frac{Q_d}{C_i} + 2\phi_F = \boxed{4.78 \text{ V}} \tag{1.4}$$

(B). For the real case, we consider the difference in work functions of the gate metal and the semiconductor.

$$\Phi_{ms} = \Phi_m - (q\chi_s + E_g/2 + (E_i - E_F)) = -0.375 \text{ eV} \tag{1.5}$$

Therefore, the threshold voltage can be calculated as

$$V_F = \Phi_{ms} - \frac{Q_d}{C_i} + 2\phi_F = \boxed{4.41 \text{ V}} \tag{1.6}$$

(C). To find the minimum capacitance, we must first find the maximum depletion width

$$W_m = 2\sqrt{\frac{\varepsilon_s kT\ln(N_a/n_i)}{q^2N_a}} = \boxed{0.217\ \mu\text{m}} \tag{1.7}$$

which allows us to find the minimum depletion capacitance as

$$C_d = \frac{\varepsilon_s}{W_m} = 4.81\times10^{-8} \text{ F/cm}^2 \tag{1.8}$$

Then, the minimum capacitance is the result of the depletion capacitance and the insulator capacitance in parallel

$$C_{min} = \frac{C_iC_d}{C_i + C_d} = \boxed{1.27\times10^{-8} \text{ F/cm}^2} \tag{1.9}$$

(D). The plot is shown in Fig. 1.1. The points V_T, V_{FB}, and C_{min} must be labeled for full credit.

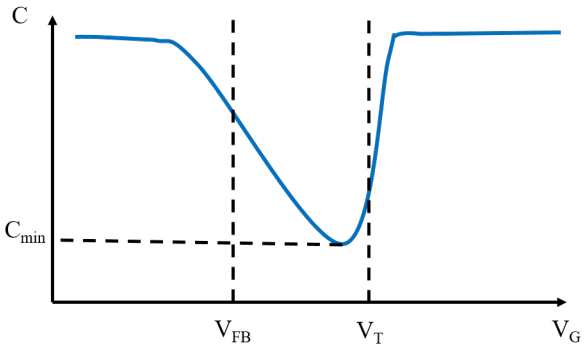

Figure 1.1: Capacitance vs. Voltage characteristics for an *n*-channel MOS capacitor.

(E). To find the ideal case threshold voltage, we follow the same procedure as above. Note, however, that the both terms in the ideal threshold equation change sign. That is,

$$V_T = -\frac{Q_d}{C_i} - 2\phi_F = \boxed{-3.49 \text{ V}} \tag{1.10}$$

In the case of real metal, we must first find the work function of the semiconductor given as $q\chi_s + Eg/2 - (E_F - E_i) = 4.258$ eV. Therefore, the threshold considering the metal work function is

$$V_T = \Phi_{ms} - \frac{Q_d}{C_i} - 2\phi_F = \boxed{-3.15 \text{ V}} \tag{1.11}$$

Note that in this case, $\Phi_{ms} > 0$.

The maximum width is calculated the same way as in part (c) above and can be found to be $\boxed{0.296\ \mu\text{m}}$. Therefore, the minimum capacitance is $\boxed{1.16\times10^{-8}\ \text{F/cm}^2}$.

The C vs. V_G plot of the *p*-channel MOS will be very similar to the *n*-channel device in part (d). The plot is shown in Fig. 1.2. Note that the curve seems reversed in voltage with respect to the *n*-channel one. Also note that flatband, threshold, and minimum capacitance must be labeled for full credit.

2. MOSFET Output Characteristics

We start by first calculating the threshold voltage for the device, ignoring the metal work function. We find

$$\phi_F = \frac{kT}{q}\ln\frac{N_a}{n_i} = 0.383 \text{ eV} \tag{2.1}$$

$$W_m = 2\sqrt{\frac{\varepsilon_s\phi_F}{qN_a}} = 1.58\times10^{-5} \text{ cm} = 0.158\ \mu\text{m} \tag{2.2}$$

$$C_i = \frac{\varepsilon_i}{d} = 2.876\times10^{-7} \text{ F/cm}^2 \tag{2.3}$$

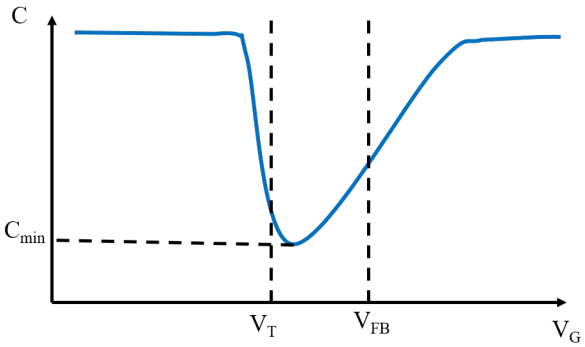

Figure 1.2: Capacitance vs. Voltage characteristics for a *p*-channel MOS capacitor.

$$V_T = -\frac{Q_D}{C_i} + 2\phi_F = 1.12 \text{ V} \tag{2.4}$$

The plots of drain current for various gate voltages are found in Fig. 4.1. Note that Eqns. 6-49, 6-52, and 6-53 are used to find the expressions for the linear and saturation currents.

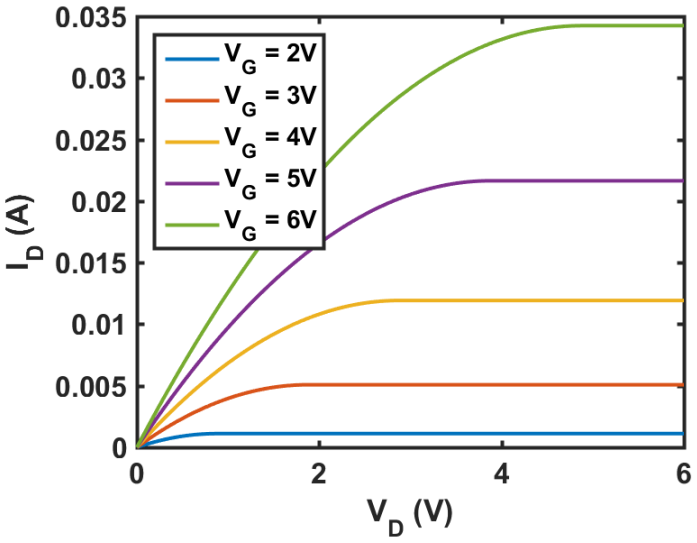

Figure 2.1: Drain current vs. drain voltage for various gate voltages.

3. MOSFET Characteristics Cont'd

(A). The plot is shown in Fig. 3.1. Note that all three regions as well as maximum capacitance must be labeled. To find the maximum capacitance,

$$C_{max} = \frac{\varepsilon_i}{d} = 1.77 \times 10^{-6} \text{ F/cm}^2 \tag{3.1}$$

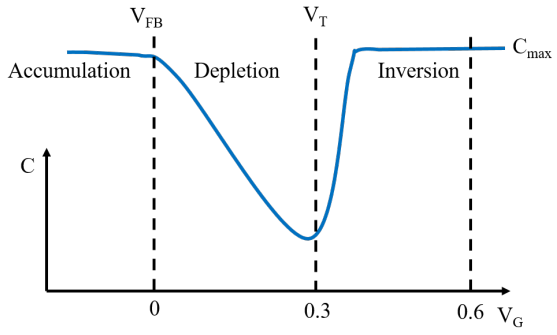

Figure 3.1: Plot of capacitance vs. V_{GS} noting the three different regions of operation as well the maximum capacitance, threshold voltage, and flat-band voltage.

(B). The plot is VERY similar to the plot for part (a) shown in Fig. 3.1. This is due to the nearby source of carriers.

(C). From Eqn. 6-53, we know that

$$I_D(sat.) \propto (V_G - V_T)^2 \tag{3.2}$$

Therefore, taking the ratio of the two equations, we find

$$\frac{800}{200} = \frac{(V_{G2} - V_T)^2 \, ent}{(V_{G1} - V_T)^2} = 4 \tag{3.3}$$

Solving then for V_{G2}, we find $V_{G2} = 0.9$ V.

(D). The plot of I_D vs. V_{GS} is shown in Fig. 3.2. Note that full credit requires labeling of 'off', 'saturation', and 'linear' regimes as well as 'V_T' and 'V_{GS}'.

(E). Since $V_{GS} < V_{DS} + V_T$, we are in the saturation regime. Therefore,

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{Z}{L} \mu C_i (V_{GS} - V_T) \tag{3.4}$$

Therefore, $g_m = 0.013$ F/s $= 13$ mA/V (or mS).

4. Integrated Circuits

(A.) The circuit diagram for a p-MOS inverter is shown in Fig. 4.1. Note that the source and drain are flipped relative to the n-MOS circuit. In general, these type of single transistor designs are undesirable because, by design, one of the states of the inverter requires a constant current flow during operation. This means that the device is constantly consuming power in one of the two states. In contrast, when the CMOS inverter is in either logic state, the current is limited to the leakage current of the transistors and is thus very low.

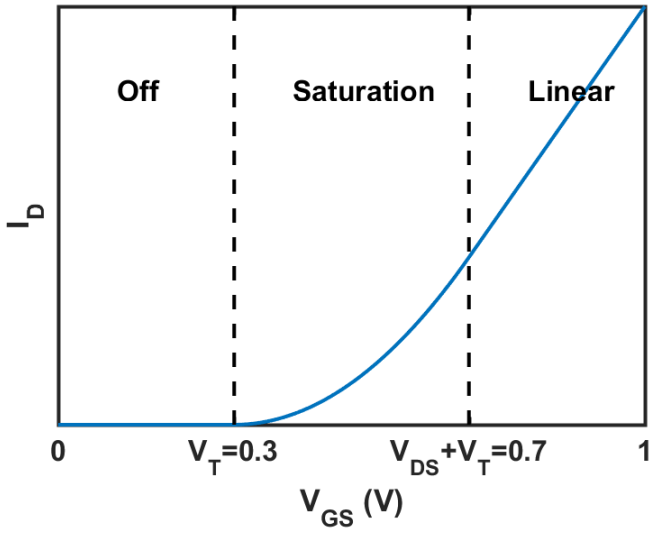

Figure 3.2: Plot of drain current vs. source-gate voltage showing the three regions of operation.

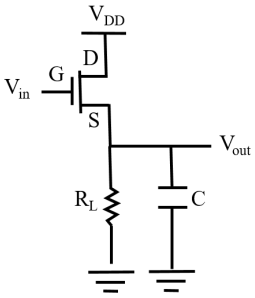

Figure 4.1: Schematic for an inverter with a p-MOSFET.

(B). To find the input voltage for the transistion region, we use the fact that in DC there is no current flowing out of the output node. Therefore, the drain current of the n-MOS must equal that of the p-MOS. So,

$$\frac{1}{2}\mu_n C_i \left(\frac{Z}{L}\right)_n (V_m - T_{TP})^2 = \frac{1}{2}\mu_p C_i \left(\frac{Z}{L}\right)_p (V_{DD} - V_m + V_{TP})^2 \tag{4.1}$$

For simplicity, we will define

$$\chi = \sqrt{\mu_n (Z/L)_n} / \sqrt{\mu_p (Z/L)_p} \tag{4.2}$$

Rearranging to solve to V_m, we find that

$$V_m = \frac{V_{DD} + \chi V_{TN} + V_{TP}}{1 + \chi} \tag{4.3}$$

In order then for V_m to be $V_{DD}/2$, $V_{TP} = -V_{TN}$ and $\chi = 1$ by inspection. That means that

$$\mu_n (Z/L)_n = \mu_p (Z/L)_p \tag{4.4}$$

This poses a design issue, where an imbalance in channel mobilities can cause our CMOS designs to have lopsided components, which ultimately hinders our designs for an integrated circuit. The problem is very noticeable in III-V materials, where the electron and hole mobilities can differ by factors of 10 or more.