ECE 340: Semiconductor Electronics

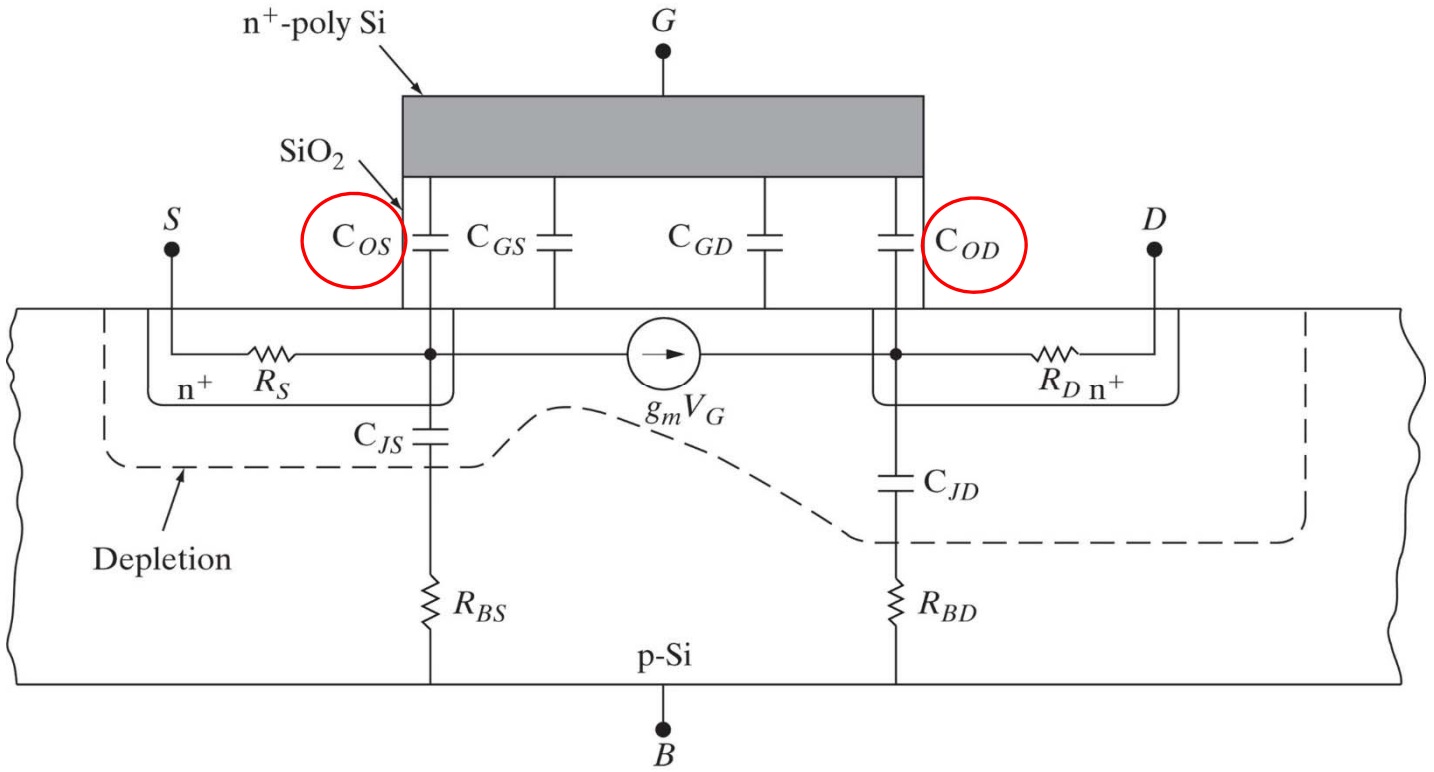
Chapter 9: Integrated Circuit

Wenjuan Zhu

Outline

- Equivalent circuit for the MOSFET
- Resistive load-NMOSFET-common-source amplifier
- CMOS inverter (Integrated Circuits)
- CMOS processing

Equivalent circuit of a MOSFET



- **Gate capacitance: sum of distributed capacitance from gate to channel (C_{GS}, C_{GD}) and overlap capacitance (C_{OS}, C_{OD}). C_{OD} is known as Miller overlap capacitance, represents a feedback path.**
- **Gate controlled constant-current source**
- **pn junction depletion capacitance (C_{JS}, C_{JD}),**
- **parasitic resistance (R_S, R_D)**

Equivalent circuit of a MOSFET

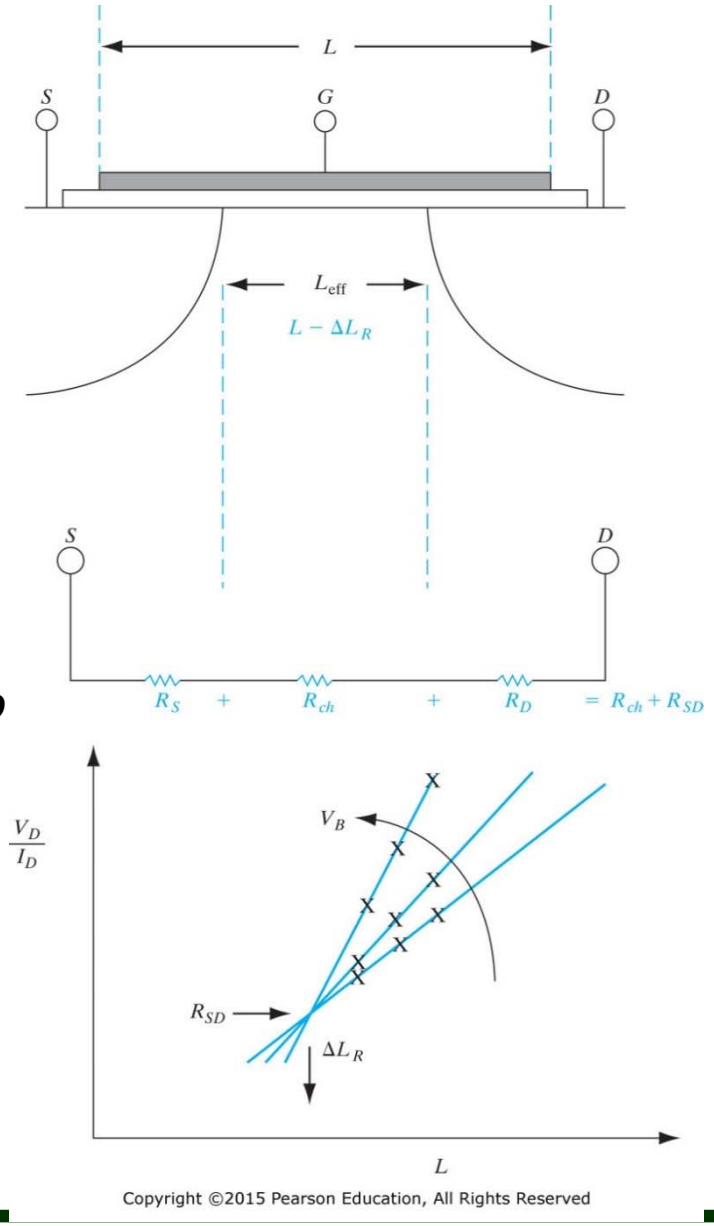
Effective channel length:

$$L_{eff} = L - \Delta L_R$$

ΔL_R is the spread of source drain under the gate

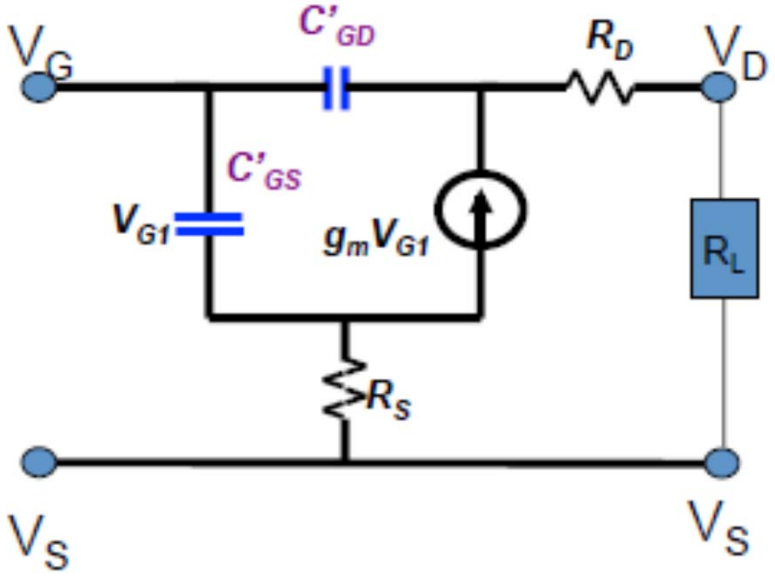
$$\frac{V_D}{I_D} = R_{Ch} + R_{SD} = \frac{L - \Delta L_R}{Z - \Delta Z} \frac{1}{\overline{\mu_n} C_i (V_G - V_T)} + R_{SD}$$

ΔZ is the width reduction due to isolation process



Equivalent circuit of MOSFET (simplified model)

- The MOSFET acts like a voltage controlled current source
- The gate-drain capacitance acts as a feedback path
- The source and drain resistance induce ohmic losses and reduce drain current for a given drain voltage



Neglecting R_S and R_D:

$$\frac{V_{out}}{V_{in}} = \frac{g_m V_G R_L}{V_G} = g_m R_L$$

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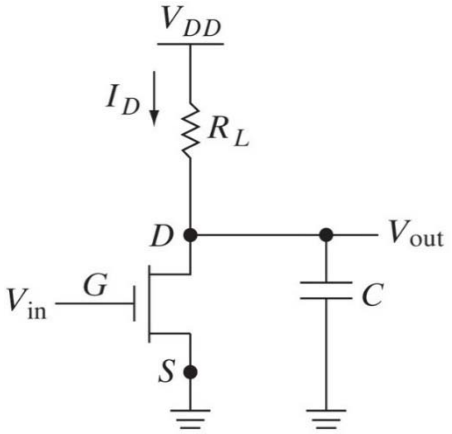
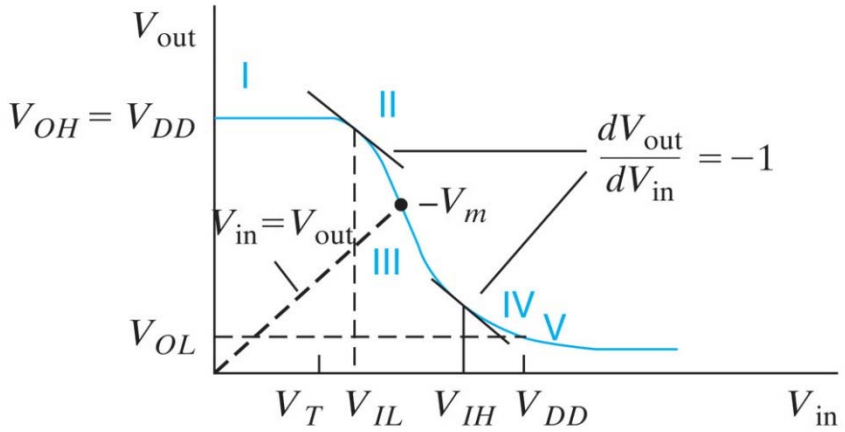
Resistive load-NMOSFET

- Gate voltage low - no current flow, no voltage drop across R_L and V_{out} is high
- Gate voltage high -current flow, large voltage drop across R_L and V_{out} is low
- Voltage Transfer Characteristic (VTC): output voltage as a functior of input bias
  - V_{OH}: logic high level
  - V_{OL}: logic low level
  - V_{IL} and V_{IH}: unity gain points (betwee V_{IL} and V_{IH} the input is amplified)
  - V_m: logic threshold, point where output equals input



(a) Inverter



(c) Voltage transfer characteristic

Resistive load-NMOSFET

- Load line used to create VTC (resistor current equals FET current)

When V_G is high, MOSFET is on:

Linear region

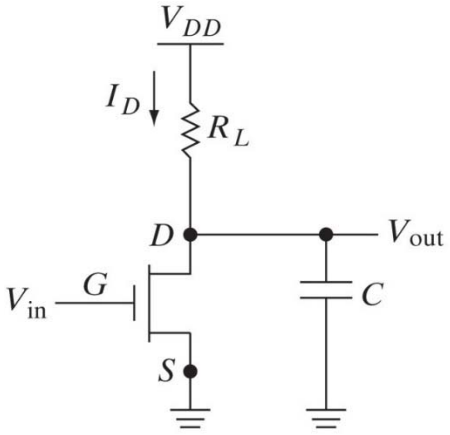
$$I_D = \frac{\overline{\mu_n} Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$

Saturation region:

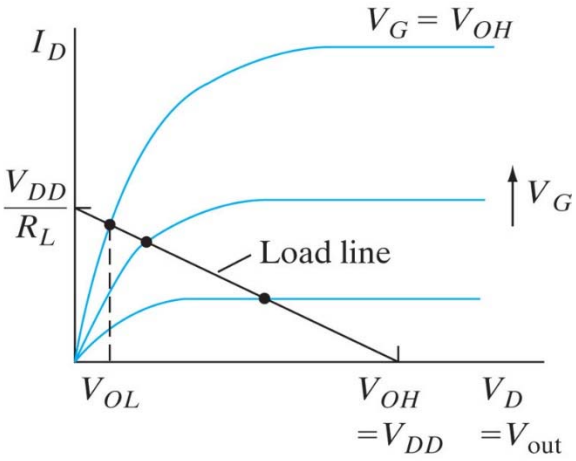
$$I_D(sat.) = \frac{Z}{2L}\overline{\mu_n} C_i (V_G - V_T)^2$$

Resistor current (equal to MOSFET current):

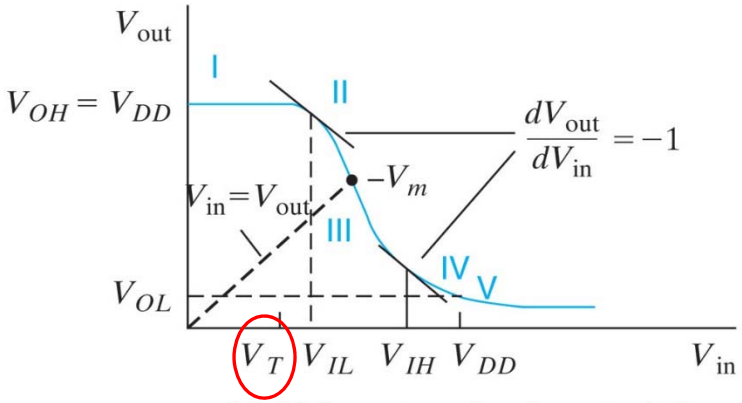
$$I_D = I_L = \frac{V_{DD} - V_{OL}}{R_L}$$



(a) Inverter



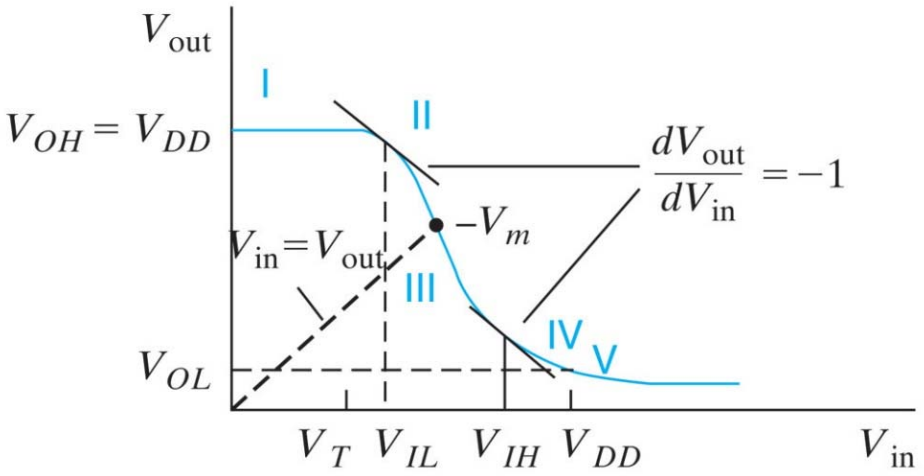
(b) Drain characteristics and load line



(c) Voltage transfer characteristic

Resistive load-NMOSFET inverter

- Ideally:
  - Region III should be as steep as possible (high gain)
  - V_m should be close to $V_{DD}/2$
- Noise immunity (noise margin) how much variation in input voltage can be tolerated while still having correct output logic level
- Problems with resistive inverter:
  - power dissipation in resistor
  - V_{OL} is not zero
- Solution: CMOS



(c) Voltage transfer characteristic

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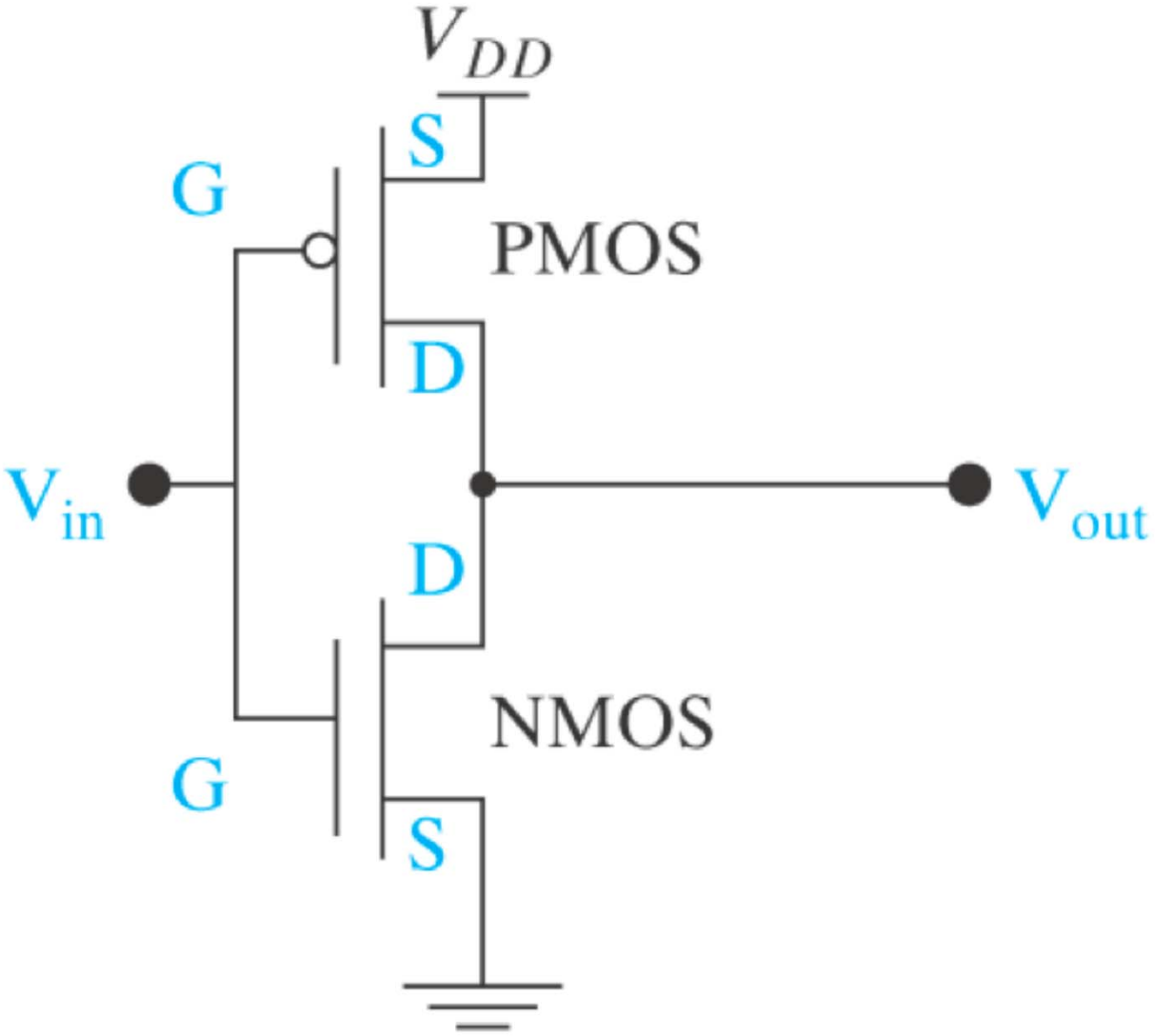
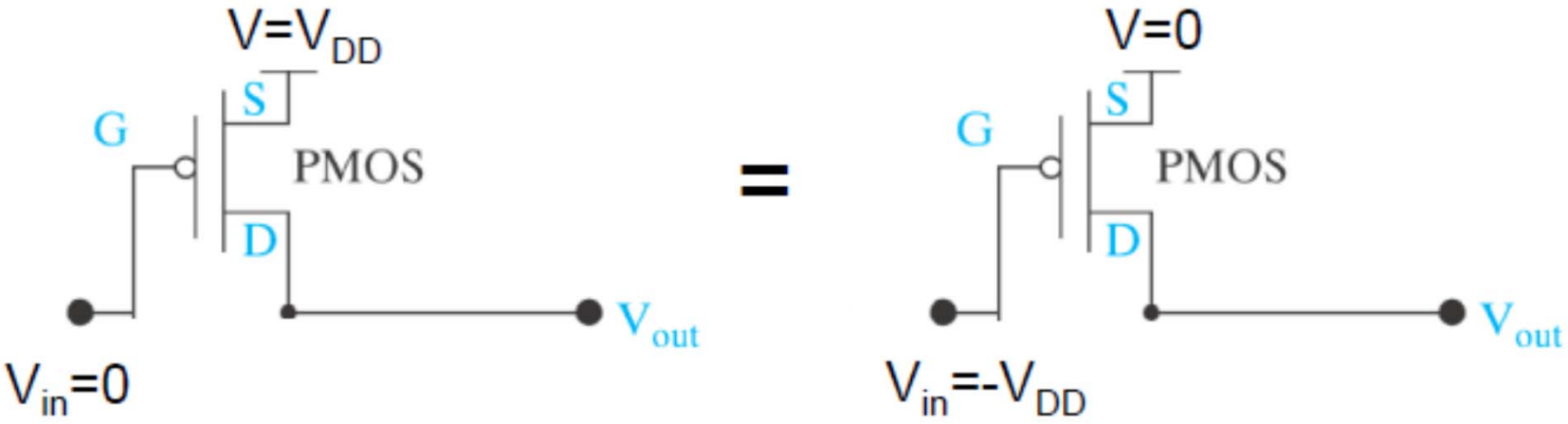
CMOS Inverter

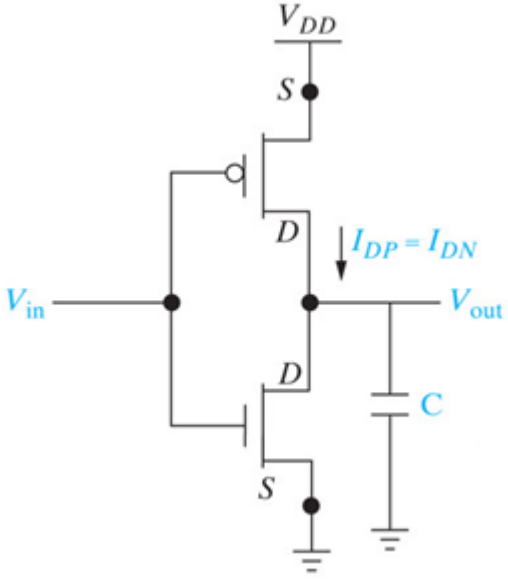


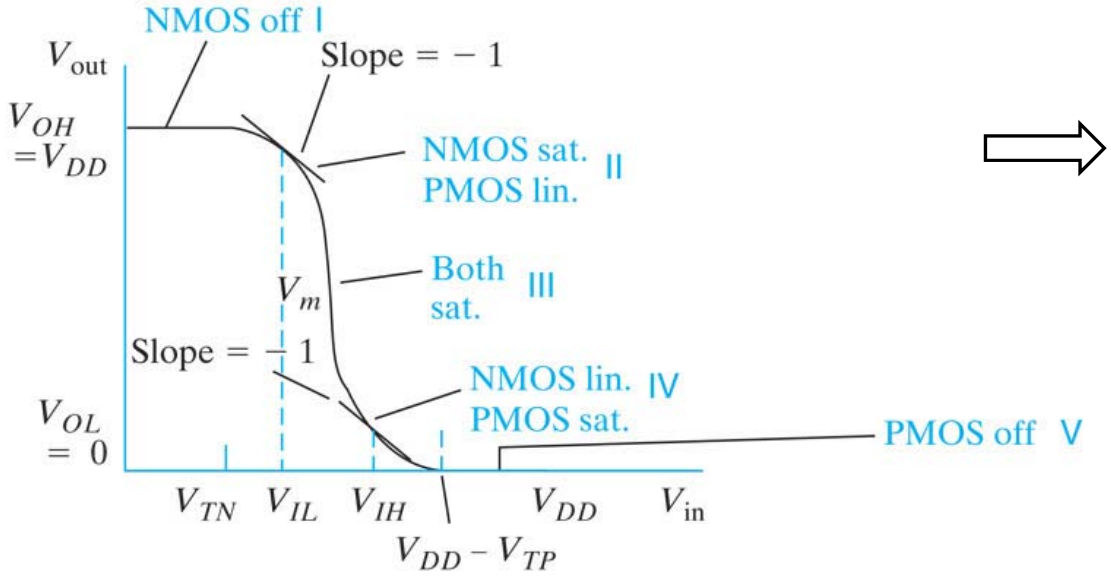
PMOSFET bias comments

From a PMOS channel conductance perspective



CMOS inverter voltage transfer characteristics

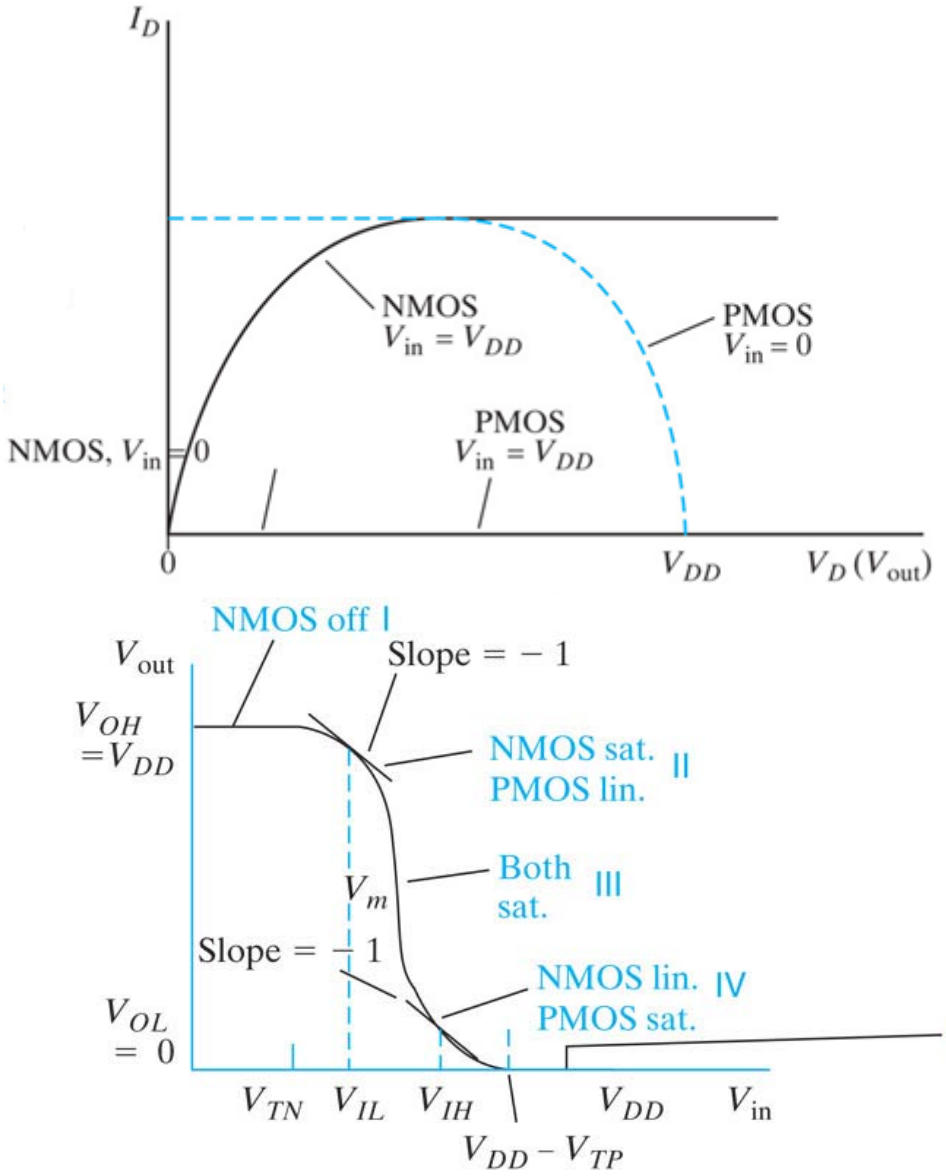




- When V_{in} is low, NMOS is off, PMOS is on →V_{out} is high
- When V_{in} is high, NMOS is on, PMOS is off →V_{out} is low

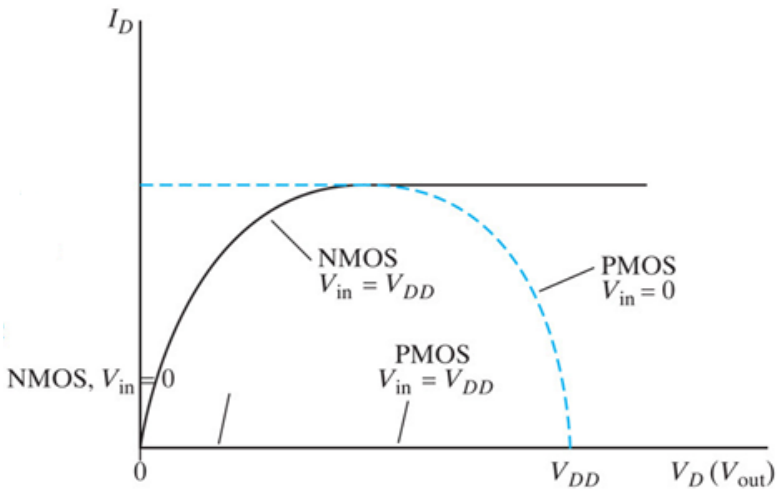
⇨ **Inverter**

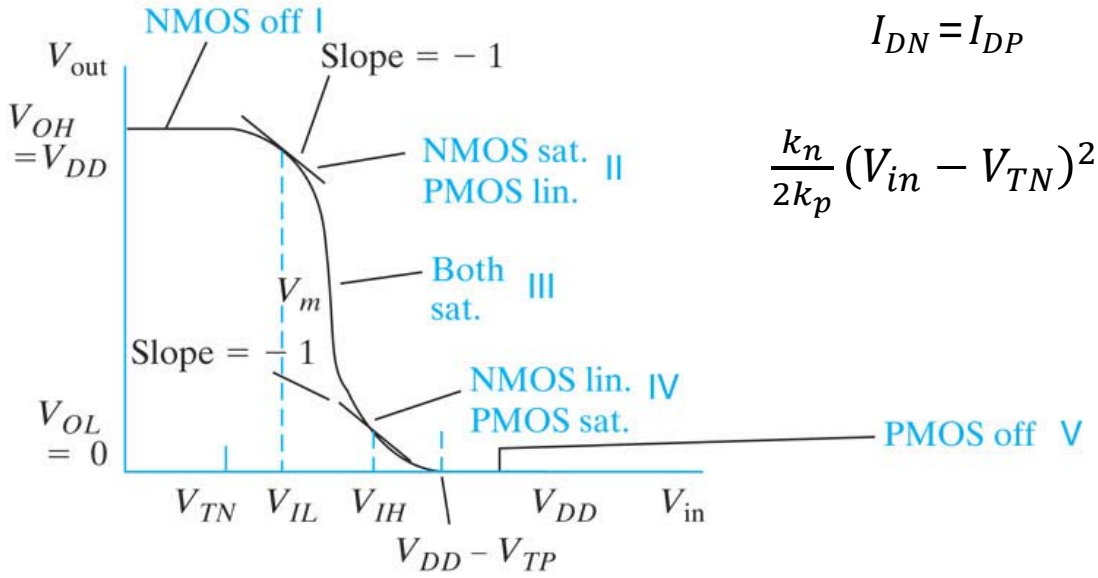
CMOS inverter voltage transfer characteristics



- Overall circuit voltage transfer characteristic determined by solving the set of equations where the NMOS current equal to the PMOS current
- The Id relationship used to determine the operation characteristic is chosen based on whether the FETs are in the linear or saturation operating regions

CMOS inverter voltage transfer characteristics





Region II Current Calculation

NMOSFET Drain Current (Saturation):

$$I_{DN} = \frac{k_n}{2}(V_{in} - V_{TN})^2$$

PMOSFET Drain Current (Linear):

$$I_{DP} = k_p\left[(V_{DD} - V_{in}) + V_{TP} - \frac{(V_{DD} - V_{out})}{2}\right](V_{DD} - V_{out})$$

To determine operation point (VTC):

$I_{DN} = I_{DP}$ So:

$$\frac{k_n}{2k_p}(V_{in} - V_{TN})^2 = \left[\frac{V_{DD}}{2} - V_{in} + V_{TP} + \frac{V_{out}}{2}\right](V_{DD} - V_{out})$$

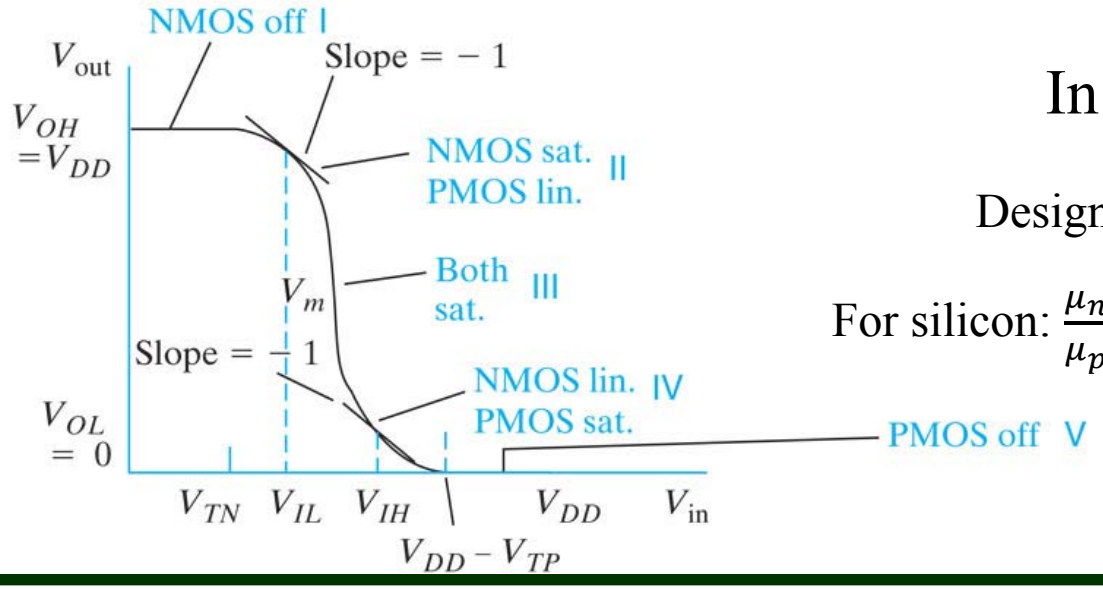
CMOS transition voltage

- VTC transition region V_m occurs at

$$V_{in} = V_{out}$$

$$\Rightarrow V_{in} = (V_{DD} + \chi V_{TN} + V_{TP})/(1+\chi)$$

$$\chi = \sqrt{\frac{k_n}{k_p}} = \sqrt{\frac{\mu_n}{\mu_p}\frac{(Z/L)_n}{(Z/L)_p}}$$



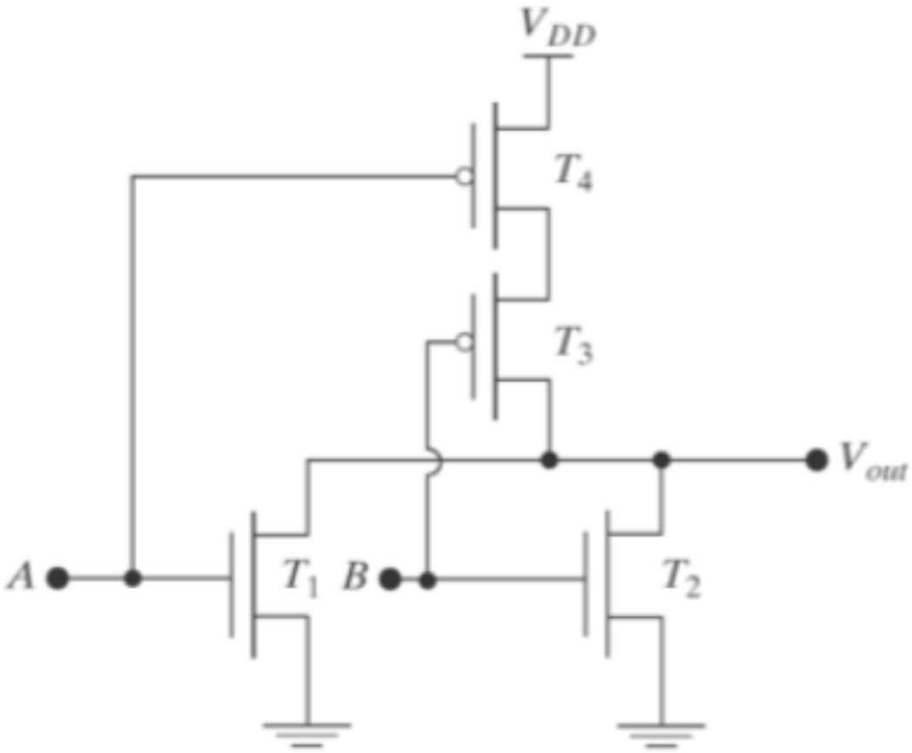
In order to have $V_m \sim \frac{V_{DD}}{2}$

Design device such that V_{TN}=-V_{TP} and χ=1

For silicon: $\frac{\mu_n}{\mu_p} \approx 2$, make device $(Z/L)_p$=2$(Z/L)_n$

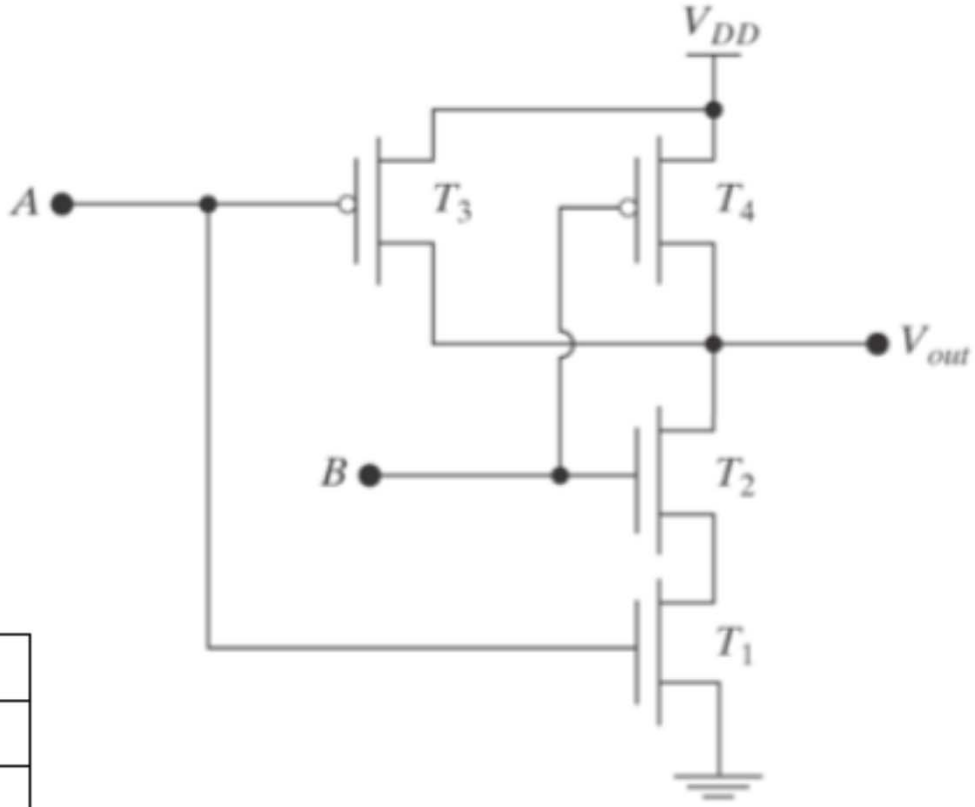
CMOS NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0



PMOS in series (slower)

CMOS NAND



A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

NMOS in series (faster)

Power dissipation

The input capacitance of the inverter is the parallel combination of the NMOSFET and PMOSFET:

$$C_{inv} = C_i\left\{(ZL)_N + (ZL)_P\right\}$$

Multiplying this term by the fan-out gives a total load capacitance of "C"

The energy expended in charging "C" is given by integrating the product of the time-dependent voltage and the time-dependent current:

$$E_C = \int i_p(t)\left[V_{DD} - v(t)\right]dt = V_{DD}\int i_p(t)dt - \int i_p(t)v(t)dt$$

but $i_p(t) = C\dfrac{dv(t)}{dt}$ so:

$$E_C = V_{DD}\int C\frac{dv(t)}{dt}dt - \int Cv(t)\frac{dv(t)}{dt}dt = CV_{DD}\int_0^{V_{DD}} dv - C\int_0^{V_{DD}} v\,dv = CV_{DD}^2 - \frac{1}{2}CV_{DD}^2 = \frac{1}{2}CV_{DD}^2$$

During a discharge cycle:

$$E_d = \int i_n(t)v(t)dt = -\int_{V_{DD}}^{0} Cv\,dv = \frac{1}{2}CV_{DD}^2$$

For a charge/discharge frequency "f":

$$P = CV_{DD}^2 f$$

Switch delay

The propagation delay time t_p is a metric for the switching speed of the gate.

$t_{PHL} \equiv$ the time for the output to transition from V_{OH} to $V_{OH}/2$

$t_{PLH} \equiv$ the time for the output to transition from V_{OL} to $V_{OH}/2$

The time needed to reach $V_{OH}/2$ is found by dividing charge stored in the capacitor by the charge or discharge current. Since the transistor providing the current is in saturation, and $I(sat).=\frac{k}{2}\left(V_{DD}-V_T\right)^2$:

$$t_{PHL}=\frac{\frac{1}{2}CV_{DD}}{I_{DN}}=\frac{\frac{1}{2}CV_{DD}}{\frac{k_N}{2}\left(V_{DD}-V_{TN}\right)^2}$$

$$t_{PLH}=\frac{\frac{1}{2}CV_{DD}}{I_{DP}}=\frac{\frac{1}{2}CV_{DD}}{\frac{k_P}{2}\left(V_{DD}+V_{TP}\right)^2}$$

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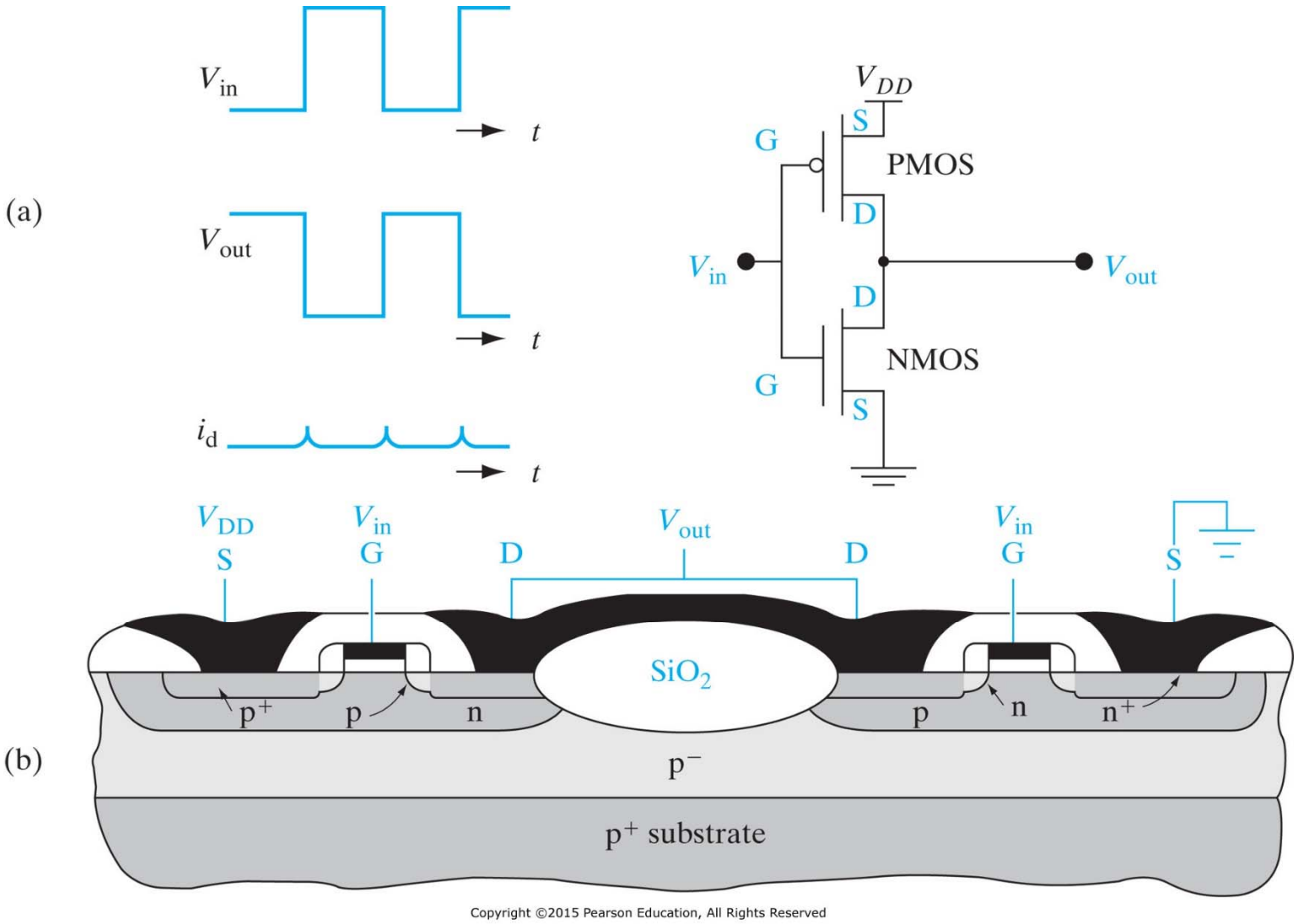
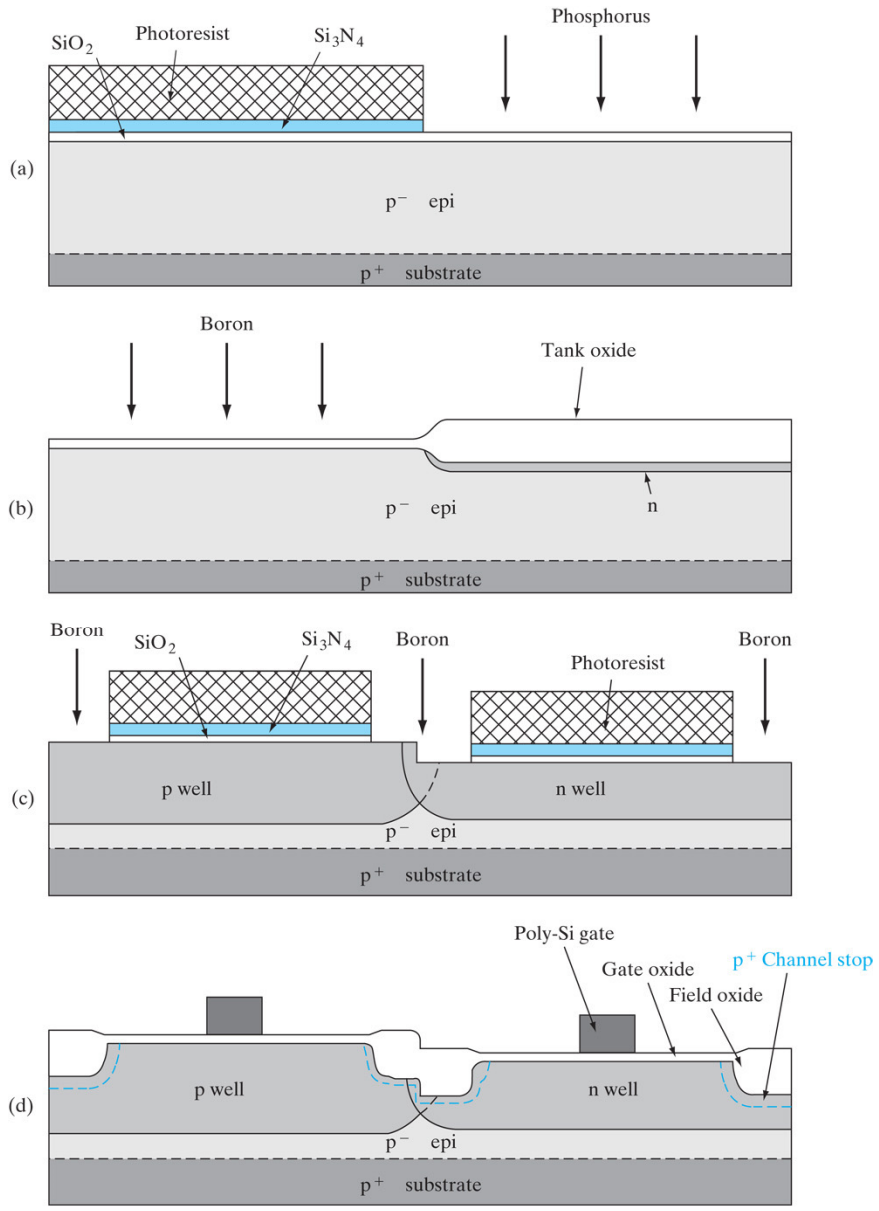
CMOS processing



Self aligned process



NMOS fabrication in p-well