Essentials of MOSFETs

Unit 1: Transistors and Circuits

Lecture 1.4: MOSFET Device Metrics

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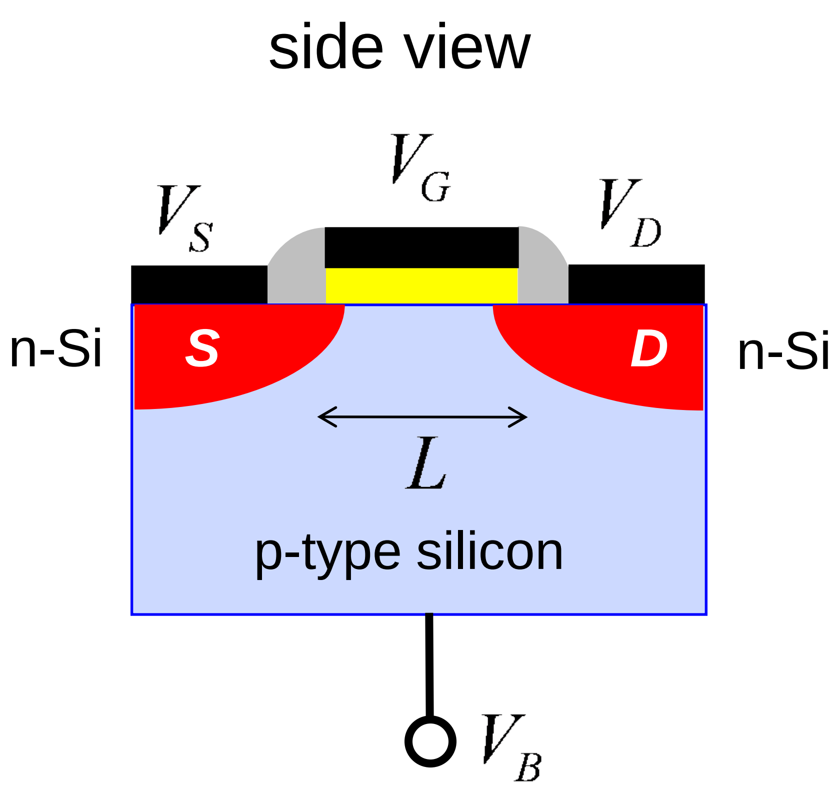
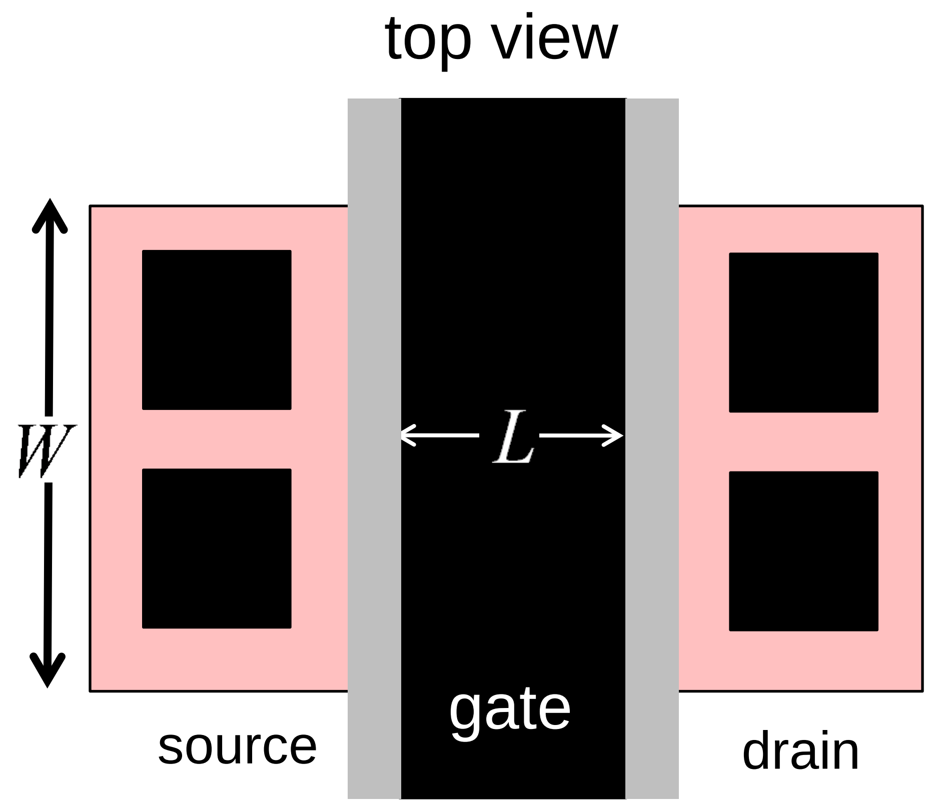
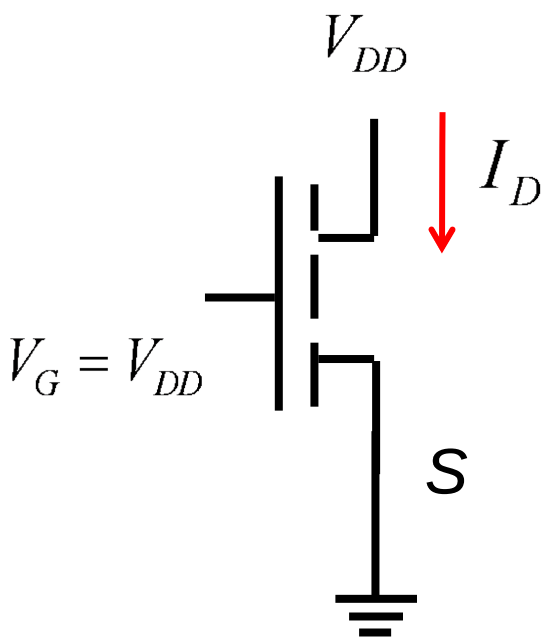
On current scales with MOSFET width

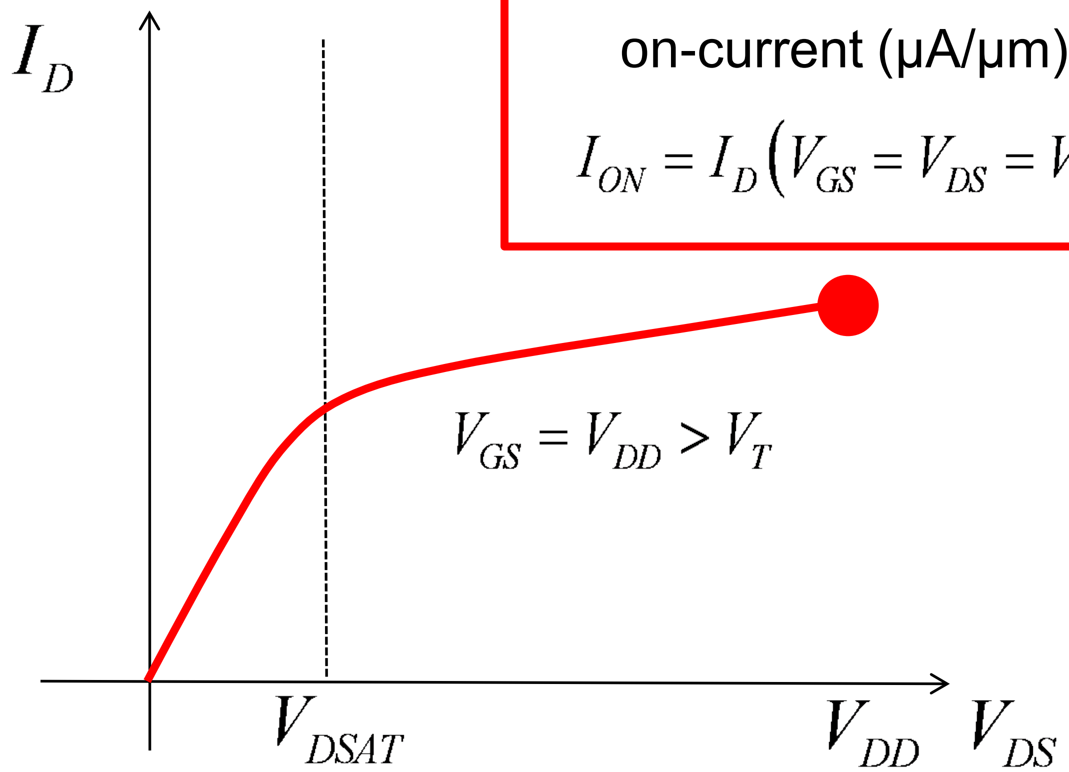




Currents will be quoted in milliamps per micrometer of width (or microamps per micrometer).

1) On-current





on-current (μA/μm)

$$I_{ON} = I_D\left(V_{GS} = V_{DS} = V_{DD}\right)$$

output characteristic:
I_D vs. V_{DS} at fixed V_{GS}

The on-current metric

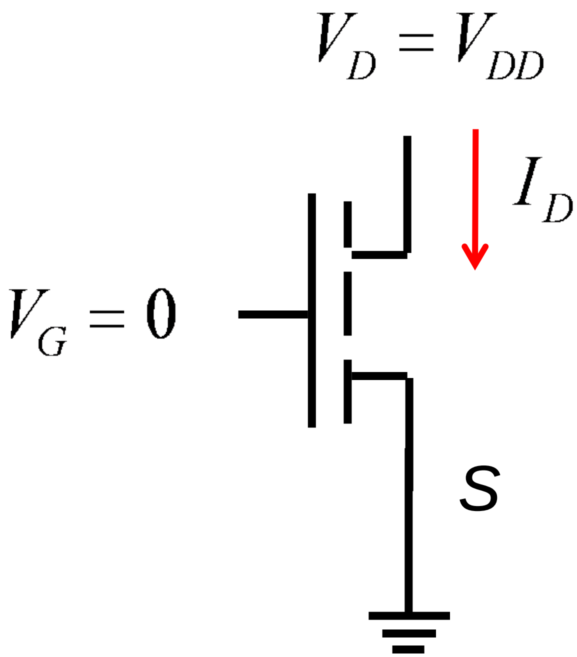
$$\boxed{I_{ON} = I_D\left(V_{GS} = V_{DS} = V_{DD}\right)}$$

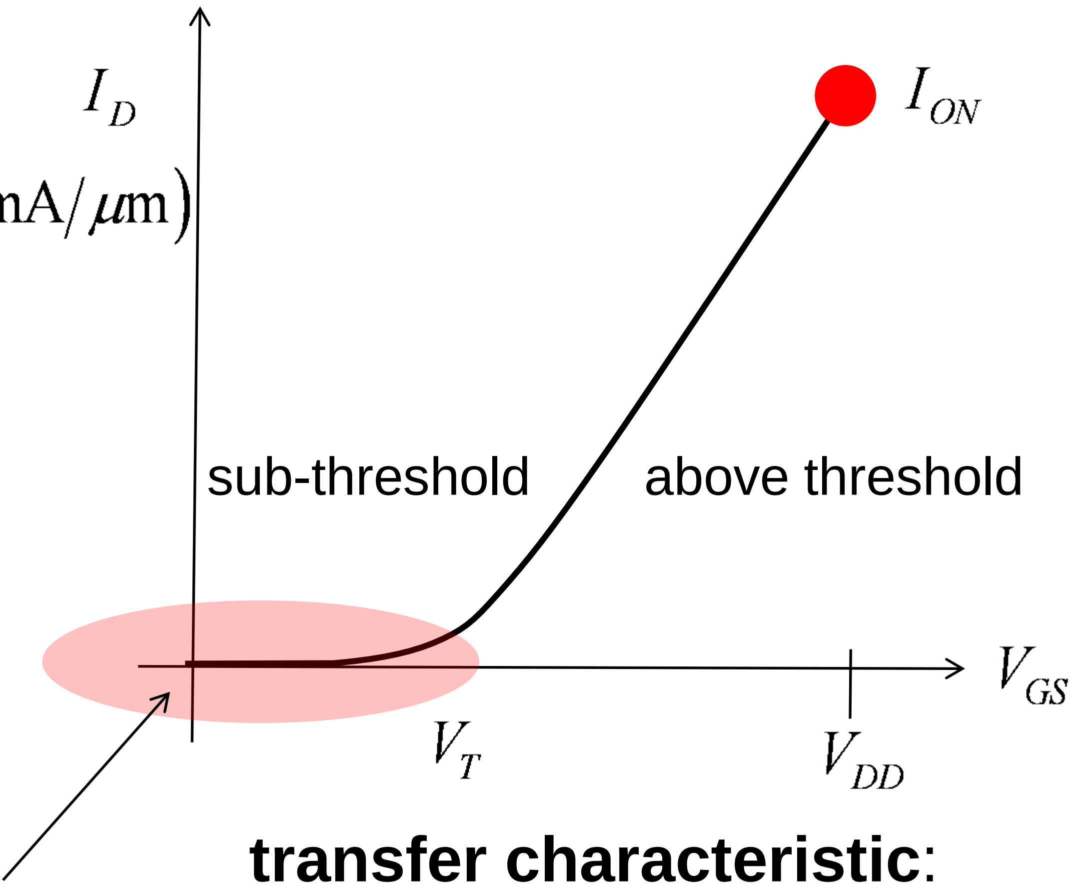
On current is an important device metric for digital electronics because it determines the maximum speed of the circuit.

$$\boxed{\tau_{cir} \propto \frac{C_{sw} V_{DD}}{I_{ON}}}$$

circuit speed

2) Off-current



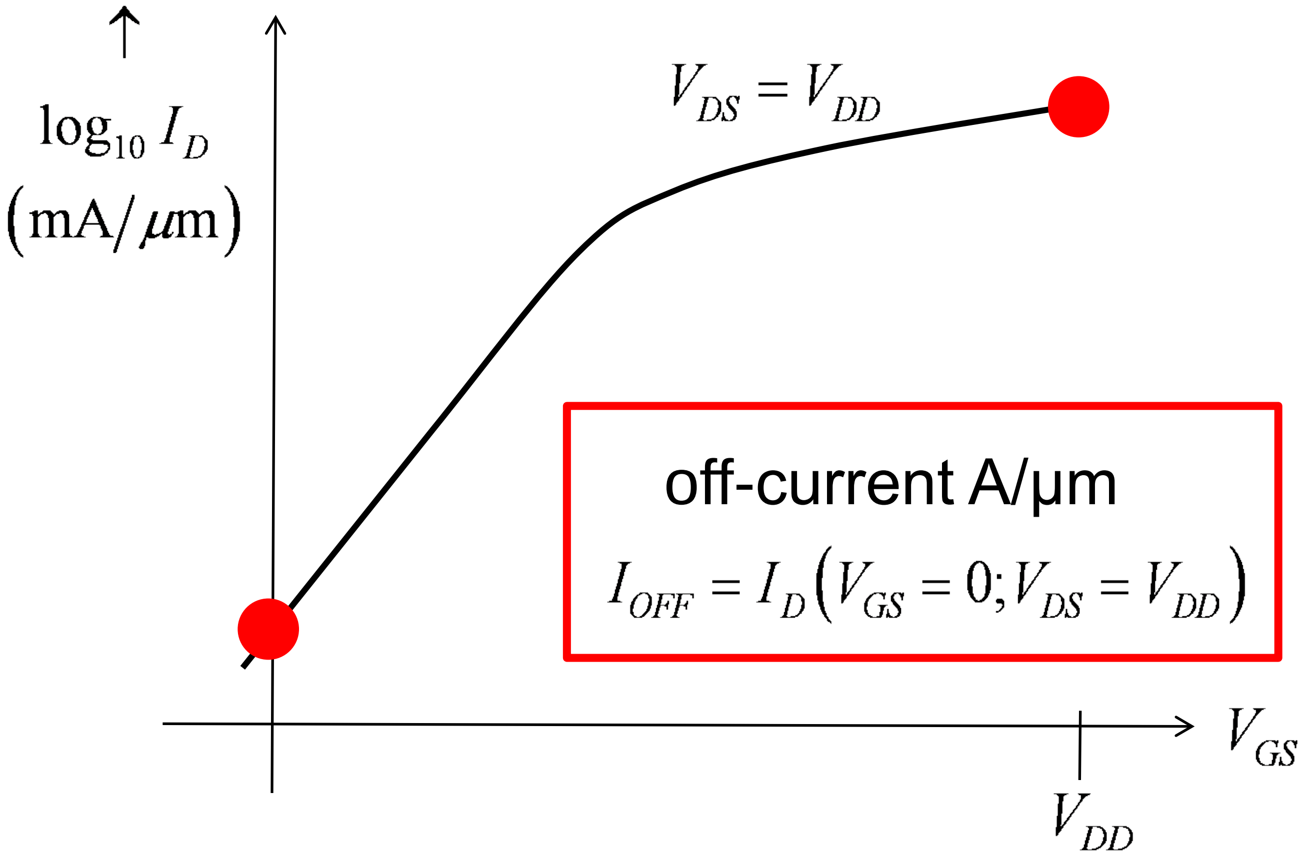


off-current

transfer characteristic:
I_D vs. V_{GS} at fixed V_{DS}

Off-current

transfer characteristic on a semi-log plot:



The off-current metric

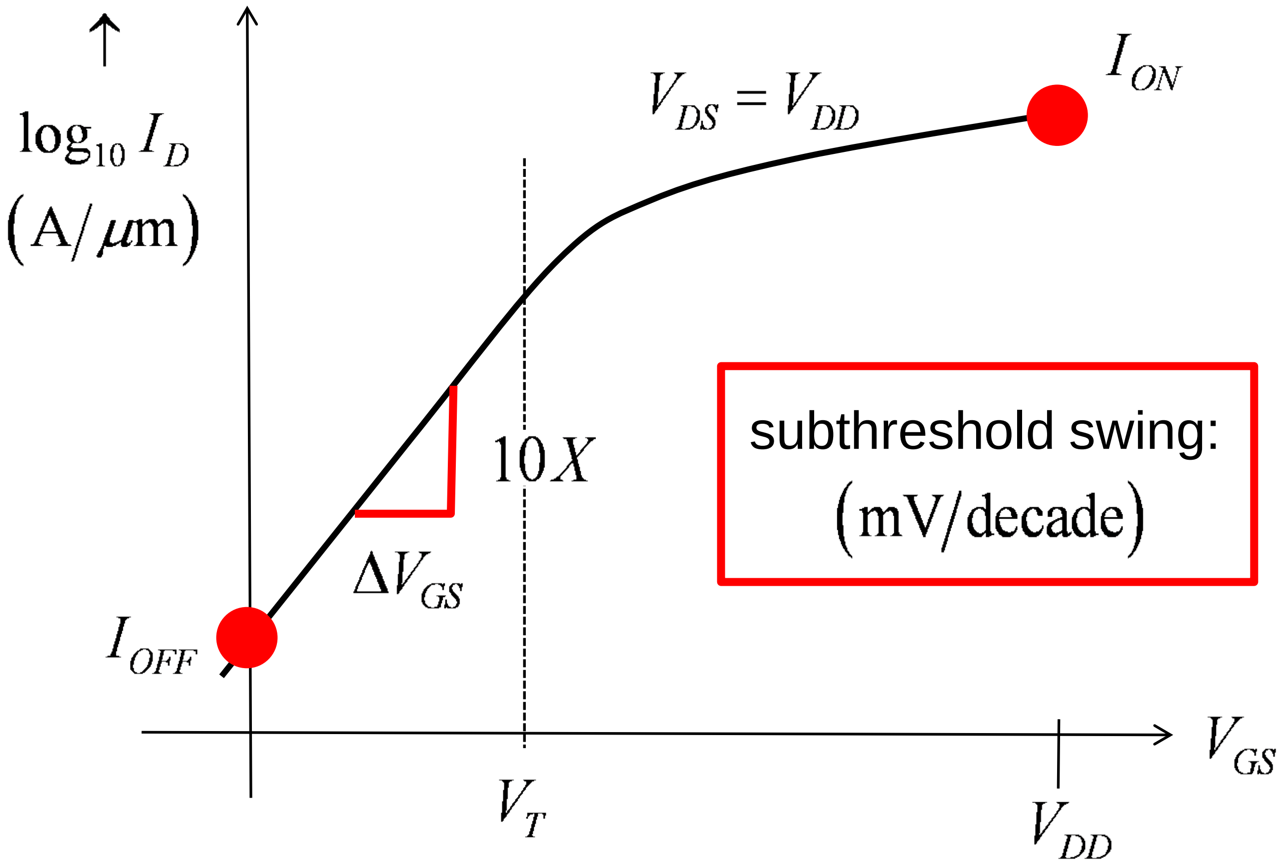
$$\boxed{I_{OFF} = I_D\left(V_{GS} = 0; V_{DS} = V_{DD}\right)}$$

Off-current is an important device metric for static power.

$$\boxed{P_{static} = N_G I_{OFF} V_{DD}}$$

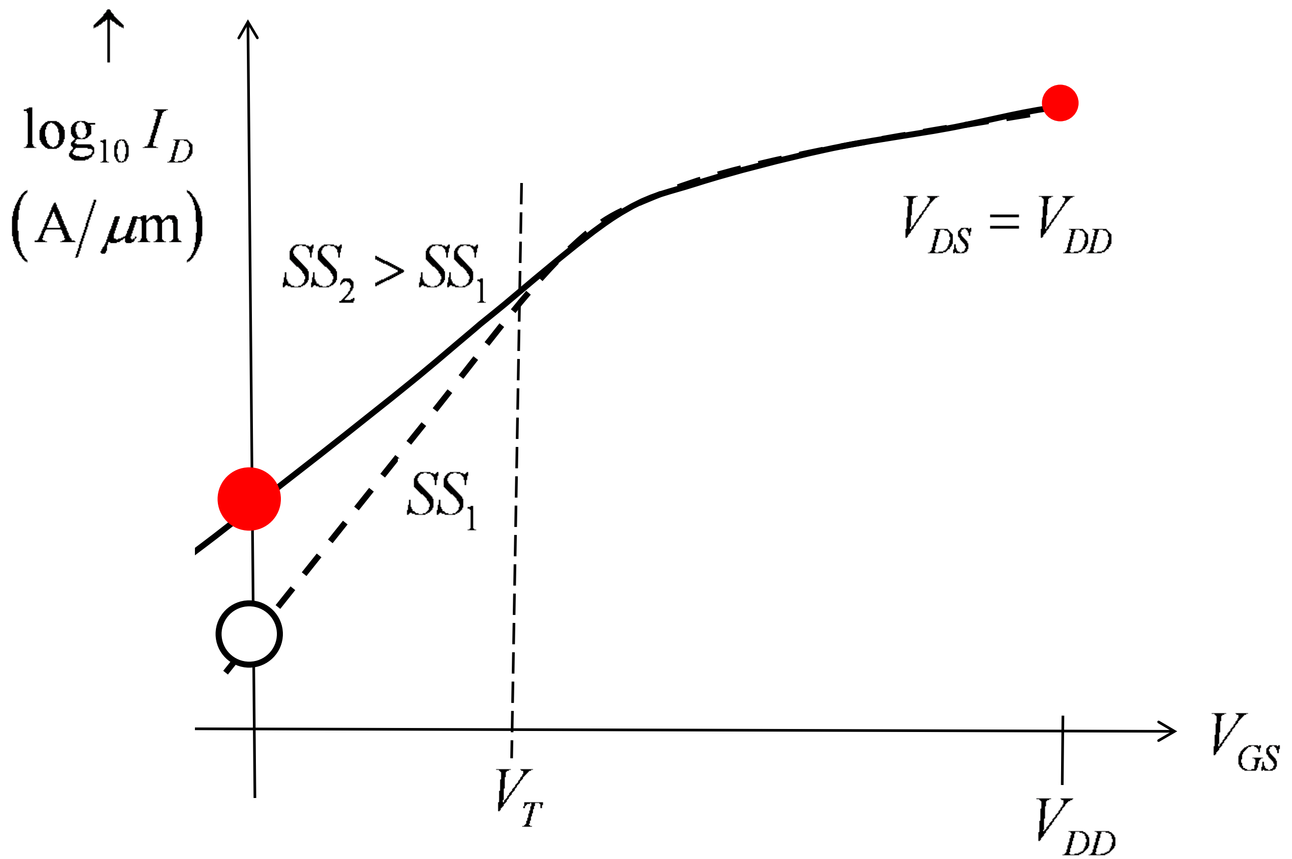
3) Subthreshold Swing

transfer characteristics:



Higher SS increases off-current (exponentially)

transfer characteristics:



SS, V_{DD}, and Power

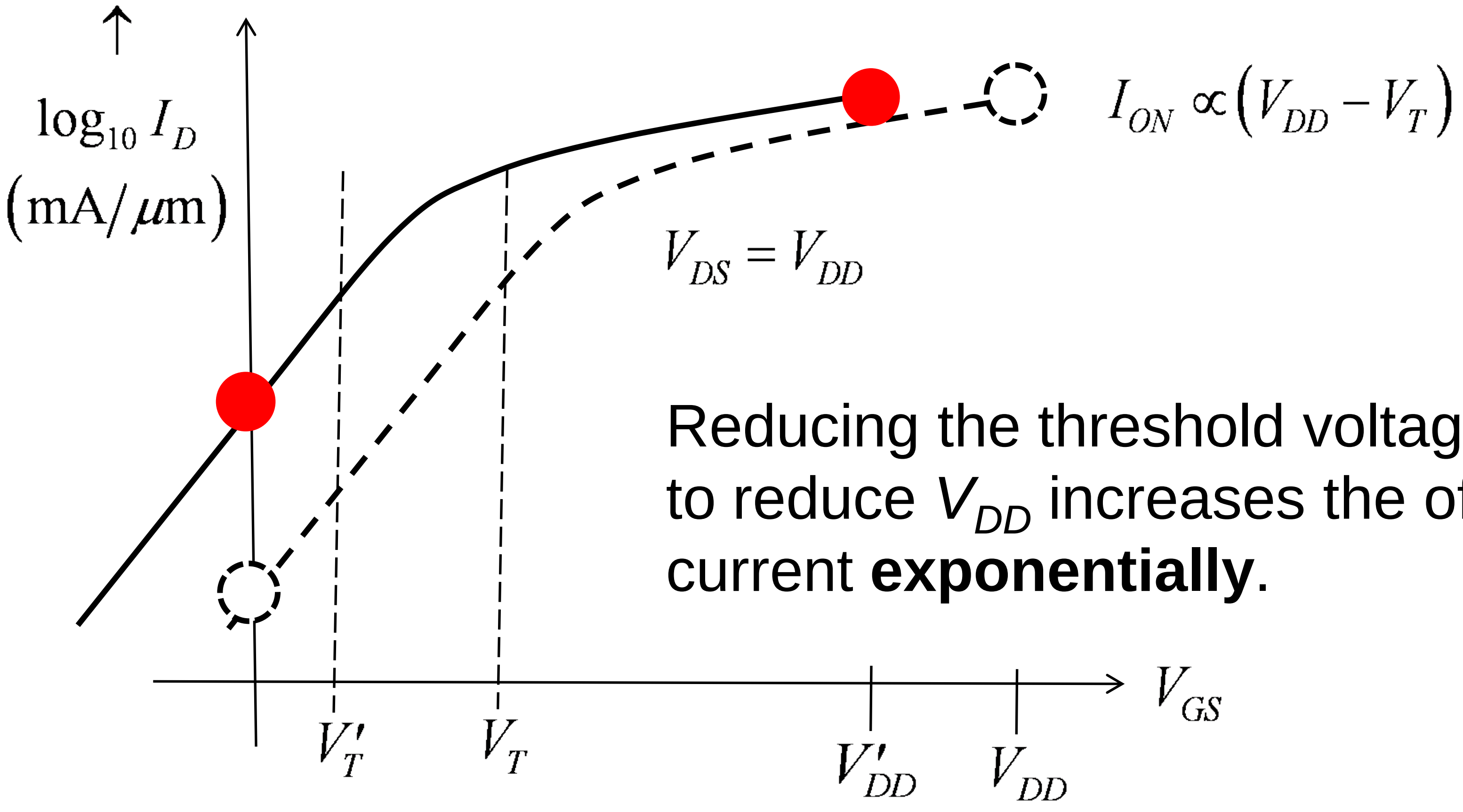
$$P_{static} = N_G I_{OFF} V_{DD}$$

$$P_{dynamic} = \alpha f C_{sw} V_{DD}^2$$

- Static power is controlled by the off-current.
- The SS determines the off-current
- To minimize dynamic power dissipation at a given frequency, we should use the lowest power supply voltage possible.
- The SS determines the minimum power supply.

Reducing V_T increases off-current (exponentially)

transfer characteristics:



Reducing the threshold voltage to reduce V_{DD} increases the off current **exponentially**.

The SS metric

$$SS = \left(\frac{\partial \left(\log_{10} I_D \right)}{\partial V_{GS}} \right)^{-1} = \frac{\mathrm{mV}}{\mathrm{decade}}$$

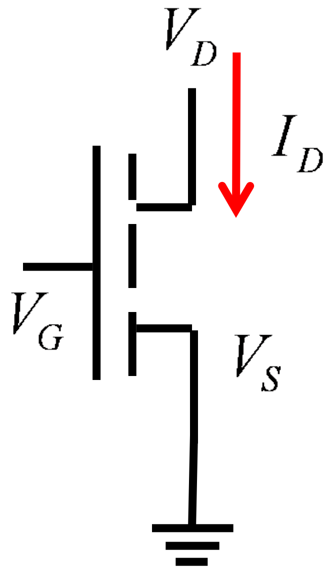
The number of mV that the gate voltage must increase to increase the drain current by a factor of 10.

SS must be minimized to minimize off-current.

SS must be minimized to minimize V_{DD}.

In a MOSFET, SS > 60 mV/decade at T = 300 K

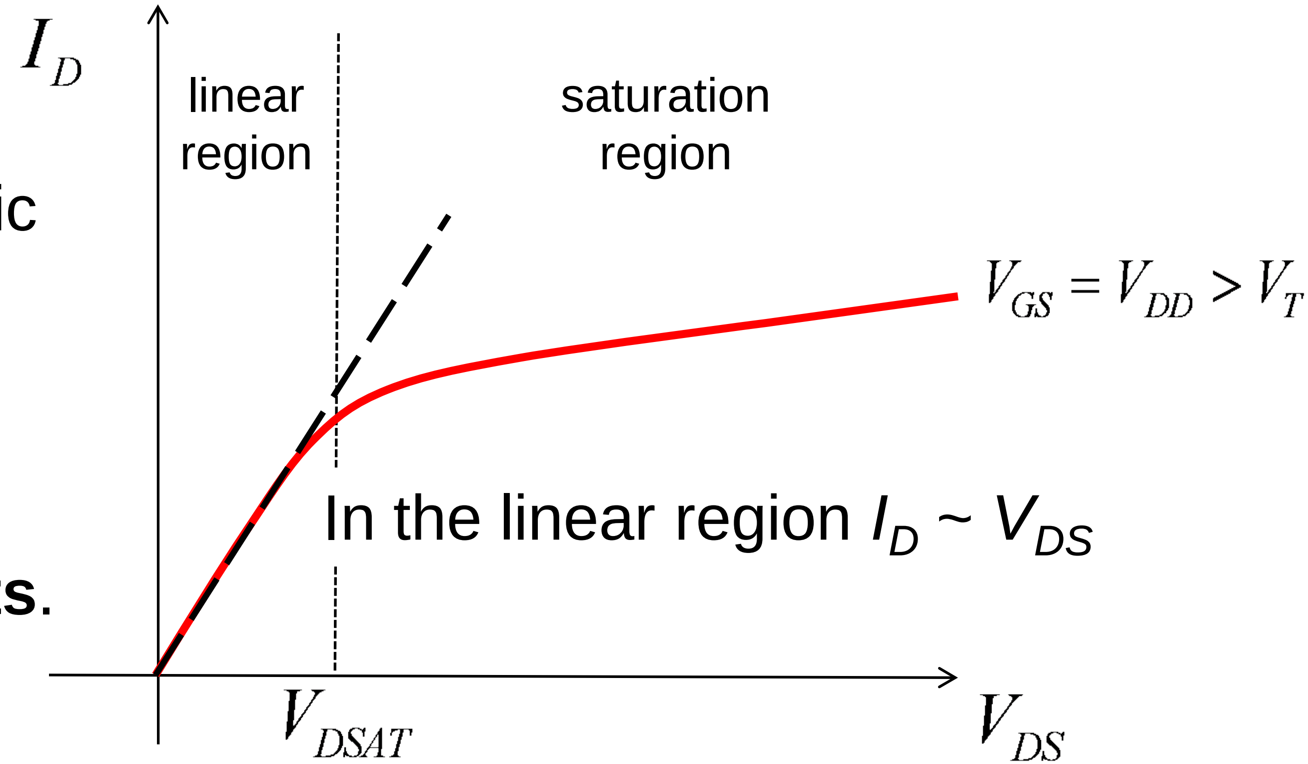
Effect of the drain voltage



Question: How does the drain voltage affect I_D?

Answer: In several different ways that are related to the same underlying physics.

Linear region



This is an intrinsic effect present in ideal and real MOSFETs, but there are other **non-ideal effects**.

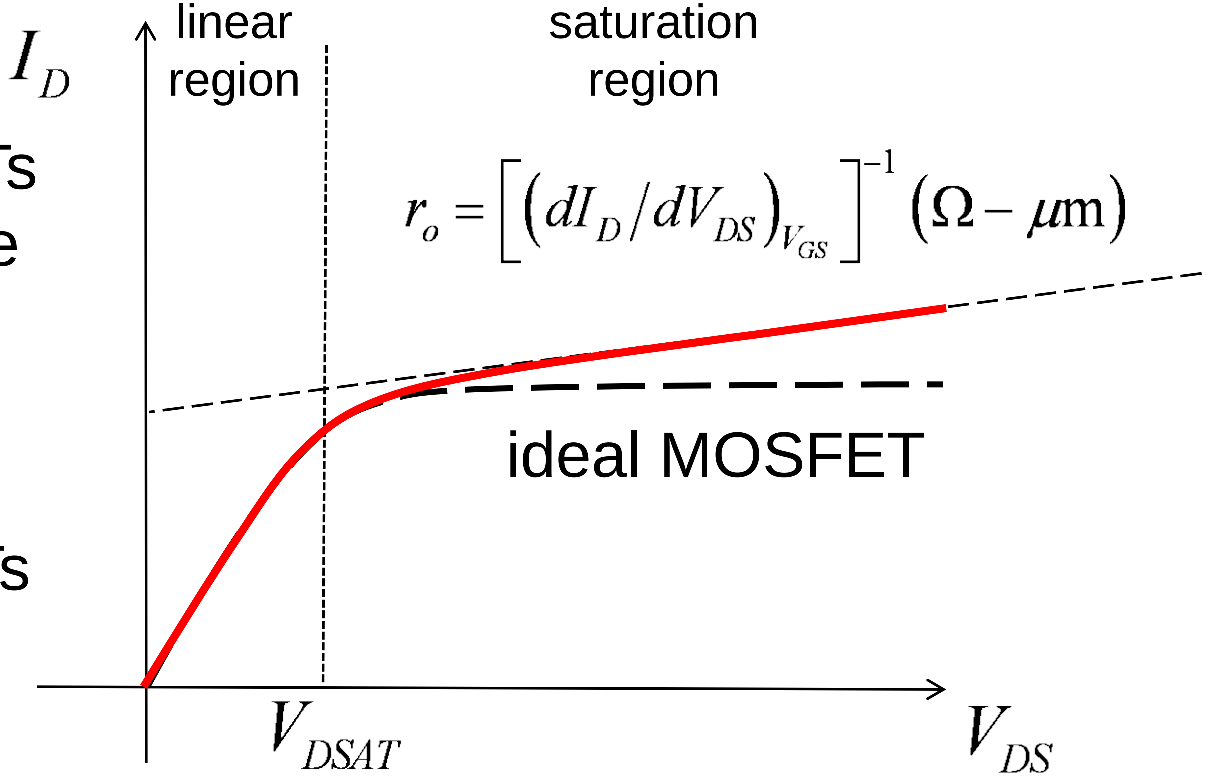
In the linear region $I_D \sim V_{DS}$

output characteristic:
I_D vs. V_{DS} at fixed V_{GS}

Effect of V_{DS} in the saturation region

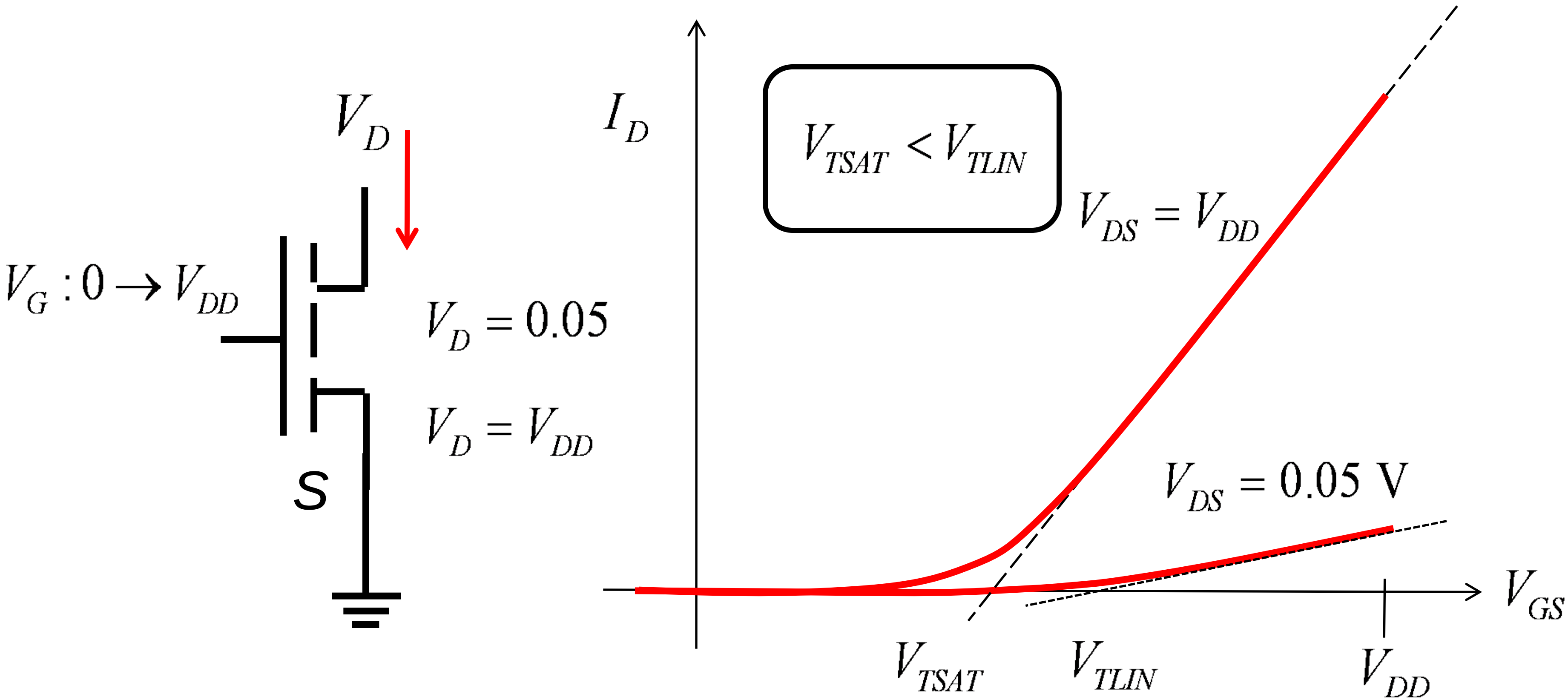
Ideal MOSFETs have an infinite output resistance.

Real MOSFETs have a finite output resistance.



output characteristic:
I_D vs. V_{DS} at fixed V_{GS}

Effect of V_{DS} on transfer characteristic

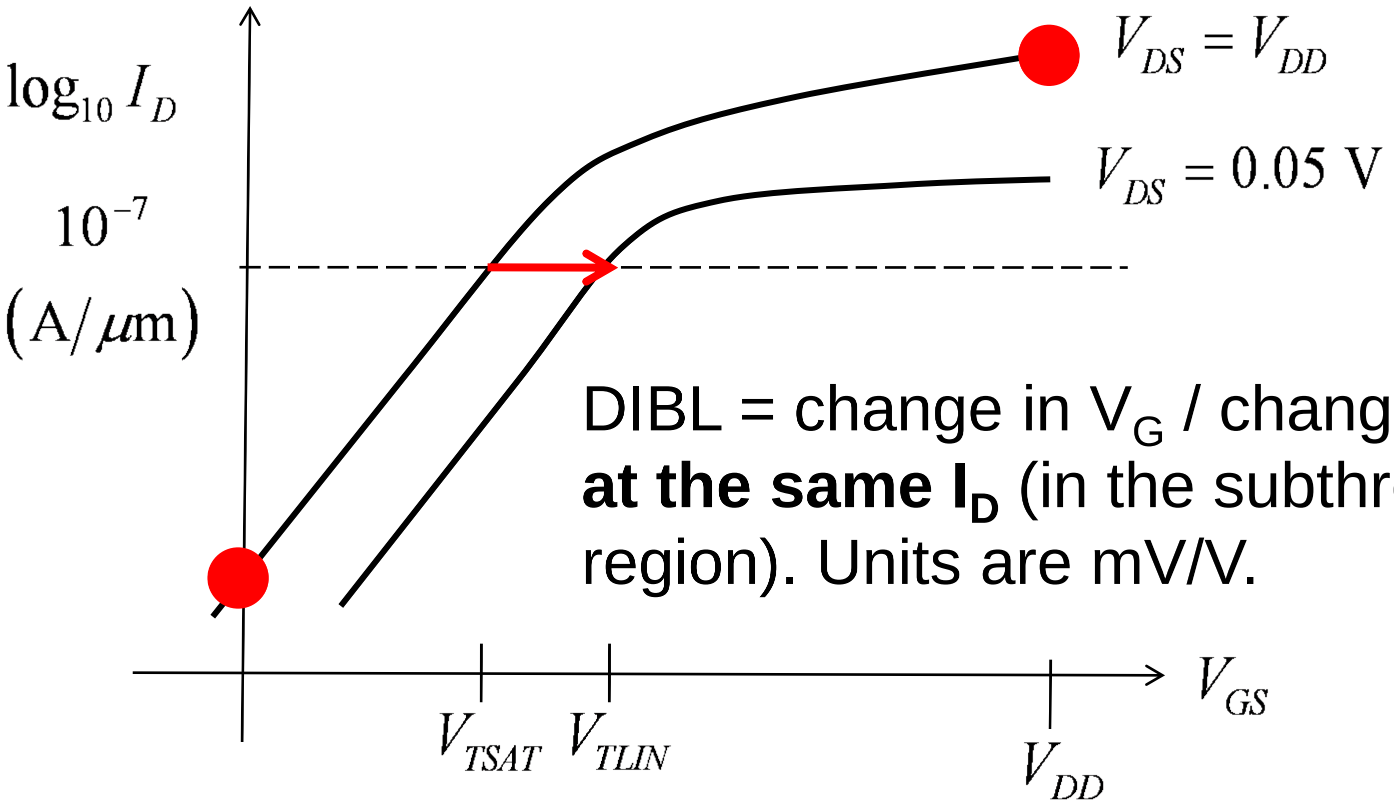


threshold voltage
in saturation region

threshold voltage
in linear region

Effect of V_{DS} in subthreshold

transfer characteristics:



DIBL = change in V_G / change in V_D **at the same I_D** (in the subthreshold region). Units are mV/V.

Drain voltage non-idealities

All of these non-ideal effects:

-threshold voltage dependence on V_{DS}
-non-infinite output resistance
-DIBL

Are due to the same physics. A single metric is used to asses the magnitude of all these effects.

DIBL: **D**rain **I**nduced **Barrier** **L**owering

4) The DIBL metric

$$DIBL = \left.\frac{\partial V_{GS}}{\partial V_{DS}}\right|_{I_D} = \frac{\mathrm{mV}}{\mathrm{V}}$$

DIBL = change in V_G / change in V_D **at the same $\mathbf{I_D}$** (in the subthreshold region). Units are mV/V.

The higher the DIBL, the more sensitive the threshold voltage is to the drain voltage (and the lower the output resistance).

Key Figures of Merit for digital applications

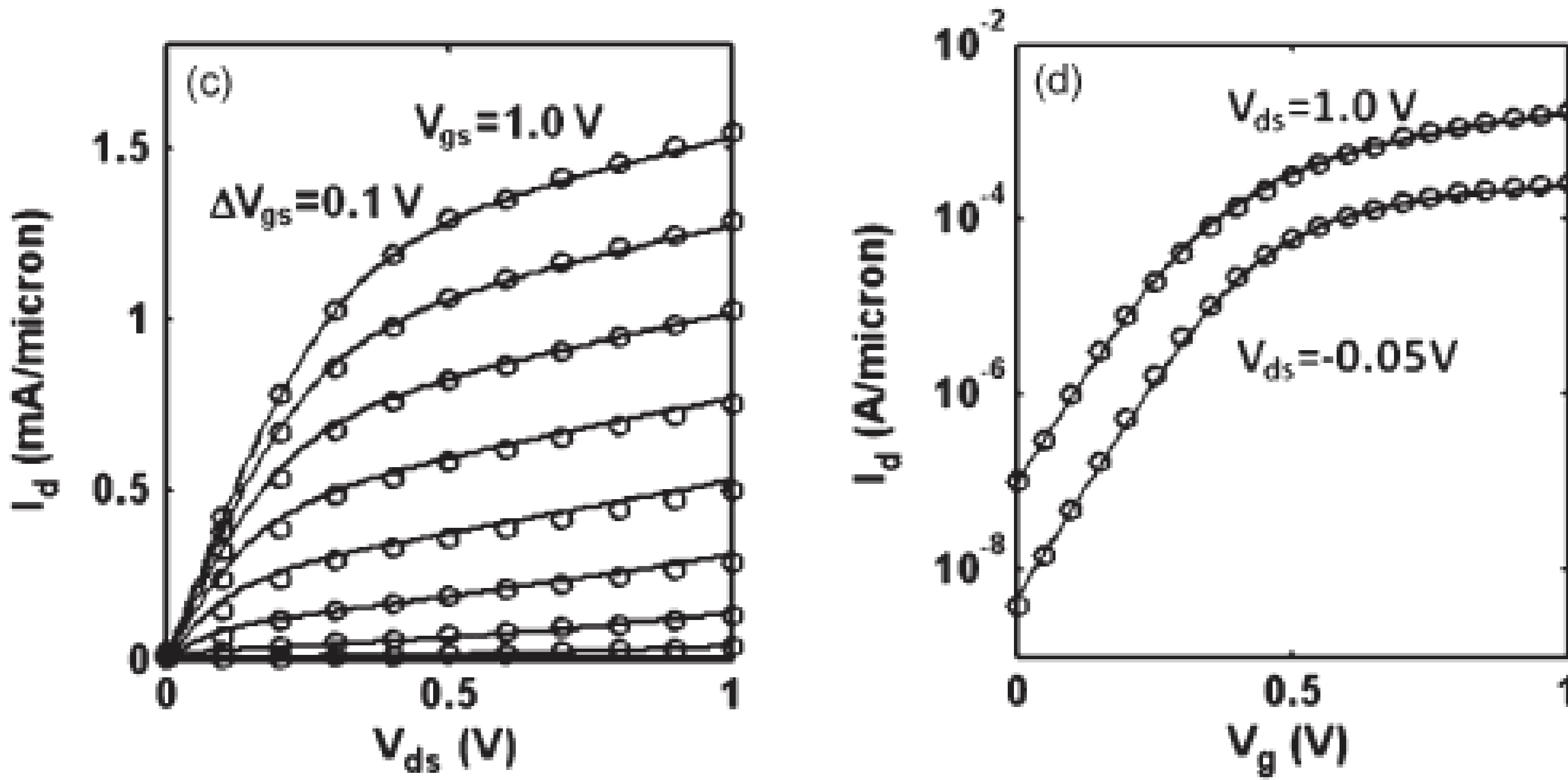
1) On current

2) Off-current

3) Subthreshold swing

4) DIBL

Example: 32 nm N-MOS technology



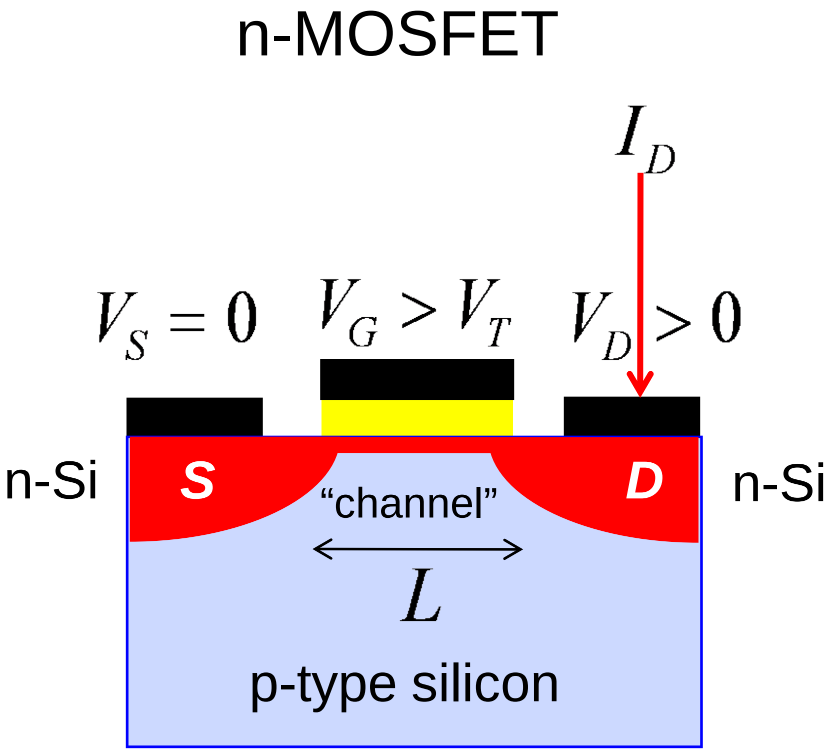
$$I_{ON} \approx 1.55\ \mu\text{A}/\mu\text{m}$$

$$I_{OFF} \approx 10^{-7}\ \text{A}/\mu\text{m}$$

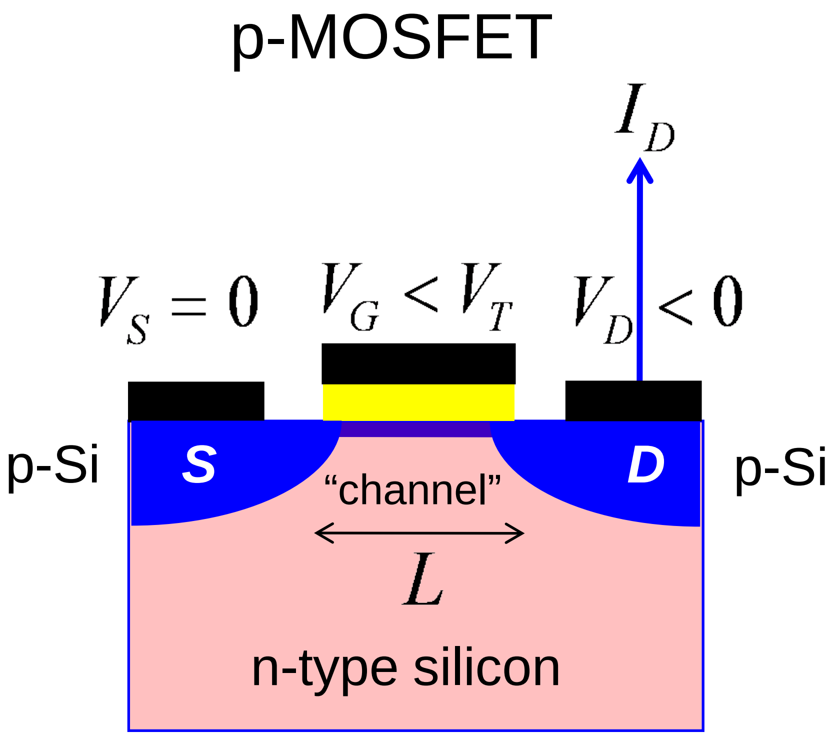
$$SS \approx 105\ \text{mV/decade}$$

$$DIBL \approx 160\ \text{mV/V}$$

N-channel vs. P-channel MOSFET

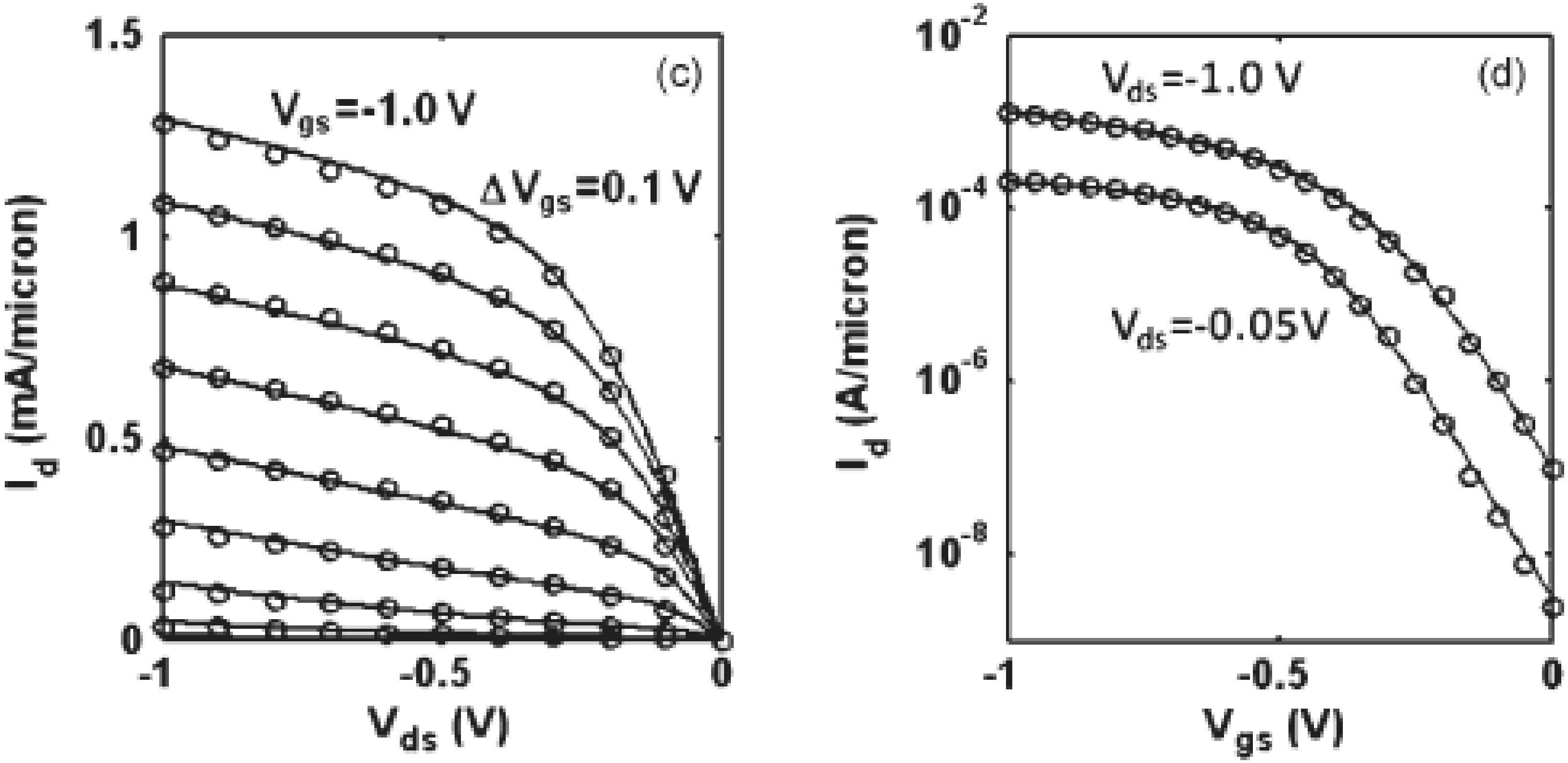


side view

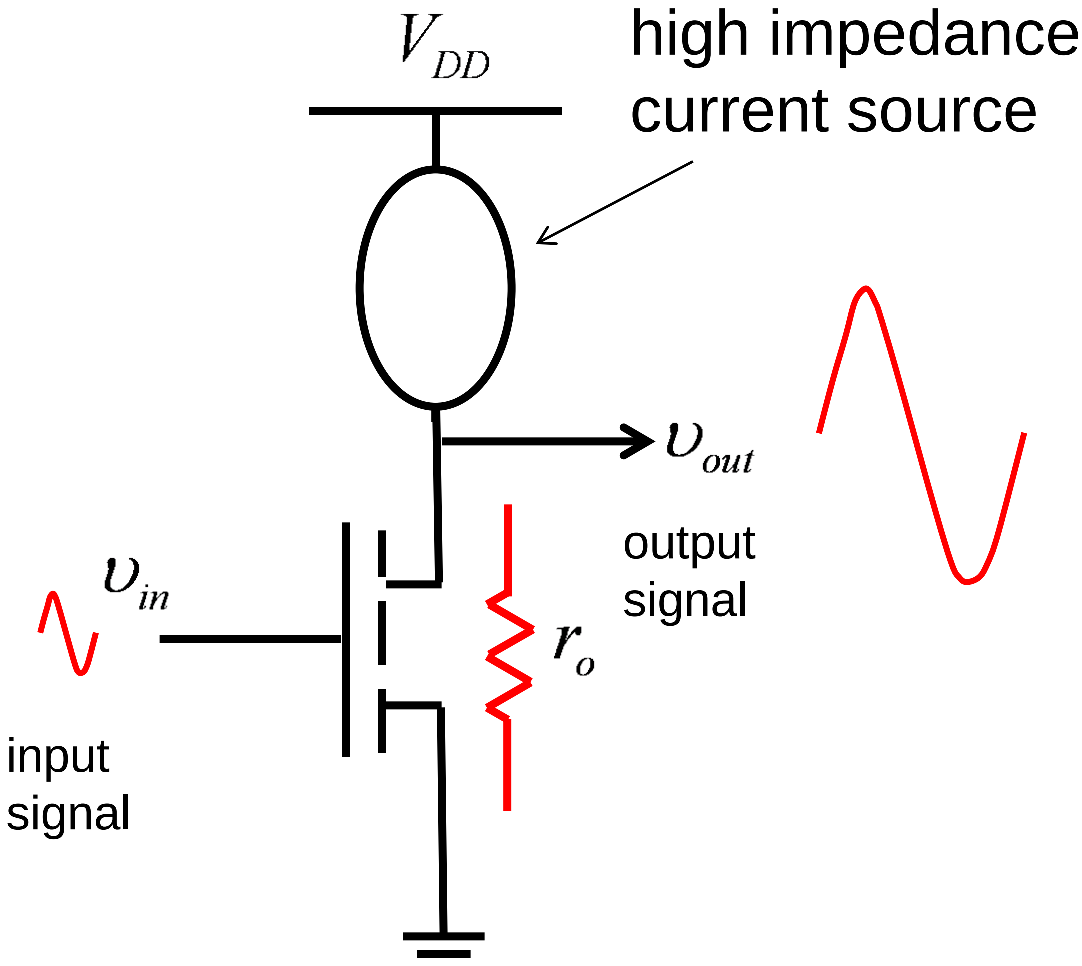


side view

Example: 32 nm P-MOS technology



Analog device metrics



$$\boxed{A_v(\max) = -g_m r_o}$$

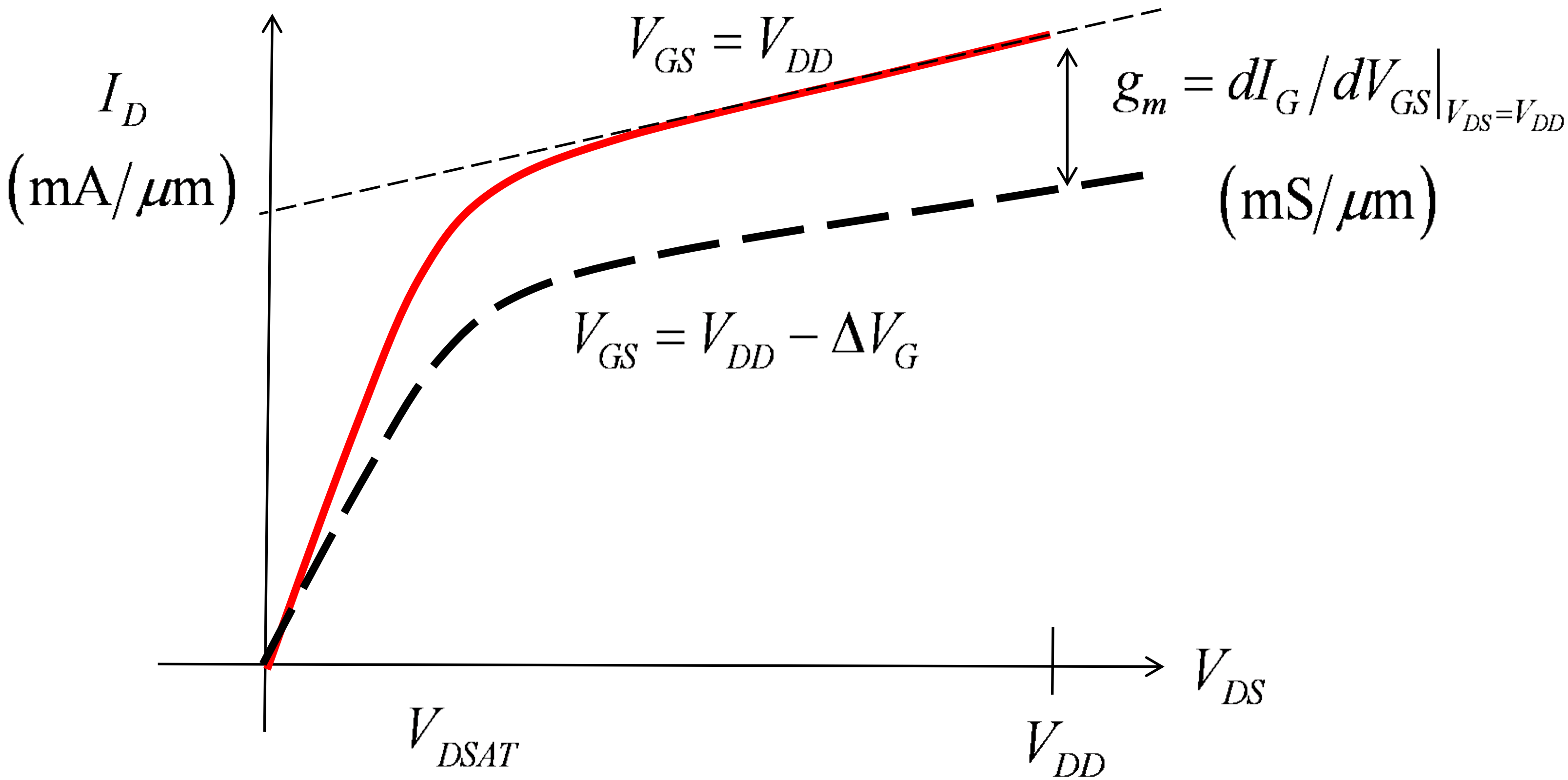
g_m and r_0 are important analog device metrics

(also f_T, f_{max}, linearity, noise, mismatch, etc.)

Lundstrom: 2018

Analog device metrics

$$r_o = \left[\left(dI_D / dV_{DS} \right)_{V_{GS}=V_{DD}} \right]^{-1} \Omega - \mu\text{m}$$



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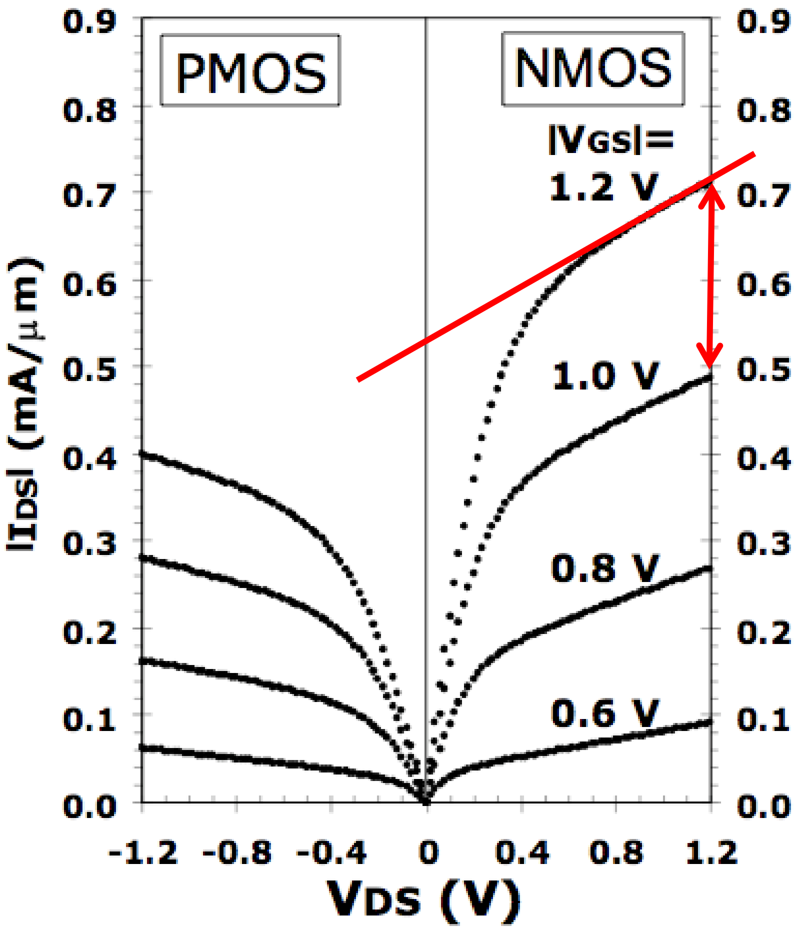
Self-gain for 65 nm technology



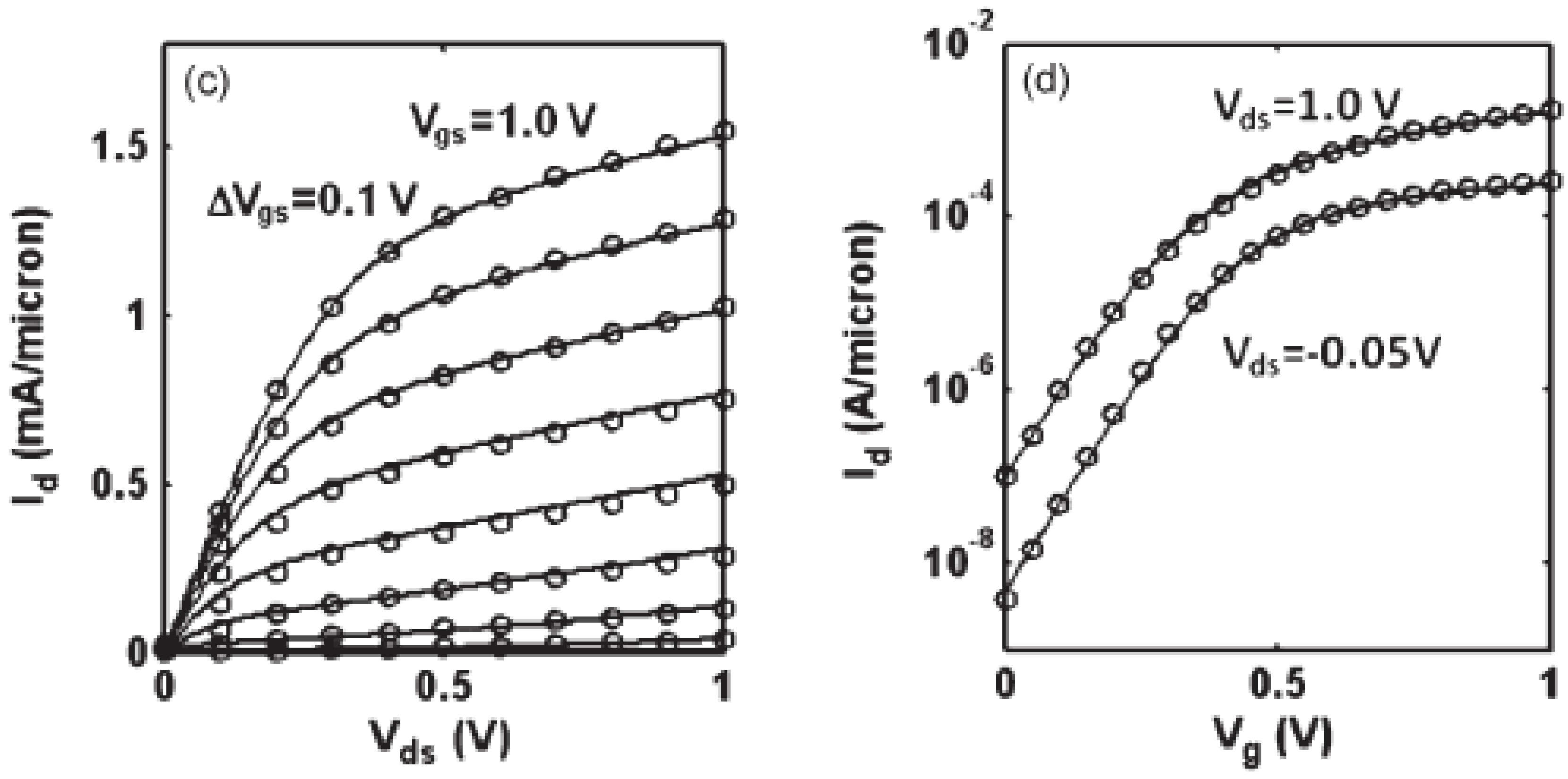
$$g_m \approx \frac{0.2 \text{ mA}/\mu\text{m}}{0.2 \text{ V}} = 1 \text{ mS}/\mu\text{m}$$

$$r_o \approx \frac{1.2 \text{ V}}{0.18 \text{ mA}/\mu\text{m}} \approx 7 \text{ k}\Omega\text{-}\mu\text{m}$$

$$\left|A_\upsilon(\max)\right| = g_m r_o \approx 7$$

C.-H. Jan. et al., 2005 IEDM

32 nm N-MOS technology



$g_m = 2.5\ \text{mS}/\mu\text{m}$ $\qquad r_0 \approx 2.2\ \text{k}\Omega - \mu\text{m}$ $\qquad \left|A_\upsilon(\max)\right| = g_m r_o \approx 5.5$

Recap

Given the measured characteristics of a MOSFET, you should be able to determine:

1. on-current: I_{ON}
2. off-current: I_{OFF}
3. subthreshold swing, SS
4. drain induced barrier lowering: DIBL

5. output resistance: r_o
6. *transconductance:* g_m

threshold voltage: V_T (lin) and V_T (sat)
drain saturation voltage: V_{DSAT}

Our goal in this course is to understand these device metrics and parameters.

Summary

Key device metrics for digital applications are on-current, off-current, SS, and DIBL.

Key device metrics for analog applications are small signal transconductance, output resistance, and self-gain.

Given a set of IV characteristics, you should be able to extract these metrics.

Our focus is this course is to relate these device metrics to the underlying physics.

Next topic: Compact circuit models

Device metrics help device engineers and circuit design engineers to relate, in a general way, device performance to circuit performance.

Actual circuit design requires more. The next lecture is a short introduction to **compact circuit models**.