

# Depletion region 耗尽：载流子的耗尽

In semiconductor physics, the **depletion region**, also called **depletion layer**, **depletion zone**, **junction region**, **space charge region** or **space charge layer**, is **an insulating region within a conductive, doped semiconductor material where the mobile charge carriers have been diffused away, or have been forced away by an electric field**. The only elements left in the depletion region are ionized donor or acceptor impurities.

**This region of uncovered positive and negative ions is called the depletion region due to the depletion of carriers in this region.**

The depletion region is so named because it is formed from a conducting region by removal of all free charge carriers, leaving none to carry a current. Understanding the depletion region is key to explaining modern semiconductor electronics: diodes, bipolar junction transistors, field-effect transistors, and variable capacitance diodes all rely on depletion region phenomena.

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## Formation in a p–n junction

A depletion region forms instantaneously across a p–n junction. It is most easily described when the junction is in thermal equilibrium or in a steady state: in both of these cases the properties of the system do not vary in time; they have been called dynamic equilibrium.<sup>[1][2]</sup>

Electrons and holes diffuse into regions with lower concentrations of them, much as ink diffuses into water until it is uniformly distributed. By definition, the N-type semiconductor has an excess of free electrons (in the conduction band) compared to the P-type semiconductor, and the P-type has an excess of holes (in the valence band) compared to the N-type. Therefore, when N-doped and P-

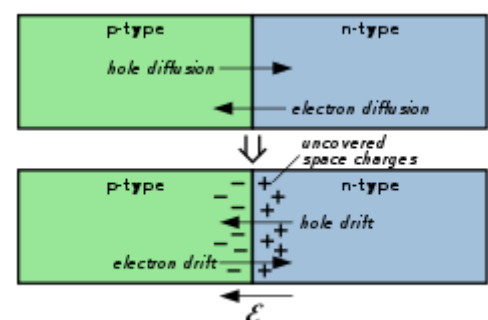


Figure 1. Top: p–n junction before diffusion; Bottom: After equilibrium is reached

doped semiconductors are placed together to form a junction, free electrons in the N-side conduction band migrate (diffuse) into the P-side conduction band, and holes in the P-side valence band migrate into the N-side valence band.

Following transfer, the diffused electrons come into contact with holes and are eliminated by recombination in the P-side. Likewise, the diffused holes are recombined with free electrons so eliminated in the N-side. The net result is that the diffused electrons and holes are gone. In a N-side region near to the junction interface, free electrons in the conduction band are gone due to (1) the diffusion of electrons to the P-side and (2) recombination of electrons to holes that are diffused from the P-side. Holes in a P-side region near to the interface are also gone by a similar reason. **As a result, majority charge carriers (free electrons for the N-type semiconductor, and holes for the P-type semiconductor) are depleted in the region around the junction interface, so this region is called the depletion region or depletion zone.** Due to the majority charge carrier

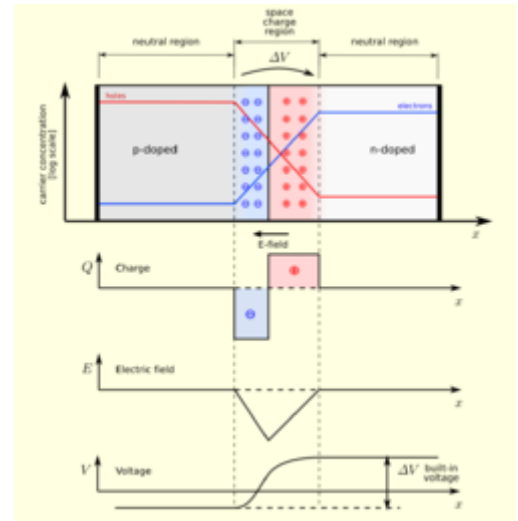


Figure 2. From Top to Bottom; Top: hole and electron concentrations through the junction; Second: charge densities; Third: electric field; Bottom: electric potential

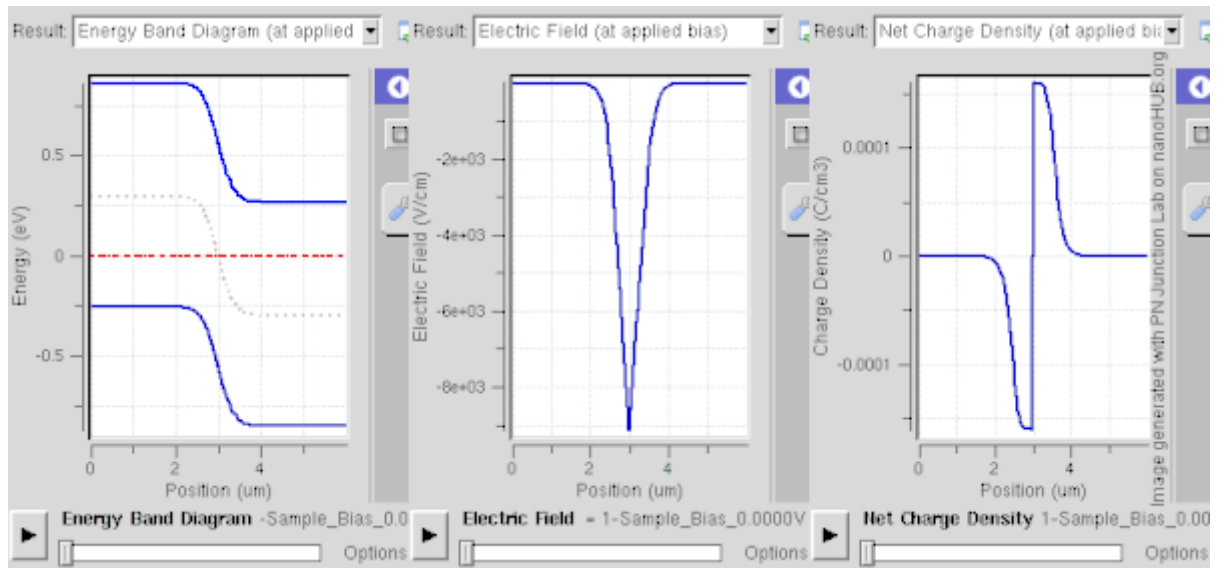


Figure 3. A PN junction in forward bias mode, the depletion width decreases. Both p and n junctions are doped at a  $1e15/cm^3$  doping level, leading to built-in potential of  $\sim 0.59V$ . Observe the different Quasi Fermi levels for conduction band and valence band in n and p regions (red curves).

diffusion described above, the depletion region is charged; the N-side of it is positively charged and the P-side of it is negatively charged. This creates an electric field that provides a force opposing the charge diffusion. When the electric field is sufficiently strong to cease further diffusion of holes and electrons, the depletion region reaches the equilibrium. Integrating the electric field across the depletion region determines what is called the **built-in voltage** (also called the junction voltage or barrier voltage or contact potential).

Physically speaking, charge transfer in semiconductor devices is from (1) the charge carrier drift by the electric field and (2) the charge carrier diffusion due to the spatially varying carrier concentration. In the P-side of the depletion region, where holes drift by the electric field with the electrical conductivity  $\sigma$  and diffuse with the diffusion constant  $D$ , the net current density is given by

$$\mathbf{J} = \sigma \mathbf{E} - eD \nabla p,$$

where  $\mathbf{E}$  is the electric field,  $e$  is the elementary charge ( $1.6 \times 10^{-19}$  coulomb), and  $p$  is the hole density (number per unit volume). The electric field makes holes drift along the field direction, and for diffusion holes move in the direction of decreasing concentration, so for holes a negative current results for a positive density gradient. (If the carriers are electrons, the hole density  $p$  is replaced by the electron density  $n$  with negative sign; in some cases, both electrons and holes must be included.) When the two current components balance, as in the p–n junction depletion region at dynamic equilibrium, the current is zero due to the Einstein relation, which relates  $D$  to  $\sigma$ .

## Forward bias

Forward bias (applying a positive voltage to the P-side with respect to the N-side) narrows the depletion region and lowers the barrier to carrier injection (shown in the figure to the right). In more detail, majority carriers get some energy from the bias field, enabling them to go into the region and neutralize opposite charges. The more bias the more neutralization (or screening of ions in the region) occurs. The carriers can be recombined to the ions but thermal energy immediately makes recombined carriers transition back as Fermi energy is in proximity. When bias is strong enough that the depletion region becomes very thin, the diffusion component of the current (through the junction interface) greatly increases and the drift component decreases. In this case, the net current flows from the P-side to the N-side. The carrier density is large (it varies exponentially with the applied bias voltage), making the junction conductive and allowing a large forward current.<sup>[3]</sup> The mathematical description of the current is provided by the Shockley diode equation. The low current conducted under reverse bias and the large current under forward bias is an example of rectification.

## Reverse bias

Under reverse bias (applying a negative voltage to the P-side with respect to the N-side), the potential drop (i.e., voltage) across the depletion region increases. Essentially, majority carriers are pushed away from the junction, leaving behind more charged ions. Thus the depletion region is widened and its field becomes stronger, which increases the drift component of current (through the junction interface) and decreases the diffusion component. In this case, the net current flows from the N-side to the P-side. The carrier density (mostly, minority carriers) is small and only a very small *reverse saturation current* flows.

## Determining the depletion layer width

From a full depletion analysis as shown in figure 2, the charge would be approximated with suddenly drop at its limit points which in reality is gradually and explained by Poisson's equation. The amount of flux density would then be<sup>[4]</sup>

$$\frac{Q_n}{x_n} = qN_d$$

$$\frac{Q_p}{x_p} = -qN_a$$

where  $Q_n$  and  $Q_p$  are the amount of negative and positive charge respectively,  $x_n$  and  $x_p$  are the distance for negative and positive charge respectively with zero at the center,  $N_a$  and  $N_d$  are the amount of acceptor and donor atoms respectively and  $q$  is the electron charge.

Taking the integral of the flux density  $D$  with respect to distance  $dx$  to determine electric field  $E$  (i.e. Gauss's law) creates the second graph as shown in figure 2:

$$E = \frac{\int D dx}{\epsilon_s}$$

where  $\epsilon_s$  is the permittivity of the substance. Integrating electric field with respect to distance determines the electric potential  $V$ . This would also equal to the built in voltage  $\Delta V$  as shown in Figure 2.

$$V = \int E dx = \Delta V$$

The final equation would then be arranged so that the function of depletion layer width  $x_n$  would be dependent on the electric potential  $V$ .

$$x_n = \sqrt{\frac{2\epsilon_s}{q} \frac{N_a}{N_d} \frac{1}{N_a + N_d} (\Delta V)}$$

$$x_p = \sqrt{\frac{2\epsilon_s}{q} \frac{N_d}{N_a} \frac{1}{N_a + N_d} (\Delta V)}$$

In summary,  $x_n$  and  $x_p$  are the negative and positive depletion layer width respectively with respect to the center,  $N_a$  and  $N_d$  are the amount of acceptor and donor atoms respectively,  $q$  is the electron charge and  $\Delta V$  is the built-in voltage, which is usually the independent variable.<sup>[4]</sup>

## Formation in an MOS capacitor

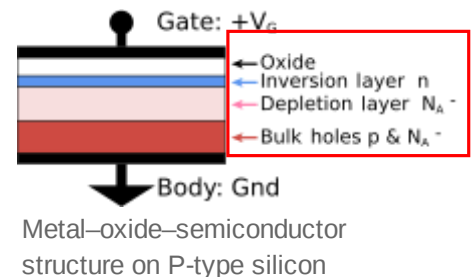
Another example of a depletion region occurs in the MOS capacitor. It is shown in the figure to the right, for a P-type substrate. Supposing that the semiconductor initially is charge neutral, with the charge due to holes exactly balanced by the negative charge due to acceptor doping impurities. If a positive voltage now is applied to the gate, which is done by introducing positive charge  $Q$  to the gate, then some positively charged holes in the semiconductor nearest the gate are repelled by the positive charge on the gate, and exit the device through the bottom contact.

They leave behind a *depleted* region that is insulating because no mobile holes remain; only the immobile, negatively charged acceptor impurities. The greater the positive charge placed on the gate, the more positive the applied gate voltage, and the more holes that leave the semiconductor surface, enlarging the depletion region. (In this device there is a limit to how wide the depletion width may become. It is set by the onset of an inversion layer of carriers in a thin layer, or channel, near the surface. The above discussion applies for positive voltages low enough that an inversion layer does not form.)

If the gate material is polysilicon of opposite type to the bulk semiconductor, then a spontaneous depletion region forms if the gate is electrically shorted to the substrate, in much the same manner as described for the p–n junction above. For more on this, see polysilicon depletion effect.

The principle of **charge neutrality** says the sum of positive charges must equal the sum of negative charges:

$$n + N_A = p + N_D ,$$



where  $n$  and  $p$  are the number of free electrons and holes, and  $N_D$  and  $N_A$  are the number of ionized donors and acceptors "per unit of length", respectively. In this way, both  $N_D$  and  $N_A$  can be viewed as doping spatial densities. If we assume full ionization and that  $n, p \ll N_D, N_A$ , then:

$$qN_A w_P \approx qN_D w_N .$$

where  $w_P$  and  $w_N$  are depletion widths in the  $p$  and  $n$  semiconductor, respectively. This condition ensures that the net negative acceptor charge exactly balances the net positive donor charge. The total depletion width in this case is the sum  $w = w_N + w_P$ . A full derivation for the depletion width is presented in reference.<sup>[5]</sup> This derivation is based on solving the Poisson equation in one dimension – the dimension normal to the metallurgical junction. The electric field is zero outside of the depletion width (seen in above figure) and therefore Gauss's law implies that the charge density in each region balance – as shown by the first equation in this sub-section. Treating each region separately and substituting the charge density for each region into the Poisson equation eventually leads to a result for the depletion width. This result for the depletion width is:

$$w \approx \left[ \frac{2\epsilon_r \epsilon_0}{q} \left( \frac{N_A + N_D}{N_A N_D} \right) (V_{bi} - V) \right]^{\frac{1}{2}}$$

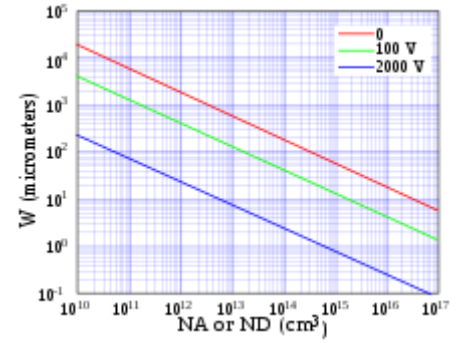
where  $\epsilon_r$  is the relative dielectric permittivity of the semiconductor,  $V_{bi}$  is the built-in voltage, and  $V$  is the applied bias. The depletion region is not symmetrically split between the  $n$  and  $p$  regions - it will tend towards the lightly doped side.<sup>[6]</sup> A more complete analysis would take into account that there are still *some* carriers near the edges of the depletion region.<sup>[7]</sup> This leads to an additional  $-2kT/q$  term in the last set of parentheses above.

## Depletion width in MOS capacitor

As in  $p$ - $n$  junctions, the governing principle here is charge neutrality. Let us assume a  $P$ -type substrate. If positive charge  $Q$  is placed on gate with area  $A$ , then holes are depleted to a depth  $w$  exposing sufficient negative acceptors to exactly balance the gate charge. Supposing the dopant density to be  $N_A$  acceptors per unit volume, then charge neutrality requires the depletion width  $w$  to satisfy the relationship:

$$Q/A = qN_A w$$

If the depletion width becomes wide enough, then electrons appear in a very thin layer at the semiconductor-oxide interface, called an **inversion layer** because they are oppositely charged to the holes that prevail in a  $P$ -type material. When an inversion layer forms, the depletion width ceases to expand with increase in gate charge  $Q$ . In this case, neutrality is achieved by attracting more electrons into the inversion layer. In the MOSFET, this inversion layer is referred to as the channel.



The total width of the depletion region is a function of applied reverse-bias and impurity concentration

## Electric field in depletion layer and band bending

Associated with the depletion layer is an effect known as band bending. This effect occurs because the electric field in the depletion layer varies linearly in space from its (maximum) value  $E_m$  at the gate to zero at the edge of the depletion width:<sup>[8]</sup>

$$E_m = \frac{Q}{A\epsilon_0} = qN_A \frac{w}{\epsilon_0},$$

where  $\epsilon_0 = 8.854 \times 10^{-12}$  F/m,  $F$  is the farad and  $m$  is the meter. This linearly-varying electric field leads to an electrical potential that varies quadratically in space. The energy levels, or energy bands, *bend* in response to this potential.

## See also

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- Capacitance voltage profiling
- Metal–oxide–semiconductor structure
- Semiconductor diodes

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