Essentials of MOSFETs

Unit 1: Transistors and Circuits

Lecture 1.2: Digital Circuits

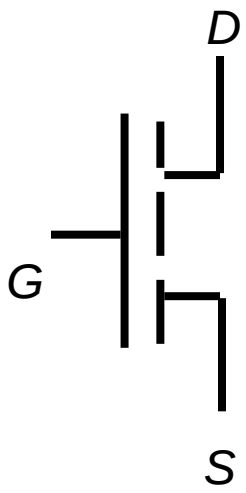
Mark Lundstrom

lundstro@purdue.edu
Electrical and Computer Engineering
Purdue University
West Lafayette, Indiana USA

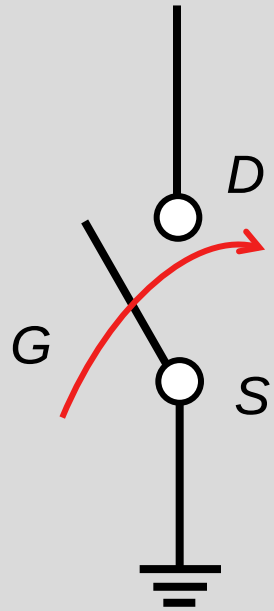
PURDUE UNIVERSITY

Applications of MOSFETs

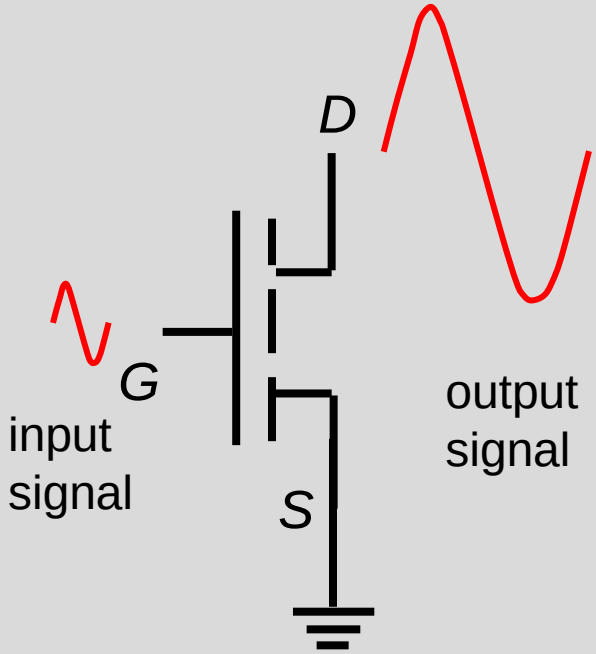
symbo



digital

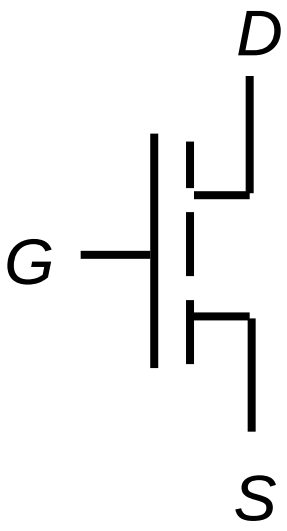


analog

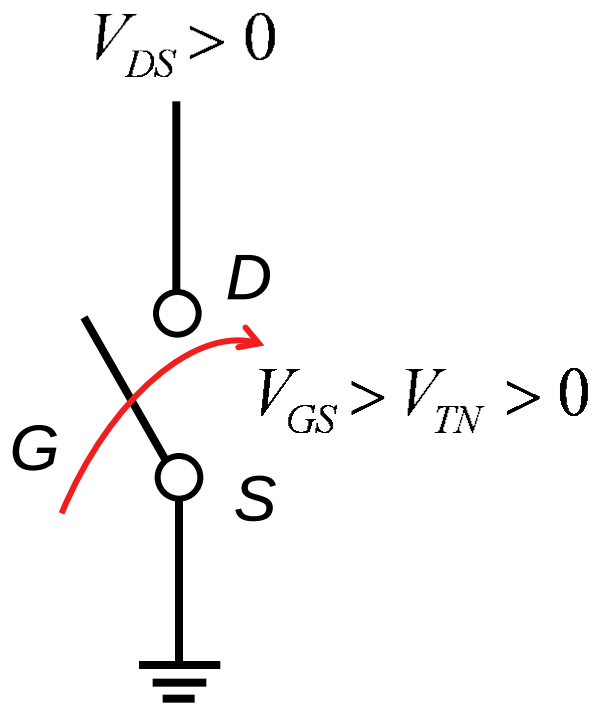


N-MOSFET as a switch

N-MOSFET
symbol

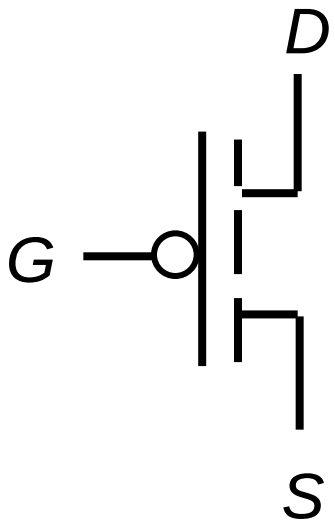


switch

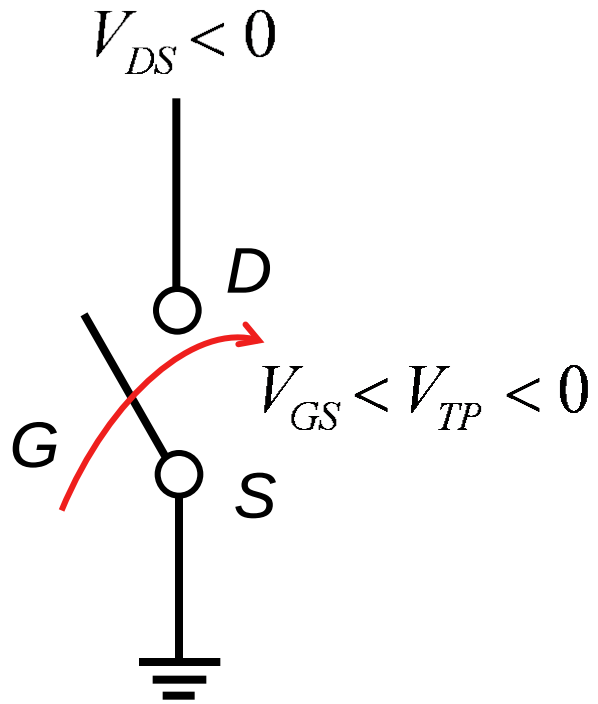


P-MOSFET as a switch

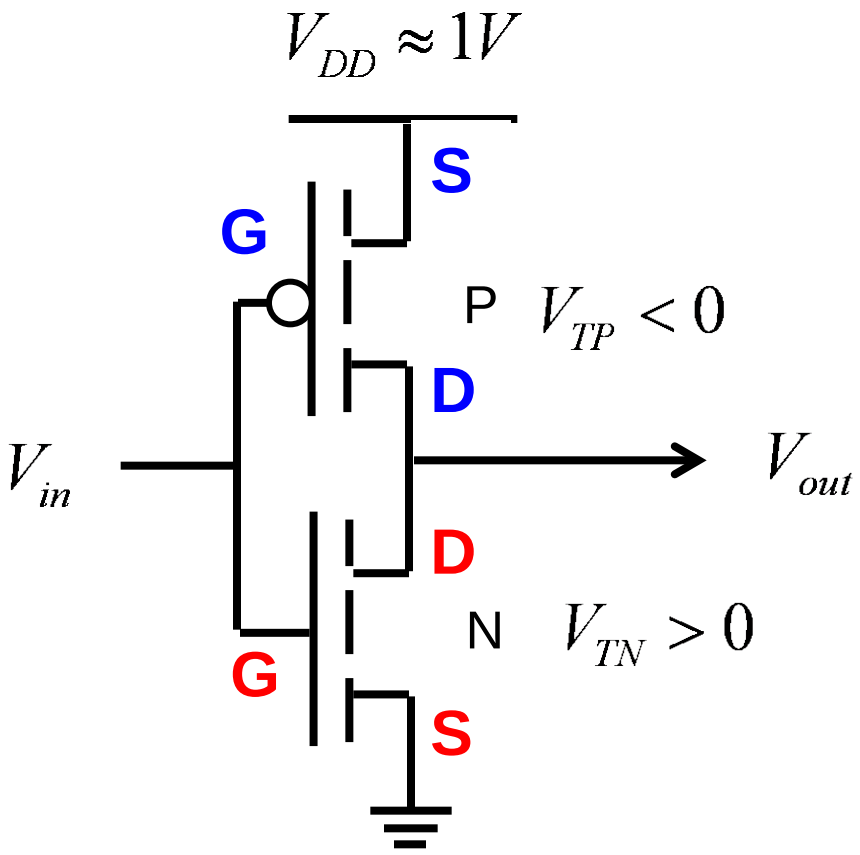
P-MOSFET symbol



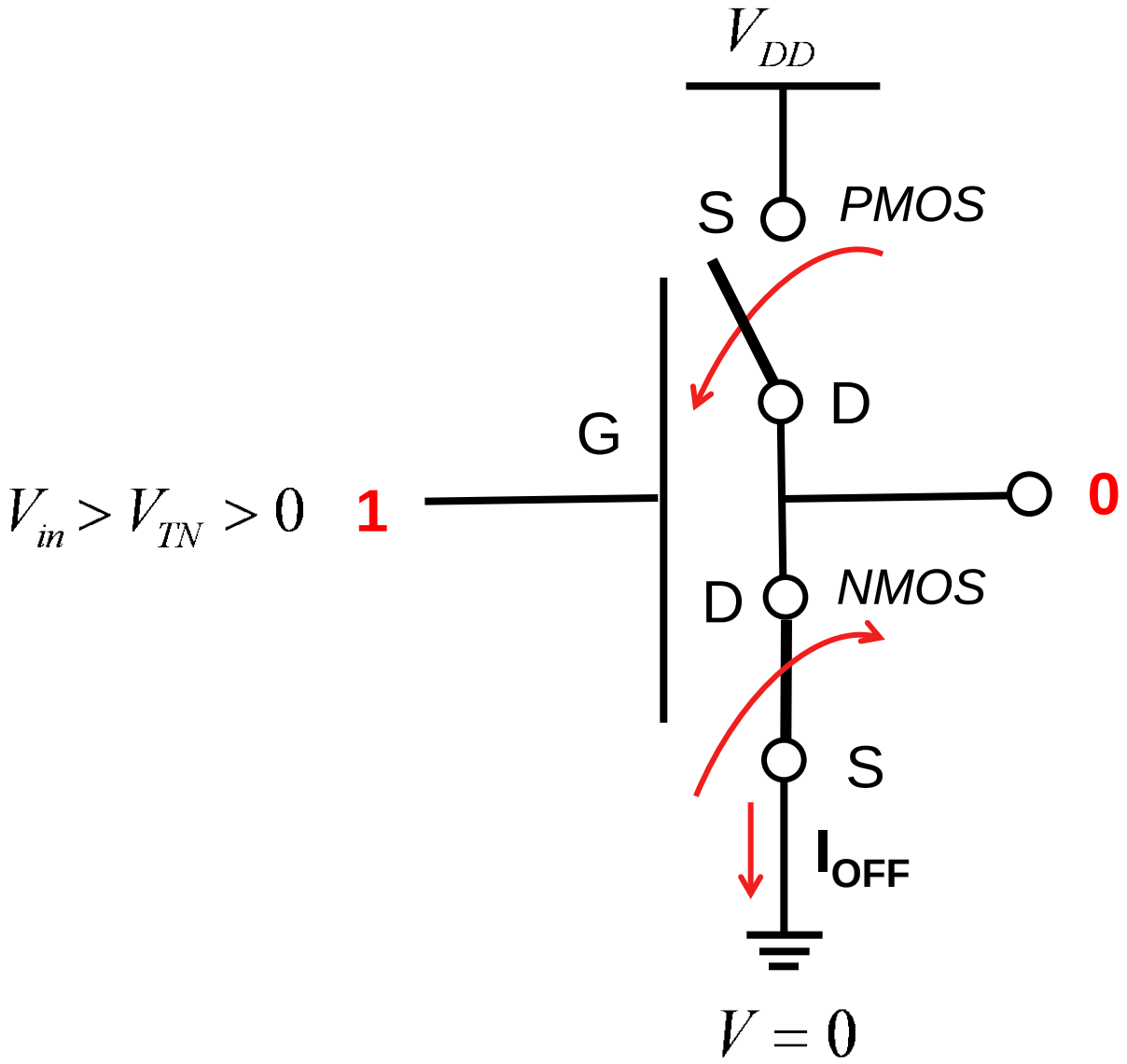
switch



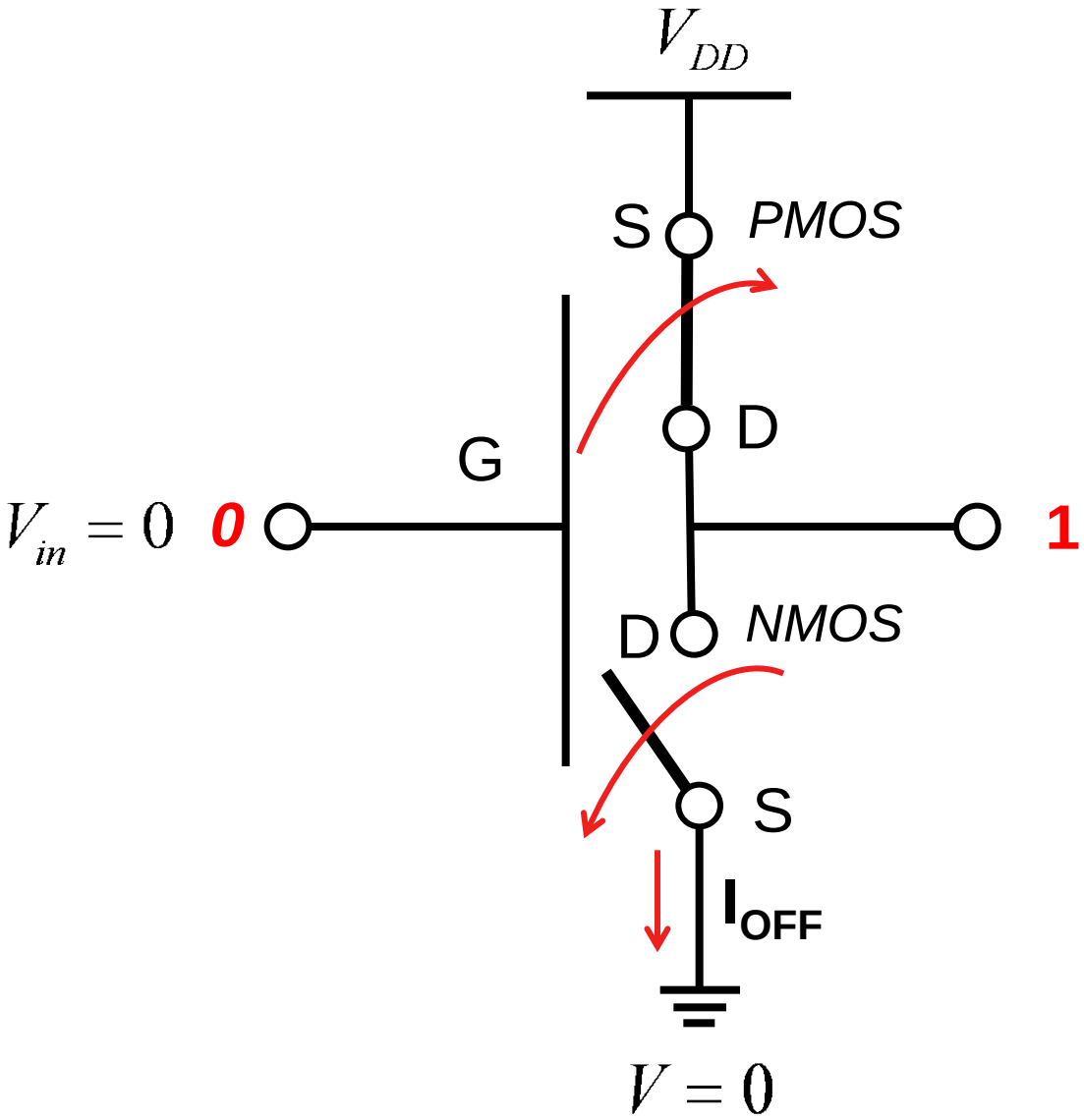
CMOS Inverter



CMOS inverter

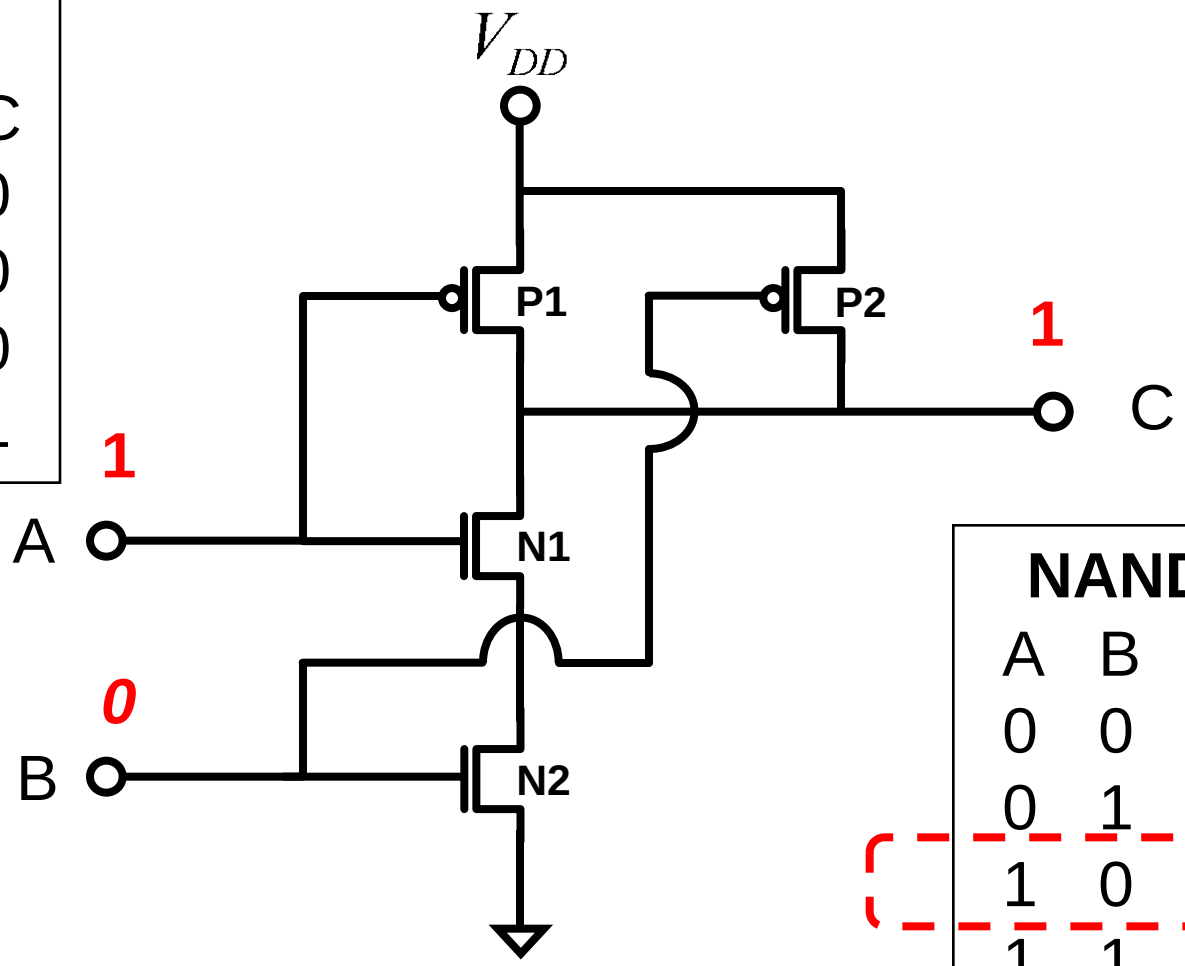


CMOS inverter



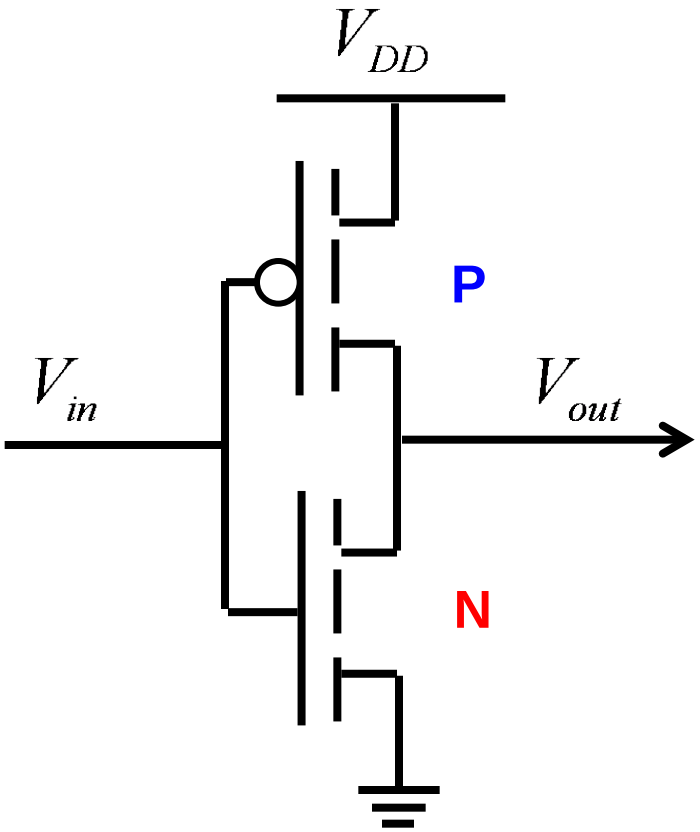
Two input NAND gate

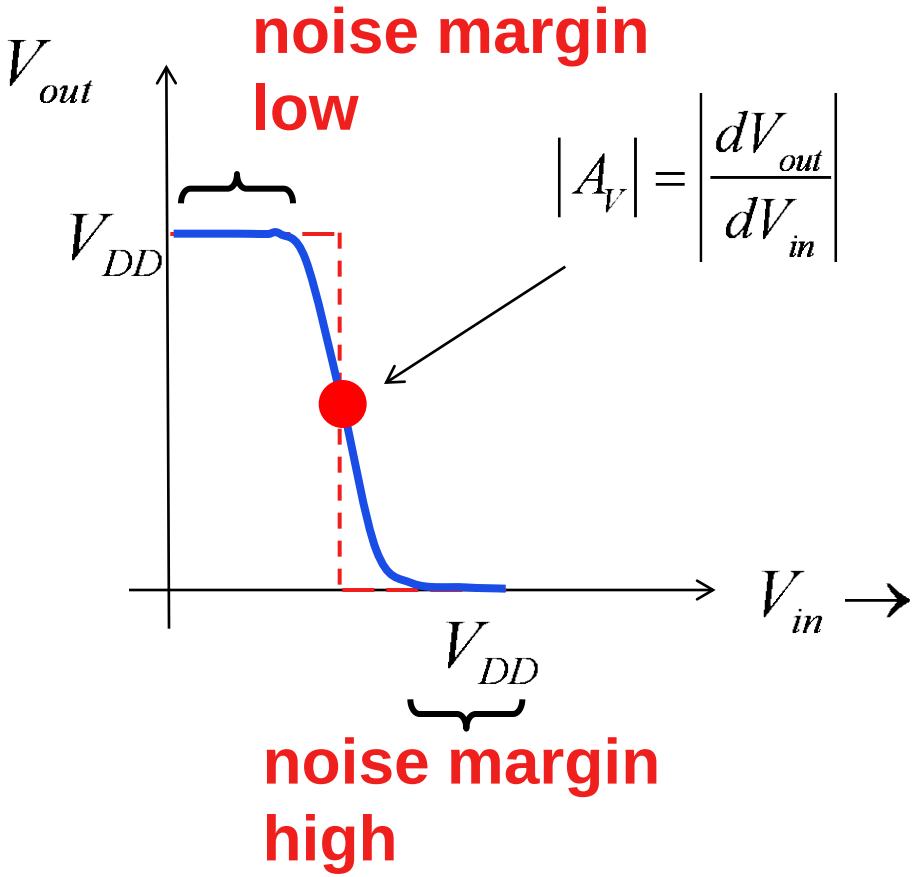
AND		
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1



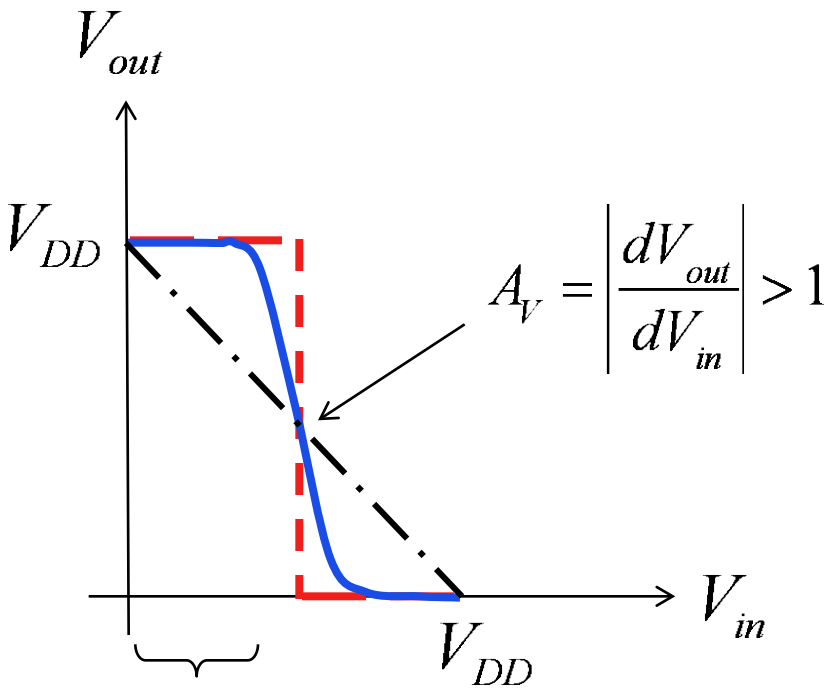
NAND		
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Transfer characteristics





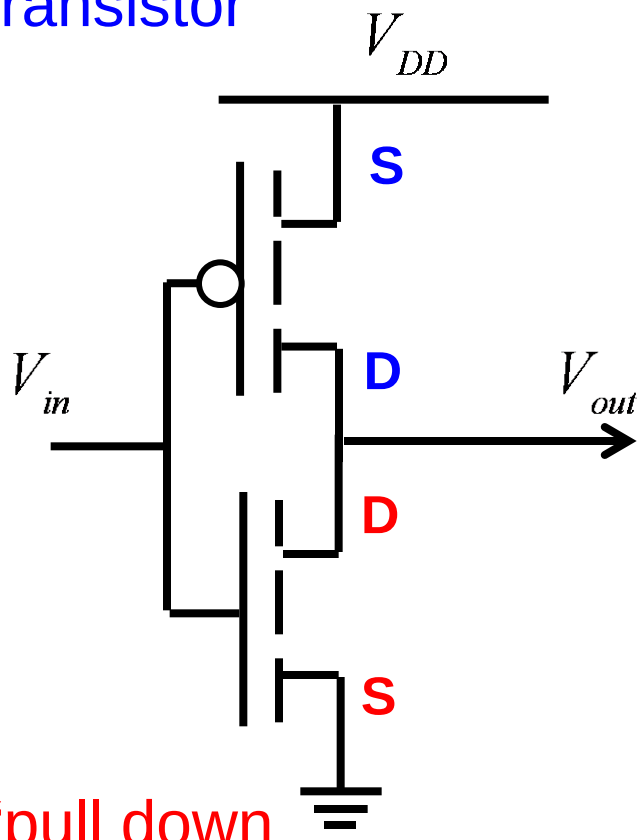
Gain restores signal levels



noise margin

CMOS inverter

"pull up transistor"



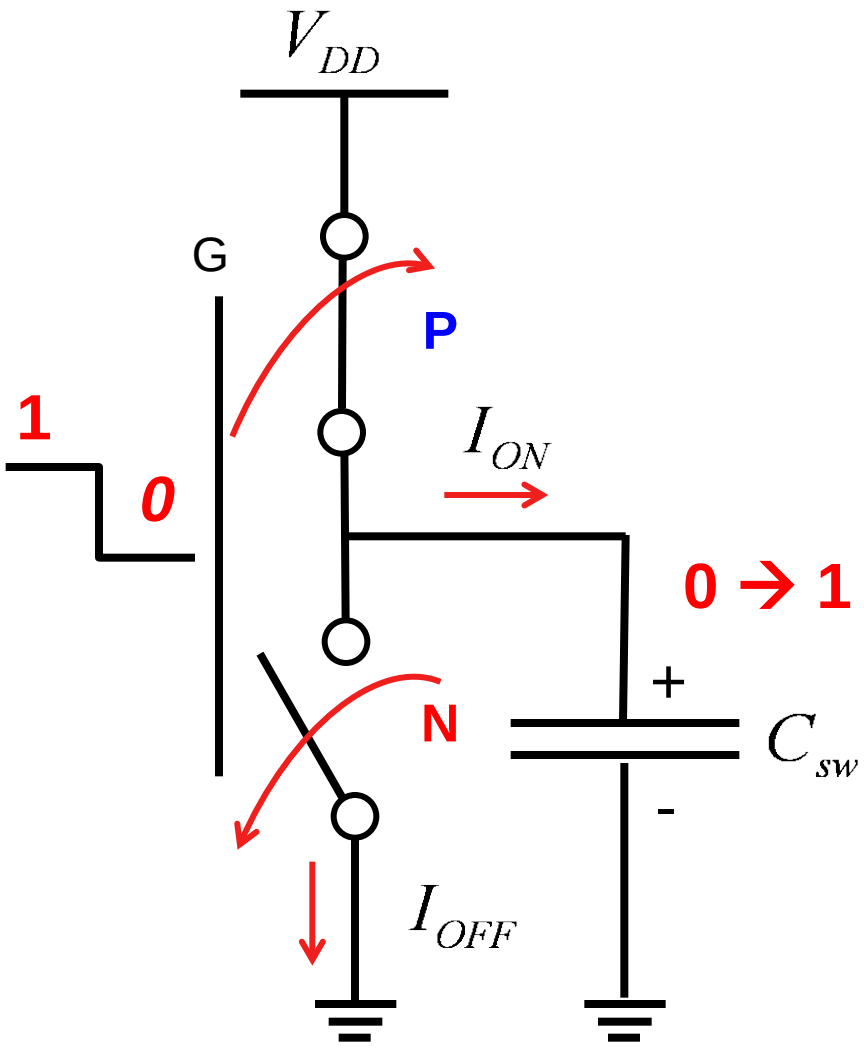
"pull down transistor"

1) little current flows (power dissipation) unless switching

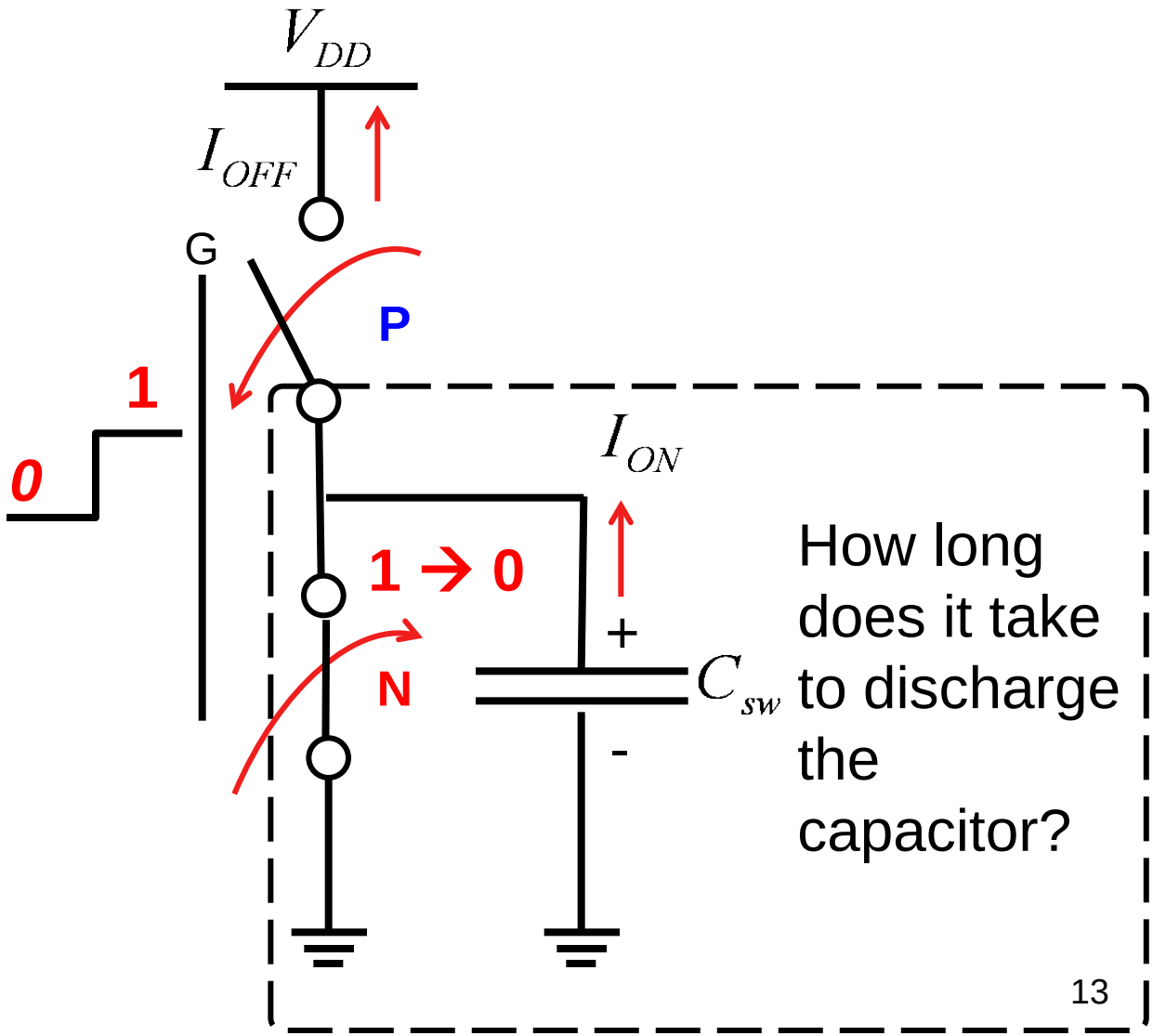
2) good noise margins if device has voltage gain

What determines ***speed*** *and* ***power****?*

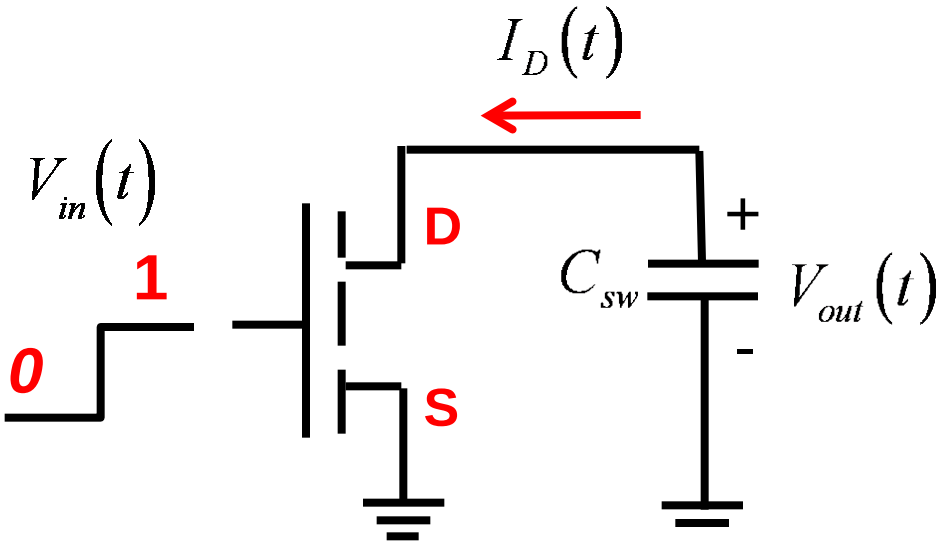
Switching (input 1 to 0)



Switching (input 0 to 1)



Discharging time



$$Q = C_{sw} V_{DD}$$

$$I_{ON} = \frac{Q}{\tau}$$

$$\tau = \frac{C_{sw} V_{DD}}{I_{ON}}$$

DC on-current controls switching time.

System speed

until ~1990:

device delay > interconnect delay

90 nm technology:

device delay: ~ 1ps

1 mm interconnect delay: ~ 6 ps

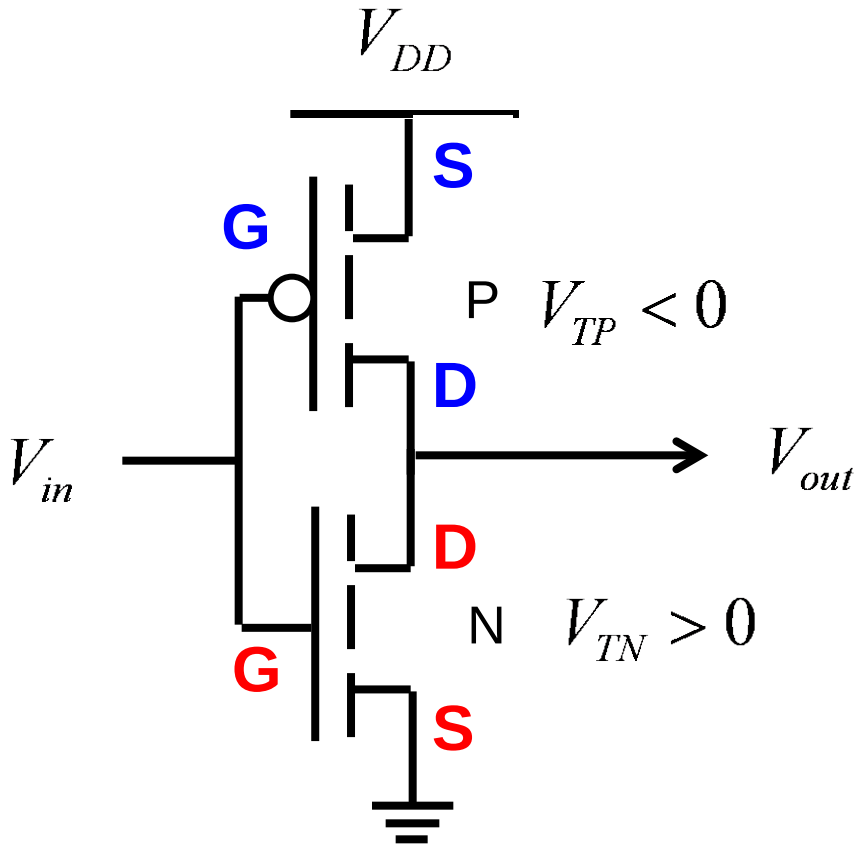
2015 (10 nm technology):

device delay: ~0.1ps

1 mm interconnect: ~30ps

J. Meindl, “Beyond Moore’s law: the interconnect era, ” *Computing in Science and Engineering*, 2003

Power dissipation

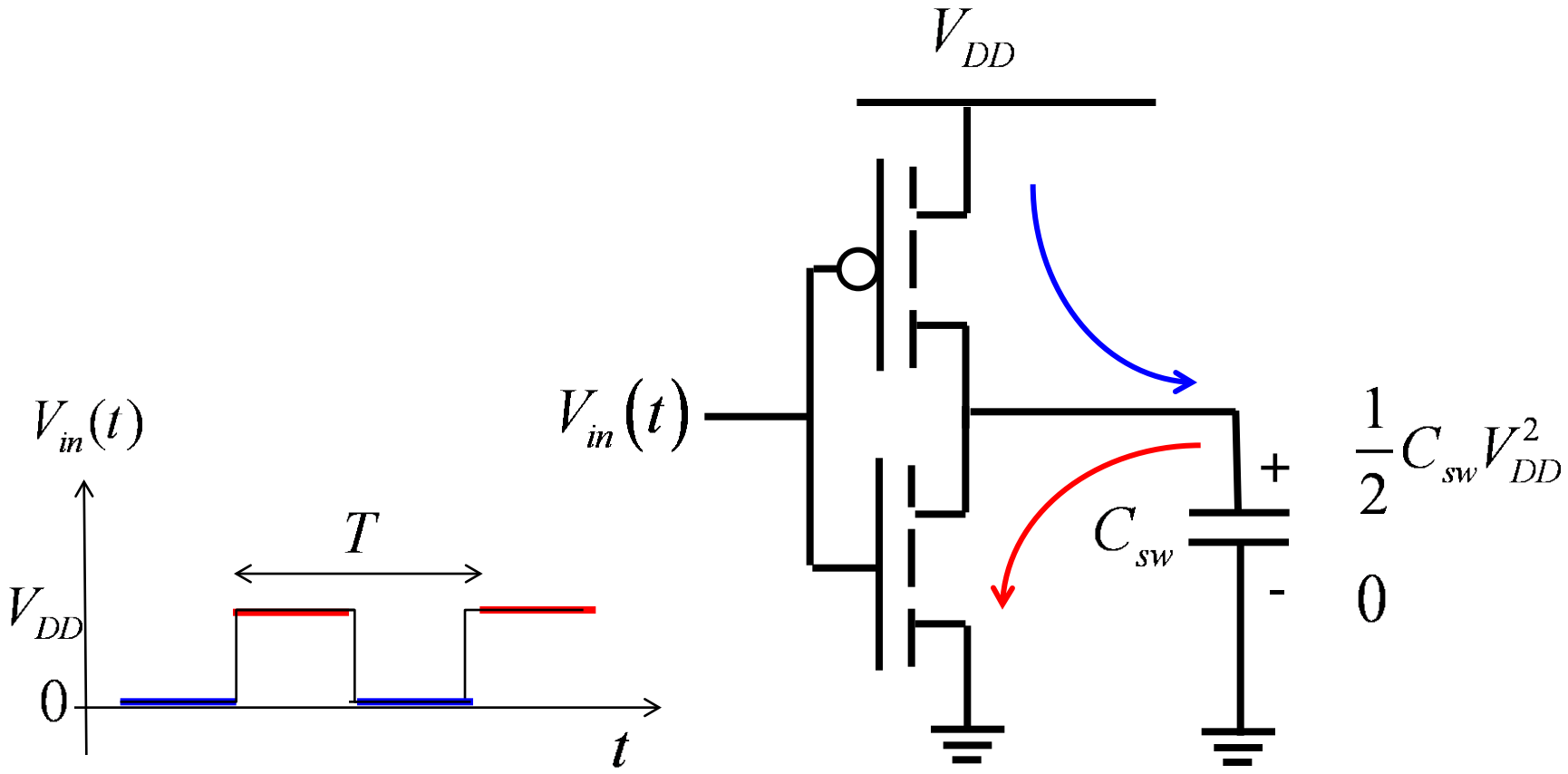


Switching speed is inversely proportional to the DC on-current.

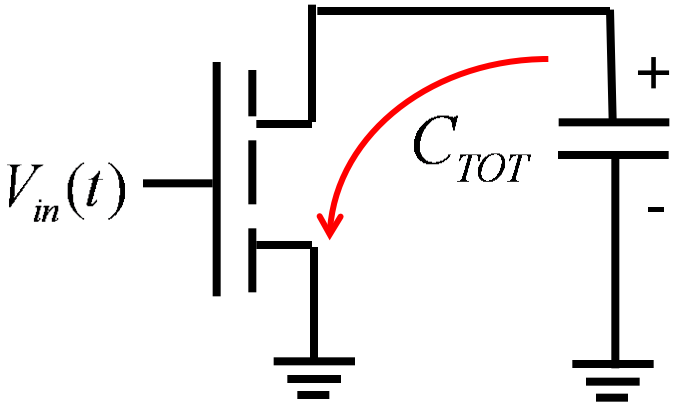
The ideal CMOS inverter only dissipates power while switching (**dynamic power**).

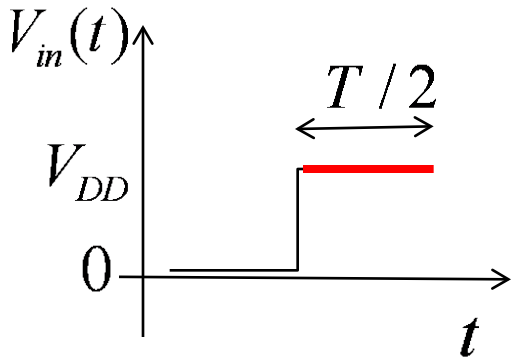
Real CMOS also dissipates power when not switching (**static power**).

Dynamic power



Dynamic power





$$E_C(0) = \frac{1}{2} C_{sw} V_{DD}^2$$

$$E_C(T/2) = 0$$

$$P_{dynamic} = \frac{\Delta E}{T/2} = \frac{C_{sw} V_{DD}^2}{T} = f C_{sw} V_{DD}^2$$

$$P_{dynamic} = \alpha f C_{sw} V_{DD}^2$$

switching “activity”

Dynamic power

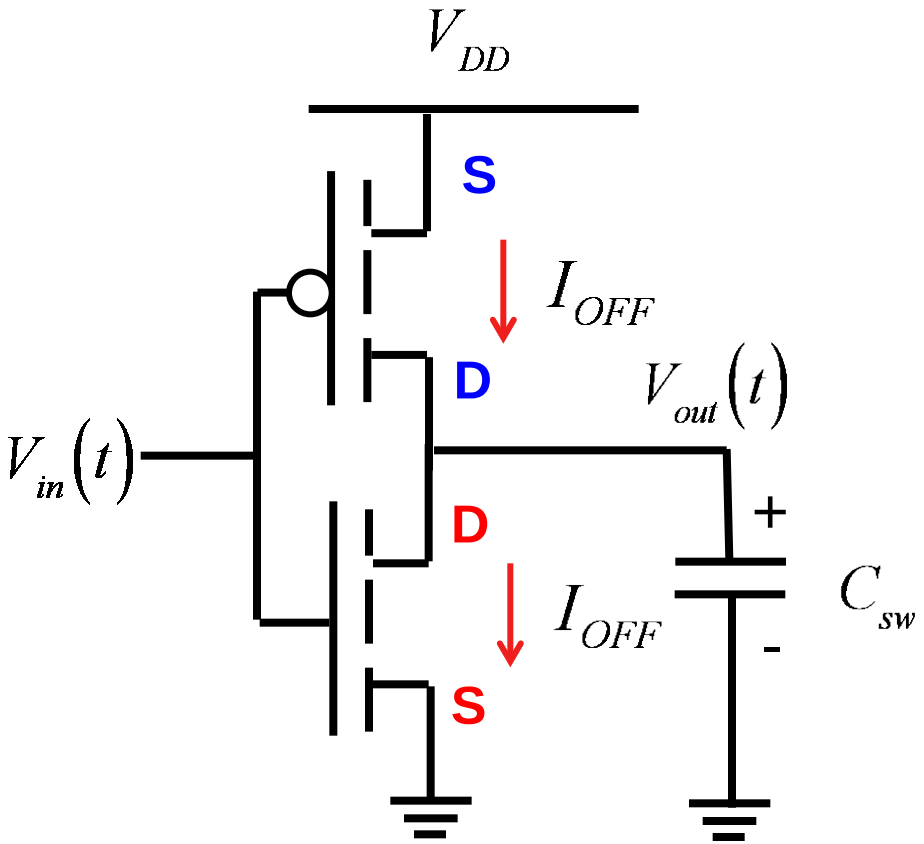
$$P_{dynamic} = \alpha f C_{sw} V_{DD}^2$$

switching “activity”

At a given frequency, the dynamic power is proportional to **the power supply voltage squared** and to the **frequency**.

What determines the **static power**?

Static power



$$P_{static} = I_{off} V_{DD}$$

N_G = no. of gates

$$P_{static} = N_G I_{off} V_{DD}$$

CMOS speed and power

$$\tau = C_{sw} V_{DD} / I_{ON}$$

$$P_{\text{dynamic}} = \alpha f C_{sw} V_{DD}^2$$

$$P_{\text{static}} = N_G I_{OFF} V_{DD}$$

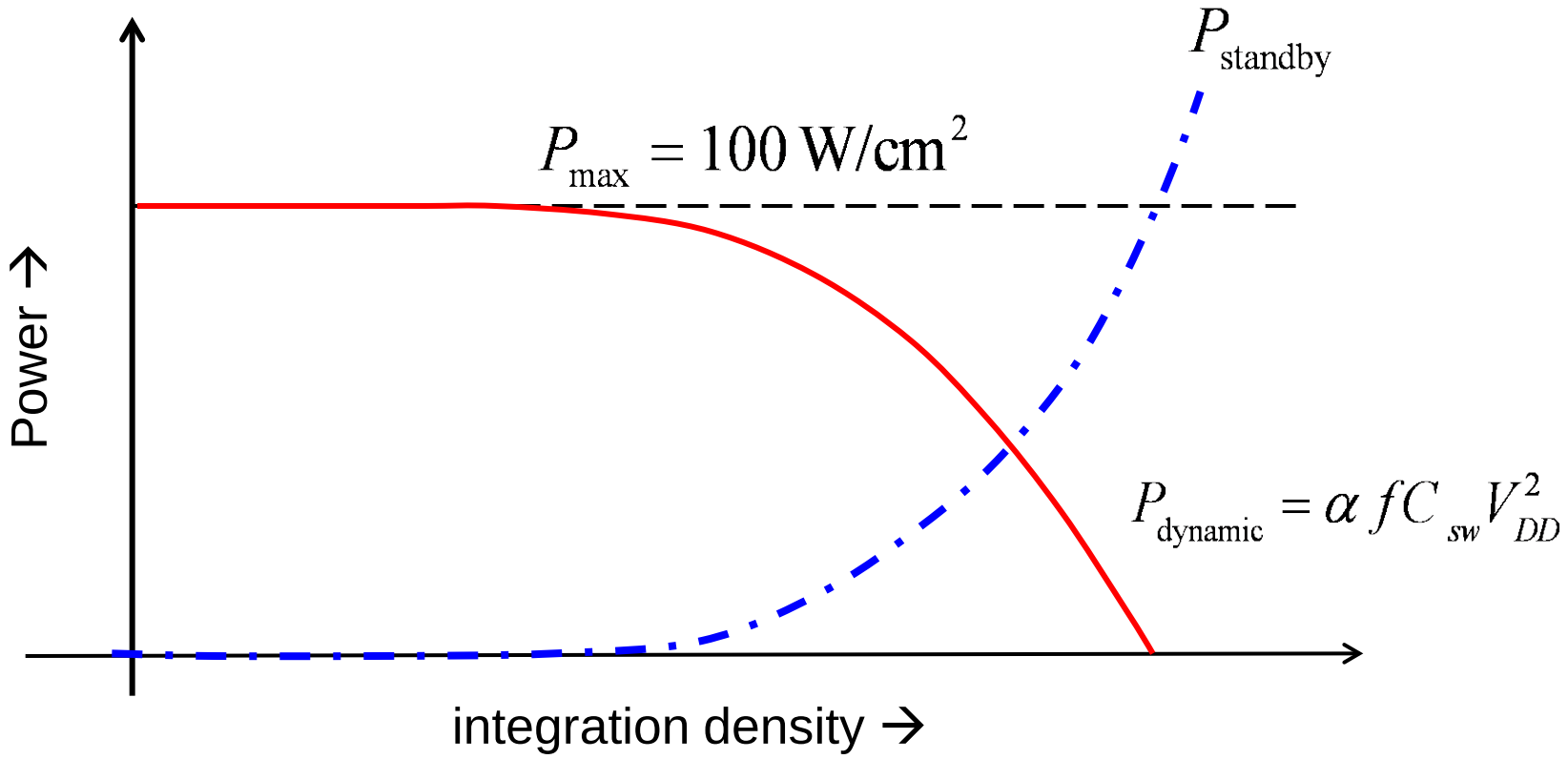
1) Higher on-current means higher speed

2) Faster operation means more dynamic power

3) Lower V_{DD} means lower power

4) More leakage means more power dissipation

Power constrained design



(after Dave Frank, IBM)

Summary

Complementary MOS (CMOS) makes use of NMOS and PMOS transistors.

The basic building block of CMOS logic is the CMOS inverter.

Voltage gain is required for noise margins.

On-current, off-current, and power supply voltage are key parameters.

Next topic: A primer on analog circuits

We now understand what's important for digital circuits. In the next lecture, we'll take a quick look **at analog and radio frequency** circuits.