# Unit 5: Additional Topics

# Lecture 5.1: Limits of MOSFETs

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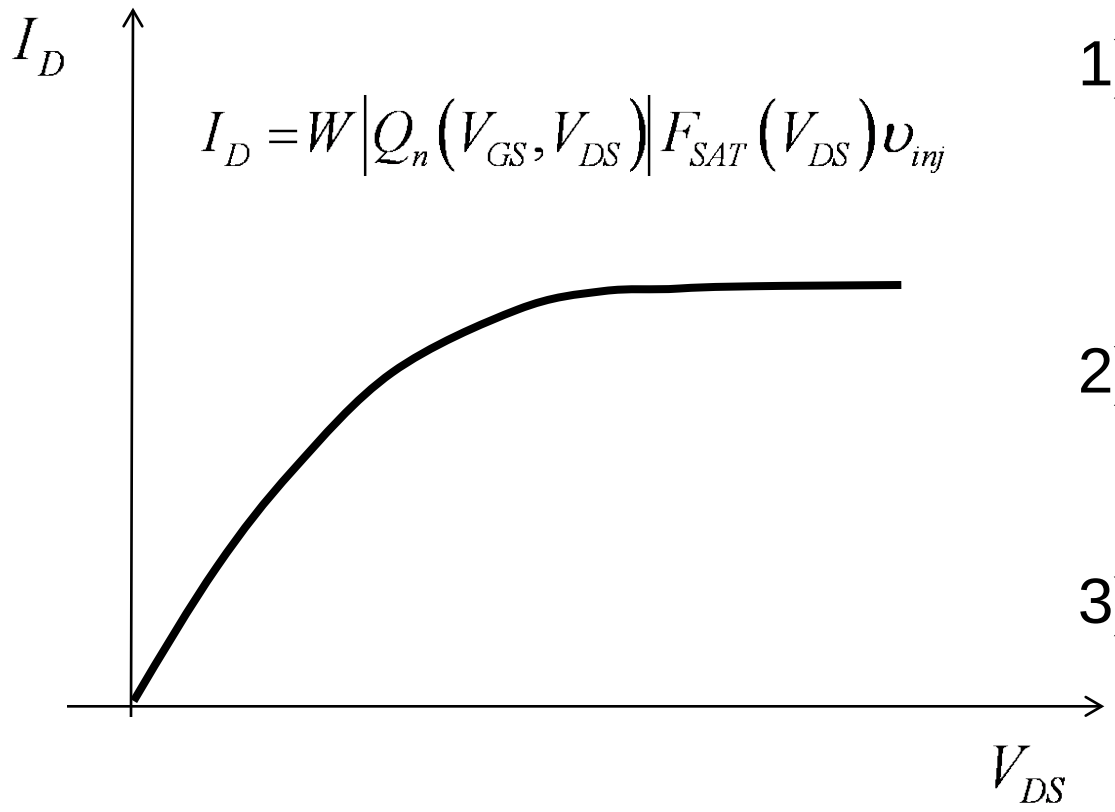
# Questions (for digital logic)



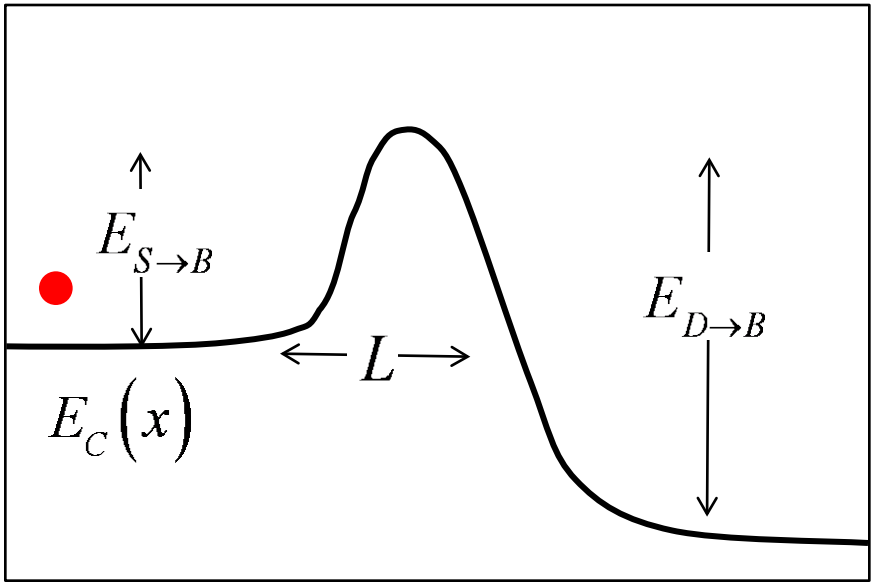

1) What are the fundamental limits of MOSFETs?

2) How close are we to those limits today?

3) What sets the limits in practice?

# MOSFETs are barrier controlled devices

Off-state

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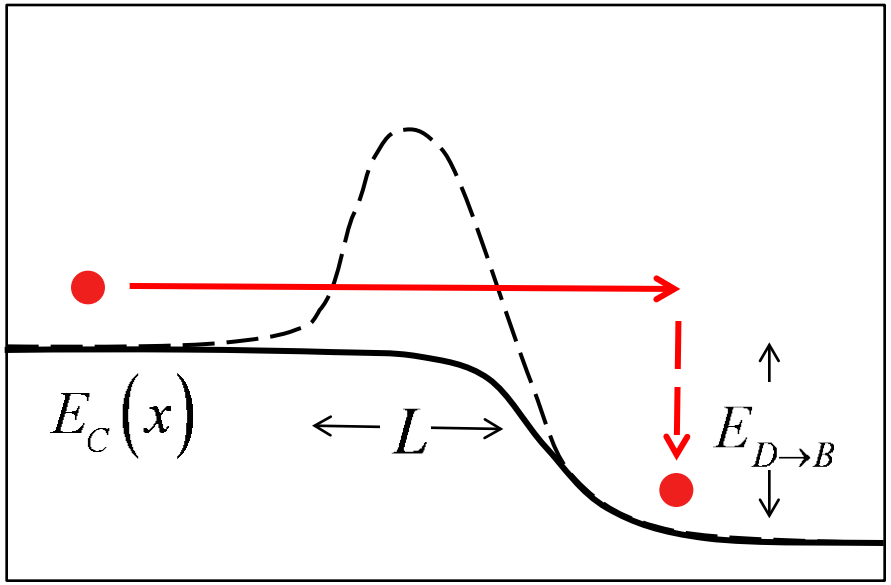



(Recall Lecture 2.2)

# Fundamental limits of MOSFETs

We will use some very simple arguments to estimate some ultimate limits for transistors. Our approach is similar to (but not quite the same) as the approach of Zhirnov, *et al*.

V. V. Zhirnov, R.K. Cavin III, J.A. Hutchby, and G.I. Bourianoff, ”Limits to Binary Logic Switch Scaling – A Gedanken Model,” *Proc. IEEE*, **91**, pp. 1934 - 1939 , 2003.

# Three questions

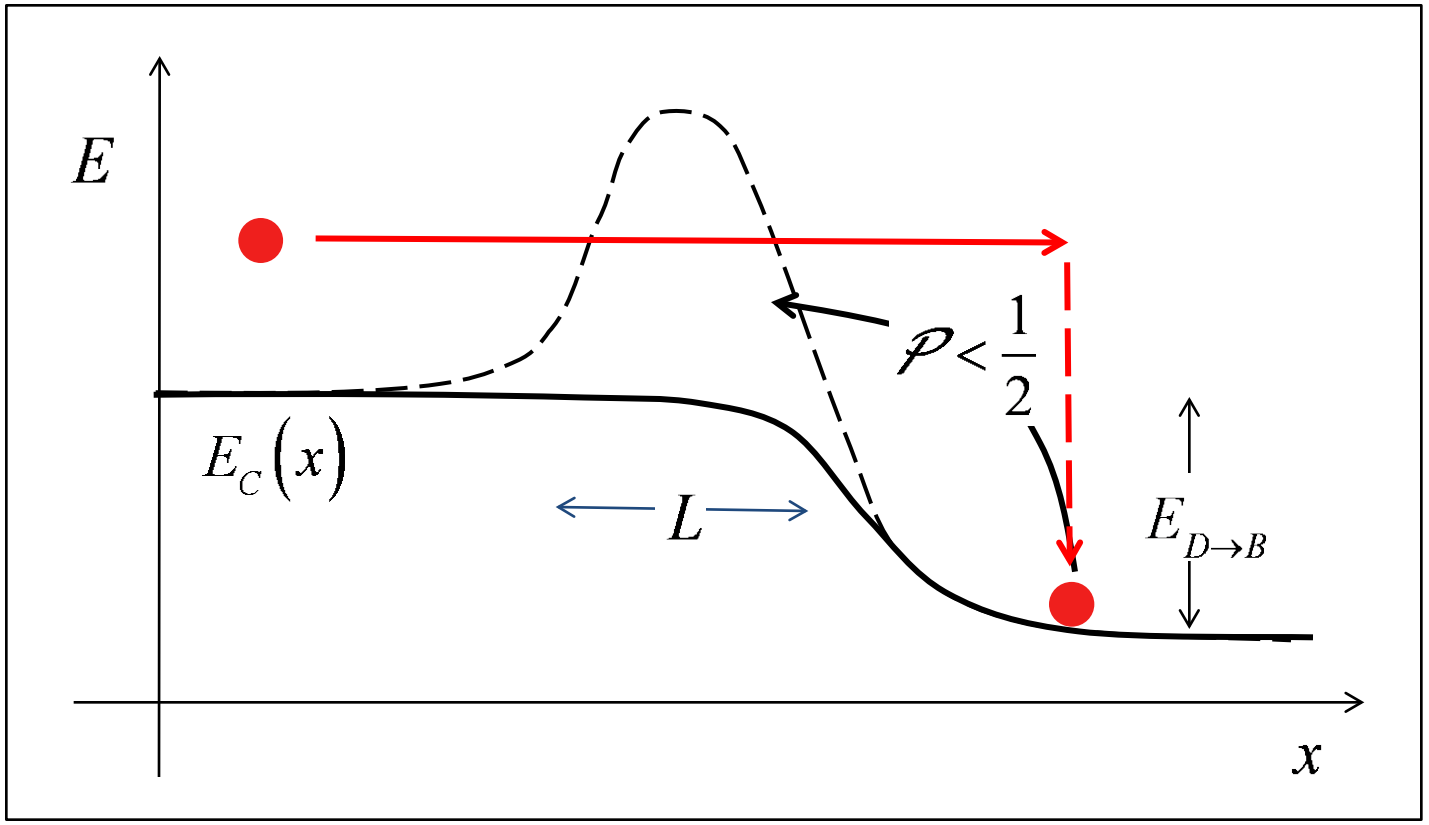
1) What is the minimum switching energy for a MOSFET?

2) What is the minimum channel length?

3) What is the minimum switching time?

# 1) Minimum switching energy

On-state



# Minimum switching energy

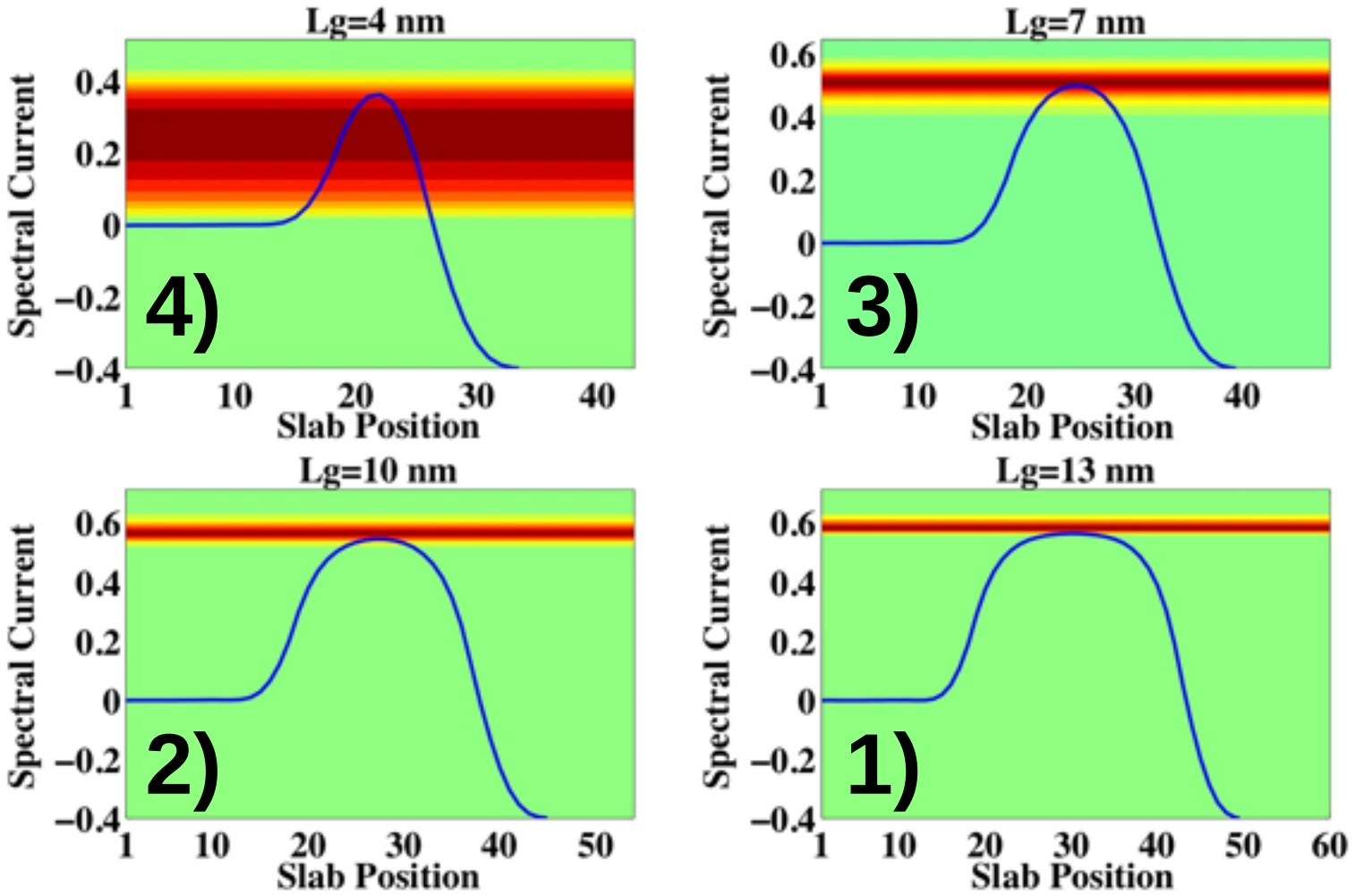
To have a switching event, the electron must stay in the drain and not be thermionically re-emitted back to the source. We require:

$$\mathcal{P} = e^{-E_{D\to B}/k_B T} < \frac{1}{2}$$

$$e^{-E_{\min}/k_B T} = \frac{1}{2}$$

$$E_{\min} = k_B T \ln 2$$

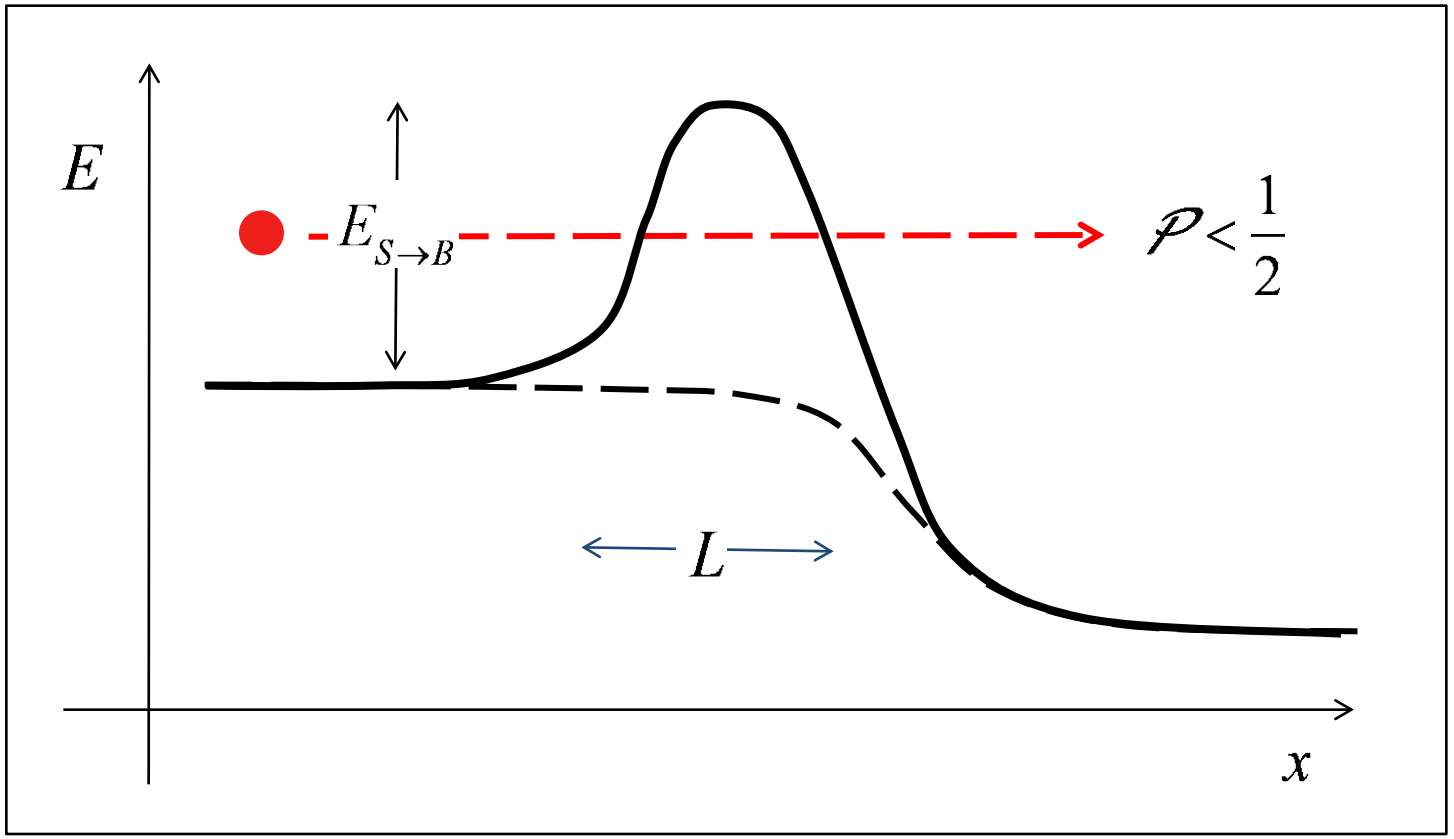
# 2) Minimum channel length and QM tunneling




(Provided by M. Luisier, ETH Zurich)

# Minimum channel length

Off-state



# Minimum channel length

$$\mathcal{P} = e^{-2\sqrt{2m^* E_{S\to B}}L/\hbar}$$ (WKB approximation)

$$\mathcal{P} < \frac{1}{2}$$ (To say that the device is off)

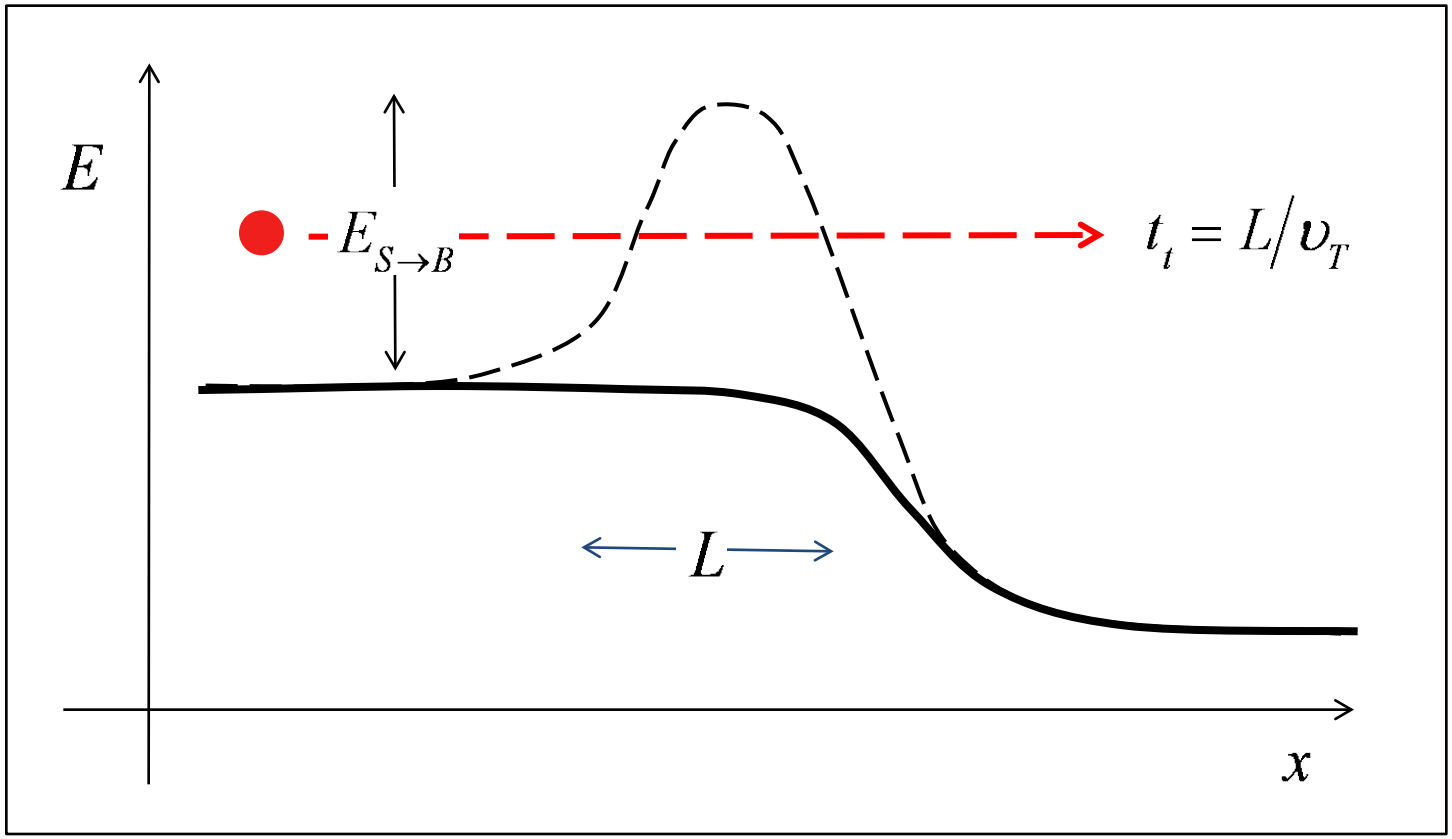
$$L > \frac{\hbar}{\sqrt{2m^* E_{S\to B}}}$$

$$E_{S\to B} = E_{\min}$$

$$L_{\min} = \frac{\hbar}{\sqrt{2m^* E_{\min}}}$$

# 3) Minimum switching time

On-state



# Minimum switching time

The minimum switching time is the **transit time** – the time it takes for an electron to cross the channel.

$$t_t = \frac{L}{\upsilon_T}$$

$$\tau_{\min} = \frac{L_{\min}}{\upsilon_T} \qquad \upsilon_T = \sqrt{\frac{2k_BT}{\pi m^*}} \qquad E_{\min} = k_BT\ln 2$$

(Discarding some constants on the order of unity…)

$$\tau_{\min} = \frac{\hbar}{E_{\min}}$$

# “Fundamental limits”

$$E_{\min} = k_B T \ln 2 = 0.017 \text{ eV}$$

$$L_{\min} = \frac{\hbar}{\sqrt{2m^* E_{\min}}} = 1.5 \text{ nm} \qquad \left(m^* = m_0\right)$$

$$\tau_{\min} = \frac{\hbar}{E_{\min}} = 40 \text{ fs}$$

# Discussion

The minimum switching energy, $E_{\min} = k_B T \ln 2$, is usually derived using thermodynamic arguments.

The minimum channel length and switching times can also be derived from the two quantum mechanical uncertainty relations:

$$\Delta E \Delta t \geq \frac{\hbar}{2}$$

$$\Delta p \Delta x \geq \frac{\hbar}{2}$$

# Discussion

The fact that the fundamental limits for MOSFETs can also be derived with some very general thermodynamic and quantum mechanic arguments, suggests that they apply to any switching device.

# 22 nm technology

$$V_{DD} = 0.7 \text{ V}$$

$$C_{inv} \approx 2.9 \times 10^{-6} \text{ F/cm}^2$$

$$C_G = C_{inv}(WL) \approx 24 \times 10^{-18} \text{ F}$$

$$W = L = 22 \text{ nm}$$

$$I_{ON} \approx 1 \times 10^{-3} \text{ A}/\mu\text{m}$$

$$\frac{1}{2} C_G V_{DD}^2 \approx 1200 \times E_{\min}$$

$$L = 22 \text{ nm} = 15 \times L_{\min}$$

$$\tau = \frac{C_G V_{DD}}{I_{ON}} \approx 11 \times \tau_{\min}$$

Channel length and switching time are within about a factor of 10 above fundamental limits. Energy (and power) are orders of magnitude larger that the fundamental limits.

# What sets the limits in practice?

1) Minimum switching energy: $E_{\min} = k_B T \ln(2)$

In practice, the switching energy is: $E_{sw\,n} = \frac{1}{2} C_{sw} V_{DD}^2$

The switching capacitance includes all the parasitic capacitances and the capacitance of the wiring. It can be quite large (~1 fF/node).

The power supply voltage is far above the minimum because low error computation requires an on-off ratio of ~$10^4$. The MOSFET IV characteristic then dictates that $V_{DD}$ ~ 1 V.

# What sets the limits in practice?

2) Minimum channel length: $L_{\min} = \frac{\hbar}{\sqrt{2m^* E_{\min}}}$

The fundamental limit is set by quantum mechanical tunneling assuming an on-off ratio of 1.

In practice, 2D electrostatics is the main concern (leading to the replacement of planar FETs by FinFETs).

The increasing cost of lithography is also a concern.

# What sets the limits in practice?

3) Minimum switching speed: $\tau_{\min} = \frac{\hbar}{E_{\min}}$

In practice, the switching speed is: $\tau_{dev} = \frac{C_{dev} V_{DD}}{I_{ON}}$

The device capacitance includes a parasitic capacitance.

$$C_{dev} = WLC_{inv} + C_{par}$$

The parasitic gate-drain capacitance is a larger and larger fraction of the total gat capacitance.

# Summary

1) Transistors are approaching some very fundamental limits.

2) Practical, technology considerations such as series resistance, parasitic capacitance, BTBT leakage currents, etc. are likely to set the practical limits.

3) It is unlikely that any digital switching device that is fundamentally better than a MOSFET exists.

# Next topic

We have focused on digital and analog applications of MOSFETs, but there are other applications.

For example, MOSFETs can be used as switching devices in power electronic systems.