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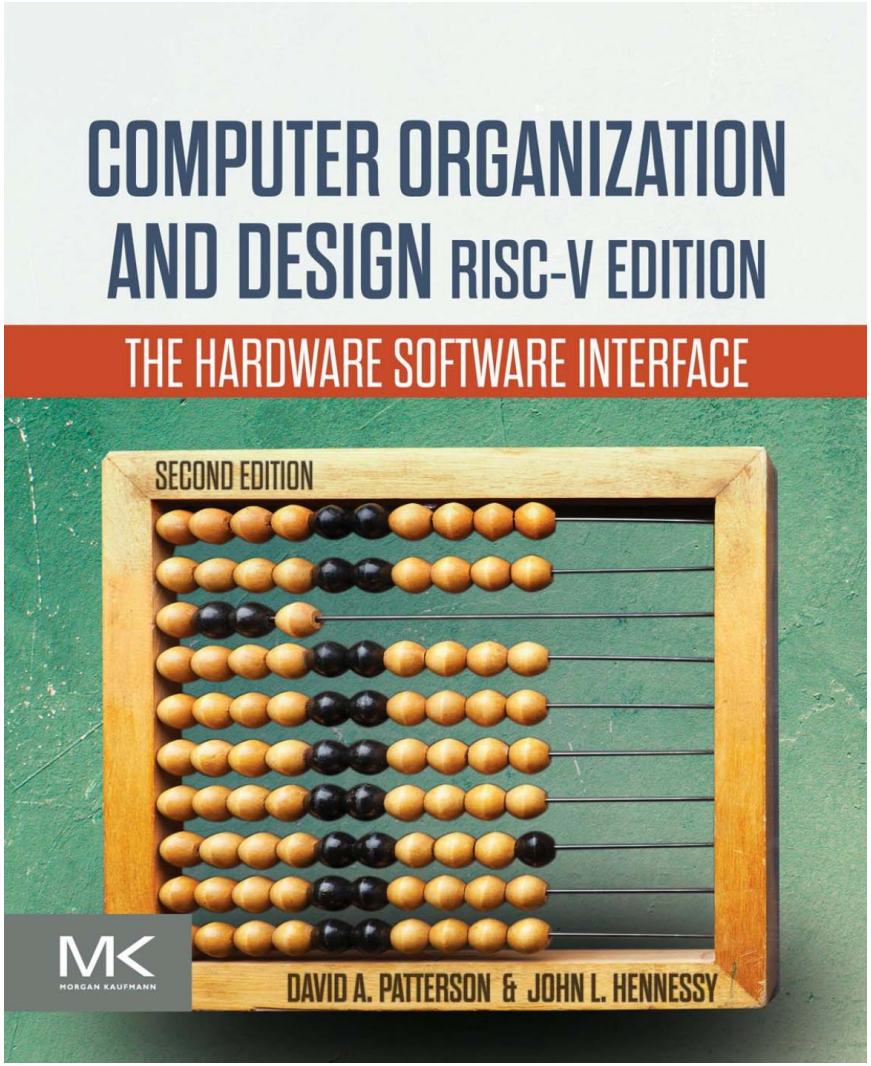
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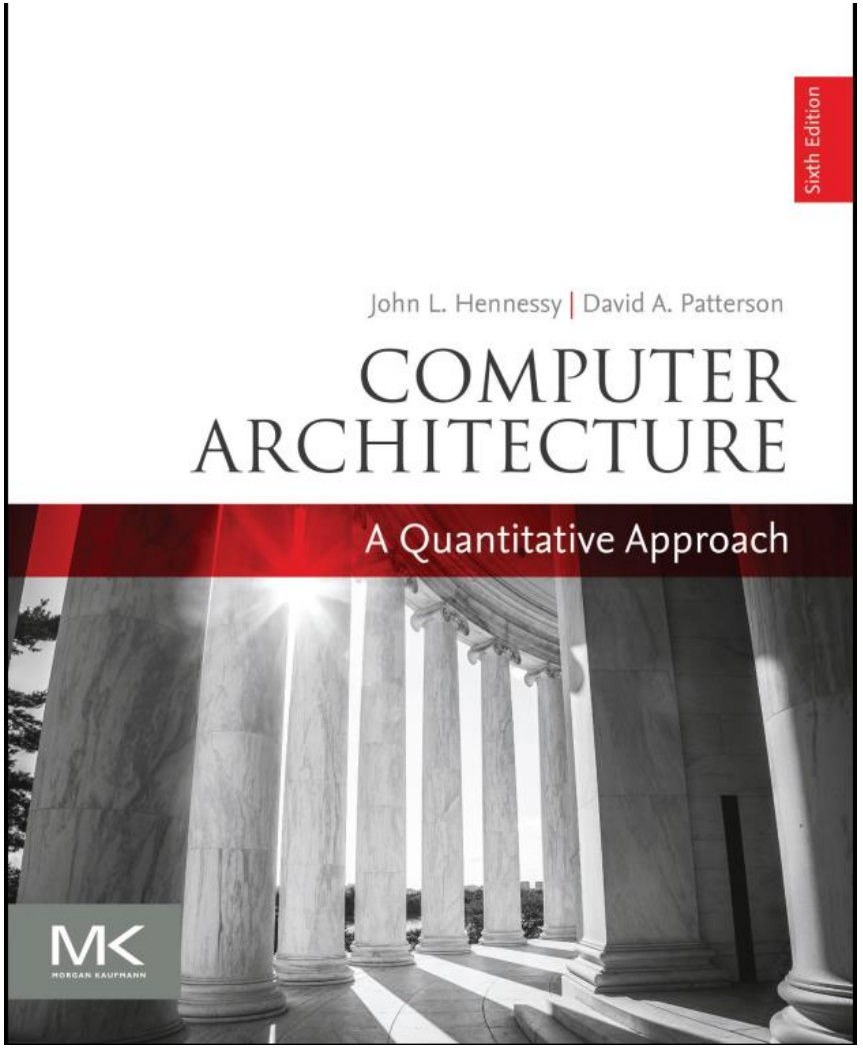
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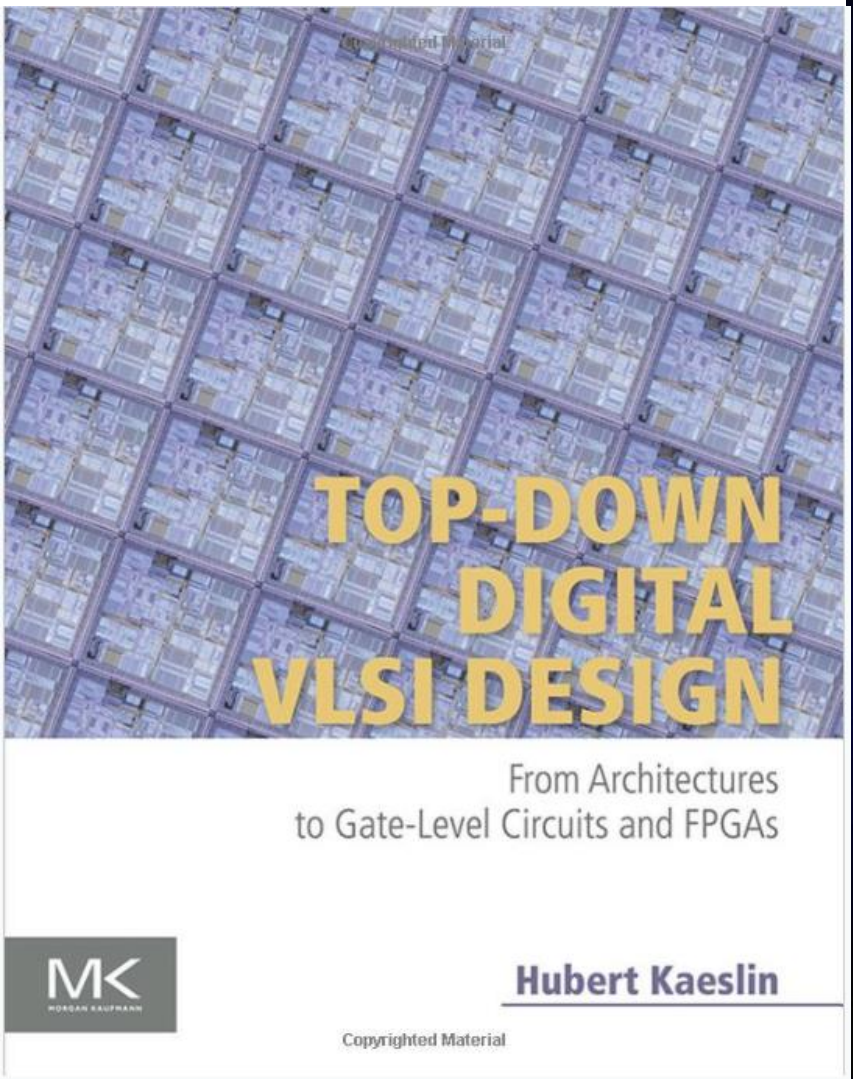
TOP-DOWN
DIGITAL
VLSI DESIGN
From Architectures
to Gate-Level Circuits and FPGAs
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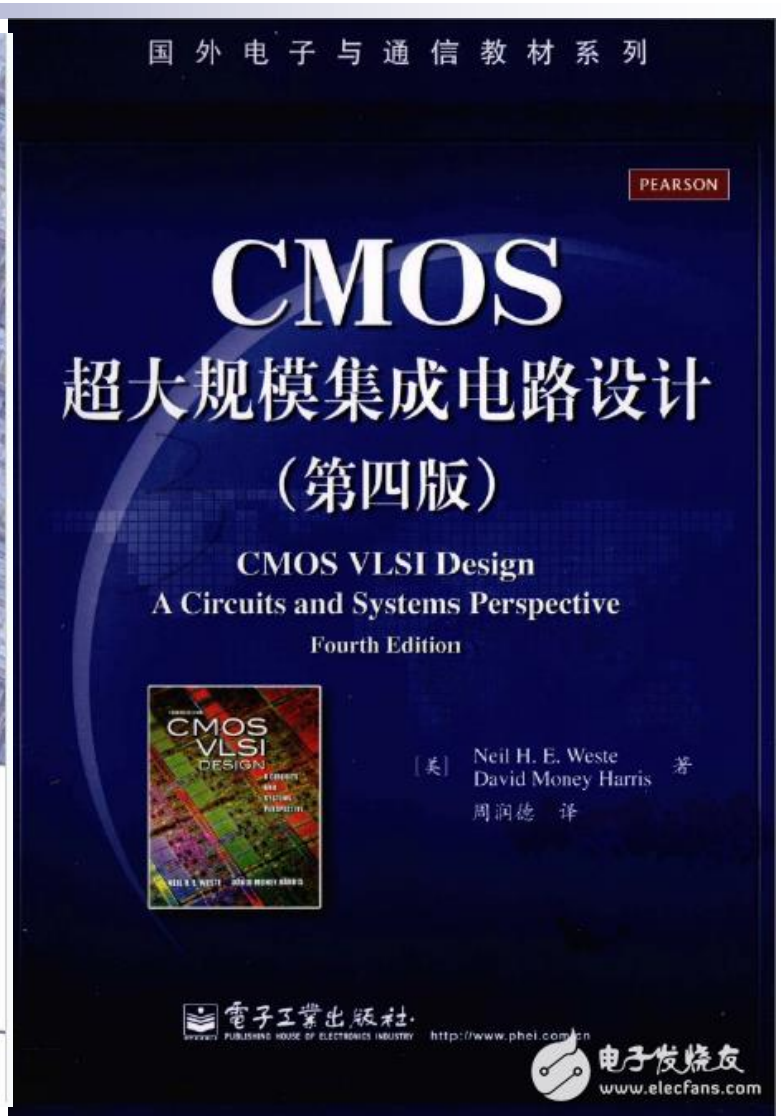
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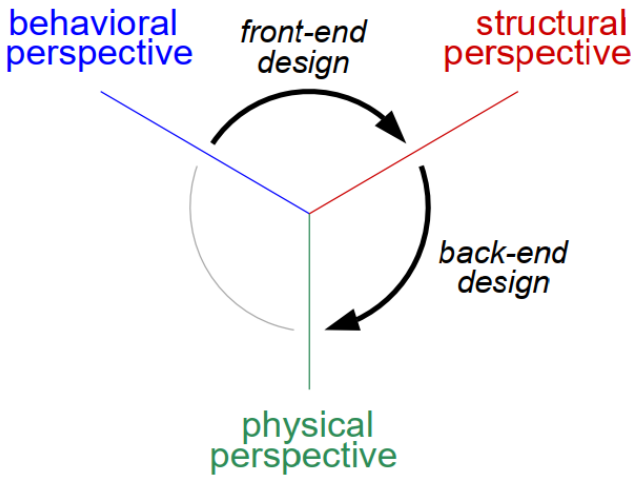
Chapter 0

VLSI Design Overview

The Concepts behind VLSI

- The economic impact of VLSI
- VLSI viewed from five different perspectives
  - Circuit complexity
  - Marketing
  - Fabrication
  - Design
  - Business



- Design flow in digital VLSI
  - Front-end (architecture and circuit design)
  - Back-end (layout design and verification)

Economic impact

- Worldwide semiconductor market by vendors

Semiconductors account for almost 0.55% of the world gross domestic product. (2018年全球GDP总量约为84.84万亿美元)

Table 1. Top 10 Semiconductor Vendors by Revenue, Worldwide, 2018 (Millions of U.S. Dollars)

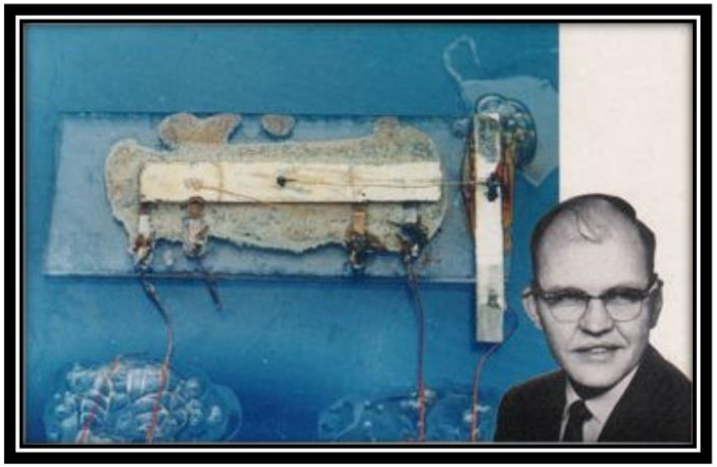
2018 Rank	2017 Rank	Vendor	2018 Revenue	2018 Market Share (%)	2017 Revenue	2017-2018 Growth (%)
1	1	Samsung Electronics	73,649	15.5	61,158	20.4
2	2	Intel	66,290	14.0	58,725	12.9
3	3	SK hynix	36,240	7.6	26,370	37.4
4	4	Micron Technology	29,742	6.3	22,895	29.9
5	6	Broadcom	16,261	3.4	15,405	5.6
6	5	Qualcomm	15,375	3.2	16,099	-4.5
7	7	Texas Instruments	14,593	3.1	13,651	6.9
8	11	ST Microelectronics	9,213	1.9	8,021	14.9
9	9	Western Digital	9,078	1.9	9,159	-0.9
10	10	NXP Semiconductors	9,022	1.9	8,746	3.2
		Top-10	**279,463**	**58.8**	**240,229**	**16.3**
		Others (outside Top 10)	**195,168**	**41.2**	**181,494**	**7.5**
		Total Market	**474,631**	**100.0**	**421,723**	**12.5**

Source: Gartner (April 2019)

Economic impact

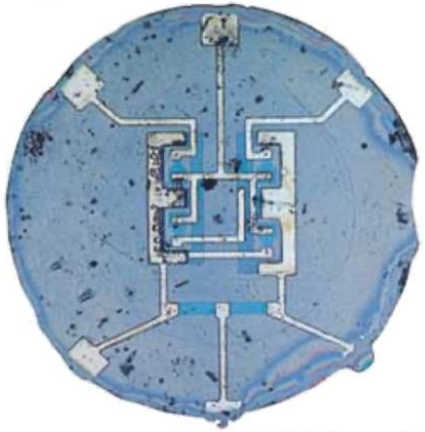
- Microelectronics drives the information age
  - Microelectronics has an enormous economic leverage as any progress there spurs innovations in " downstream" industries and services.
  - While computing, telecommunication, and entertainment products existed before the advent of microelectronics, today's information society would not have been possible without.
  - The almost total penetration has been made possible by a long-running drop of cost per function at a rate of 25 to 29% per year.

Economic impact

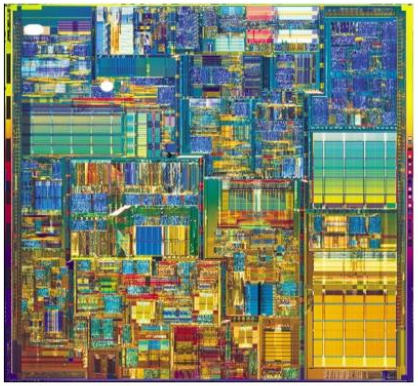


1958， Jack S. Kilby
Integrated Devices

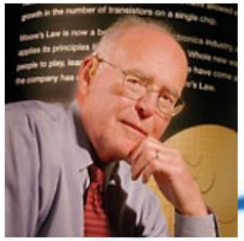
2000，J. Kilby, Nobel physics prize



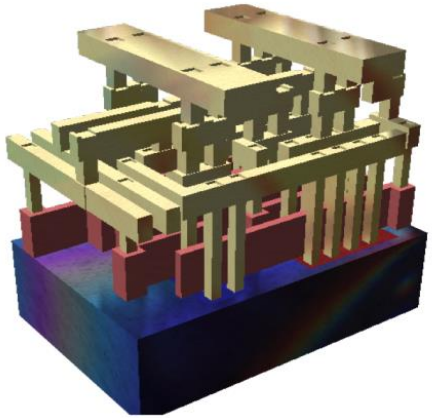
1959，R. Noyce
Integrated Devices with interconnect



Pentium IV



INTegrated ELectronics



VLSI viewed from 5 perspectives

Golden Moore & Von Neumann

戈登·摩尔 Golden Moore

Down Scaling 按比例缩小

P4004：1971年世界上第一个微处理器在英特尔公司诞生

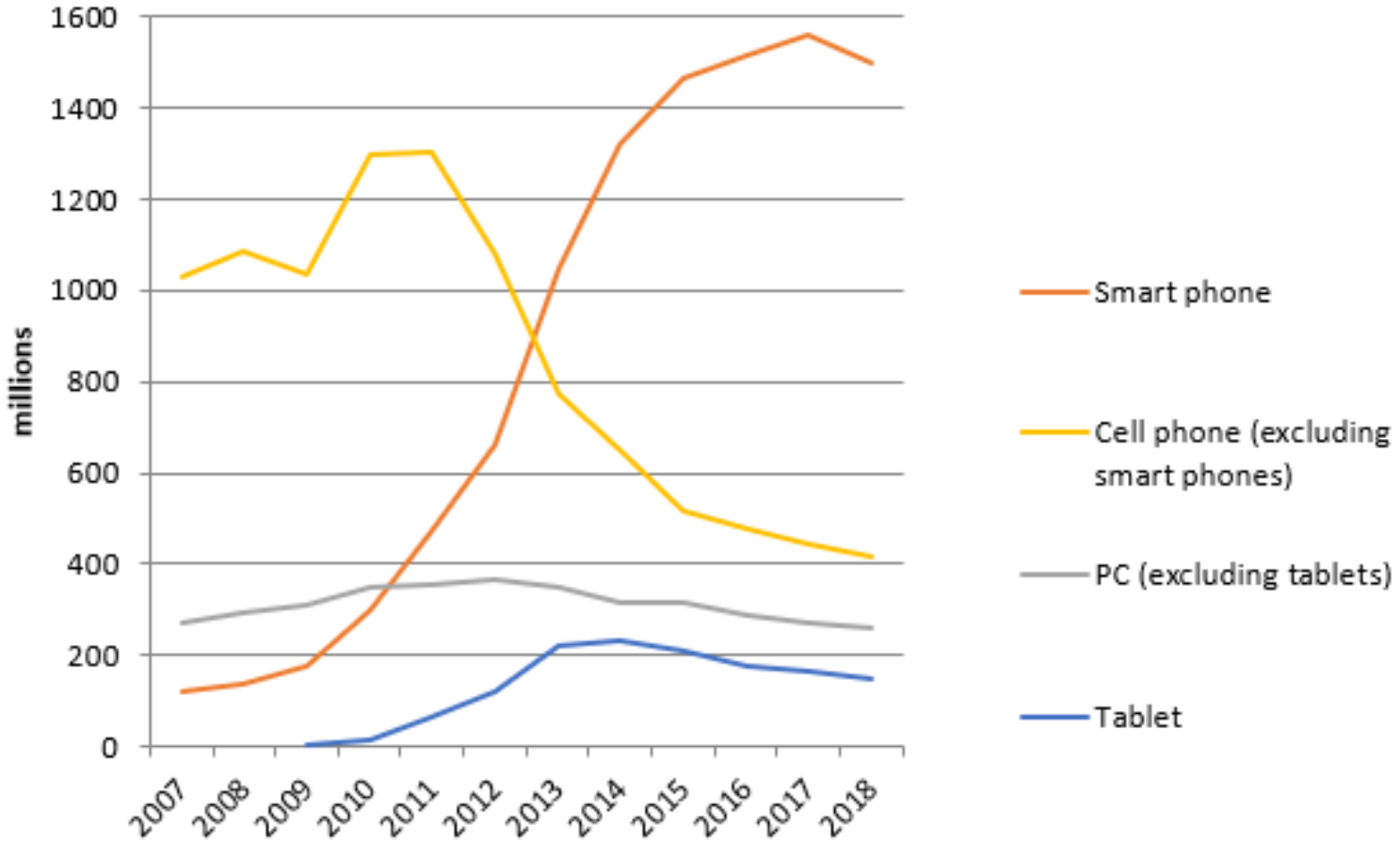
Von Neumann 约翰·冯·诺依曼

Von Neumann Architecture 冯·诺依曼 体系结构

Semiconductor (半导体)

Computer (计算机)

The PostPC Era



The PostPC Era

- Personal Mobile Device (PMD)
  - Battery operated
  - Connects to the Internet
  - Hundreds of dollars
  - Smart phones, tablets, electronic glasses
- Cloud computing
  - Warehouse Scale Computers (WSC)
  - Software as a Service (SaaS)
  - Portion of software run on a PMD and a portion run in the Cloud
  - Amazon and Google

The PostPC Era

Ubiquitous Integrated Circuits/Chips

Data Center, Server, Desktop, Laptop, Embedded Systems:
Microprocessor, GPU, ASIC, FPGA, Analog IC, RF IC etc.

VLSI viewed from 5 perspectives

- 1st perspective：Circuit complexity
- How large is that circuit?
  - Geometric chip size
  - Transistor count
  - Gate-equivalents
    - 1 GE —> 1 two-input nand —> 4 MOSFETs in static CMOS

Circuit complexity	GEs of logic + bits of memory
Small-scale integration (SSI)	1 ... 10
Medium-scale integration (MSI)	10 ... 100
Large-scale integration (LSI)	100 ... 10 000
Very-large-scale integration (VLSI)	10 000 ... 1 000 000
Ultra-large-scale integration (ULSI)	1 000 000 ...

VLSI viewed from 5 perspectives

- A logic family is a collection of digital subfunctions that
  - assemble to arbitrary logic, arithmetic and storage functions
  - are compatible among themselves electrically
  - share a common fabrication technology

Acronym	Meaning
MOS	Metal Oxide Semiconductor
FET	Field Effect Transistor (n- or p-channel)
BJT	Bipolar Junction Transistor (npn or pnp)
CMOS	Complementary MOS (circuit or technology)
static CMOS	data stored in bistable subckts and retained indefinitely
dynamic CMOS	data stored as electrical charges to be refreshed

VLSI viewed from 5 perspectives

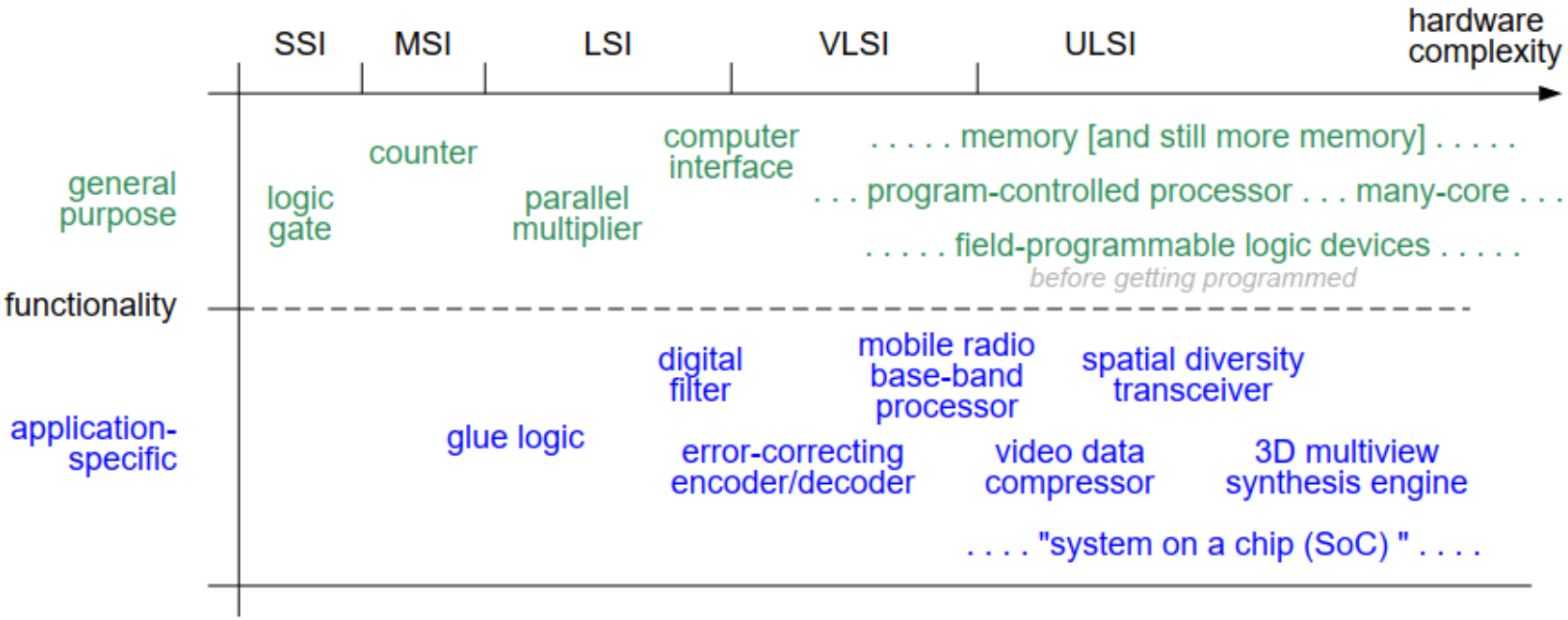
- 2nd perspective：Marketing
- How do functionality and target markets relate to each other?
- General-purpose IC：Either very simple or of generic functionality.
  - simple: gates, flip-flops, counters, adders, etc.
  - generic: RAMs, ROMs, microcomputers, many DSPs, etc.

VLSI viewed from 5 perspectives

- 2nd perspective：Marketing
- Application-specific integrated circuit (ASIC)
  - Application-specific standard product (ASSP):
    - designed for a specific task and sold to various customers. Examples: graphics accelerators, cellular radio chip sets, smart card chips, etc.
  - User-specific integrated circuit (USIC):
    - designed and produced for a single company.
    - Examples: Apple A4,5,6,... SoC introduced with the iPad, various audio processors for hearing aids.

VLSI viewed from 5 perspectives

- Circuit complexity
- Functionality



VLSI viewed from 5 perspectives

- 3rd perspective: Manufacturing

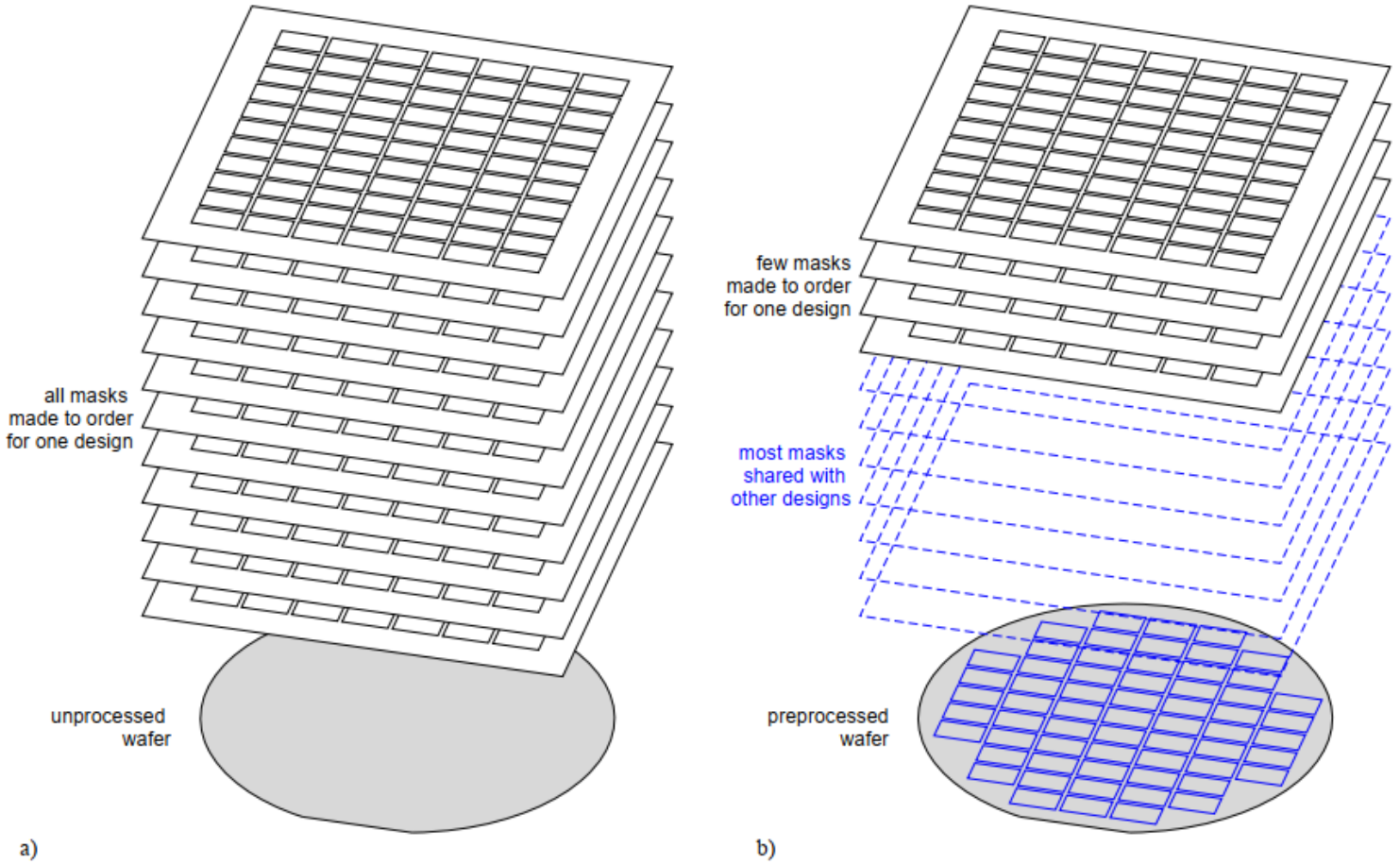


Figure: Full-custom (a) and semi-custom (b) masks sets compared.

VLSI viewed from 5 perspectives

- 3rd perspective: Manufacturing
- Full-custom IC All fabrication layers, full set of photomasks.
- Semi-custom IC (gate array, sea-of-gates, structured ASIC). A few metal layers only, subset of photomasks.
- Field-programmable logic (SPLD, CPLD, FPGA). Customization occurs electrically, no masks involved.

VLSI viewed from 5 perspectives

The different ages of Scaling (different methods for different times)

- **I. Geometrical Scaling (1975-2002)**
  - Reduced horizontal and vertical physical dimensions
  - Improved performance of planar transistors.
- **II. Equivalent Scaling (2003-2024)**
  - Reduced horizontal (only) dimensions
  - New materials and new physical effects
  - New vertical structures instead of the planar transistors
- **III. 3D Power Scaling (2025-2040)**
  - Transition to complete vertical device structures
  - Heterogeneous integration
  - Reduced power consumption

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view I
- Which levels of detail are being addressed during a part's design?
  - Hand layout：Desired geometric shapes manually drawn to scale.
    - + optimum density, performance and device matching.
    - − slow, cumbersome, and prone to errors.

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view I
- Which levels of detail are being addressed during a part's design?
  - Cell-based design by means of schematic entry：Manual drawing of cell-level circuits followed by automatic place & route.
    - Standard cells: small universal building blocks, preestablished layout, fully characterized. Examples: logic gates, flip-flops, adder slices, etc.

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view I
- Which levels of detail are being addressed during a part's design?
  - Cell-based design by means of schematic entry：Manual drawing of cell-level circuits followed by automatic place & route.
    - Megacells: much larger size and complexity than standard cells. Examples: microprocessor cores and peripherals, A/D and D/A converters.

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view I
- Which levels of detail are being addressed during a part's design?
  - Cell-based design by means of schematic entry: Manual drawing of cell-level circuits followed by automatic place & route.
    - Macrocells: layout put together on a per case basis according to specs from a limited collection of layout tiles. Examples: RAMs and ROMs.

VLSI viewed from 5 perspectives

TABLE 14.3 Typical standard cell library

Gate Type	Variations	Options
Inverter/Buffer/ Tristate Buffers		Wide range of power options, 1x, 2x, 4x, 8x, 16x, 32x, 64x minimum size inverter
NAND/AND	2–8 inputs	High, normal, low power
NOR/OR	2–8 inputs	High, normal, low power
XOR/XNOR		High, normal, low power
AOI/OAI	21, 22	High, normal, low power
Multiplexers	Inverting/noninverting	High, normal, low power
Adder/Half Adder		High, normal, low power
Latches		High, normal, low power
Flip-Flops	D, with and without synch/asynch set and reset, scan	High, normal, low power
I/O Pads	Input, output, tristate, bidirectional, boundary scan, slew rate limited, crystal oscillator	Various drive levels (1–16 mA) and logic levels

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view II
- Automatic circuit synthesis
  - Logic synthesis: accepts logic equations, truth tables, and state graphs; generates gate-level netlists for combinat. logic and for finite state machines (FSM) —> absorbed in today's EDA flows.

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view II
- Automatic circuit synthesis
  - Register transfer level (RTL) synthesis:
    - Circuit viewed as a network of storage elements — registers and also RAMs — held together by combinational logic.
    - Behavioral specs allowed to include arithmetic functions, string operations, arrays, enumerated types, etc.
- Technology-independent, supports parametrization —> favors reuse.

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view III
- Architecture synthesis Starts from a purely algorithmic description. Source code includes no explicit indications for how to marshal data processing operations and hardware resources.

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view III
- Architecture synthesis
  - 1. Identify the computational and storage requirements.
  - 2. Select a suitable building block for each processing and storage operation.
  - 3. Establish a cycle-based schedule for carrying out the algorithm.
  - 4. Decide on a hardware organization able to execute the resulting work plan.

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view III
- Architecture synthesis
  - 5. Keeping track of data moves and operations for each clock cycle, translate into the necessary instructions for RTL synthesis.

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view III
- Architecture synthesis
  - —> Formidable optimization problem. Pros and cons:
    - + Rapid exploration of design space. Good results in specialized areas.
    - − Does not normally yield optimal results for arbitrary applications.
    - Expertise in architecture design and RTL coding still appreciated.

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view IV
- Design with virtual components VCs (aka intellectual property modules or cores) are HDL synthesis packages made available to others on a commercial basis.

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view IV
- Design with virtual components
  - Vendor develops a major function into a synthesis model for sale.
  - Licensee buys VC, incorporates it into his design, then carries out all the rest (synthesis, place & route, and overall verification).

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view IV
- Design with virtual components
  - VCs are portable across fabrication technologies (soft modules), standard/macro/megacells are process-specific (hard modules).
  - Most VCs implement fairly common subfunctions, parametrization is sought to cover more applications.

VLSI viewed from 5 perspectives

- 4th perspective: The design engineer's point of view IV
- Design with virtual components
  - Examples: processor cores, all sorts of filters, audio and/or video en/decoders, cipher functions, error correction en/decoders, USB, FireWire, and other interfaces.

VLSI viewed from 5 perspectives

- Options for capturing a design with EDA tools: (Two or three approaches are typically combined.)
  - Hand layout: Confined to niches (such as memories, analog subcircuits, library cells, and high-performance datapaths).
  - Schematic entry: Important at its time, largely confined to analog circuit design today.

VLSI viewed from 5 perspectives

- Options for capturing a design with EDA tools: (Two or three approaches are typically combined.)
  - RTL synthesis: VHDL or SystemVerilog code automatic $\overset{automatic}{\longmapsto}$ gate-level netlist. Universally adopted.
  - Architecture synthesis: SW code $\overset{automatic}{\longmapsto}$ RTL synthesis model. Research goal, viable for specific fields of applications.
  - Incorporation of VCs: Purchased HDL code automatic $\overset{automatic}{\longmapsto}$ gate-level netlist. Routine practice today.

VLSI viewed from 5 perspectives

- A second IC classification scheme
  - Fabrication depth
  - Level of abstraction for design entry.

Fabricat. depth	Electrical configuration	Semi-custom fabrication	Full-custom fabrication	
Design level	Cell-based as obtained from ○ synthesis with VCs in HDL form, ○ synthesis from captive HDL code, ○ schematic entry, or a mix of these			Hand layout
Product name	Field-programmable logic device (FPGA, CPLD)	Gate-array, sea-of-gates, or structured ASIC	Standard cell IC	Full-custom IC

VLSI viewed from 5 perspectives

- Competitive pressure has incited the industry to look at design automation from a wider perspective
  - Correct-by-construction methodology by supporting progressive refinement starting with a virtual prototype.
  - Explore the architectural solution space more systematically and more rapidly than with RTL synthesis.
    - LISA, high-level synthesis from SystemC, etc.

VLSI viewed from 5 perspectives

- Competitive pressure has incited the industry to look at design automation from a wider perspective
  - Make it possible to start software development before hardware design is completed.
  - Improve the coverage and efficiency of functional verification.
    - deal with system-level transactions
    - take advantage of formal verification
    - e, PSL, Vera SystemVerilog

VLSI viewed from 5 perspectives

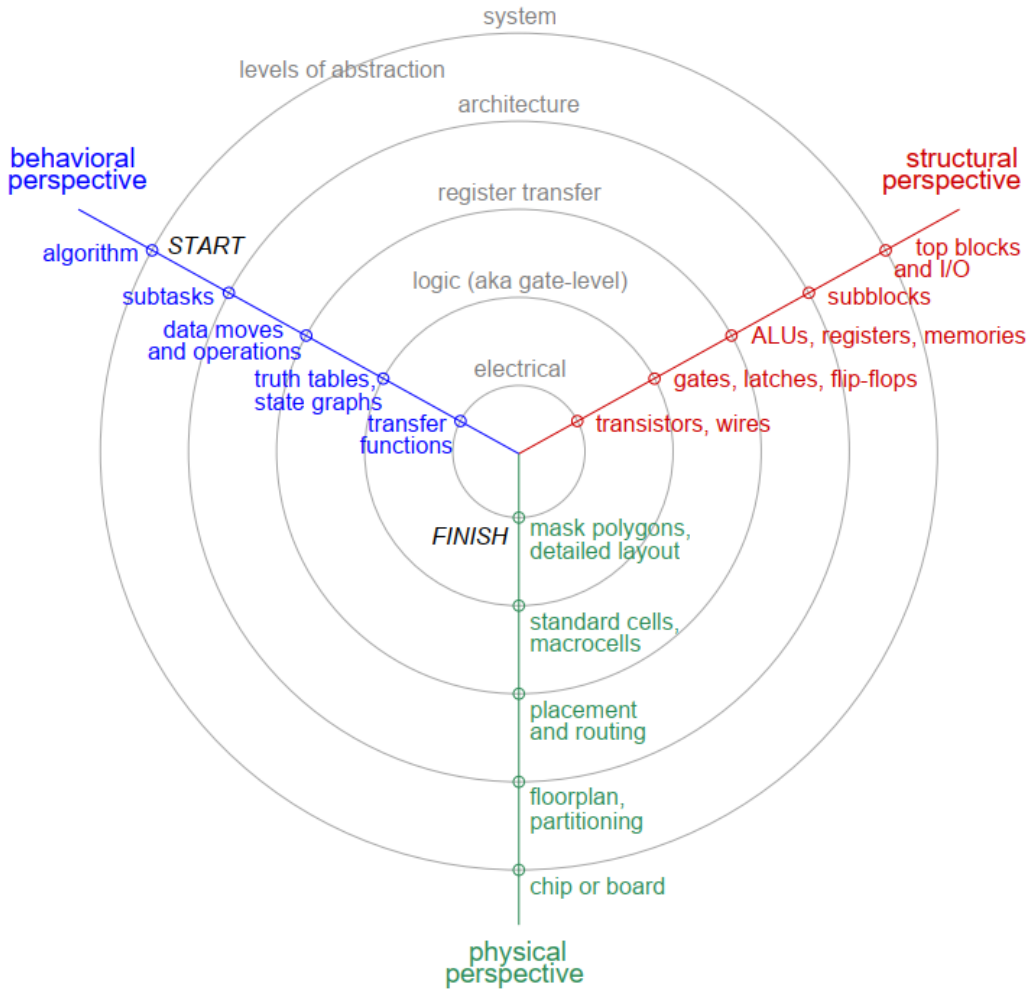
- 5th perspective: Business models
- Players in semiconductor markets
  - Integrated device manufacturer (IDM) : Intel
  - Silicon foundry : TSMC
  - Fabless chip vendor: Qualcomm
  - Fab-lite chip vendor : Luxtera
  - Intellectual property (IP) vendor : ARM
  - System house : Apple

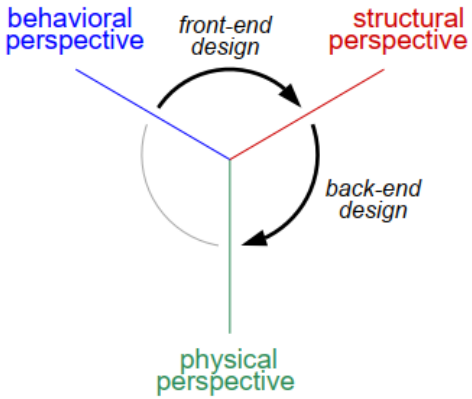
VLSI viewed from 5 perspectives

- 5th perspective: Business models
- What has made these new business models possible?
- Three factors came together to make fabless operation possible:
  - Generous integration densities at low costs.
  - Proliferation of high-performance engineering workstations and EDA software
  - Availability of know-how in VLSI design outside IC manufacturing companies. (This is where this course comes in.)

The VLSI design flow

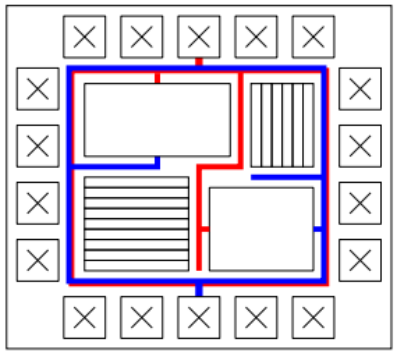
The Y-chart





The VLSI design flow

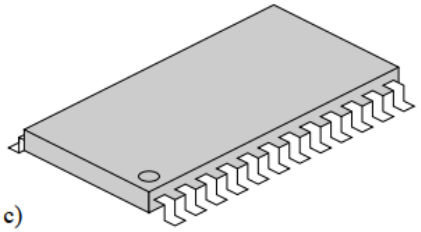
More design views



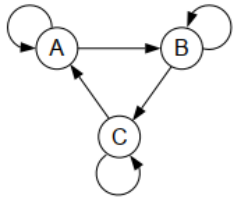
a)

```
architecture seriesexpansion of cosine is
begin
  process (theta) is
    variable sum, term : real;
    variable n : natural;
  begin
    sum := 1.0;
    term := 1.0;
    n := 0;
    while abs term > abs (sum / 1.0E6) loop
      n := n+2;
      term := (-term)*theta**2 / real(((n-1)*n));
      sum <= sum+term;
    end loop;
    result <= sum;
  end process;
end architecture seriesexpansion;
```

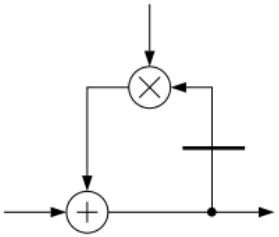
b)



c)

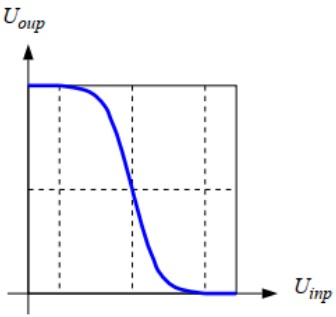


state graph
(models reactive behavior)

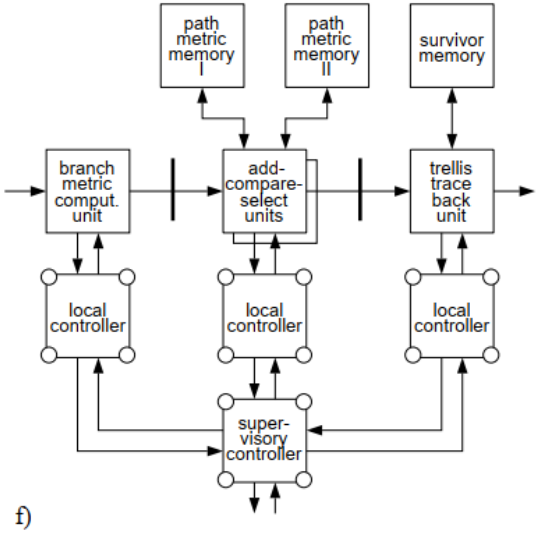


data dependency graph
(models transformatorial behavior)

d)



e)



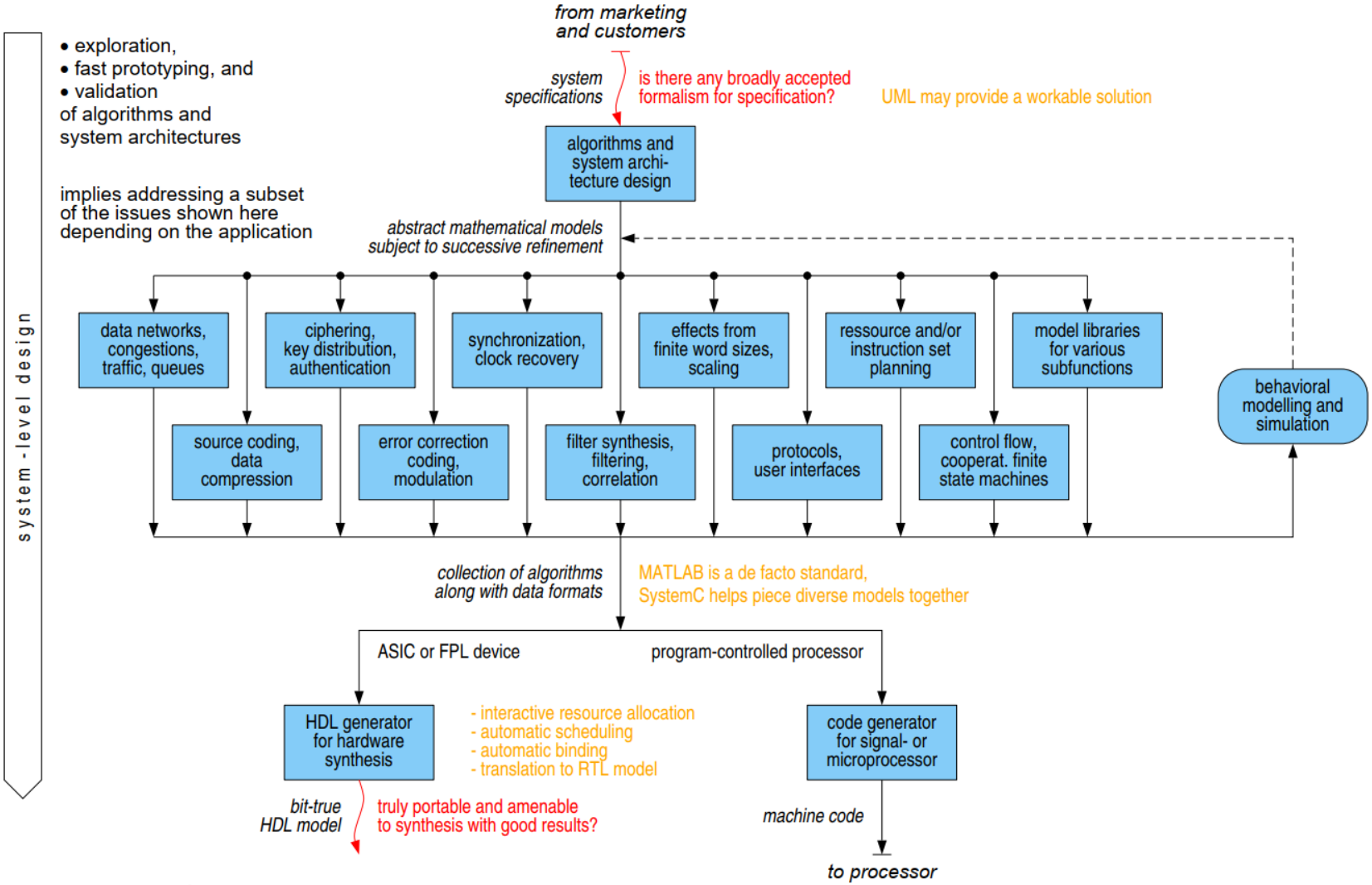
f)

Figure: Floorplan (a), software model (b), encapsulated chip (c), graphical formalisms (d), transfer characteristic (e), and block diagram (f) (simplified).

System-level design

- Decisions taken at this stage determine the final outcome more than anything else:
  - Specify the functionality and characteristics of the system to be
  - Partition the system's functionality into subtasks
  - Explore alternative hardware and software tradeoffs
  - Decide on make or buy for all major building blocks
  - Decide on interfaces and protocols for data exchange
  - Decide on data formats, operating modes, exception handling, etc.
  - Define, model, evaluate and refine the various subtasks
- Result: System-level model.

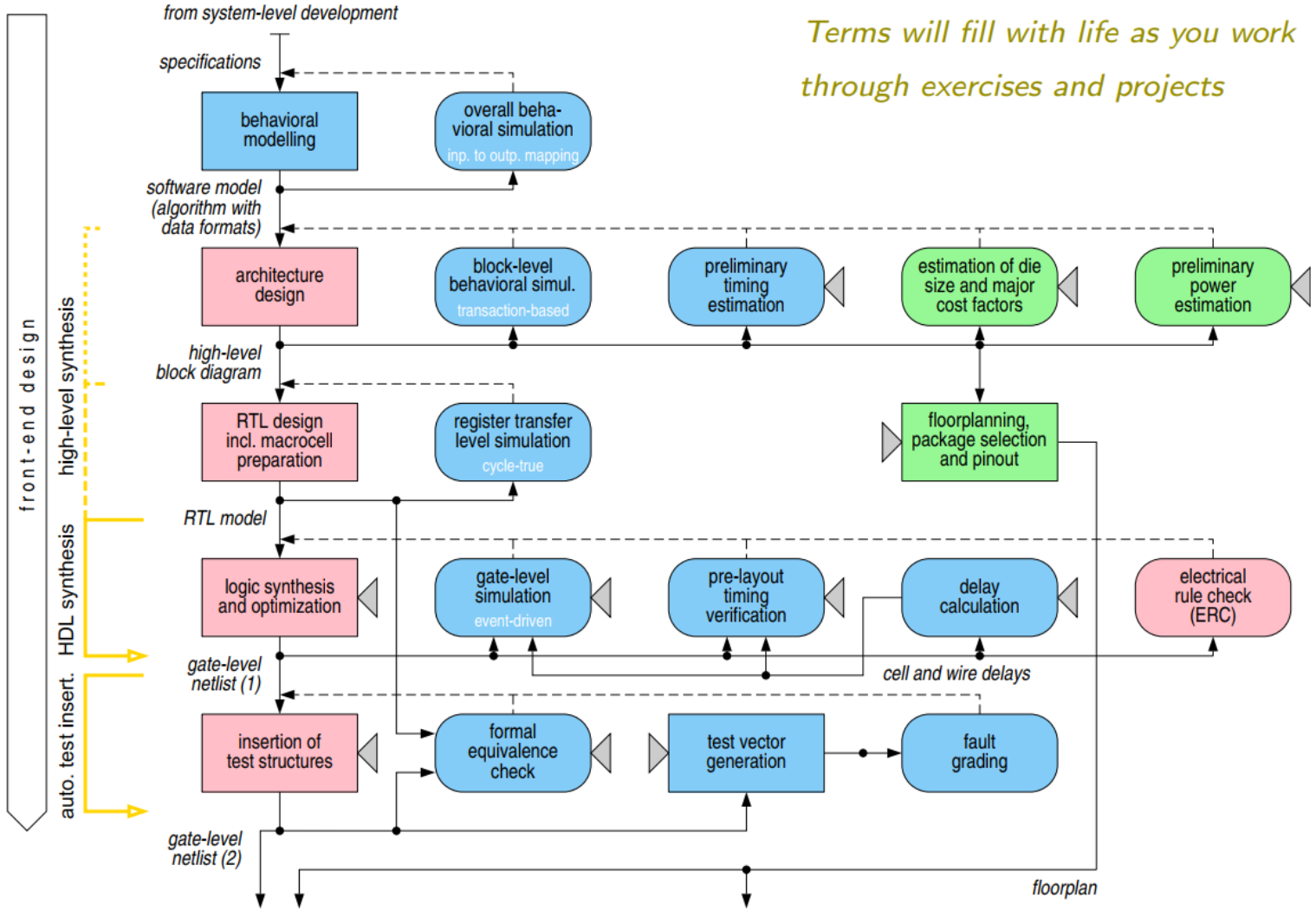
System-level design flow



Algorithm design

- Streamline computations in view of their implementation in hardware:
  - Cut down computational burden and memory requirements
  - Find compromises between computational complexity and accuracy
  - Contain effects due to finite word-length computation
  - Decide on number representation schemes
  - Evaluate alternatives and selecting the one best suited
  - Quantify the minimum required computational resources
- Result: Bit-true software model.

VLSI design flow - Front-end



Architecture design I

- Take important high-level decisions:
  - Partition a computational task in view of a hardware realization.
  - Organize the interplay of the various subtasks.
  - Allocate hardware resources to each subtask. 7! allocation
  - Define datapaths and controllers.
  - Decide between off-chip RAMs, on-chip RAMs, and registers.
  - Decide on communication topologies and protocols (parallel, serial).
  - Define how much parallelism to provide in hardware.
  - Decide where to opt for pipelining and to what degree.
  - Decide on a circuit style and fabrication process.
  - Get a first estimate of the circuit's size and cost.
- Results: High-level block diagram and preliminary floorplan.

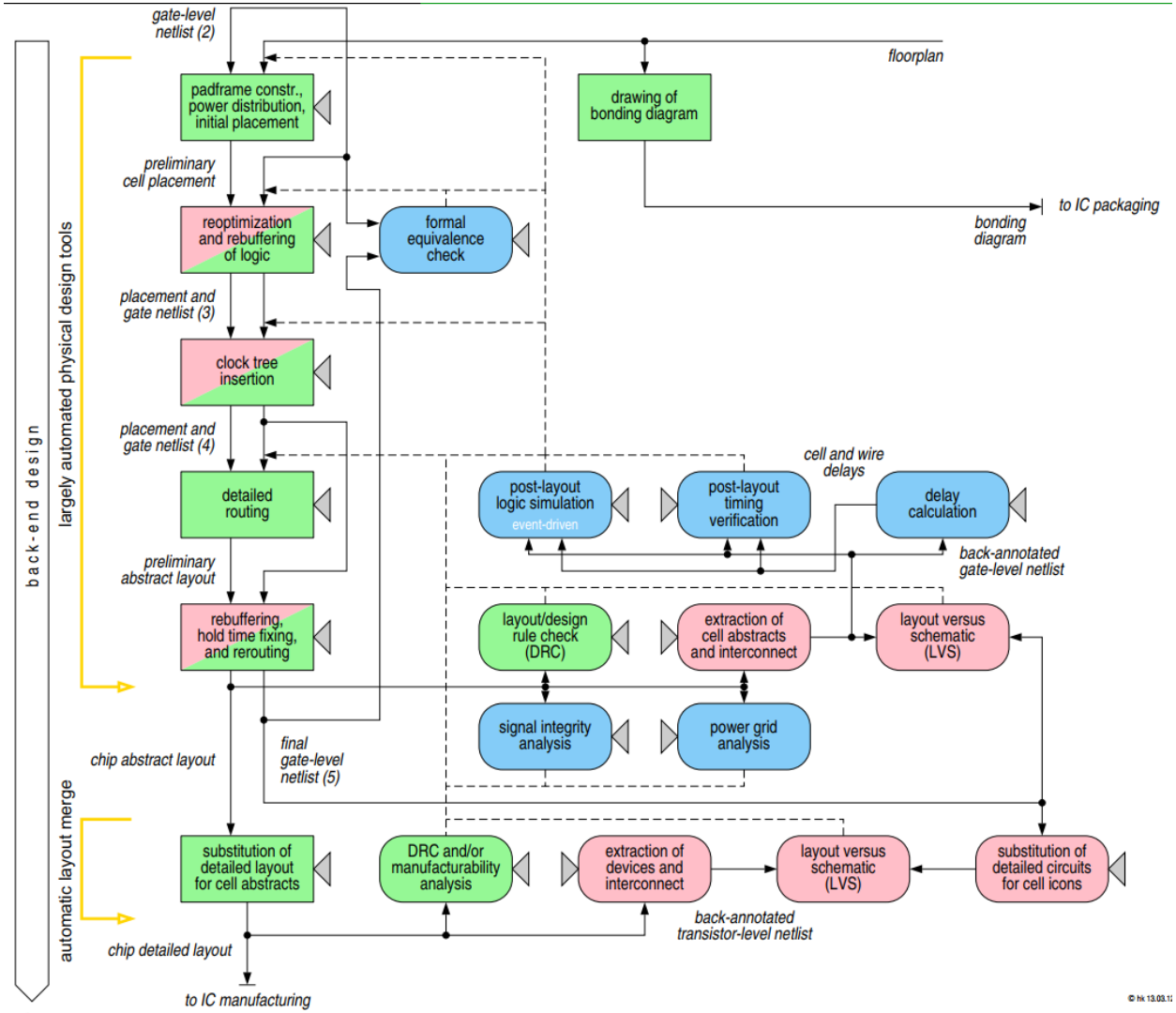
Architecture design II

- Work out lower-levels details of an architecture by deciding:
  - How to implement arithmetic and logic units?
  - Whether to use hardwired logic or microcode for a controller?
  - When to use a ROM rather than random logic?
  - What operations to perform during which clock cycle? 7! scheduling
  - What operations to carry out on which processing unit? 7! binding
  - What clocking discipline to adopt?
  - What time interval to use as the basic clock period?
  - Where to prefer a bidirectional bus over a unidirectional one?
  - How to control the access to a bus with multiple drivers?

Architecture design II

- Work out lower-levels details of an architecture by deciding:
  - By what test strategy to ensure testability?
  - How to initialize the circuit?
- Results: Set of more detailed diagrams and verified RTL code.

VLSI design flow - Back-end



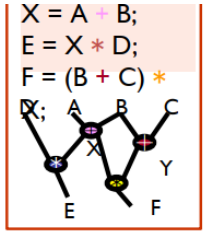
Physical design

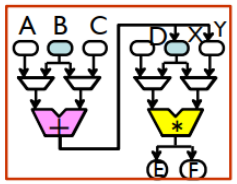
- Steps:
  - Floorplanning (begins during front-end design)
  - Padframe generation and power distribution
  - Intial placement of cells
  - Reoptimization and rebuffering
  - Clock tree insertion
  - Detailed routing
  - Rebuffering and hold time fixing
  - Chip assembly (global routing, padframe generation, etc.)
  - Substitution of detailed layout for cell abstracts
- Result: Polygon layout data for mask preparation (GDS II)

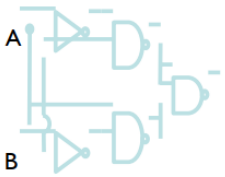
Physical design verification

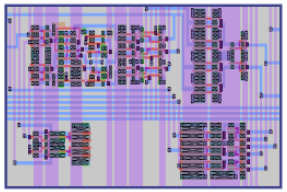
- Prior to fabrication, all layout data need to be checked to protect against fatal mishaps. The set of instruments available includes:
  - Check conformity of layout with geometric rules (DRC)
  - Search for patterns likely to be detrimental to yield
  - Layout extraction (re-)obtains the actual circuit netlist
  - Layout-versus-schematic (LVS)
  - Post-layout timing verification
  - Post-layout simulation
- Result: Either proof of geometric integrity or error list.

IC design flow









System/Behavioral Descriptions

High-level Synthesis
高层次综合

- Scheduling;
- Binding;
- Allocation.

Register Transfer Level Descriptions

Logic Synthesis
逻辑综合

- Logic Optimization;
- Technology Mapping.

Gate Level Netlist

Physical Synthesis
物理综合/芯片布图

- Floorplanning
- Placement;
- Routing;
- etc.

Layout mask

Design Automation

The leitmotiv of VLSI design

- Common theme throughout the design flow: Many analysis steps and corrective loops (rounded boxes, backward arrows).
- Any design flaw found after tapeout or, even worse, after prototype fabrication wastes important amounts of time and money.
- Redesigns are so devastating that the entire semiconductor industry is committed to: " First time right" design is the guiding principle.
- VLSI engineers typically spend much more time verifying a circuit than actually designing it.