Xinlong Wu

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wulongxin.com github.com/Xinlong-Wu

Summary

Information Technology student with background in Computer Sciences(Compiler). Strong technical proficiency with work history in Compiler and OpenSource Community. In-depth knowledge of RISCV Architecture. Also has experience in Web front-end/back-end and game development. Have used build tools such as Make/CMake/Ninja Proficiency in using common Linux command line commands such as grep / kill / man. Self-directed Work Study Student motivated to apply education and experience in job role. Excellent listener comfortable completing various tasks to keep operations running smoothly. Dedicated to continuous improvement and building career foundation. Offers strong administrative, time management and multitasking skills.

Education

Master of Computing (Advanced) 2023.07 - 2024.12
ANU

Bachelor of Information Technology 2019.07 - 2022.12
Royal Melbourne Institute of Technology (RMIT)

Internship

Lixiang Auto Driving 2024.12 - Present
AI Compiler Intern

PLCT Lab, Institute of Software, Chinese Academy of Sciences 2020-01 - 2024.11
Internship Student

- Involved in the development and contribution of the LLVM compiler
- Implementing the scalar crypto extension for LLVM (one of the patchs)
- Implementing the code size reduction extension for LLVM
- Porting DotNet Mono JIT to run at RISC-V Arch

Project And Activities

MonoJIT RISC-V Porting 2022.12
PLCT Lab

- Porting DotNet Mono JIT to run at RISC-V Arch
- submit code to upstream

Game Design & Develop 2023.07 - 2023.11
ANU Course

- Design a Jumping Game
- Build 3D Modules

RISC-V Code Size Reduction extension for LLVM 2022.01 - 2023.05
PLCT Lab

- Implement Machine Code layer of LLVM for Zc-ext
- Adjust stack order for posh/pop Inst
- Compress insts to their corresponding Zc insts

Publications

- RISC-V Load/store Instruction Reduction Based on Linker Relaxation. 10.15888/j.cnki.csa.008841

Related Links

- Personal Websites(Chinese): www.wulongxin.com
- Github: github.com/Xinlong-Wu

CPU Core Designer 2022.03 - 2022.08

Yi Sheng Yi Xin

- Implementing a simple simulator for the RISCV architecture
- Designing IP Cores with chisel and verifying them with verilator
- Verify chip logic with DiffTest

RISC-V Scalar Crypto extension for LLVM 2021.1 - 2021.12

PLCT Lab

- Implement Machine Code layer of LLVM for K-ext
- Implement Intrinsic function of LLVM for K-ext
- Implement C header file of LLVM for K-ext

Organiser (Question Maker) 2020.04 - 2020.06

2020 Guangdong-Macao CPC Programming Competition (Online Competition)

- Preparing the program running environment of competition
- Preparing questions for competitions
- Answering questions from participants during the competition
- Post answers after the competition

Skills

- Programming Languages: C/C++、Python、JavaScript、Java、C#
- Compiler Technology: clang、LLVM、GDB、LLD
- Simulator/Emulator: QEMU、Spike
- HardWare Tech: Digital and Analog Circuits、Verilog、Chisel
- LaTeX
- Verbal and Written Communication
- Teamwork and Collaboration
- Print Production
- Multitasking and Organization
- Telephone Etiquette
- Fast Learner
- Correspondence Writing
- Public Speaking