

## Zcmd v0.1

This document is in the Development state. Assume everything can change. For more information see: <https://riscv.org/spec-state>

RV32	RV64	Mnemonic	Instruction
!	!	cm.decbnez t0, imm	<a href="#">cm.decbnez: Decrement and branch, 16-bit encoding</a>

# cm.decbnez: This is in the *development* phase, for benchmarking and prototyping only

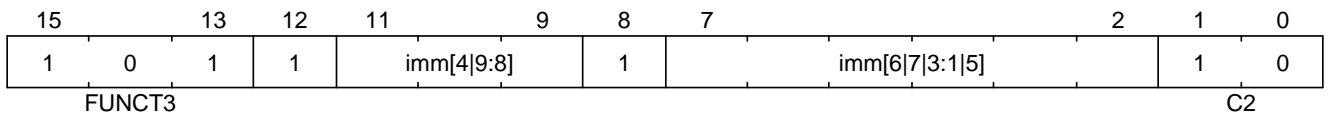
## Synopsis

Decrement and branch, 16-bit encoding

## Mnemonic

cm.decbnez *t0*, *offset*

## Encoding (RV32, RV64)



NOTE

In the current proposal only *t0* can be decremented, future versions may allow more registers

## Description

This instruction decrements *t0*, and increments the PC by the sign extended immediate if *t0* is zero after the decrement.

## Prerequisites

C or Zca

## 32-bit equivalent

None

## Operation

```
//This is not SAIL, it's pseudo-code. The SAIL hasn't been written yet.

t0 = 5;
X(t0) = X(t0) -1;
if (X(t0)==0) PC+=sext(imm); else PC+=2;
```

## Included in

Extension	Minimum version	Lifecycle state
Zcmd ( <a href="#">Zcmd v0.1</a> )	0.1	Development