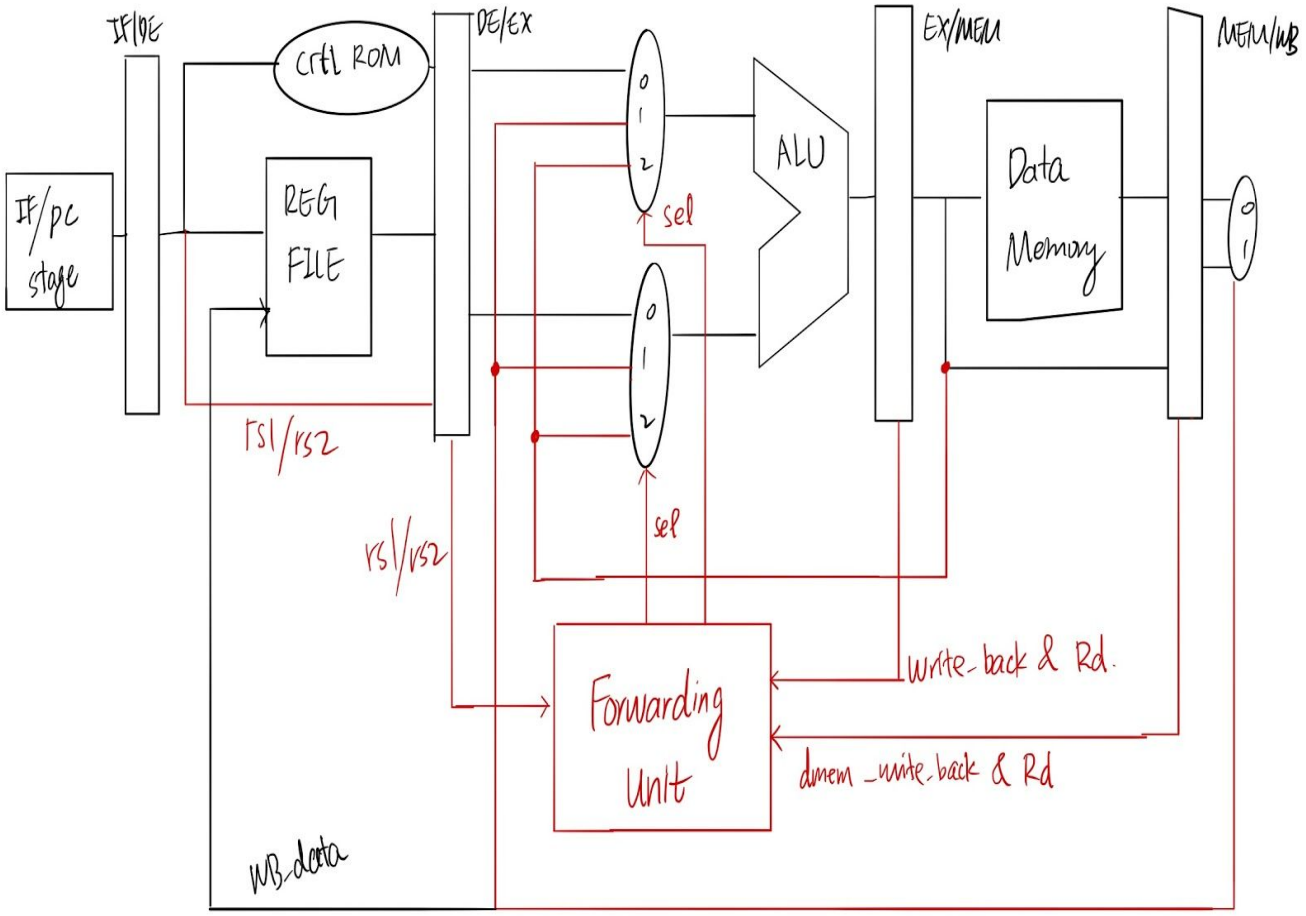
Hazard detection

1. WB.dr == ID.sr: WB to ID forwarding
2. WB.dr == EX.sr: WB to EX forwarding
3. MEM.dr == EX.sr: MEM to EX forwarding

Diagram:



Notes:

1.There are two *write_back & rd* wire which is from *reg-reg* operation and data memory operations.

2.*RS1/RS2* information is got from IR_data.

3. The diagram has overall been simplified

Forwarding logic:

```
module fwd (
        input logic write,
        input logic [4:0] rs,
        input logic [4:0] rd,
        output logic forward
);

always_comb begin
        if (write == 1  && rs==rd && rs!=0 && rd!=0)
                forward = 1;
        else
                forward = 0;
end
```