EL 6463 – Homework 2

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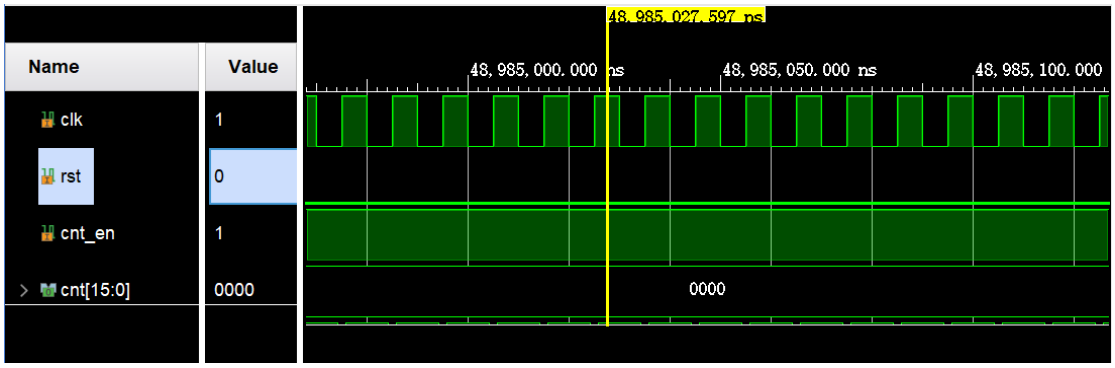
Link to the video:
https://drive.google.com/file/d/1k1Cl0AqQf0EhzrTYzOGWji9lVgErfbSA/view?usp=sharing

Task1: design

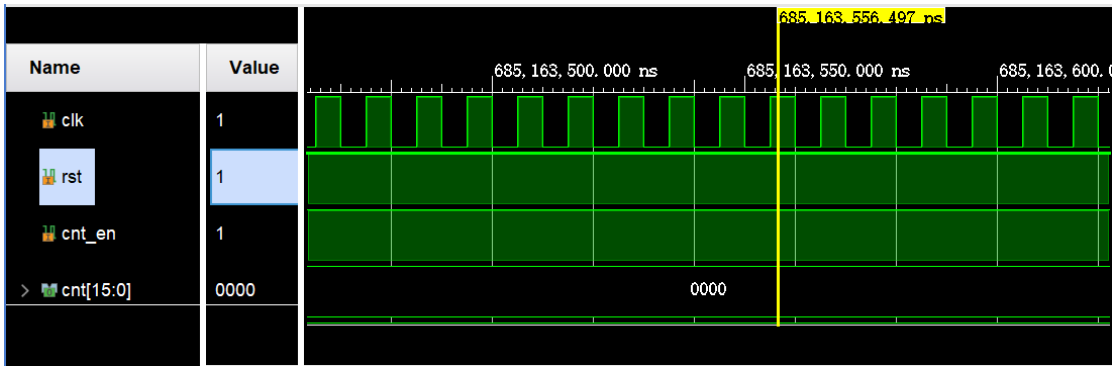
Because the speed of 16bit counter is too fast, the change of counter cannot be seen from the change of LED, so in this project, the last 16 bits of a 42bit counter are intercepted to control the blinking of LED.

Task 2: functional simulation of each of the 2 counters

- **functional simulation of the CounterA: Verilog, Counts UP**
  case 1:
  clk: 100MHz, rst=0, cnt_en=1

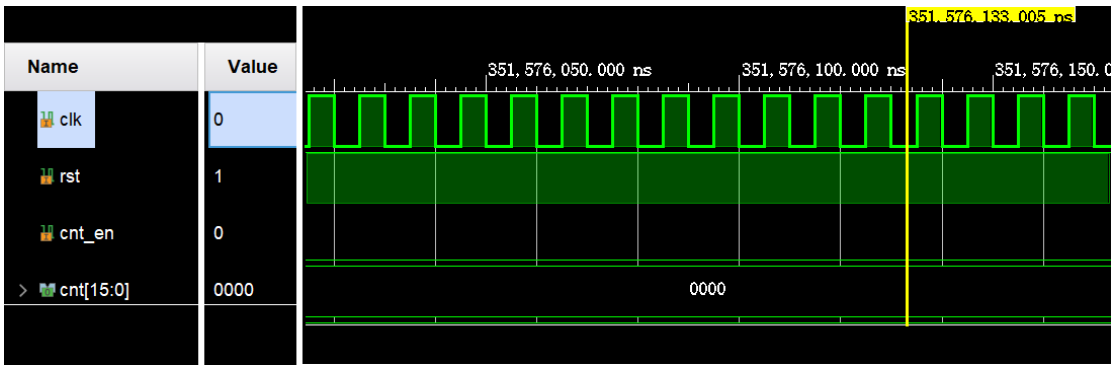


  case 2:
  clk: 100MHz, rst=1, cnt_en=1



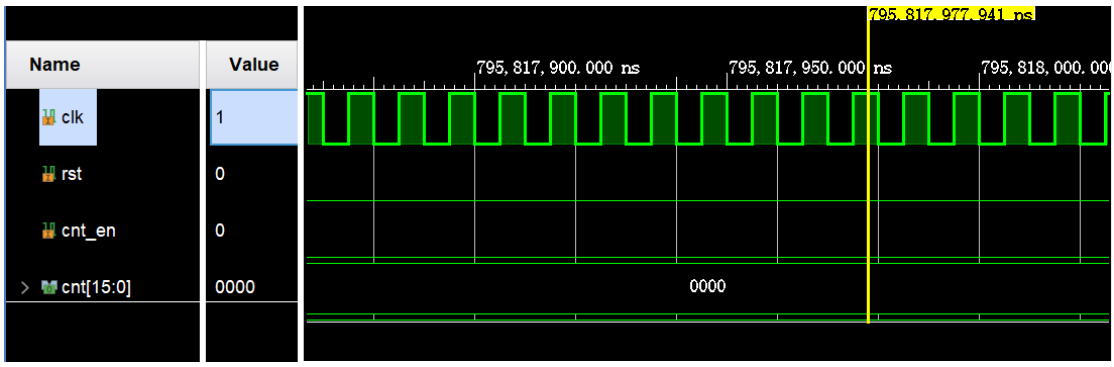
case 3:

clk: 100MHz, rst=1, cnt_en=0



case 4:

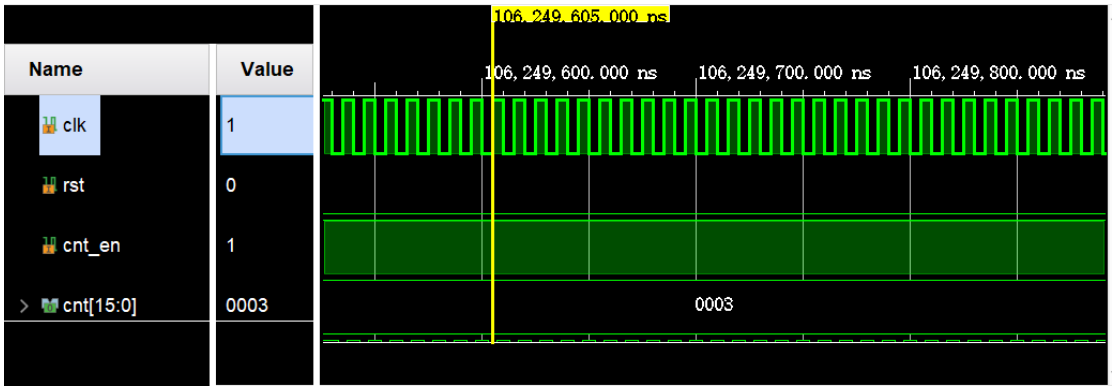
clk: 100MHz, rst=0, cnt_en=0



- **functional simulation of the CounterB: VHDL, Counts DOWN**

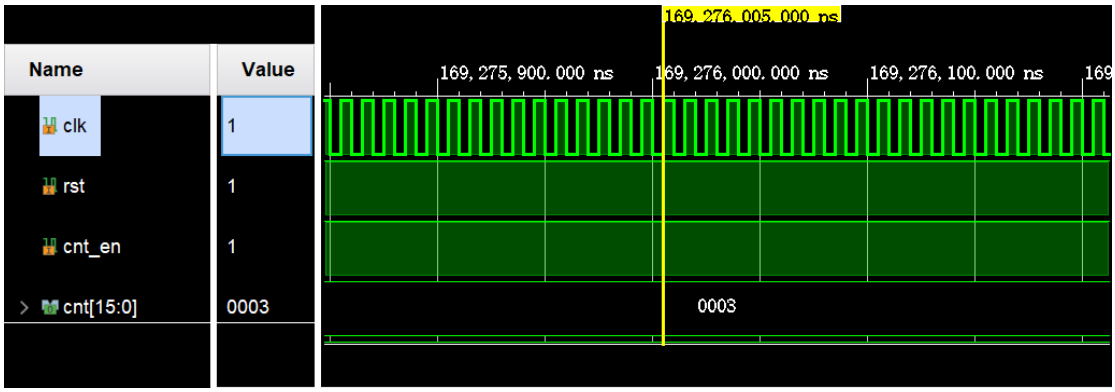
case 1:

clk: 100MHz, rst=0, cnt_en=1



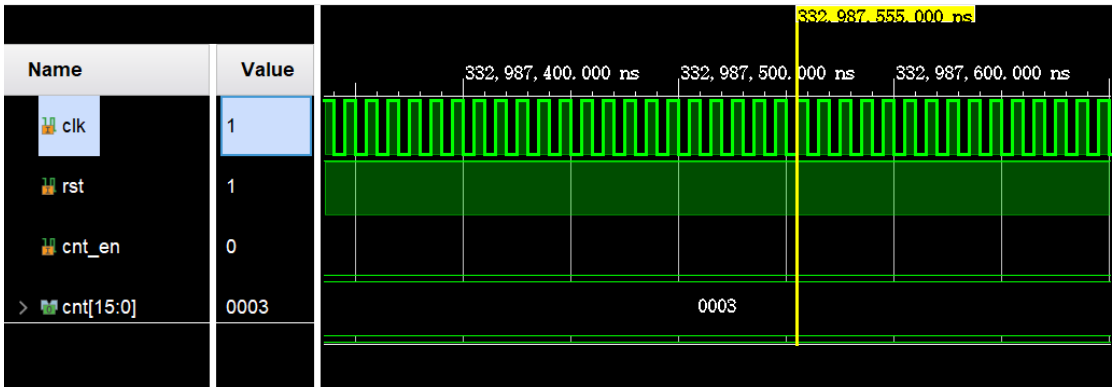
case 2:

clk: 100MHz, rst=1, cnt_en=1



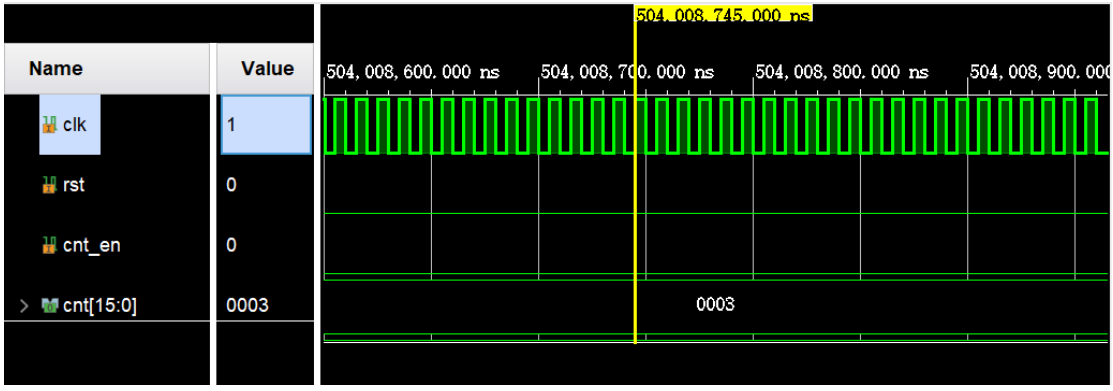
case 3:

clk: 100MHz, rst=1, cnt_en=0



case 4:

clk: 100MHz, rst=0, cnt_en=0

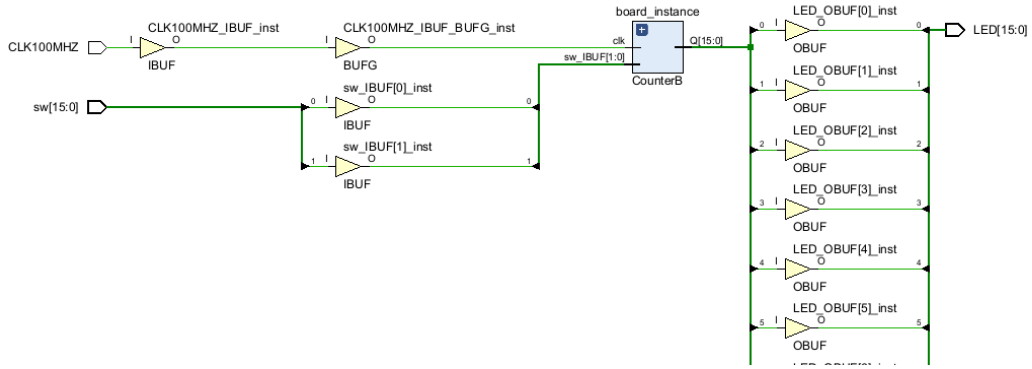


Task 3: Schematic of each of the 2 counters

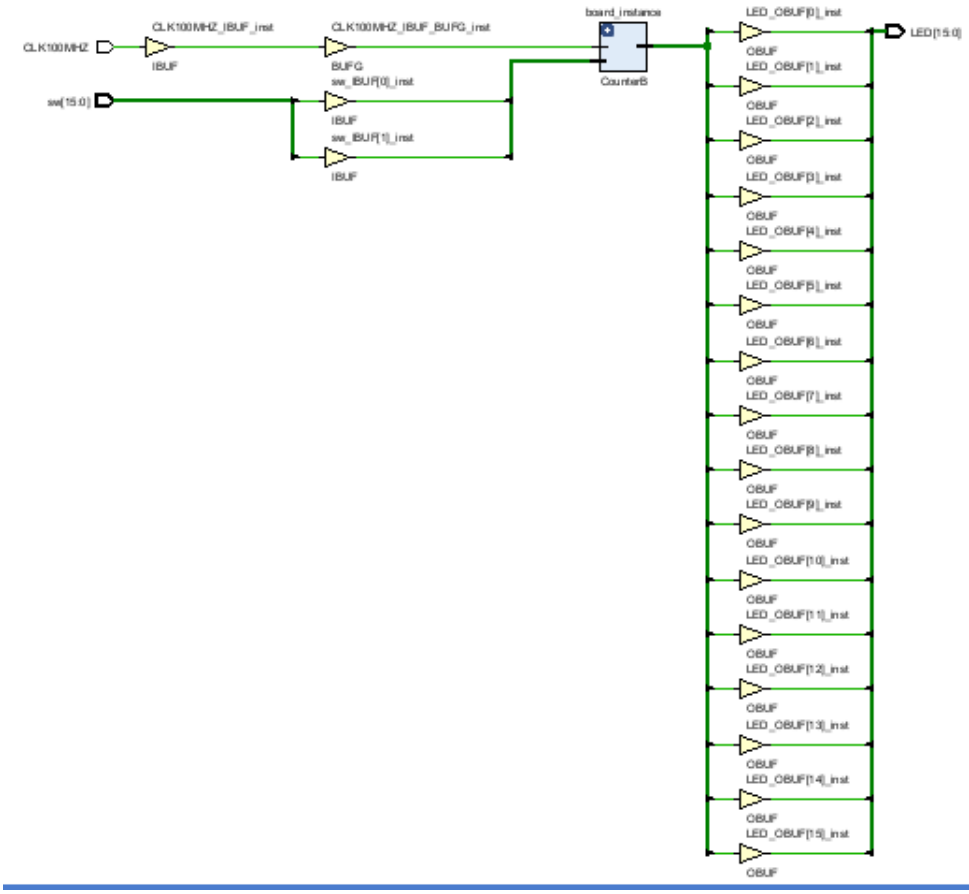
The diagram has three input and one output. The counters use 100MHz input clock as an input clock. Then, use sw[0] to control the input active-high reset signal, use sw[1] to control the input enable signal for counting. Finally, get an 16bit output.

- **Schematic of the CounterA: Verilog, Counts UP**

  In detail

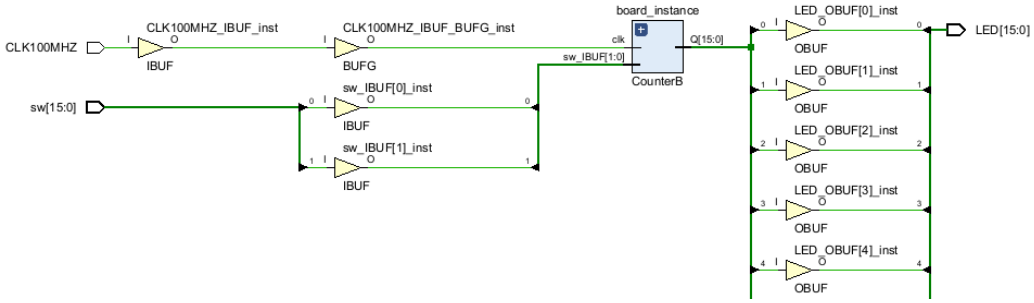


  Overall

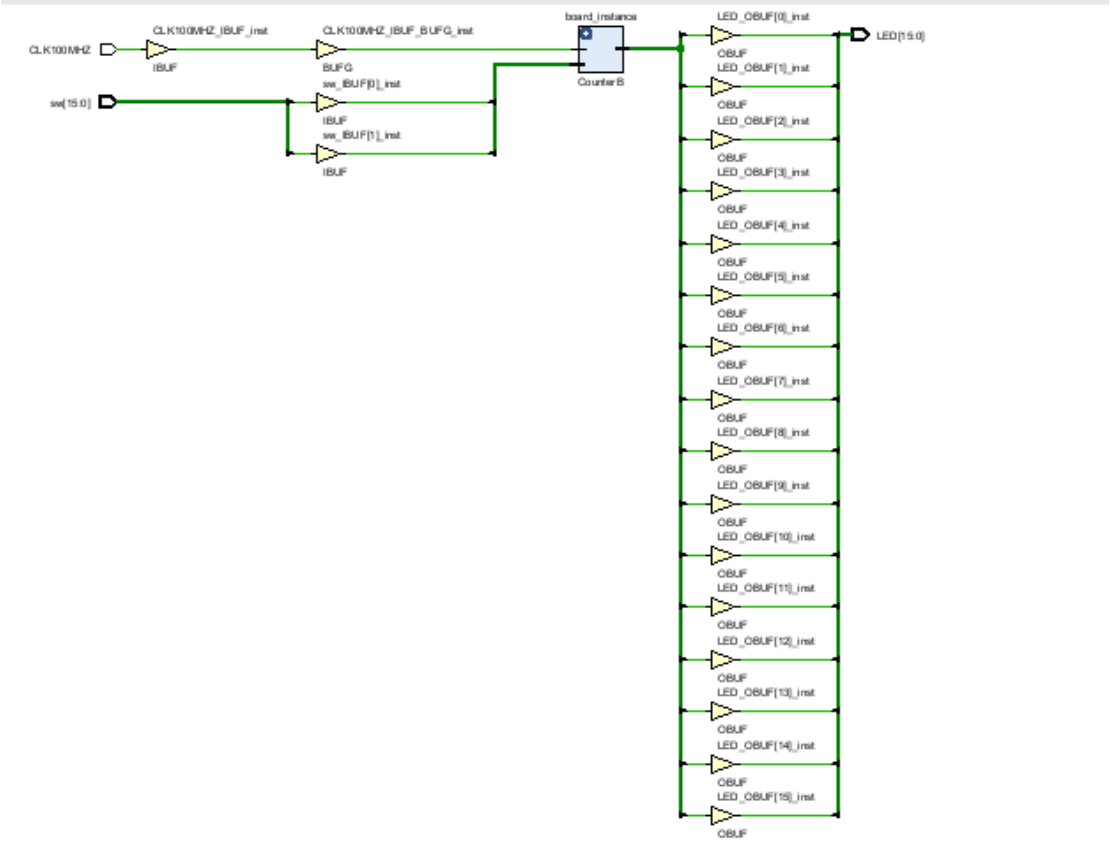


- **Schematic of the CounterB: VHDL, Counts DOWN**

  In detail



  Overall



Difference between the Verilog and VHDL hardware

1. compared to VHDL, Verilog requires fewer lines of code to complete the same task
2. VHDL does not allow mixing or manipulating variables with different classes, while Verilog does