EL 6463 – Homework 1

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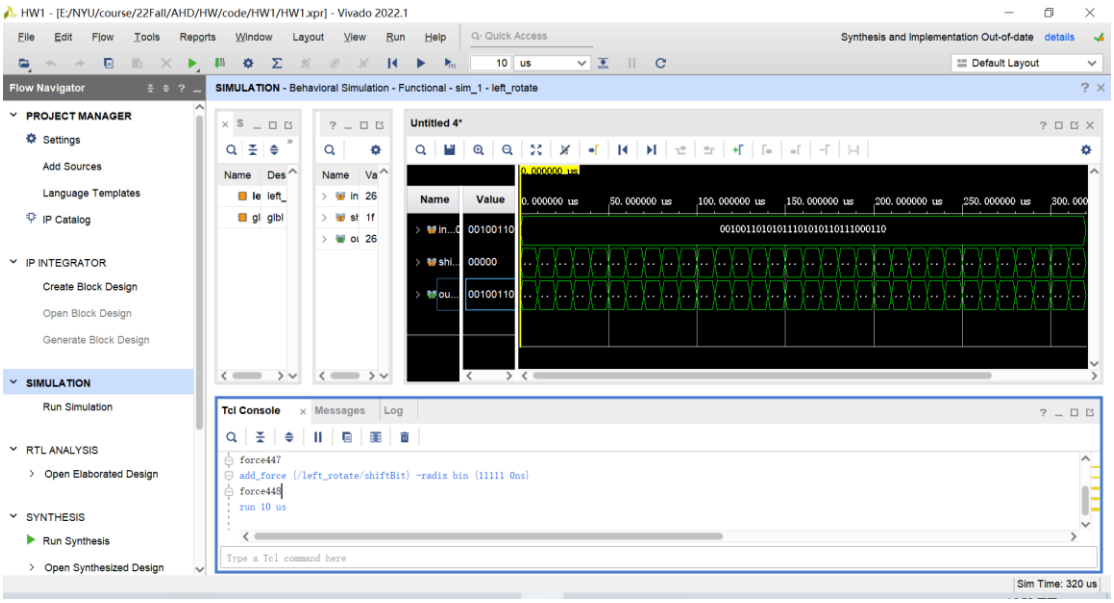
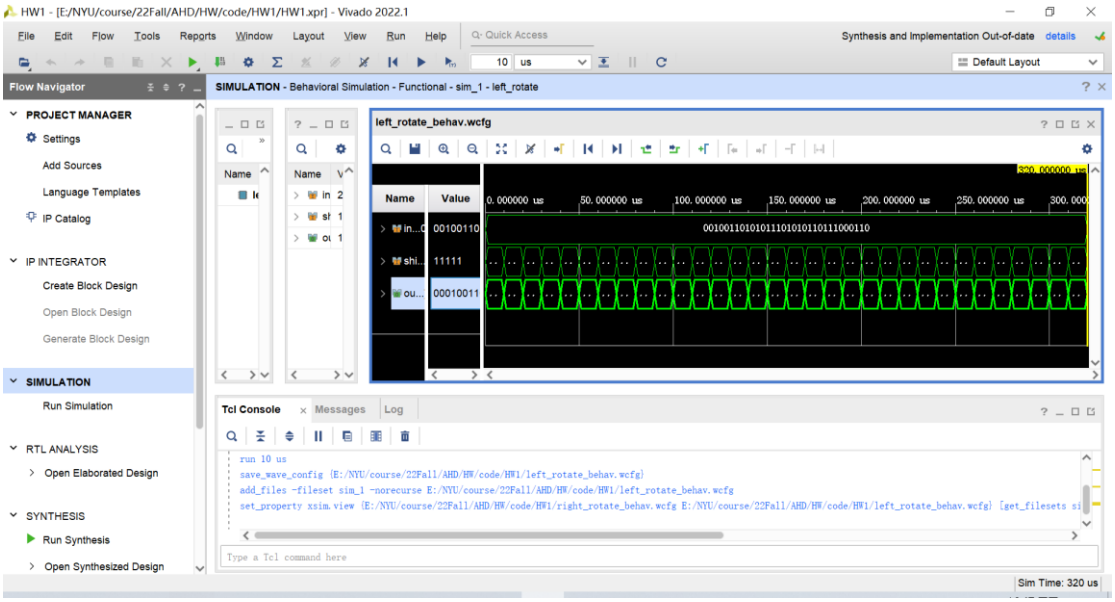
a. Screenshots of simulation outputs

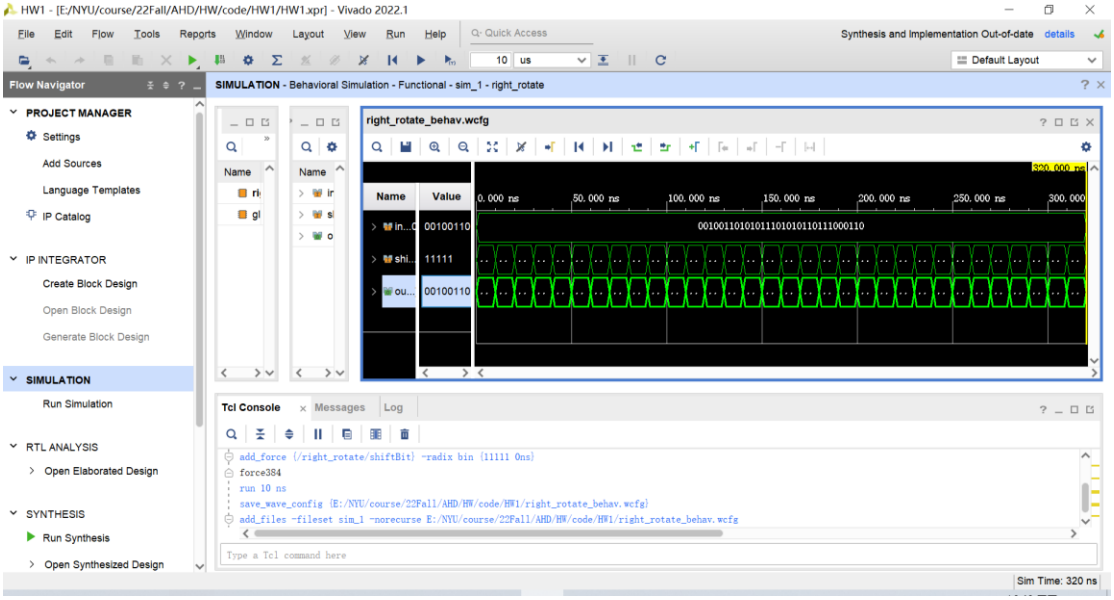
- Left rotate – Verilog



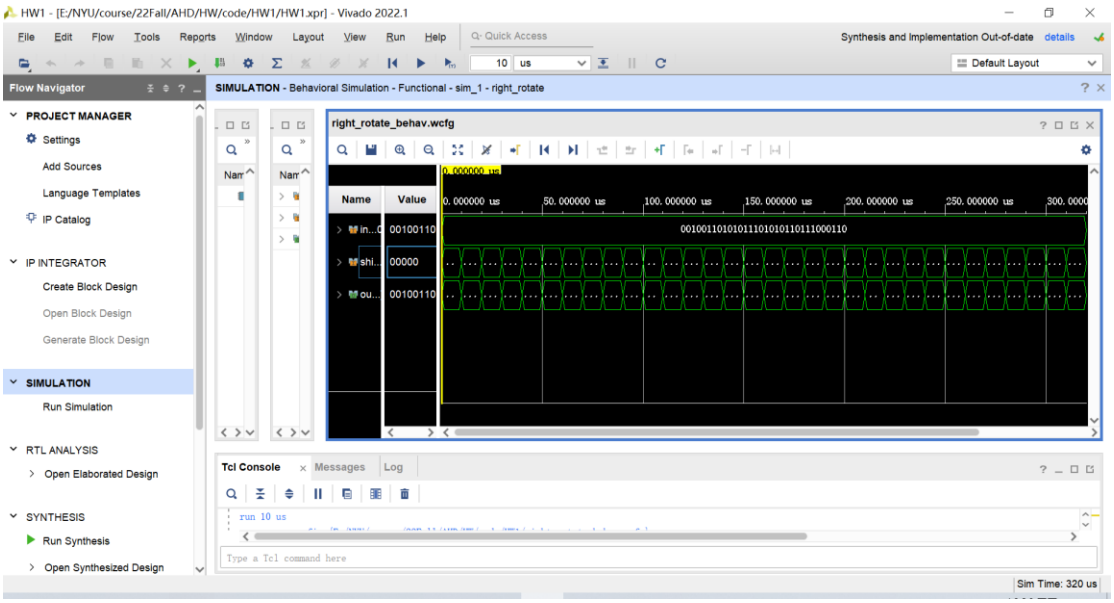
- Left rotate – VHDL



- right rotate – Verilog

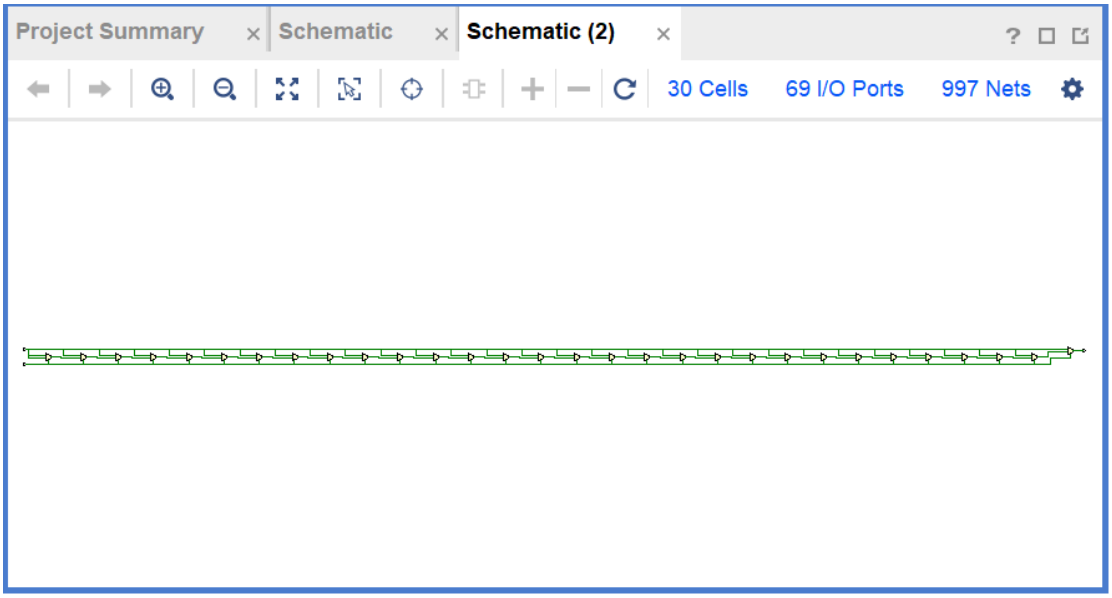


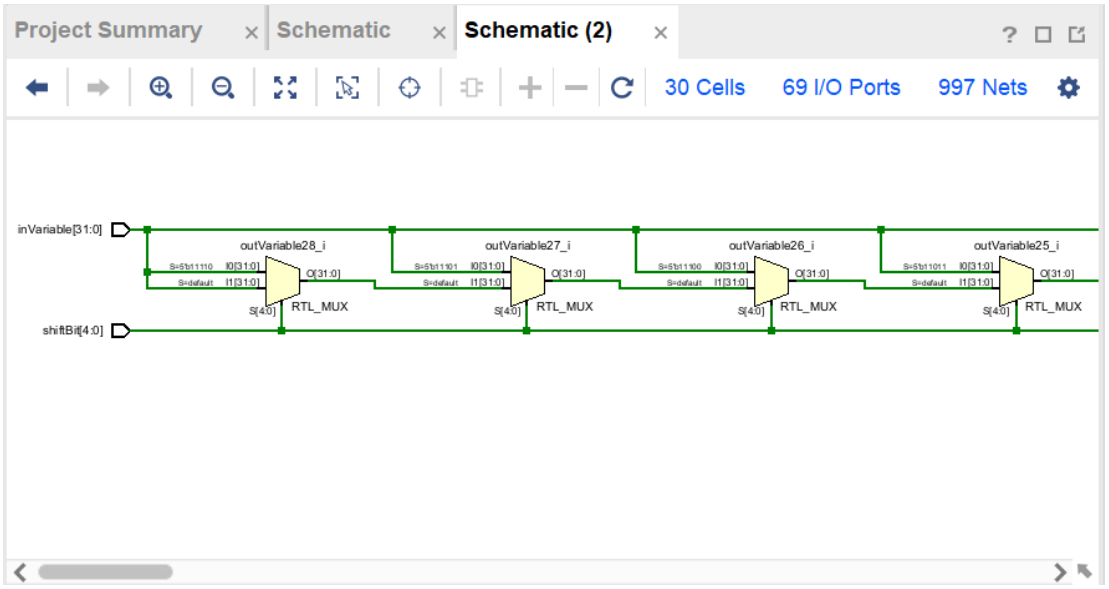
- right rotate – VHDL



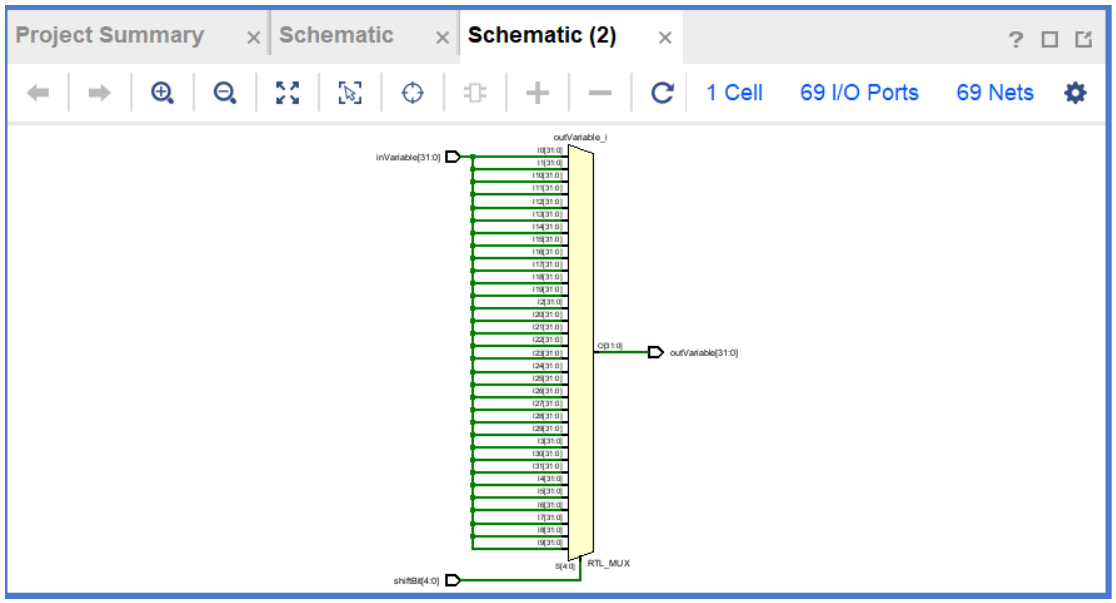
b. Block Diagram

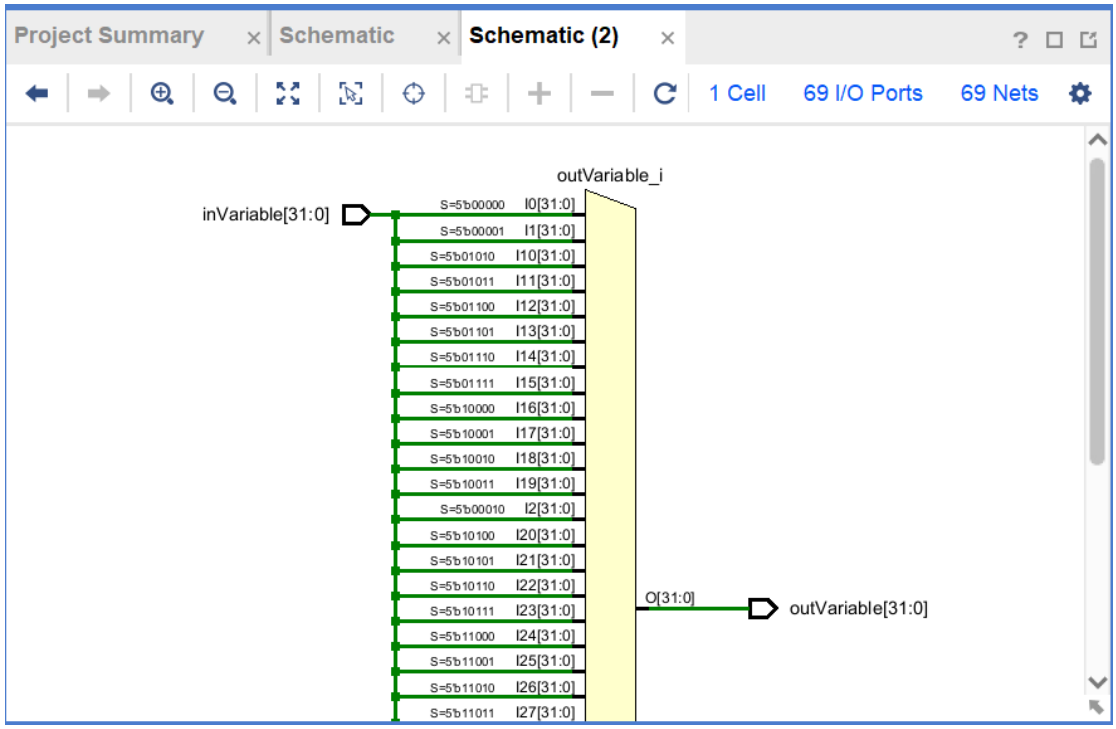
- Left rotate – Verilog



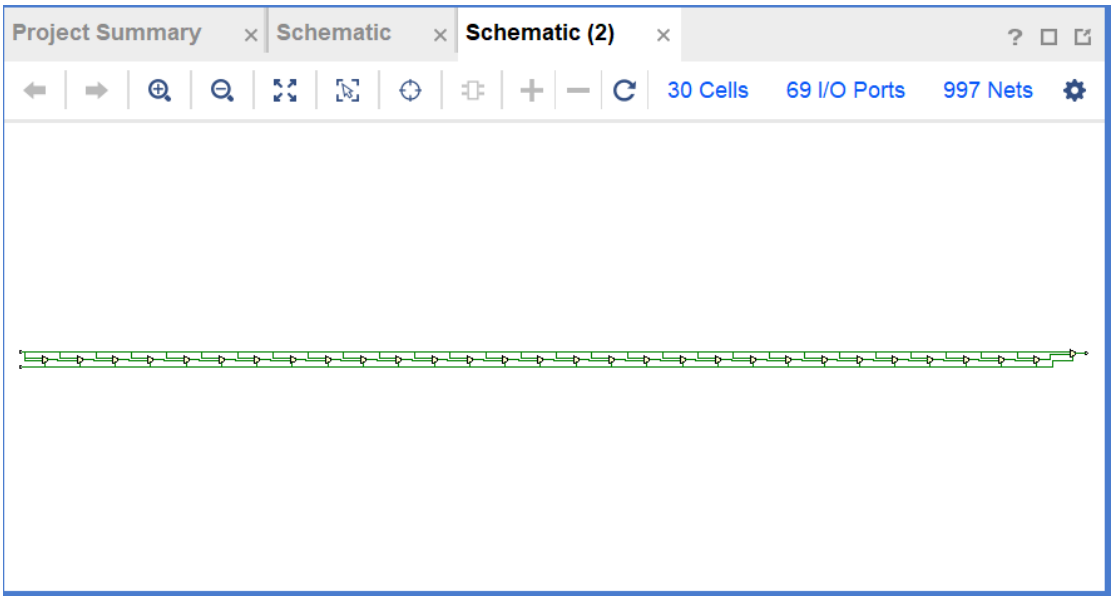


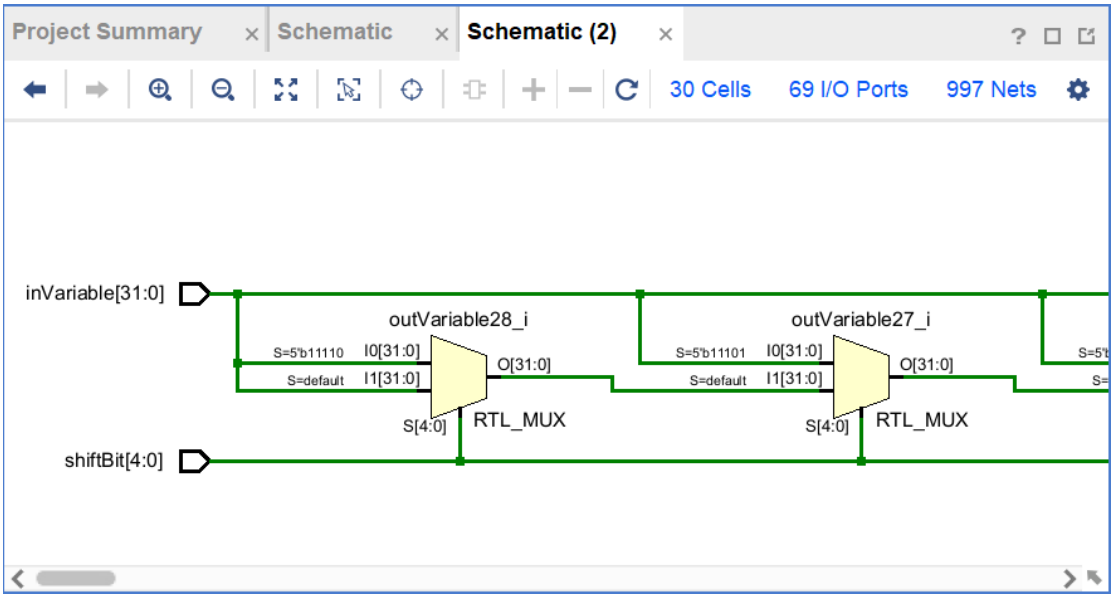
- left rotate – VHDL



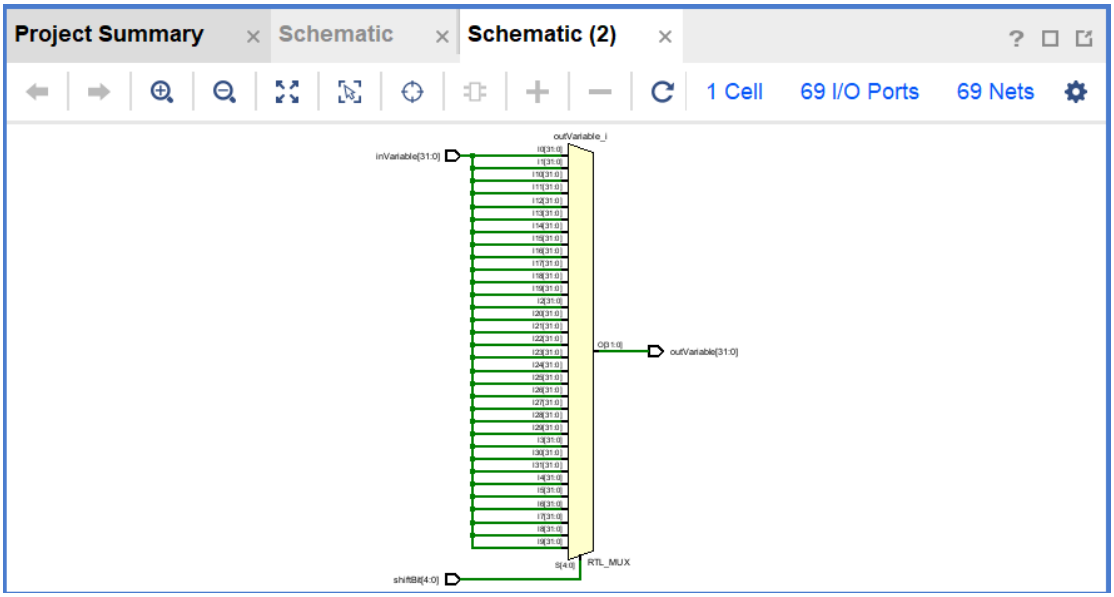


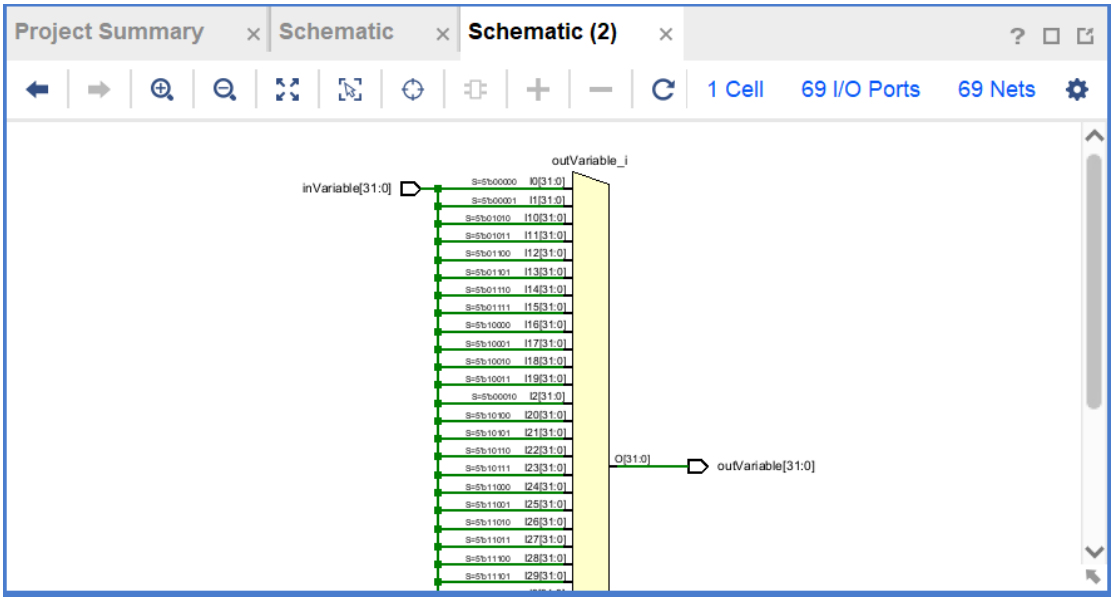
- right rotate – Verilog





- right rotate – VHDL





c. Answer the question: are the logic gates derived from the Verilog and VHDL equivalent?
The format of logic gates derived from the Verilog and VHDL are different, but the functionality of corresponding logic gates is the same. For example, the left rotate logic gates derived from the Verilog and VHDL looks different. However, they have the same simulation output.

d. Link to the video:
https://drive.google.com/file/d/1A5LfxhxZ1ONEt7EgyAhyDNkauMHL11Pj/view?usp=sharing