EL 6463 – Homework 3

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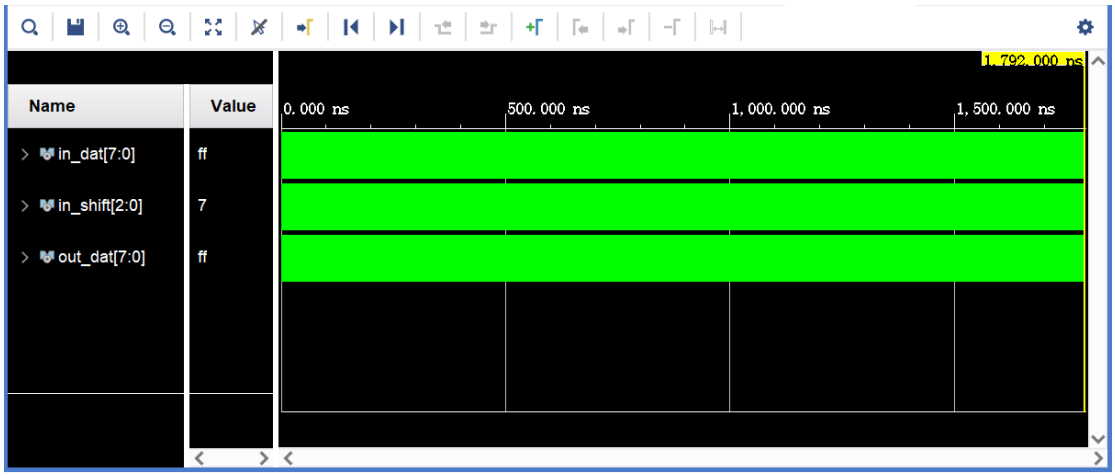
HW1 (a) - testbench written in VHDL

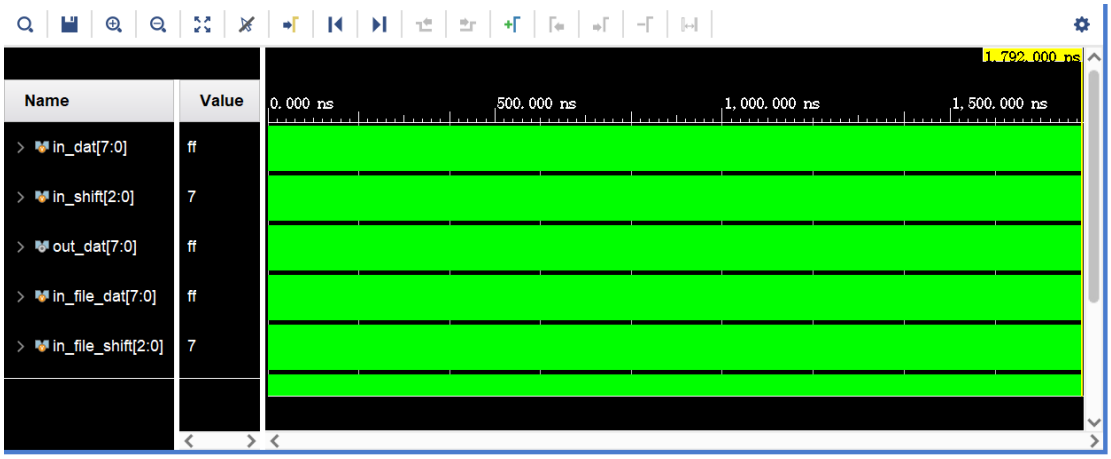
For left rotate written in VHDL, the following screenshot shows all $2^8 \times (2^3 - 1) = 1792$ test cases pass the test.




```
Note: All test cases passed successfully
Time: 1792 ns  Iteration: 0  Process: /test_left_rotate_vhdl/line__54  File: E:/NYU/course/22Fall/AHD/HW/code/HW3/HW3.srcs/sim_1/new/test_left_rotate_vhdl.vhd
$stop called at time : 1792 ns : File "E:/NYU/course/22Fall/AHD/HW/code/HW3/HW3.srcs/sim_1/new/test_left_rotate_vhdl.vhd" Line 80
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_left_rotate_vhdl_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 10000ns
launch_simulation: Time (s): cpu = 00:00:06 ; elapsed = 00:00:13 . Memory (MB): peak = 1226.570 ; gain = 0.000
```

HW1 (d) - testbench written in Verilog

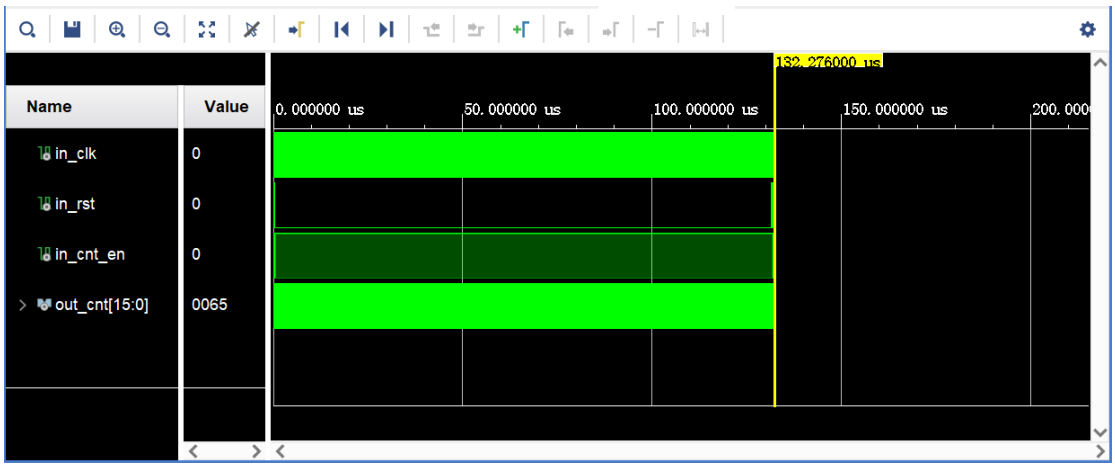
For right rotate written in Verilog, the following screenshot shows all $2^8 \times (2^3 - 1) = 1792$ test cases pass the test.




```
The test cases file was opended.
All test cases passed successfully
$stop called at time : 1792 ns : File "E:/NYU/course/22Fall/AHD/HW/code/HW3/HW3.srcs/sim_1/new/test_right_rotate_verilog.v" Line 70
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_right_rotate_verilog_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 10000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:13 . Memory (MB): peak = 1226.570 ; gain = 0.000
```

HW2 (a) - testbench written in VHDL

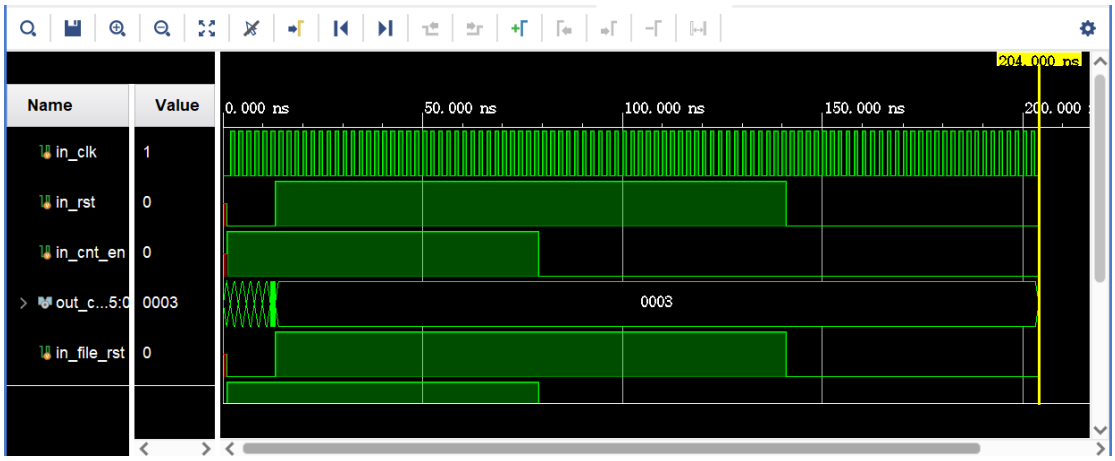
For up counter written in Verilog, the following screenshot shows all test cases pass the test which is writtem in VHDL.




```
Note: All test cases passed successfully
Time: 132276 ns  Iteration: 0  Process: /test_CounterA/line__55  File: E:/NYU/course/22Fall/AHD/HW/code/HW3/HW3.srcs/sim_1/new/test_CounterA.vhd
$stop called at time : 132276 ns : File "E:/NYU/course/22Fall/AHD/HW/code/HW3/HW3.srcs/sim_1/new/test_CounterA.vhd" Line 91
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_CounterA_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 10000000ns
launch_simulation: Time (s): cpu = 00:00:08 ; elapsed = 00:00:14 . Memory (MB): peak = 2314.281 ; gain = 0.000
```

HW2 (b) - testbench written in Verilog

For down counter written in VHDL, the following screenshot shows all test cases pass the test which is writtem in Verilog.




```
The test cases file was opended.
All test cases passed successfully
$stop called at time : 204 ns : File "E:/NYU/course/22Fall/AHD/HW/code/HW3/HW3.srcs/sim_1/new/test_CounterB.v" Line 67
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_CounterB_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 10000000ns
launch_simulation: Time (s): cpu = 00:00:06 ; elapsed = 00:00:15 . Memory (MB): peak = 2314.281 ; gain = 0.000
```

Question 3

Using the VHDL test-bench (1), is it possible to validate the Data Dependent Right Rotate from HW1 (d) which is written in Verilog? Explain.

ANS: It is possible. One of the examples is showed when using VHDL written the test-bench for HW2 (a) CounterA, where CounterA design source is written in Verilog. The test-bench can run correctly. Moreover, it can also be validated that when the design source code is written in VHDL, the test-bench code can also be written in Verilog. One of the examples is showed when using Verilog written the test-bench for HW2 (b) CounterB, where CounterB design source is written in VHDL. Therefore, the using of VHDL and Verilog can be mixed.