Homework 1 (5%) Due: 2:00 PM, Friday 16 Sept.

Basic Combinational Design (e.g, OR-AND and FULL ADDER) and Functional Simulation

Overview

The purpose of this homework is to encourage you to familiarise yourself with the tools and languages used in this course.

Part 1: Set up Vivado Tools

In this course, we will be using Xilinx Vivado Design Suite tools for our digital design. Vivado provides synthesis and simulation functionality.

On your own machines:

- Xilinx offers a free version of the tools that you can download and install on your own computers.
  i. https://www.xilinx.com/support/download.html
  ii. Download version 2022.1.
- YouTube instructions: https://www.youtube.com/watch?v=ZTAfESmWKXE
- Vivado can be installed on Windows and Linux platforms
- If you use a Mac, you will need to use BootCamp, or set up a Virtual Machine with a Windows or Linux guest (VirtualBox and VMware (Workstation Player) are free options). Hammond recommends VMware workstation with an Ubuntu virtual machine.

Check that you have a working setup before proceeding.

Part 2: Model simple designs and test them

In the lectures, you have been introduced to concepts around modeling digital hardware designs using a Hardware Description Language (HDL). Your task is to model the following using **both VHDL and Verilog**.

Tasks:

1. Implement and Simulate a design (in **both** VHDL and Verilog) that can perform data dependent left rotate.
2. Implement and Simulate a design (in **both** VHDL and Verilog) that can perform data dependent right rotate.
3. Film a short video explaining the design and simulation process you used. You may choose to use the recording system built in to Powerpoint, or a screen recording software such as OBS (https://obsproject.com/) (which is free and open source). Include and explain a drawing of the modeled design.

Deliverables:

1. Submit a zip file with your VHDL and Verilog files and a PDF report containing:
   a. Screenshots of your simulation outputs
      i. Test cases: All possibilities of all inputs
   b. Submit Block Diagram.
      i. Draw the equivalent logic gates for each of your four codes.
   c. Answer the question: are the logic gates derived from the Verilog and VHDL equivalent?
   d. Your link to the video from part (2), below.
2. Upload a video to YouTube or your NYU google drive, include the link to the video in the PDF from (1).
   a. Video can be 3 minutes max.
   b. Explain the process of the design and simulation of your functionality.
   c. Ensure the video is watchable without signing in (i.e. make it viewable with link).