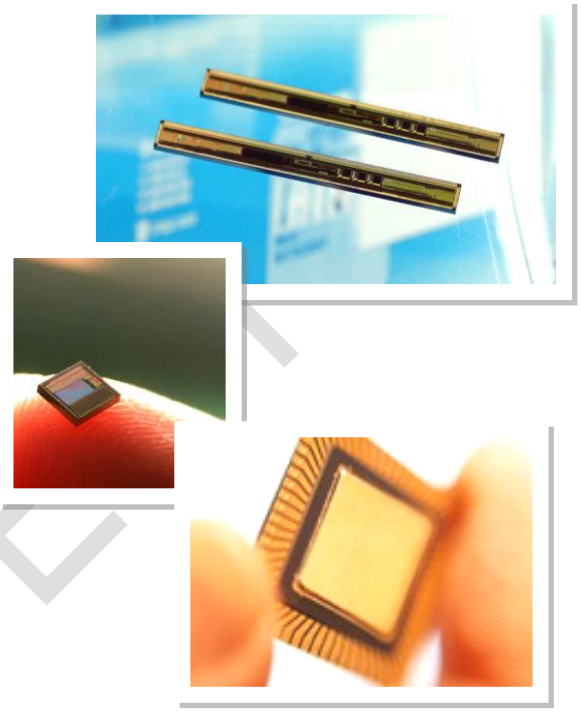
Raydium 瑞鼎科技股份有限公司
Raydium Semiconductor Corporation



RM69A10 Data Sheet

Single Chip Driver with 16.7M color

for 720RGBx1280 OLED driver

Revision：0.2

Date：Mar, 30 2023

Revision History

Version No.	Date	Description	Page	Modified By	Checked By
0.1	2023/02/06	First Release		Howard Hsiung	CN.Lin
0.2	2023/03/30	Modify WATCH_OSC_IN pin description Update register: 8A00h	13 89	Howard Hsiung	CN.Lin

TABLE OF CONTENTS

1 General Description

The RM69A10 device is a single-chip solution for LTPS/LTPO AMOLED that incorporates gate drivers and is capable of 720RGBX1280 with internal GRAM. It includes a internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit.

The RM69A10 supports MIPI Interface, 8-bit system interfaces, serial peripheral interfaces (SPI), dual serial peripheral interfaces (Dual-SPI) and quad serial peripheral interfaces (QAD-SPI). The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The RM69A10 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses support 16.7M-color images and a deep standby mode for lower power consumption.

2 Features

- **Single chip MUX1:2/ MUX1:3/ MUX1:4/ MUX1:6 LTPS/LTPO AMOLED controller/driver with display RAM and DeMura RAM**
- **Display resolution option**
  - 160~720 RGB X 1280 with MUX1:3
  - 160~720 SPR X 1280 with MUX1:2
  - 720~1440 RGB X 640 with MUX1:6
  - 720~1440 SPR X 640 with MUX1:4

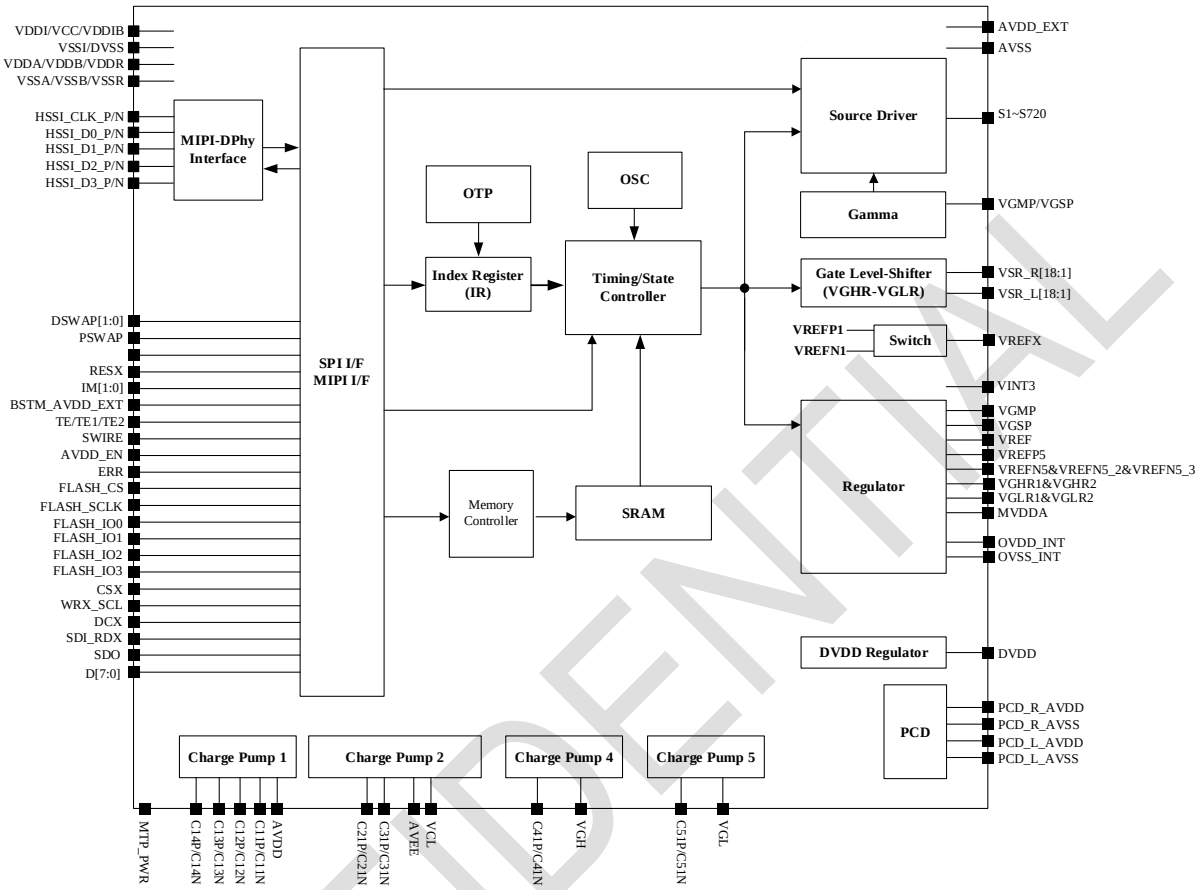
  Note: Basing on different MUX design and the max frame ram (720RGBx1280), source setting and gate can be adjusted. Please confirm the resolution for different mux design with Raydium.
- **Display mode (Color mode)**
  - Full color mode: 16.7M-colors
  - Deep color mode: 1073.7M colors (30-bit, VESA 3.75x compression input)
  - Idle mode: 16.7M-colors, 8-colors
- **Interface**
  - Serial peripheral interface (SPI)
  - Dual serial peripheral interface (Dual-SPI)
  - Quad serial peripheral interface (Quad-SPI)
  - MIPI Display Serial Interface
    - Support 1lane/2lane/4lane (1lane: 1Gbps)
    - Maximum total bit rate is 3.4Gbps of 4 data lanes in 24-bit data format,
      2.5Gbps of 4 data lanes in 18-bit data format, and
      2.2Gbps of 4 data lanes in 16-bit data format
- **Interface pixel format**
  - MIPI: RGB888/ RGB666/ RGB565
  - SPI: RGB888/ RGB666/ RGB565/ RGB332
- **Abundant color display and drawing functions**
  - Programmable γ-correction function for 16.7 million color display
  - Individual gamma correction setting for RGB dots
  - Partial display function
- **Power Saving Mode**
  - Dynamic ELVSS for power saving
  - Low Frame Rate Select
  - Internal OLED power mode
  - Always on display(AOD) function
- **Display effect compensation**
  - Support Optical DeMura function for AMOLED
  - Global IR drop compensation
  - Cross-talk compensation
- **Build-in panel crack detection**

- **Support Shape Edge Smooth function**
- **Support Status Active Reporting function**
- **Support S-wire interface for power IC control**
- **On chip**
  - VREFP/VREFN voltage generator for panel voltage
  - VGHR/VGLR voltage for gate control signal
  - Internal oscillator for display clock
  - Source output MUX 1-2, MUX 1-3, MUX 1-4, MUX 1-6 with 720ch source output pins
  - Supports gate control signals to gate driver in the panel
- **Logic / interface power supply voltage VDDI = 1.65V ~ 1.95V**
- **Analog power supply voltage VDDA/VDDB/VDDR = 2.7V ~ 3.6V**
- **Analog power supply voltage AVDD_EXT = 5.0V ~ 8.0V (BSTM_AVDDEXT=1)**
- **Output voltage levels**
  - Positive gate driver voltage range for VGHR1/VGHR_2: 3 ~ 12.0V
  - Negative gate driver voltage range for VGLR1/VGLR_2: -2V ~ -12.0V
  - VREFP panel voltage range : 0.5V ~ 7.2V (AVDD-0.3V)
  - VREFN panel voltage range : -0.5V ~ -7.2V (AVEE+0.3V)
  - Step-up 1,2 output voltage range for AVDD: 5.0 ~ 8.0V, AVEE: -2.8 ~ -8.0V
  - Gamma high/low voltage range for VGMP: 2.0V ~ 7.7V (Max<=AVDD-0.3v) , VGSP: 0V, 0.2125V ~ 4.5V
- **Package: COF/COP**
- **Chip size evaluation : 14450um x 1950um(including scribe line)**

■ **Power Supply Specifications**

No.	Item		Description
1	Source Driver		720 pins (720 x RGB)
2	gate control timing Level shift		VGHR1-VGLR1/ VGHR_2-VGLR_2
3	Input Voltage	VDDI (VDDIB)	1.65 ~ 1.95V
		VCC	Connect to VDDI
		VCI (VDDA/VDDB/VDDR)	2.70 ~ 3.60V
		AVDD_EXT	5.0V ~ 8.0V (BSTM_AVDDEXT=1)
4	OLED drive voltages	AVDD	5.0V ~ 8.0V
		VGHR	3V ~ 12.0V
		VGLR	-2V ~ -12.0V
		VREFP5	0.5V ~ 7.2V (Max<=AVDD-0.3v)
		VREFN5	-0.5V ~ -7.2V (Min>=AVEE+0.3v)
		OVDD_INT	2.0~6.0v (Max<=AVDD-0.3v)
		OVSS_INT	-0.4 ~ -4.7V (Min>=AVEE+0.3v)
5	Internal step-up circuits	AVDD	VCI+VDDI, 2xVCI, 2xVCI+VDDI, 3xVCI
		AVEE	-1xVCI, VCL-VDDI, VCL-VCI, 2xVCL-VDDI, 2xVCL-VCI
		VGH	AVDD, AVDD+VDDI, AVDD+VCI, 2xAVDD
		VGL	AVEE, AVEE-VDDI, AVEE-VCI, AVEE+VCL-VDDI, AVEE+VCL-VCI

3 Block Diagram



Interface

The RM69A10 supports MIPI DSI interface. MIPI DSI can access both internal command and display data.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a drive voltage, which corresponds to grayscale level set in the γ correction register. The RM69A10 displays 16.7M colors at the maximum.

Power Supply Circuit

The power supply circuit generates supply voltages to OLED panel, VGH, VGL.

Timing Generating

The timing controller generates timing signals for internal circuits such as the display timing.

Oscillator

The RM69A10 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

The OLED display driver circuit consists of 720 source drivers (S1~S720). The gate signal consists of VSR_R/L[18:1] and outputs either VGHR/VGHR2 or VGLR/VGLR2 level.

4 Pin Description

4.1 Power Supply Pins

Signal	I/O	Function
VDDB	P	Power supply for DC/DC converter VDDB, VDDA and VDDR should be the same input voltage level
VDDA	P	Power supply for analog system VDDB, VDDA and VDDR should be the same input voltage level
VDDR	P	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level
VDDI	P	Power supply for interface system except MIPI interface. VDDI and VDDIB should be the same input voltage level.
VDDIB	P	Power supply for charge pump. VDDI and VDDIB should be the same input voltage level.
VCC	P	Power supply for DVDD regulator. VCC pin can connect to VDDI pin..
AVDD_EXT	P	1. When BSTM_AVDD_EXT=0, AVDD power from DDIC internal charge pump, AVDD_EXT pin connect to the AVDD pin of DDIC. 2. When BSTM_AVDD_EXT=1, AVDD power from External Power IC, AVDD_EXT pin connect to the AVDD output of Power IC.
VSSB	P	System ground for DC/DC converter
VSSA	P	System ground for analog system
VSSR	P	System ground for regulator system
VSSAM	P	System ground for internal MIPI analog system
VSSI	P	System ground for interface system except MIPI interface
DVSS	P	System ground for internal digital system
AVSS	P	System ground for source OP system.
MTP_PWR	P	MTP programming power supply pin (6V typical) Must be left open or connected in normal condition.

4.2 Interface Pins

Signal	I/O	Function
CSX	I	Chip select input pin (“Low” enable) in SPI I/F. If not used, please connect to VDDI.
WRX_SCL	I	A synchronous clock signal in SPI I/F. If not used, please connect to VSSI.
DCX	I	Display data / command selection in 4-wire SPI I/F. DCX = ”0” : Command DCX = ”1” : Display data or Parameter If not used, please connect to VSSI.
SDI_RDX	I/O	SDI: Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal. If not used, please leave it Open.
SDO	O	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. If not used, please open this pin.
D[7:0]	I/O	QSPI will use D0 & D1 pin. These pins are not used for MIPI, please leave it Open.

4.3 MIPI Interface Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>HSSI_CLK_P
HSSI_CLK_N</td><td>I</td><td>These pins are DSI-CLK+/- differential clock signals of data lane if MIPI interface is used. If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI _D0_P
HSSI _D0_N</td><td>I/O</td><td>These pins are DSI-D0+/- differential data signals of data lane if MIPI interface is used. If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D1_P
HSSI_D1_N</td><td>I/O</td><td>These pins are DSI-D1+/- differential data signals of data lane if MIPI interface is used. If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D2_P
HSSI_D2_N</td><td>I/O</td><td>These pins are DSI-D2+/- differential data signals of data lane if MIPI interface is used. If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D3_P
HSSI_D3_N</td><td>I/O</td><td>These pins are DSI-D3+/- differential data signals of data lane if MIPI interface is used. If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>DSWAP[1:0]
PSWAP</td><td>I</td><td>Input pins to select lane sequence and polarity for data transmission
<table>
<tr><th>PSWAP</th><th>DSWAP[1:0]</th><th>HSSI_D3_P</th><th>HSSI_D3_N</th><th>HSSI_D0_P</th><th>HSSI_D0_N</th><th>HSSI_CLK_P</th><th>HSSI_CLK_N</th><th>HSSI_D1_P</th><th>HSSI_D1_N</th><th>HSSI_D2_P</th><th>HSSI_D2_N</th></tr>
<tr><td rowspan="4">0</td><td>00</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr>
<tr><td>01</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D3+</td><td>D3-</td></tr>
<tr><td>10</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr>
<tr><td>11</td><td>D3+</td><td>D3-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td></tr>
<tr><td rowspan="4">1</td><td>00</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr>
<tr><td>01</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td><td>D3-</td><td>D3+</td></tr>
<tr><td>10</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr>
<tr><td>11</td><td>D3-</td><td>D3+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td></tr>
</table></td></tr>
</table>

NOTE: “1” = VDDI level, “0” = VSSI level.

4.4 Interface Logic Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>RESX</td><td>I</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>IM[1:0]</td><td>I</td><td>Interface type selection. The connections of IM[1:0] which not shown in table are invalid.
<table>
<tr><th>IM[1:0]</th><th>Display Data</th><th>Command</th></tr>
<tr><td>00</td><td>MIPI / 3-wire SPI</td><td>MIPI / 3-wire SPI</td></tr>
<tr><td>01</td><td>MIPI / 4-wire SPI</td><td>MIPI / 4-wire SPI</td></tr>
<tr><td>10</td><td>MIPI / QUAD – SPI</td><td>MIPI / QUAD – SPI</td></tr>
<tr><td>11</td><td>Reserved</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>TE/TE1/TE2</td><td>O</td><td>General purpose output pins which include TE (by frame and by scan line) and signals which is activated and selected by register command. If not used, please open this pin.</td></tr>
<tr><td>BSTM_AVDD_EXT</td><td>I</td><td>BSTM_AVDD_EXT=0, AVDD power from DDIC internal charge pump
BSTM_AVDD_EXT=1, AVDD power from External Power IC</td></tr>
<tr><td>SWIRE</td><td>O</td><td>Swire protocol setting pin of Power IC, If not used, please open this pin.</td></tr>
<tr><td>AVDD_EN</td><td>O</td><td>This signal is used to enable and control the AVDD voltage of external DC/DC. If not used, please open this pin..</td></tr>
<tr><td>WATCH_OSC_IN</td><td>I</td><td>The oscillator input of OSC tracking function. (For example: crystal oscillator= 32.768kHz)
If not used, please connect to VSSI.</td></tr>
<tr><td>ERR</td><td>O</td><td>Output pin used to monitor display driver state and error status
If not used, please open this pin.</td></tr>
<tr><td>FLASH_CS</td><td>O</td><td>I/O pins to Flash for Demura function</td></tr>
<tr><td>FLASH_SCLK</td><td>O</td><td>I/O pins to Flash for Demura function</td></tr>
<tr><td>FLASH_IO0</td><td>I/O</td><td>I/O pins to Flash for Demura function</td></tr>
<tr><td>FLASH_IO1</td><td>I/O</td><td>I/O pins to Flash for Demura function</td></tr>
<tr><td>FLASH_IO2</td><td>I/O</td><td>I/O pins to Flash for Demura function</td></tr>
<tr><td>FLASH_IO3</td><td>I/O</td><td>I/O pins to Flash for Demura function</td></tr>
<tr><td>PCD_L_AVDD
PCD_L_AVSS</td><td>O</td><td>Input pins used for panel crack detection.
Please connect PCD_L_AVDD, and PCD_L _AVSS together by a routing trace on the panel when utilizing PCD function. Or just leave them open when not utilizing</td></tr>
</table>

PCD_R_AVDD PCD_R_AVSS	O	Input pins used for panel crack detection. Please connect PCD_R_AVDD and PCD_R _AVSS together by a routing trace on the panel when utilizing PCD function. Or just leave them open when not utilizing

NOTE: “1” = VDDI level, “0” = VSSI level.

4.5 Driver Output Pins (Pins for Panel)

Signal	I/O	Function
S1 ~ S720	O	Pixel electrode driving output.
DMY1 ~ DMY41	O	Dummy pad, leave it Open.
VSR_L[18:1] VSR_R[18:1]	O	VSR control signals, Level shift output, (VGHR-VGLR)

4.6 DC/DC Convert Pins

Signal	I/O	Function
AVDD	O	Output voltage from step-up circuit 1, generated from VDDB. Connect a capacitor for stabilization.
AVEE	O	Output voltage from step-up circuit 2, generated from VDDB. Connect a capacitor for stabilization.
VCL	O	Output voltage from step-up circuit 2, generated from VDDB. Connect a capacitor for stabilization.
VGH	O	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
VGL	O	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	IO	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement.
C21P, C21N C31P, C31N	IO	Capacitor connection pins for the step-up circuit which generate VCL and AVEE. Connect capacitor as requirement.
C41P, C41N	IO	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
C51P, C51N	IO	Capacitor connection pins for the step-up circuit which generate VGL. Connect capacitor as requirement.
VGHR	O	Output voltage generated from VGH. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
VGHR_2	O	Output voltage generated from VGH. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
VGLR	O	Output voltage generated from VGL. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.

VGLR_2	O	Output voltage generated from VGL. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
OVDD_INT	O	LDO output used for OLED panel display. Connect a capacitor for stabilization. When not in use, please open this pin.
OVSS_INT	O	LDO output used for OLED panel display Connect a capacitor for stabilization. When not in use, please open this pin.
VGMP	O	Output voltage generated from AVDD. LDO output for positive gamma high voltage.
VGSP	O	Output voltage generated from AVDD. LDO output for positive gamma low voltage.
VREF	O	Regulator output for internal reference voltage. Connect capacitor for stabilization.
DVDD	O	Regulator output for logic system power. Connect capacitor for stabilization.
MVDDA	O	Regulator output for internal MIPI circuit power. Connect capacitor for stabilization.
VREFP5	O	Regulator output for VREFP5. Connect capacitor for stabilization.
VREFN5	O	Regulator output for VREFN5. Connect capacitor for stabilization.
VREFN5_2	O	Regulator output for VREFN5_2. Connect capacitor for stabilization.
VREFN5_3	O	Regulator output for VREFN5_3. Connect capacitor for stabilization.
VREFX	O	Output for VREFN5 or VREFP5

4.7 Test Pins

Signal	I/O	Function
ANALOG_TEST 1~3	O	Test pin, not accessible to user. Must be left open.
TEST[1]~[3]	IO	Test pin, not accessible to user. Must be left open.
TESTEN	I	Test pin, not accessible to user. Must be left open., Internal pull low
EXTCLK	I	Test pin, not accessible to user. Must be left open.
TEST_I2C_SCL	I	Test pin, not accessible to user. Please connect to VDDI.
TEST_I2C_SDA	I	Test pin, not accessible to user. Please connect to VDDI.
DUMMY[1]~[7]	I	Dummy PAD, leave it open
DUMMY_R1~R6	I	The same pad name short together internally Please leave them open when not utilizing

5 Function Description

5.1 Interface Type Selection

Interface type selection. The connections of IM[1:0] which not shown in table are invalid.

IM[1:0]	Display Data	Command
00	MIPI / 3-wire SPI	MIPI / 3-wire SPI
01	MIPI / 4-wire SPI	MIPI / 4-wire SPI
10	MIPI / QUAD-SPI	MIPI / QUAD-SPI
11	Reserved	Reserved

5.2 SPI/DUAL-SPI Interface

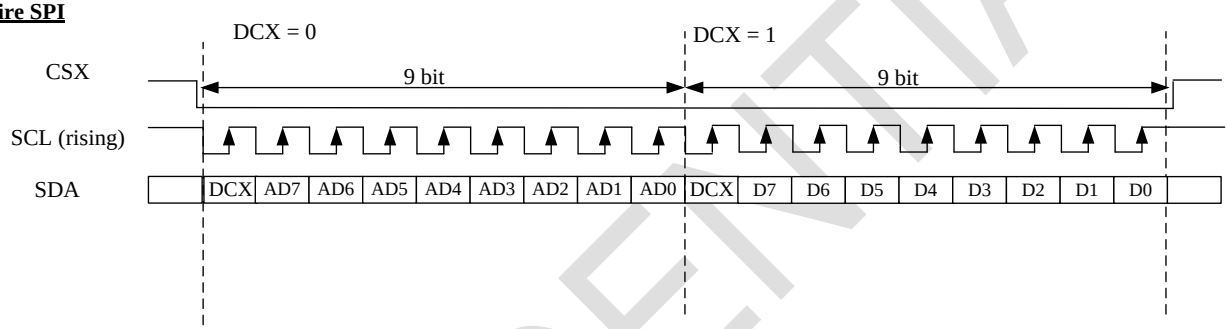
3-wire / 4-wire SPI/DUAL-SPI Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The 3-wire/4-wire SPI interface utilizes CSX, SCL and SDA signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

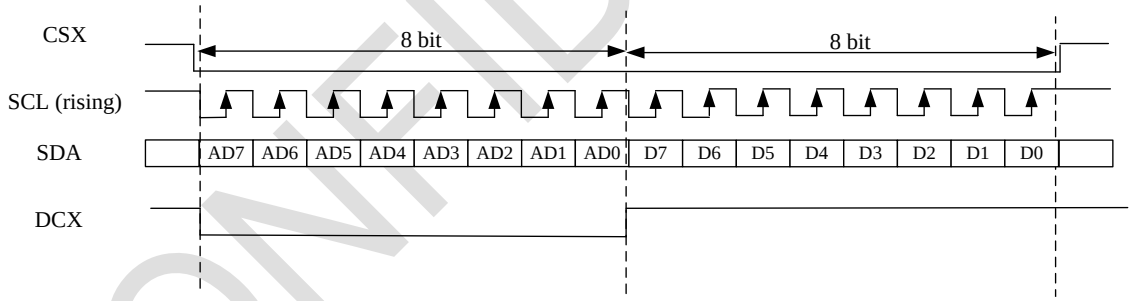
During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. The 3-wire serial data contains DCX bit and a transmission byte. DCX bit is driven low while command information is on the interface and is pulled high when data is present.

The 3-wire/4-wire SPI interface write command sequences are described in the following figure.

3-wire SPI



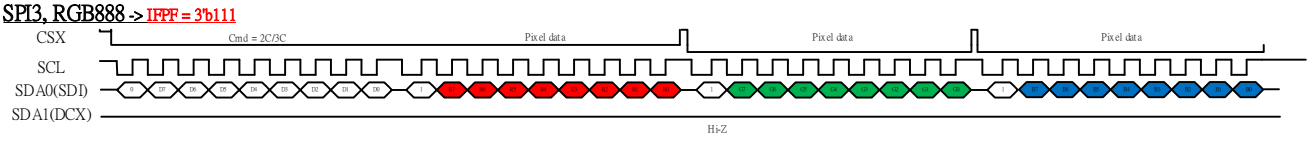
4-wire SPI



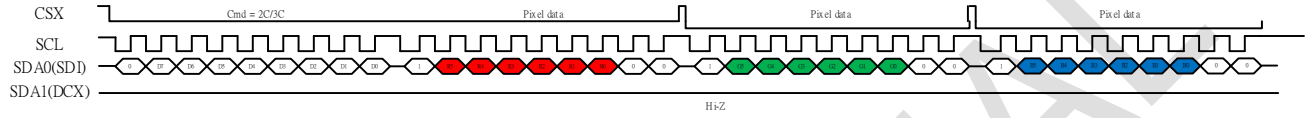
The 3-wire/4-wire SPI interface write display data sequences are described in the following figure.

When DSPI_en =0, the host sends data by SDA only.

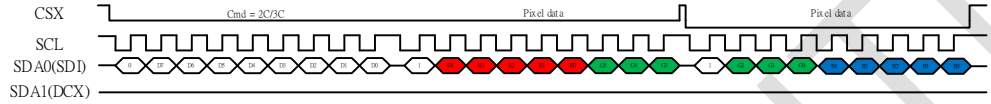
SPI3, RGB888 -> IFPF = 3'b111



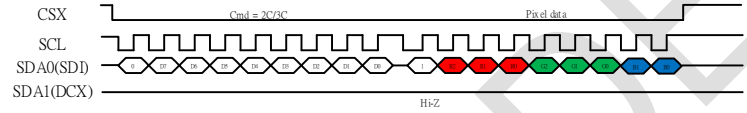
SPI3, RGB666 -> IFPF = 3'b110



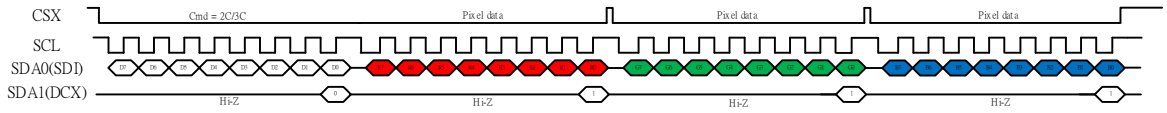
SPI3, RGB565 -> IFPF = 3'b101



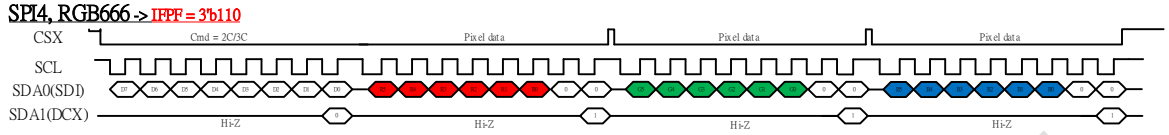
SPI3, RGB332 -> IFPF = 3'b010



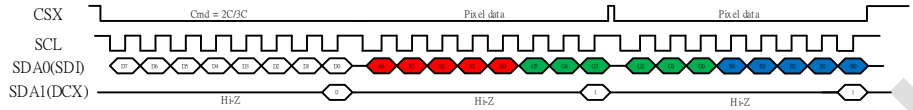
SPI4, RGB888 -> IFPF = 3'b111



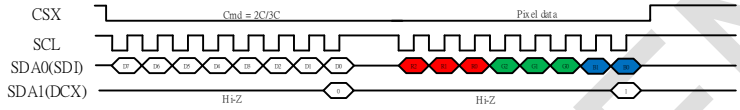
SPI4, RGB666 -> IFPF = 3'b110



SPI4, RGB565 -> IFPF = 3'b101

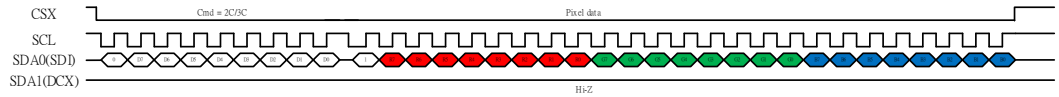


SPI4, RGB332 -> IFPF = 3'b010

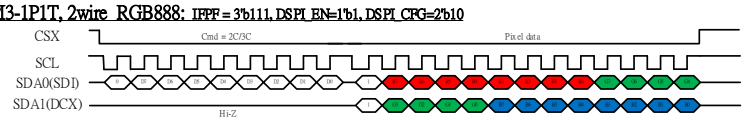


When DSPI_en =1(DUAL-SPI), the host sends data by SDA and DCX.

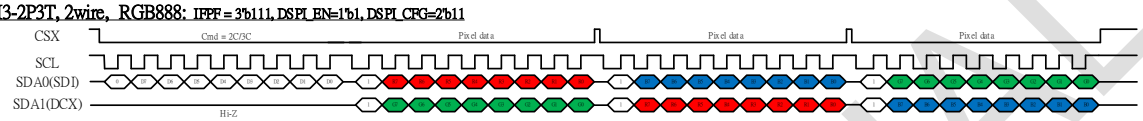
SPI3, 1wire, RGB888: IFPF = 3'b111, DSPI_EN = 1'b1, DSPI_CFG=2'b00



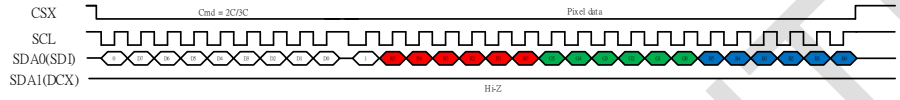
SPI3-1P1T, 2wire RGB888: IFPF = 3'b111, DSPI_EN=1'b1, DSPI_CFG=2'b10



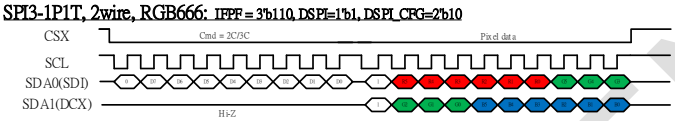
SPI3-2P3T, 2wire, RGB888: IFPF = 3'b111, DSPI_EN=1'b1, DSPI_CFG=2'b11



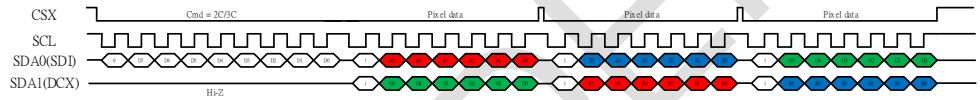
SPI3-1wire, RGB666: IFPF = 3'b110, DSPI_EN=1'b1, DSPI_CFG=2'b00



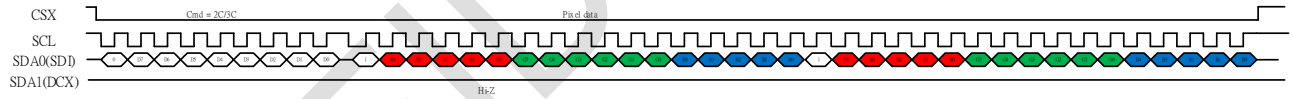
SPI3-1P1T, 2wire, RGB666: IFPF = 3'b110, DSPI=1'b1, DSPI_CFG=2'b10



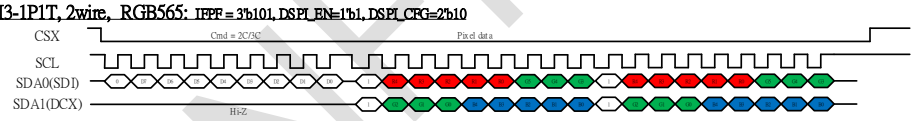
SPI3-2P3T, 2wire, RGB666: IFPF = 3'b110, DSPI_EN=1'b1, DSPI_CFG=2'b11



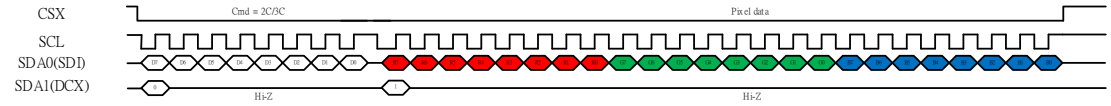
SPI3-1wire, RGB565: IFPF = 3'b101, DSPI_EN=1'b1, DSPI_CFG=2'b00



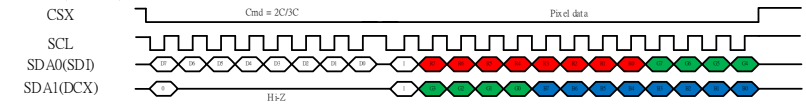
SPI3-1P1T, 2wire, RGB565: IFPF = 3'b101, DSPI_EN=1'b1, DSPI_CFG=2'b10



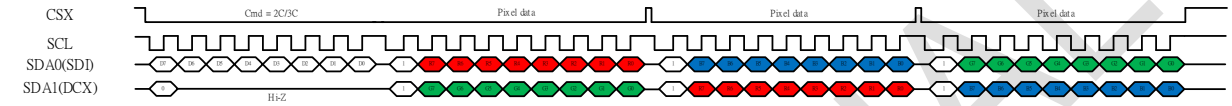
SPI4-1wire, RGB888: IFPF = 3'b111, DSPI_EN=1'b1, DSPI_CFG=2'b00



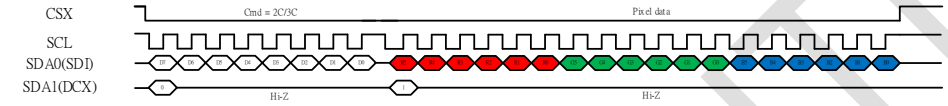
SPI4-1P1T, 2wire, RGB888: IFPF = 3'b111, DSPI_EN=1'b1, DSPI_CFG=2'b10



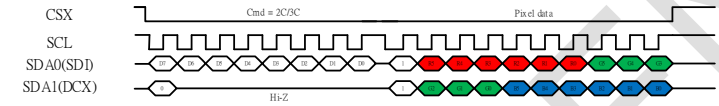
SPI4-2P3T, 2wire, RGB888: IFPF = 3'b111, DSPI_EN=1'b1, DSPI_CFG=2'b11



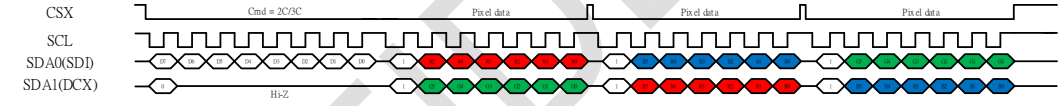
SPI4-1wire, RGB666: IFPF = 3'b110, DSPI_EN=1'b1, DSPI_CFG=2'b00



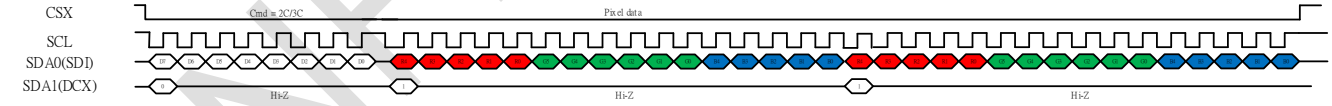
SPI4-1P1T, 2wire, RGB666: IFPF = 3'b110, DSPI_EN=1'b1, DSPI_CFG=2'b10



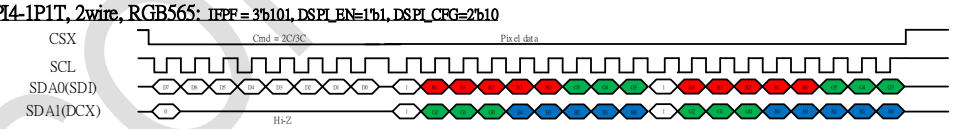
SPI4-2P3T, 2wire, RGB666: IFPF = 3'b110, DSPI_EN=1'b1, DSPI_CFG=2'b11



SPI4-1wire, RGB565: IFPF = 3'b101, DSPI_EN=1'b1, DSPI_CFG=2'b00



SPI4-1P1T, 2wire, RGB565: IFPF = 3'b101, DSPI_EN=1'b1, DSPI_CFG=2'b10



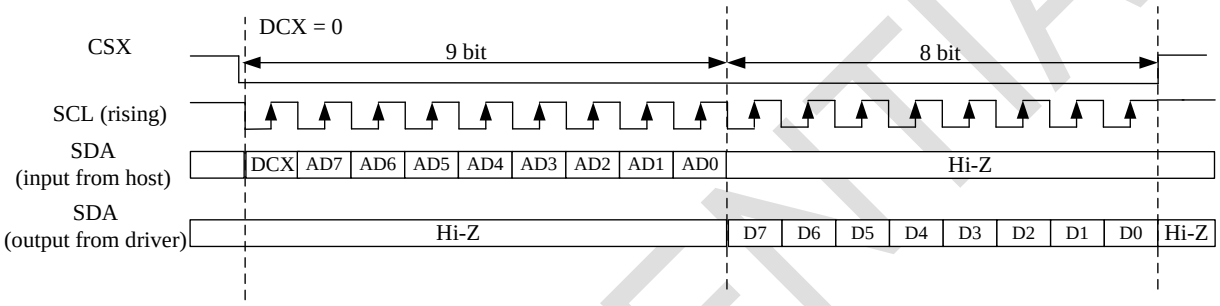
5.3 3-wire / 4-wire SPI Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The 3-wire/4-wire SPI interface utilizes CSX, SCL and SDA signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL.

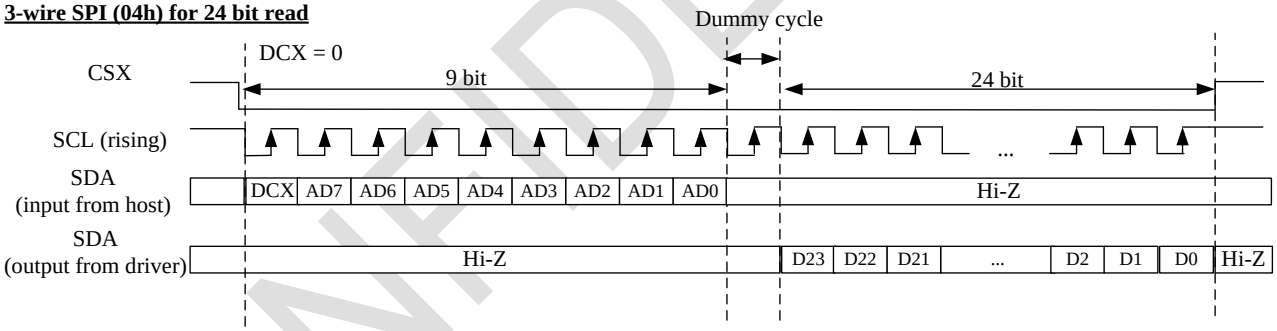
During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. The 3-wire serial data contains DCX bit and a transmission byte. DCX is driven low while command information is on the interface and is pulled high when data is present.

The 3-wire/4-wire SPI interface read command sequences are described in the following figure.

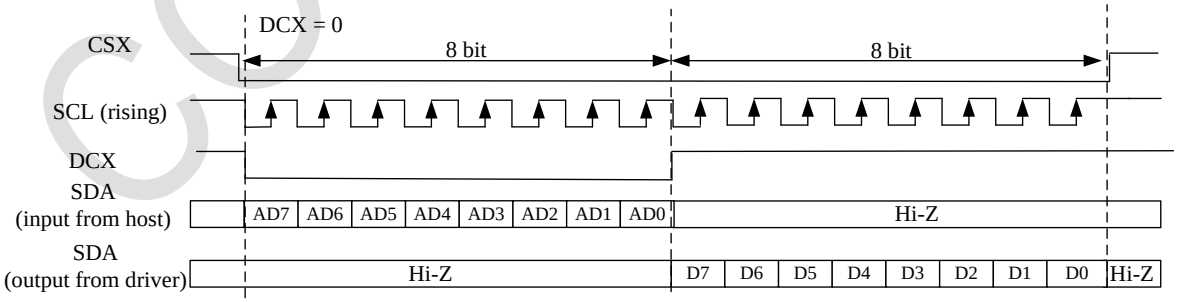
3-wire SPI (0Ah/0B/0Ch/0Dh/0Eh/0Fh/DAh/DBh/DCh) for 8 bit read



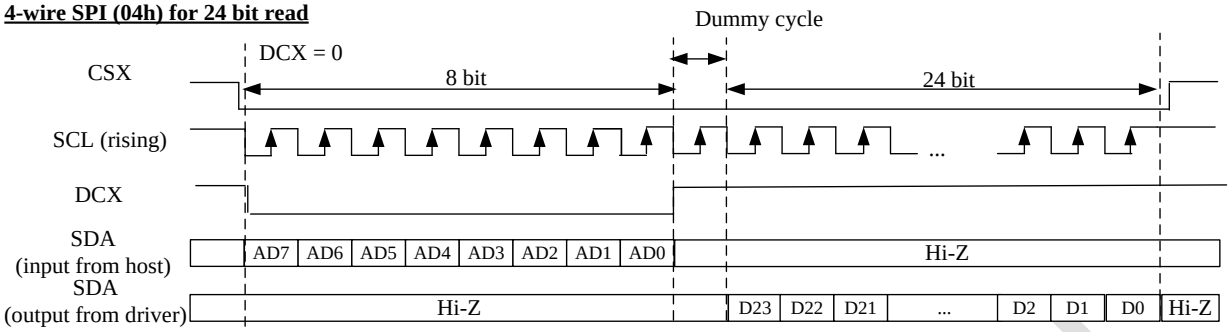
3-wire SPI (04h) for 24 bit read



4-wire SPI (0Ah/0B/0Ch/0Dh/0Eh/0Fh/DAh/DBh/DCh) for 8 bit read



4-wire SPI (04h) for 24 bit read

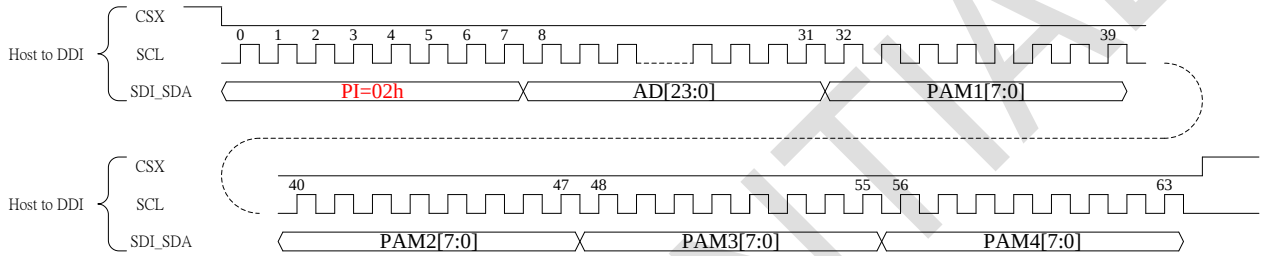


5.4 QUAD-SPI protocol

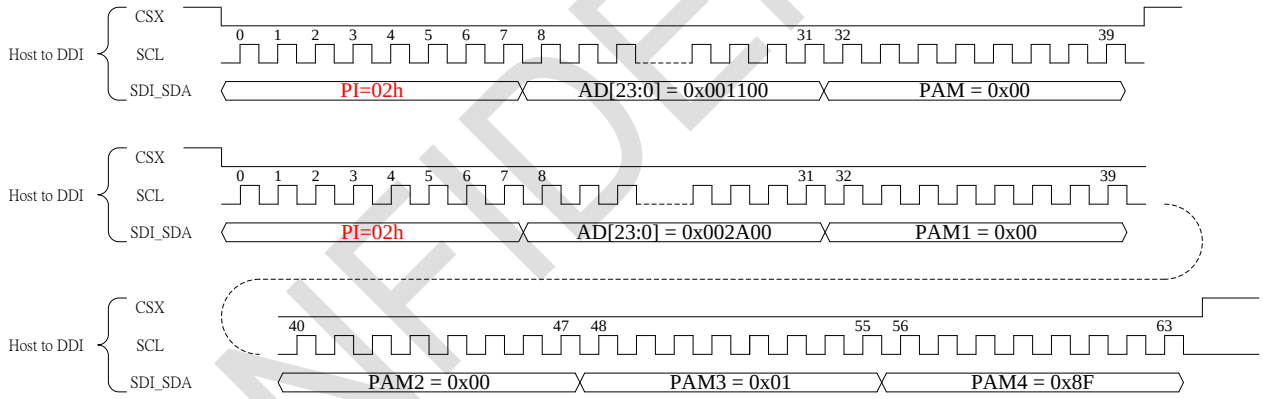
QUAD-SPI provides 1-wire for writing / reading command, and 4-wire for writing pixel data. CSX is the chip selection and it is low active property. SCL is driven from high to low then pulled back to high during the write cycle for clock input. SDI_SDA is for 1-wire command writing (PI=02h), 1-wire command reading (PI=03h) and 4-wire pixel data transmission (PI=12h or 32h). DCX and D[1:0] are for 4-wire mode pixel data transmission.

5.5 QUAD-SPI command format

The QUAD-SPI interface write command sequences are described in the following figure.
AD[23:0] is the command address and its contend is {8'h00, CMD[7:0], 8'h00}.
PAM*[7:0] is the command parameter, and PI[7:0] is the packet instruction for QUAD-SPI protocol format decoding.



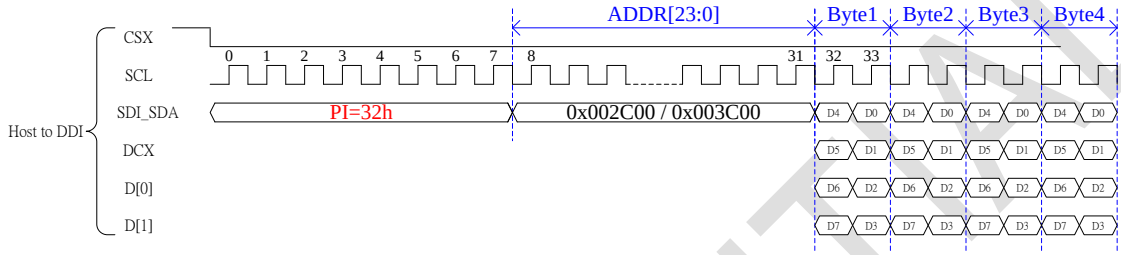
For example: SLPOUT and memory column setting (multi parameters)



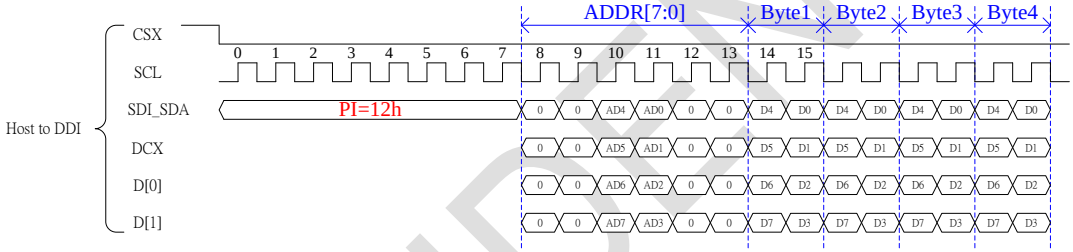
5.6 QUAD-SPI pixel writing format

The QUAD-SPI interface write pixel data sequences are described in the following figure.
AD[23:0] is the driver IC command address, 0x002C00 or 0x003C00.
Data*[7:0]: the pixel data

Two kinds of ADDR format which is distinguished by the preceding packet (32h or 12h).
ADDR is 24bits: ADDR is made up 002C00 or 003C00



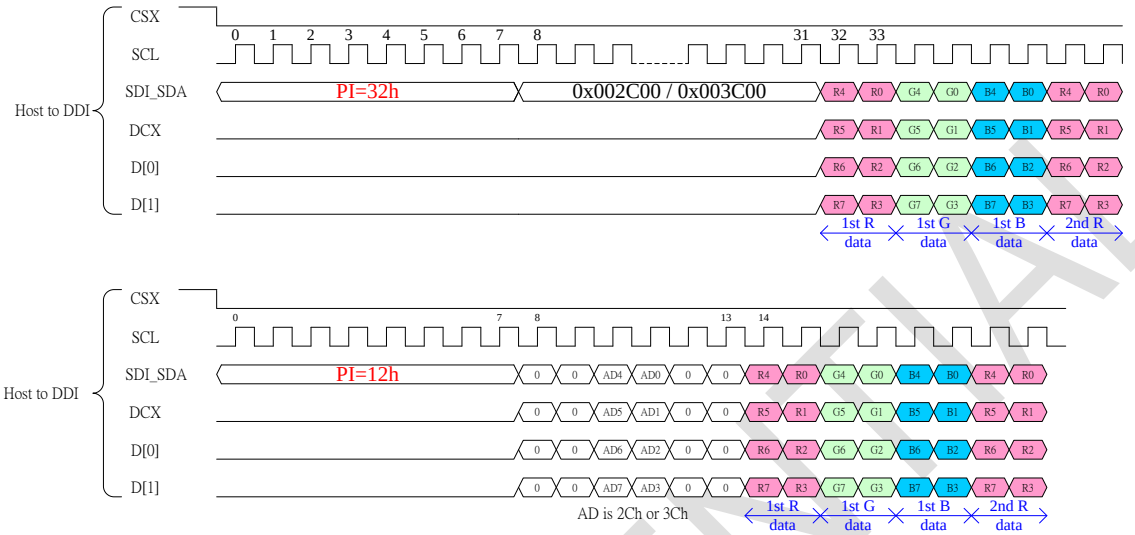
ADDR is 8bits: ADDR is 2C or 3C



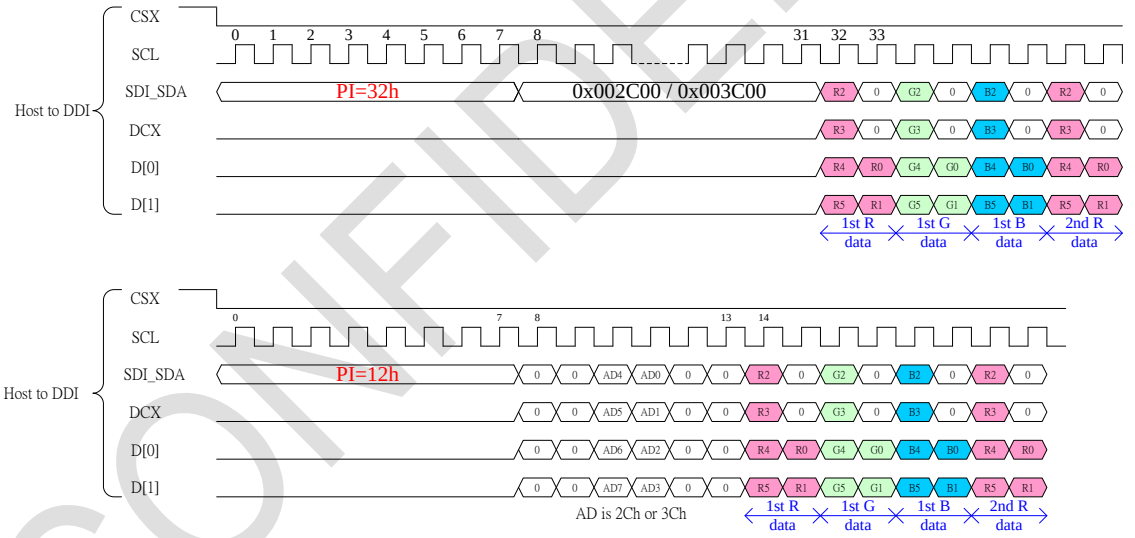
5.7 QUAD-SPI pixel writing color format

The QUAD-SPI interface supported RGB888, RGB666, RGB565, RGB332 for the following formats.

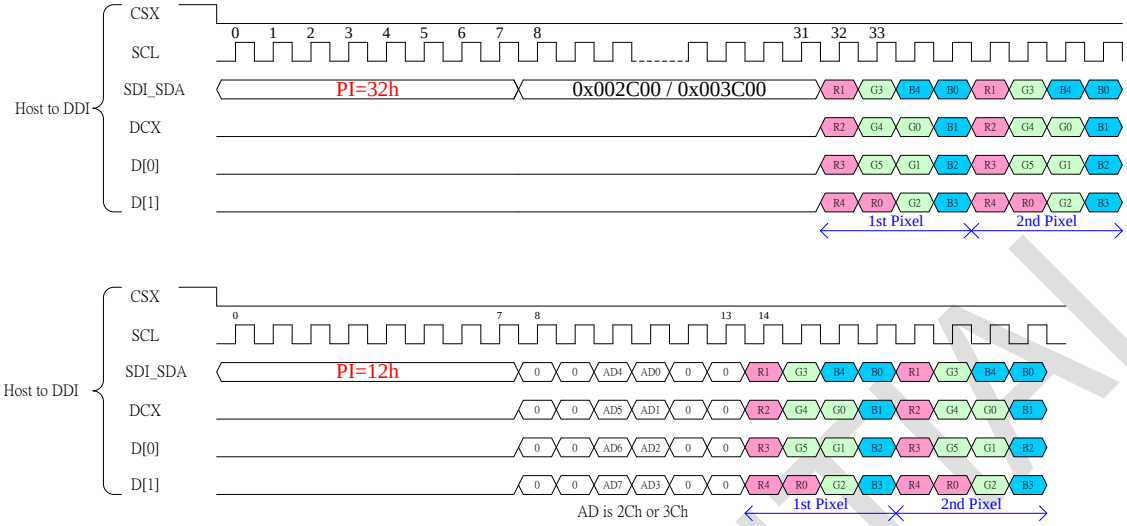
RGB888:



RGB666:



RGB565:

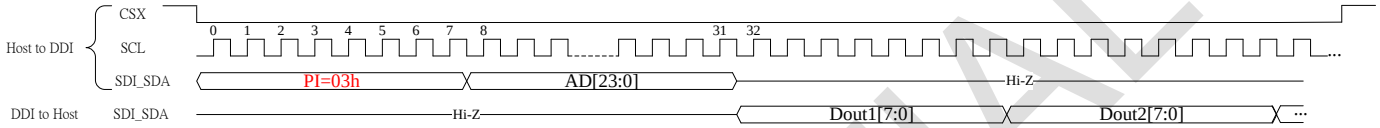


5.8 QUAD-SPI Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The QUAD-SPI interface utilizes CSX, SCL and SDI_SDA signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high.

QUAD-SPI read format:



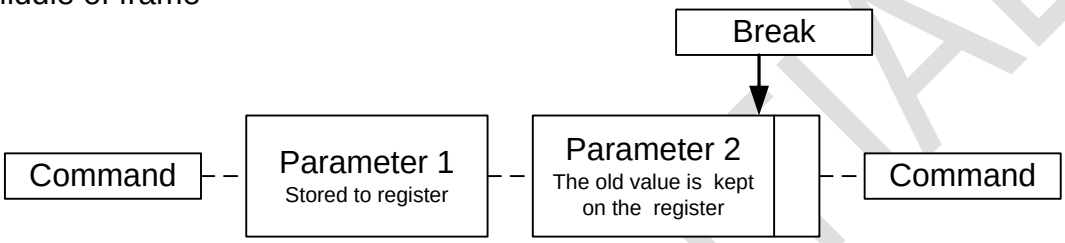
AD is made up {8'h00, CMD[7:0], 8'h00}

5.9 Break and Pause Sequence

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

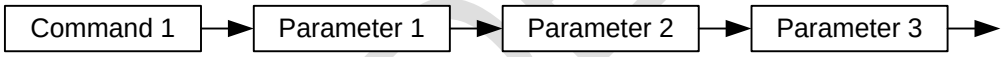
The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

1. Middle of frame

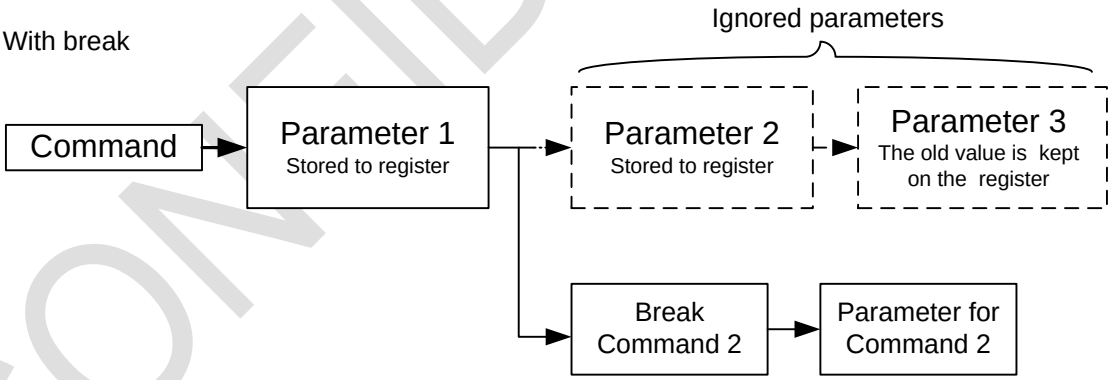


2. Between frames

Without break



With break



Break can be e.g. another command or noise pulse.

5.10 Display Serial Interface (DSI)

DSI-compliant peripherals support either of two basic modes of operation, *Command Mode* and *Video Mode*. The mode definitions reflect the intended use of DSI for display interconnect but not intend to restrict DSI from operating in other applications.

Command Mode refers to the operation in which transactions primarily take the form of sending commands to a display module, which incorporates a display controller including local registers. It requires a bidirectional interface so that systems can utilize this mode to write data onto or to read data from those local registers. The host processor indirectly controls activity of the peripheral by sending commands and parameters to the display controller. Moreover, the host processor can also read status information of a display module via it.

Video Mode refers to operation in which a real-time pixel stream data send from the host processor to the peripheral. Under normal operation, display module relies on host processor to transmit image data with sufficient bandwidth to avoid flicker or other visible artifacts shown in the displayed image. Video information should only be transmitted by using High Speed Mode.

Configuration between the host and client

Lane Pair	Available Operation Mode	Clock/Data Input Mode
Clock Lane	Unidirectional Clock Lane	Forward High-Speed Clock Input
Data Lane 0	Bi-directional Data Lane Bi-directional Escape Mode	Forward High-Speed Data Input Bi-directional LPDT
Data Lane 1	Unidirectional Data Lane Escape Mode	Forward High-Speed Data Input No LPDT
Data Lane 2	Unidirectional Data Lane Escape Mode	Forward High-Speed Data Input No LPDT
Data Lane 3	Unidirectional Data Lane Escape Mode	Forward High-Speed Data Input No LPDT

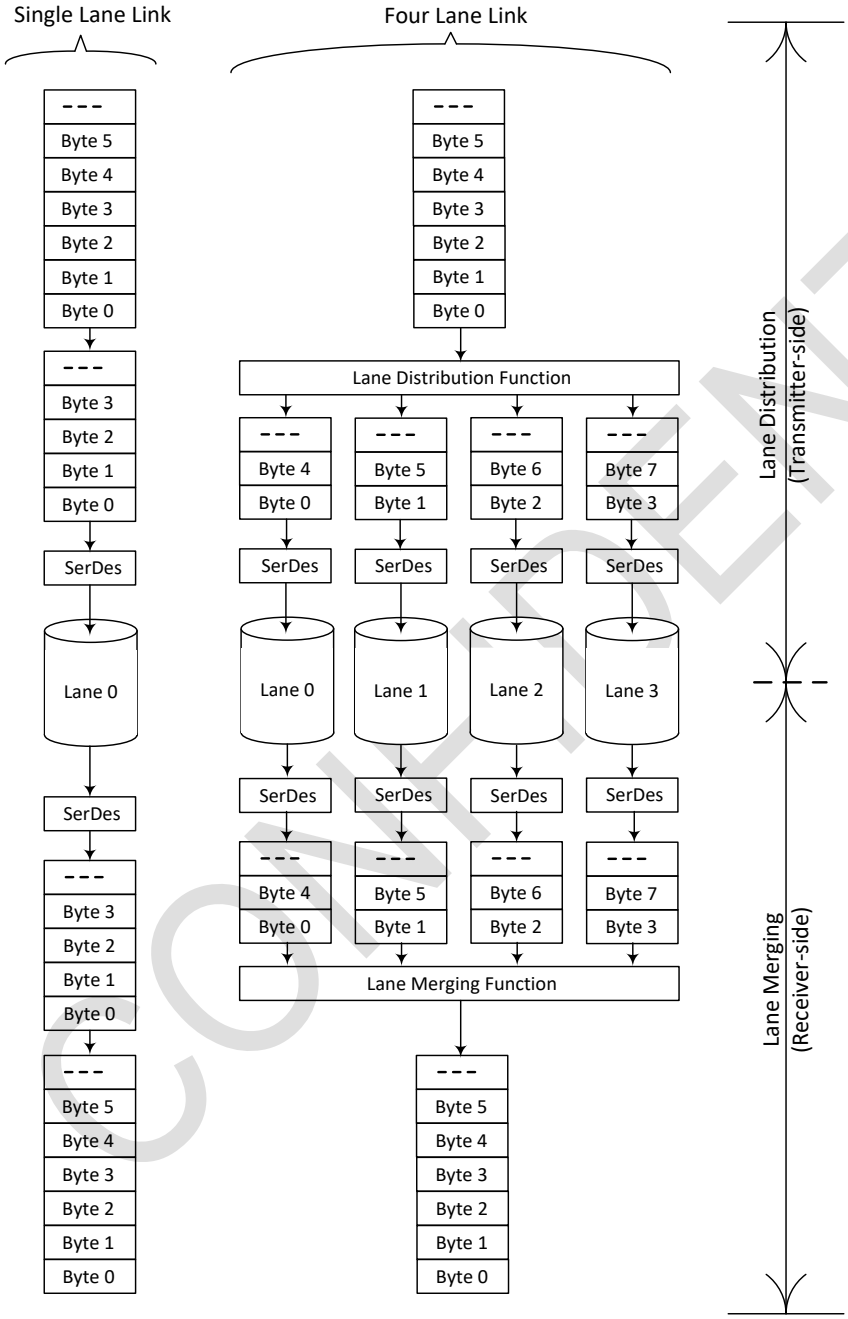
Notes:
1. We recommend users to stay in *STOP* state for 500ns when switching from LPDT to HSDT.
2. We recommend users to adopt *EoTp* to enhance overall robustness of the system during HSDT.

5.11 Video Mode Format Support

Video Mode	Support
Burst mode	Yes
Non burst mode	Yes
Sync event mode	Yes
Sync pulses mode	Yes

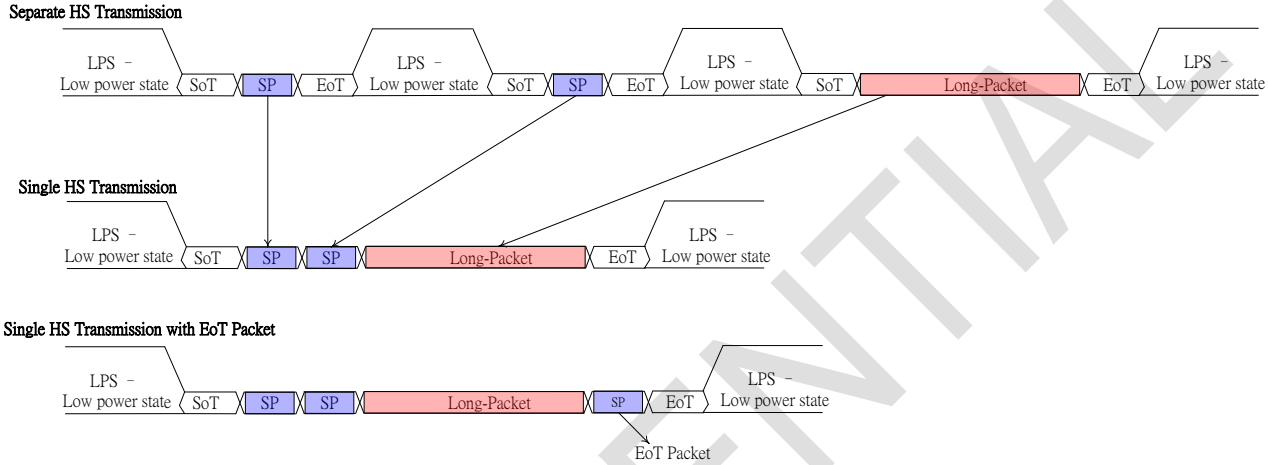
5.12 Multi-Lane Distribution and Merging

On the transmitter side of a *DSI Link*, parallel data, signal events, and commands are converted to packets and sent across the serial Link. On the other hand, the receiver side of a *DSI Link* performs the data conversion, decomposing deceived packets into parallel data, signal events and commands. The data processing flow is shown in the following for one-lane operation (left-side) and four-lane operation (right-side).



5.13 Multiple Packet per Transmission

There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS data transmission can be started, the transmitter issues a SoT sequence to the receiver. After that, data or command packets can be transmitted via HS mode. Multiple packets may exist within a single HS transmission and at the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In HS mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT issued by the PHY layer between packets.



Operation State:

LPS -- Low Power State (also called LP-11)

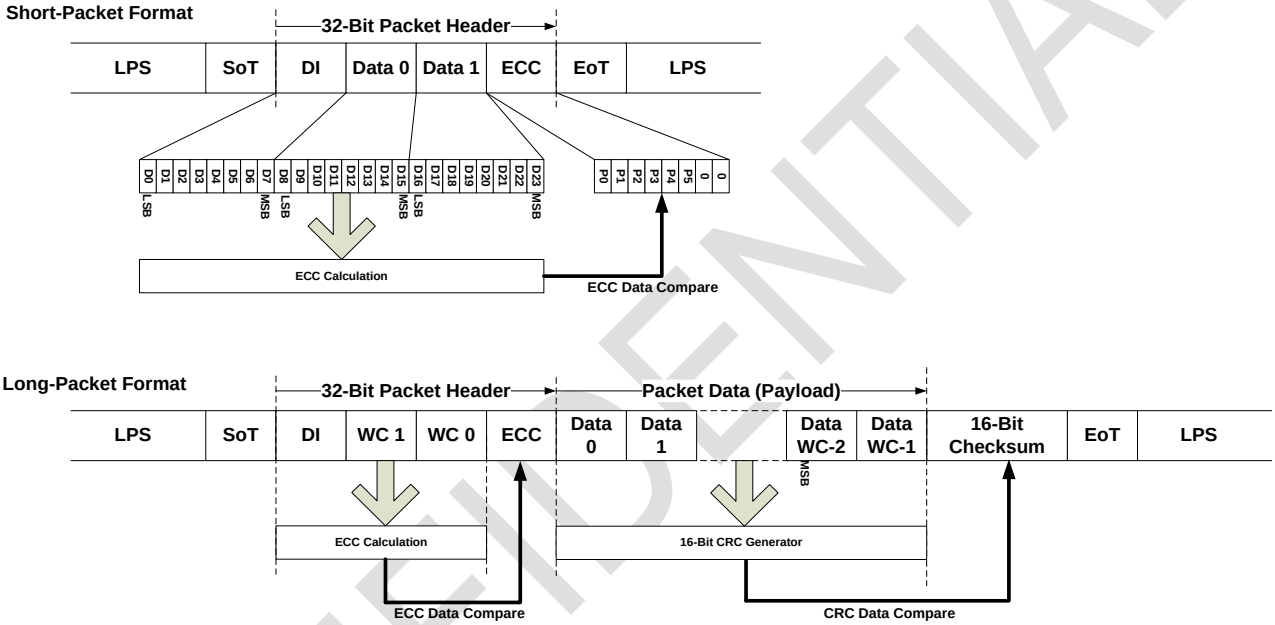
SoT -- Start-of-Transmission

EoT -- End-of-Transmission

5.14 Packet Composition

There are two categories of packet size, and they are *short* packets and *long* packets, respectively. Short packets are four bytes in length including the 1 byte DI (data identifier), 2 byte data, and 1 byte ECC (error correction code) for the packet header.

As to the long packets, they comprise of 1 byte DI, 2 byte WC (word count), Data 0, Data 1…Data WC-1, and finally 2 byte checksum. *Word Count* represents the number of total data bytes of this long packet, and *Checksum* is a 16-bit CRC generator to check packet data. If the calculated checksum of receiver is equal to the number contained in the packet, then those packet data are regard as correct. However, if the comparison result is non-equal, the packet data are considered to be incorrect. The packet formats of both short packet and long packet are depicted in the following.



The byte DI[7:0] (data identifier) contains of two important information. One is the peripheral selection through the 2-bit virtual channel identifier VC=DI[7:6], and the other is the 6-bit data type field DT=DI[5:0]. The VC is always 2'b00 for the real application. The data type field specifies the short or long packet type and the packet format.

Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

ECC shall always be generated and appended in the Packet Header from the host processor. Peripherals with Bidirectional Links shall also generate and send ECC. The byte ECC allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

The number of parity or error check bits required is given by the Hamming rule, which uses parity to correct a single-bit error or detect a two-bit error, but are not capable of doing both simultaneously. DSI uses Hamming-modified codes where an extra parity bit is used to support both single error correction as well as two-bit error detection.

Since Packet Headers are fixed at four bytes (twenty-four data bits and eight ECC bits), P6 and P7 of the ECC byte are unused and shall be set to zero by the transmitter. The receiver shall ignore P6 and P7 and set both bits to zero before processing ECC. The parity bits of ECC are defined as below:

P7 = 0

P6 = 0

P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

ECC Parity Generation Rules, the encoding of parity and decoding of syndromes:

Data Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
0	0	0	0	0	0	1	1	1	0x07
1	0	0	0	0	1	0	1	1	0x0B
2	0	0	0	0	1	1	0	1	0x0D
3	0	0	0	0	1	1	1	0	0x0E
4	0	0	0	1	0	0	1	1	0x13
5	0	0	0	1	0	1	0	1	0x15
6	0	0	0	1	0	1	1	0	0x16
7	0	0	0	1	1	0	0	1	0x19
8	0	0	0	1	1	0	1	0	0x1A
9	0	0	0	1	1	1	0	0	0x1C
10	0	0	1	0	0	0	1	1	0x23
11	0	0	1	0	0	1	0	1	0x25
12	0	0	1	0	0	1	1	0	0x26
13	0	0	1	0	1	0	0	1	0x29
14	0	0	1	0	1	0	1	0	0x2A
15	0	0	1	0	1	1	0	0	0x2C
16	0	0	1	1	0	0	0	1	0x31
17	0	0	1	1	0	0	1	0	0x32
18	0	0	1	1	0	1	0	0	0x34
19	0	0	1	1	1	0	0	0	0x38
20	0	0	0	1	1	1	1	1	0x1F
21	0	0	1	0	1	1	1	1	0x2F
22	0	0	1	1	0	1	1	1	0x37
23	0	0	1	1	1	0	1	1	0x3B

5.15 Processor-to-Peripheral Transactions

■ **Sync Event packet**

Sync Events are all short packets and time-accurately. They can perform like the start and end of sync pulses. To represent timing information as accurately as possible, a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Hence, a V Sync End event implies an H Sync Start event for the last line of the VSA. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty if keeping data line(s) in HS mode.

Data Type	Data Type (Binary)	Description	Packet size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short

■ **End-of-Transmission EoT packet**

This short packet is used to indicate the end of a high speed (HS) transmission, and it will enhance overall system reliability. Although the main objective of the EoT packet is to enhance robustness of HS transmission, DDI can also detect and interpret arriving EoT packet even in LP mode.

Data Type	Data Type (Binary)	Description	Packet size
08h	00 1000	End of Transmission packet (EoTp)	Short

■ **Generic Short Write / Read packet**

Generic Short WRITE request is a short packet for sending data to the peripheral. Generic READ request is a short packet for acquiring data from the peripheral.

Data Type	Data Type (Binary)	Description	Packet size
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short

■ **DCS Short Write / Read packet**

DCS short write command is used to write a single data byte command to display module. If there is a valid parameter byte, data type bit 4 shall be set to 1. If there is no valid parameter byte, data type bit 4 shall be set to 0 and the parameter byte shall be 00h. DCS read command is used to request data from DDI.

Data Type	Data Type (Binary)	Description	Packet size
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short

■ **Generic Long Write**

This is used to transmit arbitrary blocks of data from a host processor to a peripheral.

Data Type	Data Type (Binary)	Description	Packet size
29h	10 1001	Generic Long Write	Long

■ **DCS Long Write**

The commands are used to send larger blocks of data to a display module.

Data Type	Data Type (Binary)	Description	Packet size
39h	11 1001	DCS Long Write / write_LUT Command Packet	Long

■ **Set Maximum Return Packet Size**

This command specifies the maximum size of the payload in a long packet transmission from a display module to host processor.

Data Type	Data Type (Binary)	Description	Packet size
37h	11 0111	Set Maximum Return Packet Size	Short

■ **Null Packet**

This is a mechanism for keeping the data lane(s) in high speed mode while sending dummy data.

Data Type	Data Type (Binary)	Description	Packet size
09h	00 1001	Null Packet, no data	Long

■ **Blanking Packet**

A Blanking packet is used to convey blanking timing information in a Long packet. The packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Blanking packets may contain arbitrary data as payload.

Data Type	Data Type (Binary)	Description	Packet size
19h	01 1001	Blanking Packet, no data	Long

■ **Reserved Data Packet**

Data Type	Data Type (Binary)	Description	Packet size
02h	00 0010	reserved	Short
12h	01 0010	reserved	Short
22h	10 0010	reserved	Short
32h	11 0010	reserved	Short
03h	00 0011	reserved	Short
04h	00 0100	reserved	Short

24h	10 0100	reserved	Short

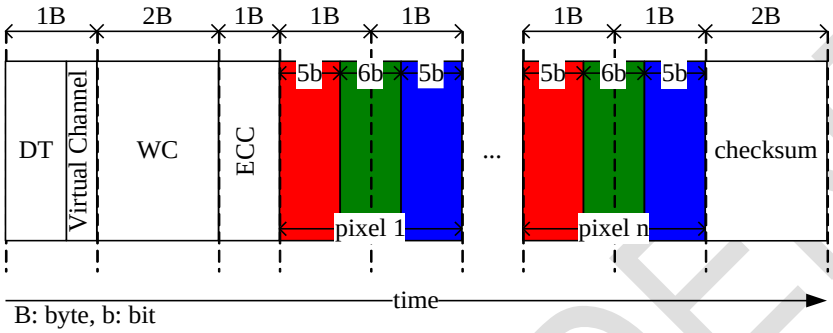
5.16 Packed Pixel Stream Format

There are 4 kinds of data input formats, and they are 16-bit RGB(5-6-5), loosely packed 18-bit RGB(6-6-6), and 24-bit RGB(8-8-8) data format. They have their own data type as shown in the following table.

Data Type	Data Type (Binary)	Description	Packet size
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

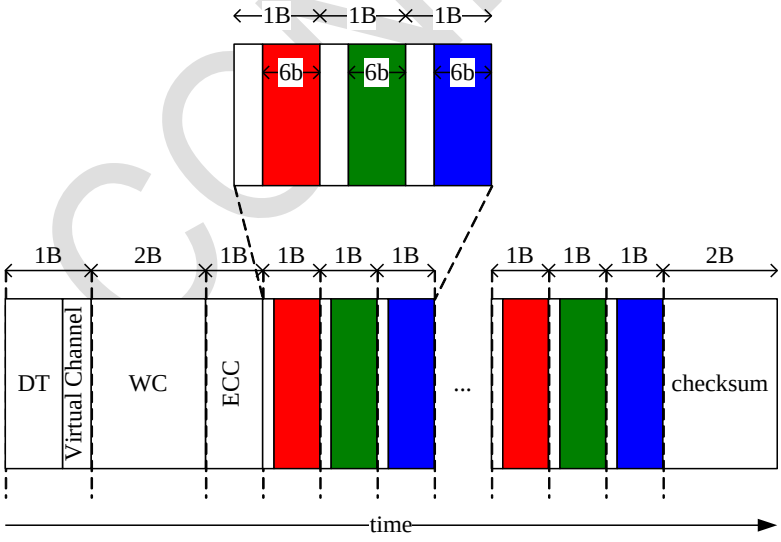
■ **16-bit Format, Data Type: 0x0Eh**

The pixel data of this 16-bit data format comprise of five bits red, six bits green, and five bits blue. The green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.



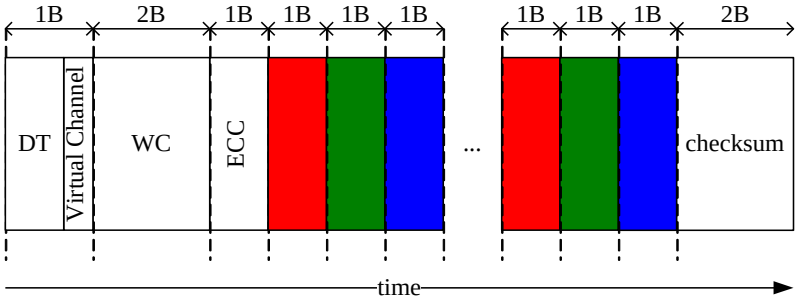
■ **18-bit Loosely Packed Format, Data Type: 0x2Eh**

The pixel data of this 18-bit pixel loosely packed format comprises of six bits red, six bits green, and six bits blue. But, the difference between this format and previously mentioned compact format is each R, G or B color component is the same six bits but shifted 2bits to the upper bits of byte. Within a color component, the LSB is sent first, the MSB last.



■ **24-bit Format, Data Type: 0x3Eh**

The pixel data of this 24-bit data format is eight bits red, eight bits green and eight bits blue. Within a color component, the LSB is sent first, the MSB last.



5.17 Peripheral-to-Processor (Reverse Direction) LP Transactions

All command-mode systems require bidirectional capability to transmit and receive READ data, acknowledge, error information and etc. to the host processor. Multi-Lane system shall use Data Lane-0 for all peripheral-to-processor transmission. And the transmission is allowable only under low-power mode.

Packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction, *Short* and *Long* packet structures. BTA sequence, that is used to pass the bus control from one to the other, shall take place soon after every peripheral-to-processor transaction. There are four major data transmission from a peripheral to its processor:

- *Tearing Effect.* It is a Trigger message sent to convey display timing information to the host processor.
- *Acknowledge*. It is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication, either triggers or packets, is received by the peripheral with no errors. Please refer to section 6.2.5 for the detailed description.
- *Acknowledge and Error Report*: It is a Short packet sent if any errors were detected in preceding transmissions from the host processor. Please refer to section 6.2.6 for the detailed description.
- *Response to Read Request*. It may be a Short or Long packet that returns data requested by the preceding READ command from the processor. Please refer to section 6.2.7 for the detailed description.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packets, and then return bus control to the host processor. Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

- Following a non-Read command, the peripheral shall respond with *Acknowledge* if no errors were detected or stored since the last peripheral to host communication.
- Following a Read request, the peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication.
- Following a Read request, if only a *single-bit ECC error* was detected and corrected, the peripheral shall send the requested READ data in a long or short packet, followed by a 4-byte *Acknowledge and Error Report* packet in the same LP transmission.
- Following a non-Read command, if only a *single-bit ECC error* was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte *Acknowledge and Error Report* packet.
- Following a Read request, if multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte *Acknowledge and Error Report* packet without sending Read data.
- Following a non-Read command, if multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte *Acknowledge and Error Report* packet.
- Following any command, if SoT Error, SoT Sync Error, or DSI VC ID invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte *Acknowledge and*

Error Report response, with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication, in the two-byte error field.

- Following any command, if EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte *Acknowledge and Error Report* packet with appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

Acknowledge and Error Report confirms that the preceding command or data sent from the processor to a peripheral was received and indicates what type of error detected on the transmissions. Error report is of short packet type that comprised of two bytes following the data identifier byte (Byte-0). An ECC byte (Byte-3) follows the two error report bytes to form a complete short packet. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”. The following table shows the bit assignment for all error report:

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Reserved
14	Reserved
15	Reserved

5.18 Peripheral-to-Processor Transaction – Detail Format Description

- ***Acknowledge and Error Repor***t

It is sent in response to any command, or read, request, with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.

Data type (hex)	Description	Packet size
02h	Acknowledge and Error Report	Short

- ***Generic Short Read Response***

It is a short-packet response to *Generic READ Request*. Packet composition is data identifier (DI) byte, two bytes payload, and one ECC byte. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

Data type (hex)	Description	Packet size
11h	Generic Short Read Response, 1 byte returned	Short
12h	Generic Short Read Response, 2 bytes returned	Short

- ***Generic Long Read Response***

It is a long-packet response to *Generic READ Request*. Packet composition is DI byte, two bytes Word Count, ECC byte, N bytes of payload, and two bytes Checksum. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

Data type (hex)	Description	Packet size
1Ah	Generic Long Read response	Long

- ***DCS Long Read Response***

It is a long-packet response to *DCS Read Request*. Packet composition is DI byte, two bytes Word Count, ECC byte, N bytes payload, and two bytes Checksum. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

Data type (hex)	Description	Packet size
1Ch	DCS Long Read response	Long

- ***DCS Short Read Response***

It is a short-packet response to *DCS Read Request*. Packet composition is DI byte, two bytes payload, and ECC byte. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

Data type (hex)	Description	Packet size
21h	DCS Short Read Response, 1 byte returned	Short
22h	DCS Short Read Response, 2 bytes returned	Short

5.19 Tearing Effect Output

The tearing effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

Tearing Effect Line Mode

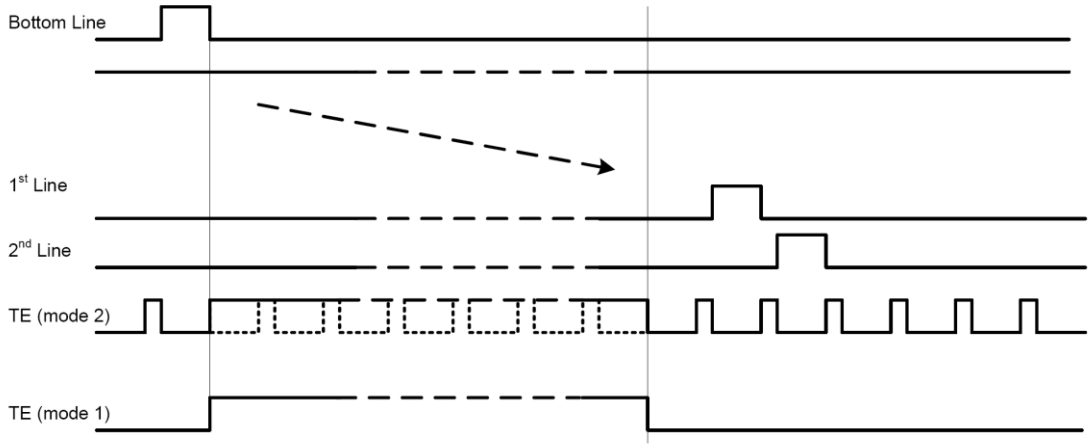
Mode 1, the tearing effect output signal consists of V-sync information only:

tvdh = The display is not updated from the frame memory.
tvdl = The display is updated from the frame memory.

Mode 2, the tearing effect output signal consists of V-sync and H-sync information:

thdh = The display is not updated from the frame memory.
thdl = The display is updated from the frame memory.

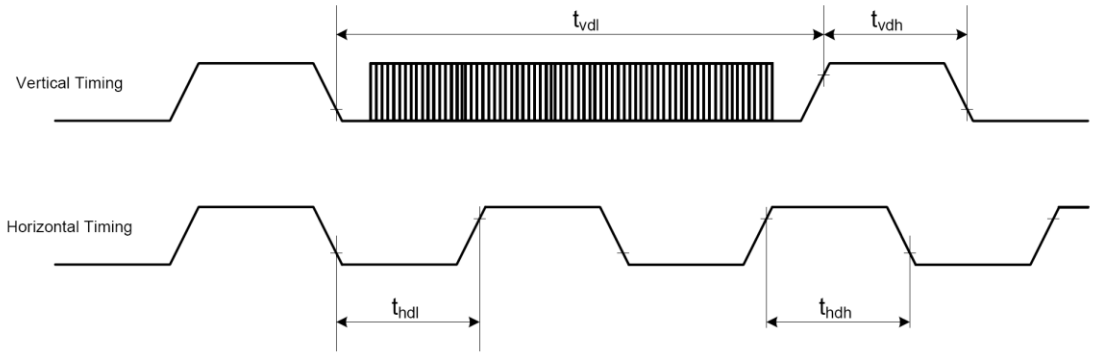
Note. V-sync signal can be used as reference point to prevent tearing effect.
Any data writing must align with V-sync signal. Only once data writing will be allowed during one V-sync interval.



Note. During Sleep In mode, the tearing effect output signal is active low.

Tearing Effect Line Timing

The tearing effect signal is described as below:

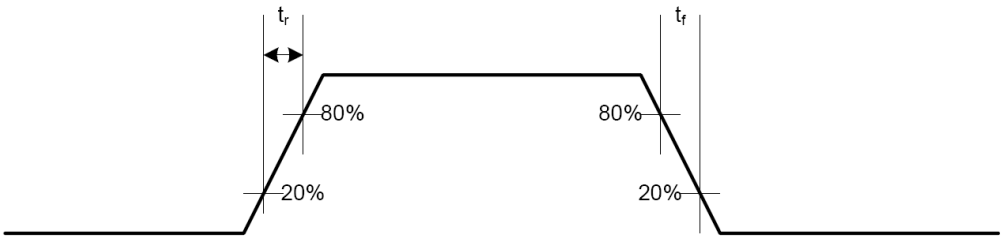


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
tvdl	Vertical timing low duration	TBD	TBD	ms	It depends on the vertical timing setting.
tvdh	Vertical timing high duration	TBD	TBD	us	It depends on the vertical timing setting.
thdl	Horizontal timing low duration	TBD	TBD	us	It depends on the horizontal timing setting.
thdh	Horizontal timing high duration	1.8	TBD	us	

Notes:

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the HOST and should be used as shown below to avoid tearing effect:

The Tearing Effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

TEON (0x35h)	TELOM(0x35h[0])	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

5.20 Picture Parameter Set (PPS)

5.20.1 Compression Mode Command, Data Type = 00 0111 (0x07)

Some display stream compression parameters may be configured using the Compression Mode Command, which is a short packet consisting of a DI byte, a two-byte payload and an ECC byte. This packet signals whether compression is enabled or disabled and the coding system used to create a bitstream or codestream that is carried by the Compressed Pixel Stream data type transaction. This data type writes the compression mode parameters listed in Table PPS setting to the peripheral in advance of the codestream with timing dependency.

Table PPS setting

SP Byte	Bit Location	Bit Description And Assigned Values
Data 0	7:6	Reserved, bits equal 0
Data 0	5:4	PPS selector 00 = PPS Table 1
Data 0	3	Reserved
Data 0	2:1	Algorithm identifier 00 = VESA DSC Standard 1.1 11 = vendor-specific algorithm 01, 10 = reserved, not used
Data 0	0	0 = compression disabled (default) 1 = compression enabled
Data 1	7:0	Reserved, bits equal 0

The Command mode contains a two-bit PPS Selector that may be used to enable a pre-stored PPS Table for controlling the compression decoder parameters. The processor sends this data type to change the decoder parameters that shall take effect following the next vertical sync or internal vertical sync (if using command mode). The PPS Selector is an optional field; if no table is stored in the receiver, the selector shall be 00b.

5.20.2 Picture Parameter Set (0x0A)

The Picture Parameter Set (PPS) data type is a long packet used to transmit a pre-defined set of parameters that control a compression coding system. The packet shall consist of a DI byte, a two-byte, non-zero WC, an ECC byte, a payload containing WC bytes, and a two-byte checksum.
The size, content and timing context of this long packet is defined by the coding system designated in the Compression Mode data type,Compression Mode Command, and transported in the Compressed Image Format data type, Compressed Pixel Stream. Using this long packet, for example, may replace adding header markers to a bitstream.

If the peripheral receiver supports multiple, stored PPS tables, the received new PPS data is stored in the table designated by the Compression Mode PPS Selector if the table is writable.

5.20.3 Compressed Pixel Stream, Long Packet, Data Type = 00 1011 (0x0B)

The Compressed Pixel Stream is a long packet that carries compressed data to a Video Mode display module. This packet shall consist of a DI byte, a two-byte non-zero WC, an ECC byte, a payload containing WC bytes and a two-byte checksum, shown in Figure 30.

This is an optional packet, but if the pixel data is compressed, this packet shall carry the compressed image data when the Compression Mode packet (Compression Mode Command,) has signaled that compression is enabled.

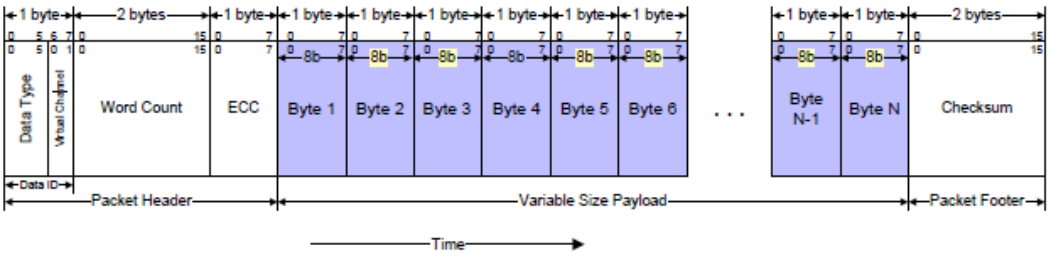


Figure 30 Compressed Pixel Stream Format, Long Packet

6. Command

6.1 Command List

Table of User Command Set (Command 1)

CMD1	Para	Instruction	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	-	NOP	No argument								-
01h	-	Soft reset	No argument								-
05h	-	Get number of errors on DSI	D[7:0]								00h
0Ah	00h	Get power mode	BSTON	IDMON	PTLON	SLPOUT	NORON	DISPON	-	-	-
0Bh	00h	Get address mode	-	MX	-	-	-	-	-	-	00h
0Ch	00h	Get pixel format	SPI_IFPF_SEL	VIPF2	VIPF1	VIPF0	-	IFPF2	IFPF1	IFPF0	77h
0Dh	00h	Get display mode	-	-	INVON	ALLPON	ALLPOFF	-	-	-	00h
0Eh	00h	Get signal mode	TEON	TELOM	-	-	-	-	-	ERR	00h
0Fh	00h	Get diagnostic result	-	-	-	-	-	-	-	CMP_BIT	00h
10h	-	Enter sleep mode	No argument								-
11h	-	Exit sleep mode	No argument								-
12h	-	Enter partial mode	No argument								
13h	-	Enter normal mode	No argument								
20h	-	Exit invert mode	No argument								-
21h	-	Enter invert mode	No argument								-
22h	-	Set all pixels off	No argument								-
23h	-	Set all pixels on	No argument								-
28h	-	Set display off	No argument								-
29h	-	Set display on	No argument								-
2Ah	00h	Set column address	SC[10:8]								00h
	01h		SC[7:0]								00h
	02h		EC[10:8]								02h
	03h		EC[7:0]								CFh
2Bh	00h	Set row (page) address	SP[10:8]								00h
	01h		SP[7:0]								00h
	02h		EP[10:8]								04h
	03h		EP[7:0]								FFh
2Ch	-	Write memory start	-								-
2Fh	00h	HFR Control									00h
30h	00h	Set partial rows	SR[10:8]								00h
	01h		SR[7:0]								00h
	02h		ER[10:8]								04h
	03h		ER[7:0]								FFh
31h	00h	Set partial columns	SC[10:8]								00h
	01h		SC[7:0]								00h
	02h		EC[10:8]								02h
	03h		EC[7:0]								CFh
34h	-	Set tear off	No argument								-
35h	00h	Set tear on	-	-	-	-	-	-	-	TELOM	00h
36h	00h	Set address mode	-	MX	-	-	-	-	-	-	00h
38h	-	Exit idle mode	No argument								-

39h	-	Enter idle mode	No argument								-
3Ah	00h	Set pixel format	SPI_IFPF_SEL	VIPF2	VIPF1	VIPF0	-	IFPF2	IFPF1	IFPF0	77h
3Ch	-	Write memory continuous	-								-
44h	00h	Set tear scan line	STS[15:8]								00h
	01h		STS[7:0]								00h
4Fh	00h	Set deep standby mode	-	-	-	-	-	-	-	DSTB	00h
51h	00h	Write display brightness	DBV[11:8] (input)								00h
	01h		DBV[7:0] (input)								00h
52h	00h	Read display brightness	DBV[11:8] (output)								00h
	01h		DBV[7:0] (output)								00h
53h	00h	Dimming Control for BC	-	-	1	-	BC_DIM_EN	-	-		20h
54h	00h	Read control display	-	-	1	-	BC_DIM_EN	-	-		20h
55h	00h	Write RAD-ACL control	-	-	-	-	-	-	RAD_ACL[1:0]		00h
56h	00h	Read RAD-ACL control	-	-	-	-	-	-	RAD_ACL[1:0]		00h
8Ah	00h	LTPO Control	ltpo_mc[7:0]								00h
	01h		ltpo_en[7:0]								00h
A1h	00h	Read DDB start	SID[15:8]								00h
	01h		SID[7:0]								00h
	02h		MID[15:8]								00h
	03h		MID[7:0]								00h
	04h		RID[15:8]								00h
	05h		RID[7:0]								00h
	06h		1	1	1	1	1	1	1	1	FFh
A8h	00h	Read DDB continue	SID[15:8]								00h
	01h		SID[7:0]								00h
	02h		MID[15:8]								00h
	03h		MID[7:0]								00h
	04h		RID[15:8]								00h
	05h		RID[7:0]								00h
	06h		1	1	1	1	1	1	1	1	FFh
AAh	00h	Read first checksum	FCS[7:0]								00h
AFh	00h	Read continue checksum	CCS[7:0]								00h
FEh	00h	Write CMD page switch	CMD_PG_SEL[7:0]								00h
FFh	00h	Read CMD page	CMD_PG_SEL[7:0]								00h

6.2 Command Description

6.2.1 NOP (0000h)

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	0000h	No Argument								

Description	This command is an empty command; it does not have any effect on the display module. X = Don't care.
Restriction	None

6.2.2 SWRESET(0100h) : Software Reset

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	0100h	No Argument								

Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)
Restriction	Software Reset Command cannot be sent during Sleep Out sequence. Any new command cannot be sent for 10-frame period until the RM69A10 enters Sleep-In mode. Do not send any command.

6.2.3 RDNUMED(0500h) : Read Number of Errors on DSI

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	0500h	D7	D6	D5	D4	D3	D2	D1	D0	00

Description	The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below. D[6..0] bits are telling a number of the parity errors. D[7] is set to “1” if there is overflow with D[6..0] bits. D[7..0] bits are set to “0”s (as well as RDDSM(0Eh)’s D0 are set “0” at the same time) after there is sent the first parameter information (= The read function is completed). This command is used for MIPI DSI only. It is no function for others interface operation.
Restriction	-

6.2.4 RDDPM (0A00h) : Read Display Power Mode

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	0A00h	D7	D6	D5	D4	D3	D2	D1	D0	08

Description

This command indicates the current status of the display as described in the table below:

Bit	Symbol	Description	Comment
D7	BSTON	Booster Voltage Status	'1'=Booster on, '0'=Booster off
D6	IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
D5	PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off
D4	SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In
D3	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
D2	DISON	Display On/Off	'1' = Display On, '0' = Display Off
D1	Reserved		0
D0	Reserved		0

Description

This command indicates the current status of the display as described in the table below:

Bit	Symbol	Description	Comment
D6	MX	Column Address Increment	0: Increasing in horizontal 1: Decreasing in horizontal
others	Reserved	-	-

6.2.5 RDDCOLMOD (0C00h): Read Display Pixel Format

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	0C00h	SPI_IFPF_SEL	VIPF[2]	VIPF[1]	VIPF[0]	0	IFPF[2]	IFPF[1]	IFPF[0]	77

Description

To return the status of 0x3A00.

This command sets the pixel format for the RGB image data used by the interface.

If SPI_IFPF_SEL(3Ah-D7) = 1:
The SPI/QSPI interface will use VIPF[2:0] as pixel format setting specifically, and the other interface will use IFPF[2:0].

If SPI_IFPF_SEL(3Ah-D7) = 0:
All interface will use IFPF[2:0] as pixel format setting

Control Interface Color Format	IFPF[2]	IFPF[1]	IFPF[0]
SPI 8 bit/pixel (256 colors); SPI 3-3-2 (Support IF: SPI3/SPI4/QSPI)	0	1	0
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,144 colors)	1	1	0
24bit/pixel (16.7M colors)	1	1	1

6.2.6 RDDIM (0D00h): Read Display Image Mode

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	0D00h	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

The display module returns the display image mode status.

Bit	Symbol	Description	Comment
D7	Reserved		‘0’
D6	Reserved		‘0’
D5	INVON	Inversion On/Off	“1” = Inversion is On, “0” = Inversion is Off
D4	ALLON	All Pixel On	‘0’ = Normal display ‘1’ = White display
D3	ALLOFF	All Pixel Off	‘0’ = Normal display ‘1’ = Black display
D2~ D0	Reserved		‘000’

6.2.7 RDDSM (0E00h): Read Display Signal Mode

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	0E00h	TEON	TELOM	-	-	-	-	-	ERR	00

Description

The display module returns the Display Signal Mode.

Bit	Symbol	Description	Comment
D7	TEON	Tearing Effect Line On/Off	“1” = On, “0” = Off
D6	TELOM	Tearing effect line mode	“0” = mode1, “1” = mode2
D5	Reserved		‘0’
D4	Reserved		‘0’
D3	Reserved		‘0’
D2	Reserved		‘0’
D1	Reserved		‘0’
D0	ERR	Error on DSI	‘0’ = No Error ‘1’ = Error

6.2.8 RDDSDR (0F00h): Read Display Self-Diagnostic Result

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	0F00h	0	0	0	0	0	0	0	CMP_BIT	00

Description	The display module returns the self-diagnostic results following a Sleep Out command.

Bit	Symbol	Description	Comment
D0	CMP_BIT	self-diagnostic results of checksum comparison	‘0’

6.2.9 SLPIN (1000h): Sleep In

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	1000h	No Argument								

Description	This command causes the display module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped. The control Interface such as registers is still working and keeps its values.
Restriction	This command has no effect when the display module is already in Sleep mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). It must wait 5msec before sending next command for the supply voltages and clock circuits to stabilize. It must wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

6.2.10 SLPOUT (1100h): Sleep Out

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	1100h	No Argument								

Description	This command causes the display module to exit Sleep mode.
Restriction	This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize. The host processor must wait 60 milliseconds after sending a Sleep Out command before sending a Sleep-In command. The display module loads the display module's default values to the registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received.

6.2.11 PTLON (1200h): Partial Display Mode On

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	1200h	No Argument								

Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the Partial Area (30h) command. To leave Partial Display Mode, the Normal Display Mode On (13h) command should be written.
Restriction	This command has no effect when Partial Display Mode is already active.

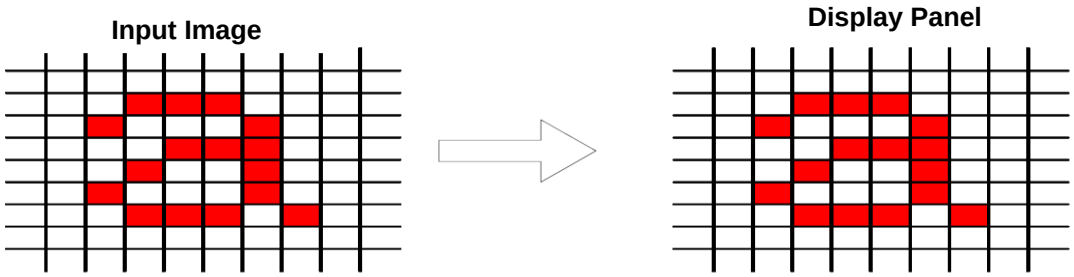
6.2.12 NORON (1300h): Normal Display Mode On

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	1300h	No Argument								

Description	This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial Display mode.
Restriction	This command has no effect when Normal Display mode is already active.

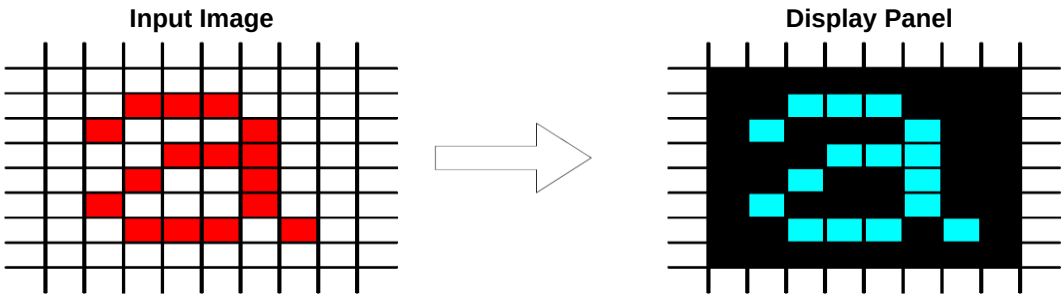
6.2.13INVOFF (2000H): Display Inversion Off

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	2000h	No Argument								

Description	This command causes the display module to stop inverting the image data on the display device. No status bits are changed. 
Restriction	This command has no effect when the display module is not inverting the display image.

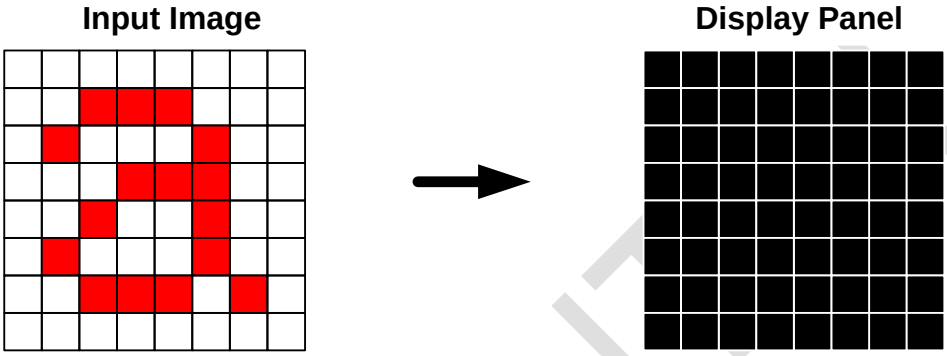
6.2.14INVON (2100H): Display Inversion On

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	2100h	No Argument								

Description	This command causes the display module to invert the image data only on the display device. No status bits are changed. 
Restriction	This command has no effect when module is already in inversion on mode.

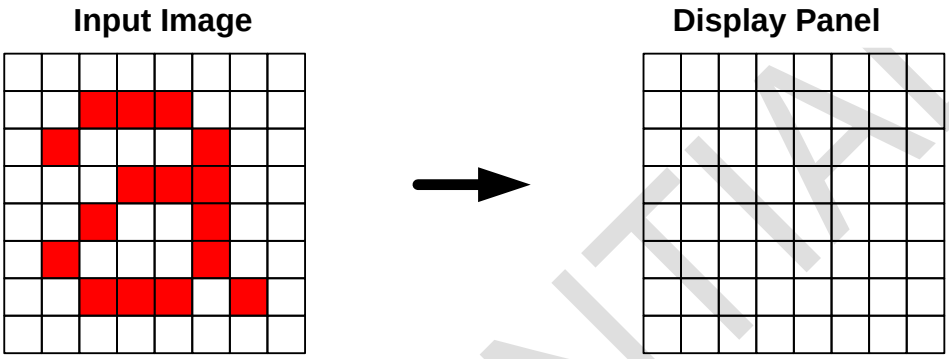
6.2.15 ALLPOFF (2200H): All Pixel Off

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	2200h	No Argument								

Description	This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status.  “All Pixels On”, “Normal Display Mode On” or “Partial Mode On” commands are used to leave this mode. The display panel is showing the content of the Input Image after “Normal Display On” and “Partial Mode On” commands.
Restriction	-

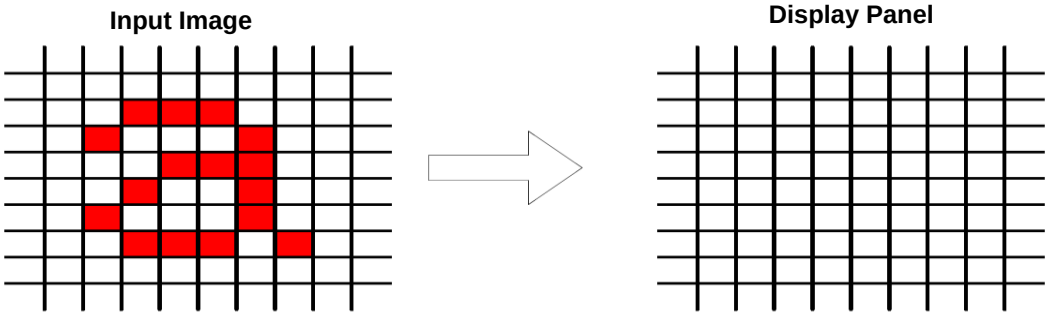
6.2.16 ALLPON (2300H): All Pixel On

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	2300h	No Argument								

Description	This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status.  “All Pixels Off”, “Normal Display Mode On” or “Partial Mode On” commands are used to leave this mode. The display panel is showing the content of the Input Image after “Normal Display On” and “Partial Mode On” commands.
Restriction	-

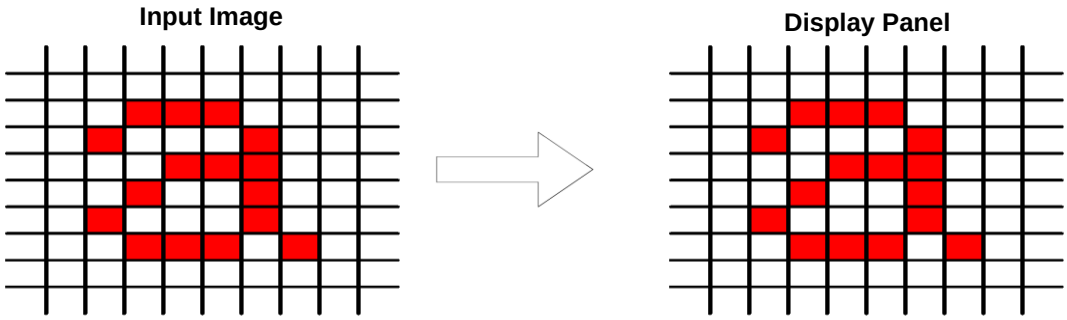
6.2.17 DISPOFF (2800h): Display Off

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	2800h	No Argument								

Description	This command causes the display module to stop displaying the image data on the display device. No status bits are changed. 
Restriction	This command has no effect when module is already in display off mode.

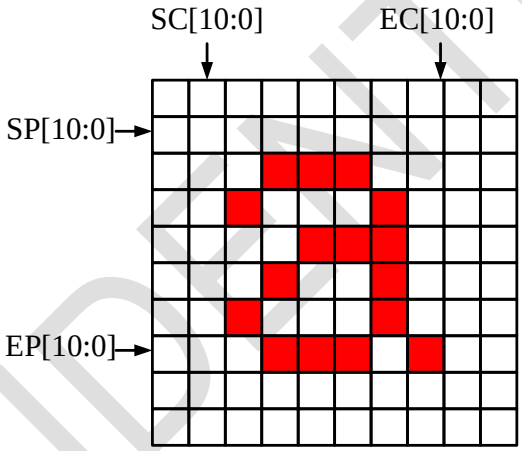
6.2.18 DISPON (2900h): Display On

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	2900h	No Argument								

Description	This command causes the display module to start displaying the image data on the display device. No status bits are changed. 
Restriction	This command has no effect when module is already in display on mode.

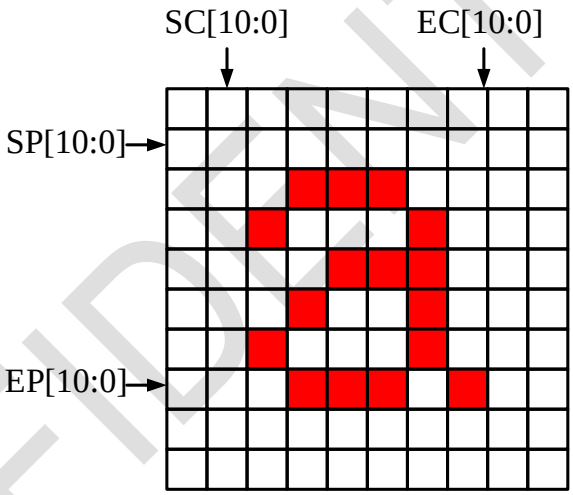
6.2.19CASET(2A00h~2A03h) : Set Column Start Address

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	2A00h	-	-	-	-	-	SC10	SC9	SC8	00
	2A01h	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
	2A02h	-	-	-	-	-	EC10	EC9	EC8	01
	2A03h	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	DF

Description	This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands. This command makes no change on the other driver status. The values of SC[10:0] and EC[10:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory. 
Restriction	(1) SC[10:0] always must be equal to or less than EC[10:0]. (2) The SC[10:0] and EC[10:0]-SC[10:0]+1 must can be divisible by 4. (3) In VESA DSC mode, SC[10:0]/EC[10:0] shall configure to match the slice boundary

6.2.20 RASET(2B00h~2B03h) : Set Row Start Address

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	2B00h	-	-	-	-	-	SP10	SP9	SP8	00
	2B01h	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00
	2B02h	-	-	-	-	-	EP10	EP9	EP8	01
	2B03h	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	DF

Description	This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. This command makes no change on theother driver status. The values of SP[10:0] and EP[10:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory. 
Restriction	(1) SP[10:0] always must be equal to or less than EP[10:0]. (2) The SP[10:0] and EP[10:0]-SP[10:0]+1 must can be divisible by 2. (3) In VESA DSC mode, SP[10:0]/EP[10:0] shall configure to match the slice boundary

6.2.21 RAMWR (2C00h): Memory Write

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	2C00h	0	0	1	0	1	1	0	0	2C
	1st Pixel	$D_1$7	$D_1$6	$D_1$5	$D_1$4	$D_1$3	$D_1$2	$D_1$1	$D_1$0	
	:	:	:	:	:	:	:	:	:	
	Nth Pixel	D_N7	D_N6	D_N5	D_N4	D_N3	D_N2	D_N1	D_N0	

Description	This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands.
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.

6.2.22HFR_CTL (2F00h): HFR Control

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	2F00h	0	0	0	0	HP_mode	HFR_mode	HFR_mode_sel[1:0]		00

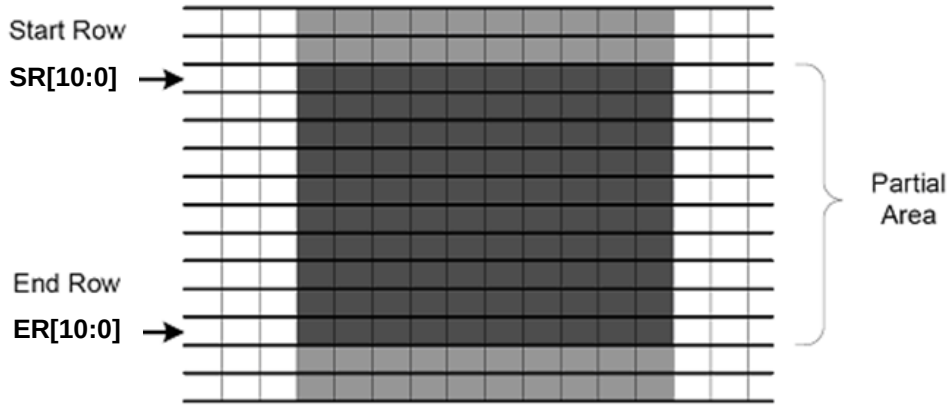
Description	

Parameter	Description
HP_mode	1: High perfomane mode Display 0: normal display mode
HFR_mode	1: High Frame rate mode Display 0: normal display mode
HFR_mode_sel[1:0]	Setting 0~2 for 3 different frame rate

Restriction	-

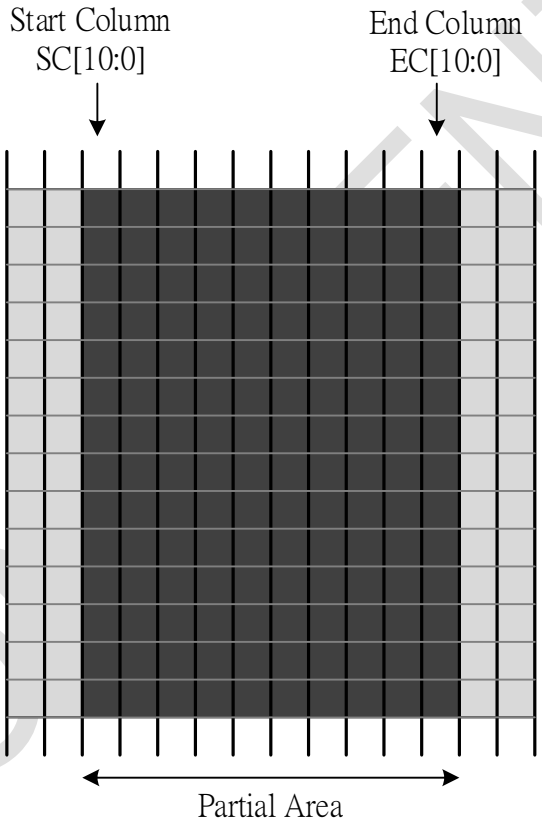
6.2.23PTLAR (3000h): Partial Area

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	3000h	-	-	-	-	-	SR10	SR9	SR8	00
	3001h	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
	3002h	-	-	-	-	-	ER10	ER9	ER8	01
	3003h	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	DF

Description	This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. If End Row > Start Row 
Restriction	SR[10:0] and ER[10:0] settings should be within max available Display Area.

6.2.24PTLAR (3100h): Vertical Partial Area

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	3100h	-	-	-	-	-	SC10	SC9	SC8	00
	3101h	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
	3102h	-	-	-	-	-	EC10	EC9	EC8	01
	3103h	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	DF

Description	This command defines the Vertical Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Column (SC) and the second the End Column (EC), as illustrated in the following figure. If End Column > Start Column 
Restriction	SC[10:0] and EC[10:0] settings should be within max available Display Area.

6.2.25TEOFF (3400h): Tearing Effect Line OFF

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	3400h	No Argument								

Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.
Restriction	This command has no effect when the Tearing Effect output is already off.

6.2.26 TEON (3500h): Tearing Effect Line ON

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	3500h	0	0	0	0	0	0	0	TELOM	00

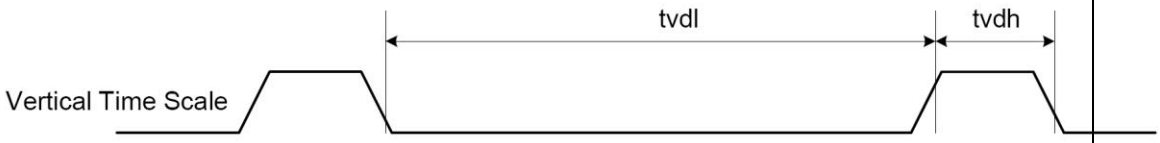
Description

Bit	Symbol	Description	Comment
D0	TELOM	Output mode of TE signal	0:only V-blanking 1:V-blanking +H-blanking

This command turns on the tearing Effect output signal on the TE signal line.
The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.

If TELOM = 0:

The Tearing Effect Output line consists of V-Blanking information only.



If TELOM = 1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

This command has no effect when Tearing Effect output is already ON.

6.2.27IDMOFF (3800h): Idle Mode Off

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	3800h	No Argument								

Description	This command causes the display module to exit Idle mode.
Restriction	This command has no effect when the display module is not in Idle mode.

6.2.28IDMON (3900h): Enter_idle_mode

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	3900h	No Argument								

Description	This command causes the display module to enter Idle Mode.
Restriction	This command has no effect when module is already in idle on mode.

6.2.29 COLMOD (3A00h): Interface Pixel Format

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	3A00h	SPI_IFPF_SEL	VIPF[2]	VIPF[1]	VIPF[0]	0	IFPF[2]	IFPF[1]	IFPF[0]	77

Description

This command sets the pixel format for the RGB image data used by the interface.
If SPI_IFPF_SEL(3Ah-D7) = 1:
The SPI/QSPI interface will use VIPF[2:0] as pixel format setting individually, and the other interface will use IFPF[2:0].
If SPI_IFPF_SEL(3Ah-D7) = 0:
All interface use IFPF[2:0] as pixel format setting

Control Interface Color Format	IFPF[2]	IFPF[1]	IFPF[0]
SPI 8 bit/pixel (256 colors); SPI 3-3-2 (Support IF: SPI3/SPI4)	0	1	0
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,144 colors)	1	1	0
24bit/pixel (16.7M colors)	1	1	1

Restriction

VESA DSC mode only support IFPF = 7.

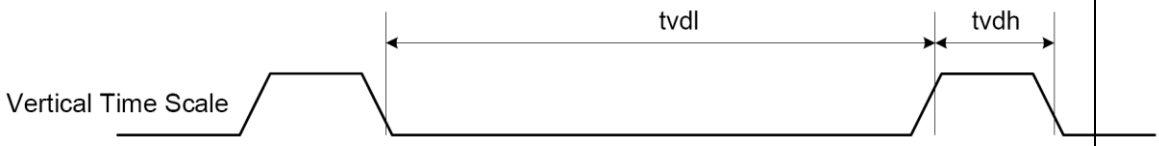
6.2.30 RAMWRC (3C00h): Memory Continuous Write

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	3C00h	0	0	1	1	1	1	0	0	3C
	1st Pixel	$D_1$7	$D_1$6	$D_1$5	$D_1$4	$D_1$3	$D_1$2	$D_1$1	$D_1$0	
	:	:	:	:	:	:	:	:	:	
	Nth Pixel	D_N7	D_N6	D_N5	D_N4	D_N3	D_N2	D_N1	D_N0	

Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.

6.2.31 STESL(4400h) : Set_Tear_Scanline

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	4400h	STS[15]	STS[14]	STS[13]	STS[12]	STS[11]	STS[10]	STS[9]	STS[8]	00
	4401h	STS[7]	STS[6]	STS[5]	STS[4]	STS[3]	STS[2]	STS[1]	STS[0]	00

Description	This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line STS[15:0]. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. 
Restriction	The Tearing Effect Output line is active low when the display module is in Sleep mode.

6.2.32DSTBON (4F00h): Deep Standby Mode On

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	4F00h	0	0	0	0	0	0	0	DSTB	00

Description	This command is used to enter deep standby mode. DSTB=”1”, enter deep standby mode.
Restriction	Notes: 1. To exit Deep Standby Mode, input low pulse more than 3ms to pin RESX. 2. For MIPI IF, if deep standby mode is used, please pull HSSI_CLK_P/N & HSSI_D0~D3_P/N to GND after executing deep standby command. 3. Please unlock DSTB key to 0x5AA5 value before use this command. 4. After entering into DSTB mode, all the MIPI signals must stay at ULPS mode (LP-00) to prevent from extra current from MIPI pins to MVDDA (=0V at DSTB mode) thru internal ESD diode.

6.2.33WRDISBV (5100h): Write Display Brightness

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	5100h	DBV[7:0]								00
W	5101h	DBV[15:8]								00

Description	This command is used to adjust brightness value. In 8-bit mode: Brightness value is 5100[7:0] (range is 0x00 ~ 0xFF) In 10-bit mode: Brightness value is {5100[1:0], 5101[7:0]} (0x000 ~ 0x3FF) In 12-bit mode: Brightness value is {5100[3:0], 5101[7:0]} (0x000 ~ 0xFFF)
Restriction	The display supplier cannot use this command for tuning

6.2.34WRCTRLD (5300h): Write Display Control

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	5300h	0	0	1	0	BC_DIM EN	0	0	0	28

Description	BC_DIM_EN: Display dimming control ,1=enable
Restriction	The display supplier cannot use this command for tuning

6.2.35RDCTRLD (5400h): Read Display Control

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	5400h	0	0	1	0	BC_DIMEN	0	0	0	28

Description	BC_DIM_EN: Display dimming control ,1=enable
Restriction	-

6.2.36WRRADACL (5500h): RAD_ACL Control

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	5500h	0	0	0	0	0	0	RAD_ACL[1:0]		00

Description	This command is used to control Raydium specific function for ACL (Auto Current Limit) RAD_ACL[1:0]=11, Enable Raydium ACL function. RAD_ACL[1:0]=00, Disable Raydium ACL function.
Restriction	-

6.2.37 LTPO_CTL (8A00h): LTPO Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WR	8A00h	0	0	0	mc_en	mc_ucs[3:0]				00h

Description

Parameter	Description
mc_en	1: mode control enable 0: mode control disable
mc_ucs[3:0]	Mode control index

mc_ucs[3:0]	
0	Mode Control Setting 1
1	Mode Control Setting 2
…	…
14	Mode Control Setting 15
15	Mode Control Setting 16

Restriction

-

6.2.38 RDDDBS(A100h) : Read_DDB_Start

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	A100h	SID[7]	SID [6]	SID [5]	SID [4]	SID [3]	SID [2]	SID [1]	SID [0]	00
	A101h	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	00
	A102h	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	00
	A103h	MID[15]	MID[14]	MID[13]	MID[12]	MID[11]	MID[10]	MID[9]	MID[8]	00
	A104h	RID[7]	RID[6]	RID[5]	RID[4]	RID[3]	RID[2]	RID[1]	RID[0]	00
	A105h	RID[15]	RID[14]	RID[13]	RID[12]	RID[11]	RID[10]	RID[9]	RID[8]	00
	A106h	1	1	1	1	1	1	1	1	FF

Description	1st parameter: Supplier ID code 2nd parameter: Supplier ID code 3rd parameter: Module ID 4th parameter: Module ID 5th parameter: Module revision information 6th parameter: Module revision information 7th Exit code (FFh).
Restriction	

6.2.39 RDDDBC(A800h) : Read DDB Continuous

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	A800h	SID[7]	SID [6]	SID [5]	SID [4]	SID [3]	SID [2]	SID [1]	SID [0]	00
	A801h	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	00
	A802h	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	00
	A803h	MID[15]	MID[14]	MID[13]	MID[12]	MID[11]	MID[10]	MID[9]	MID[8]	00
	A804h	RID[7]	RID[6]	RID[5]	RID[4]	RID[3]	RID[2]	RID[1]	RID[0]	00
	A805h	RID[15]	RID[14]	RID[13]	RID[12]	RID[11]	RID[10]	RID[9]	RID[8]	00
	A806h	1	1	1	1	1	1	1	1	FF

Description	RDDDBS/RDDDBC command returns the supplier identification and display module mode/revision information. *Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block.* *Note: For use example,* *1. Set maximum return packet size=3* *2. Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0]* *3. Read* 0xA8*, return 3 bytes MID[15:8], RID[7:0], RID[15:8]*
Restriction	A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue command is undefined.

6.2.40 RDFCS(AA00h)：Read First Checksum

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	AA00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	00

Description	This command returns the first checksum what has been calculated from “User Command Set” area registers (not include “Manufacture Command Set) and the frame memory after the write access to those registers and/or frame memory has been done.
Restriction	It will be necessary to wait 150ms after there is the last write access on “User Command Set” area registers before there can read this checksum value.

6.2.41 RDCCS(AF00h) : Read Continue Checksum

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	AF00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00

Description	This command returns the continue checksum what has been calculated continuously after the first checksum has been calculated from “User Command Set” area registers and the frame memory after the write access to those registers and/or frame memory has been done.
Restriction	It will be necessary to wait 300ms after there is the last write access on “User Command Set” area registers before there can read this checksum value in the first time.

6.2.42 Set_SPI Mode (C400h) : Set_SPI Mode

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	C400h	SPI_WRAM	0	DSPI_CFG 1	DSPI_CFG 0	0	0	0	DSPI_EN	00

Description

Bit	Description	Value
DSPI_EN	DAUL SPI MODE Enable	0: disable 1: enable
DSPI_CFG[1:0]	DAUL SPI MODE Selection	00: 1P1T for 1 wire 10: 1P1T for 2 wire 11: 2P3T for 2 wire 01: reserved
SPI_WRAM	This command is used in SPI/SPINK interfaces. Making sure to set SPI_WRAM=1 before host writes SRAM via SPI/SPINK interfaces.	0: disable 1: SPI interface write RAM enable

Restriction

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When RM69A10 is used out of the absolute maximum ratings, the RM69A10 may be permanently damaged. To use the RM69A10 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the RM69A10 will malfunction and cause poor reliability.

item	Symbol	Value	Unit
Power supply voltage	VDDI	-0.3 ~ + 3.6	V
Power supply voltage	VDD (VDDA, VDDB, VDDR)	-0.3 ~ + 5.5	V
Supply voltage (MV)	AVDD- AVSS	-0.3 ~ + 8.8	V
	AVSS- AVEE	-0.3 ~ + 8.8	V
Supply voltage (HV)	VGH- VGL	-0.3 ~ + 32	V
MIPI Differential Input	HSSI_CLK_P/ HSSI_CLK_N HSSI_D0_P/ HSSI_D0_N HSSI_D1_P/ HSSI_D1_N HSSI_D2_P/ HSSI_D2_N	-0.3 ~ 1.35	V
Input voltage	VIN	-0.3 ~ VDDI+ 0.3	V
Output voltage	VO	-0.3 ~ VDDI+ 0.3	V
Operating temperature	Topr	-40 ~ + 85	°C
Storage temperature	Tstg	-55 ~ + 125	°C
Notes: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation. Therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.			

7.2 ESD Protection Level

Model	Test Condition	Level
Human Body Mode	R = 1.5 kohm / C = 100 pF	Pass 3KV
Machine Mode	R = 0 ohm / C = 200 pF	Pass 300V

7.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than ±200 mA.

7.4 DC Characteristics

Basic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Related Pins
Analog Power Supply Voltage	VDD	Operation Voltage	2.7	2.8	3.6	V	Note 1
I/O pin Power Supply Voltage	VDDI	I/O supply voltage	1.65	1.8	1.95	V	Note 1,2
Logic High level input voltage	VIH	VDDI = 1.65V ~ 1.95V	0.8* VDDI	-	VDDI	V	Note 3
Logic Low level input voltage	VIL	VDDI = 1.65V ~ 1.95V	0.0	-	0.2* VDDI	V	Note 3
Logic High level Output voltage	VOH	Iout = -1 mA	0.8* VDDI	-	VDDI	V	Note 3
Logic Low level Output voltage	VOL	Iout = +1 mA	0.0	-	0.2* VDDI	V	Note 3
Logic High level input current (Except MIPI)	IIHD	Vin=0~VDDI			1	uA	Note 3
Logic Low level input current (Except MIPI)	IILD	Vin=0~VDDI	-1			uA	Note 3
Logic High level input current (MIPI)	IIHD	Vin=0~VDDI			1	uA	Note 3
Logic Low level input current (MIPI)	IILD	Vin=0~VDDI	-1			uA	Note 3
AVDD booster voltage	AVDD		5.0		8.0	V	Note 3
AVEE booster voltage	AVEE		-8		-2.8	V	Note 3
VGH booster voltage	VGH		AVDD		2xAVDD	V	Note 3
VGL booster voltage	VGL		AVEE+VCL -VCI		AVEE,	V	Note 3
Voltage difference between VGH and VGL	VGHL	|VGH-VGL|			30	V	Note 3
Gamma reference voltage	VGMP		2.0		7.7	V	Note 3,4
Gamma reference voltage	VGSP		0.0		4.5	V	Note 3
OSC	Fosc		69.92	76	82.08	MHz	
Channel deviation voltage	VDEV	Sout ≥ AVDD-1.0V, and 0V < Sout ≤ 1.0V				mV	TBD
Channel deviation voltage	VDEV	1.0V < Sout < AVDD-1.0V				mV	TBD

Notes:

1. VDD means VDDA, VDDR, VDDB. And VSS means VSSA, VSSR, VSSB, AVSS, VSSAM. VDDB, VDDA and VDDR should be the same input voltage level and larger than VDDI voltage.
2. Recommend VDDI=1.8V for power saving.
3. Ta(ambient temperature) ranges from -30℃ to 85 ℃.
4. VGMP <= AVDD – 0.2V

7.5 Operation Current

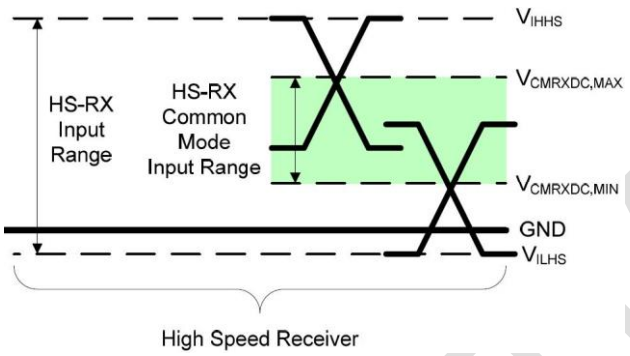
VCI=2.8V and VDDI=1.8V

Parameter	Symbol	Condition	Max.	Unit
Sleep In Mode	I_SLP_VCI	VDDI=VCC=1.8V VCI=VDDA=VDDB=VDDR=2.8V HSSI_D0P/N=HSSI_D1P/N=HSSI_CKP/N=LP-11 Ta = 25deg	TBD	uA
	I_SLP_VDDI		TBD	uA
Deep Standby Mode	I_DSTB_VCI	VDDI=VCC=1.8V VCI=VDDA=VDDB=VDDR=2.8V HSSI_D0P/N=HSSI_D1P/N=HSSI_CKP/N=0 Ta = 25deg	TBD	uA
	I_DSTB_VDDI		TBD	uA

7.6 MIPI Characteristics

7.6.1 High-Speed Receiver Specification

DC Specifications

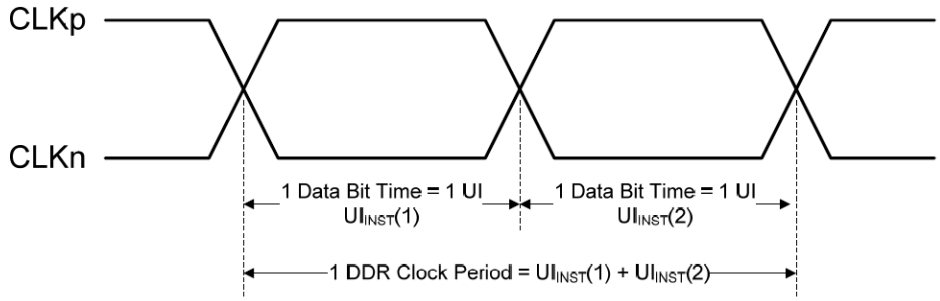


Parameter	Description	Min	Nom	Max	Units	Note
VCMRX(DC)	Common-mode voltage HS receive mode	70		330	mV	1,2
VIDTH	Differential input high threshold			70	mV	
VIDTL	Differential input low threshold	-70			mV	
VIHHS	Single-ended input high voltage			460	mV	1
VILHS	Single-ended input low voltage	-40			mV	1
ZID	Differential input impedance	80	100	125	Ω	

Notes:
1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

7.6.2 Forward high speed transmissions

DDR Clock Definition



Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	1		12.5	ns	1,2

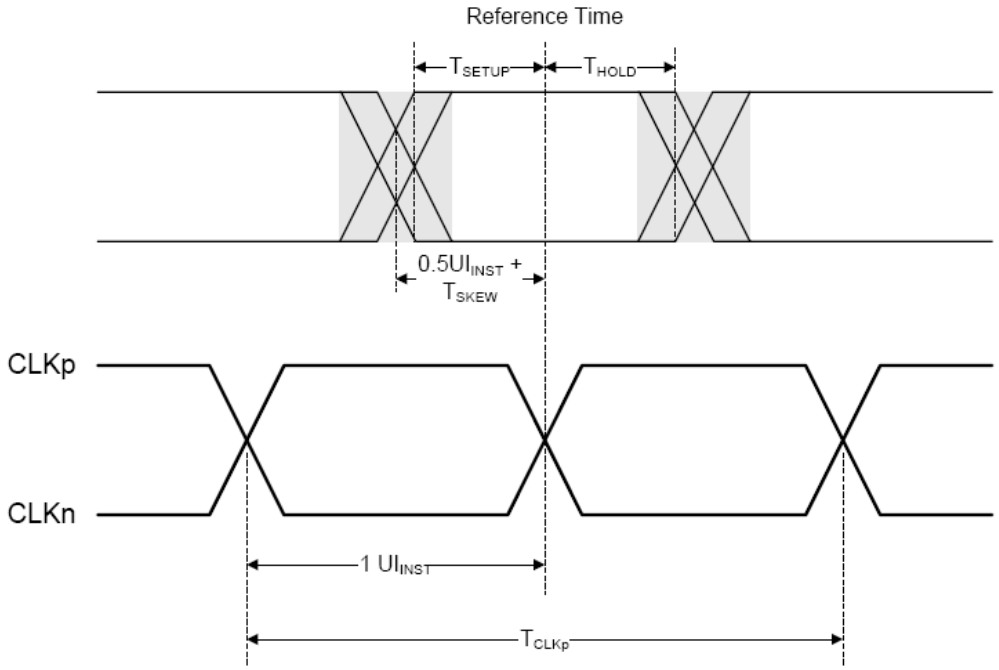
Notes:
1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Data-Clock Timing Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data to Clock Skew [measured at transmitter]	$T_{SKEW[TX]}$	-0.15		0.15	UI_{INST}	1
Data to Clock Setup Time [receiver]	$T_{SETUP[RX]}$	0.15			UI_{INST}	2
Clock to Data Hold Time [receiver]	$T_{HOLD[RX]}$	0.15			UI_{INST}	2

Notes:
1. Total silicon and package delay budget of 0.3*UI_{INST}
2. Total setup and hold window for receiver of 0.3*UIINST

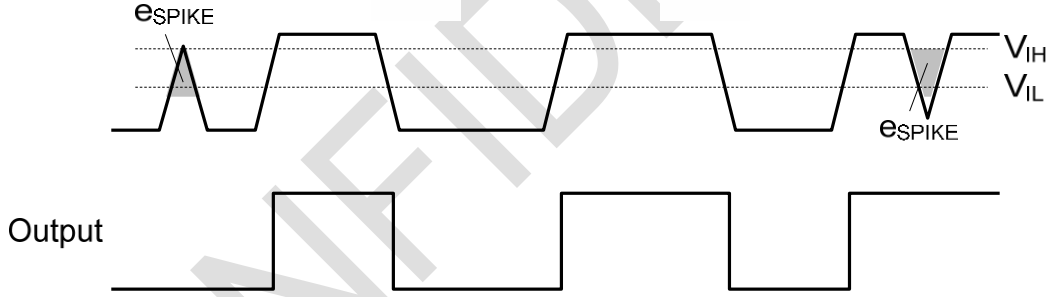
7.6.3 Data to Clock Timing Definitions



7.6.4 Low power transceiver specifications

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Logic high level input voltage	VIHCD	Contention Detection (Lane_D0)	450		1350	mV
Logic low level input voltage	VILCD	Contention Detection (Lane_D0)	0		200	mV
Logic high level input voltage	VIH-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1)	880	-	1350	mV
Logic low level input voltage	VIL-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1	0		550	mV
Logic low level input voltage	VIL-ULPS	LP-Rx ULPS (Lane_CK, Lane_D0, Lane_D1)	0		300	mV
Logic high level input voltage	VOH-LPTX	Contention Detection (Lane_D0)	1.1	1.2	1.3	V
Logic low level input voltage	VOL-LPTX	Contention Detection (Lane_D0)	-50	0	50	mV
eSPIKE(1.2.3)	Fig. 2	Input pulse rejection			300	V.ps

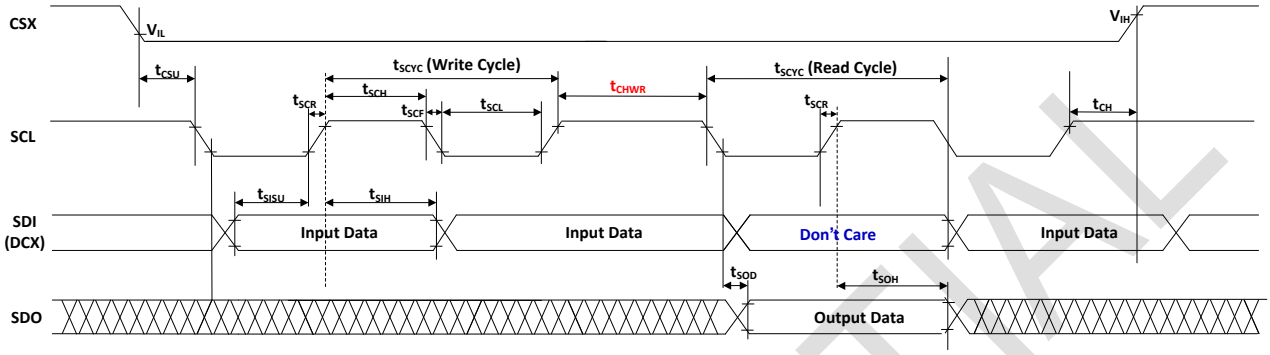
Notes:
Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 State.
An impulse less than this will not change the receiver state.
In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
Input Glitch Rejection of Low Power Receivers as follow.



7.7 AC Characteristics

7.7.1 SPI/DUAL-SPI Characteristics

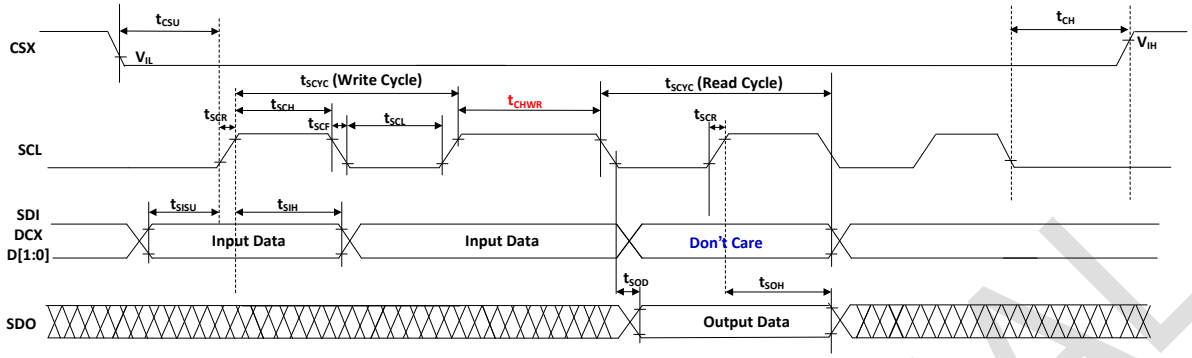
3/4-wire SPI



Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock cycle	t_{SCYC}	Write	TBD			ns
		Read				ns
Clock high pulse width	t_{SCH}	Write				ns
	t_{SCH}	Read				ns
Clock low pulse width	t_{SCL}	Write				ns
	t_{SCL}	Read				ns
Clock rise time	t_{SCR}	0.2*VDDI -> 0.8*VDDI				ns
Clock fall time	t_{SCF}	0.8*VDDI -> 0.2*VDDI				ns
Chip select setup time	t_{CSU}					ns
Chip select hold time	t_{CH}					ns
Data input setup time	t_{SISU}	To V_{IL} of SCL's rising edge				ns
Data input hold time	t_{SIH}					ns
Access time of output data	t_{SOD}	From V_{IL} of SCL's falling edge				ns
Hold time of output data	t_{SOH}	From V_{IH} of SCL's rising edge				ns
Transition time from Write cycle to Read cycle	t_{CHWR}	From V_{IH} of SCL's rising edge				ns

Notes:
(1) Logic high and low levels are specified as 80% and 20% of VDDI for Input signals.
(2) For the 4-wire SPI, the DCX's timing is the same as input data.
(3) Ta = -30°C to 70°C, VDDI=1.65V to 1.95V, VCI=2.7V to 3.6V, and VSS=0V

7.7.2 QUAD-SPI Characteristics



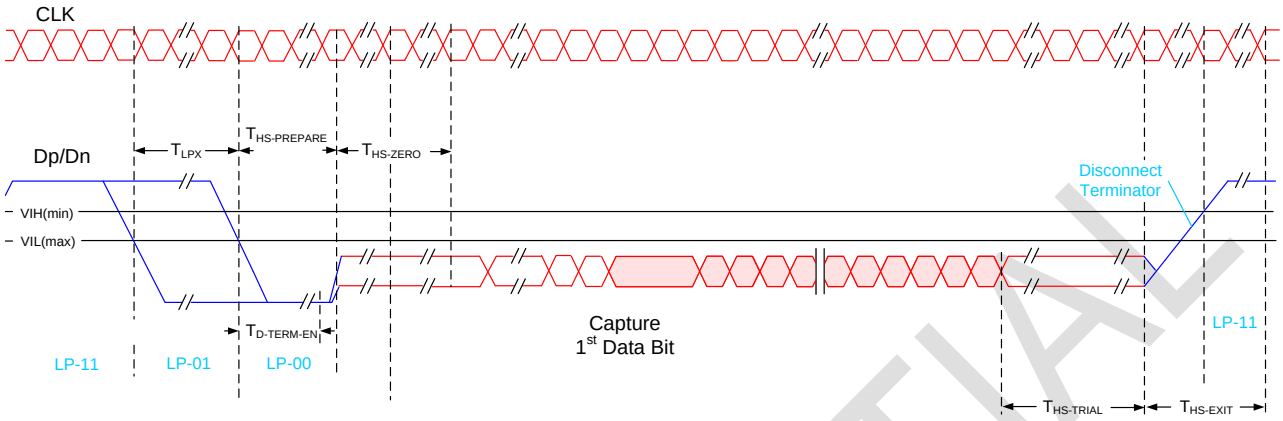
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock cycle	t_{SCYC}	Write	TBD			ns
		Read				ns
Clock high pulse width	t_{SCH}	Write				ns
	t_{SCH}	Read				ns
Clock low pulse width	t_{SCL}	Write				ns
	t_{SCL}	Read				ns
Clock rise time	t_{SCR}	0.2*VDDI -> 0.8*VDDI				ns
Clock fall time	t_{SCF}	0.8*VDDI -> 0.2*VDDI				ns
Chip select setup time	t_{CSU}					ns
Chip select hold time	t_{CH}					ns
Data input setup time	t_{SISU}	To V_{IL} of SCL's rising edge				ns
Data input hold time	t_{SIH}					ns
Access time of output data	t_{SOD}	From V_{IL} of SCL's falling edge				ns
Hold time of output data	t_{SOH}	From V_{IH} of SCL's rising edge				ns
Transition time from Write cycle to Read cycle	t_{CHWR}	From V_{IH} of SCL's rising edge				ns

Note: The max SCL frequency for each pixel data format is specified as the below table.
Note: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.
Note: Ta = -30 to 70 °C, VDDI=1.95V to 3.3V, VCI=2.7V to 3.6V, GND=0V
Note: 4-wire QSPI support transfer rate in pixel data write

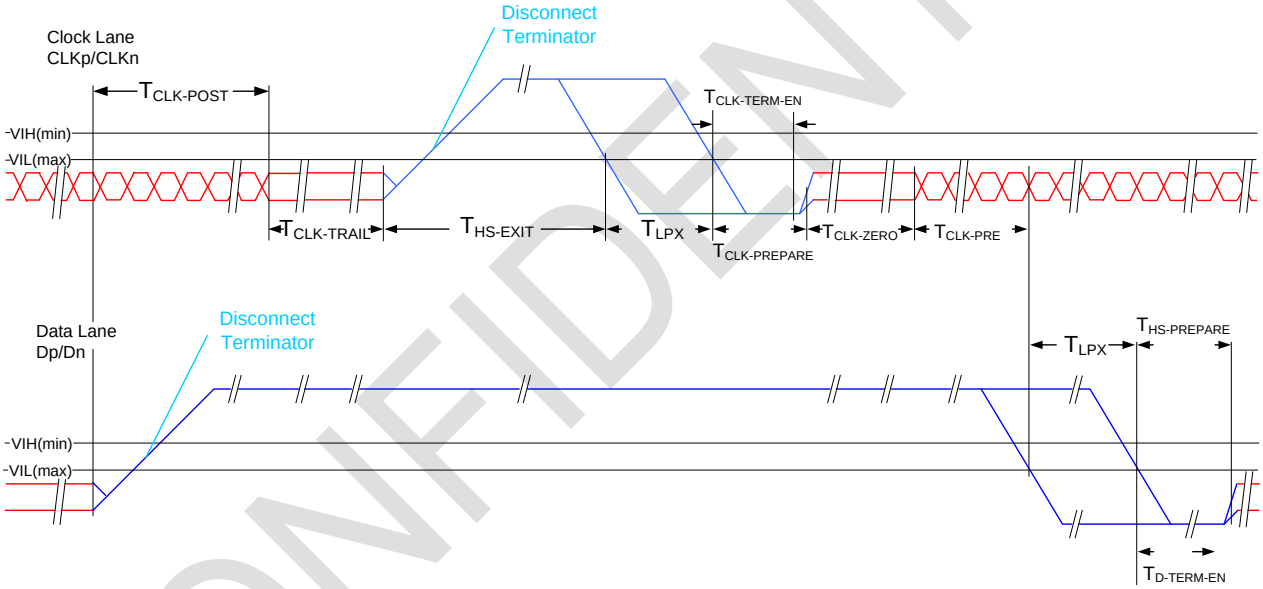
		4-wire QSPI suppor transfer rate
Pixel Data Write	RGB888	50MHz
	RGB666	50MHz
	RGB565	50MHz

7.7.3 DSI Timing Characteristics

HS Data Transmission Burst



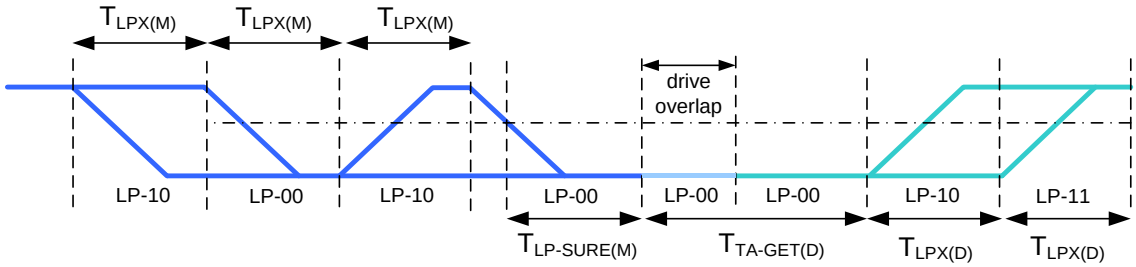
HS clock transmission



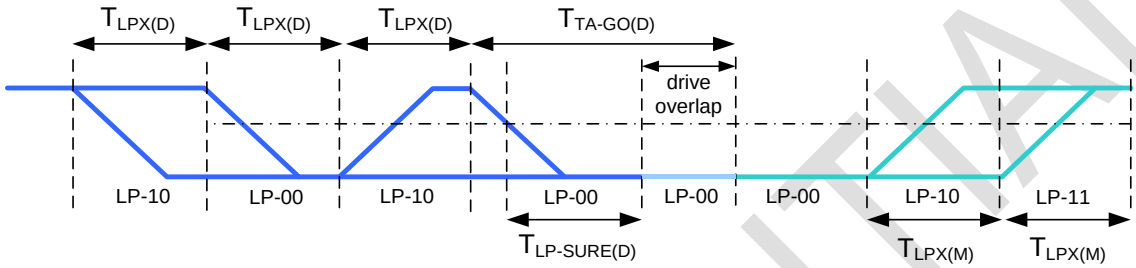
Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL .	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	Time for Dn to reach VTERM-EN		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	Time for Dn to reach VTERM-EN		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		100	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	165ns + 10*UI			**ns**
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max.(60+4*UI, 24*UI)			ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	100		145+10*UI	ns

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



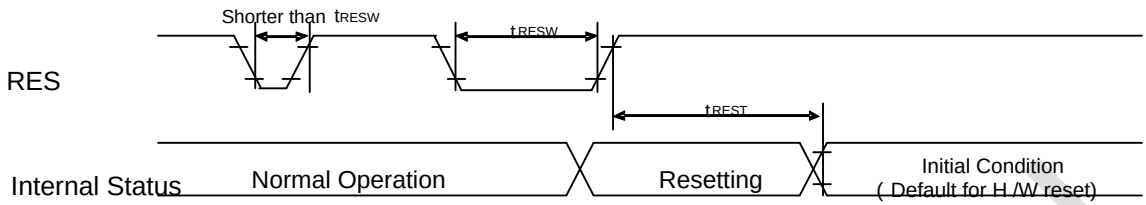
Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		**150**	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		**150**	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

NOTE:
1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

7.7.4 Reset Timing



Reset input timing:

VDDI=1.65 to 1.95V, VCI=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	30	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	20	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

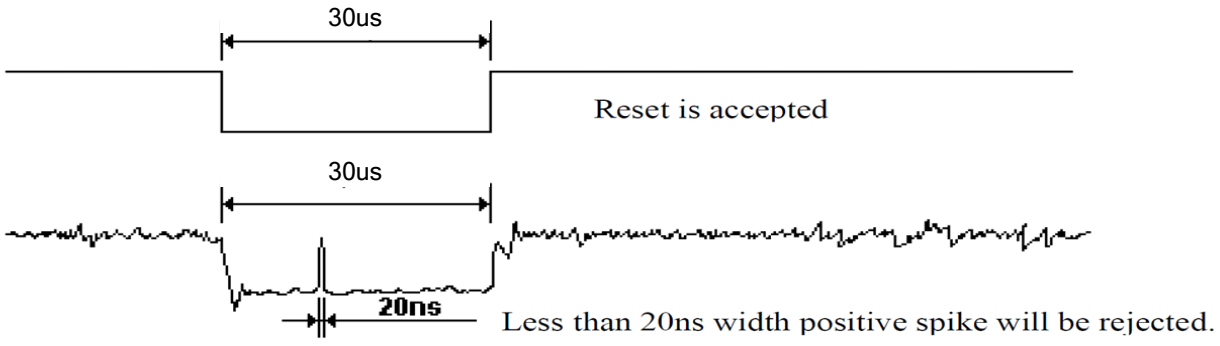
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 30μs	Reset
Between 5μs and 30μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 20ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

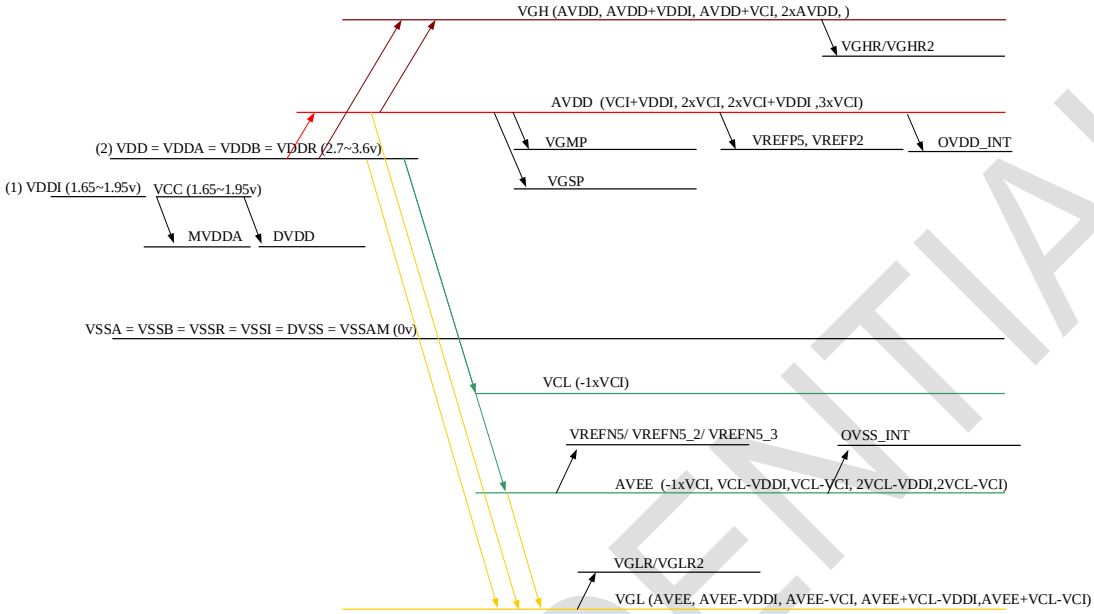


Note 5. It is necessary to wait 20msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 Power Generation

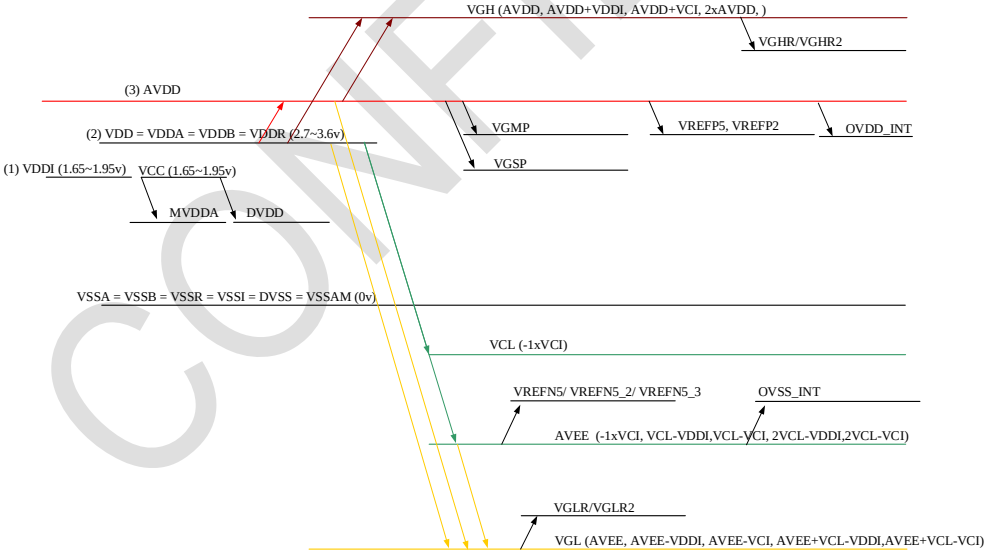
8.1 2-Power Mode (VDDI / VCI)

BSTM_EXTAVDD=0, Input Power= VDDI, VCI

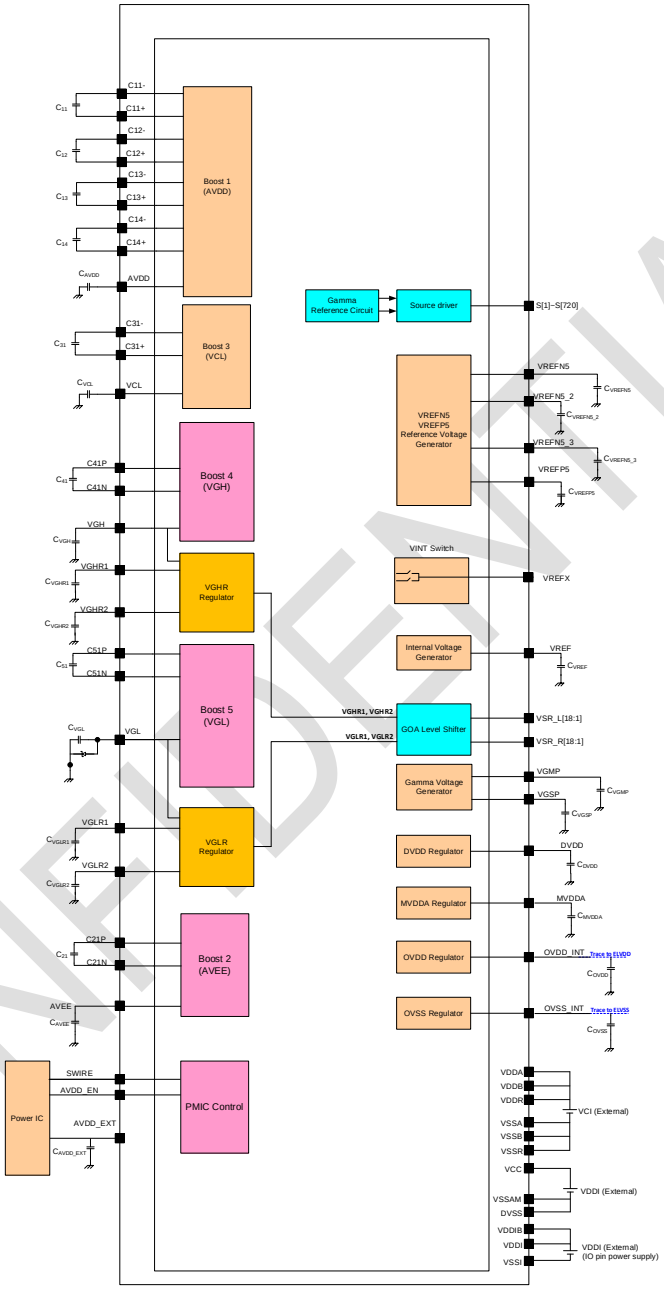


8.2 3-Power Mode (VDDI / VCI / AVDD)

BSTM_EXTAVDD=1, Input Power= VDDI, VCI, AVDD



8.2 DC/DC Converter Circuit



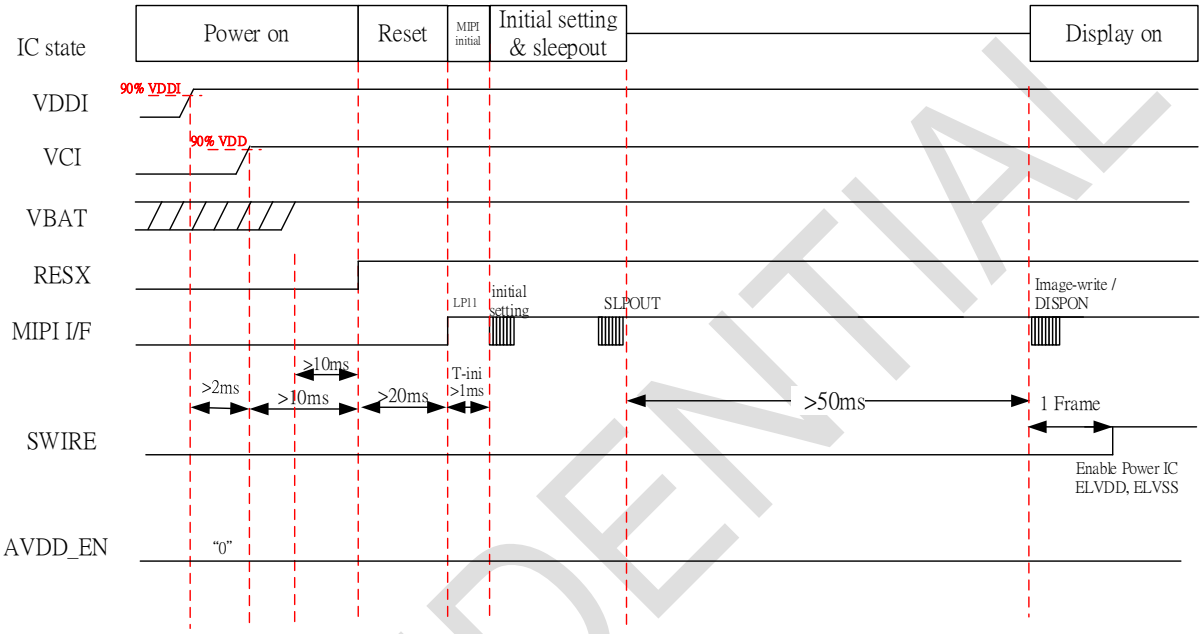
8.3 External Components

No.	Signal name	Values	Max ability
1	VDDA, VDDB, VDDR (VCI)	Cap , 2.2uF	6.3V
2	VDDI, VDDIB, VCC (VDDIO)	Cap , 2.2uF	6.3V
3	VREF	Cap , 22nF	6.3V
4	DVDD	Cap , 2.2uF	6.3V
5	MVDDA	Cap , 2.2uF	6.3V
6	VREFN5	Cap , 2.2uF	10V
7	VREFN5_2	Cap , 2.2uF	10V
8	VREFN5_3	Cap , 2.2uF	10V
9	VREFP5	Cap , 2.2uF	10V
10	VGMP	Cap , 1.0uF	10V
11	VGSP	Cap , 1.0uF	10V
12	VGHR	Cap , 2.2uF	25V
13	VGHR_2	Cap , 2.2uF	25V
14	VGLR	Cap , 2.2uF	25V
15	VGLR_2	Cap , 2.2uF	25V
16	OVDD_INT	Cap , 2.2uF	10V
17	OVSS_INT	Cap , 2.2uF	10V
18	C11P/C11N	Cap , 1.0uF	6.3V
19	C12P/C12N	Cap , 1.0uF	6.3V
20	C13P/C13N	Cap , 1.0uF	6.3V
21	C14P/C14N	Cap , 1.0uF	6.3V
22	AVDD	Cap , 2.2uF	16V
23	C21P/C21N	Cap , 1.0uF	16V
24	AVEE	Cap , 2.2uF	16V
25	C31P/C31N	Cap , 1.0uF	6.3V
26	VCL	Cap , 2.2uF	10V
27	C41P/C41N	Cap , 1.0uF	16V
28	VGH	Cap , 2.2uF	25V
29	C51P/C51N	Cap , 1.0uF	16V
30	VGL	Cap , 2.2uF	25V
31	VGL (VGL-GND)	Schottky Diode	V_F≤0.35V at I_F=10mA V_R>20V

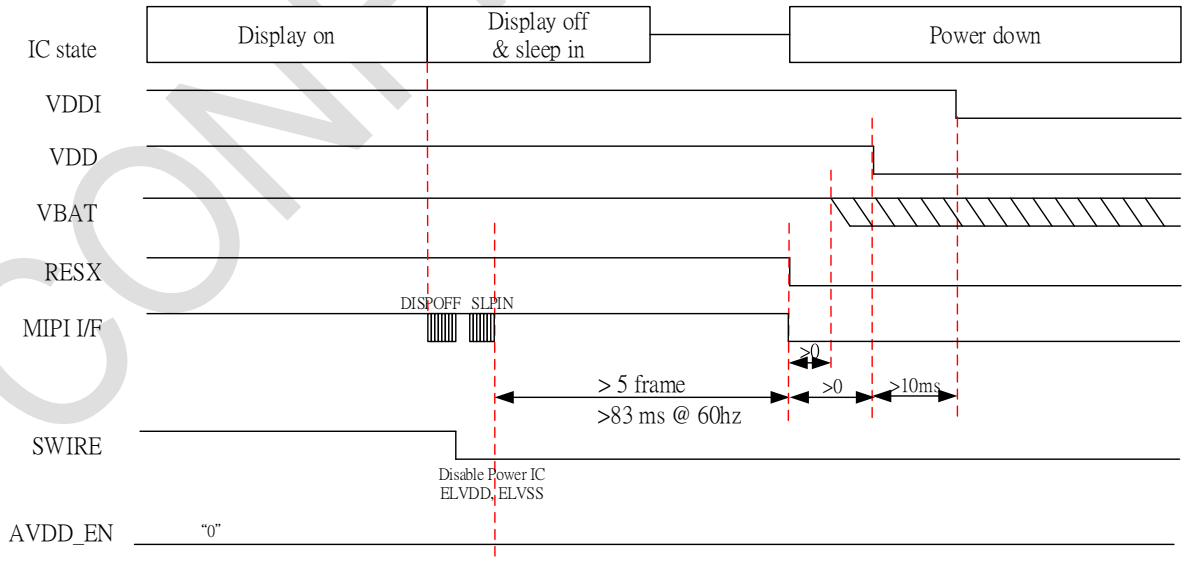
8.4 Power on/off sequence and timing

2-Power Mode (VDDI / VCI)
BSTM_EXTAVDD=0

Power On sequence

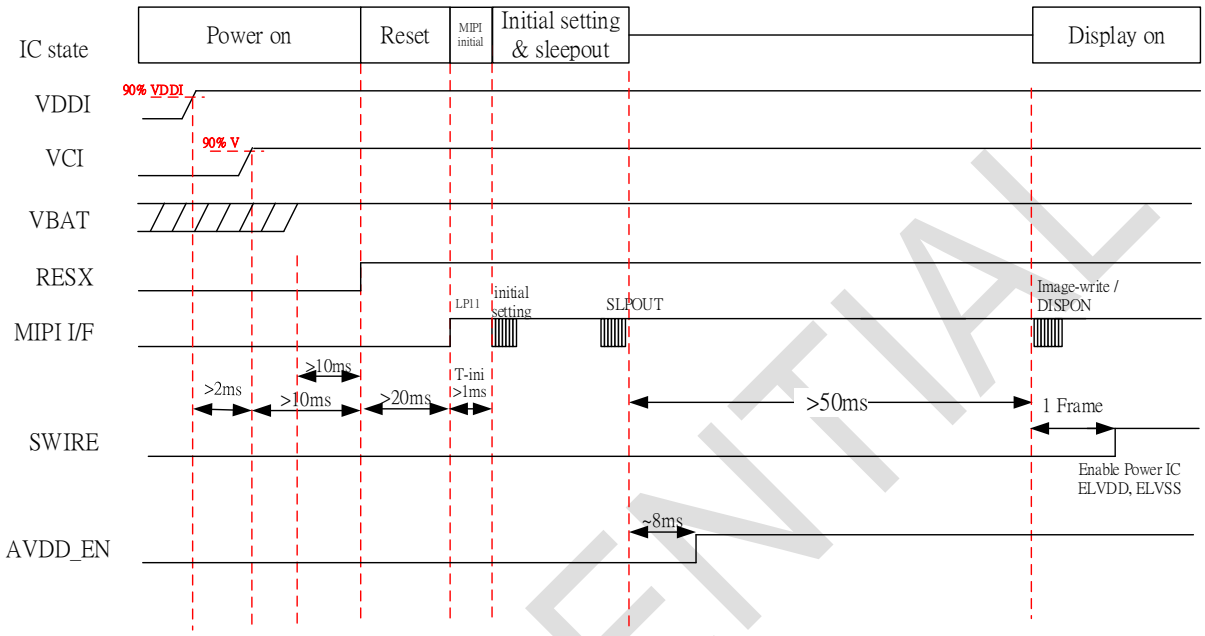


Power Off sequence

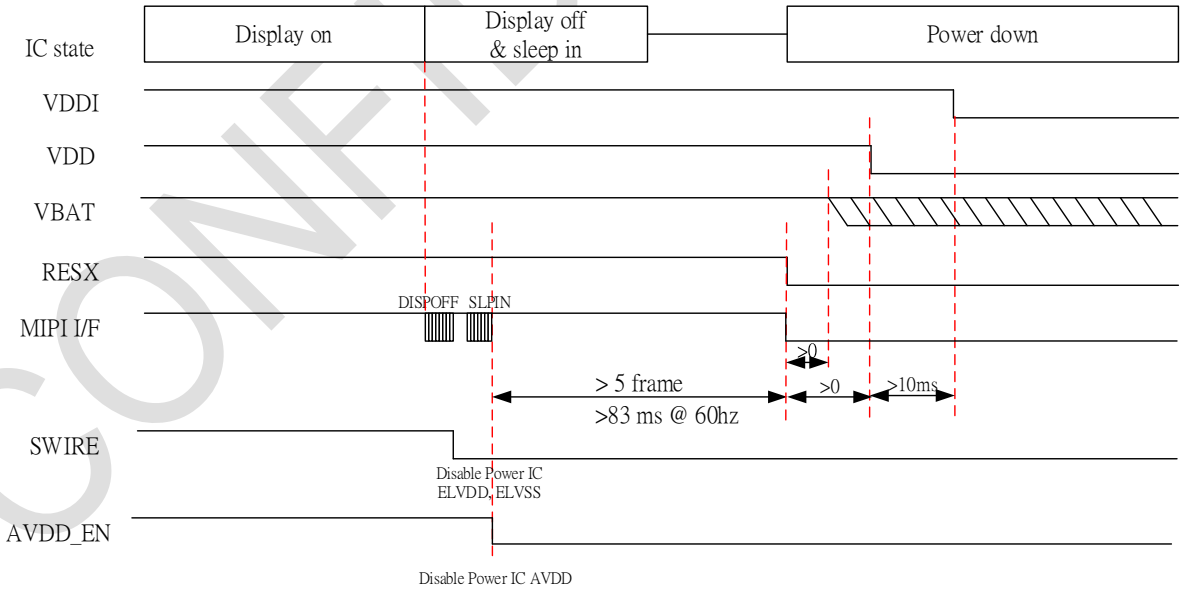


3-Power Mode (VDDI / VCI / AVDD_EXT)
BSTM_EXTAVDD=1

Power On sequence



Power Off sequence



8.5 Power Level Modes

Normal display mode on = NORON
Partial mode on = PTLON
Idle mode off = IDMOFF
Idle mode on = IDMON
Sleep out = SLPOUT
Sleep in = SLPIN
Deep standby mode = DSTBON

Definition example:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
In this mode, the display is able to show maximum 16.7M colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
In this mode, part of the display is used with maximum 16.7M colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
In this mode, the full display is used with 8 or 16.7M colors.
4. Partial Mode On, Idle Mode On, Sleep Out
In this mode, part of the display is used with 8 or 16.7M colors.
5. Sleep In Mode.
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random.
6. Deep Standby Mode.
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The interface and registers are not working. Contents of the frame memory are random.
7. Power Off Mode
In this mode, VDDI and VDDA/VDDR/VDDB are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.

8.6 Maximum Series Resistance

Pin Name	Type	Max Resistance	Unit
VDDA, VDDB, VDDR, VDDI, VDDIB, VCC	Power Supply	5	Ω
AVSS, VSSAM, DVSS, VSSI, VSSA, VSSR, VSSB	Power Supply	5	Ω
AVDD, AVDDD_EXT	Power Input/Output	5	Ω
DVDD	Power Input/Output	5	Ω
AVEE, VCL	Power Output	5	Ω
VGH, VGL	Power Output	5	Ω
C11P/N~C12P/N	Capacitor Connection	5	Ω
C21P/N~C22P/N	Capacitor Connection	5	Ω
C31P/N~C32P/N	Capacitor Connection	5	Ω
C41P/N	Capacitor Connection	5	Ω
C51P/N	Capacitor Connection	5	Ω
VGHR, VGHR_2, VGLR, VGLR_2	Power Output	5	Ω
OVDD_INT/OVSS_INT	Power Output	5	Ω
VGMP/VGSP/VREF	Power Output	5	Ω
MVDDA	Power Output	5	Ω
VREFP5/VREFN5/VREFN5_2/VREFN5_3/VREFX	Power Output	5	Ω
HSSI_CLK_P/N, HSSI_D0_P/N HSSI_D1_P/N, HSSI_D2_P/N	MIPI Interface I/O	5	Ω
TE, TE1, TE2, SWIRE, AVDD_EN, ERR	Digital Output I/O	20	Ω
RESX,WATCH_OSC_IN	Digital I/O	20	Ω
CSX, D/CX, SCL, SDI_RDX, SDO, D[0]~D[7] FLASH_CS/FLASH_SCLK/ FLASH_IO0~3	Interface I/O	5	Ω
IM[1 :0], PSWAP,DSWAP[1 :0], BSTM_AVDDEXT	Input I/O	100	Ω
MTP_PWR	Power Supply	5	Ω
S[1]~S[720]	Source output	20	Ω
VSR_L[1]~ VSR_L[18], VSR_R[1]~ VSR_R[18]	GOA,SWoutput	20	Ω