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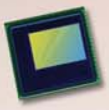

datasheet

PRELIMINARY SPECIFICATION

1/4" color CMOS QSXGA (5 megapixel) image sensor
with OmniBSI+™ technology

OV5645

color CMOS QSXGA (5 megapixel) image sensor with OmniBSI+™ technology

datasheet (CSP3)
PRELIMINARY SPECIFICATION

version 1.1
july 2012

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- toys
- PC multimedia
- digital still cameras

ordering information

- **OV05645-A66A** (color, lead-free)
  66-pin CSP3

features

- 1.4 µm x 1.4 µm pixel with OmniBSI+™ technology for high performance (high sensitivity, low crosstalk, low noise, improved quantum efficiency)
- optical size of 1/4"
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB), automatic band filter (ABF), automatic 50/60 Hz luminance detection, and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC 16-zone size/position/weight control, mirror and flip, cropping, windowing, and panning
- image quality controls: color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defective pixel canceling, and noise canceling
- support for output formats: RAW RGB, RGB565/555/444, YUV422/420, YCbCr422
- support for video or snapshot operations
- support for internal and external frame synchronization for frame exposure mode
- support for LED and flash strobe mode
- support for horizontal and vertical sub-sampling, binning
- support for minimizing artifacts on binned image
- support for data compression output
- support for anti-shake
- standard serial SCCB interface
- dual lane MIPI output interface
- embedded 1.5V regulator for core power
- programmable I/O drive capability, I/O tri-state configurability
- support for black sun cancellation
- support for images sizes: 5 megapixel, and any arbitrary size scaling down from 5 megapixel
- support for auto focus control (AFC) with embedded AF VCM driver
- embedded microcontroller
- suitable for module size of 8.5 x 8.5 x <6mm with both CSP and RW packaging

key specifications (typical)

- **active array size:** 2592 x 1944
- **power supply:**
  core: 1.5V ± 5% (with embedded 1.5V regulator)
  analog: 2.6 ~ 3.0V (2.8V typical)
  I/O: 1.8V / 2.8V
- **power requirements:**
  active: TBD
  standby: TBD
- **temperature range:**
  operating: -30°C to 70°C junction temperature (see **table 8-1**)
  stable image: 0°C to 50°C junction temperature (see **table 8-1**)
- **output formats:** 8-/10-bit RGB RAW, RGB565/555/444, YUV422/420, YCbCr422 output
- **lens size:** 1/4"
- **lens chief ray angle:** 29.1° (see **figure 10-2**)
- **input clock frequency:** 6~27 MHz
- **max S/N ratio:** 36 dB
- **dynamic range:** TBD
- maximum image transfer rate:
  QSXGA (2592x1944): 15 fps
  1080p: 30 fps
  1280x960: 45 fps
  720p: 60 fps
- **sensitivity:** TBD
- **shutter:** rolling shutter / frame exposure
- **maximum exposure interval:** 1964 x t_{ROW}
- **pixel size:** 1.4 µm x 1.4 µm
- **dark current:** TBD
- **image area:** 3673.6 µm x 2738.4 µm
- **package dimensions:** 6200 µm x 4860 µm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV5645 image sensor. The package information is shown in section 9.

table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description
A1	NC	–	no connect
A2	DVDD	power	power for digital circuit
A3	DOGND	ground	ground for I/O circuit
A4	SPI_CLK	I/O	SPI data clock input
A5	DGND	ground	ground for digital circuit
A6	FREX	I/O	frame exposure / mechanical shutter
A7	GPIO1	I/O	GPIO port 1
A8	DOVDD	power	power for I/O circuit
A9	DGND	ground	ground for digital circuit
A10	NC	–	no connect
B1	DGND	ground	ground for digital circuit
B2	DVDD	power	power for digital circuit
B3	DOVDD	power	power for I/O circuit
B4	AVDD	power	power for analog circuit
B5	DVDD	power	power for digital circuit
B6	GPIO3	I/O	GPIO port 3
B7	GPIO0	I/O	GPIO port 0
B8	DOGND	ground	ground for I/O circuit
B9	DVDD	power	power for digital circuit
B10	AVDD	power	power for analog circuit
C1	DGND	ground	ground for digital circuit
C2	DOVDD	power	power for I/O circuit
C3	AGND	ground	ground for analog circuit
C4	SPI_D1	I/O	SPI data 1 input
C5	SPI_D0	I/O	SPI data 0 input
C6	STROBE	I/O	strobe output

table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description
C7	GPIO2	I/O	GPIO port 2
C8	PWDNB	input	power down (active low with internal pull down resistor)
C9	RESETB	input	reset (active low with internal pull up resistor)
C10	AGND	ground	ground for analog circuit
D1	NC	–	no connect
D10	NC	–	no connect
E1	NC	–	no connect
E10	NC	–	no connect
F1	NC	–	no connect
F10	NC	–	no connect
G1	DGND	ground	ground for digital circuit
G2	SIOD	I/O	SCCB data
G3	SIOC	input	SCCB input clock
G4	VSYNC	I/O	DVP VSYNC output
G5	MCN	I/O	MIPI TX clock lane negative output
G6	MCP	I/O	MIPI TX clock lane positive output
G7	DOGND	ground	ground for I/O circuit
G8	VCMSINK	I/O	analog I/O
G9	VN	reference	internal analog reference
G10	AVDD	power	power for analog circuit
H1	DGND	ground	ground for digital circuit
H2	DVDD	power	power for digital circuit
H3	DOVDD	power	power for I/O circuit
H4	MDN0	I/O	MIPI TX first data lane negative output
H5	MDP0	I/O	MIPI TX first data lane positive output
H6	MDN1	I/O	MIPI TX second data lane negative output
H7	MDP1	I/O	MIPI TX second data lane positive output
H8	VCMGND	I/O	analog I/O
H9	VCMGND	I/O	analog I/O
H10	AGND	ground	ground for analog circuit

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description
J1	NC	–	no connect
J2	DVDD	power	power for digital circuit
J3	XVCLK	input	system input clock
J4	SGND	ground	ground for sensor circuit
J5	EGND	ground	ground for MIPI TX circuit
J6	EVDD	reference	power for MIPI TX circuit
J7	PVDD	power	power for PLL circuit
J8	VCMSINK	I/O	analog I/O
J9	VH	reference	internal analog reference
J10	NC	–	no connect

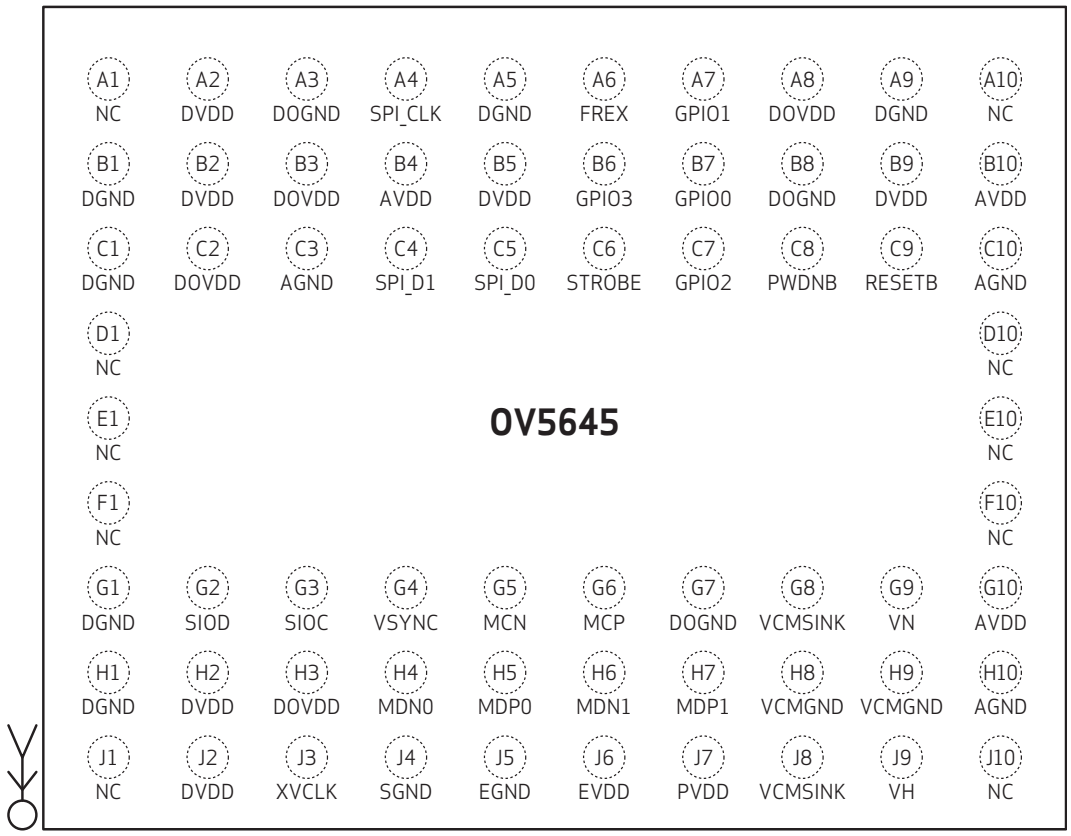
table 1-2 configuration under various conditions (sheet 1 of 2)

pin number	signal name	RESET_B	after RESET_B release	software standby	hardware standby
A4	SPI_CLK	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
A6	FREX	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
A7	GPIO1	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
B6	GPIO3	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
B7	GPIO0	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
C4	SPI_DAT1	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
C5	SPI_DAT0	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
C6	STROBE	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
C7	GPIO2	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
C8	PWDNB	input	input	input	input

table 1-2 configuration under various conditions (sheet 2 of 2)

pin number	signal name	RESET_B	after RESET_B release	software standby	hardware standby
C9	RESET_B	input	input	input	input
G2	SIOD	high-z	open drain	open drain	high-z
G3	SIOC	high-z	input	input	high-z
G4	VSYNC	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
G5	MCN	high	high	low by default (configurable)	low by default (configurable)
G6	MCP	high	high	low by default (configurable)	low by default (configurable)
G9	VN	high-z	high-z	high-z	high-z
H4	MDN0	high	high	low by default (configurable)	low by default (configurable)
H5	MDP0	high	high	low by default (configurable)	low by default (configurable)
H6	MDN1	high	high	low by default (configurable)	low by default (configurable)
H7	MDP1	high	high	low by default (configurable)	low by default (configurable)
J3	XVCLK	input	input	input	input
J9	VH	high-z	high-z	high-z	high-z

figure 1-1 pin diagram



5645_CSP3_DS_1_1

2 system level description

2.1 overview

The OV5645 color image sensor is a low voltage, high-performance, 1/4-inch 5 megapixel CMOS image sensor that provides the full functionality of a single chip 5 megapixel (2592x1944) camera using OmniBSI+™ technology in a small footprint. It provides full-frame, sub-sampled, windowed or arbitrarily scaled 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV5645 has an image array capable of operating at up to 15 frames per second (fps) 5 megapixel resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface or embedded microcontroller. In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise and smearing, to produce a clean, fully stable, color image.

The OV5645 has an embedded microcontroller, which can be combined with an internal autofocus engine and programmable general purpose I/O modules (GPIO) for external autofocus control. It also provides an anti-shake function with an internal anti-shake engine. For identification and storage purposes, the OV5645 also includes a one-time programmable (OTP) memory.

The OV5645 uses serial MIPI port for data transmission.

2.2 architecture

The OV5645 sensor core generates streaming pixel data at a constant frame rate, indicated by HREF and VSYNC. **figure 2-1** shows the functional block diagram of the OV5645 image sensor.

The timing generator outputs clocks to access the rows of the image array, precharging and sampling the rows of the imaging array sequentially. In the time between precharging and sampling a row, the charge in the pixels decrease with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV5645 block diagram

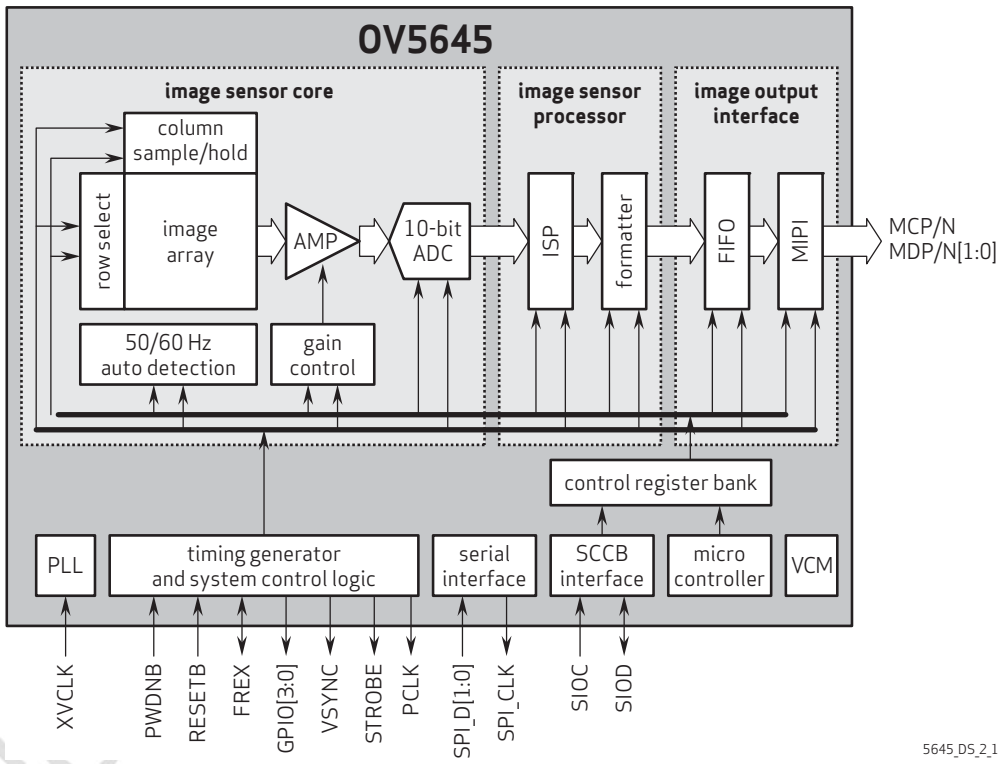
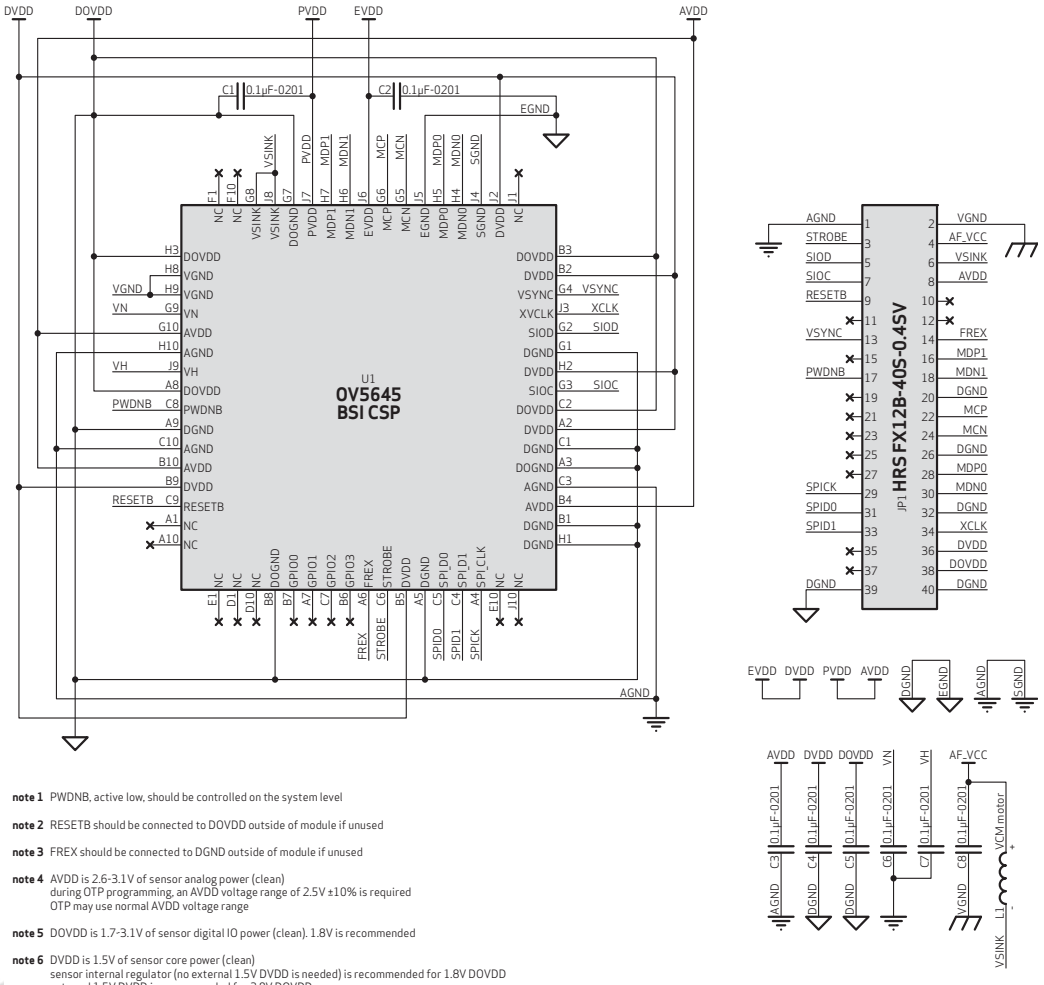


figure 2-2 reference schematic



note 1 PWDNB, active low, should be controlled on the system level

note 2 RESETB should be connected to DOVDD outside of module if unused

note 3 FREX should be connected to DGND outside of module if unused

note 4 AVDD is 2.6-3.1V of sensor analog power (clean)
during OTP programming, an AVDD voltage range of 2.5V ±10% is required
OTP may use normal AVDD voltage range

note 5 DOVDD is 1.7-3.1V of sensor digital IO power (clean). 1.8V is recommended

note 6 DVDD is 1.5V of sensor core power (clean)
sensor internal regulator (no external 1.5V DVDD is needed) is recommended for 1.8V DOVDD
external 1.5V DVDD is recommended for 2.8V DOVDD

note 7 sensor AGND and DGND should be separated and connected to a single point outside PCB (they should not be connected inside module).

note 8 DGND and EGND should be two separated nets and only connected at a single point inside the module

note 9 AGND and SGND should be two separated nets and only connected at a single point inside the module

note 10 capacitors should be close to the related sensor pins

note 11 if more space is available, use capacitor of 1µF-0402 between DVDD and DGND

note 12 EVDD/EGND are power/ground for MIPI core
MCP and MCN are MIPI clock lane positive and negative output
MDP0 and MDN0 are MIPI first data lane positive and negative output
MDP1 and MDN1 are MIPI second data lane positive and negative output

note 13 traces of MCP, MCN, MDP0, MDN0, MDP1 and MDN1 should have the same or similar length
differential impedance of the clock pair and data pair transmission lines should be controlled at 100 Ohm

note 14 traces from AF_VCC to L1+ and L1- to pin VSINK, and the trace of VGND needs to be wide because of 100 mA high electrical current

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2.3 format and frame rate

table 2-1 format and frame rate

format	resolution	frame rate (fps)	methodology	MIPI (total bit rate, Mbps)		
				Raw10	Raw8	YUV422
5 Mpixel	2592x1944	15	no scaling	840	672	1344
SXGA	1280x960	45	2x2 binning	840	672	1344
1080p	1920x1080	30	cropping	840	672	1344
720p	1280x720	60	cropping + 2x2 binning	840	672	1344

2.4 I/O control

The OV5645 I/O pad direction and driving capability can be easily adjusted. **table 2-2** lists the driving capability and direction control registers of the I/O pads.

table 2-2 driving capability and direction control for I/O pads (sheet 1 of 2)

function	register	default value	R/W	description
output drive capability control	0x302C	0x02	RW	Bit[7:6]: output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
CSD[1:0] I/O control	0x3016	0x00	RW	Bit[3:2]: input/output control for the CSD[1:0] pins 0: input 1: output
CSD[1:0] output select	0x301C	0x00	RW	Bit[3:2]: output selection for the CSD[1:0] pins 0: normal data path 1: register-controlled value
CSD[1:0] output value	0x3019	0x00	RW	Bit[3:2]: CSD[1:0] output value
CSD[1:0] input value	0x3050	–	R	Bit[7:6]: CSD[1:0] input value
VSYNC I/O control	0x3017	0x00	RW	Bit[6]: input/output control for the VSYNC pin 0: input 1: output

table 2-2 driving capability and direction control for I/O pads (sheet 2 of 2)

function	register	default value	R/W	description
VSYNC output select	0x301D	0x00	RW	Bit[6]: output selection for the VSYNC pin 0: normal data path 1: register-controlled value
VSYNC output value	0x301A	0x00	RW	Bit[6]: VSYNC output value
VSYNC input value	0x3051	–	R	Bit[6]: VSYNC input value
CSK I/O control	0x3017	0x00	RW	Bit[4]: input/output control for the CSK pin 0: input 1: output
CSK output select	0x301D	0x00	RW	Bit[4]: output selection for the CSK pin 0: normal data path 1: register-controlled value
CSK output value	0x301A	0x00	RW	Bit[4]: CSK output value
CSK input value	0x3051	–	R	Bit[4]: CSK input value
GPIO I/O control	0x3018	0x00	RW	Bit[3:0]: input/output control for the GPIO[3:0] pins 0: input 1: output
GPIO output select	0x301E	0x00	RW	Bit[3:0]: output selection for the GPIO[3:0] pins 0: normal data path 1: register-controlled value
GPIO output value	0x301B	0x00	RW	Bit[3:0]: GPIO[3:0] output value
GPIO input value	0x3052	–	R	Bit[3:0]: GPIO[3:0] input value

2.5 system clock control

The OV5645 PLL allows for an input clock frequency ranging from 6~27 MHz and has a maximum VCO frequency of 1000 MHz.

figure 2-3 PLL diagram

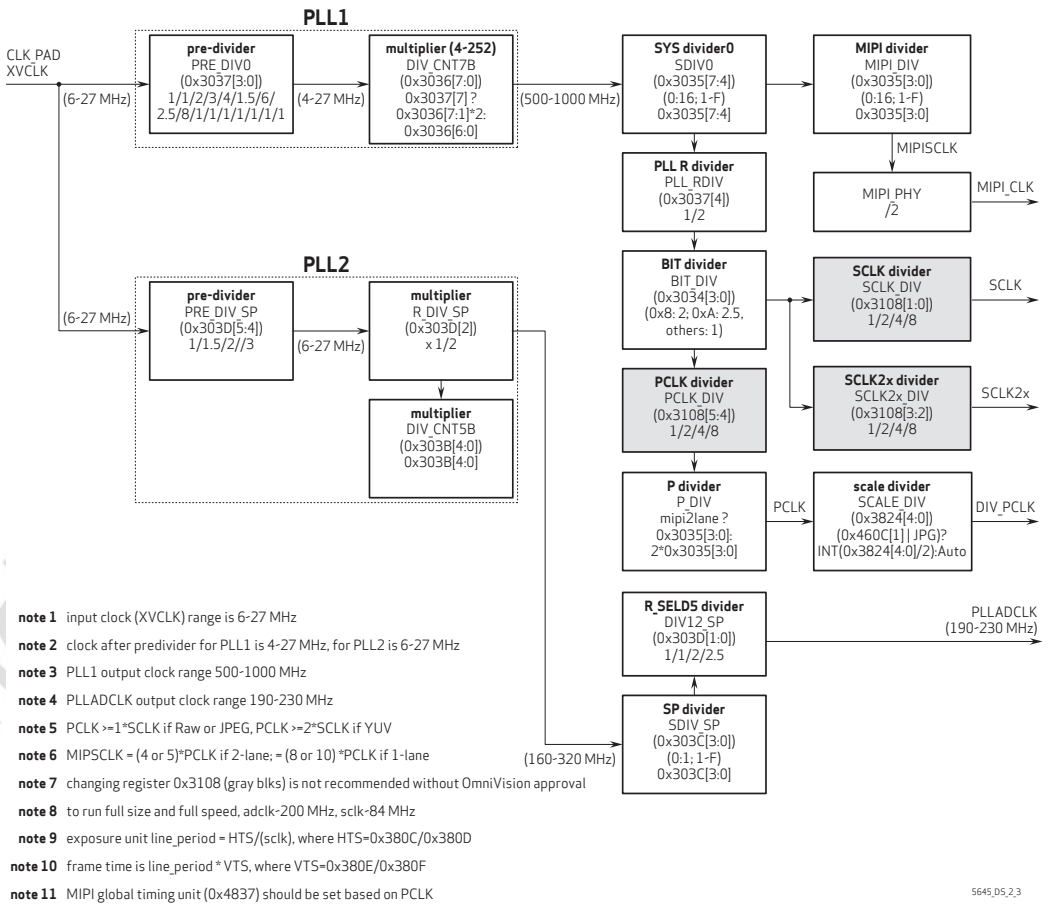


table 2-3 PLL configurations

configuration	register 0x3034	register 0x3035	register 0x3036	register 0x3037	register 0x3108[a]	register 0x303B	register 0x303C	register 0x303D
default	0x1A	0x11	0x69	0x13	0x16	0x19	0x11	0x30
MIPI 8-bit	0x18	0x11	0x54	0x13	0x01	0x19	0x11	0x30

a. register 0x3108 shall be kept at 0x01 for all settings due to the relation constraints of the different internal clocks

2.6 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Group write is supported in order to update a group of registers in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary.

The OV5645 supports up to four groups. These groups share 1 KB RAM and the size of each group is programmable by adjusting the start address. The group hold start addresses range from 0x40 to 0x7F, where the unit is 16 bytes.

table 2-4 group sharing registers

address	register name	default value	R/W	description
0x3200	GROUP ADDR0	0x40	RW	Start Address for Group0 {group_addr0[7:0], 4'h0}
0x3201	GROUP ADDR1	0x4A	RW	Start Address for Group1 {group_addr1[7:0], 4'h0}
0x3202	GROUP ADDR2	0x54	RW	Start Address for Group2 {group_addr2[7:0], 4'h0}
0x3203	GROUP ADDR3	0x5E	RW	Start Address for Group3 {group_addr3[7:0], 4'h0}

The group write function is controlled by register **0x3212**.

table 2-5 group write registers

address	register name	default value	R/W	description
0x3212	SRM GROUP ACCESS	–	W	SRM Group Access Bit[7]: Group launch enable Bit[6]: Test mode access group Bit[5]: Group launch Bit[4]: Group hold end Bit[3:0]: Group ID 00xx: Group ID 01xx: Reserved 1xxx: Reserved
0x3213	SRM GROUP STATUS	–	R	SRM Group Status Bit[7]: Store default Bit[6]: Restore Bit[5]: Group hold Bit[4]: Group launch Bit[3]: Group write Bit[2:0]: Group select

The SCCB will enter group write mode after writing to register **0x3212** with a valid group ID. The subsequent registers will be held to the buffer specified by the group_id instead of writing to the registers. Make sure the number of registers does not exceed the capacity of the group. Setting group_hold_end to 1 will exit the group write mode. After that, setting both group_launch and group_launch_en to 1 will write the buffered values to the real registers. Multiple groups of registers can be prepared before writing to the real registers but be sure the correct group_id is specified when the group write is launched.

The following is an example demonstrating the group write operation:

```
78  3212  00    Enable group0
78  3600  00    Write registers to be held in group0
78  3601  01
78  3212  10    End group0
78  3212  01    Enable group1
78  3602  02    Write registers to be held in group1
78  3603  03
78  3212  11    End group1

.......................Other direct register access

78  3212  02    Enable group2
78  3604  04    Write registers to be held in group2
78  3605  05
78  3212  12    End group2

78  3212  A0    Launch group0

.......................Other direct register access

78  3212  03    Enable group3
78  3606  06    Write registers to be held in group3
78  3607  07
78  3212  13    End group3

78  3212  A1    Launch group1
78  3212  A2    Launch group2
78  3212  A3    Launch group3
```

2.7 power up sequence

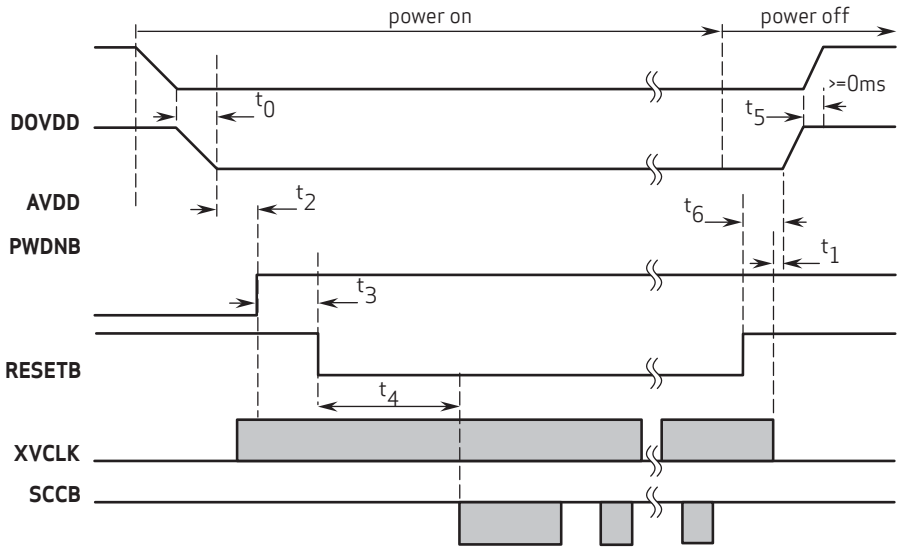
Based on the system power configuration (1.8V or 2.8V for I/O power, using external DVDD or internal DVDD, requiring access to the SCCB during power up period or not), the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred. If 2.8V is used for I/O power, due to a high voltage drop in the internal DVDD regulator, there is a potential heating issue. Hence, for a 2.8V power system, OmniVision recommends using an external DVDD power supply. Due to the higher power down current when using external DVDD, OmniVision strongly recommends cutting off all power, including the external DVDD, when the sensor is not in use in the case of 2.8V I/O and external DVDD.

2.7.1 power up with internal DVDD

For powering up with an internal DVDD and SCCB access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. PWDNB is active low with an asynchronized design (does not need clock)
3. PWDNB must be low if SCCB is accessed during the power up period
4. if PWDNB pin is controlled as below, for PWDNB to go high, power must first become stable. System needs to drive PWNDB to high as the sensor has an internal pull down on PWDNB pin (AVDD to PWDNB ≥ 5 ms)
5. RESETB is active low with an asynchronized design
6. master clock XVCLK should be provided at least 1 ms before host accesses the sensor's registers
7. host can access SCCB bus (if shared) during entire period. 20ms after RESETB goes high, host can access the sensor's registers to initialize sensor

figure 2-4 power up timing with internal DVDD



note $t_0 \geq 0$ms, delay from DOVDD stable to AVDD stable, it is recommended to power up AVDD shortly after DOVDD has been powered up
$t_1 \geq 0$ms, delay from XVCLK off to AVDD off
$t_2 \geq 5$ms, delay from AVDD stable to sensor power up stable, PWDNB can be driven high after this point, XVCLK can be turned on after power on
$t_3 \geq 1$ms, delay from sensor power up stable to RESETB pull up
$t_4 \geq 20$ms, delay from RESETB pull high to SCCB initialization
$t_5 \geq 0$ms, delay from AVDD off to DOVDD off
$t_6 \geq 0$ms, delay from RESETB pull low to AVDD off

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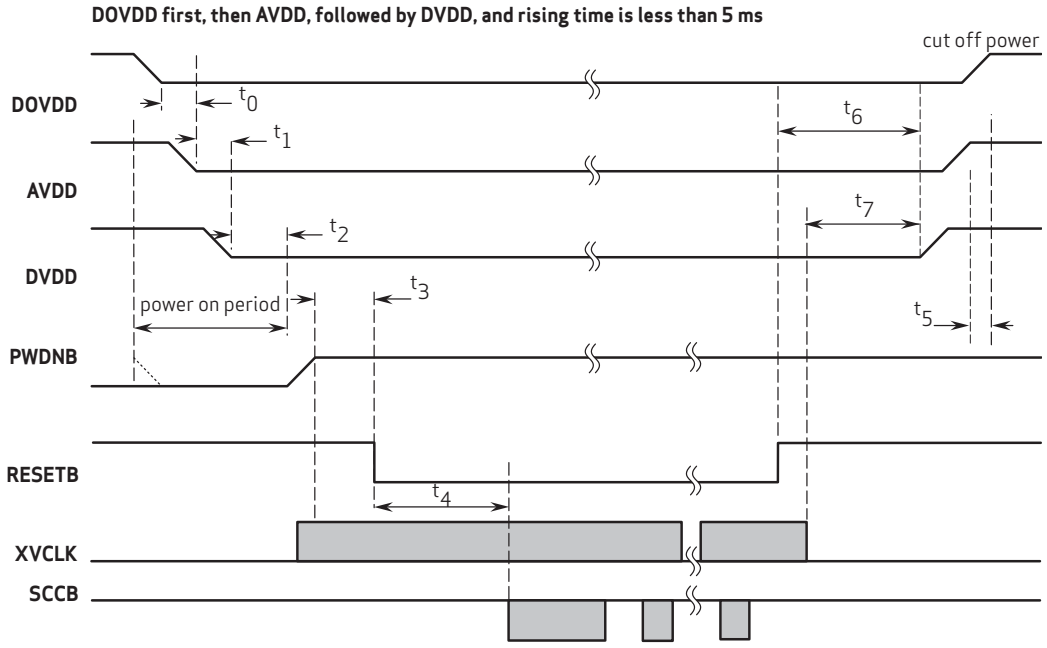
2.7.2 power up with external DVDD source

For powering up with an external DVDD source and SCCB access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. when AVDD and DVDD are turned ON, make sure AVDD becomes stable before DVDD becomes stable
3. PWDNB is active low with an asynchronized design (does not need clock), PWDNB must be low if SCCB is accessed during the power up period
4. if PWDNB pin is controlled as below, for PWDNB to go high, power must first become stable. System needs to drive PWDNB to high as the sensor has an internal pull down on PWDNB pin (DVDD to PWDNB ≥ 5 ms)
5. all power supplies are cut off when the camera is not in use (power down mode is not recommended)
6. RESETB is active low with an asynchronized design
7. master clock XVCLK should be provided at least 1 ms before host accesses the sensor's registers
8. host can access SCCB bus (if shared) during entire period. 20ms after RESETB goes high, host can access the sensor's registers to initialize sensor

figure 2-5 power up timing with external DVDD source



note $t_0 \geq 0$ ms: delay from DOVDD stable to AVDD stable, it is recommended to power up AVDD shortly after DOVDD has been powered up
$t_1 \geq 0$ ms: delay from AVDD stable to DVDD stable
$t_2 \geq 5$ ms: delay from DVDD stable to sensor power up stable
$t_3 \geq 1$ms, delay from sensor power up stable to RESETB pull up
$t_4 \geq 20$ms, delay from RESETB pull high to SCCB initialization
$t_5 \geq 0$ms, delay from AVDD off to DOVDD off
$t_6 \geq 0$ms, delay from RESETB pull low to DVDD off
$t_7 \geq 0$ms, delay from XVCLK off to DVDD off

5640_DS_2_5

2.8 reset

The OV5645 sensor includes a **RESETB** pin that forces a complete hardware reset when it is pulled low (GND). The OV5645 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register **0x3008**[7] to high.

Manually applying a hard reset upon power up is required even though on-chip reset is included. The hard reset is active low with an asynchronized design. The reset pulse width should be greater than or equal to 1 ms.

2.9 hardware and software standby

Two suspend modes are available for the OV5645:

- hardware standby
- SCCB software standby

To initiate hardware standby mode, the **PWDNB** pin must be tied to low (while in MIPI mode, set register 0x300E[4:3] to 2'b11 before the PWDNB pin is set to low). When this occurs, the OV5645 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software standby through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

3 block level description

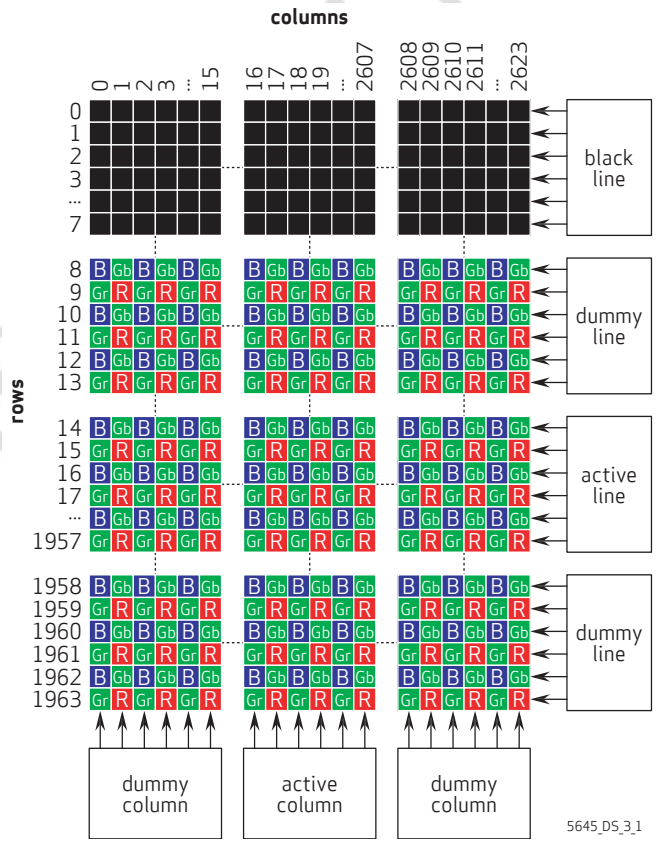
3.1 pixel array structure

The OV5645 sensor has an image array of 2624 columns by 1964 rows (5,153,536 pixels). figure 3-1 shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 5,153,536 pixels, 5,038,848 (2592x1944) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

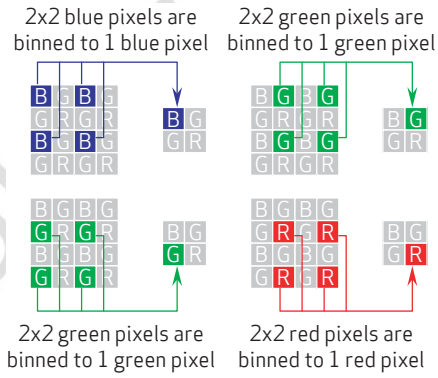
figure 3-1 sensor array region color filter layout



3.2 subsampling

There are two subsampling modes in the OV5645: binning and skipping. Both are acceptable methods of reducing output resolution while maintaining the field of view. Binning is usually preferred as it increases the pixel's signal-to-noise ratio. When the binning function is ON, voltage levels of adjacent pixels are averaged. In skipping mode (binning function is OFF), alternate pixels, which are not output, are merely skipped. The OV5645 supports 2x2 binning. **figure 3-2** illustrates 2x2 binning, where the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged before entering the ADC. See **table 3-1** for horizontal and vertical binning registers.

figure 3-2 example of 2x2 binning



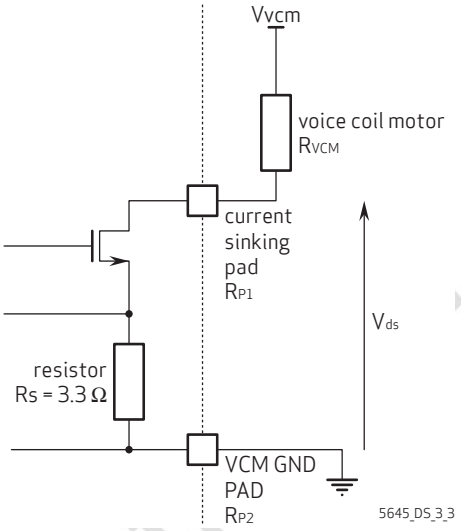
Sensor timing adjustment is necessary after applying binning. Please consult your local OmniVision FAE for details.

table 3-1 horizontal and vertical binning registers

address	register name	default value	R/W	description
0x3820	TIMING_TC_REG20	0x40	RW	Bit[0]: Vertical binning 0: Disable 1: Enable
0x3821	TIMING_TC_REG21	0x00	RW	Bit[0]: Horizontal binning 0: Disable 1: Enable

3.3 VCM driver

figure 3-3 VCM block diagram



The maximum SINK current can be estimated as:

- ISINK = (Vvcm - Vds) / (Rs + Rvcm + Rp1 + Rp2)
- Vds is the transistor headroom
- Rp1 and Rp2 are the resistance in the current path
- RVCM is the resistance of the voice coil motor.

The OV5645 VCM driver is a single 10-bit DAC with 100 mA output current sink capability. It is designed for linear control of the VCM. The DAC is controlled via the SCCB interface with clock rates up to 400 Hz. The OV5645 VCM driver provides three types of output current control modes that allow users to adjust transient response of the sinking current.

3.3.1 output current control mode

The OV5645 VCM driver uses 4 bits (S3, S2, S1, and S0) to control the output current response.

1. S[3:0] = X000: Directly jump mode: code directly jumps to target code. Output current transient response time (see **table 3-2**.)
2. S[3:0] = 0001 to 0111: Single step mode: code increases/decreases by a single step. Single step time durations are 50µs, 100µs, 200µs, 400µs, 800µs, 1600µs, and 3200µs, which are controlled by S2, S1, and S0 (see **table 3-4**.)
3. S[3:0] = 1001 to 1111: Multi-code steps mode: Code increases/decreases in multi-code steps. If the target code and the current code have a difference larger than 128, the 64-code step is applied first. When the difference in between target and current codes is no more than 128 but larger than 16, the 16-code step is used. When the difference is less than 16, it will directly jump to the target code. Single step time options are 50µs, 100µs, 200µs, 400µs, 800µs, 1600µs, and 3200µs, which are controlled by S2, S1, and S0, (see **table 3-5**.)

table 3-2 VCM driver control

function	register	description
current transient response control	0x3602	Bit[3:0]: Current transient response control x000: mode 0 0001~0111: mode 1 1001~1111: mode 2
10-bit DAC code	0x3603[5:0], 0x3602[7:4]	0x3603[5:0]: D[9:4] 0x3602[7:4]: D[3:0]
clock divider	0x3605[3:0], 0x3606[7:0]	divide external clock to obtain a 20 kHz clock for VCM control block VCM control clock = external clock / Rdiv[11:0]

table 3-3 VCM control registers

address	register name	default value	R/W	description
0x3603	VCM[15:8]	0x01	RW	Bit[7]: PD Bit[5:0]: D[9:4]
0x3602	VCM[7:0]	0x50	RW	Bit[7:4]: D[3:0] Bit[3]: S3 Bit[2:0]: S[2:0]
0x3605	SLEW[11:8]	0x46	RW	Bit[3:0]: Rdiv[11:8]
0x3604	SLEW[7:0]	0x05	RW	Bit[7:0]: Rdiv[7:0]
0x3606	VCM CURRENT	0x00	RW	Bit[2:0]: VCM output current control 000: 0.71 * Id 001: 0.77 * Id 010: 0.83 * Id 011: 0.91 * Id 100: 1.00 * Id 101: 1.11 * Id 110: 1.25 * Id 111: 1.43 * Id

table 3-4 single step mode

mode	S3	S2	S1	S0	single step transition time	full scale transition time (1023 steps)
single step mode	0	0	0	1	50µs	51.15ms
	0	0	1	0	100µs	102.3ms
	0	0	1	1	200µs	204.6ms
	0	1	0	0	400µs	409.2ms
	0	1	0	1	800µs	818.4ms
	0	1	1	0	1600µs	1.637s
	0	1	1	1	3200µs	3.274s

table 3-5 multi-code step mode

mode	S3	S2	S1	S0	single step transition time	full scale transition time (22 steps)[a]
single step mode	1	0	0	1	50µs	1.1ms
	1	0	1	0	100µs	2.2ms
	1	0	1	1	200µs	4.4ms
	1	1	0	0	400µs	8.8ms
	1	1	0	1	800µs	17.6ms
	1	1	1	0	1600µs	35.2ms
	1	1	1	1	3200µs	70.4ms

a. a full scale transition includes fourteen 64-code steps, seven 16-code steps and one directly jump step.

figure 3-4 1/4 to 3/4 scale settling time (directly jump mode, VDD = 3.0V)

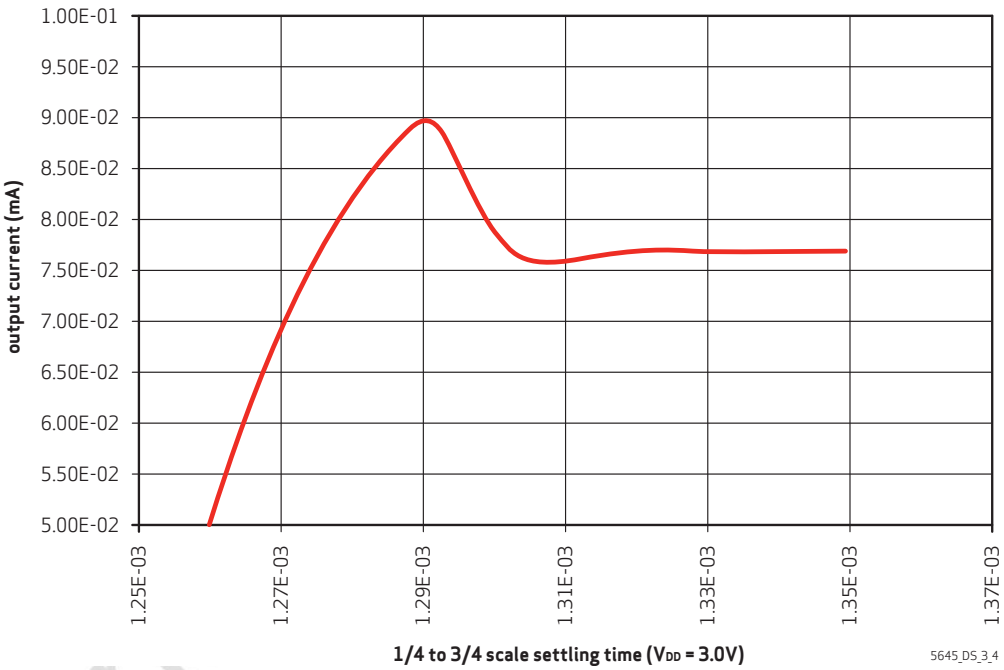
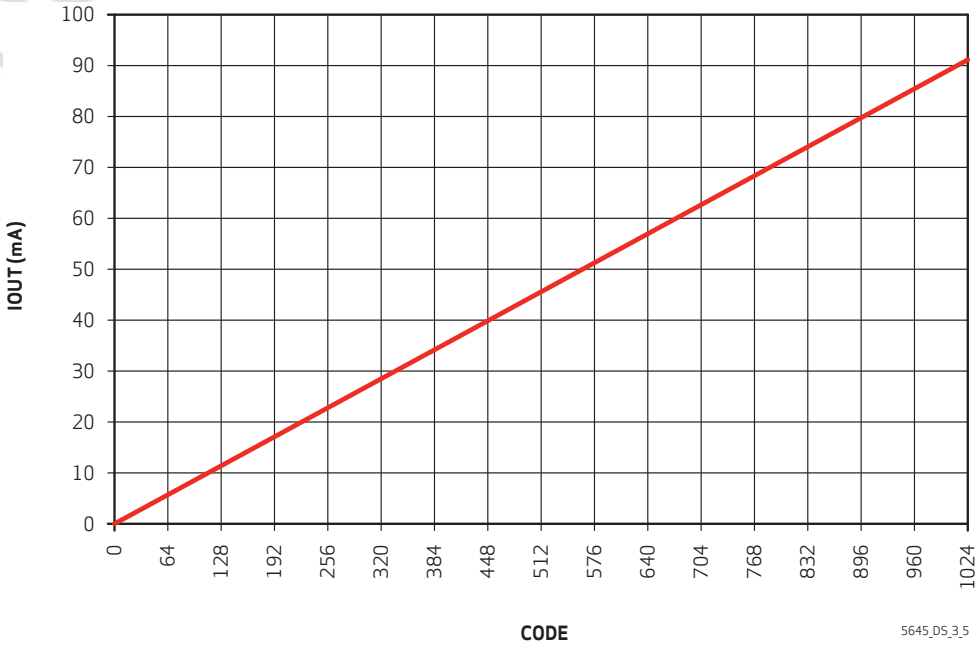


figure 3-5 sink current vs. code (VDD = 3.0V, reg 0x30A5 = 0x05, VCM resistance = 23ohms)



4 image sensor core digital functions

4.1 mirror and flip

The OV5645 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**). In flip, the OV5645 does not need additional settings because the ISP block will auto-detect whether the pixel is in the red line or blue line and make the necessary adjustments.

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

5645_DS_4_1

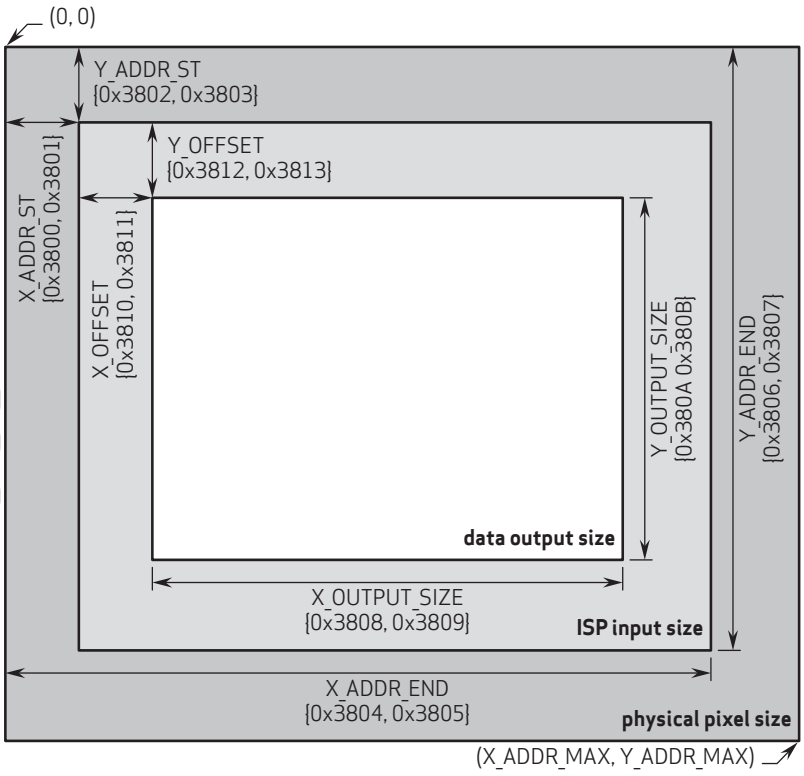
table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3820	TIMING TC REG20	0x40	RW	Timing Control Bit[2]: ISP vflip Bit[1]: Sensor vflip
0x3821	TIMING TC REG21	0x00	RW	Timing Control Bit[2]: ISP mirror Bit[1]: Sensor mirror

4.2 image windowing

The OV5645 uses registers 0x3800 ~ 0x3814 for image windowing. **figure 4-2** illustrates how the registers define the windowing size. Physical pixel size is the total pixel array size we have in the sensor. The ISP input size is the total pixel data read from pixel array. Typically, the larger ISP input size is, the less maximum frame rate can be reached. The data output size is the image output size of OV5645. This size is windowed from ISP input size and is defined by x_offset and y_offset as **figure 4-2** shows.

figure 4-2 image windowing



5645_DS_4_2

figure 4-3 shows the windowing configuration when scaling function is enabled. The pre-scaling image size is the ISP input size subtracted by two times of offsets for both horizontal and vertical.

figure 4-3 image windowing configuration

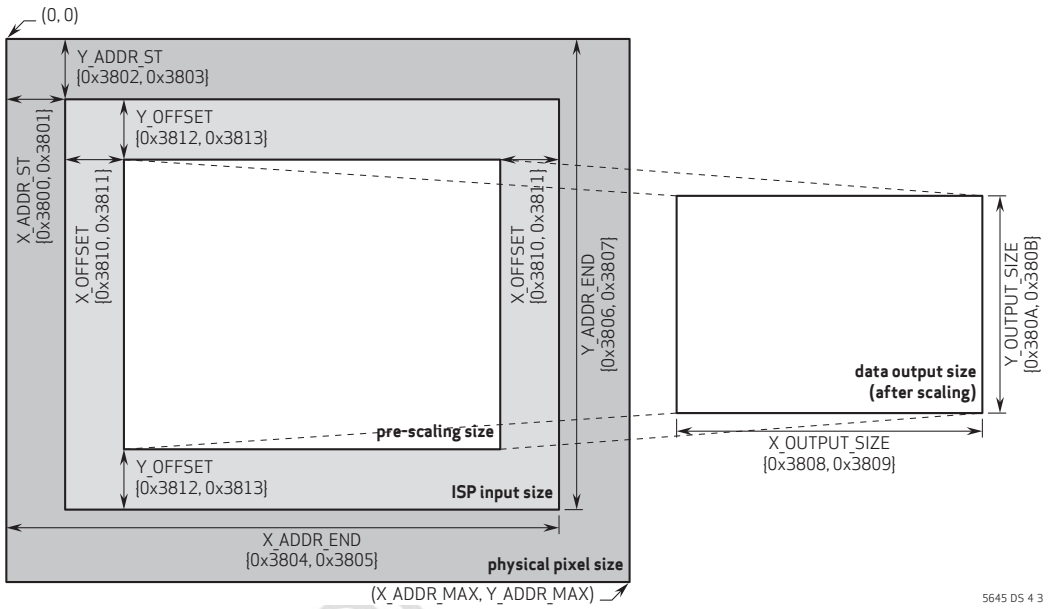


table 4-2 image windowing registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	TIMING HS	0x00	RW	Bit[3:0]: X address start[11:8]
0x3801	TIMING HS	0x00	RW	Bit[7:0]: X address start[7:0]
0x3802	TIMING VS	0x00	RW	Bit[2:0]: Y address start[10:8]
0x3803	TIMING VS	0x00	RW	Bit[7:0]: Y address start[7:0]
0x3804	TIMING HW	0x0A	RW	Bit[3:0]: X address end[11:8]
0x3805	TIMING HW	0x3F	RW	Bit[7:0]: X address end[7:0]
0x3806	TIMING VH	0x07	RW	Bit[2:0]: Y address end[10:8]
0x3807	TIMING VH	0x9F	RW	Bit[7:0]: Y address end[7:0]
0x3808	TIMING DVPHO	0x0A	RW	Bit[3:0]: DVP output horizontal width[11:8]
0x3809	TIMING DVPHO	0x20	RW	Bit[7:0]: DVP output horizontal width[7:0]
0x380A	TIMING DVPVO	0x07	RW	Bit[2:0]: DVP output vertical height[10:8]
0x380B	TIMING DVPVO	0x98	RW	Bit[7:0]: DVP output vertical height[7:0]

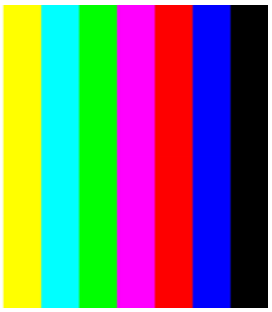
table 4-2 image windowing registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x380C	TIMING HTS	0x0B	RW	Bit[3:0]: Total horizontal size[11:8]
0x380D	TIMING HTS	0x1C	RW	Bit[7:0]: Total horizontal size[7:0]
0x380E	TIMING VTS	0x07	RW	Bit[7:0]: Total vertical size[15:8]
0x380F	TIMING VTS	0xB0	RW	Bit[7:0]: Total vertical size[7:0]
0x3810	TIMING HOFFSET	0x00	RW	Bit[3:0]: ISP horizontal offset[11:8]
0x3811	TIMING_HOFFSET	0x10	RW	Bit[7:0]: ISP horizontal offset[7:0]
0x3812	TIMING VOFFSET	0x00	RW	Bit[2:0]: ISP vertical offset[10:8]
0x3813	TIMING VOFFSET	0x04	RW	Bit[7:0]: ISP vertical offset[7:0]

4.3 test pattern

For testing purposes, the OV5645 offers one type of test pattern, color bar.

figure 4-4 test pattern



color bar

table 4-3 test pattern selection control

address	register name	default value	R/W	description
0x503D	PRE ISP TEST SETTING 1	0x00	RW	Bit[7]: Color bar enable 0: Test disable 1: Color bar enable Bit[3:2]: Color bar style 00: Standard eight color bar 01: Gradual change at vertical mode 1 10: Gradual change at horizontal 11: Gradual change at vertical mode 2

4.4 50/60Hz detection

When the integration time is not an integer multiple of the period of light intensity, the image will flicker. The function of the detector is to detect whether the sensor is under a 50 Hz or 60 Hz light source so that the basic step of integration time can be determined. Contact your local OmniVision FAE for auto detection settings.

4.5 AEC/AGC algorithms

The auto exposure control (AEC) and auto gain control (AGC) allows the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-4**.

table 4-4 AEC/AGC algorithm functions

address	register name	default value	R/W	description
0x3500	AEC PK EXPOSURE	0x00	RW	Exposure Output Bit[3:0]: Exposure[19:16]
0x3501	AEC PK EXPOSURE	0x02	RW	Exposure Output Bit[7:0]: Exposure[15:8]
0x3502	AEC PK EXPOSURE	0x00	RW	Exposure Output Bit[7:0]: Exposure[7:0] Lower four bits are a fraction of a line; they should be 0 since OV5645 does not support fraction line exposure
0x3503	AEC PK MANUAL	0x00	RW	AEC Manual Mode Control Bit[1]: AGC manual 0: Auto enable 1: Manual enable Bit[0]: AEC manual 0: Auto enable 1: Manual enable
0x350A	AEC PK REAL GAIN	0x00	RW	Real Gain Bit[1:0]: Real gain[9:8]
0x350B	AEC PK REAL GAIN	0x10	RW	Real Gain Bit[7:0]: Real gain[7:0]
0x350C	AEC PK VTS	0x00	RW	AEC VTS Output Bit[7:0]: VTS[15:8]
0x350D	AEC PK VTS	0x00	RW	AEC VTS Output Bit[7:0]: VTS[7:0]

4.5.1 average-based algorithm

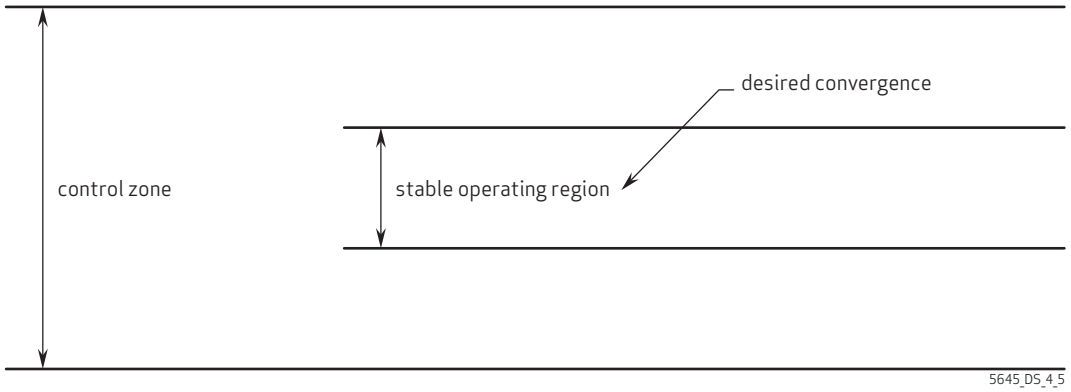
The average-based AEC controls image luminance using registers (0x3A0F), (0x3A10), (0x3A1B), and (0x3A1E). In average-based mode, the value of register (0x3A0F) indicates the high threshold value, and the value of register (0x3A10) indicates the low threshold value. The value of register (0x3A1B) indicates the high threshold value for image change from stable state to unstable state and the value of register (0x3A1E) indicates the low threshold value for image change from stable state to unstable state. When the target image luminance average value AVG READOUT (0x56A1) is within the range specified by registers (0x3A1B) and (0x3A1E), the AEC keeps the image exposure and gain. When register AVG READOUT (0x56A1) is greater than the value in register (0x3A1B), the AEC will decrease the image exposure and gain until it falls into the range of {0x3A10, 0x3A0F}. When register AVG READOUT (0x56A1) is less than the value in register (0x3A1E), the AEC will increase the image exposure and gain until it falls into the range of {0x3A10, 0x3A0F}. Accordingly, the value in register (0x3A0F) should be greater than the value in register (0x3A10). The gap between the values of registers (0x3A1B) and (0x3A1E) controls the image stability.

The AEC function supports both manual and auto speed selections in order to bring the image exposure into the range set by the values in registers (0x3A0F) and (0x3A10). For manual mode, the speed supports both normal and fast speed selection. AEC set to normal mode will allow for the slowest step increment or decrement in the image exposure to maintain the specified range. AEC set to fast mode will provide for an approximate ten-step increment or decrement in the image exposure to maintain the specified range. For auto mode, the speed step will automatically be adjusted according to the difference between the target and present values. The auto ratio of steps can be set by register bits AVG READOUT (0x56A1); thus, the AEC speed can be adjusted automatically by the image average value or controlled manually.

Register (0x3A11) and register (0x3A1F) controls the fast AEC range in manual speed selection made. If the target image AVG READOUT (0x56A1) is greater than (0x3A11), AEC will decrease by half. If register AVG READOUT (0x56A1) is less than (0x3A1F), AEC will double.

As shown in desired convergence, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size of fast and slow conditions.

figure 4-5 desired convergence



As for auto mode, the AEC will automatically calculate the steps needed based on the difference between target and current values. So, the outer control zone is meaningless for this mode.

table 4-5 AEC functions

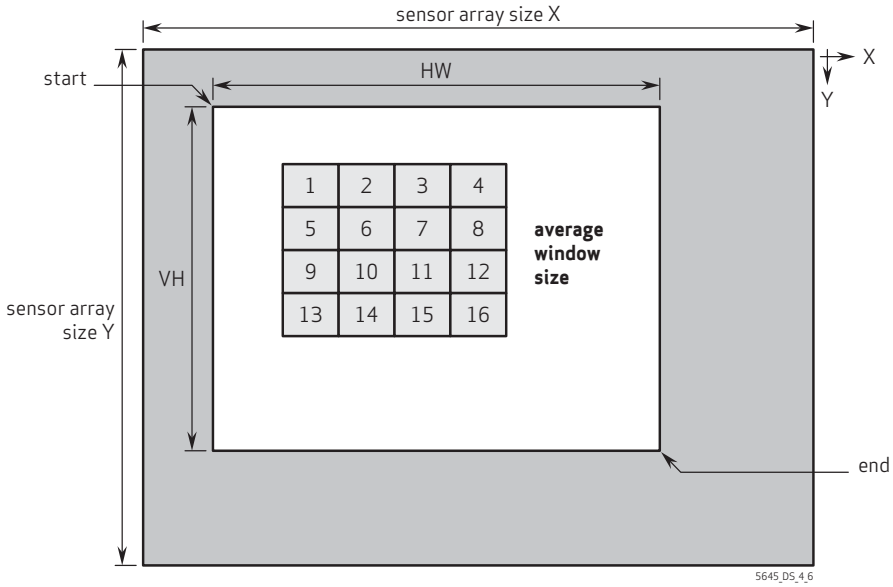
address	register name	default value	R/W	description
0x3A0F	AEC CTRL0F	0x78	RW	Stable Range High Limit (enter) Bit[7:0]: WPT
0x3A10	AEC CTRL10	0x68	RW	Stable Range Low Limit (enter) Bit[7:0]: BPT
0x3A11	AEC CTRL11	0xD0	RW	Step Manual Mode, Fast Zone High Limit Bit[7:0]: vpt_high
0x3A1B	AEC CTRL1B	0x78	RW	Stable Range High Limit (go out) Bit[7:0]: WPT2
0x3A1E	AEC CTRL1E	0x68	RW	Stable Range Low Limit (go out) Bit[7:0]: BPT2
0x3A1F	AEC CTRL1F	0x40	RW	Step Manual Mode, Fast Zone Low Limit Bit[7:0]: vpt_low

For the average-based AEC/AGC algorithm, the measured window is horizontally and vertically adjustable and divided by sixteen (4x4) zones (see **figure 4-6**). Each zone (or block) is 1/16th of the image and has a 4-bit weight in calculating the average luminance (YAVG). The 4-bit weight could be n/16 where n is from 0 to 15. The final YAVG is the weighted average of the sixteen zones.

4.5.1.1 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. By properly setting x_start, x_end, y_start, and y_end as shown in **figure 4-6**, a 4x4 grid average window is defined. It will automatically divide each zone into 4x4 zones. The average value is the weighted average of the 16 sections. **table 4-6** lists the corresponding registers.

figure 4-6 average-based window definition



note 1 = window 0,0 / 2 = window 0,1 / 3 = window 0,2 ..... 16 = window 3,3

table 4-6 timing control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3810	TIMING HOFFSET	0x00	RW	Bit[3:0]: ISP horizontal offset[11:8]
0x3811	TIMING_HOFFSET	0x04	RW	Bit[7:0]: ISP horizontal offset[7:0]
0x3812	TIMING VOFFSET	0x11	RW	Bit[3:0]: ISP vertical offset[11:8]
0x3813	TIMING VOFFSET	0x11	RW	Bit[7:0]: ISP vertical offset[7:0]
0x3808	TIMING DVPHO	0x07	RW	Bit[3:0]: DVP output horizontal width[11:8]
0x3809	TIMING DVPHO	0x98	RW	Bit[7:0]: DVP output horizontal width[7:0]
0x380A	TIMING DVPVO	0x0B	RW	Bit[3:0]: DVP output vertical height[11:8]
0x380B	TIMING DVPVO	0x1C	RW	Bit[7:0]: DVP output vertical height[7:0]
0x501D	ISP MISC	0x00	RW	Bit[4]: Average size manual enable
0x5680	X START	0x00	RW	Bit[3:0]: X start[11:8] Horizontal start position for average window high byte, valid when 0x501D[4]=1
0x5681	X START	0x00	RW	Bit[7:0]: X start[7:0] Horizontal start position for average window low byte, valid when 0x501D[4]=1

table 4-6 timing control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x5682	Y START	0x00	RW	Bit[2:0]: Y start[10:8] Vertical start position for average window low byte, valid when 0x501D[4]=1
0x5683	Y START	0x00	RW	Bit[7:0]: Y start[7:0] Vertical start position for average window low byte, valid when 0x501D[4]=1
0x5684	X WINDOW	0x10	RW	Bit[3:0]: Window X[11:8] Horizontal end position for average window high byte, valid when 0x501D[4]=1
0x5685	X WINDOW	0xA0	RW	Bit[7:0]: Window X[7:0] Horizontal end position for average window low byte, valid when 0x501D[4]=1.
0x5686	Y WINDOW	0x0C	RW	Bit[2:0]: Window Y[10:8] Vertical end position for average window high byte, valid when 0x501D[4]=1
0x5687	Y WINDOW	0x78	RW	Bit[7:0]: Window Y[7:0] Vertical end position for average window low byte, valid when 0x501D[4]=1
0x5688	WEIGHT00	0x11	RW	Bit[7:4]: Window 01 weight Bit[3:0]: Window 00 weight
0x5689	WEIGHT01	0x11	RW	Bit[7:4]: Window 03 weight Bit[3:0]: Window 02 weight
0x568A	WEIGHT02	0x11	RW	Bit[7:4]: Window 11 weight Bit[3:0]: Window 10 weight
0x568B	WEIGHT03	0x11	RW	Bit[7:4]: Window 13 weight Bit[3:0]: Window 12 weight
0x568C	WEIGHT04	0x11	RW	Bit[7:4]: Window 21 weight Bit[3:0]: Window 20 weight
0x568D	WEIGHT05	0x11	RW	Bit[7:4]: Window 23 weight Bit[3:0]: Window 22 weight
0x568E	WEIGHT06	0x11	RW	Bit[7:4]: Window 31 weight Bit[3:0]: Window 30 weight
0x568F	WEIGHT07	0x11	RW	Bit[7:4]: Window 33 weight Bit[3:0]: Window 32 weight

4.6 AEC/AGC steps

The AEC and AGC work together to achieve optimal exposure and gain based on the environmental illumination. In order to achieve the best signal-to-noise ratio (SNR), extending the exposure time is always preferred to raising the analog gain when the illumination level is decreasing. Similarly, with increasing illumination, decreasing the gain prior to shortening the exposure time is preferred.

4.6.1 auto exposure control (AEC)

The function of the AEC is to calculate the integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain the same.

To avoid image flickering under a periodic light source, the integration time can be adjusted in steps of integer multiples of the period of the light source. This new AEC step system is called the banding filter, suggesting that the exposure time is not continuous but falls in some steps.

4.6.1.1 banding mode ON with AEC

In Banding ON mode, the exposure time will fall in steps of integer multiples of the period of light intensity. This design is to reject image flickering when the light source is not steady but periodical.

For a given light flickering frequency, the band step can be expressed in units of row period.

Band Step = 'period of light intensity' × 'frame rate' × 'rows per frame'.

The band steps for 50Hz and 60Hz light sources can be set in registers {0x3A08[1:0], 0x3A09[7:0]} and {0x3A0A[1:0], 0x3A0B[7:0]}, respectively.

When auto-banding is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If auto banding is disabled, the minimum integration time is one band step. Auto banding can be set in register bit 0x3A00[5].

4.6.1.2 banding mode OFF with AEC

When banding mode is OFF, integration time increases/decreases as normal. It is not necessarily multiples of band steps.

4.6.1.3 night mode

The OV5645 supports long integration time such as 1 frame, 2 frames, 3 frames, 4 frames, 5 frames, 6 frames, 7 frames, and 8 frames in dark conditions.This is achieved by slowing down the original frame rate and waiting for exposure. Night mode ceiling can be set in register bits {0x3A02[7:0], 0x3A03[7:0], 0x3A14[7:0], 0x3A15[7:0]}. Night mode can be disabled by setting register bit 0x3A00[2] to 0. Also, when in night mode, the increase and decrease step can be based on band or frames, depending on register 0x3A05[6]. The minimum increase/decrease step can be one band. The step can be based both on bands and frames.

4.6.2 manual exposure control

To manually change exposure value, you must first set both 0x3503[0], where 0x3503[0] enables manual exposure control. In auto exposure mode, the extra exposure values (larger than 1 frame) in registers 0x350C/0x350D automatically change. In manual exposure mode, these registers will not automatically change. The manually set

exposure in registers 0x3500~0x3502 must be less than the maximum exposure value in {0x380E, 0x380F} + {0x350C,0x350D}. The exposure value in registers 0x3500~0x3502 is in units of line*16 - the low 4 bits (0x3502[3:0]) is the fraction of line, the maximum value in {0x380E + 0x380F} + {0x350C, 0x350D} is in unit of line. If the manually set exposure value is less than one pre-defined frame period (e.g., 1/15 second in 15fps), there is no need to change 0x380E/0x380F. If the exposure value needs to be set beyond the pre-defined frame period; in other words, if the frame period needs to be extended to extend exposure time, then the maximum frame value in 0x380E/0x380F needs to be set first, then the exposure can be set in registers 0x3500~0x3502 accordingly.

4.6.3 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise. Thus, AGC usually starts after AEC is full. However, in cases where adjacent AEC step changes are too large (>1/16), AGC steps should be inserted in between; otherwise, the integration time will keep switching between two adjacent steps and the image flickers.

4.6.3.1 integration time between 1~16 rows

When integration time is less than 16 rows, the changes between adjacent AEC steps are larger than 1/16, which may possibly make the image oscillate between two AEC levels; thus, some AGC steps are added in between.

4.6.3.2 gain insertion between AEC banding steps

When banding mode is ON, the integration time changes in step of the period of light intensity. For the first 16 band steps, since the exposure time change between adjacent steps is larger than 1/16, AGC steps are inserted to ensure image stability.

4.6.3.3 gain insertion between night mode steps

Between night mode steps (e.g., integration time = 1 frame and 2 frames), AGC steps are inserted to ensure no adjacent step change is larger than 1/16.

4.6.3.4 when AEC reaches maximum

When AEC reaches its maximum while the image is still too dark, the gain starts to increase until the new frame average falls into the stable range or AGC reaches its maximum. The AGC ceiling can be set in {0x3A18[9:8], 0x3A19[7:0]}.

4.6.4 manual gain control

To manually change gain, first set register bit 0x3503[1] to enable manual control, then change the values in 0x350A/0x350B for the manual gain. The OV5645 has a maximum of 64x gain.

4.7 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration. There are three main functions of the BLC:

- Combining two ADC data paths into one data path
- Adjusting all normal pixel values based on the values of the black levels
- Applying multiplication to all pixel values based on digital gain

Black level adjustments can be made with registers 0x4000 through 0x4013.

table 4-7 BLC control functions

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x89	RW	BLC Control 00 Bit[0]: BLC enable
0x4002	BLC CTRL02	0x45	RW	Bit[7]: Format change enable BLC update when format changes
0x4003	BLC CTRL03	0x08	RW	Bit[7]: BLC redo enable Write 1 into it will trigger a BLC redo N frames begin, N is 0x4003[5:0] Bit[6]: BLC freeze Bit[5:0]: Manual frame number
0x4005	BLC CTRL05	0x18	RW	Bit[1]: BLC always update 0: Normal freeze 1: BLC always update
0x4009	BLACK LEVEL	0x10	RW	Bit[7:0]: BLC black level target at 10-bit range

4.8 light frequency selection

The OV5645 can detect the light flickering frequency. When this function is enabled, the sensor can detect the light frequency and select the corresponding banding filter value. To remove banding, the banding filter should be turned on and the banding filter value should be set to the appropriate value.

table 4-8 light frequency registers

address	register name	default value	R/W	description
0x3C01	5060HZ_CTRL1	0x00	RW	Bit[7]: Band manual enable 0: Auto 1: Manual
0x3C00	5060HZ_CTRL2	0x00	RW	Bit[2]: Band value manual setting 0: 60 Hz light 1: 50 Hz light
0x3C0C	5060HZ_CTRLC	–	R	Bit[0]: Band50/60 0: 60 Hz light 1: 50 Hz light

4.9 digital gain

The OV5645 supports 1/2/4 digital gain. Normally, the gain is controlled automatically by the automatic gain control (AGC) block.

4.10 strobe flash and frame exposure

4.10.1 strobe flash control

The strobe signal is programmable. It supports both LED and Xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB interface. Flash modules are triggered by the rising edge by default or by the falling edge if the signal polarity is changed. It supports the following flashlight modes (see **table 4-9**).

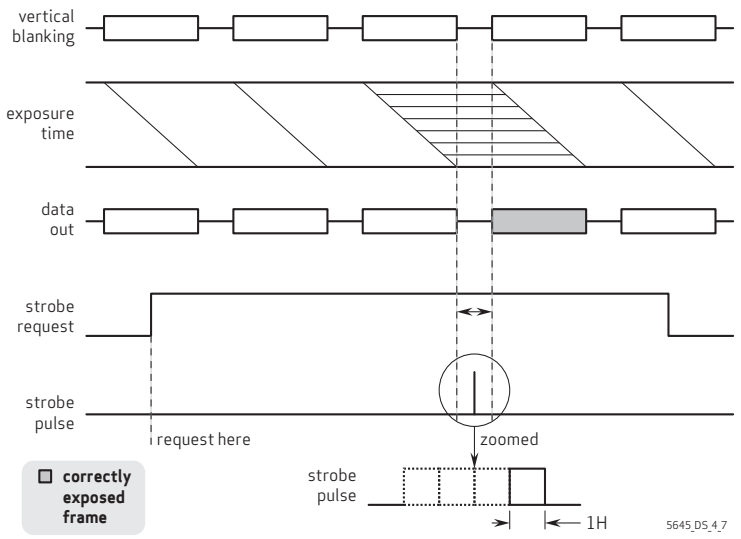
table 4-9 flashlight modes

mode	output	AEC / AGC	AWB
xenon	one-pulse	no	no
LED 1	pulse	no	no
LED 2	pulse	no	yes
LED 3	continuous	yes	yes

4.10.1.1 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see **figure 4-7**). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H, depending on register 0x3B00[3:2], where H is one row period.

figure 4-7 xenon flash mode



4.10.1.2 LED 1 & 2 mode

Two frames after the strobe request is submitted, the third frame is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set correctly (see **figure 4-8**). If end request is not sent, the strobe signal is activated intermittently until the strobe end request is set (see **figure 4-9**). The number of skipped frames is programmable using registers {0x3A1C, 0x3A1D}.

figure 4-8 LED 1 & 2 mode - one pulse output

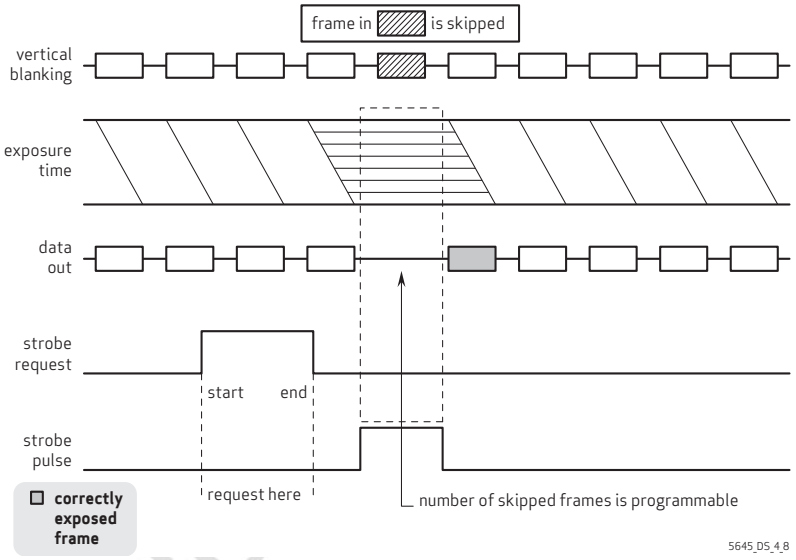
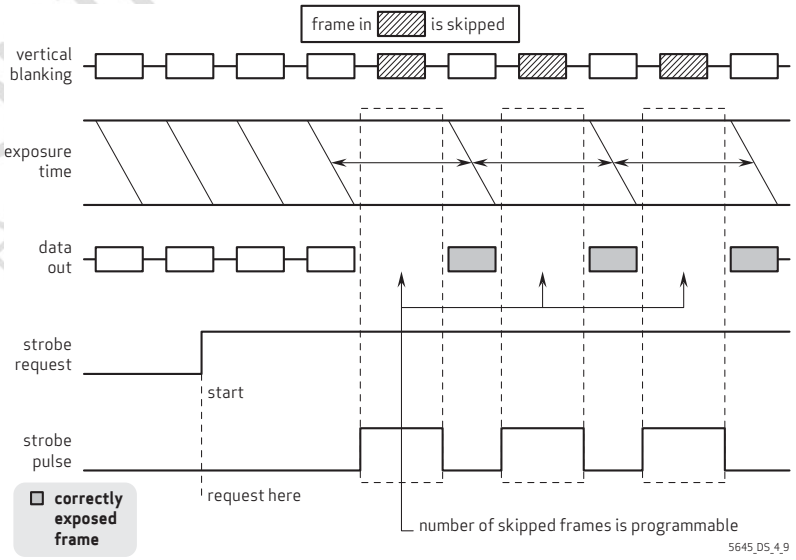


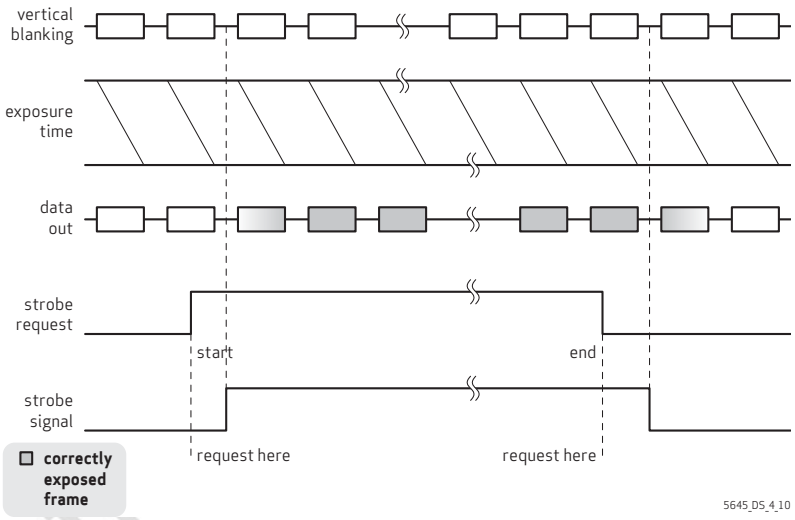
figure 4-9 LED 1 & 2 mode - multiple pulse output



4.10.1.3 LED 3 mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see **figure 4-10**).

figure 4-10 LED 3 mode



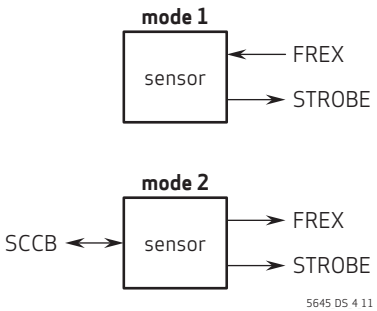
4.10.2 frame exposure (FREX) mode

In FREX mode, all pixels in the frame start integration at the same time, rather than integrating row by row. After a user-defined exposure time (either by external control in mode 1 or registers {0x3811, 0x3B04, 0x3B05} in mode 2), the mechanical shutter should be closed, preventing further integration, and then the image begins to read out. After the readout finishes, the shutter opens again and the sensor resumes normal mode, waiting for the next FREX request.

The OV5645 supports two modes of FREX (see **figure 4-11**):

- mode 1 - frame exposure and shutter control requests come from the external system via the FREX pin. The sensor will send a strobe output signal to control the flash light.
- mode 2 - frame exposure request comes from the external system via the SCCB register 0x3B08[0]. The sensor will output two signals, shutter control signal through the FREX pin and strobe signal through the STROBE pin.

figure 4-11 FREX modes



In mode 1, the FREX pin is configured as an input while it is configured as an output in mode 2. In both mode 1 and mode 2, the strobe output is irrelevant with the rolling strobe function. When in rolling shutter mode, the strobe function and this FREX/shutter control function do not work at the same time.

4.10.3 FREX strobe flash control

See **table 4-10** for FREX strobe control functions.

table 4-10 FREX strobe control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Strobe Control Bit[7]: Strobe request ON/OFF 0: OFF/BLC 1: ON Bit[6]: Strobe pulse reverse Bit[3:2]: width_in_xenon Bit[1:0]: Strobe mode 00: Xenon 01: LED 1 10: LED 2 11: LED 3
0x3B01	FREX EXPOSURE 02	0x00	RW	Bit[7:0]: FREX exposure time[23:16]
0x3B02	FREX SHUTTER DELAY 01	0x08	RW	Bit[4:0]: Shutter delay time[12:8]
0x3B03	FREX SHUTTER DELAY 00	0x00	RW	Bit[7:0]: Shutter delay time[7:0] Unit: 64x sclk cycle
0x3B04	FREX EXPOSURE 01	0x04	RW	Bit[7:0]: FREX exposure time[15:8]
0x3B05	FREX EXPOSURE 00	0x00	RW	Bit[7:0]: FREX exposure time[7:0] Unit: Tline
0x3B06	FREX CTRL 07	0x04	RW	Bit[7:4]: FREX frame delay Bit[3:0]: Strobe width[3:0]
0x3B07	FREX MODE	0x08	RW	Bit[1:0]: FREX mode selection 00: FREX strobe mode0 01: FREX strobe mode1 1x: Rolling strobe
0x3B08	FREX REQUEST	0x00	RW	FREX Request
0x3B09	FREX HREF DELAY	0x02	RW	FREX HREF Delay

table 4-10 FREX strobe control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B0A	FREX RST LENGTH	0x04	RW	Bit[2:0]: FREX precharge length 000: 1/16 Tline 001: 1/8 Tline 010: 1/4 Tline 011: 1/2 Tline 100: 1 Tline 101: 2 Tline 110: 4 Tline 111: 8 Tline
0x3B0B	STROBE WIDTH	0x00	RW	Bit[7:0]: Strobe width[19:12]
0x3B0C	STROBE WIDTH	0x3D	RW	Bit[7:0]: Strobe width[11:4]

4.11 one time programmable (OTP) memory

The OV5645 has a total of 256 bits (32 bytes) of embedded one time programmable (OTP) memory. It can be programmed through a normal SCCB write and read back through a normal SCCB read. The AVDD voltage range during OTP programming is 2.5V±5% and during OTP read, there is no such restriction.

The first 5 bytes (0x3D00~0x3D04) are reserved for OmniVision and the remaining 27 bytes (0x3D05~0x3D1F) can be used by users including module vendors.

table 4-11 OTP control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D20	OTP PROGRAM CTRL[a]	0x00	RW	Bit[7]: OTP program busy Bit[1]: OTP program speed 0: Fast 1: Slow Bit[0]: OTP program enable
0x3D21	OTP READ CTRL[a]	0x00	RW	Bit[7]: OTP read busy Bit[1]: OTP read speed 0: Fast 1: Slow Bit[0]: OTP read enable
0x3D00	OTP DATA00[b]	0x00	RW	OTP Dump/Load Data00
0x3D01	OTP DATA01[b]	0x00	RW	OTP Dump/Load Data01
0x3D02	OTP DATA02[b]	0x00	RW	OTP Dump/Load Data02
0x3D03	OTP DATA03[b]	0x00	RW	OTP Dump/Load Data03
0x3D04	OTP DATA04[b]	0x00	RW	OTP Dump/Load Data04

table 4-11 OTP control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D05	OTP DATA05	0x00	RW	OTP Dump/Load Data05
0x3D06	OTP DATA06	0x00	RW	OTP Dump/Load Data06
0x3D07	OTP DATA07	0x00	RW	OTP Dump/Load Data07
0x3D08	OTP DATA08	0x00	RW	OTP Dump/Load Data08
0x3D09	OTP DATA09	0x00	RW	OTP Dump/Load Data09
0x3D0A	OTP DATA0A	0x00	RW	OTP Dump/Load Data0a
0x3D0B	OTP DATA0B	0x00	RW	OTP Dump/Load Data0b
0x3D0C	OTP DATA0C	0x00	RW	OTP Dump/Load Data0c
0x3D0D	OTP DATA0D	0x00	RW	OTP Dump/Load Data0d
0x3D0E	OTP DATA0E	0x00	RW	OTP Dump/Load Data0e
0x3D0F	OTP DATA0F	0x00	RW	OTP Dump/Load Data0f
0x3D10	OTP DATA10	0x00	RW	OTP Dump/Load Data10
0x3D11	OTP DATA11	0x00	RW	OTP Dump/Load Data11
0x3D12	OTP DATA12	0x00	RW	OTP Dump/Load Data12
0x3D13	OTP DATA13	0x00	RW	OTP Dump/Load Data13
0x3D14	OTP DATA14	0x00	RW	OTP Dump/Load Data14
0x3D15	OTP DATA15	0x00	RW	OTP Dump/Load Data15
0x3D16	OTP DATA16	0x00	RW	OTP Dump/Load Data16
0x3D17	OTP DATA17	0x00	RW	OTP Dump/Load Data17
0x3D18	OTP DATA18	0x00	RW	OTP Dump/Load Data18
0x3D19	OTP DATA19	0x00	RW	OTP Dump/Load Data19
0x3D1A	OTP DATA1A	0x00	RW	OTP Dump/Load Data1a
0x3D1B	OTP DATA1B	0x00	RW	OTP Dump/Load Data1b
0x3D1C	OTP DATA1C	0x00	RW	OTP Dump/Load Data1c
0x3D1D	OTP DATA1D	0x00	RW	OTP Dump/Load Data1d
0x3D1E	OTP DATA1E	0x00	RW	OTP Dump/Load Data1e
0x3D1F	OTP DATA1F	0x00	RW	OTP Dump/Load Data1f

a. AVDD must be 2.1V ± 5% when writing/programming OTP, otherwise there will be reliability issues. There is no such limitation when reading OTP under normal operating conditions.

b. 0x3D00~0x3D04 are reserved for OmniVision internal use only

The following sections provide instructions on how to program the OTP (can only be done once) and how to read back the OTP (can be done multiple times). Before read/write, make sure all sensor powers are properly provided and the sensor is up and running. The OTP module is at default enabled state, 0x3000[4] is 0 and 0x3004[4] is 1.

4.11.1 OTP program

An example of programming OTP addresses 0x3D0C~0x3D0F is shown below. Make sure non-programmable memory addresses, 0x3D00~0x3D0B, are at default value of 0 to avoid accidental programming to other OTP addresses.

```
78 3D20 00
78 3D21 00
78 3D0C 20
78 3D0D 41
78 3D0E 41
78 3D0F 11

78 3D20 01 // program the above 4 byte data
#delay 10ms
78 3D20 00
```

Note that the procedure shown above can only be performed once for each sensor.

4.11.2 OTP read

After programming and at any time after the sensor is powered on, use the procedure shown below to read back the OTP values. Before each read, the user can clear 0x3D00~0x3D1F registers first if just finished write.

```
//OTP Read
78 3D20 00
78 3D21 00
78 3D21 01 //Load data to registers
#delay 1ms
79 3D0C ; read back OTP data
79 3D0D ; read back OTP data
79 3D0E ; read back OTP data
79 3D0F ; read back OTP data
#delay 10ms
78 3D21 00
```

5 image sensor processor digital functions

5.1 ISP general controls

The ISP module provides lens correction, gamma, de-noise, sharpen, auto focus, etc. These functions are enabled by registers 0x5000 ~ 0x5005.

table 5-1 ISP general control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	ISP Control 00 Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[5]: RAW gamma enable 0: Disable 1: Enable Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Color interpolation (CIP) enable 0: Disable 1: Enable
0x5001	ISP CONTROL 01	0x01	RW	ISP Control 01 Bit[7]: Special Digital Effects (SDE) enable 0: Disable 1: Enable Bit[5]: Scaling enable 0: Disable 1: Enable Bit[2]: UV average enable 0: Disable 1: Enable Bit[1]: Color matrix enable 0: Disable 1: Enable Bit[0]: Auto white balance (AWB) enable 0: Disable 1: Enable

table 5-1 ISP general control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5003	ISP CONTROL 03	0x08	RW	ISP Control 03 Bit[2]: Bin enable 0: Disable 1: Enable Bit[1]: Draw window for AFC enable 0: Disable 1: Enable Bit[0]: Solarize enable 0: Disable 1: Enable
0x5005	ISP CONTROL 05	0x36	RW	ISP Control 05 Bit[6]: AWB bias manual enable 0: Disable 1: Enable Bit[5]: AWB bias on enable 0: Disable 1: Enable Bit[4]: AWB bias plus enable 0: Disable 1: Enable Bit[2]: LENC bias on enable 0: Disable 1: Enable Bit[1]: GMA bias on enable 0: Disable 1: Enable Bit[0]: LENC bias manual enable 0: Disable 1: Enable
0x501E	ISP MISC	0x00	RW	Bit[6]: Scale ratio manual enable

table 5-1 ISP general control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5020	DITHER CTRL 0	0x00	RW	RGB Dither Control Bit[6]: Dither register control selection enable 0: From register control 1: From system control Bit[5:4]: R channel register control when 0x501E[6] = 0 00: Not allowed 01: RGB444 10: RGB565/555 11: Not allowed Bit[3:2]: G channel register control when 0x501E[6] = 0 00: Not allowed 01: RGB444 10: RGB565/555 11: Not allowed Bit[1:0]: B channel register control when 0x501E[6] = 0 00: Not allowed 01: RGB444 10: RGB565/555 11: Not allowed

5.2 lens correction (LENC)

The lens correction (LENC) algorithm compensates for the illumination drop off in the corners due to the lens. Based on the radius of each pixel to the lens, the algorithm calculates a gain for each pixel and then corrects each pixel with the calculated gain to compensate for the light distribution due to the lens curvature. The LENC calculation is based on sensor gain and therefore automatically adjusts with sensor gain. Also, the LENC supports the subsample function in both horizontal and vertical directions. Contact your local OmniVision FAE for lens correction settings (registers 0x5800~0x5849).

table 5-2 LENC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable
0x583E	MAX GAIN	0x40	R/W	Bit[7:0]: Maximum gain
0x583F	MIN GAIN	0x20	R/W	Bit[7:0]: Minimum gain
0x5840	MIN Q	0x18	R/W	Bit[6:0]: Minimum Q
0x5841	LENC CTRL59	0x0D	R/W	Bit[3]: Add BLC enable 0: Disable BLC add back function 1: Enable BLC add back function Bit[2]: BLC enable 0: Disable BLC function 1: Enable BLC function Bit[1]: Gain manual enable Bit[0]: Auto Q enable 0: Used constant Q (0x40) 1: Used calculated Q
0x5842	BR HSCALE	0x01	RW	Bit[2:0]: br h scale[10:8] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5843	BR HSCAL	0x2B	RW	Bit[7:0]: br h scale[7:0] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block

table 5-2 LENC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5844	BR VSCALE	0x01	RW	Bit[2:0]: br v scale[10:8] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5845	BR VSCALE	0x8D	RW	Bit[7:0]: br v scale[7:0] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5846	G HSCALE	0x01	RW	Bit[2:0]: g h scale[10:8] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5847	G HSCAL	0x8F	RW	Bit[7:0]: g h scale[7:0] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5848	G VSCALE	0x01	RW	Bit[2:0]: g v scale[10:8] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5849	G VSCALE	0x09	RW	Bit[7:0]: g v scale[7:0] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block

5.3 auto white balance (AWB)

The purpose of the auto white balance (AWB) block is to avoid unrealistic colors so that objects that appear white to the human eye are rendered white in the final image or video. This image sensor supports manual white balance and both simple and advanced auto white balance. Advanced AWB takes into account the *color temperature* of a light source. For advanced AWB settings, contact your local OmniVision FAE.

table 5-3 AWB control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x01	RW	Bit[0]: Auto white balance enable 0: Disable 1: Enable
0x5181	AWB CONTROL 01	0x58	RW	Bit[7:6]: Step local Bit[5:4]: Step fast Bit[3]: Slop 8x Bit[2]: Slop 4x Bit[1]: One zone Bit[0]: AVG all
0x5182	AWB CONTROL 02	0x11	RW	Bit[7:4]: Maximum local counter Bit[3:0]: Maximum fast counter
0x5183	AWB CONTROL 03	0x90	RW	Bit[7]: AWB simple enable 0: AWB advance 1: AWB simple Bit[6]: YUV enable 1: Simple YUV enable Bit[5]: AWB preset Bit[4]: AWB simf Bit[3:2]: AWB win
0x5184	AWB CONTROL 04	0x25	RW	Bit[7:6]: Counter area selection Bit[5]: G enable Bit[4:2]: Counter limit control Bit[1:0]: Counter threshold
0x5185	AWB CONTROL 05	0x24	RW	Bit[7:4]: Stable range unstable Threshold for unstable to stable change Bit[3:0]: Stable range stable Threshold for stable to un-stable change
0x5186~ 0x5190	AWB CONTROL	–	–	Advanced AWB Control Registers
0x5191	AWB CONTROL 17	0xFF	RW	Bit[7:0]: AWB top limit
0x5192	AWB CONTROL 18	0x00	RW	Bit[7:0]: AWB bottom limit
0x5193	AWB CONTROL 19	0xF0	RW	Bit[7:0]: Red limit
0x5194	AWB CONTROL 20	0xF0	RW	Bit[7:0]: Green limit

table 5-3 AWB control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5195	AWB CONTROL 21	0xF0	RW	Bit[7:0]: Blue limit
0x5196	AWB CONTROL 22	0x03	RW	Bit[5]: AWB freeze Bit[3:2]: AWB simple selection 00: AWB simple from after AWB gain 01: AWB simple from after RAW GMA 10: AWB simple from after AWB gain 11: AWB simple from after RAW GMA Bit[1]: Fast enable Bit[0]: AWB bias stat
0x5197	AWB CONTROL 23	0x02	RW	Bit[7:0]: Local limit
0x519E	AWB CONTROL 30	0x00	RW	Bit[3]: Local limit select Bit[2]: Simple stable select
0x519F	AWB CURRENT R GAIN	–	R	Bit[3:0]: Current R setting[11:8]
0x51A0	AWB CURRENT R GAIN	–	R	Bit[7:0]: Current R setting[7:0]
0x51A1	AWB CURRENT G GAIN	–	R	Bit[3:0]: Current G setting[11:8]
0x51A2	AWB CURRENT G GAIN	–	R	Bit[7:0]: Current G setting[7:0]
0x51A3	AWB CURRENT B GAIN	–	R	Bit[3:0]: Current B setting[11:8]
0x51A4	AWB CURRENT B GAIN	–	R	Bit[7:0]: Current B setting[7:0]
0x51A5	AWB AVERAGE R	–	R	Bit[7:0]: Average R[9:2]
0x51A6	AWB AVERAGE G	–	R	Bit[7:0]: Average G[9:2]
0x51A7	AWB AVERAGE B	–	R	Bit[7:0]: Average B[9:2]
0x51D0	AWB CONTROL74	–	R	Bit[5]: R large Bit[4]: G large Bit[3]: B large Bit[2:1]: Current type

5.4 raw gamma

Gamma correction converts the linear response data of the image sensor to compensate for properties of human vision. It maximizes the use of digital data relative to how humans perceive light and color. Higher gain is added at low light levels and lower gain at higher light levels. This non-linear function can be described by the power function, whose exponent value is called gamma. This module is designed to implement the gamma curve correction in piece-wise linear segments. Gamma is done in the RAW domain.

table 5-4 raw gamma control registers

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	Bit[5]: Raw gamma enable 0: Disable GMA 1: Enable GMA
0x5001	ISP CONTROL 01	0x01	RW	Bit[7]: Special digital effect enable 0: Disable 1: Enable
0x5481	GAMMA YST00	0x26	RW	Bit[7:0]: Y yst 00
0x5482	GAMMA YST01	0x35	RW	Bit[7:0]: Y yst 01
0x5483	GAMMA YST02	0x48	RW	Bit[7:0]: Y yst 02
0x5484	GAMMA YST03	0x57	RW	Bit[7:0]: Y yst 03
0x5485	GAMMA YST04	0x63	RW	Bit[7:0]: Y yst 04
0x5486	GAMMA YST05	0x6E	RW	Bit[7:0]: Y yst 05
0x5487	GAMMA YST06	0x77	RW	Bit[7:0]: Y yst 06
0x5488	GAMMA YST07	0x80	RW	Bit[7:0]: Y yst 07
0x5489	GAMMA YST08	0x88	RW	Bit[7:0]: Y yst 08
0x548A	GAMMA YST09	0x96	RW	Bit[7:0]: Y yst 09
0x548B	GAMMA YST0A	0xA3	RW	Bit[7:0]: Y yst 0A
0x548C	GAMMA YST0B	0xAF	RW	Bit[7:0]: Y yst 0B
0x548D	GAMMA YST0C	0xC5	RW	Bit[7:0]: Y yst 0C
0x548E	GAMMA YST0D	0xD7	RW	Bit[7:0]: Y yst 0D
0x548F	GAMMA YST0E	0xE8	RW	Bit[7:0]: Y yst 0E
0x5490	GAMMA YST0F	0x0F	RW	Bit[7:0]: Y yst 0F

5.5 defect pixel cancellation (DPC)

Primarily due to process anomalies, pixel defects in the sensor array will occur, generating incorrect pixel levels and color values. The purpose of the defect pixel cancellation (DPC) is to remove the effects caused by defective pixels. To correctly remove defective pixels, the proper threshold should first be determined. Additionally, there are special functions available for those pixels located at the image boundary.

table 5-5 DPC control register

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable

5.6 color interpolation (CIP)

The CIP functions include de-noising of raw images, RAW to RGB interpolation, and edge enhancement. In sensor RAW format, each pixel will be either R, G or B. CIP will calculate the other two color values using neighboring pixel. Thus, we get the full RGB information for each pixel. For edge enhancement, the OV5645 provides both manual and auto modes.

table 5-6 CIP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	Bit[0]: Color interpolation enable 0: Disable 1: Enable
0x5301	CIP SHARPENMT THRESHOLD 2	0x48	RW	Color Interpolation Sharpen MT Threshold 2
0x5302	CIP SHARPENMT OFFSET1	0x18	RW	CIP Sharpen MT Offset1 (Y edge mt manual setting when 0x5308[6]=1)
0x5303	CIP SHARPENMT OFFSET2	0x0E	RW	CIP Sharpen MT Offset2
0x5304	CIP DNS THRESHOLD 1	0x08	RW	CIP DNS Threshold 1
0x5305	CIP DNS THRESHOLD 2	0x48	RW	CIP DNS Threshold 2

table 5-6 CIP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5306	CIP DNS OFFSET1	0x09	RW	CIP DNS Offset1 (DNS threshold manual setting when 0x5308[4]=1)
0x5307	CIP DNS OFFSET2	0x16	RW	CIP DNS Offset2
0x5308	CIP CTRL	0x25	RW	Bit[6]: CIP edge MT manual enable Bit[4]: CIP DNS manual enable Bit[2:0]: CIP threshold for BR sharpen
0x5309	CIP SHARPENTH THRESHOLD 1	0x08	RW	CIP Sharpen TH Threshold 1
0x530A	CIP SHARPENTH THRESHOLD 2	0x48	RW	CIP Sharpen TH Threshold 2
0x530B	CIP SHARPENTH OFFSET1	0x04	RW	CIP Sharpen TH Offset1 (Sharpen threshold manual setting when 0x5308[6]=1)
0x530C	CIP SHARPENTH OFFSET2	0x06	RW	CIP Sharpen TH Offset2
0x530D	CIP EDGE MT AUTO	–	R	CIP Edge MT Auto Read
0x530E	CIP DNS THRESHOLD AUTO	–	R	CIP DNS Threshold Auto Read
0x530F	CIP SHARPEN THRESHOLD AUTO	–	R	CIP Sharpen Threshold Auto Read

5.7 color matrix (CMX)

The main purpose of the Color Matrix (CMX) function is to cancel out crosstalk and convert color space. Given the color correction matrix, CCM, and RGB to YUV conversion matrix, RGB2YUV, the combined matrix is:

$$CMX = \begin{bmatrix} cmx00 & cmx01 & cmx02 \\ cmx10 & cmx11 & cmx12 \\ cmx20 & cmx21 & cmx22 \end{bmatrix} = RGB2YUV \times CCM \times \begin{bmatrix} 1 & -0.25 & 0.75 \\ 1 & -0.25 & -0.25 \\ 1 & 0.75 & -0.25 \end{bmatrix}$$

$$\text{where } \begin{bmatrix} R \\ G \\ B \end{bmatrix} = CCM \begin{bmatrix} R_0 \\ G_0 \\ B_0 \end{bmatrix}$$

The CMX is then normalized by $2^{0x5394[3:0]}$.

table 5-7 CMX control registers

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x01	RW	Bit[1]: Color matrix enable 0: Disable 1: Enable
0x5380	CMX CTRL	0x00	RW	Bit[1]: CMX precision switch 0: 1.7 mode 1: 2.6 mode
0x5381	CMX1	0x20	RW	Bit[1]: CMX1 for Y
0x5382	CMX2	0x64	RW	Bit[7:0]: CMX2 for Y
0x5383	CMX3	0x08	RW	Bit[7:0]: CMX3 for Y
0x5384	CMX4	0x30	RW	Bit[7:0]: CMX4 for U
0x5385	CMX5	0x90	RW	Bit[7:0]: CMX5 for U
0x5386	CMX6	0xC0	RW	Bit[7:0]: CMX6 for U
0x5387	CMX7	0xA0	RW	Bit[7:0]: CMX7 for V
0x5388	CMX8	0x98	RW	Bit[7:0]: CMX8 for V
0x5389	CMX9	0x08	RW	Bit[7:0]: CMX9 for V
0x538A	CMXSIGN	0x01	RW	Cmxsign Bit[0]: CMX9 sign
0x538B	CMXSIGN	0x98	RW	Cmxsign Bit[7]: CMX8 sign Bit[6]: CMX7 sign Bit[5]: CMX6 sign Bit[4]: CMX5 sign Bit[3]: CMX4 sign Bit[2]: CMX3 sign Bit[1]: CMX2 sign Bit[0]: CMX1 sign

5.8 UV average

The main function of the UV average is to average the U/V channel value using special filters.

table 5-8 UV average register

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x4F	RW	Bit[2]: UV average enable 0: Disable 1: Enable

5.9 scaling

The main purpose of the scaling function is to zoom out the image. According to the new width and new height of the new image, the module uses the values of several pixels to generate the values of one pixel. The values of some pixels are divided and used in two or more adjacent pixels. The scaling function supports up to 32x scale.

table 5-9 UV average register

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x01	RW	Bit[5]: Scale enable 0: Disable 1: Enable
0x5601	SCALE CTRL 1	0x00	RW	Bit[6:4]: HDIV RW DCW scale times 000: DCW 1 time 001: DCW 2 time 010: DCW 4 time 100: DCW 8 time 101: DCW 16 time Others: DCW 16 time Bit[2:0]: VDIV RW DCW scale times 000: DCW 1 time 001: DCW 2 time 010: DCW 4 time 100: DCW 8 time 101: DCW 16 time Others: DCW 16 time
0x5602	SCALE CTRL 2	0x02	RW	XSC High Bits
0x5603	SCALE CTRL 3	0x00	RW	XSC Low Bits
0x5604	SCALE CTRL 4	0x02	RW	YSC High Bits
0x5605	SCALE CTRL 5	0x00	RW	YSC Low Bits
0x5606	SCALE CTRL 6	0x00	RW	Bit[3:0]: Voffset

5.10 UV adjust

The main function of the UV adjust is to adjust the U/V channel value according to sensor gain. It supports both manual and auto modes.

The UV adjust function is integrated in SDE. The main function of the UV adjust is to adjust the U/V channel value according to sensor gain. It supports both manual and auto modes

5.10.1 manual mode

By setting SDE CTRL 0[1] (0x5580) to 1 and SDE CTRL 8[6] (0x5588) to 1, UV adjust is controlled only by register SAT U[7:0] (0x5583) and SAT V[7:0] (0x5584) for U and V gains, respectively.

5.10.2 auto mode

When the UV adjust is set for auto mode (0x5580[1]=1 and 0x5588[6]=0), the UV adjust curve parameters (see **figure 5-1**) should be entered into the corresponding registers. The UV adjust parameters, UV adj th1, UV adj th2, and offset low, offset high should be entered into the registers to set the curve. To get these values, first set the values of UV adj th1, UV adj th2, offset low and offset high. Then, calculate the values of a and k as follows:

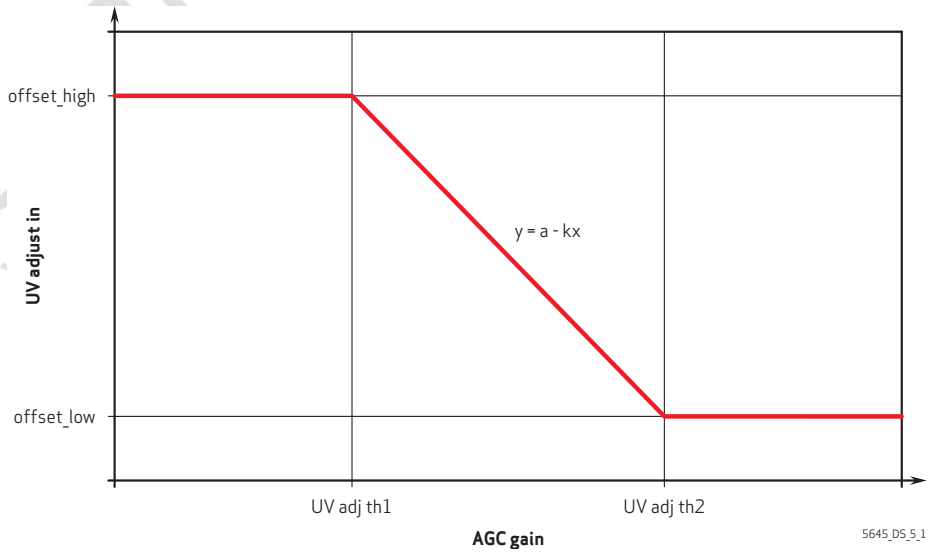
k = (offset high - offset low) / (UV adj th2 - UV adj th1)

a = offset high + (offset high - offset low)/(UV adj th2 - UV adj th1)

Registers to be changed:

- UV adj th1[8:0] = registers 0x5589[7:0]
- UV adj th2[8:0] = registers {0x558A[0], 0x558B[7:0]}
- offset high = register 0x5583[7:0] (when 0x5580[1]=1 and 0x5588[6]=0)
- offset low = register 0x5584[7:0] (when 0x5580[1]=1 and 0x5588[6]=0)

figure 5-1 UV adjust graph



5.11 special digital effects (SDE)

The special digital effects (SDE) functions include hue/saturation control, brightness, and contrast. SDE also supports negative, black/white, sepia, greenish, blueish, redish, solarize and other image effects.

table 5-10 SDE control registers

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x01	RW	Bit[7]: Special digital effect enable 0: Disable 1: Enable
0x5581	SDE CTRL1	0x80	RW	Bit[7:0]: Hue cos coefficient
0x5582	SDE CTRL2	0x00	RW	Bit[7:0]: Hue sin coefficient
0x5583	SDE CTRL3	0x40	RW	Bit[7:0]: Saturation U when 0x5580[1]=1 and 0x5588[6]=1, max value for UV adjust when 0x5580[1]=1 and 0x5588[6]=0; or fixed U when 0x5580[3]=1
0x5584	SDE CTRL4	0x40	RW	Bit[7:0]: Saturation V when 0x5580[1]=1 and 0x5588[6]=1, min value for UV adjust when 0x5580[1]=1 and 0x5588[6]=0; or Vreg when 0x5580[4]=1
0x5585	SDE CTRL5	0x00	RW	Bit[7:0]: Yoffset for contrast when 0x5044[3]=1; or fixed Y when 0x5580[7]=1
0x5586	SDE CTRL6	0x20	RW	Bit[7:0]: Y gain for contrast
0x5587	SDE CTRL7	0x00	RW	Bit[7:0]: Y bright for contrast
0x5588	SDE CTRL8	0x01	RW	Bit[6]: UV adjust manual enable Bit[5]: Sign5 for hue V, cos Bit[4]: Sign4 for hue U, cos Bit[3]: Sign3 Y bright sign for contrast 0: Keep Y bright sign 1: Negative Y bright sign Bit[2]: Sign2 Y offset sign for contrast when 0x5044[3]=1 0: Keep Y offset sign 1: Negative Y offset sign Bit[1]: Sign1 for hue V, sin Bit[0]: Sign0 for hue U, sin
0x5589	SDE CTRL9	0x01	RW	Bit[7:0]: UV adjust threshold 1 Valid when 0x5580[1]=1
0x558A	SDE CTRL10	0x01	RW	Bit[0]: UV adjust threshold 2[8] Valid when 0x5580[1]=1
0x558B	SDE CTRL11	0xFF	RW	Bit[7:0]: UV adjust threshold 2[7:0] Valid when 0x5580[1]=1
0x558C	SDE CTRL12	–	R	Bit[7:0]: UV adjust value read out

5.12 ISP format

table 5-11 ISP format control registers

address	register name	default value	R/W	description
0x501F	FORMAT MUX CONTROL	0x00	RW	Format MUX Control Bit[2:0]: Format selection 000: ISP YUV422 001: ISP RGB 010: ISP dither 011: ISP RAW (DPC) 100: SNR RAW 101: ISP RAW (CIP)

5.13 draw window

The draw window module is used to display a window on top of live video. It is usually used by autofocus to display a focus window.

table 5-12 draw window registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5003	ISP CONTROL 03	0x08	RW	Bit[1]: Draw window for AFC enable 0: Disable 1: Enable
0x501F	FORMAT MUX CONTROL	0x00	RW	Bit[2:0]: Format select 000: ISP YUV422 001: ISP RGB 010: ISP dither 011: ISP RAW (DPC) 100: SNR RAW 101: ISP RAW (CIP)
0x5027	DRAW WINDOW CONTROL 00	0x02	RW	Bit[0]: Draw window control 0: No fixed Y 1: Fixed Y
0x5028	DRAW WINDOW LEFT POSITION CONTROL	0x04	RW	Bit[3:0]: Draw window left[11:8]
0x5029	DRAW WINDOW LEFT POSITION CONTROL	0x90	RW	Bit[7:0]: Draw window left[7:0]
0x502A	DRAW WINDOW RIGHT POSITION CONTROL	0x05	RW	Bit[3:0]: Draw window right[11:8]

table 5-12 draw window registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x502B	DRAW WINDOW RIGHT POSITION CONTROL	0x90	RW	Bit[7:0]: Draw window right[7:0]
0x502C	DRAW WINDOW TOP POSITION CONTROL	0x03	RW	Bit[2:0]: Draw window top[10:8]
0x502D	DRAW WINDOW TOP POSITION CONTROL	0x6C	RW	Bit[7:0]: Draw window top[7:0]
0x502E	DRAW WINDOW BOTTOM POSITION CONTROL	0x04	RW	Bit[2:0]: Draw window bottom[10:8]
0x502F	DRAW WINDOW BOTTOM POSITION CONTROL	0x2C	RW	Bit[7:0]: Draw window bottom[7:0]
0x5030	DRAW WINDOW HORIZONTAL BOUNDARY WIDTH CONTROL	0x00	RW	Bit[3:0]: Draw window horizontal boundary width[11:8]
0x5031	DRAW WINDOW HORIZONTAL BOUNDARY WIDTH CONTROL	0x14	RW	Bit[7:0]: Draw window horizontal boundary width[7:0]
0x5032	DRAW WINDOW VERTICAL BOUNDARY WIDTH CONTROL	0x00	RW	Bit[2:0]: Draw window vertical boundary width[10:8]
0x5033	DRAW WINDOW VERTICAL BOUNDARY WIDTH CONTROL	0x14	RW	Bit[7:0]: Draw window vertical boundary width[7:0]
0x5034	DRAW WINDOW Y CONTROL	0x80	RW	Bit[7:0]: Fixed Y for draw window
0x5035	DRAW WINDOW U CONTROL	0x2A	RW	Bit[7:0]: Fixed U for draw window
0x5036	DRAW WINDOW V CONTROL	0x14	RW	Bit[7:0]: Fixed V for draw window

6 image sensor output interface digital functions

6.1 system control

System control registers include clock, reset control, and PLL configure. Individual modules can be reset or clock gated by setting the appropriate registers.

table 6-1 system control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3000	SYSTEM RESET00	0x30	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset BIST Bit[6]: Reset MCU program memory Bit[5]: Reset MCU Bit[4]: Reset OTP Bit[3]: Reset STB Bit[2]: Reset D5060 Bit[1]: Reset timing control Bit[0]: Reset array control
0x3001	SYSTEM RESET01	0x08	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset AWB registers Bit[6]: Reset AFC Bit[5]: Reset ISP Bit[4]: Reset FC Bit[3]: Reset S2P Bit[2]: Reset BLC Bit[1]: Reset AEC registers Bit[0]: Reset AEC
0x3002	SYSTEM RESET02	0x1C	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset VFIFO Bit[5]: Reset format Bit[1]: Reset format MUX Bit[0]: Reset average
0x3003	SYSTEM RESET03	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[5]: Reset digital gain compensation Bit[4]: Reset SYNC FIFO Bit[3]: Reset PSRAM Bit[2]: Reset ISP FC Bit[1]: Reset MIPI Bit[0]: Reset SPI_RX

table 6-1 system control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3004	CLOCK ENABLE00	0xCF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable BIST clock Bit[6]: Enable MCU program memory clock Bit[5]: Enable MCU clock Bit[4]: Enable OTP clock Bit[3]: Enable STROBE clock Bit[2]: Enable D5060 clock Bit[1]: Enable timing control clock Bit[0]: Enable array control clock
0x3005	CLOCK ENABLE01	0xF7	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable AWB register clock Bit[6]: Enable AFC clock Bit[5]: Enable ISP clock Bit[4]: Enable FC clock Bit[3]: Enable S2P clock Bit[2]: Enable BLC clock Bit[1]: Enable AEC register clock Bit[0]: Enable AEC clock
0x3006	CLOCK ENABLE02	0xE3	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable PSRAM clock Bit[6]: Enable FMT clock Bit[1]: Enable format MUX clock Bit[0]: Enable average clock
0x3007	CLOCK ENABLE03	0xFF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable digital gain compensation clock Bit[6]: Enable SYNC FIFO clock Bit[5]: Enable ISPFC SCLK clock Bit[4]: Enable MIPI PCLK clock Bit[3]: Enable MIPI clock Bit[2]: Enable SPI_RX SCLK clock Bit[1]: Enable VFIFO PCLK clock Bit[0]: Enable VFIFO SCLK clock
0x3008	SYSTEM CTROL0	0x02	RW	System Control Bit[7]: Software reset Bit[6]: Software power down
0x3034	SC PLL CONTRL0	0x1A	RW	Bit[6:4]: PLL charge pump control Bit[3:0]: MIPI bit mode 0x8: 8-bit mode 0xA: 10-bit mode

table 6-1 system control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3035	SC PLL CONTRL1	0x11	RW	Bit[7:4]: System clock divider Slow down all clocks Bit[3:0]: Scale divider for MIPI MIPI PCLK/SERCLK can be slowed down
0x3036	SC PLL CONTRL2	0x69	RW	Bit[7:0]: PLL multiplier (4~252) Can be any integer for 4~127 and only even integer for 128~252
0x3037	SC PLL CONTRL3	0x03	RW	Bit[4]: PLL root divider 0: Bypass 1: Divided by 2 Bit[3:0]: PLL pre-divider 1, 2, 3, 4, 6, 8
0x3039	SC PLL CONTRL 5	0x00	RW	Bit[7]: PLL bypass

6.2 microcontroller unit (MCU)

The MCU firmware can be downloaded by writing to registers starting from 0x8000. A total of 6 KB of program memory can be used for program storage. Before downloading the firmware, the user must enable the MCU clock by setting register 0x3000[5] to 1'b1. After downloading the firmware, set register 0x3000[5] to 1'b0 to enable the MCU. The MCU interrupts are triggered by several internal signals for firmware development.

table 6-2 MCU control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3F00	MC CTRL 00	0x00	RW	Bit[0]: MCU soft reset 1: Reset MCU
0x3F01	MC INTERRUPT MASK0	0x00	RW	Mask0 for Interrupt (0: disable interrupt bit; 1: enable interrupt bit) Bit[7]: JFIFO over flow Bit[6]: JFIFO end of image Bit[5]: ISP end of frame Bit[4]: ISP start of frame Bit[3]: AFC done Bit[2]: AWB done Bit[1]: VFIFO full Bit[0]: VFIFO empty
0x3F02	MC INTERRUPT MASK1	0x00	RW	Mask1 for Interrupt (0: disable interrupt bit; 1: enable interrupt bit) Bit[7]: AEC done Bit[6]: ISP average done Bit[5]: AEC trigger Bit[4]: JPG over size Bit[3]: SRM operation start Bit[2]: SRM operation done Bit[1]: DVP frame counter change Bit[0]: BLC start of frame
0x3F03	MC READ INTERRUPT ADDRESS	0x70	RW	Bit[7:0]: Set high byte for SCCB address that will trigger interrupt when read
0x3F04	MC READ INTERRUPT ADDRESS	0x00	RW	Bit[7:0]: Set low byte for SCCB address that will trigger interrupt when read
0x3F05	MC WRITE INTERRUPT ADDRESS	0x70	RW	Bit[7:0]: Set high byte for SCCB address that will trigger interrupt when written
0x3F06	MC WRITE INTERRUPT ADDRESS	0x04	RW	Bit[7:0]: Set low byte for SCCB address that will trigger interrupt when written

table 6-2 MCU control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3F0C	MC INTERRUPT0 STATUS	0x00	RW	Interrupt0 Status Indicator Bit[5]: ISP EOF Bit[4]: ISP SOF Bit[2]: AWB done Bit[1]: VFIFO full Bit[0]: VFIFO empty
0x3F0D	MC INTERRUPT1 STATUS	0x00	RW	Interrupt1 Status Indicator Bit[7]: AEC done Bit[6]: Average done Bit[5]: AEC trigger Bit[3]: MIPI turn around Bit[2]: MIPI low power contention detect Bit[0]: BLC SOF

6.3 frame control (FC)

Frame control (FC) is used to mask some specified frames by setting the appropriate registers.

table 6-3 FC control registers

address	register name	default value	R/W	description
0x4201	FRAME CONTROL 00	0x00	RW	Control Passed Frame Number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode Bit[3:0]: Frame ON number
0x4202	FRAME CONTROL 01	0x00	RW	Control Masked Frame Number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode Bit[3:0]: Frame OFF number

6.4 format description

Format control converts the internal data format into the desired output format including YUV, RGB, or RAW.

table 6-4 format control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x4300	FORMAT CONTROL 00	0xF8	RW	Format Control 00 Bit[7:4]: Output format of formatter module 0x0: RAW Bit[3:0]: Output sequence 0x0: BGBG... / GRGR... 0x1: GBGB... / RGRG... 0x2: GRGR... / BGBG... 0x3: RGRG... / GBGB... 0x4~0xF: Not allowed 0x1: Y8 Bit[3:0]: Does not matter 0x2: YUV444/RGB888 (not available for full resolution) Bit[3:0]: Output sequence 0x0: YUVYUV..., or GBRGBR... 0x1: YVUYVU..., or GRBGRB... 0x2: UYVUYV..., or BGRBGR... 0x3: VYUVYU..., or RGBRGB... 0x4: UVYUVY..., or BRGBRG... 0x5: VUYVUY..., or RBGRBG... 0x6~0xE: Not allowed 0xF: UYVUYV..., or BGRBGR... 0x3: YUV422 Bit[3:0]: Output sequence 0x0: YUYV... 0x1: YVYU... 0x2: UYVY... 0x3: VYUY... 0x4~0xE: Not allowed 0xF: UYVY... 0x4: YUV420 Bit[3:0]: Output sequence 0x0: YYYY... / YUYV... 0x1: YYYY... / YVYU... 0x2: YYYY... / UYVY... 0x3: YYYY... / VYUY... 0x4: YUYV... / YYYY...

table 6-4 format control registers (sheet 2 of 5)

address	register name	default value	R/W	description
				0x5: YVYU... / YYYY... 0x6: UYVY... / YYYY... 0x7: VYUY... / YYYY... 0x8~0xE: Not allowed 0xF: YYYY... / UYVY... 0x5: YUV420 (for MIPI only) Bit[3:0]: Output sequence 0x0~0xD: Not allowed 0xE: VYYVYY... / UYYUYY... 0xF: UYYUYY... / VYYVYY... 0x6: RGB565 Bit[3:0]: Output sequence 0x0: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x1: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x2: {g[4:0],r[5:3]}, {r[2:0],b[4:0]} 0x3: {b[4:0],r[5:3]}, {r[2:0],g[4:0]} 0x4: {g[4:0],b[5:3]}, {b[2:0],r[4:0]} 0x5: {r[4:0],b[5:3]}, {b[2:0],g[4:0]} 0x6~0xE: Not allowed 0xF: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} 0x7: RGB555 format 1 Bit[3:0]: Output sequence 0x0: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x1: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0]} 0x2: {g[4:0],r[4:2]}, {r[1:0],1'b0,b[4:0]} 0x3: {b[4:0],r[4:2]}, {r[1:0],1'b0,g[4:0]} 0x4: {r[4:0],b[4:2]}, {b[1:0],1'b0,g[4:0]} 0x5: {g[4:0],b[4:2]}, {b[1:0],1'b0,r[4:0]} 0x6~0xE: Not allowed 0xF: {g[1:0],1'b0,b[4:0]}, {r[4:0],g[4:2]} 0x8: RGB555 format 2 Bit[3:0]: Output sequence 0x0: {1'b0,b[4:0],g[4:3]}, {g[2:0],r[4:0]}

table 6-4 format control registers (sheet 3 of 5)

address	register name	default value	R/W	description
				0x1: {1'b0,r[4:0],g[4:2]}, {g[2:0],b[4:0]} 0x2: {1'b0,g[4:0],r[4:2]}, {r[2:0],b[4:0]} 0x3: {1'b0,b[4:0],r[4:2]}, {r[2:0],g[4:0]} 0x4: {1'b0,r[4:0],b[4:2]}, {b[2:0],g[4:0]} 0x5: {1'b0,g[4:0],b[4:2]}, {b[2:0],r[4:0]} 0x6: {b[4:0],1'b0,g[4:3]}, {g[2:0],r[4:0]} 0x7: {r[4:0],1'b0,g[4:2]}, {g[2:0],b[4:0]} 0x8: {g[4:0],1'b0,r[4:2]}, {r[2:0],b[4:0]} 0x9: {b[4:0],1'b0,r[4:2]}, {r[2:0],g[4:0]} 0xA: {r[4:0],1'b0,b[4:2]}, {b[2:0],g[4:0]} 0xB: {g[4:0],1'b0,b[4:2]}, {b[2:0],r[4:0]} 0xC~0xF: Not allowed
				0x9: RGB444 format 1 Bit[3:0]: Output sequence 0x0: {1'b0,b[3:0],2'h0,g[3]}, {g[2:0],1'b0,r[3:0]} 0x1: {1'b0,r[3:0],2'h0,g[3]}, {g[2:0],1'b0,b[3:0]} 0x2: {1'b0,g[3:0],2'h0,r[3]}, {r[2:0],1'b0,b[3:0]} 0x3: {1'b0,b[3:0],2'h0,r[3]}, {r[2:0],1'b0,g[3:0]} 0x4: {1'b0,r[3:0],2'h0,b[3]}, {b[2:0],1'b0,g[3:0]} 0x5: {1'b0,g[3:0],2'h0,b[3]}, {b[2:0],1'h0,r[3:0]} 0x6: {b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0} 0x7: {r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x8: {g[3:0],1'b0,r[3:1]}, {r[0],2'h0,b[3:0],1'b0} 0x9: {b[3:0],1'b0,r[3:1]}, {r[0],2'h0,g[3:0],1'b0} 0xA: {r[3:0],1'b0,b[3:1]}, {b[0],2'h0,g[3:0],1'b0} 0xB: {g[3:0],1'b0,b[3:1]}, {b[0],2'h0,r[3:0],1'b0} 0xC~0xE: Not allowed

table 6-4 format control registers (sheet 4 of 5)

address	register name	default value	R/W	description
				0xF: {g[0],2'h2,b[3:0],1'b1}, {r[3:0],1'b1,g[3:1]} 0xA: RGB444 format 2 Bit[3:0]: Output sequence 0x0: {4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x1: {4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x2: {4'b0,b[3:0]}, {r[3:0],g[3:0]} 0x3: {4'b0,r[3:0]}, {b[3:0],g[3:0]} 0x4: {4'b0,g[3:0]}, {b[3:0],r[3:0]} 0x5: {4'b0,g[3:0]}, {r[3:0],b[3:0]} 0x6: {b[3:0],g[3:0],2'h0}, {r[3:0],b[3:0],2'h0, g[3:0],r[3:0],2'h0} 0x7: {r[3:0],g[3:0],2'h0}, {b[3:0],r[3:0],2'h0, g[3:0],b[3:0],2'h0} 0x8: {b[3:0],r[3:0],2'h0}, {g[3:0],b[3:0],2'h0, r[3:0],g[3:0],2'h0} 0x9: {r[3:0],b[3:0],2'h0}, {g[3:0],r[3:0],2'h0, b[3:0],g[3:0],2'h0} 0xA: {g[3:0],b[3:0],2'h0}, {r[3:0],g[3:0],2'h0, b[3:0],r[3:0],2'h0} 0xB: {g[3:0],r[3:0],2'h0}, {b[3:0],g[3:0],2'h0, r[3:0],b[3:0],2'h0} 0xC~0xF: Not allowed 0xB~0xE: Not allowed 0xF: Bypass formatter module (not recommended) Bit[3:0]: Output format 0x8: Raw 0x9: YUV422 0xA: YUV444 0xE: VYYVYY.../UYYUYY 0xF: UYYUYY.../VYYVYY

table 6-4 format control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x4301	FORMAT CONTROL 01	0x00	RW	Format Control 01 Bit[1:0]: YUV422 UV control 00: U/V generated from average 01: U/V generated from first pixel 10: Not valid 11: U/V generated from second pixel
0x4302	YMAX VALUE	0x03	RW	Bit[1:0]: Y max clip value[9:8]
0x4303	YMAX VALUE	0xFF	RW	Bit[7:0]: Y max clip value[7:0]
0x4304	YMIN VALUE	0x00	RW	Bit[1:0]: Y min clip value[9:8]
0x4305	YMIN VALUE	0x00	RW	Bit[7:0]: Y min clip value[7:0]
0x4306	UMAX VALUE	0x03	RW	Bit[1:0]: U max clip value[9:8]
0x4307	UMAX VALUE	0xFF	RW	Bit[7:0]: U max clip value[7:0]
0x4308	UMIN VALUE	0x00	RW	Bit[1:0]: U min clip value[9:8]
0x4309	UMIN VALUE	0x00	RW	Bit[7:0]: U min clip value[7:0]
0x430A	VMAX VALUE	0x03	RW	Bit[1:0]: V max clip value[9:8]
0x430B	VMAX VALUE	0xFF	RW	Bit[7:0]: V max clip value[7:0]
0x430C	VMIN VALUE	0x00	RW	Bit[1:0]: V min clip value[9:8]
0x430D	VMIN VALUE	0x00	RW	Bit[7:0]: V min clip value[7:0]
0x4310	VSYNC_WIDTH	0x00	RW	Bit[7:0]: VSYNC width In terms of lines
0x4311	VSYNC_WIDTH H	0x04	RW	Bit[7:0]: VSYNC width[15:9] In terms of pixel numbers
0x4312	VSYNC WIDTH L	0x00	RW	Bit[7:0]: VSYNC width[7:0] In terms of pixel numbers
0x4313	VSYNC CTRL	0x00	RW	Bit[7:5]: Debug mode Bit[4]: VSYNC polarity Bit[3:2]: VSYNC output select Bit[1]: VSYNC mode 3 Bit[0]: VSYNC mode 2
0x4314	VSYNC DELAY1	0x00	RW	Bit[7:0]: VSYNC trigger to VSYNC delay[23:16]
0x4315	VSYNC DELAY2	0x00	RW	Bit[7:0]: VSYNC trigger to VSYNC delay[15:8]
0x4316	VSYNC DELAY3	0x00	RW	Bit[7:0]: VSYNC trigger to VSYNC delay[7:0]

6.5 mobile industry processor interface (MIPI)

The OV5645 provides one clock lane and two data lanes for the communications link between sensor (transmitter) and receiver in a mobile device. It follows MIPI specifications D-PHY 0.89 and above and CSI2-V1, and supports all mandatory MIPI features. Most of the optional features (e.g., LP transfer mode) are not supported unless otherwise specified in this specification. For any further questions, contact your local OmniVision FAE for more details.

table 6-5 MIPI transmitter registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Lane select 0: Use lane1 as default data lane 1: Use lane2 as default data lane Bit[2]: Idle status 0: MIPI bus will be LP00 when no packet to transmit 1: MIPI bus will be LP11 when no packet to transmit
0x4801	MIPI CTRL 01	0x0F	RW	MIPI Control 01 Bit[4]: PH bit order for ECC 0: {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]} Bit[3]: PH byte order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[2]: PH byte order2 for ECC 0: {DI,WC} 1: {WC,DI}
0x4805	MIPI CTRL 05	0x10	RW	Bit[7]: MIPI lane1 disable 1: Disable MIPI data lane1 Lane1 will be LP00 Bit[6]: MIPI lane1 disable 1: Disable MIPI data lane1 Lane1 will be LP00 Bit[5]: LPX Global timing select 0: Auto calculate t_lpx_o in pclk2x domain, unit clk2x 1: Use lp_p_min[7:0]

table 6-5 MIPI transmitter registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x480A	MIPI DATA ORDER	0x00	RW	Bit[2]: Bit order reverse Bit[1:0]: Bit position adjust 01: {data[7:0],data[9:8]} 10: {data[1:0],data[9:2]}
0x4818	MIN HS ZERO H	0x00	RW	High Byte of Minimum Value of hs_zero Unit ns
0x4819	MIN HS ZERO L	0x96	RW	Low Byte of Minimum Value of hs_zero hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	MIN MIPI HS TRAIL H	0x00	RW	High Byte of Minimum Value of hs_trail Unit ns
0x481B	MIN MIPI HS TRAIL L	0x3C	RW	Low Byte of Minimum Value of hs_trail hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	MIN MIPI CLK ZERO H	0x01	RW	High Byte of Minimum Value of clk_zero
0x481D	MIN MIPI CLK ZERO L	0x86	RW	Low Byte of Minimum Value of clk_zero clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	MIN MIPI CLK PREPARE H	0x00	RW	High Byte of Minimum Value of clk_prepare Unit ns
0x481F	MIN MIPI CLK PREPARE L	0x3C	RW	Low Byte of Minimum Value of clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	MIN CLK POST H	0x00	RW	High Byte of Minimum Value of clk_post Unit ns
0x4821	MIN CLK POST L	0x56	RW	Low Byte of Minimum Value of clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	MIN CLK TRAIL H	0x00	RW	High Byte of Minimum Value of clk_trail Unit ns
0x4823	MIN CLK TRAIL L	0x3C	RW	Low Byte of Minimum Value of clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	MIN LPX PCLK H	0x00	RW	High Byte of Minimum Value of lpx_p Unit ns
0x4825	MIN LPX PCLK L	0x32	RW	Low Byte of Minimum Value of lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	MIN HS PREPARE H	0x00	RW	High Byte of Minimum Value of hs_prepare Unit ns
0x4827	MIN HS PREPARE L	0x32	RW	Low Byte of Minimum Value of hs_prepare hs_prepare_real = hs_prepare_min_o + Tui*ui_hs_prepare_min_o

table 6-5 MIPI transmitter registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x4828	MIN HS EXIT H	0x00	RW	High Byte of Minimum Value of hs_exit Unit ns
0x4829	MIN HS EXIT L	0x64	RW	Low Byte of Minimum Value of hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	MIN HS ZERO/UI	0x05	RW	Minimum UI Value of hs_zero Unit UI
0x482B	MIN HS TRAIL/UI	0x04	RW	Minimum UI Value of hs_trail Unit UI
0x482C	MIN CLK ZERO/UI	0x00	RW	Minimum UI Value of clk_zero Unit UI
0x482D	MIN CLK PREPARE/UI	0x00	RW	Minimum UI Value of clk_prepare Unit UI
0x482E	MIN CLK POST/UI	0x34	RW	Minimum UI Value of clk_post Unit UI
0x482F	MIN CLK TRAIL/UI	0x00	RW	Minimum UI Value of clk_trail Unit UI
0x4830	MIN LPX PCLK/UI	0x00	RW	Minimum UI Value of lpx_p(pclk2x domain) Unit UI
0x4831	MIN HS PREPARE/UI	0x04	RW	Minimum UI Value of hs_prepare Unit UI
0x4832	MIN HS EXIT/UI	0x00	RW	Minimum UI Value of hs_exit Unit UI
0x4837	PCLK PERIOD	0x10	RW	Period of Pixel Clock, pclk_div = 1, and 1-bit Decimal

7 register tables

The following tables provide descriptions of the device control registers contained in the OV5645. For all registers enable/disable bits, ENABLE = 1 and DISABLE = 0.

7.1 system and IO pad control [0x3000 - 0x3052]

table 7-1 system and IO pad control registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x3000	SYSTEM RESET00	0x30	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset BIST Bit[6]: Reset MCU program memory Bit[5]: Reset MCU Bit[4]: Reset OTP Bit[3]: Reset STB Bit[2]: Reset D5060 Bit[1]: Reset timing control Bit[0]: Reset array control
0x3001	SYSTEM RESET01	0x08	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset AWB registers Bit[6]: Reset AFC Bit[5]: Reset ISP Bit[4]: Reset FC Bit[3]: Reset S2P Bit[2]: Reset BLC Bit[1]: Reset AEC registers Bit[0]: Reset AEC
0x3002	SYSTEM RESET02	0x1C	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset VFIFO Bit[6]: Debug mode Bit[5]: Reset format Bit[4:2]: Not used Bit[1]: Reset format MUX Bit[0]: Reset average
0x3003	SYSTEM RESET03	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7:6]: Debug mode Bit[5]: Reset digital gain compensation Bit[4]: Reset SYNC FIFO Bit[3]: Reset PSRAM Bit[2]: Reset ISP FC Bit[1]: Reset MIPI Bit[0]: Reset SPI_RX

table 7-1 system and IO pad control registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x3004	CLOCK ENABLE00	0xCF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable BIST clock Bit[6]: Enable MCU program memory clock Bit[5]: Enable MCU clock Bit[4]: Enable OTP clock Bit[3]: Enable STROBE clock Bit[2]: Enable D5060 clock Bit[1]: Enable timing control clock Bit[0]: Enable array control clock
0x3005	CLOCK ENABLE01	0xF7	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable AWB register clock Bit[6]: Enable AFC clock Bit[5]: Enable ISP clock Bit[4]: Enable FC clock Bit[3]: Enable S2P clock Bit[2]: Enable BLC clock Bit[1]: Enable AEC register clock Bit[0]: Enable AEC clock
0x3006	CLOCK ENABLE02	0xE3	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable PSRAM clock Bit[6]: Enable FMT clock Bit[5:2]: Debug mode Bit[1]: Enable format MUX clock Bit[0]: Enable average clock
0x3007	CLOCK ENABLE03	0xFF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable digital gain compensation clock Bit[6]: Enable SYNC FIFO clock Bit[5]: Enable ISPFC SCLK clock Bit[4]: Enable MIPI PCLK clock Bit[3]: Enable MIPI clock Bit[2]: Enable SPI_RX SCLK clock Bit[1]: Enable VFIFO PCLK clock Bit[0]: Enable VFIFO SCLK clock

table 7-1 system and IO pad control registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x3008	SYSTEM CTRL0	0x02	RW	System Control Bit[7]: Software reset Bit[6]: Software power down Bit[5]: Debug mode Bit[4]: SRB clock sync enable Bit[3]: Isolation suspend select Bit[2]: MIPI reset mask Bit[1]: MIPI suspend mask Bit[0]: MIPI reset select
0x3009	MIPI PCLK DIVIDER CTRL	0x01	RW	MIPI PCLK Divider Control Bit[7]: MIPI PDIV separate 1: MIPI PCLK divider separate setting from MIPI serial clock Bit[5:0]: MIPI PCLK divider
0x300A	SENSOR CHIP ID HIGH BYTE	0x56	R	Chip ID High Byte
0x300B	SENSOR CHIP ID LOW BYTE	0x45	R	Chip ID Low Byte
0x300C	SYSTEM DIVIDER CONTROL 2	0x22	RW	SDIV Bit[7]: Debug mode Bit[6:4]: For div mc clock Bit[2:0]: For r_sdiv
0x300D	MIPI CTRL0	0x00	RW	Bit[7:5]: Debug mode Bit[4]: Option for MIPI dis data lane Bit[3]: Option for MIPI clock lane Bypass clock lane latch in MIPI PHY Bit[2]: Pull down MIPI clock lane Bit[1]: Pull down MIPI data lane2 Bit[0]: Pull down MIPI data lane1

table 7-1 system and IO pad control registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x300E	MIPI CONTROL 00	0x58	RW	MIPI Control 00 Bit[7:5]: mipi_lane_mode 001: One lane mode 010: Two lane mode Others: Debug mode Bit[4]: MIPI TX PHY power down 0: Debug mode 1: Power down PHY HS TX Bit[3]: MIPI RX PHY power down 0: Debug mode 1: Power down PHY LP RX module Bit[2]: mipi_en 0: DVP enable 1: MIPI enable Bit[1]: MIPI suspend register MIPI system suspend register 0: Debug mode 1: Suspend Bit[0]: Lane disable option
0x300F~ 0x3015	DEBUG MODE	–	–	Debug Mode
0x3016	PAD OUTPUT ENABLE 00	0x00	RW	Input/Output Control (0: input; 1: output) Bit[7:2]: Debug mode Bit[1]: Strobe output enable Bit[0]: SIOD output enable
0x3017	PAD OUTPUT ENABLE 01	0x00	RW	Input/Output Control (0: input; 1: output) Bit[7]: FREX output enable Bit[6]: VSYNC output enable Bit[5]: Reserved Bit[4]: CSK output enable Bit[3:0]: Debug mode
0x3018	PAD OUTPUT ENABLE 02	0x00	RW	Input/Output Control (0: input; 1: output) Bit[7:4]: Debug mode Bit[3:0]: GPIO0 output enable

table 7-1 system and IO pad control registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x3019	PAD OUTPUT VALUE 00	0xF0	RW	Pad Output Value Bit[7]: MIPI data lane option Bypass latch in MIPI PHY Bit[6]: MIPI lane2 state in sleep mode 0: LP00 1: LP11 Bit[5]: MIPI lane1 state in sleep mode 0: LP00 1: LP11 Bit[4]: MIPI CLK lane state in sleep mode 0: LP00 1: LP11 Bit[3:2]: Debug mode Bit[1]: Strobe Bit[0]: SIOD
0x301A	PAD OUTPUT VALUE 01	0x00	RW	GPIO Output Value 01 Bit[7]: FREX Bit[6]: VSYNC Bit[5]: Reserved Bit[4]: CSK Bit[3:0]: Reserved
0x301B	PAD OUTPUT VALUE 02	0x00	RW	GPIO Output Value 02 Bit[7:4]: Reserved Bit[3:0]: GPIO0[3:0]
0x301C	PAD SELECT 00	0x00	RW	Output Selection for GPIO Bit[7:4]: Debug mode Bit[3:2]: IO CSD[1:0] select Bit[1]: IO strobe select Bit[0]: IO SIOD select
0x301D	PAD SELECT 01	0x00	RW	Output Selection for GPIO Bit[7]: FREX select Bit[6]: VSYNC select Bit[5]: Reserved Bit[4]: IO PCLK select Bit[3:0]: Reserved
0x301E	PAD SELECT 02	0x00	RW	Output Selection for GPIO Bit[7:4]: Reserved Bit[3:0]: Chip revision
0x301F	DEBUG MODE	–	–	Debug Mode
0x302A	CHIP REVISION	0xB0	R	Bit[7:4]: Process 0xA: FSI 0xB: BSI Bit[3:0]: Chip revision
0x302B	DEBUG MODE	–	–	Debug Mode

table 7-1 system and IO pad control registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x302C	PAD CONTROL 00	0x02	RW	Pad Control Bit[7:6]: Output drive capability 00: 1x 01: 2x 10: 3x 11: 4x Bit[5]: pd_dato_en Bit[4:2]: Reserved Bit[1]: FREX enable Bit[0]: STROBE IN enable
0x302D~ 0x3034	SYSTEM CONTROL	–	RW	System Control Registers Changing these values is not recommended
0x3035	SC PLL CONTRL1	0x11	RW	Bit[7:4]: System clock divider Slow down all clocks Bit[3:0]: Scale divider for MIPI MIPI PCLK/SERCLK can be slowed down
0x3036	SC PLL CONTRL2	0x69	RW	Bit[7:0]: PLL multiplier (4~252) Can be any integer from 4~127 and only even integers from 128~252
0x3037	SC PLL CONTRL3	0x03	RW	Bit[7:5]: Debug mode Bit[4]: PLL root divider 0: Bypass 1: Divided by 2 Bit[3:0]: PLL pre-divider 1,2,3,4,6,8
0x3038	SC PLL CONTRL 4	0x00	RW	Bit[7]: PLL multiplier debug enable Bit[1:0]: PLL multiplier1 debug control bits
0x3039	SC PLL CONTRL 5	0x00	RW	Bit[7]: PLL bypass Bit[6:0]: Debug mode
0x303A	SC PLLS CTRL0	0x00	RW	Bit[7]: PLLS bypass Bit[6:0]: Debug mode
0x303B	SC PLLS CTRL1	0x19	RW	Bit[7:5]: Debug mode Bit[4:0]: PLLS multiplier
0x303C	SC PLLS CTRL2	0x11	RW	Bit[7]: Debug mode Bit[6:4]: PLLS charge pump control Bit[3:0]: PLLS system divider

table 7-1 system and IO pad control registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x303D	SC PLLS CTRL3	0x30	RW	Bit[7:6]: Debug mode Bit[5:4]: PLLS pre-divider 00: /1 01: /1.5 10: /2 11: /3 Bit[3]: Debug mode Bit[2]: PLLS root divider 0: /1 1: /2 Bit[1:0]: PLLS seld5 00: /1 01: /1 10: /2 11: /2.5
0x303E~ 0x304F	SYSTEM CONTROL	–	RW	System Control Registers Changing these values is not recommended
0x3050	IO PAD VALUE	–	R	Read Pad Value Bit[7:6]: CSD[1:0] Bit[5]: Debug mode Bit[4]: FREX Bit[3]: PWDNB Bit[2]: Debug mode Bit[1]: SIOC Bit[0]: Debug mode
0x3051	IO PAD VALUE	–	R	Read Pad Value Bit[7]: OTP memory out Bit[6]: VSYNC Bit[5]: Debug mode Bit[4]: CSK Bit[3:0]: Debug mode
0x3052	IO PAD VALUE	–	R	Pad Input Status Bit[7:4]: Debug mode Bit[3:0]: GPIO1

7.2 SCCB control [0x3100 - 0x3108]

table 7-2 SCCB control registers

address	register name	default value	R/W	description
0x3100	SCCB_ID	0x78	RW	SCCB Slave ID
0x3101	DEBUG MODE	–	–	Debug Mode
0x3102	SCCB SYSTEM CTRL0	0x00	RW	Bit[7]: Debug mode Bit[6]: MIPI SC reset Bit[5]: SRB reset Bit[4]: SCCB slave reset Bit[3]: rst_pon_sccb Bit[2]: Debug mode Bit[1]: MIPI PHY reset Bit[0]: PLL reset
0x3103	SCCB SYSTEM CTRL1	0x00	RW	PLL Clock Select Bit[7:2]: Debug mode Bit[1]: Select PLL input clock 0: From pre divider clock modulator 1: From PLL Bit[0]: Debug mode
0x3104~ 0x3107	SCCB SYSTEM CTRL0	–	RW	SCCB Control Registers Changing these values is not allowed
0x3108	SYSTEM ROOT DIVIDER	0x16	RW	Pad Clock Divider for SCCB Clock Bit[7:6]: Debug mode Bit[5:4]: PCLK root divider 00: PCLK = pll_clki 01: PCLK = pll_clki/2 10: PCLK = pll_clki/4 11: PCLK = pll_clki/8 Bit[3:2]: sclk2x root divider 00: SCLK2x = pll_clki 01: SCLK2x = pll_clki/2 10: SCLK2x= pll_clki/4 11: SCLK2x= pll_clki/8 Bit[1:0]: SCLK root divider 00: SCLK = pll_clki 01: SCLK = pll_clki/2 10: SCLK= pll_clki/4 11: sclk= pll_clki/8

7.3 SRB control [0x3200 - 0x3211]

table 7-3 SRB control registers

address	register name	default value	R/W	description
0x3200	GROUP ADDR0	0x40	RW	SRAM Group Address0
0x3201	GROUP ADDR1	0x4A	RW	SRAM Group Address1
0x3202	GROUP ADDR2	0x54	RW	SRAM Group Address2
0x3203	GROUP ADDR3	0x5E	RW	SRAM Group Address3
0x3204~ 0x3211	GROUP WRITE CONTROL REGISTERS	–	RW	Group Write Registers Changing these values is not recommended
0x3212	SRM GROUP ACCESS	–	W	SRM Group Access Bit[7]: Group launch enable Bit[6]: Test mode access group Bit[5]: Group launch Bit[4]: Group hold end Bit[3:0]: Group ID 00xx: Group ID 01xx: Reserved 1xxx: Reserved
0x3213	SRM GROUP STATUS	–	R	SRM Group Status Bit[7]: Store Bit[6]: Restore Bit[5]: Group hold Bit[4]: Group launch Bit[3]: Group write Bit[2:0]: Group select

7.4 powerkeep domain AWB gain control [0x3400 - 0x3406]

table 7-4 powerkeep domain AWB gain control registers

address	register name	default value	R/W	description
0x3400	AWB R GAIN	0x04	RW	Bit[3:0]: AWB R gain[11:8]
0x3401	AWB R GAIN	0x00	RW	Bit[7:0]: AWB R gain[7:0]
0x3402	AWB G GAIN	0x04	RW	Bit[3:0]: AWB G gain[11:8]
0x3403	AWB G GAIN	0x00	RW	Bit[7:0]: AWB G gain[7:0]
0x3404	AWB B GAIN	0x04	RW	Bit[3:0]: AWB B gain[11:8]

table 7-4 powerkeep domain AWB gain control registers

address	register name	default value	R/W	description
0x3405	AWB B GAIN	0x00	RW	Bit[7:0]: AWB B gain[7:0]
0x3406	AWB MANUAL CONTROL	0x00	RW	Bit[7:1]: Debug mode Bit[0]: AWB gain manual enable 0: Auto 1: Manual

7.5 AEC/AGC control [0x3500 - 0x350D]

table 7-5 AEC/AGC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3500	AEC PK EXPOSURE	0x00	RW	Exposure Output Bit[7:4]: Debug mode Bit[3:0]: Exposure[19:16]
0x3501	AEC PK EXPOSURE	0x02	RW	Exposure Output Bit[7:0]: Exposure[15:8]
0x3502	AEC PK EXPOSURE	0x00	RW	Long Channel Exposure Output Bit[7:0]: Exposure[7:0]
0x3503	AEC PK MANUAL	0x00	RW	AEC Manual Mode Control Bit[7:2]: Debug mode Bit[1]: AGC manual 0: Auto enable 1: Manual enable Bit[0]: AEC manual 0: Auto enable 1: Manual enable
0x3504~ 0x3505	DEBUG MODE	–	–	Debug Mode
0x3506	AEC REAL GAIN READ	–	R	Bit[7:2]: Debug mode Bit[1:0]: AEC real gain output[9:8]
0x3507	AEC REAL GAIN READ	–	R	Bit[7:0]: AEC real gain output[7:0]
0x3508~ 0x3509	DEBUG MODE	–	–	Debug Mode
0x350A	AEC PK REAL GAIN	0x00	RW	Real Gain Bit[7:2]: Debug mode Bit[1:0]: Real gain[9:8]
0x350B	AEC PK REAL GAIN	0x10	RW	Real Gain Bit[7:0]: Real gain[7:0]

table 7-5 AEC/AGC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x350C	AEC PK VTS	0x00	RW	AEC Add VTS Output Bit[7:0]: Add VTS[15:8]
0x350D	AEC PK VTS	0x00	RW	AEC Add VTS Output Bit[7:0]: Add VTS[7:0]

7.6 timing control [0x3800 - 0x3821]

table 7-6 timing control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	TIMING HS	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: X address start[11:8]
0x3801	TIMING HS	0x00	RW	Bit[7:0]: X address start[7:0]
0x3802	TIMING VS	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Y address start[11:8]
0x3803	TIMING VS	0x00	RW	Bit[7:0]: Y address start[7:0]
0x3804	TIMING HW	0x0A	RW	Bit[7:4]: Debug mode Bit[3:0]: X address end[11:8]
0x3805	TIMING HW	0x3F	RW	Bit[7:0]: X address end[7:0]
0x3806	TIMING VH	0x07	RW	Bit[7:3]: Debug mode Bit[2:0]: Y address end[10:8]
0x3807	TIMING VH	0x9F	RW	Bit[7:0]: Y address end[7:0]
0x3808	TIMING DVPHO	0x0A	RW	Bit[7:4]: Debug mode Bit[3:0]: DVP output horizontal width[11:8]
0x3809	TIMING DVPHO	0x20	RW	Bit[7:0]: DVP output horizontal width[7:0]
0x380A	TIMING DVPVO	0x07	RW	Bit[7:3]: Debug mode Bit[2:0]: DVP output vertical height[10:8]
0x380B	TIMING DVPVO	0x98	RW	Bit[7:0]: DVP output vertical height[7:0]
0x380C	TIMING HTS	0x0B	RW	Bit[7:5]: Debug mode Bit[4:0]: Total horizontal size[12:8]
0x380D	TIMING HTS	0x1C	RW	Bit[7:0]: Total horizontal size[7:0]
0x380E	TIMING VTS	0x07	RW	Bit[7:0]: Total vertical size[15:8]
0x380F	TIMING VTS	0xB0	RW	Bit[7:0]: Total vertical size[7:0]

table 7-6 timing control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3810	TIMING HOFFSET	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: ISP horizontal offset[11:8]
0x3811	TIMING_HOFFSET	0x10	RW	Bit[7:0]: Horizontal offset[7:0]
0x3812	TIMING VOFFSET	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: Vertical offset[10:8]
0x3813	TIMING VOFFSET	0x04	RW	Bit[7:0]: Vertical offset[7:0]
0x3814	TIMING X INC	0x11	RW	Bit[7:4]: Horizontal odd subsample increment Bit[3:0]: Horizontal even subsample increment
0x3815	TIMING Y INC	0x11	RW	Bit[7:4]: Vertical odd subsample increment Bit[3:0]: Vertical even subsample increment
0x3816	HSYNC START	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: HSYNC start point[11:8]
0x3817	HSYNC START	0x00	RW	Bit[7:0]: HSYNC start point[7:0]
0x3818	HSYNC WIDTH	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: HSYNC width[11:8]
0x3819	HSYNC WIDTH	0x00	RW	Bit[7:0]: HSYNC width[7:0]
0x3820	TIMING TC REG20	0x40	RW	Timing Control Bit[7:5]: Debug mode Bit[4]: Blackline vflip Bit[3]: ISP vflip Bit[2]: ISP vflip Bit[1]: Sensor vflip Bit[0]: Vertical binning enable
0x3821	TIMING TC REG21	0x00	RW	Timing Control Bit[7:6]: Debug mode Bit[5]: JPEG enable Bit[4:3]: Debug mode Bit[2]: ISP mirror Bit[1]: Sensor mirror Bit[0]: Horizontal binning enable

7.7 AEC/AGC power down domain control [0x3A00 - 0x3A25]

table 7-7 AEC/AGC power down domain control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3A00	AEC CTRL00	0x78	RW	AEC System Control (0: disable; 1: enable) Bit[7]: Debug mode Bit[6]: Less one line enable Bit[5]: Band function enable Bit[4]: Less 1 band enable Bit[3]: Start selection Bit[2]: Night mode Bit[1]: New balance function Bit[0]: Freeze
0x3A01	AEC MIN EXPOSURE	0x01	RW	Minimum Exposure Output Limit Bit[7:0]: Minimum exposure
0x3A02	AEC MAX EXPO (60HZ)	0x3D	RW	60Hz Maximum Exposure Output Limit Bit[7:0]: Maximum exposure[15:8]
0x3A03	AEC MAX EXPO (60HZ)	0x80	RW	60Hz Maximum Exposure Output Limit Bit[7:0]: Maximum exposure[7:0]
0x3A04	DEBUG MODE	–	–	Debug Mode
0x3A05	AEC CTRL05	0x30	RW	AEC System Control 2 Bit[7]: Debug mode Bit[6]: frame insert 0: In night mode, insert frame disable 1: In night mode, insert frame enable Bit[5]: Step auto enable 0: Step manual mode 1: Step auto mode Bit[4:0]: Step auto ratio In step auto mode, step ratio setting to adjust speed
0x3A06	AEC CTRL06	0x10	RW	AEC System Control 3 Bit[7:5]: Debug mode Bit[4:0]: Step manual setting 1 Step manual Increase mode fast step
0x3A07	AEC CTRL07	0x18	RW	AEC Manual Step Register Bit[7:4]: Step manual setting 2 Step manual, slow step Bit[3:0]: Step manual setting 3 Step manual, decrease mode fast step
0x3A08	AEC B50 STEP	0x01	RW	50Hz Band Width Bit[7:2]: Debug mode Bit[1:0]: B50 step[9:8]

table 7-7 AEC/AGC power down domain control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3A09	AEC B50 STEP	0x27	RW	50Hz Band Width Bit[7:0]: B50 step[7:0]
0x3A0A	AEC B60 STEP	0x00	RW	60Hz Band Width Bit[7:2]: Debug mode Bit[1:0]: B60 step[9:8]
0x3A0B	AEC B60 STEP	0xF6	RW	60Hz Band Width Bit[7:0]: B60 step[7:0]
0x3A0C	AEC CTRL0C	0xE4	RW	Bit[7:4]: E1 max Decimal line high limit zone Bit[3:0]: E1 min Decimal line low limit zone
0x3A0D	AEC CTRL0D	0x08	RW	60Hz Max Bands in One Frame Bit[7:6]: Debug mode Bit[5:0]: B60 max
0x3A0E	AEC CTRL0E	0x06	RW	50Hz Max Bands in One Frame Bit[7:6]: Debug mode Bit[5:0]: B50 max
0x3A0F	AEC CTRL0F	0x78	RW	Stable Range High Limit (Enter) Bit[7:0]: WPT
0x3A10	AEC CTRL10	0x68	RW	Stable Range Low Limit (Enter) Bit[7:0]: BPT
0x3A11	AEC CTRL11	0xD0	RW	Step Manual Mode, Fast Zone High Limit Bit[7:0]: VPT high
0x3A12	DEBUG MODE	–	–	Debug Mode
0x3A13	AEC CTRL13	0x40	RW	Bit[7]: Debug mode Bit[6]: Pre-gain enable Bit[5:0]: Pre-gain value 0x40 = 1x
0x3A14	AEC MAX EXPO (50HZ)	0x0E	RW	50Hz Maximum Exposure Output Limit Bit[7:4]: Debug mode Bit[3:0]: Max exposure[11:8]
0x3A15	AEC MAX EXPO (50HZ)	0x40	RW	50Hz Maximum Exposure Output Limit Bit[7:0]: Max exposure[7:0]
0x3A16	DEBUG MODE	–	–	Debug Mode

table 7-7 AEC/AGC power down domain control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3A17	AEC CTRL17	0x01	RW	Gain Base When in Night Mode Bit[7:2]: Debug mode Bit[1:0]: Gain night threshold 00: 00 01: 10 10: 30 11: 70
0x3A18	AEC GAIN CEILING	0x03	RW	Gain Output Top Limit Bit[7:2]: Debug mode Bit[1:0]: AEC gain ceiling[9:8] Real gain format
0x3A19	AEC GAIN CEILING	0xE0	RW	Gain Output Top Limit Bit[7:0]: AEC gain ceiling[7:0] Real gain format
0x3A1A	AEC DIFF MIN	0x04	RW	Reserved Default Value for This Register Bit[7:0]: Difference minimal
0x3A1B	AEC CTRL1B	0x78	RW	Stable Range High Limit (Go Out) Bit[7:0]: WPT2
0x3A1C	LED ADD ROW	0x06	RW	Exposure Values Added When Strobe is On Bit[7:0]: AEC LED add row[15:8]
0x3A1D	LED ADD ROW	0x18	RW	Exposure Values Added When Strobe is On Bit[7:0]: AEC LED add row[7:0]
0x3A1E	AEC CTRL1E	0x68	RW	Stable Range Low Limit (Go Out) Bit[7:0]: BPT2
0x3A1F	AEC CTRL1F	0x40	RW	Step Manual Mode, Fast Zone Low Limit Bit[7:0]: VPT low
0x3A20	AEC CTRL20	0x20	RW	Bit[7:3]: Debug mode Bit[2]: Strobe option Bit[1:0]: Debug mode
0x3A21	AEC CTRL21	0x78	RW	Bit[7]: Debug mode Bit[6:4]: Insert frame number Bit[3:0]: Debug mode
0x3A22~ 0x3A24	DEBUG MODE	–	–	Debug Mode
0x3A25	AEC CTRL25	0x00	RW	Bit[7:5]: Debug mode Bit[4:2]: Freeze counter Bit[1:0]: Debug mode
0x3A50	AEC READ 50	–	R	Bit[7:0]: Average readout
0x3A51	AEC READ 51	–	R	Bit[7:2]: Debug mode Bit[1:0]: Current state readout

table 7-7 AEC/AGC power down domain control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3A52	AEC READ 52	–	R	Bit[7:3]: Debug mode Bit[2]: Increase current Bit[1]: Decrease current Bit[0]: Balance current
0x3A53	AEC READ 53	–	R	Bit[7:6]: Debug mode Bit[5]: AEC update Bit[4]: Ch Bit[3]: Ch3 Bit[2]: Ch2 Bit[1]: Ch1 Bit[0]: Ch0
0x3A54	AEC READ 54	–	R	Bit[7:4]: Debug mode Bit[3:0]: Step[11:8] readout
0x3A55	AEC READ 55	–	R	Bit[7:0]: Step[7:0] readout
0x3A56	AEC READ 56	–	R	Bit[7:0]: e tmp[31:24] readout
0x3A57	AEC READ 57	–	R	Bit[7:0]: e tmp[23:16] readout
0x3A58	AEC READ 58	–	R	Bit[7:0]: e tmp[15:8] readout
0x3A59	AEC READ 59	–	R	Bit[7:0]: e tmp[7:0] readout
0x3A5A	AEC READ 5a	–	R	Bit[7:0]: e tmp pg[31:24] readout
0x3A5B	AEC READ 5b	–	R	Bit[7:0]: e tmp pg[23:16] readout
0x3A5C	AEC READ 5c	–	R	Bit[7:0]: e tmp pg[15:8] readout
0x3A5D	AEC READ 5d	–	R	Bit[7:0]: e tmp pg[7:0] readout
0x3A5E	AEC READ 5e	–	R	Bit[7:0]: AEC VTS[15:8] readout
0x3A5F	AEC READ 5f	–	R	Bit[7:0]: AEC VTS[7:0] readout
0x3A60	AEC READ 60	–	R	Bit[7:4]: Debug mode Bit[3]: LED add dummy Bit[2]: LED model2 Bit[1]: 5060 new Bit[0]: 5060
0x3A61	AEC READ 61	–	R	Bit[7:5]: Debug mode Bit[4:0]: Max 1 frame[12:8]
0x3A62	AEC READ 62	–	R	Bit[7:0]: Max 1 frame[7:0]
0x3A63	AEC READ 63	–	R	Bit[7:1]: Debug mode Bit[0]: Sensor gain[8]
0x3A64	AEC READ 64	–	R	Bit[7:0]: Sensor gain[7:0]

7.8 strobe control [0x3B00 - 0x3B0C]

table 7-8 strobe registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Bit[7]: Strobe request on/off 0: Off 1: On Bit[6]: Strobe pulse reverse Bit[5:4]: Debug mode Bit[3:2]: width_in_xenon Bit[1:0]: Strobe mode 00: Xenon 01: LED1 10: LED2 11: LED3
0x3B01	FREX EXPOSURE 02	0x00	RW	Bit[7:0]: FREX exposure time[23:16]
0x3B02	FREX SHUTTER DELAY 01	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: Shutter delay time[13:8]
0x3B03	FREX SHUTTER DELAY 00	0x00	RW	Bit[7:0]: Shutter delay time[7:0] Unit: 64x SCLK cycle
0x3B04	FREX EXPOSURE 01	0x04	RW	Bit[7:0]: FREX exposure time[15:8]
0x3B05	FREX EXPOSURE 00	0x00	RW	Bit[7:0]: FREX exposure time[7:0] Unit: Tline
0x3B06	FREX CTRL 07	0x04	RW	Bit[7:4]: FREX frame delay Bit[3:0]: Strobe width[3:0]
0x3B07	FREX MODE	0x08	RW	FREX Mode Selection Bit[1:0]: FREX mode 00: FREX strobe mode0 01: FREX strobe mode1 1x: Rolling strobe
0x3B08	FREX REQUEST	0x00	RW	FREX Request
0x3B09	FREX HREF DELAY	0x02	RW	FREX HREF Delay
0x3B0A	FREX RST LENGTH	0x04	RW	Bit[7:3]: Debug mode Bit[2:0]: FREX precharge length 000: 1/16 Tline 001: 1/8 Tline 010: 1/4 Tline 011: 1/2 Tline 100: 1 Tline 101: 2 Tline 110: 4 Tline 111: 8 Tline

table 7-8 strobe registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B0B	STROBE WIDTH	0x00	RW	Bit[7:0]: Strobe width[19:12]
0x3B0C	STROBE WIDTH	0x3D	RW	Bit[7:0]: Strobe width[11:4]

7.9 50/60Hz detector control [0x3C00 - 0x3C1E]

table 7-9 5060Hz detector registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3C00	5060HZ CTRL00	0x00	RW	Bit[7]: Debug mode Bit[6]: Inverse SCLK Bit[5]: Time counter threshold divisor enable Bit[4]: Low limit enable Bit[3]: Debug mode Bit[2]: Band50 default value Bit[1:0]: Time counter threshold 00: 1s 01: 2s 10: 4s 11: 8s
0x3C01	5060HZ CTRL01	0x00	RW	Bit[7]: Band manual enable Bit[6]: Band begin reset enable Bit[5]: Sum auto mode enable Bit[4]: Band counter enable Bit[3:0]: Band counter Counter threshold for band change
0x3C02	5060HZ CTRL02	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Low light threshold No detection under low light Bit[7:6]: Low light limit mode
0x3C03	5060HZ CTRL03	0x00	RW	Bit[7:0]: Counter threshold for low light
0x3C04	5060HZ CTRL04	0x20	RW	Bit[7:0]: Threshold for low sum
0x3C05	5060HZ CTRL05	0x70	RW	Bit[7:0]: Threshold for high sum
0x3C06	LIGHT METER1 THRESHOLD	0x00	RW	Bit[7:0]: Lightmeter1 threshold[15:8]
0x3C07	LIGHT METER1 THRESHOLD	0x00	RW	Bit[7:0]: Lightmeter1 threshold[7:0]
0x3C08	LIGHT METER2 THRESHOLD	0x01	RW	Bit[7:0]: Lightmeter2 threshold[15:8]

table 7-9 5060Hz detector registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3C09	LIGHT METER2 THRESHOLD	0x2C	RW	Bit[7:0]: Lightmeter2 threshold[7:0]
0x3C0A	SAMPLE NUMBER	0x4E	RW	Bit[7:0]: Sample number[15:8]
0x3C0B	SAMPLE NUMBER	0x1F	RW	Bit[7:0]: Sample number[7:0]
0x3C0C	SIGMADELTA CTRL0C	–	R	Bit[7:4]: Band counter Bit[1]: Sign bit of sum50/60 Bit[0]: Band50/60 0: 60Hz light 1: 50Hz light
0x3C0D	SUM 50	–	R	Bit[7:5]: Debug mode Bit[4:0]: Sum50[28:24]
0x3C0E	SUM 50	–	R	Bit[7:0]: Sum50[23:16]
0x3C0F	SUM 50	–	R	Bit[7:0]: Sum50[15:8]
0x3C10	SUM 50	–	R	Bit[7:0]: Sum50[7:0]
0x3C11	SUM 60	–	R	Bit[7:5]: Debug mode Bit[4:0]: Sum60[28:24]
0x3C12	SUM 60	–	R	Bit[7:0]: Sum60[23:16]
0x3C13	SUM 60	–	R	Bit[7:0]: Sum60[15:8]
0x3C14	SUM 60	–	R	Bit[7:0]: Sum60[7:0]
0x3C15	SUM 50 60	–	R	Bit[7:0]: Sum50/60[15:8]
0x3C16	SUM 50 60	–	R	Bit[7:0]: Sum50/60[7:0]
0x3C17	BLOCK COUNTER	–	R	Bit[7:0]: Block counter[15:8]
0x3C18	BLOCK COUNTER	–	R	Bit[7:0]: Block counter[7:0]
0x3C19	B6	–	R	Bit[7:0]: B6[15:8]
0x3C1A	B6	–	R	Bit[7:0]: B6[7:0]
0x3C1B	LIGHTMETER OUTPUT	–	R	Bit[7:4]: Debug mode Bit[3:0]: Light meter output[19:16]
0x3C1C	LIGHTMETER OUTPUT	–	R	Bit[7:0]: Light meter output[15:8]
0x3C1D	LIGHTMETER OUTPUT	–	R	Bit[7:0]: Light meter output[7:0]
0x3C1E	SUM THRESHOLD	–	R	Sum Threshold
0x3C1F	5060HZ CTRL1F	–	R	5060Hz Register 0x1F

7.10 OTP control [0x3D00 - 0x3D21]

table 7-10 OTP control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D00	OTP DATA00	0x00	RW	OTP Dump/Load Data00
0x3D01	OTP DATA01	0x00	RW	OTP Dump/Load Data01
0x3D02	OTP DATA02	0x00	RW	OTP Dump/Load Data02
0x3D03	OTP DATA03	0x00	RW	OTP Dump/Load Data03
0x3D04	OTP DATA04	0x00	RW	OTP Dump/Load Data04
0x3D05	OTP DATA05	0x00	RW	OTP Dump/Load Data05
0x3D06	OTP DATA06	0x00	RW	OTP Dump/Load Data06
0x3D07	OTP DATA07	0x00	RW	OTP Dump/Load Data07
0x3D08	OTP DATA08	0x00	RW	OTP Dump/Load Data08
0x3D09	OTP DATA09	0x00	RW	OTP Dump/Load Data09
0x3D0A	OTP DATA0A	0x00	RW	OTP Dump/Load Data0a
0x3D0B	OTP DATA0B	0x00	RW	OTP Dump/Load Data0b
0x3D0C	OTP DATA0C	0x00	RW	OTP Dump/Load Data0c
0x3D0D	OTP DATA0D	0x00	RW	OTP Dump/Load Data0d
0x3D0E	OTP DATA0E	0x00	RW	OTP Dump/Load Data0e
0x3D0F	OTP DATA0F	0x00	RW	OTP Dump/Load Data0f
0x3D10	OTP DATA10	0x00	RW	OTP Dump/Load Data10
0x3D11	OTP DATA11	0x00	RW	OTP Dump/Load Data11
0x3D12	OTP DATA12	0x00	RW	OTP Dump/Load Data12
0x3D13	OTP DATA13	0x00	RW	OTP Dump/Load Data13
0x3D14	OTP DATA14	0x00	RW	OTP Dump/Load Data14
0x3D15	OTP DATA15	0x00	RW	OTP Dump/Load Data15
0x3D16	OTP DATA16	0x00	RW	OTP Dump/Load Data16
0x3D17	OTP DATA17	0x00	RW	OTP Dump/Load Data17
0x3D18	OTP DATA18	0x00	RW	OTP Dump/Load Data18
0x3D19	OTP DATA19	0x00	RW	OTP Dump/Load Data19
0x3D1A	OTP DATA1A	0x00	RW	OTP Dump/Load Data1A

table 7-10 OTP control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D1B	OTP DATA1B	0x00	RW	OTP Dump/Load Data1B
0x3D1C	OTP DATA1C	0x00	RW	OTP Dump/Load Data1C
0x3D1D	OTP DATA1D	0x00	RW	OTP Dump/Load Data1D
0x3D1E	OTP DATA1E	0x00	RW	OTP Dump/Load Data1E
0x3D1F	OTP DATA1F	0x00	RW	OTP Dump/Load Data1F
0x3D20	OTP PROGRAM CTRL	0x00	RW	Bit[7]: OTP program busy Bit[6:2]: Debug mode Bit[1]: OTP program speed 0: Fast 1: Slow Bit[0]: OTP program enable
0x3D21	OTP READ CTRL	0x00	RW	Bit[7]: OTP read busy Bit[6:2]: Debug mode Bit[1]: OTP read speed 0: Fast 1: Slow Bit[0]: OTP read enable

7.11 BIST control [0x3E00 - 0x3EFF]

table 7-11 BIST registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3E00	BIST_START_ADDRESS	0x00	RW	Bit[7:0]: Specify BIST start address[15:8]
0x3E01	BIST_START_ADDRESS	0x00	RW	Bit[7:0]: Specify BIST start address[7:0]
0x3E02	BIST_END_ADDRESS	0x0F	RW	Bit[7:0]: Specify BIST end address[15:8]
0x3E03	BIST_END_ADDRESS	0xDB	RW	Bit[7:0]: Specify BIST end address[7:0]
0x3E04	BIST_R4	0x14	RW	BIST Option Count Bit[7:5]: Byte select in read only mode Bit[4:0]: BIST option count Specify BIST operation number It can be set from 5'h02 to 5'h14
0x3E05	BIST_R5	0x00	RW	BIST Special Data Bit[7:0]: Specify data written into memory in special mode
0x3E06	BIST_R6	0x03	RW	SRAM Select Specify SRAM Select

table 7-11 BIST registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3E07	BIST CTRL07	0x20	RW	Bit[7]: BIST start specifies BIST start It should first be high, then low Bit[6]: Specify BIST restart Bit[5]: BIST mode specifies BIST test mode 0: Manual mode 1: Auto mode Bit[4]: Special BIST special mode Bit[3]: Specify read only mode Bit[2:0]: Debug mode
0x3E0C	BIST CTRL12	–	R	Bit[4]: BIST busy specifies BIST busy status Bit[2:0]: BIST error byte specifies BIST error type
0x3E0D	BIST RESULT00	0x00	RW	BIST Test Result00 (0: BIST pass; 1: BIST error) Bit[7:1]: Debug mode Bit[0]: mc_pram
0x3E0E	BIST RESULT01	0x00	RW	BIST Test Result01 (0: BIST pass; 1: BIST error) Bit[7]: SRM Bit[6]: PFIFO2 Bit[5]: PFIFO1 Bit[4]: VFIFO Bit[3]: spi_rx Bit[2]: Scale2 Bit[1]: Scale1 Bit[0]: DPC4
0x3E0F	BIST RESULT02	0x00	RW	BIST Test Result02 (0: BIST pass; 1: BIST error) Bit[7]: DPC3 Bit[6]: DPC2 Bit[5]: DPC1 Bit[4]: CIP3 Bit[3]: CIP2 Bit[2]: CIP1 Bit[1]: AWB Bit[0]: MCU IRAM

7.12 MC control [0x3F00 - 0x3F0D]

table 7-12 MC registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3F00	MC CTRL00	0x00	RW	Bit[7:5]: Debug mode Bit[4]: DW8051 manual reset enable Bit[3]: DW8051 manual reset Bit[2]: IRAM manual reset enable Bit[1]: IRAM manual reset Bit[0]: Soft reset MCU 0: Debug mode 1: Reset MCU
0x3F01	MC INTERRUPT MASK0	0x00	RW	Bit[7:0]: Mask0 for interrupt 0: Disable interrupt bit 1: Enable interrupt bit
0x3F02	MC INTERRUPT MASK1	0x00	RW	Bit[7:0]: Mask1 for interrupt 0: Disable interrupt bit 1: Enable interrupt bit
0x3F03	MC READ INTERRUPT ADDRESS	0x70	RW	Bit[7:0]: Set high byte for SCCB address that will trigger interrupt when read
0x3F04	MC READ INTERRUPT ADDRESS	0x00	RW	Bit[7:0]: Set low byte for SCCB address that will trigger interrupt when read
0x3F05	MC WRITE INTERRUPT ADDRESS	0x70	RW	Bit[7:0]: Set high byte for SCCB address that will trigger interrupt when written
0x3F06	MC WRITE INTERRUPT ADDRESS	0x04	RW	Bit[7:0]: Set low byte for SCCB address that will trigger interrupt when written
0x3F08	MC INTERRUPT SOURCE SELECTION1	0x00	RW	Bit[7:6]: Interrupt1[7] source selection 0x: AEC done 10: Debug mode 11: DVP HREF falling edge Bit[5:4]: Interrupt1[6] source selection 00: ISP average done 01: FREX rising edge 10: Debug mode 11: DVP VSYNC falling edge Bit[3:2]: Interrupt1[5] source selection 00: AEC trigger 01: FREX falling edge 10: MIPI frame end 11: DVP VSYNC rising edge Bit[1:0]: Interrupt1[4] source selection 0x: JEPG over size 10: MIPI line end 11: DVP HREF rising edge

table 7-12 MC registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3F09	MC INTERRUPT SOURCE SELECTION2	0x00	RW	Bit[7:6]: Interrupt1[3] source selection 0x: Debug mode 11: SRM operation start Bit[5:4]: Interrupt1[2] source selection 0x: Debug mode 11: SRM operation done Bit[3:2]: Interrupt1[1] source selection 0x: Debug mode 11: DVP frame counter change Bit[1:0]: Interrupt1[0] source selection 0x: BLC SOF 11: Debug mode
0x3F0A	MC INTERRUPT SOURCE SELECTION3	0x00	RW	Bit[7:6]: Interrupt0[7] source selection 00: JFIFO over flow 01: ISP end frame 10: SFIFO end of frame 11: JFIFO end frame Bit[5:4]: Interrupt0[6] source selection 0x: JFIFO end of image 10: F1 FIFO write 11: VFIFO ready Bit[3:2]: Interrupt0[5] source selection 00: ISP end of frame 01: SFIFO end of frame 10: JFIFO end of frame 11: VFIFO end of frame Bit[1:0]: Interrupt0[4] source selection 00: ISP start of frame 01: SFIFO start of frame 10: JFIFO start of frame 11: VFIFO start of frame

table 7-12 MC registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3F0B	MC INTERRUPT SOURCE SELECTION4	0x00	RW	Bit[7:6]: Interrupt0[3] source selection 0x: AFC done 10: HREF falling edge 11: BIST done Bit[5:4]: Interrupt0[2] source selection 00: AWB done 01: ISP start of frame 10: SFIFO start of frame 11: JFIFO start of frame Bit[3:2]: Interrupt0[1] source selection 00: VFIFO full 01: ISP FC SOF 10: f2_fifo_wr 11: Write a specific address Bit[1:0]: Interrupt0[0] source selection 00: VFIFO empty 01: ISP line 10: ISP end of frame 11: Read a specific address
0x3F0C	MC INTERRUPT0 STATUS	–	R	Bit[7:0]: Interrupt0 status indication
0x3F0D	MC INTERRUPT1 STATUS	–	R	Bit[7:0]: Interrupt1 status indication

7.13 BLC control [0x4000 - 0x4033]

table 7-13 BLC registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x89	RW	BLC Control 00 (0: disable; 1: enable) Bit[7]: BLC median filter enable Bit[6:4]: Debug mode Bit[3]: ADC 11-bit mode Bit[2]: Apply2blackline Bit[1]: Black line average frame Bit[0]: BLC enable
0x4001	BLC CTRL01	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: BLC start line

table 7-13 BLC registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x4002	BLC CTRL02	0x45	RW	Bit[7]: Format change enable BLC update when format changes Bit[6]: BLC auto enable 0: Manual 1: Auto Bit[5:0]: Reset frame number Frame number BLC do after reset
0x4003	BLC CTRL03	0x08	RW	Bit[7]: BLC redo enable Write 1 to this bit will trigger a BLC redo N frames begin, where N is 0x4003[5:0] Bit[6]: BLC freeze Bit[5:0]: Manual frame number
0x4004	BLC CTRL04	0x08	RW	Bit[7:0]: BLC line number Specify the line number BLC process
0x4005	BLC CTRL05	0x18	RW	Bit[7:2]: Debug mode Bit[1]: BLC always update 0: Normal freeze 1: BLC always update Bit[0]: Debug mode
0x4006	BLC CTRL07	0x00	RW	Bit[7:6]: Debug mode Bit[5]: Black line number manual enable Bit[4:0]: Black number manual
0x4007	BLC CTRL07	0x00	RW	Bit[7:5]: Debug mode Bit[4:3]: Window selection 00: Full image 01: A windows not contain the first 16 pixels and the end 16 pixels 10: A windows not contain the first 1/16 image and the end 1/16 image 11: A windows not contain the first 1/8 image and the end 1/8 image Bit[2:0]: Bypass mode 0000: Bypass input data after limit to [10:0] 0001: Bypass input data[11:0] 0010: Bypass input data[12:1] 0011: Bypass debug data bbrr 0100: Bypass debug data gggg

table 7-13 BLC registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x4008	BLC CTRL08	0x00	RW	BLC Control (0: disable; 1: enable) Bit[7:4]: Debug mode Bit[3]: Flip image manual enable Bit[2]: Flip image manual Bit[1]: Flip black line manual enable Bit[0]: Flip black line manual
0x4009	BLACK LEVEL	0x10	RW	Bit[7:0]: BLC black level target at 10-bit range
0x4009	BLACK LEVEL	0x10	RW	Bit[7:0]: BLC black level target at 10-bit range
0x400C	BLC MAN0	0x00	RW	Bit[7:0]: BLCman0[15:8]
0x400D	BLC MAN0	0x00	RW	Bit[7:0]: BLCman0[7:0]
0x400E	BLC MAN1	0x00	RW	Bit[7:0]: BLCman1[15:8]
0x400F	BLC MAN1	0x00	RW	Bit[7:0]: BLCman1[7:0]
0x4010	BLC MAN2	0x00	RW	Bit[7:0]: BLCman2[15:8]
0x4011	BLC MAN2	0x00	RW	Bit[7:0]: BLCman2[7:0]
0x4012	BLC MAN3	0x00	RW	Bit[7:0]: BLCman3[15:8]
0x4013	BLC MAN3	0x00	RW	Bit[7:0]: BLCman3[7:0]
0x402C	BLACK LEVEL00	0x00	RW	Bit[7:0]: Blacklevel00[15:8] With 3 decimal
0x402D	BLACK LEVEL00	0x00	RW	Bit[7:0]: Blacklevel00[7:0] With 3 decimal
0x402E	BLACK LEVEL01	0x00	RW	Bit[7:0]: Blacklevel01[15:8] With 3 decimal
0x402F	BLACK LEVEL01	0x00	RW	Bit[7:0]: Blacklevel01[7:0] With 3 decimal
0x4030	BLACK LEVEL10	0x00	RW	Bit[7:0]: Blacklevel10[15:8] With 3 decimal
0x4031	BLACK LEVEL10	0x00	RW	Bit[7:0]: Blacklevel10[7:0] With 3 decimal
0x4032	BLACK LEVEL11	0x00	RW	Bit[7:0]: Blacklevel11[15:8] With 3 decimal
0x4033	BLACK LEVEL11	0x00	RW	Bit[7:0]: Blacklevel11[7:0] With 3 decimal
0x4050	BLC MAX	0xFF	RW	Bit[7:0]: BLC max black level
0x4051	STABLE RANGE	0x7F	RW	Bit[7:0]: BLC stable range

table 7-13 BLC registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x4052	ONE CHANNEL	0x00	RW	Bit[7:0]: BLC one channel use the average of 4 channels as black level for 4 channels
0x4060	BLC BR THRE0	0x00	RW	Bit[7:0]: BLC br thr 0
0x4061	BLC BR THRE1	0x00	RW	Bit[7:0]: BLC br thr 1
0x4062	BLC BR THRE2	0x00	RW	Bit[7:0]: BLC br thr 2
0x4063	BLC BR THRE3	0x00	RW	Bit[7:0]: BLC br thr 3
0x4064	BLC BR THRE4	0x00	RW	Bit[7:0]: BLC br thr 4
0x4065	BLC BR THRE5	0x00	RW	Bit[7:0]: BLC br thr 5
0x4066	BLC G THRE0	0x00	RW	Bit[7:0]: BLC g thr 0
0x4067	BLC G THRE1	0x00	RW	Bit[7:0]: BLC g thr 1
0x4068	BLC G THRE2	0x00	RW	Bit[7:0]: BLC g thr 2
0x4069	BLC G THRE3	0x00	RW	Bit[7:0]: BLC g thr 3
0x406A	BLC G THRE4	0x00	RW	Bit[7:0]: BLC g thr 4
0x406B	BLC G THRE5	0x00	RW	Bit[7:0]: BLC g thr 5
0x406C	BLC BRG COMP EN	0x00	RW	Bit[7:0]: BLC brg compensate enable

7.14 frame control [0x4201 - 0x4202]

table 7-14 frame control registers

address	register name	default value	R/W	description
0x4201	FRAME CTRL01	0x00	R/W	Control Passed Frame Number When both ON and OFF number set to 0x00, frame control is in bypass mode Bit[7:4]: Debug mode Bit[3:0]: Frame ON number
0x4202	FRAME CTRL02	0x00	R/W	Control Masked Frame Number When both ON and OFF number set to 0x00, frame control is in bypass mode Bit[7:4]: Debug mode Bit[3:0]: Frame OFF number

7.15 format control [0x4300 - 0x430D]

table 7-15 format control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x4300	FORMAT CONTROL 00	0xF8	RW	Format Control 00 Bit[7:4]: Output format of formatter module 0x0: RAW Bit[3:0]: Output sequence 0x0: BGBG... / GRGR... 0x1: GBGB... / RGRG... 0x2: GRGR... / BGBG... 0x3: RGRG... / GBGB... 0x4~0xF: Not allowed 0x1: Y8 Bit[3:0]: Does not matter 0x2: YUV444/RGB888 (not available for full resolution) Bit[3:0]: Output sequence 0x0: YUVYUV..., or GBRGBR... 0x1: YVUYVU..., or GRBGRB... 0x2: UYVUYV..., or BGRBGR... 0x3: VYUVYU..., or RGBRGB... 0x4: UVYUVY..., or BRGBRG... 0x5: VUYVUY..., or RBGRBG... 0x6~0xE: Not allowed 0xF: UYVUYV..., or BGRBGR... 0x3: YUV422 Bit[3:0]: Output sequence 0x0: YUYV... 0x1: YVYU... 0x2: UYVY... 0x3: VYUY... 0x4~0xE: Not allowed 0xF: UYVY... 0x4: YUV420 Bit[3:0]: Output sequence 0x0: YYYY... / YUYV... 0x1: YYYY... / YVYU... 0x2: YYYY... / UYVY... 0x3: YYYY... / VYUY... 0x4: YUYV... / YYYY... 0x5: YVYU... / YYYY... 0x6: UYVY... / YYYY...

table 7-15 format control registers (sheet 2 of 5)

address	register name	default value	R/W	description
				0x7: VYUY... / YYYY... 0x8~0xE: Not allowed 0xF: YYYY... / UYVY... 0x5: YUV420 (for MIPI only) Bit[3:0]: Output sequence 0x0~0xD: Not allowed 0xE: VYYVYY... / UYYUYY... 0xF: UYYUYY... / VYYVYY... 0x6: RGB565 Bit[3:0]: Output sequence 0x0: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x1: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x2: {g[4:0],r[5:3]}, {r[2:0],b[4:0]} 0x3: {b[4:0],r[5:3]}, {r[2:0],g[4:0]} 0x4: {g[4:0],b[5:3]}, {b[2:0],r[4:0]} 0x5: {r[4:0],b[5:3]}, {b[2:0],g[4:0]} 0x6~0xE: Not allowed 0xF: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} 0x7: RGB555 format 1 Bit[3:0]: Output sequence 0x0: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x1: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0]} 0x2: {g[4:0],r[4:2]}, {r[1:0],1'b0,b[4:0]} 0x3: {b[4:0],r[4:2]}, {r[1:0],1'b0,g[4:0]} 0x4: {r[4:0],b[4:2]}, {b[1:0],1'b0,g[4:0]} 0x5: {g[4:0],b[4:2]}, {b[1:0],1'b0,r[4:0]} 0x6~0xE: Not allowed 0xF: {g[1:0],1'b0,b[4:0]}, {r[4:0],g[4:2]} 0x8: RGB555 format 2 Bit[3:0]: Output sequence 0x0: {1'b0,b[4:0],g[4:3]}, {g[2:0],r[4:0]} 0x1: {1'b0,r[4:0],g[4:2]}, {g[2:0],b[4:0]}

table 7-15 format control registers (sheet 3 of 5)

address	register name	default value	R/W	description
				0x2: {1'b0,g[4:0],r[4:2]}, {r[2:0],b[4:0]} 0x3: {1'b0,b[4:0],r[4:2]}, {r[2:0],g[4:0]} 0x4: {1'b0,r[4:0],b[4:2]}, {b[2:0],g[4:0]} 0x5: {1'b0,g[4:0],b[4:2]}, {b[2:0],r[4:0]} 0x6: {b[4:0],1'b0,g[4:3]}, {g[2:0],r[4:0]} 0x7: {r[4:0],1'b0,g[4:2]}, {g[2:0],b[4:0]} 0x8: {g[4:0],1'b0,r[4:2]}, {r[2:0],b[4:0]} 0x9: {b[4:0],1'b0,r[4:2]}, {r[2:0],g[4:0]} 0xA: {r[4:0],1'b0,b[4:2]}, {b[2:0],g[4:0]} 0xB: {g[4:0],1'b0,b[4:2]}, {b[2:0],r[4:0]} 0xC~0xF: Not allowed 0x9: RGB444 format 1 Bit[3:0]: Output sequence 0x0: {1'b0,b[3:0],2'h0,g[3]}, {g[2:0],1'b0,r[3:0]} 0x1: {1'b0,r[3:0],2'h0,g[3]}, {g[2:0],1'b0,b[3:0]} 0x2: {1'b0,g[3:0],2'h0,r[3]}, {r[2:0],1'b0,b[3:0]} 0x3: {1'b0,b[3:0],2'h0,r[3]}, {r[2:0],1'b0,g[3:0]} 0x4: {1'b0,r[3:0],2'h0,b[3]}, {b[2:0],1'b0,g[3:0]} 0x5: {1'b0,g[3:0],2'h0,b[3]}, {b[2:0],1'h0,r[3:0]} 0x6: {b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0} 0x7: {r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x8: {g[3:0],1'b0,r[3:1]}, {r[0],2'h0,b[3:0],1'b0} 0x9: {b[3:0],1'b0,r[3:1]}, {r[0],2'h0,g[3:0],1'b0} 0xA: {r[3:0],1'b0,b[3:1]}, {b[0],2'h0,g[3:0],1'b0} 0xB: {g[3:0],1'b0,b[3:1]}, {b[0],2'h0,r[3:0],1'b0} 0xC~0xE: Not allowed 0xF: {g[0],2'h2,b[3:0],1'b1}, {r[3:0],1'b1,g[3:1]}

table 7-15 format control registers (sheet 4 of 5)

address	register name	default value	R/W	description
				0xA: RGB444 format 2 Bit[3:0]: Output sequence 0x0: {4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x1: {4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x2: {4'b0,b[3:0]}, {r[3:0],g[3:0]} 0x3: {4'b0,r[3:0]}, {b[3:0],g[3:0]} 0x4: {4'b0,g[3:0]}, {b[3:0],r[3:0]} 0x5: {4'b0,g[3:0]}, {r[3:0],b[3:0]} 0x6: {b[3:0],g[3:0],2'h0}, {r[3:0],b[3:0],2'h0, g[3:0],r[3:0],2'h0} 0x7: {r[3:0],g[3:0],2'h0}, {b[3:0],r[3:0],2'h0, g[3:0],b[3:0],2'h0} 0x8: {b[3:0],r[3:0],2'h0}, {g[3:0],b[3:0],2'h0, r[3:0],g[3:0],2'h0} 0x9: {r[3:0],b[3:0],2'h0}, {g[3:0],r[3:0],2'h0, b[3:0],g[3:0],2'h0} 0xA: {g[3:0],b[3:0],2'h0}, {r[3:0],g[3:0],2'h0, b[3:0],r[3:0],2'h0} 0xB: {g[3:0],r[3:0],2'h0}, {b[3:0],g[3:0],2'h0, r[3:0],b[3:0],2'h0} 0xC~0xF: Not allowed 0xB~0xE: Not allowed 0xF: Bypass formatter module (not recommended) Bit[3:0]: Output format 0x8: Raw 0x9: YUV422 0xA: YUV444 0xE: VYYVYY.../UYYUYY 0xF: UYYUYY.../VYYVYY
0x4301	FORMAT CONTROL 01	0x00	RW	Format Control 01 Bit[1:0]: YUV422 UV control 00: U/V generated from average 01: U/V generated from first pixel 10: Not valid 11: U/V generated from second pixel

table 7-15 format control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x4302	YMAX VALUE	0x03	RW	Bit[7:2]: Debug mode Bit[1:0]: Y max clip value[9:8]
0x4303	YMAX VALUE	0xFF	RW	Bit[7:0]: Y max clip value[7:0]
0x4304	YMIN VALUE	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Y min clip value[9:8]
0x4305	YMIN VALUE	0x00	RW	Bit[7:0]: Y min clip value[7:0]
0x4306	UMAX VALUE	0x03	RW	Bit[7:2]: Debug mode Bit[1:0]: U max clip value[9:8]
0x4307	UMAX VALUE	0xFF	RW	Bit[7:0]: U max clip value[7:0]
0x4308	UMIN VALUE	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: U min clip value[9:8]
0x4309	UMIN VALUE	0x00	RW	Bit[7:0]: U min clip value[7:0]
0x430A	VMAX VALUE	0x03	RW	Bit[7:2]: Debug mode Bit[1:0]: V max clip value[9:8]
0x430B	VMAX VALUE	0xFF	RW	Bit[7:0]: V max clip value[7:0]
0x430C	VMIN VALUE	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: V min clip value[9:8]
0x430D	VMIN VALUE	0x00	RW	Bit[7:0]: V min clip value[7:0]
0x4310	VSYNC_WIDTH	0x00	RW	Bit[7:0]: VSYNC width In terms of lines
0x4311	VSYNC_WIDTH H	0x04	RW	Bit[7:0]: VSYNC width[15:8] In terms of pixel numbers
0x4312	VSYNC WIDTH L	0x00	RW	Bit[7:0]: VSYNC width[7:0] In terms of pixel numbers
0x4313	VSYNC CTRL	0x00	RW	Bit[7:5]: Debug mode Bit[4]: VSYNC polarity Bit[3:2]: VSYNC output select Bit[1]: VSYNC mode 3 Bit[0]: VSYNC mode 2
0x4314	VSYNC DELAY1	0x00	RW	Bit[7:0]: VSYNC trigger to VSYNC delay[23:16]
0x4315	VSYNC DELAY2	0x00	RW	Bit[7:0]: VSYNC trigger to VSYNC delay[15:8]
0x4316	VSYNC DELAY3	0x00	RW	Bit[7:0]: VSYNC trigger to VSYNC delay[7:0]

7.16 VFIFO control [0x4600]

table 7-16 VFIFO registers

address	register name	default value	R/W	description
0x4600	VFIFO CTRL00	0x80	RW	VFIFO Control 00 Bit[7:6]: Debug mode Bit[5]: Compression output fixed height enable 0: In compression mode2, compression height is different in each frame 1: In compression mode2, compression height is fixed in each frame Bit[4]: Test pattern enable – incremental pattern Bit[3:0]: Debug mode

7.17 MIPI control [0x4800 - 0x4837]

table 7-17 MIPI transmitter registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[7:6]: Debug mode Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Lane select 0: Use lane1 as default data lane 1: Use lane2 as default data lane Bit[2]: Idle status 0: MIPI bus will be LP00 when no packet to transmit 1: MIPI bus will be LP11 when no packet to transmit Bit[1:0]: Debug mode

table 7-17 MIPI transmitter registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x4801	MIPI CTRL 01	0x0F	RW	MIPI Control 01 Bit[7]: Long packet data type manual enable 0: Use mipi_dt 1: Use dt_man_o as long packet data Bit[6]: Short packet data type manual enable 1: Use dt_spkt as short packet data Bit[5]: Short packet word counter manual enable 0: Use frame counter or line counter 1: Select spkt_wc_reg_o Bit[4]: PH bit order for ECC 0: {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]} Bit[3]: PH byte order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[2]: PH byte order2 for ECC 0: {DI,WC} 1: {WC,DI} Bit[1]: MARK1 enable for data lane1 1: When resume, lane1 should send MARK1 Bit[0]: MARK1 enable for data lane2 1: When resume, lane2 should send MARK1
0x4802	MIPI CTRL 02	0x00	RW	Bit[7]: Hs_prepare select 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: Clk_prepare select 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: Clk_post select 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: Clk_trail select 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: Hs_exit select 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: Hs_zero select 0: Auto calculate T_hs_zero, unit pclk2xtxie 1: Use hs_zero_min_o[7:0] Bit[1]: Hs_trail select 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: Clk_zero select 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]

table 7-17 MIPI transmitter registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x4803~ 0x4804	DEBUG MODE	–	–	Debug Mode
0x4805	MIPI CTRL 05	0x10	RW	Bit[7]: MIPI lane1 disable 1: Disable MIPI data lane1 Lane1 will be LP00 Bit[6]: MIPI lane1 disable 1: Disable MIPI data lane1 Lane1 will be LP00 Bit[5]: LPX global timing select 0: Auto calculate t_lpx_o in pclk2x domain, unit clk2x 1: Use lp_p_min[7:0] Bit[6:0]: Debug mode
0x4806	MIPI TEST CTRL	0x28	RW	Bit[7]: PRBS enable Bit[6]: MIPI test enable Bit[5]: MIPI low power output option Bit[4]: Two lane manual enable Bit[3]: Two lane manual Bit[2:0]: Debug mode
0x4807~ 0x4809	DEBUG MODE	–	–	Debug Mode
0x480A	MIPI DATA ORDER	0x00	RW	Bit[7:3]: Debug mode Bit[2]: Bit order reverse Bit[1:0]: Bit position adjust 01: {data[7:0],data[9:8]} 10: {data[1:0],data[9:2]}
0x480B~ 0x4817	DEBUG MODE	–	–	Debug Mode
0x4818	MIN HS ZERO H	0x00	RW	High Byte of Minimum Value of hs_zero Unit ns
0x4819	MIN HS ZERO L	0x96	RW	Low Byte of Minimum Value of hs_zero hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	MIN MIPI HS TRAIL H	0x00	RW	High Byte of Minimum Value of hs_trail Unit ns
0x481B	MIN MIPI HS TRAIL L	0x3C	RW	Low Byte of Minimum Value of hs_trail hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	MIN MIPI CLK ZERO H	0x01	RW	High Byte of Minimum Value of clk_zero
0x481D	MIN MIPI CLK ZERO L	0x86	RW	Low Byte of Minimum Value of clk_zero clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	MIN MIPI CLK PREPARE H	0x00	RW	High Byte of Minimum Value of clk_prepare Unit ns

table 7-17 MIPI transmitter registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x481F	MIN MIPI CLK PREPARE L	0x3C	RW	Low Byte of Minimum Value of clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	MIN CLK POST H	0x00	RW	High Byte of Minimum Value of clk_post Unit ns
0x4821	MIN CLK POST L	0x56	RW	Low Byte of Minimum Value of clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	MIN CLK TRAIL H	0x00	RW	High Byte of Minimum Value of clk_trail Unit ns
0x4823	MIN CLK TRAIL L	0x3C	RW	Low Byte of Minimum Value of clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	MIN LPX PCLK H	0x00	RW	High Byte of Minimum Value of lpx_p Unit ns
0x4825	MIN LPX PCLK L	0x32	RW	Low Byte of Minimum Value of lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	MIN HS PREPARE H	0x00	RW	High Byte of Minimum Value of hs_prepare Unit ns
0x4827	MIN HS PREPARE L	0x32	RW	Low Byte of Minimum Value of hs_prepare hs_prepare_real = hs_prepare_min_o + Tui*ui_hs_prepare_min_o
0x4828	MIN HS EXIT H	0x00	RW	High Byte of Minimum Value of hs_exit Unit ns
0x4829	MIN HS EXIT L	0x64	RW	Low Byte of Minimum Value of hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	MIN HS ZERO/UI	0x05	RW	Minimum UI Value of hs_zero Unit UI
0x482B	MIN HS TRAIL/UI	0x04	RW	Minimum UI Value of hs_trail Unit UI
0x482C	MIN CLK ZERO/UI	0x00	RW	Minimum UI Value of clk_zero Unit UI
0x482D	MIN CLK PREPARE/UI	0x00	RW	Minimum UI Value of clk_prepare Unit UI
0x482E	MIN CLK POST/UI	0x34	RW	Minimum UI Value of clk_post Unit UI
0x482F	MIN CLK TRAIL/UI	0x00	RW	Minimum UI Value of clk_trail Unit UI
0x4830	MIN LPX PCLK/UI	0x00	RW	Minimum UI Value of lpx_p(pclk2x domain) Unit UI

table 7-17 MIPI transmitter registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x4831	MIN HS PREPARE/UI	0x04	RW	Minimum UI Value of hs_prepare Unit UI
0x4832	MIN HS EXIT/UI	0x00	RW	Minimum UI Value of hs_exit Unit UI
0x4833~ 0x4836	DEBUG MODE	–	–	Debug Mode
0x4837	PCLK PERIOD	0x10	RW	Period of Pixel Clock, pclk_div = 1, and 1-bit Decimal

7.18 ISP frame control [0x4901 - 0x4902]

table 7-18 ISP frame control registers

address	register name	default value	R/W	description
0x4901	FRAME CTRL01	0x00	RW	Control Passed Frame Number When both ON and OFF number set to 0x00, frame control is in bypass mode Bit[7:4]: Debug mode Bit[3:0]: Frame ON number
0x4902	FRAME CTRL02	0x00	RW	Control Masked Frame Number When both ON and OFF number set to 0x00, frame control is in bypass mode Bit[7:4]: Debug mode Bit[3:0]: Frame OFF number

7.19 SPI receiver control [0x4B00 - 0x4B12]

table 7-19 spi_rx control registers

address	register name	default value	R/W	description
0x4B00	SPI RX CTRL00	0x06	RW	Bit[7]: Debug mode Bit[6]: SPI_rx selection 0: SPI 2.0 1: SPI 3.0 Bit[5]: Debug mode Bit[4]: Line start manual enable Bit[3]: Debug mode Bit[2]: byte_order 0: LSB first 1: MSB first Bit[1]: bit_order 0: LSB first 1: MSB first Bit[0]: Data high/low byte swap
0x4B01	SPI RX CTRL01	0x0A	RW	Bit[7]: CSK reverse Bit[6]: Debug mode Bit[5]: Raw8 enable Bit[4]: SRAM_test1 Bit[3:0]: SRAM_rm
0x4B02	SPI RX CTRL02	0x01	RW	Bit[7:6]: Debug mode Bit[5:0]: Line start manual[13:8]
0x4B03	SPI RX CTRL03	0x40	RW	Bit[7:0]: Line start manual[7:0]
0x4B04	SPI RX CTRL04	0x10	RW	Bit[7:4]: Debug mode Bit[3]: CRC request Bit[2:1]: CRC flag option Bit[0]: Debug mode
0x4B05	SPI RX CTRL05	–	R	Bit[7:0]: data_id[7:0]
0x4B06	SPI RX CTRL06	–	R	Bit[7:0]: image_width[15:8]
0x4B07	SPI RX CTRL07	–	R	Bit[7:0]: image_width[7:0]
0x4B08	SPI RX CTRL08	–	R	Bit[7:0]: image_height[15:8]
0x4B09	SPI RX CTRL09	–	R	Bit[7:0]: image_height[7:0]
0x4B0A~ 0x4B0E	DEBUG MODE	–	–	Debug Mode
0x4B0F	SPI RX CTRL0F	–	R	Bit[7]: crc_done Bit[6:0]: Debug mode
0x4B10	SPI RX CTRL10	–	R	Bit[7:0]: Debug mode for internal use only
0x4B11	SPI RX CTRL11	–	R	Bit[7:0]: SPI CRC 16[15:8]
0x4B12	SPI RX CTRL12	–	R	Bit[7:0]: SPI CRC 16[7:0]

7.20 ISP top control [0x5000 - 0x5063]

table 7-20 ISP top control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0x06	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6]: Debug mode Bit[5]: RAW GMA enable 0: Disable 1: Enable Bit[4:3]: Debug mode Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Color interpolation enable 0: Disable 1: Enable
0x5001	ISP CONTROL 01	0x01	RW	Bit[7]: Special digital effect enable 0: Disable 1: Enable Bit[6]: Debug mode Bit[5]: Scale enable 0: Disable 1: Enable Bit[4:3]: Debug mode Bit[2]: UV average enable 0: Disable 1: Enable Bit[1]: Color matrix enable 0: Disable 1: Enable Bit[0]: Auto white balance enable 0: Disable 1: Enable
0x5002	ISP CONTROL02	0x80	RW	Bit[7:0]: Debug mode

table 7-20 ISP top control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x5003	ISP CONTROL 03	0x08	RW	Bit[7:3]: Debug mode Bit[2]: Bin enable 0: Disable 1: Enable Bit[1]: Draw window for AFC enable 0: Disable 1: Enable Bit[0]: Solarize enable 0: Disable 1: Enable
0x5004	ISP CONTROL 04	0x00	RW	Bit[7:0]: Debug mode for internal use only
0x5005	ISP CONTROL 05	0x36	RW	Bit[7]: Debug mode Bit[6]: AWB bias manual enable 0: Disable 1: Enable Bit[5]: AWB bias ON enable 0: Disable 1: Enable Bit[4]: AWB bias plus enable 0: Disable 1: Enable Bit[3]: Debug mode Bit[2]: LENC bias ON enable 0: Disable 1: Enable Bit[1]: GMA bias ON enable 0: Disable 1: Enable Bit[0]: LENC bias manual enable 0: Disable 1: Enable
0x5006~ 0x501C	DEBUG MODE	–	–	Debug Mode
0x501D	ISP MISC	0x00	RW	Bit[7]: Debug mode Bit[6]: SDE AVG manual enable Bit[5]: AWB YUV2CBCR enable Bit[4]: Average size manual enable Bit[3:0]: Debug mode
0x501E	DEBUG MODE	–	–	Debug Mode

table 7-20 ISP top control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x501F	FORMAT MUX CONTROL	0x00	RW	Format MUX Control Bit[7:4]: Debug mode Bit[3]: Fmt vfirst Bit[2:0]: Format select 000: ISP YUV422 001: ISP RGB 010: ISP dither 011: ISP RAW (DPC) 100: SNR RAW 101: ISP RAW (CIP)
0x5020	DITHER CTRL 0	0x00	RW	Bit[7]: Debug mode Bit[6]: Dither mux Bit[5:4]: R dithering Bit[3:2]: G dithering Bit[1:0]: B dithering
0x5021~ 0x5026	DEBUG MODE	–	–	Debug Mode
0x5027	DRAW WINDOW CONTROL 00	0x02	RW	Bit[7:1]: Debug mode Bit[0]: Draw window control 0: No fixed Y 1: Fixed Y
0x5028	DRAW WINDOW LEFT POSITION CONTROL	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: Draw window left[11:8]
0x5029	DRAW WINDOW LEFT POSITION CONTROL	0x90	RW	Bit[7:0]: Draw window left[7:0]
0x502A	DRAW WINDOW RIGHT POSITION CONTROL	0x05	RW	Bit[7:4]: Debug mode Bit[3:0]: Draw window right[11:8]
0x502B	DRAW WINDOW RIGHT POSITION CONTROL	0x90	RW	Bit[7:0]: Draw window right[7:0]
0x502C	DRAW WINDOW TOP POSITION CONTROL	0x03	RW	Bit[7:3]: Debug mode Bit[2:0]: Draw window top[10:8]
0x502D	DRAW WINDOW TOP POSITION CONTROL	0x6C	RW	Bit[7:0]: Draw window top[7:0]
0x502E	DRAW WINDOW BOTTOMPOSITION CONTROL	0x04	RW	Bit[7:3]: Debug mode Bit[2:0]: Draw window bottom[10:8]

table 7-20 ISP top control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x502F	DRAW WINDOW BOTTOM POSITION CONTROL	0x2C	RW	Bit[7:0]: Draw window bottom[7:0]
0x5030	DRAW WINDOW HORIZONTAL BOUNDARY WIDTH CONTROL	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Draw window horizontal boundary width[11:8]
0x5031	DRAW WINDOW HORIZONTAL BOUNDARY WIDTH CONTROL	0x14	RW	Bit[7:0]: Draw window horizontal boundary width[7:0]
0x5032	DRAW WINDOW VERTICAL BOUNDARY WIDTH CONTROL	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: Draw window vertical boundary width[10:8]
0x5033	DRAW WINDOW VERTICAL BOUNDARY WIDTH CONTROL	0x14	RW	Bit[7:0]: Draw window vertical boundary width[7:0]
0x5034	DRAW WINDOW Y CONTROL	0x80	RW	Bit[7:0]: Fixed Y for draw window
0x5035	DRAW WINDOW U CONTROL	0x2A	RW	Bit[7:0]: Fixed U for draw window
0x5036	DRAW WINDOW V CONTROL	0x14	RW	Bit[7:0]: Fixed V for draw window
0x5037~ 0x503C	DEBUG MODE	–	–	Debug Mode
0x503D	PRE ISP TEST SETTING 1	0x00	RW	Bit[7]: Pre ISP test enable 0: Test disable 1: Color bar enable Bit[6]: Rolling Bit[5]: Transparent Bit[4]: Square BW Bit[3:2]: Pre ISP bar style 00: Standard 8 color bar 01: Gradual change at vertical mode 1 10: Gradual change at horizontal 11: Gradual change at vertical mode 2 Bit[1:0]: Test select 00: Color bar 01: Random data 10: Square data 11: Black image

table 7-20 ISP top control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x503E~ 0x5060	DEBUG MODE	–	–	Debug Mode
0x5061	ISP SENSOR BIAS I	–	R	ISP Sensor Bias I
0x5062	ISP SENSOR GAIN I	–	R	ISP Sensor Gain I
0x5063	ISP SENSOR GAIN I	–	R	ISP Sensor Gain I

7.21 AWB control [0x5180 - 0x51D0]

table 7-21 AWB registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x5180	AWB CONTROL 00	0xFF	RW	Bit[7:0]: AWB B block
0x5181	AWB CONTROL 01	0x58	RW	Bit[7:6]: Step local Bit[5:4]: Step fast Bit[3]: Slop 8x Bit[2]: Slop 4x Bit[1]: One zone Bit[0]: AVG all
0x5182	AWB CONTROL 02	0x11	RW	Bit[7:4]: Max local counter Bit[3:0]: Max fast counter
0x5183	AWB CONTROL 03	0x90	RW	Bit[7]: AWB simple enable 0: AWB advance 1: AWB simple Bit[6]: AWB advance 0: YUV enable 1: Simple YUV enable Bit[5]: AWB preset Bit[4]: AWB SIMF Bit[3:2]: AWB win Bit[0]: AWB FD select
0x5184	AWB CONTROL 04	0x25	RW	Bit[7:6]: Count area selection Bit[5]: G enable Bit[4:2]: Count limit control Bit[1:0]: Counter threshold
0x5185	AWB CONTROL 05	0x24	RW	Bit[7:4]: Stable range unstable Threshold for unstable to stable change Bit[3:0]: Stable range stable Threshold for stable to unstable change

table 7-21 AWB registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x5186	AWB CONTROL 06	0x10	RW	Bit[7:0]: AWB s
0x5187	AWB CONTROL 07	0x10	RW	Bit[7:0]: AWB ec
0x5188	AWB CONTROL 08	0x10	RW	Bit[7:0]: AWB fc
0x5189	AWB CONTROL 09	0x40	RW	Bit[7:0]: AWB x0
0x518A	AWB CONTROL 10	0x40	RW	Bit[7:0]: AWB y0
0x518B	AWB CONTROL 11	0x00	RW	Bit[7:0]: AWB kx
0x518C	AWB CONTROL 12	0x00	RW	Bit[7:0]: AWB ky
0x518D	AWB CONTROL 13	0x00	RW	Bit[7:0]: Day limit
0x518E	AWB CONTROL 14	0x00	RW	Bit[7:0]: A limit
0x518F	AWB CONTROL 15	0x20	RW	Bit[7:0]: Day split
0x5190	AWB CONTROL 16	0x20	RW	Bit[7:0]: A split
0x5191	AWB CONTROL 17	0xFF	RW	Bit[7:0]: AWB top limit
0x5192	AWB CONTROL 18	0x00	RW	Bit[7:0]: AWB bottom limit
0x5193	AWB CONTROL 19	0xF0	RW	Bit[7:0]: Red limit
0x5194	AWB CONTROL 20	0xF0	RW	Bit[7:0]: Green limit
0x5195	AWB CONTROL 21	0xF0	RW	Bit[7:0]: Blue limit
0x5196	AWB CONTROL 22	0x03	RW	Bit[7:6]: Debug mode Bit[5]: AWB freeze Bit[4]: Debug mode Bit[3:2]: AWB simple selection 00: AWB simple from after AWB gain 01: AWB simple from after RAW GMA 10: AWB simple from after RAW GMA 11: AWB simple from after AWB gain Bit[1]: Fast enable Bit[0]: AWB bias stat
0x5197	AWB CONTROL 23	0x02	RW	Bit[7:0]: Local limit
0x5198	AWB R GAIN MANUAL	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: AWB R gain manual[11:8] Function when 0x5196[7]=1
0x5199	AWB R GAIN MANUAL	0x00	RW	Bit[7:0]: AWB R gain manual[7:0] Function when 0x5196[7]=1
0x519A	AWB G GAIN MANUAL	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: AWB G gain manual[11:8] Function when 0x5196[7]=1

table 7-21 AWB registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x519B	AWB G GAIN MANUAL	0x00	RW	Bit[7:0]: AWB G gain manual[7:0] Function when 0x5196[7]=1
0x519C	AWB B GAIN MANUAL	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: AWB B gain manual[11:8] Function when 0x5196[7]=1
0x519D	AWB B GAIN MANUAL	0x00	RW	Bit[7:0]: AWB B gain manual[7:0] Function when 0x5196[7]=1
0x519E	AWB CONTROL 30	0x00	RW	Bit[7:4]: Debug mode Bit[3]: Local limit select Bit[2]: Simple stable select Bit[1:0]: Debug mode
0x519F	AWB CURRENT R GAIN	–	R	Bit[7:4]: Debug mode Bit[3:0]: Current R setting[11:8]
0x51A0	AWB CURRENT R GAIN	–	R	Bit[7:0]: Current R setting[7:0]
0x51A1	AWB CURRENT G GAIN	–	R	Bit[7:4]: Debug mode Bit[3:0]: Current G setting[11:8]
0x51A2	AWB CURRENT G GAIN	–	R	Bit[7:0]: Current G setting[7:0]
0x51A3	AWB CURRENT B GAIN	–	R	Bit[7:4]: Debug mode Bit[3:0]: Current B setting[11:8]
0x51A4	AWB CURRENT B GAIN	–	R	Bit[7:0]: Current B setting[7:0]
0x51A5	AWB AVERAGE B	–	R	Bit[7:0]: Average R[9:2]
0x51A6	AWB AVERAGE B	–	R	Bit[7:0]: Average G[9:2]
0x51A7	AWB AVERAGE B	–	R	Bit[7:0]: Average B[9:2]
0x51A7	AWB AVERAGE B	–	R	Bit[7:0]: Average b[9:2]
0x51A8	AWB RED SUM	–	R	Bit[7]: R sum[32]
0x51A9	AWB RED SUM	–	R	Bit[7:0]: R sum[31:24]
0x51AA	AWB RED SUM	–	R	Bit[7:0]: R sum[23:16]
0x51AB	AWB RED SUM	–	R	Bit[7:0]: R sum[15:8]
0x51AC	AWB RED SUM	–	R	Bit[7:0]: R sum[7:0]
0x51AD	DEBUG MODE	–	–	Debug Mode
0x51AE	AWB G SUM	–	R	Bit[7]: G sum[32]
0x51AF	AWB G SUM	–	R	Bit[7:0]: G sum[31:24]

table 7-21 AWB registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x51B0	AWB G SUM	–	R	Bit[7:0]: G sum[23:16]
0x51B1	AWB G SUM	–	R	Bit[7:0]: G sum[15:8]
0x51B2	AWB G SUM	–	R	Bit[7:0]: G sum[7:0]
0x51B3	DEBUG MODE	–	–	Debug Mode
0x51B4	AWB B SUM	–	R	Bit[7]: B sum[32]
0x51B5	AWB B SUM	–	R	Bit[7:0]: B sum[31:24]
0x51B6	AWB B SUM	–	R	Bit[7:0]: B sum[23:16]
0x51B7	AWB B SUM	–	R	Bit[7:0]: B sum[15:8]
0x51B8	AWB B SUM	–	R	Bit[7:0]: B sum[7:0]
0x51B9	DEBUG MODE	–	–	Debug Mode
0x51BA	DEBUG MODE	–	–	Debug Mode
0x51BB	AWB A CNT	–	R	Bit[7:6]: Debug mode Bit[5:0]: A count[21:16]
0x51BC	AWB A CNT	–	R	Bit[7:0]: A count[15:8]
0x51BD	AWB A CNT	–	R	Bit[7:0]: A count[7:0]
0x51BE	DEBUG MODE	–	–	Debug Mode
0x51BF	AWB CWF CNT	–	R	Bit[7:6]: Debug mode Bit[5:0]: CWF count[21:16]
0x51C0	AWB CWF CNT	–	R	Bit[7:0]: CWF count[15:8]
0x51C1	AWB CWF CNT	–	R	Bit[7:0]: CWF count[7:0]
0x51C2	DEBUG MODE	–	–	Debug Mode
0x51C3	AWB DAY CNT	–	R	Bit[7:6]: Debug mode Bit[5:0]: Day count[21:16]
0x51C4	AWB DAY CNT	–	R	Bit[7:0]: Day count[15:8]
0x51C5	AWB DAY CNT	–	R	Bit[7:0]: Day count[7:0]
0x51C6	DEBUG MODE	–	–	Debug Mode
0x51C7	AWB ALL CNT	–	R	Bit[7:6]: Debug mode Bit[5:0]: All count[21:16]
0x51C8	AWB ALL CNT	–	R	Bit[7:0]: All count[15:8]
0x51C9	AWB ALL CNT	–	R	Bit[7:0]: All count[7:0]
0x51CA	AWB RED CENTER	–	R	Bit[2:0]: R center[10:8]

table 7-21 AWB registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x51CB	AWB RED CENTER	–	R	Bit[7:0]: R center[7:0]
0x51CC	AWB G CENTER	–	R	Bit[7:3]: Debug mode Bit[2:0]: G center[10:8]
0x51CD	AWB G CENTER	–	R	Bit[7:0]: G center[7:0]
0x51CE	AWB B CENTER	–	R	Bit[7:3]: Debug mode Bit[2:0]: B center[10:8]
0x51CF	AWB B CENTER	–	R	Bit[7:0]: B center[7:0]
0x51D0	AWB CONTROL74	–	R	Bit[7:6]: Debug mode Bit[5]: R large Bit[4]: G large Bit[3]: B large Bit[2:1]: Current type Bit[0]: Debug mode
0x51D1	AWB SRAM CTRL	0x0A	RW	Bit[7:5]: Debug mode Bit[4]: SRAM test Bit[3:0]: SRAM rm

7.22 CIP control [0x5300 - 0x530F]

table 7-22 CIP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5300	CIP SHARPENMT THRESHOLD 1	0x08	RW	Color Interpolation Sharpen MT Threshold 1
0x5301	CIP SHARPENMT THRESHOLD 2	0x48	RW	Color Interpolation Sharpen MT Threshold 2
0x5302	CIP SHARPENMT OFFSET1	0x18	RW	CIP Sharpen MT Offset1 (Y edge mt manual setting when 0x5308[6]=1)
0x5303	CIP SHARPENMT OFFSET2	0x0E	RW	CIP Sharpen MT Offset2
0x5304	CIP DNS THRESHOLD 1	0x08	RW	CIP DNS Threshold 1
0x5305	CIP DNS THRESHOLD 2	0x48	RW	CIP DNS Threshold 2
0x5306	CIP DNS OFFSET1	0x09	RW	CIP DNS Offset1 (DNS threshold manual setting when 0x5308[4]=1)

table 7-22 CIP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5307	CIP DNS OFFSET2	0x16	RW	CIP DNS Offset2
0x5308	CIP CTRL	0x25	RW	Bit[7]: Debug mode Bit[6]: CIP edge MT manual enable Bit[4]: CIP DNS manual enable Bit[2:0]: CIP threshold for BR sharpen
0x5309	CIP SHARPENTH THRESHOLD 1	0x08	RW	CIP Sharpen TH Threshold 1
0x530A	CIP SHARPENTH THRESHOLD 2	0x48	RW	CIP Sharpen TH Threshold 2
0x530B	CIP SHARPENTH OFFSET1	0x04	RW	CIP Sharpen TH Offset1 (Sharpen threshold manual setting when 0x5308[6]=1)
0x530C	CIP SHARPENTH OFFSET2	0x06	RW	CIP Sharpen TH Offset2
0x530D	CIP EDGE MT AUTO	–	R	CIP Edge MT Auto Read
0x530E	CIP DNS THRESHOLD AUTO	–	R	CIP DNS Threshold Auto Read
0x530F	CIP SHARPEN THRESHOLD AUTO	–	R	CIP Sharpen Threshold Auto Read

7.23 CMX control [0x5380 - 0x538B]

table 7-23 CMX control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5380	CMX CTRL	0x00	RW	Bit[7:2]: Debug mode Bit[1]: CMX precision switch 0: 1.7 mode 1: 2.6 mode Bit[0]: Debug mode
0x5381	CMX1	0x20	RW	Bit[7:2]: Debug mode Bit[1]: CMX1 for Y Bit[0]: Debug mode
0x5382	CMX2	0x64	RW	Bit[7:0]: CMX2 for Y
0x5383	CMX3	0x08	RW	Bit[7:0]: CMX3 for Y
0x5384	CMX4	0x30	RW	Bit[7:0]: CMX4 for U

table 7-23 CMX control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5385	CMX5	0x90	RW	Bit[7:0]: CMX5 for U
0x5386	CMX6	0xC0	RW	Bit[7:0]: CMX6 for U
0x5387	CMX7	0xA0	RW	Bit[7:0]: CMX7 for V
0x5388	CMX8	0x98	RW	Bit[7:0]: CMX8 for V
0x5389	CMX9	0x08	RW	Bit[7:0]: CMX9 for V
0x538A	CMXSIGN	0x01	RW	Cmxsign Bit[7:1]: Debug mode Bit[0]: CMX9 sign
0x538B	CMXSIGN	0x98	RW	Cmxsign Bit[7]: CMX8 sign Bit[6]: CMX7 sign Bit[5]: CMX6 sign Bit[4]: CMX5 sign Bit[3]: CMX4 sign Bit[2]: CMX3 sign Bit[1]: CMX2 sign Bit[0]: CMX1 sign

7.24 gamma control [0x5480 - 0x5490]

table 7-24 gamma control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5480	GAMMA CONTROL00	0x00	RW	Bit[7:2]: Debug mode Bit[1]: YSLP15 manual enable Bit[0]: Bias plus on
0x5481	GAMMA YST00	0x26	RW	Bit[7:0]: Y yst 00
0x5482	GAMMA YST01	0x35	RW	Bit[7:0]: Y yst 01
0x5483	GAMMA YST02	0x48	RW	Bit[7:0]: Y yst 02
0x5484	GAMMA YST03	0x57	RW	Bit[7:0]: Y yst 03
0x5485	GAMMA YST04	0x63	RW	Bit[7:0]: Y yst 04
0x5486	GAMMA YST05	0x6E	RW	Bit[7:0]: Y yst 05
0x5487	GAMMA YST06	0x77	RW	Bit[7:0]: Y yst 06
0x5488	GAMMA YST07	0x80	RW	Bit[7:0]: Y yst 07

table 7-24 gamma control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5489	GAMMA YST08	0x88	RW	Bit[7:0]: Y yst 08
0x548A	GAMMA YST09	0x96	RW	Bit[7:0]: Y yst 09
0x548B	GAMMA YST0A	0xA3	RW	Bit[7:0]: Y yst 0A
0x548C	GAMMA YST0B	0xAF	RW	Bit[7:0]: Y yst 0B
0x548D	GAMMA YST0C	0xC5	RW	Bit[7:0]: Y yst 0C
0x548E	GAMMA YST0D	0xD7	RW	Bit[7:0]: Y yst 0D
0x548F	GAMMA YST0E	0xE8	RW	Bit[7:0]: Y yst 0E
0x5490	GAMMA YST0F	0x0F	RW	Bit[7:0]: Y yst 0F

7.25 SDE control [0x5580 - 0x558C]

table 7-25 SDE control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5580	SDE CTRL0	0x00	RW	Bit[7]: Fixed Y enable 0: Disable 1: Enable Bit[6]: Negative enable 0: Disable 1: Enable Bit[5]: Gray enable 0: Disable 1: Enable Bit[4]: Fixed V enable 0: Disable 1: Enable Bit[3]: Fixed U enable 0: Disable 1: Enable Bit[2]: Contrast enable 0: Disable 1: Enable Bit[1]: Saturation enable 0: Disable 1: Enable Bit[0]: Hue enable 0: Disable 1: Enable
0x5581	SDE CTRL1	0x80	RW	Bit[7:0]: Hue cos coefficient

table 7-25 SDE control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5582	SDE CTRL2	0x00	RW	Bit[7:0]: Hue sin coefficient
0x5583	SDE CTRL3	0x40	RW	Bit[7:0]: Saturation U when 0x5580[1]=1 and 0x5588[6]=1, max value for UV adjust when 0x5580[1]=1 and 0x5588[6]=0 or fixed U when 0x5580[3]=1
0x5584	SDE CTRL4	0x40	RW	Bit[7:0]: Saturation V when 0x5580[1]=1 and 0x5588[6]=1, min value for UV adjust when 0x5580[1]=1 and 0x5588[6]=0 or Vreg when 0x5580[4]=1
0x5585	SDE CTRL5	0x00	RW	Bit[7:0]: Y offset for contrast when 0x5044[3]=1; or fixed Y when 0x5580[7]=1
0x5586	SDE CTRL6	0x20	RW	Bit[7:0]: Y gain for contrast
0x5587	SDE CTRL7	0x00	RW	Bit[7:0]: Y bright for contrast
0x5588	SDE CTRL8	0x01	RW	Bit[7]: Debug mode Bit[5]: Sign5 for hue V, cos Bit[4]: Sign4 for hue U, cos Bit[3]: Sign3 Y bright sign for contrast 0: Keep Y bright sign 1: Negative Y bright sign Bit[2]: Sign2 Y offset sign for contrast when 0x5044[3]=1 0: Keep Y offset sign 1: Negative Y offset sign Bit[1]: Sign1 for hue V, sin Bit[0]: Sign0 for hue U, sin
0x5589	SDE CTRL9	0x01	RW	Bit[7:0]: UV adjust threshold 1 Valid when 0x5580[1]=1
0x558A	SDE CTRL10	0x01	RW	Bit[7:1]: Debug mode Bit[0]: UV adjust threshold 2[8] Valid when 0x5580[1]=1
0x558B	SDE CTRL11	0xFF	RW	Bit[7:0]: UV adjust threshold 2[7:0] Valid when 0x5580[1]=1
0x558C	SDE CTRL12	–	R	Bit[7:0]: UV adjust value read out

7.26 scale control [0x5600 - 0x5606]

table 7-26 scale registers

address	register name	default value	R/W	description
0x5600	SCALE CTRL 0	0x10	RW	Bit[7:6]: Debug mode Bit[5]: UV drop YUV444 to 422 drop mode vs. AVG mode select 0: AVG mode 1: Drop mode Bit[4]: Debug mode Bit[3]: Hround DCW hrounding 0: No horizontal rounding 1: Horizontal rounding Bit[2]: Hdrop DCW drop mode 0: Horizontal average mode 1: Horizontal drop mode Bit[1]: Vround DCW vrounding 0: No vertical rounding 1: Vertical rounding Bit[0]: Vdrop DCW drop mode 0: Vertical average mode 1: Vertical drop mode
0x5601	SCALE CTRL 1	0x00	RW	Bit[7]: Debug mode Bit[6:4]: HDIV RW DCW scale times 000: DCW 1 time 001: DCW 2 time 010: DCW 4 time 011: DCW 8 time 1xx: DCW 16 time Bit[2:0]: VDIV RW DCW scale times 000: DCW 1 time 001: DCW 2 time 010: DCW 4 time 011: DCW 8 time 1xx: DCW 16 time
0x5602	SCALE CTRL 2	0x02	RW	Bit[7:0]: XSC[15:8]
0x5603	SCALE CTRL 3	0x00	RW	Bit[7:0]: XSC[7:0]
0x5604	SCALE CTRL 4	0x02	RW	Bit[7:0]: YSC[15:8]
0x5605	SCALE CTRL 5	0x00	RW	Bit[7:0]: YSC[7:0]
0x5606	SCALE CTRL 6	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Voffset

7.27 AVG control [0x5680 - 0x56A2]

table 7-27 AVG registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5680	X START	0x00	RW	Bit[7:5]: Debug mode Bit[4:0]: X start[11:8] Horizontal start position for average window high byte, valid when 0x501D[4]=1
0x5681	X START	0x00	RW	Bit[7:0]: X start[7:0] Horizontal start position for average window low byte, valid when 0x501D[4]=1
0x5682	Y START	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: Y start[10:8] Vertical start position for average window low byte, valid when 0x501D[4]=1
0x5683	Y START	0x00	RW	Bit[7:0]: Y start[7:0] Vertical start position for average window low byte, valid when 0x501D[4]=1
0x5684	X WINDOW	0x10	RW	Bit[7:4]: Debug mode Bit[3:0]: Window X[11:8] Horizontal end position for average window high byte, valid when 0x501D[4]=1
0x5685	X WINDOW	0xA0	RW	Bit[7:0]: Window X[7:0] Horizontal end position for average window low byte, valid when 0x501D[4]=1
0x5686	Y WINDOW	0x0C	RW	Bit[7:3]: Debug mode Bit[2:0]: Window Y[10:8] Vertical end position for average window high byte, valid when 0x501D[4]=1
0x5687	Y WINDOW	0x78	RW	Bit[7:0]: Window Y[7:0] Vertical end position for average window low byte, valid when 0x501D[4]=1
0x5688	WEIGHT00	0x11	RW	Bit[7:4]: Window 01 weight Bit[3:0]: Window 00 weight
0x5689	WEIGHT01	0x11	RW	Bit[7:4]: Window 03 weight Bit[3:0]: Window 02 weight
0x568A	WEIGHT02	0x11	RW	Bit[7:4]: Window 11 weight Bit[3:0]: Window 10 weight
0x568B	WEIGHT03	0x11	RW	Bit[7:4]: Window 13 weight Bit[3:0]: Window 12 weight
0x568C	WEIGHT04	0x11	RW	Bit[7:4]: Window 21 weight Bit[3:0]: Window 20 weight

table 7-27 AVG registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x568D	WEIGHT05	0x11	RW	Bit[7:4]: Window 23 weight Bit[3:0]: Window 22 weight
0x568E	WEIGHT06	0x11	RW	Bit[7:4]: Window 31 weight Bit[3:0]: Window 30 weight
0x568F	WEIGHT07	0x11	RW	Bit[7:4]: Window 33 weight Bit[3:0]: Window 32 weight
0x5690	AVG CTRL10	0x01	RW	Bit[7:1]: Debug mode Bit[0]: AVG option 0: Sum = (4*B+9*G*2+10*R)/8 1: Sum = (B+G*2+R)
0x5691	AVG WIN 00	–	R	Bit[7:0]: Average of win 00
0x5692	AVG WIN 01	–	R	Bit[7:0]: Average of win 01
0x5693	AVG WIN 02	–	R	Bit[7:0]: Average of win 02
0x5694	AVG WIN 03	–	R	Bit[7:0]: Average of win 03
0x5695	AVG WIN 10	–	R	Bit[7:0]: Average of win 10
0x5696	AVG WIN 11	–	R	Bit[7:0]: Average of win 11
0x5697	AVG WIN 12	–	R	Bit[7:0]: Average of win 12
0x5698	AVG WIN 13	–	R	Bit[7:0]: Average of win 13
0x5699	AVG WIN 20	–	R	Bit[7:0]: Average of win 20
0x569A	AVG WIN 21	–	R	Bit[7:0]: Average of win 21
0x569B	AVG WIN 22	–	R	Bit[7:0]: Average of win 22
0x569C	AVG WIN 23	–	R	Bit[7:0]: Average of win 23
0x569D	AVG WIN 30	–	R	Bit[7:0]: Average of win 30
0x569E	AVG WIN 31	–	R	Bit[7:0]: Average of win 31
0x569F	AVG WIN 32	–	R	Bit[7:0]: Average of win 32
0x56A0	AVG WIN 33	–	R	Bit[7:0]: Average of win 33
0x56A1	AVG READOUT	–	R	Bit[7:0]: High 8 bits of average value
0x56A2	AVG WEIGHT SUM	–	R	Bit[7:0]: Average weight sum

7.28 DPC control [0x5780 - 0x57FF]

table 7-28 CMX control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5780	DPC CTRL00	0x1C	RW	DPC Control (0: disable; 1: enable) Bit[7]: Tail enable Bit[6]: sat enable Bit[5]: Cluster enable Bit[4]: Same color channel enable Bit[3]: Different color channel enable Bit[2]: Smooth enable Bit[1]: Black/white sensor mode enable Bit[0]: Man mode enable
0x5781	DPC CTRL01	0x13	RW	Bit[7:5]: Debug mode Bit[4]: Color line enable Bit[3:2]: Debug mode Bit[1:0]: Edge option 00: Padding 10 01: Padding 1FFF 10: Padding 13FF 11: Padding 2 pixel on the left and right edge
0x5782	DPC VNUM	0x03	RW	Bit[7:2]: Debug mode Bit[1:0]: Maximum number of the relating defect pixel in vertical line
0x5783	DPC WTHRE	0x08	RW	Bit[7]: Debug mode Bit[6:0]: Threshold value for detecting white pixel
0x5784	DPC BTHRE	0x20	RW	Bit[7]: Debug mode Bit[6:0]: Threshold value for detecting black pixel
0x5785	DPC THRE1	0x10	RW	Bit[7]: Debug mode Bit[6:0]: Used in recovery Used to select the normal pixel during recovery
0x5786	DPC THRE2	0x08	RW	Bit[7]: Debug mode Bit[6:0]: Used in recovery
0x5787	DPC THRE3	0x10	RW	Bit[7:0]: Used in check-below module
0x5788	DPC THRE4	0x10	RW	Bit[7]: Debug mode Bit[6:0]: Used in detection
0x5789	DPC WTHRE LIST0	0x08	RW	Bit[7]: Debug mode Bit[6:0]: List for white pixel threshold calculation

table 7-28 CMX control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x578A	DPC WTHRE LIST1	0x04	RW	Bit[7]: Debug mode Bit[6:0]: List for white pixel threshold calculation
0x578B	DPC WTHRE LIST2	0x02	RW	Bit[7]: Debug mode Bit[6:0]: List for white pixel threshold calculation
0x578C	DPC WTHRE LIST3	0x02	RW	Bit[7]: Debug mode Bit[6:0]: List for white pixel threshold calculation
0x578D	DPC BTHRE LIST0	0x0C	RW	Bit[7]: Debug mode Bit[6:0]: List for black pixel threshold calculation
0x578E	DPC BTHRE LIST1	0x06	RW	Bit[7]: Debug mode Bit[6:0]: List for black pixel threshold calculation
0x578F	DPC BTHRE LIST2	0x02	RW	Bit[7]: Debug mode Bit[6:0]: List for black pixel threshold calculation
0x5790	DPC BTHRE LIST3	0x02	RW	Bit[7]: Debug mode Bit[6:0]: List for black pixel threshold calculation
0x5791	DPC SAT	0xFF	RW	Bit[7:0]: DPC sat
0x57A0	DPC READ 0	–	R	Bit[7:2]: Debug mode Bit[1:0]: Color smooth
0x57A1	DPC READ 1	–	R	Bit[7]: Debug mode Bit[6:0]: White threshold read
0x57A2	DPC READ 2	–	R	Bit[7]: Debug mode Bit[6:0]: Black threshold read
0x57A3	DPC READ 3	–	R	Bit[7]: Debug mode Bit[6:0]: Threshold1 read
0x57A4	DPC READ 4	–	R	Bit[7:0]: Threshold2 read
0x57A5	DPC READ 5	–	R	Bit[7:0]: Threshold3 read
0x57A6	DPC READ 6	–	R	Bit[7]: Debug mode Bit[6:0]: Threshold4 read

7.29 LENC control [0x5800 - 0x5849]

table 7-29 LENC control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5800	GMTRX00	0x10	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 00
0x5801	GMTRX01	0x10	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 01
0x5802	GMTRX02	0x10	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 02
0x5803	GMTRX03	0x10	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 03
0x5804	GMTRX04	0x10	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 04
0x5805	GMTRX05	0x10	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 05
0x5806	GMTRX10	0x10	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 06
0x5807	GMTRX11	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 07
0x5808	GMTRX12	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 08
0x5809	GMTRX13	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 09
0x580A	GMTRX14	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 0A
0x580B	GMTRX15	0x10	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 0B
0x580C	GMTRX20	0x10	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 0C
0x580D	GMTRX21	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 0D
0x580E	GMTRX22	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 0E
0x580F	GMTRX23	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 0F
0x5810	GMTRX24	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 10

table 7-29 LENC control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x5811	GMTRX25	0x10	RW	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 11
0x5812	GMTRX30	0x10	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 12
0x5813	GMTRX31	0x08	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 13
0x5814	GMTRX32	0x00	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 14
0x5815	GMTRX33	0x00	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 15
0x5816	GMTRX34	0x08	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 16
0x5817	GMTRX35	0x10	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 17
0x5818	GMTRX40	0x10	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 18
0x5819	GMTRX41	0x08	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 19
0x581A	GMTRX42	0x08	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 1A
0x581B	GMTRX43	0x08	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 1B
0x581C	GMTRX44	0x08	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 1C
0x581E	GMTRX45	0x10	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 1D
0x581E	GMTRX50	0x10	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 1E
0x581F	GMTRX51	0x10	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 1F
0x5820	GMTRX52	0x10	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 20
0x5821	GMTRX53	0x10	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 21
0x5822	GMTRX54	0x10	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 22
0x5823	GMTRX55	0x10	R/W	Bit[7:6]: Debug mode Bit[5:0]: Green matrix 23

table 7-29 LENC control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x5824	BRMATRX00	0xAA	R/W	Bit[7:4]: Blue matrix 00 Bit[3:0]: Red matrix 00
0x5825	BRMATRX01	0xAA	RW	Bit[7:4]: Blue matrix 01 Bit[3:0]: Red matrix 01
0x5826	BRMATRX02	0xAA	RW	Bit[7:4]: Blue matrix 02 Bit[3:0]: Red matrix 02
0x5827	BRMATRX03	0xAA	RW	Bit[7:4]: Blue matrix 03 Bit[3:0]: Red matrix 03
0x5828	BRMATRX04	0xAA	RW	Bit[7:4]: Blue matrix 04 Bit[3:0]: Red matrix 04
0x5829	BRMATRX05	0xAA	RW	Bit[7:4]: Blue matrix 05 Bit[3:0]: Red matrix 05
0x582A	BRMATRX06	0x99	RW	Bit[7:4]: Blue matrix 06 Bit[3:0]: Red matrix 06
0x582B	BRMATRX07	0x99	RW	Bit[7:4]: Blue matrix 07 Bit[3:0]: Red matrix 07
0x582C	BRMATRX08	0x99	RW	Bit[7:4]: Blue matrix 08 Bit[3:0]: Red matrix 08
0x582D	BRMATRX09	0xAA	RW	Bit[7:4]: Blue matrix 09 Bit[3:0]: Red matrix 09
0x582E	BRMATRX20	0xAA	RW	Bit[7:4]: Blue matrix 20 Bit[3:0]: Red matrix 20
0x582F	BRMATRX21	0x99	RW	Bit[7:4]: Blue matrix 21 Bit[3:0]: Red matrix 21
0x5830	BRMATRX22	0x88	RW	Bit[7:4]: Blue matrix 22 Bit[3:0]: Red matrix 22
0x5831	BRMATRX23	0x99	RW	Bit[7:4]: Blue matrix 23 Bit[3:0]: Red matrix 23
0x5832	BRMATRX24	0xAA	RW	Bit[7:4]: Blue matrix 24 Bit[3:0]: Red matrix 24
0x5833	BRMATRX30	0xAA	RW	Bit[7:4]: Blue matrix 30 Bit[3:0]: Red matrix 30
0x5834	BRMATRX31	0x99	RW	Bit[7:4]: Blue matrix 31 Bit[3:0]: Red matrix 31
0x5835	BRMATRX32	0x99	RW	Bit[7:4]: Blue matrix 32 Bit[3:0]: Red matrix 32
0x5836	BRMATRX33	0x99	RW	Bit[7:4]: Blue matrix 33 Bit[3:0]: Red matrix 33

table 7-29 LENC control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x5837	BRMATRX34	0xAA	RW	Bit[7:4]: Blue matrix 34 Bit[3:0]: Red matrix 34
0x5838	BRMATRX40	0xAA	R/W	Bit[7:4]: Blue matrix 40 Bit[3:0]: Red matrix 40
0x5839	BRMATRX41	0xAA	R/W	Bit[7:4]: Blue matrix 41 Bit[3:0]: Red matrix 41
0x583A	BRMATRX42	0xAA	R/W	Bit[7:4]: Blue matrix 42 Bit[3:0]: Red matrix 42
0x583B	BRMATRX43	0xAA	R/W	Bit[7:4]: Blue matrix 43 Bit[3:0]: Red matrix 43
0x583C	BRMATRX44	0xAA	R/W	Bit[7:4]: Blue matrix 44 Bit[3:0]: Red matrix 44
0x583D	LENC BR OFFSET	0x88	R/W	Bit[7:4]: LENC b offset Bit[3:0]: LENC r offset
0x583E	MAX GAIN	0x40	R/W	Bit[7:0]: Maximum gain
0x583F	MIN GAIN	0x20	R/W	Bit[7:0]: Minimum gain
0x5840	MIN Q	0x18	R/W	Bit[7]: Debug mode Bit[6:0]: Minimum Q
0x5841	LENC CTRL59	0x0D	R/W	Bit[7:4]: Debug mode Bit[3]: Add BLC enable 0: Disable BLC add back function 1: Enable BLC add back function Bit[2]: BLC enable 0: Disable BLC function 1: Enable BLC function Bit[1]: Gain manual enable Bit[0]: Auto Q enable 0: Used constant Q (0x40) 1: Used calculated Q
0x5842	BR HSCALE	0x01	RW	Bit[7:3]: Debug mode Bit[2:0]: br h scale[10:8] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5843	BR HSCAL	0x2B	RW	Bit[7:0]: br h scale[7:0] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block

table 7-29 LENC control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x5844	BR VSCALE	0x01	RW	Bit[7:3]: Debug mode Bit[2:0]: br v scale[10:8] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5845	BR VSCALE	0x8D	RW	Bit[7:0]: br v scale[7:0] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x5846	G HSCALE	0x01	RW	Bit[7:3]: Debug mode Bit[2:0]: g h scale[10:8] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5847	G HSCAL	0x8F	RW	Bit[7:0]: g h scale[7:0] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5848	G VSCALE	0x01	RW	Bit[7:3]: Debug mode Bit[2:0]: g v scale[10:8] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5849	G VSCALE	0x09	RW	Bit[7:0]: g v scale[7:0] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5850	LENC READOUT	–	R	LENC X Offset
0x5851	LENC READOUT	–	R	LENC X Offset
0x5852	LENC READOUT	–	R	LENC Y Offset
0x5853	LENC READOUT	–	R	LENC Y Offset

table 7-29 LENC control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x5854	LENC READOUT	–	R	Bit[7:6]: Debug mode Bit[5]: Flip Bit[4]: Mirror Bit[3:2]: Y skip Bit[1:0]: X skip
0x5855	LENC READOUT	–	R	Bit[7:4]: Debug mode Bit[3]: Overflow gh Bit[2]: Overflow brh Bit[1]: Overflow gv Bit[0]: Overflow brv
0x5856	LENC READOUT	–	R	LENC m nq

7.30 AFC control [0x6000 - 0x603F]

table 7-30 AFC control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x6000	AFC CTRL00	0xFF	RW	AFC Control 00 Bit[7:5]: Debug mode Bit[4]: Edge filter enable 0: afc_edge module will not update 1: afc_edge module will update Bit[3]: Edge filter b select Edge b filters select 0: Edge selects b2 1: Edge selects b1 Bit[2:0]: Edge filter a select Edge a filters select 001: Edge selects a1 010: Edge selects a2 100: Edge selects a4 101: Edge selects a5
0x6001	AFC CTRL01	0xFF	RW	AFC Control 01 Bit[7:0]: Edge window0 left This window coordinate Others: Edge selects a1
0x6002	AFC CTRL02	0xFF	RW	AFC Control 02 Bit[7:0]: Edge window0 top This window coordinate

table 7-30 AFC control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x6003	AFC CTRL03	0xFF	RW	AFC Control 03 Bit[7:0]: Edge window0 right This window coordinate
0x6004	AFC CTRL04	0xFF	RW	AFC Control 04 Bit[7:0]: Edge window0 bottom This window coordinate This bottom must be larger than any other
0x6005	AFC CTRL05	0xFF	RW	AFC Control 05 Bit[7:0]: Edge window1 left This window coordinate
0x6006	AFC CTRL06	0xFF	RW	AFC Control 06 Bit[7:0]: Edge window1 top This window coordinate
0x6007	AFC CTRL07	0xFF	RW	AFC Control 07 Bit[7:0]: Edge window1 right This window coordinate
0x6008	AFC CTRL08	0xFF	RW	AFC Control 08 Bit[7:0]: Edge window1 bottom This window coordinate
0x6009	AFC CTRL09	0xFF	RW	AFC Control 09 Bit[7:0]: Edge window2 left This window coordinate
0x600A	AFC CTRL10	0xFF	RW	AFC Control 10 Bit[7:0]: Edge window2 top This window coordinate
0x600B	AFC CTRL11	0xFF	RW	AFC Control 11 Bit[7:0]: Edge window2 right This window coordinate
0x600C	AFC CTRL12	0xFF	RW	AFC Control 12 Bit[7:0]: Edge window2 bottom This window coordinate
0x600D	AFC CTRL13	0xFF	RW	AFC Control 13 Bit[7:0]: Edge window3 left This window coordinate
0x600E	AFC CTRL14	0xFF	RW	AFC Control 14 Bit[7:0]: Edge window3 top This window coordinate
0x600F	AFC CTRL15	0xFF	RW	AFC Control 15 Bit[7:0]: Edge window3 right This window coordinate

table 7-30 AFC control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x6010	AFC CTRL16	0xFF	RW	AFC Control 16 Bit[7:0]: Edge window3 bottom This window coordinate
0x6011	AFC CTRL17	0xFF	RW	AFC Control 17 Bit[7:0]: Edge window4 left This window coordinate
0x6012	AFC CTRL18	0xFF	RW	AFC Control 18 Bit[7:0]: Edge window4 top This window coordinate
0x6013	AFC CTRL19	0xFF	RW	AFC Control 19 Bit[7:0]: Edge window4 right This window coordinate
0x6014	AFC CTRL20	0xFF	RW	AFC Control 20 Bit[7:0]: Edge window4 bottom This window coordinate
0x6015	AFC CTRL21	–	R	AFC Control 21 Bit[7:6]: Debug mode Bit[5:0]: Window0 filter a[29:24]
0x6016	AFC CTRL22	–	R	AFC Control 22 Bit[7:0]: Window0 filter a[23:16]
0x6017	AFC CTRL23	–	R	AFC Control 23 Bit[7:0]: Window0 filter a[15:8]
0x6018	AFC CTRL24	–	R	AFC Control 24 Bit[7:0]: Window0 filter a[7:0]
0x6019	AFC CTRL25	–	R	AFC Control 25 Bit[7:6]: Debug mode Bit[5:0]: Window0 filter b[29:24]
0x601A	AFC CTRL26	–	R	AFC Control 26 Bit[7:0]: Window0 filter b[23:16]
0x601B	AFC CTRL27	–	R	AFC Control 27 Bit[7:0]: Window0 filter b[15:8]
0x601C	AFC CTRL28	–	R	AFC Control 28 Bit[7:0]: Window0 filter b[7:0]
0x601D	AFC CTRL29	–	R	AFC Control 29 Bit[7:6]: Debug mode Bit[5:0]: Window1 filter a[29:24]
0x601E	AFC CTRL30	–	R	AFC Control 30 Bit[7:0]: Window1 filter a[23:16]
0x601F	AFC CTRL31	–	R	AFC Control 31 Bit[7:0]: Window1 filter a[15:8]

table 7-30 AFC control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x6020	AFC CTRL32	–	R	AFC Control 32 Bit[7:0]: Window1 filter a[7:0]
0x6021	AFC CTRL33	–	R	AFC Control 33 Bit[7:6]: Debug mode Bit[5:0]: Window1 filter b[29:24]
0x6022	AFC CTRL34	–	R	AFC Control 34 Bit[7:0]: Window1 filter b[23:16]
0x6023	AFC CTRL35	–	R	AFC Control 35 Bit[7:0]: Window1 filter b[15:8]
0x6024	AFC CTRL36	–	R	AFC Control 36 Bit[7:0]: Window1 filter b[7:0]
0x6025	AFC CTRL37	–	R	AFC Control 37 Bit[7:6]: Debug mode Bit[5:0]: Window2 filter a[29:24]
0x6026	AFC CTRL38	–	R	AFC Control 38 Bit[7:0]: Window2 filter a[23:16]
0x6027	AFC CTRL39	–	R	AFC Control 39 Bit[7:0]: Window2 filter a[15:8]
0x6028	AFC CTRL40	–	R	AFC Control 40 Bit[7:0]: Window2 filter a[7:0]
0x6029	AFC CTRL41	–	R	AFC Control 41 Bit[7:6]: Debug mode Bit[5:0]: Window2 filter b[29:24]
0x602A	AFC CTRL42	–	R	AFC Control 42 Bit[7:0]: Window2 filter b[23:16]
0x602B	AFC CTRL43	–	R	AFC Control 43 Bit[7:0]: Window2 filter b[15:8]
0x602C	AFC CTRL44	–	R	AFC Control 44 Bit[7:0]: Window2 filter b[7:0]
0x602D	AFC CTRL45	–	R	AFC Control 45 Bit[7:6]: Debug mode Bit[5:0]: Window3 filter a[29:24]
0x602E	AFC CTRL46	–	R	AFC Control 46 Bit[7:0]: Window3 filter a[23:16]
0x602F	AFC CTRL47	–	R	AFC Control 47 Bit[7:0]: Window3 filter a[15:8]
0x6030	AFC CTRL48	–	R	AFC Control 48 Bit[7:0]: Window3 filter a[7:0]

table 7-30 AFC control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x6031	AFC CTRL49	–	R	AFC Control 49 Bit[7:6]: Debug mode Bit[5:0]: Window3 filter b[29:24]
0x6032	AFC CTRL50	–	R	AFC Control 50 Bit[7:0]: Window3 filter b[23:16]
0x6033	AFC CTRL51	–	R	AFC Control 51 Bit[7:0]: Window3 filter b[15:8]
0x6034	AFC CTRL52	–	R	AFC Control 52 Bit[7:0]: Window3 filter b[7:0]
0x6035	AFC CTRL53	–	R	AFC Control 53 Bit[7:6]: Debug mode Bit[5:0]: Window4 filter a[29:24]
0x6036	AFC CTRL54	–	R	AFC Control 54 Bit[7:0]: Window4 filter a[23:16]
0x6037	AFC CTRL55	–	R	AFC Control 55 Bit[7:0]: Window4 filter a[15:8]
0x6038	AFC CTRL56	–	R	AFC Control 56 Bit[7:0]: Window4 filter a[7:0]
0x6039	AFC CTRL57	–	R	AFC Control 57 Bit[7:6]: Debug mode Bit[5:0]: Window4 filter b[29:24]
0x603A	AFC CTRL58	–	R	AFC Control 58 Bit[7:0]: Window4 filter b[23:16]
0x603B	AFC CTRL59	–	R	AFC Control 59 Bit[7:0]: Window4 filter b[15:8]
0x603C	AFC CTRL60	–	R	AFC Control 60 Bit[7:0]: Window4 filter b[7:0]
0x603D	AFC READ58	–	R	AFC Read 58 Bit[7:0]: Window4 filter b[23:16]
0x603R	AFC READ59	–	R	AFC Read 59 Bit[7:0]: Window4 filter b[15:8]
0x603F	AFC READ60	–	R	AFC Read 60 Bit[7:0]: Window4 filter b[7:0]

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +95°C
supply voltage (with respect to ground)[b]	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		±200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

b. for negative voltage with respect to ground, V_{DD-A} (-4.5V), V_{DD-C} (-3V), V_{DD-IO} (-4.5V)

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +70°C junction temperature
stable image temperature[b]	0°C to +50°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-30°C < T_J < 70°C) (sheet 1 of 2)

symbol	parameter	min	typ	max	unit
power supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}[a]	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.71	1.8	3.0	V
internal DVDD short to DVDD, DVP output, AVDD = 2.8V, DOVDD = 2.8V					
I_{DD-A}	operating current 2592 x 1944 @ 15 fps		TBD	TBD	mA
I_{DD-DO}			TBD	TBD	mA
I_{DD-A}	operating current 1080p @ 30 fps		TBD	TBD	mA
I_{DD-DO}			TBD	TBD	mA
I_{DD-A}	operating current 720p @ 60 fps		TBD	TBD	mA
I_{DD-DO}			TBD	TBD	mA
I_{DD-A}	operating current 720 @ 30 fps YUV		TBD	TBD	mA
I_{DD-DO}			TBD	TBD	mA
I_{DD-A}	operating current VGA @ 30 fps		TBD	TBD	mA
I_{DD-DO}			TBD	TBD	mA
internal DVDD, EVDD short to DVDD, MIPI output, AVDD = 2.8V, DOVDD = 1.8V					
I_{DD-A}	operating current 2592 x 1944 @ 15 fps		TBD	TBD	mA
I_{DD-DO}			TBD	TBD	mA
I_{DD-A}	operating current 2592 x 1944 @ 15 fps YUV		TBD	TBD	mA
I_{DD-DO}			TBD	TBD	mA
I_{DD-A}	operating current 1080p @ 30 fps		TBD	TBD	mA
I_{DD-DO}			TBD	TBD	mA
I_{DD-A}	operating current 1080p @ 30 fps YUV		TBD	TBD	mA
I_{DD-DO}			TBD	TBD	mA
I_{DD-A}	operating current 720 @ 30 fps YUV		TBD	TBD	mA
I_{DD-DO}			TBD	TBD	mA

table 8-3 DC characteristics (-30°C < T_J < 70°C) (sheet 2 of 2)

symbol	parameter	min	typ	max	unit
external DVDD, EVDD short to DVDD, DVP output, AVDD = 2.8V, DOVDD = 2.8V					
I_{DD-A}	operating current 2592 x 1944 @ 15 fps		TBD	TBD	mA
I_{DD-D}			TBD	TBD	mA
I_{DD-DO}			TBD	TBD	mA
standby current					
$I_{DDS-SCCB}$	standby current[b]		20	50	µA
$I_{DDS-PWDNB}$			20	50	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs[c]					
V_{IL}	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}	SIOC and SIOD	1.26	1.8	3.0	V

a. using the internal DVDD regulator is strongly recommended for minimum power down current

b. standby current is based on room temperature

c. based on DOVDD = 1.8V.

8.4 AC characteristics

table 8-4 AC characteristics (T_A = 25°C, V_{DD-A} = 2.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		30		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	settling time for hardware reset			<1	ms
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-5 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)[a]	6	24	54	MHz
t_r, t_f	clock input rise/fall time[b]			5 (10[c])	ns

a. for input clock range 6~27 MHz, the OV5645 can tolerate input clock period jitter up to 1ns peak-to-peak, for input clock range to 54MHz, the OV5645 can tolerate input clock period jitter up to 500ps peak-to-peak

b. if the PLL is bypassed, the delay from input clock to output clock is approximately 4~5 ns

c. if using the internal PLL

figure 8-1 SCCB interface timing

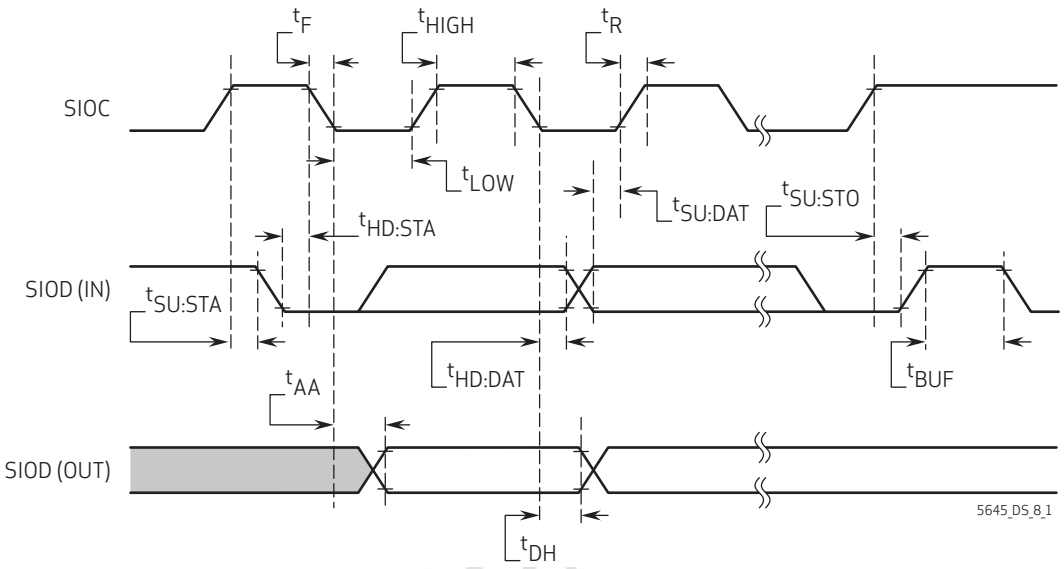


table 8-6 SCCB interface timing specifications[a]

symbol	parameter	min	typ	max	unit
f_{SIOC}	clock frequency			400	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SIOC low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400kHz mode

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

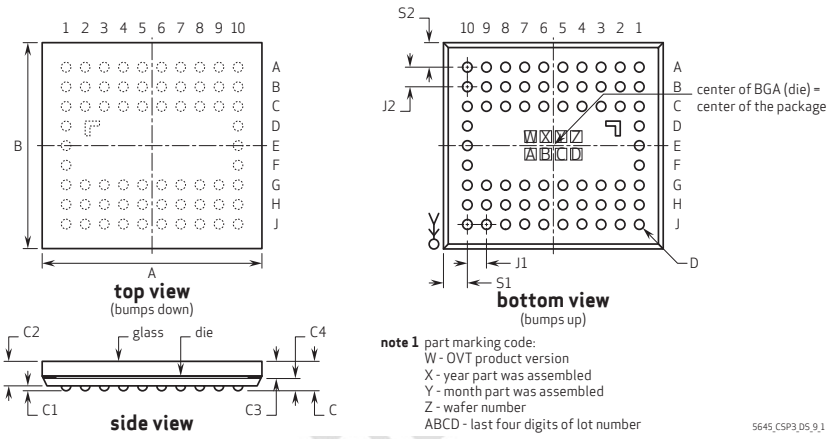


table 9-1 package dimensions

parameter	symbol	min	typ	max	unit
package body dimension x	A	6175	6200	6225	µm
package body dimension y	B	4835	4860	4885	µm
package height	C	700	760	820	µm
ball height	C1	100	130	160	µm
package body thickness	C2	585	630	675	µm
cover glass thickness	C3	425	445	465	µm
image plane height	C4	260	315	370	µm
ball diameter	D	220	250	280	µm
total pin count	N		66 (10 NC)		
pin count x-axis	N1		10		
pin count y-axis	N2		9		
pins pitch x-axis	J1		600		µm
pins pitch y-axis	J2		500		µm
edge-to-pin center distance analog x	S1	370	400	430	µm
edge-to-pin center distance analog y	S2	400	430	460	µm

9.2 IR reflow specifications

note
The OV5645 uses a lead-free package.

figure 9-2 IR reflow ramp rate requirements

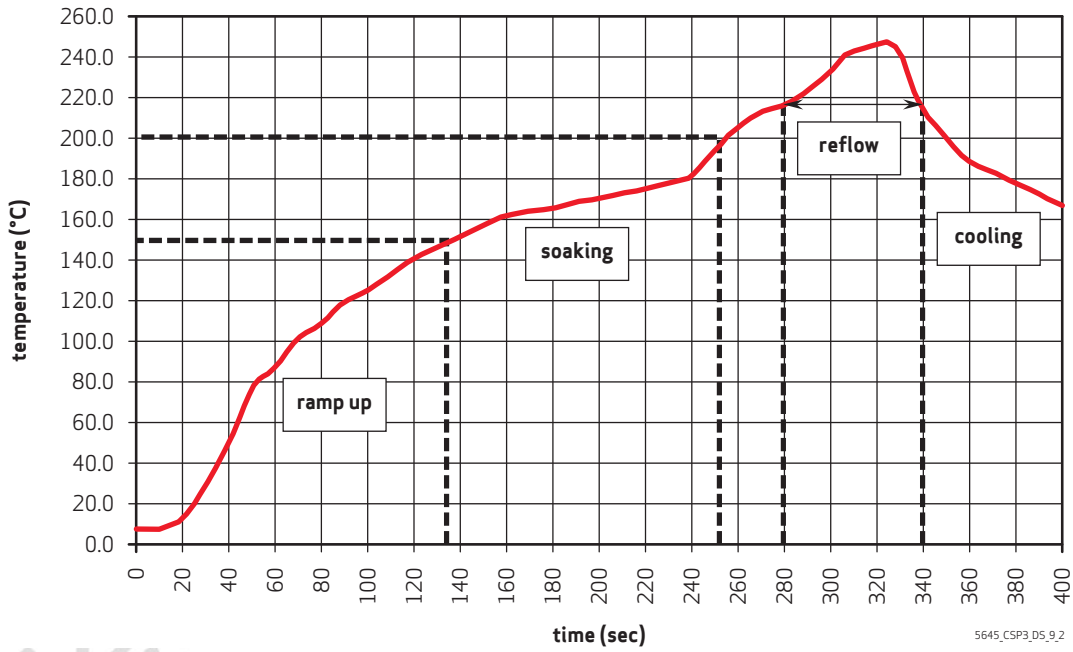


table 9-2 reflow conditions[ab]

zone	description	exposure
ramp up	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
reflow	temperature higher than 217°C	30 ~ 120 seconds
peak	maximum temperature in SMT	245°C
cooling	cooling from 217°C to room temperature	temperature slope ≤ 6°C per second

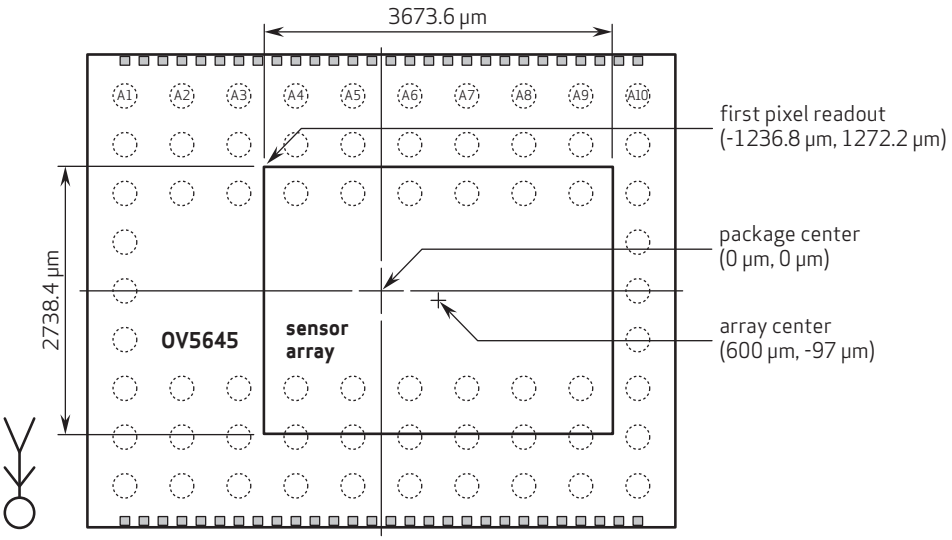
a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM<500 as recommendation

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A10 oriented down on the PCB.

5645_CSP3_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

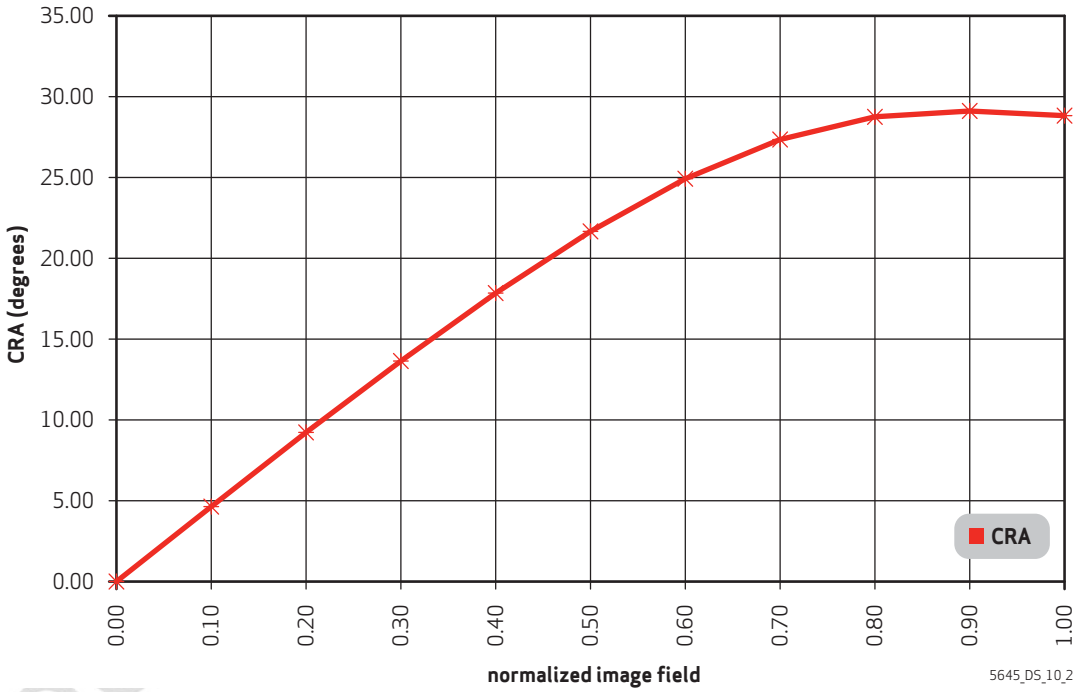


table 10-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0.00		0.00
0.10		4.6
0.20		9.2
0.30		13.7
0.40		17.8
0.50		21.7
0.60		24.9
0.70		27.3
0.80		28.7
0.90		29.1
1.00		28.9

revision history

version 1.0 06.07.2012

- initial release

version 1.1 07.17.2012

- changed all instances of PWDN to PWDNB throughout entire datasheet
- in table 1-1, changed pin description for pin A7 to" GPIO port 1", pin B6 to" GPIO port 3" and pin A7 to "GPIO port 2
- on page i, under key specifications, added "RGB565/555/444, YUV422/420, YCbCr422" to output formats
- in section 2, updated figures 2-1 and 2-4
- in section 2.7.1, changed list number two description from "...active high..." to "...active low..., list number three description "...must go high..." to "...must be low...", list number four from "...to go low..." to "...to go high..." and added "System needs to drive PWNDB to high as the sensor has an internal pull down on PWDNB pin"
- in section 2.7.2, changed list number three description from "...is active high...must go high..." to "...is active low...must be low...", list number four description from "...to go low..." to "...to go high..." and added "System needs to drive PWNDB to high as the sensor has an internal pull down on PWDNB pin"
- in section 2.9, changed section description from "...pad must be tied to high...pin is set to high..." to "...pad must be tied to low...pin is set to low..." in first sentence of second paragraph
- in section 4.11, removed "FAE used" from last sentence of section description
- in sub-section 4.11.1, changed "3D10" to "3D20" in seventh line of code
- in sub-section 4.11.2, changed "0x3D05" to "0x3D00" in second sentence of section description
- in section 5.2, changed third sentence of section description to "The LENC calculation is based on sensor gain and therefore automatically adjusts with sensor gain"
- in section 5.3, added "and advanced" to second sentence and changed "Advance" to "Advanced" in third sentence of section description
- in table 8-5, removed row for symbol f_{PCLK}

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