

Product Specification

- ❖ Product Name: AMOLED
- ❖ Model Name: DO0143FAT01
- ❖ Description: 1.43 inch (466 x 466)

Proposed by			Customer's Approval
Designed	Checked	Approved	

Document Revision History

Rev. No.	Date	Contents	Remark
0.0	2023-08-30	-Initial issue	Preliminary

1.General Description:

- Driving Mode: Active Matrix.
- Color Mode: Full Color (65K/262K/16.7M color)
- Display Format: 1.43" (466 x 466)
- Display Driver IC : SH8601 or Compatible
- Touch Driver IC : FT3268 or Compatible
- Display Interface: SPI 3-wire/ SPI 4-wire/QSPI/I8080-8Bits/MIPI-DSI 1Lane
- Touch Interface: IIC [Slave Addr A[6:0]---0X38]
- Application: Handheld & PDA
- RoHS Compatible

2.Mechanical Data

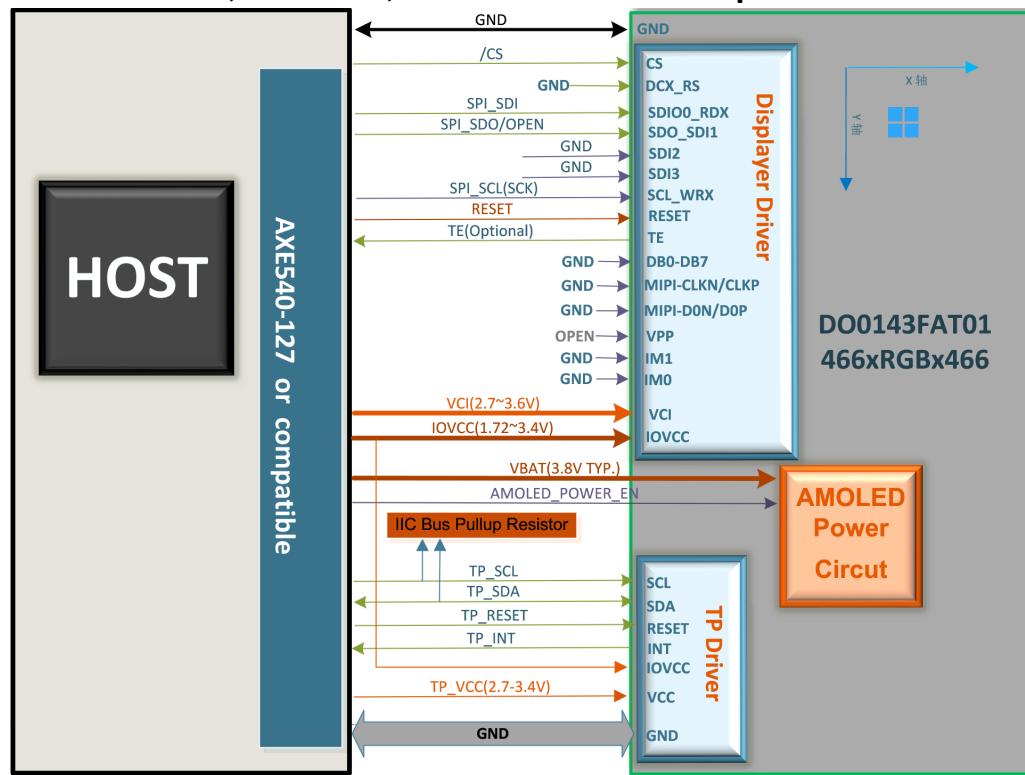
Item	Specification	unit
Display Mode	AMOLED	-
Dimensional outline [Without Cover Lens]	39.15(W) x 39.3(H) x0.8 (T)	mm
Number of dots	466(W) x RGB x 466(H)	dots
Active area	36.35(W) x 36.35(H)	mm
Diagonal Inch	1.43	inch
Pixel pitch	78*78	μm
Weight	TBD	g

*See attached drawing for details.

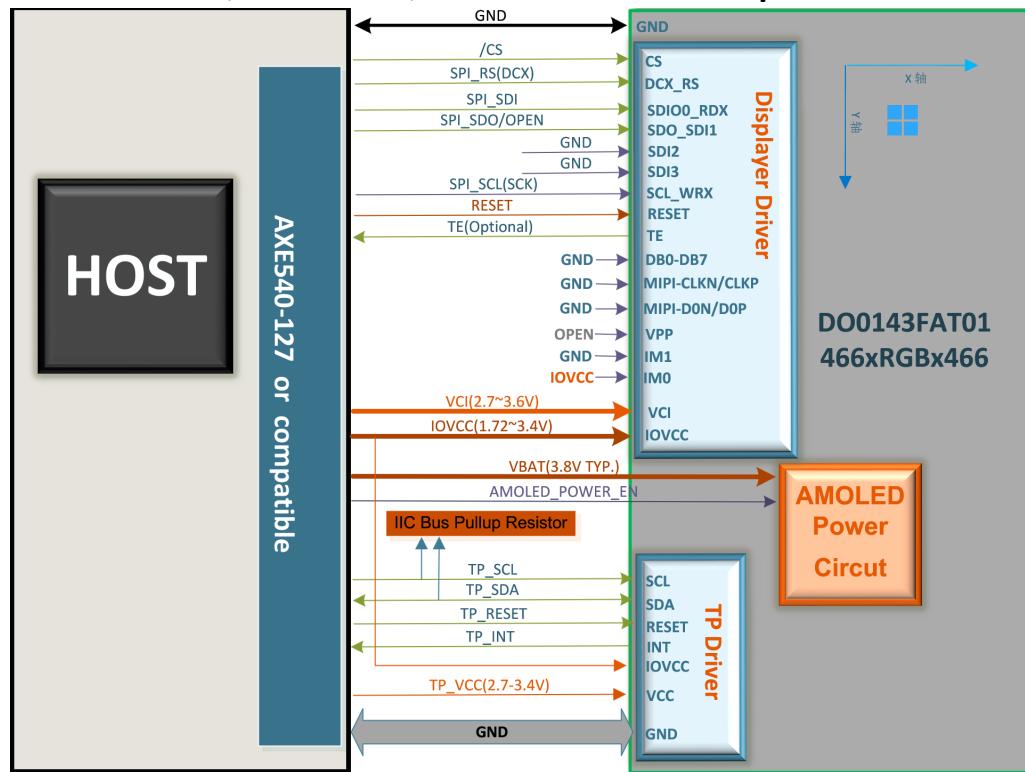
3. Block Diagram

DO0143FAT01 support various interfaces, and interfaces are selected by the IM[1:0] pins.

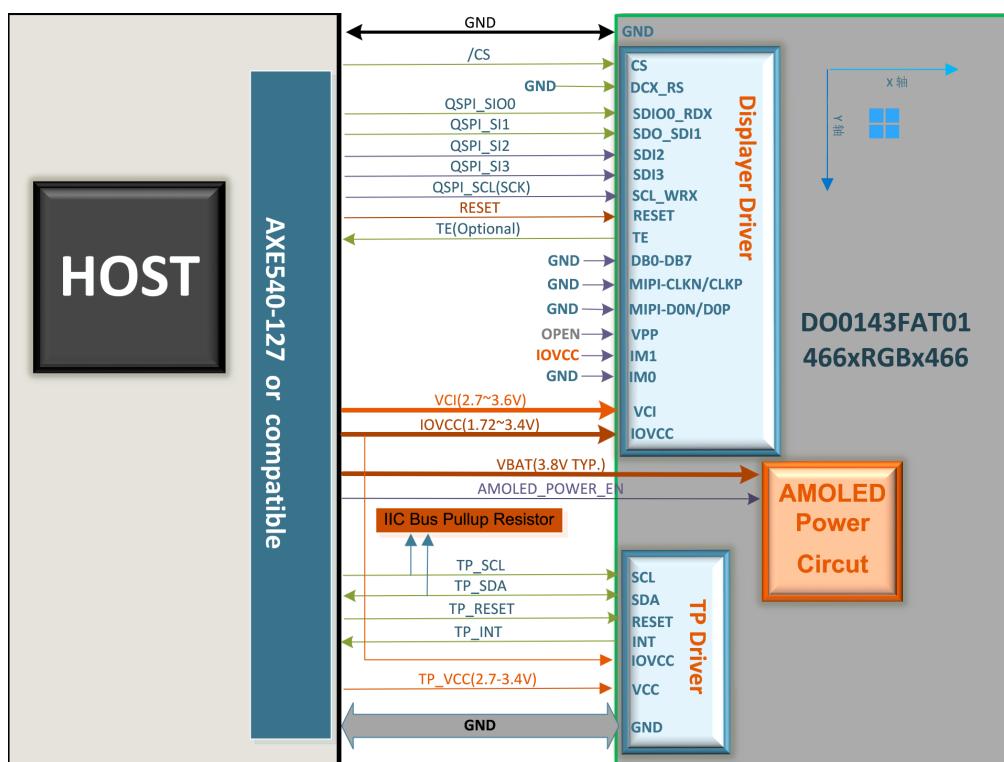
A: If IM1=GND,IM0=GND, DO0143FAT01 set to **spi-3wire interface**



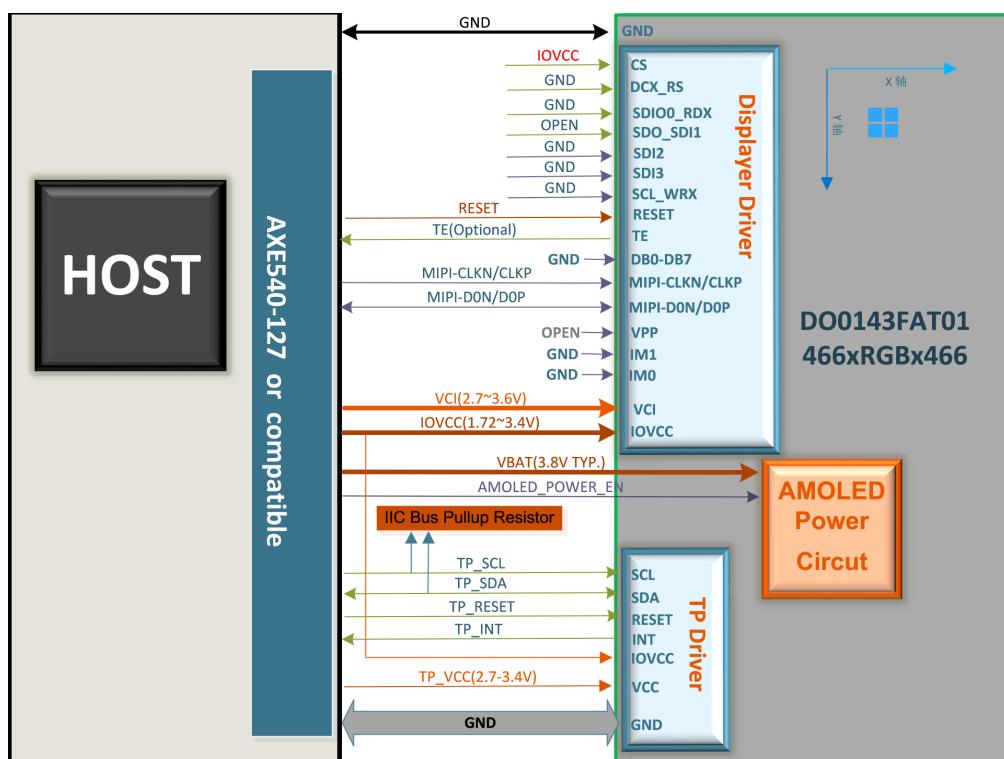
B: If IM1=GND,IM0=IOVCC, DO0143FAT01 set to **spi-4wire interface**



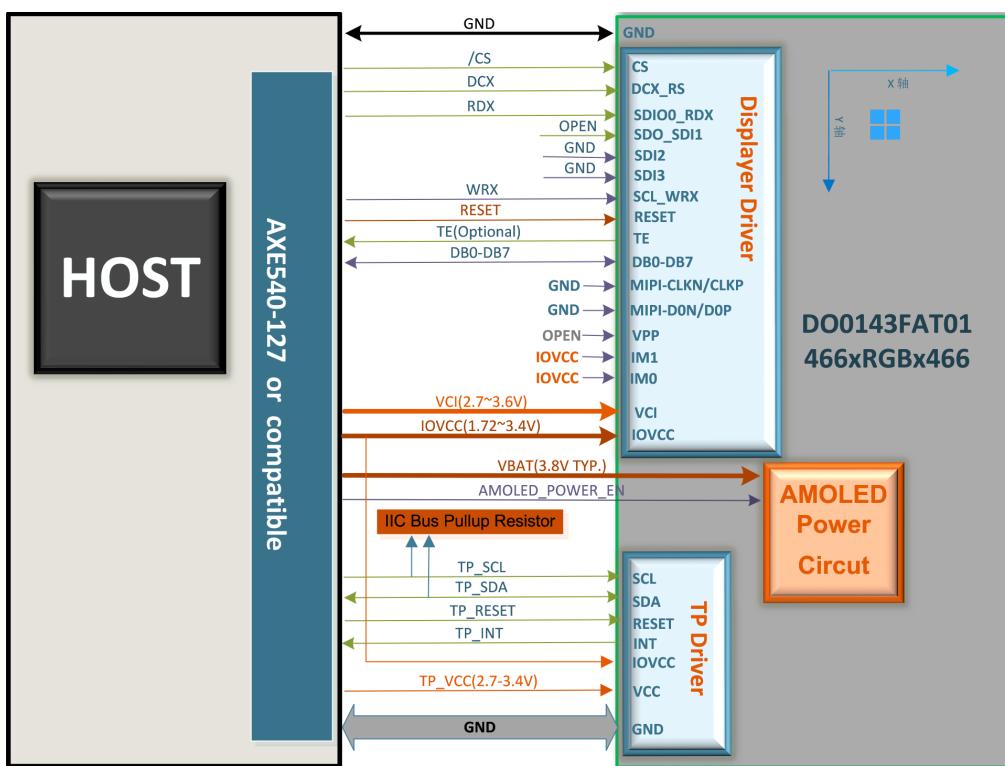
C: If IM1=IOVCC,IM0=GND, DO0143FAT01 set to QSPI interface



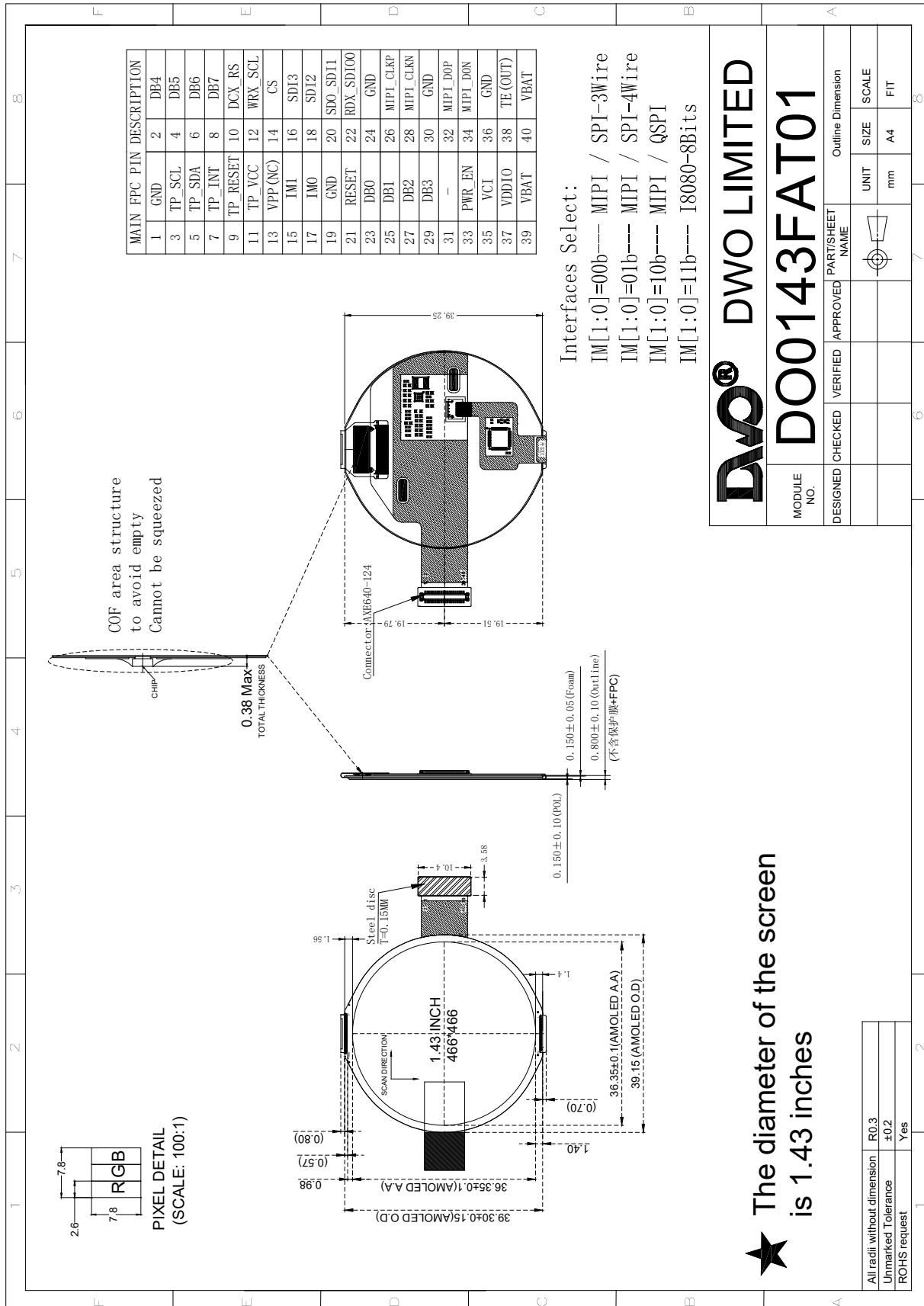
D: If IM1=GND,IM0=GND, CS=IOVCC, DO0143FAT01 set to MIPI-DSI interface



E: If IM1=IOVCC,IM0=IOVCC, DO0143FAT01 set to I8080-8Bits



4.Dimension



5.Pin Description

Recomend Connector : AXE540-127.(AXE640124 on AMOLED)

NO.	Pin Name	I/O	Description
1	GND	P	Ground Terminal
3	TP_SCL	I	Touch Panel Clock Input. Communication Voltage follow IOVCC If not used, please open this pin.
5	TP_SDA	I/O	Touch Panel Data Input and output. Communication Voltage follow IOVCC If not used, , please open this pin.
7	TP_INT	O	Touch Panel Interrupt Output. If not used, please open this pin.
9	TP_RESET	I	TP Reset signal Input. Communication Voltage follow IOVCC If not used, , please open this pin.
11	TP_VCC	P	Analog Voltage for TP Driver (2.7~3.4V)
13	VPP(NC)	P	OTP Power Supply(Let it open).
15	IM1	I	Interface type selection
17	IM0	I	Interface type selection
19	GND	P	Ground Terminal
21	RESET	I	AMOLED Reset signal Input
23	DB0	I/O	Bi-directional data bus for 80-series MPU I/F [LSB]
25	DB1	I/O	Bi-directional data bus for 80-series MPU I/F
27	DB2	I/O	Bi-directional data bus for 80-series MPU I/F
29	DB3	I/O	Bi-directional data bus for 80-series MPU I/F
31	NC	-	No connected
33	PWR_EN	I	Power IC enable control pin.
35	VCI_IN	P	Analog Voltage for Display Driver (2.7~3.6V)
37	VDDIO(IOVCC)	P	Driver IC(Touch + Display) Digital I/O Power Supply(1.72~3.4V)
39	VBAT	P	Battery Voltage 3.8V TYP. (2.9-4.5V)
NO.	Pin Name	I/O	Description
2	DB4	I/O	Bi-directional data bus for 80-series MPU I/F
4	DB5	I/O	Bi-directional data bus for 80-series MPU I/F
6	DB6	I/O	Bi-directional data bus for 80-series MPU I/F
8	DB7	I/O	Bi-directional data bus for 80-series MPU I/F [MSB]
10	DCX_RS	I	Display data / command selection in 80-series MPU I/F and SPI

			4-wire I/F. D/CX = "0" : Command; D/CX = "1" : Display data or Parameter
12	WRX_SCL	I	WRX : Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F.
14	CS	I	Chip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F. If not used(MIPI Interface), please connect these pin to IOVCC.
16	SDI3	I	Serial Data Input in QSPI,data Lane 3. If not used, please connect these pins to GND.
18	SDI2	I	Serial Data Input in QSPI,data Lane 2. If not used, please connect these pins to GND.
20	SDO_SDI1	I/O	Serial Data Input in QSPI,data Lane 2. Serial Data Output in SPI_3Wire/ SPI_4Wire Data Input Signal at Dual Input Mode. If not used, please connect these pins to GND.
22	RDX_SDIO0	I/O	Serial Data Input in QSPI,data Lane 0. Serial Data intput in SPI_3Wire/ SPI_4Wire Data Input Signal at Dual Input Mode. RDX : Reads strobe signal to write data when RDX is "Low" in 80-series MPU interface. If not used, please connect these pins to GND.
24	GND	P	Ground Terminal
26	MIPI_CLKP	I	Differential clock signals if MIPI interface. If not used, please connect these pins to GND.
28	MIPI_CLKN	I	Differential clock signals if MIPI interface. If not used, please connect these pins to GND.
30	GND	P	Ground Terminal
32	MIPI_DOP	I/O	Differential data signals if MIPI interface. If not used, please connect these pins to GND.
34	MIPI_DON	I/O	Differential data signals if MIPI interface. If not used, please connect these pins to GND.
36	GND	P	Ground Terminal
38	TE	O	Tearing Effect
40	VBAT	P	Battery Voltage 3.8V TYP. (2.9-4.5V)

6. DC Characteristics

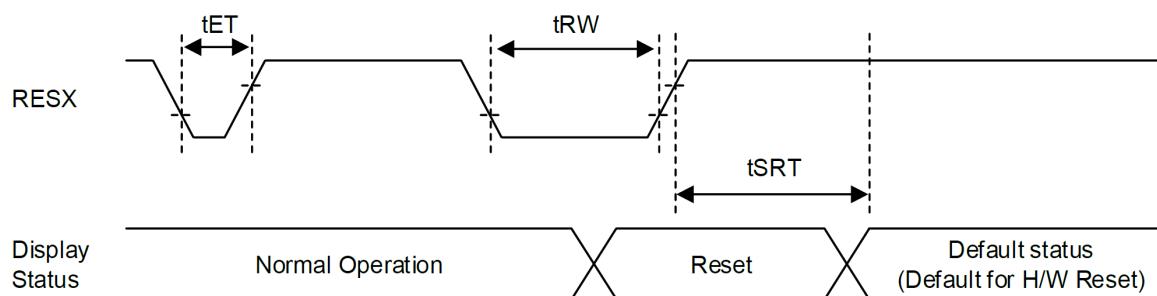
Test Conditions :Voltage Referenced to VSS=0V, IOVCC = 1.8V, VCC=3.3V,VBAT=3.3V,TA = 25°C
Unless otherwise specified

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Supply voltage (Display)	VCC			2.7	3.3	3.6	V
	IOVCC			1.65	1.8	3.3	V
	ELVDD	-		2.9	3.8	4.5	V
Input voltage	'L' level	VIL	IOVCC=1.65V ~3.3V	GND	-	0.2*IOVCC	V
	'H' level	VIH		0.8*IOVCC	-	IOVCC	V
Output voltage	'L' level	VOL	I(OH)=-1mA I(OL)=+1mA	GND	-	0.2*IOVCC	V
	'H' level	VOH		0.8*IOVCC	-	IOVCC	V
Current (Display)	Sleep out mode	I _{VCC}	Full white display, 350nits,	-	2.2	-	mA
		I _{IOVCC}		-	1.9	-	mA
		I _{VBAT}		-	55	-	mA
	Sleep in mode	I _{VCC}		-	30	50	uA
		I _{IOVCC}		-	50	100	uA
		I _{VBAT}		-	50	TBD	uA
	Deep Standby Mode	I _{VCC}		-	2	3	uA
		I _{IOVCC}		-	2	3	uA
		I _{VBAT}		-	50	TBD	uA
Frame Frequency		f _{FRM}		-	45	-	Hz

7.AC characteristics

7-1 Reset Timing

Reset timing characteristic



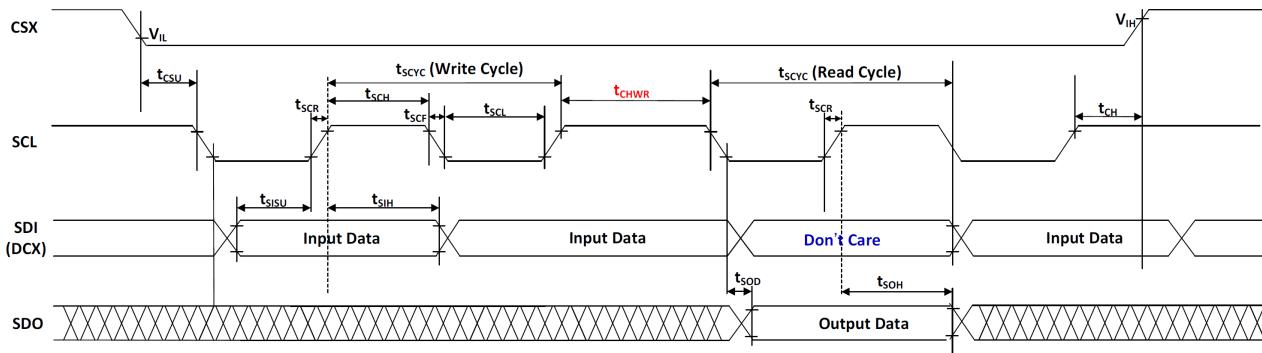
VSS=0V, VDDIO=1.7V to 3.3V, VCI=2.5V to 3.3V, Ta = -30 to 70°C

Parameter	Symbol	Pad	Min.	Typ.	Max.	Unit	Note
Reset low pulse width	tRW	RESX	10	—	—	μs	—
Secure reset completion time	tSRT	RESX	—	—	5	ms	Reset during Sleep In mode
		RESX	—	—	150		Reset during Sleep Out mode
Reset un-reacted pulse width	tET	RESX			5	μs	—

7-2 SPI Timing

SPI-3Wire/ SPI-4Wire Interface Characteristics

3/4-wire SPI

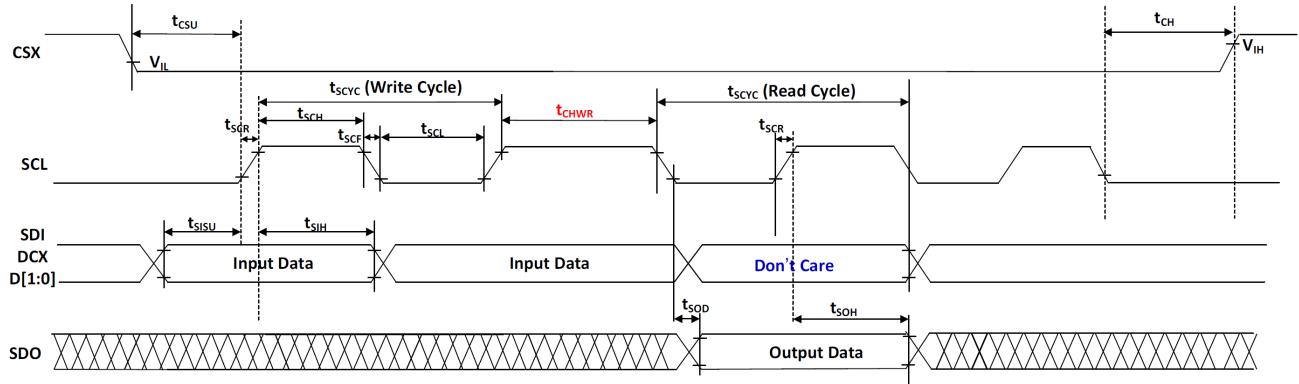


Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock cycle	t _{SCYC}	Write	20			ns
		Read	300			ns
Clock high pulse width	t _{SCH}	Write	6.5			ns
		Read	140			ns
Clock low pulse width	t _{SCL}	Write	6.5			ns
		Read	140			ns
Clock rise time	t _{SCR}	0.2*VDDI -> 0.8*VDDI			3.5	ns
Clock fall time	t _{SCF}	0.8*VDDI -> 0.2*VDDI			3.5	ns
Chip select setup time	t _{CSU}		10			ns
Chip select hold time	t _{CH}		10			ns
Data input setup time	t _{SISU}	To V _{IL} of SCL's rising edge	5			ns
Data input hold time	t _{SIH}		5			ns
Access time of output data	t _{SOD}	From V _{IL} of SCL's falling edge			120	ns
Hold time of output data	t _{SOH}	From V _{IH} of SCL's rising edge	5			ns
Transition time from Write cycle to Read cycle	t _{CHWR}	From V _{IH} of SCL's rising edge	150			ns

Notes:

- (1) Logic high and low levels are specified as 80% and 20% of VDDI for Input signals.
- (2) For the 4-wire SPI, the DCX's timing is the same as input data.
- (3) Ta = -30°C to 70°C, VDDI=1.65V to 3.3V, VCI=2.7V to 3.6V, and VSS=0V

7-3 QSPI Interface Characteristics



Note: The max SCL frequency for each pixel data format is specified as the below table.

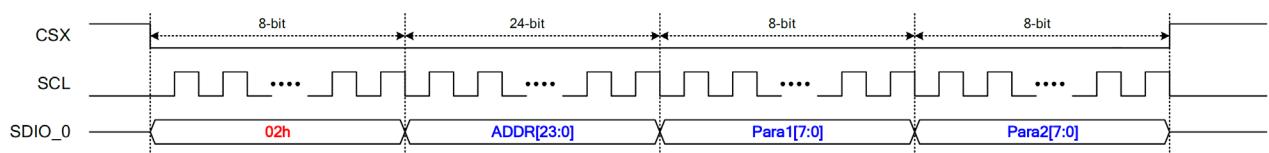
Note: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

Note: $T_a = -30$ to 70 °C, VDDI=1.65V to 3.3V, VCI=2.7V to 3.6V, GND=0V

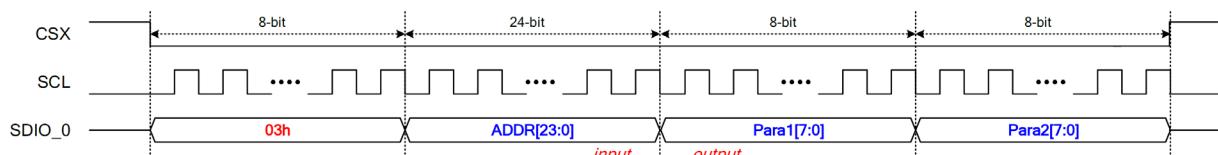
QSPI Timing

Quad SPI Interface Protocol – Register Read and Write

Command Write

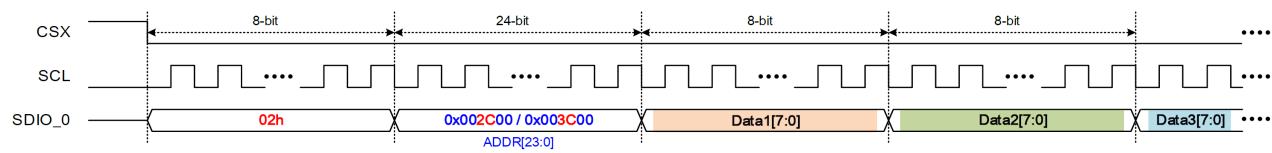


Command Read

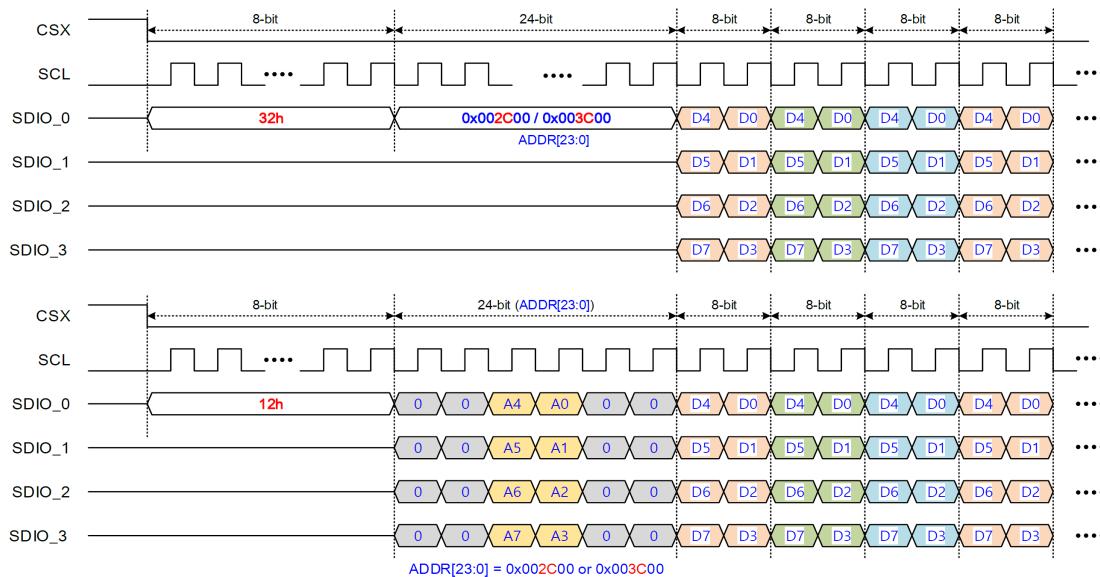


Quad SPI Interface Protocol – Pixel Interface

1-Wire Pixel Write

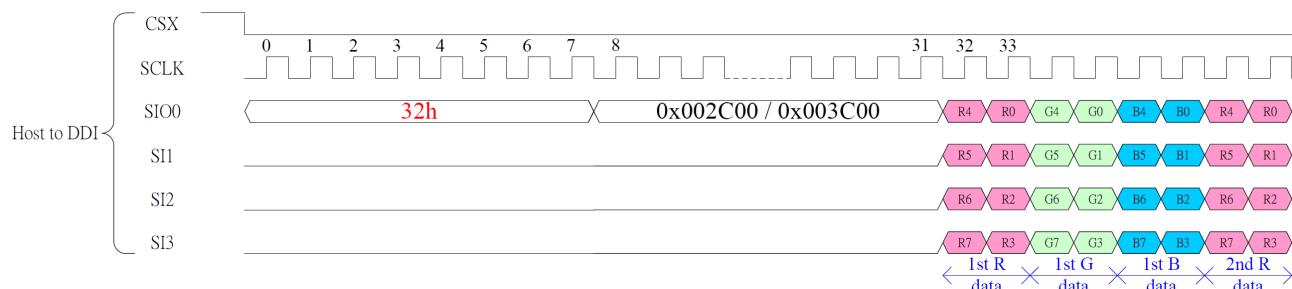


4-Wire Pixel Write

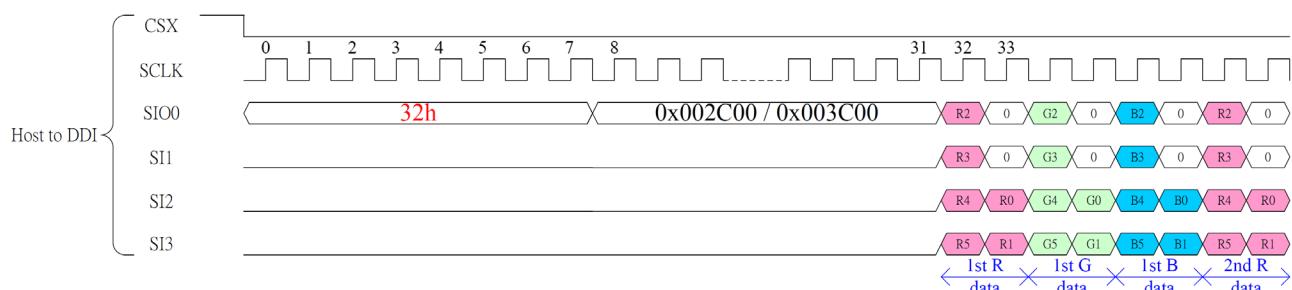


SPI-4Lanes Pixel Write Data Waveform

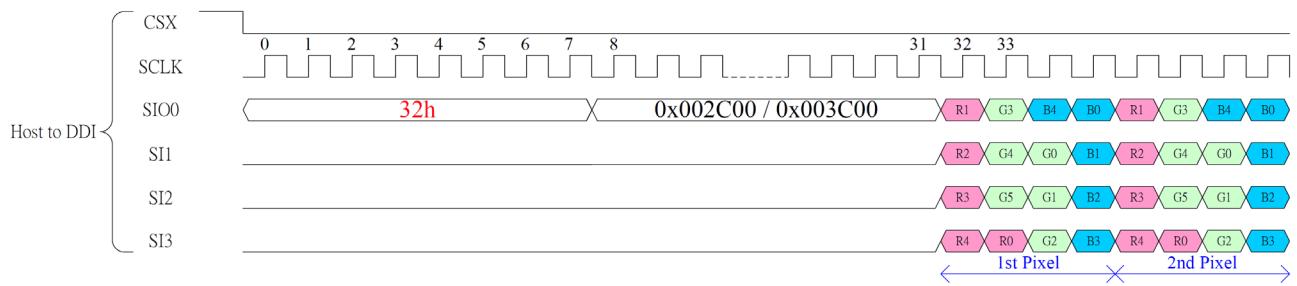
RGB888 – 4-Lanes



RGB666 – 4-Lanes

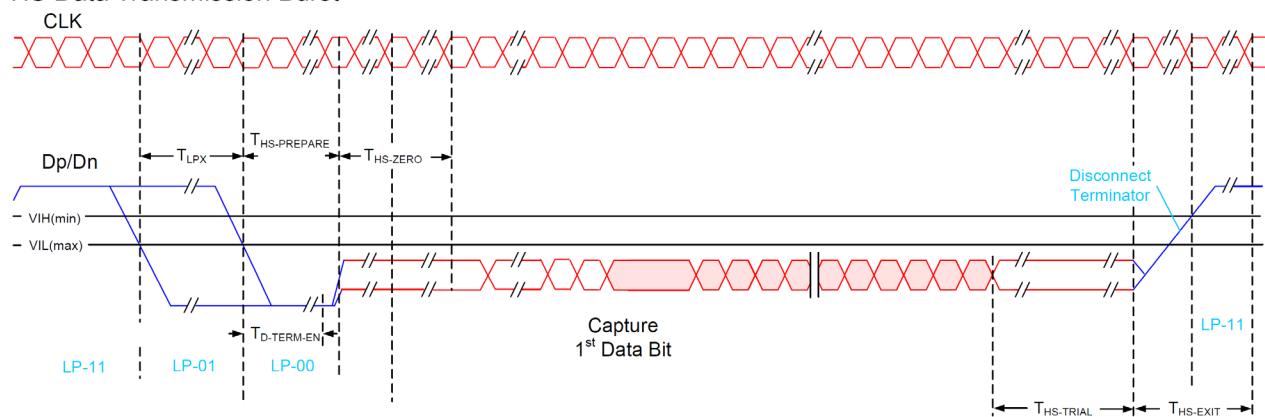


RGB565 – 4-Lanes

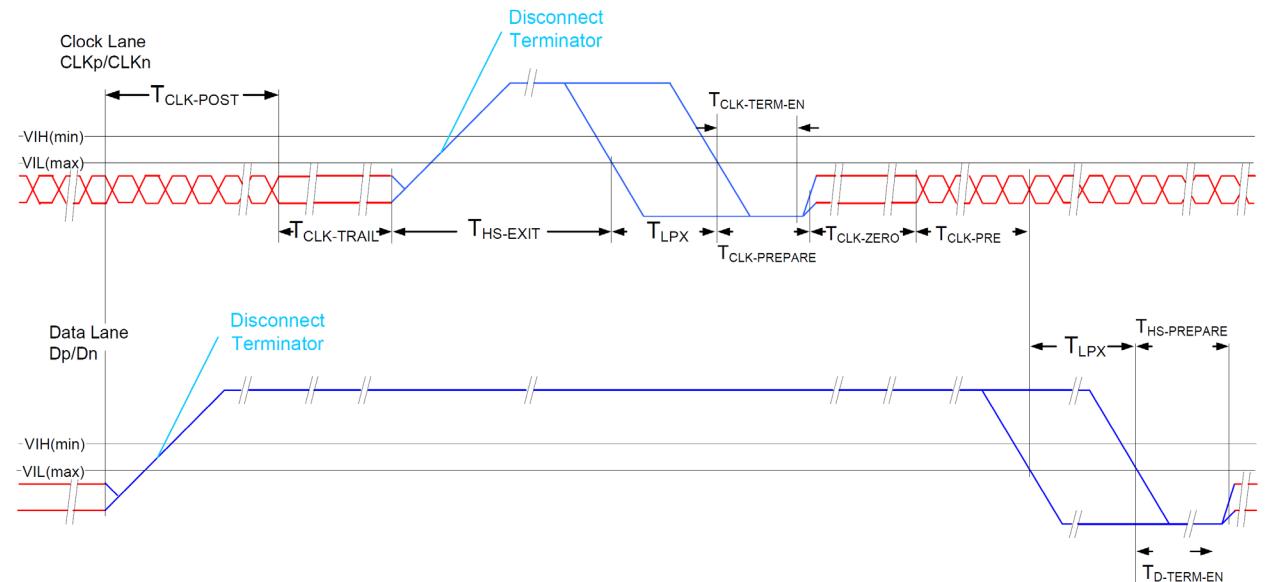


7-4 MIPI-DSI 1 lane Interface Characteristics

HS Data Transmission Burst



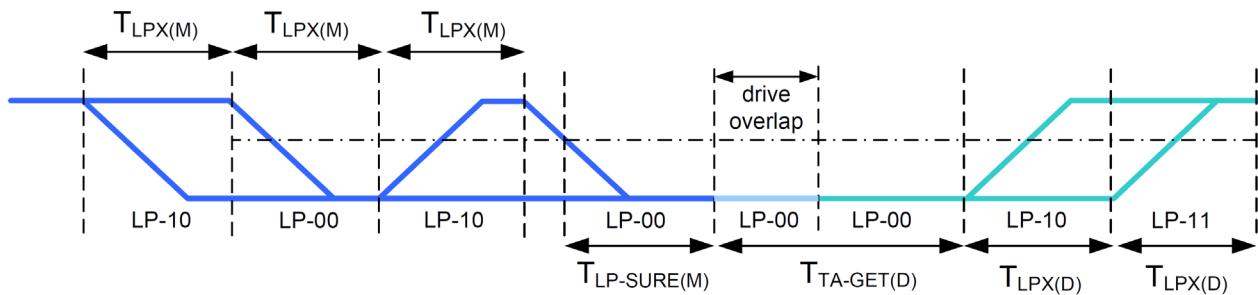
HS clock transmission



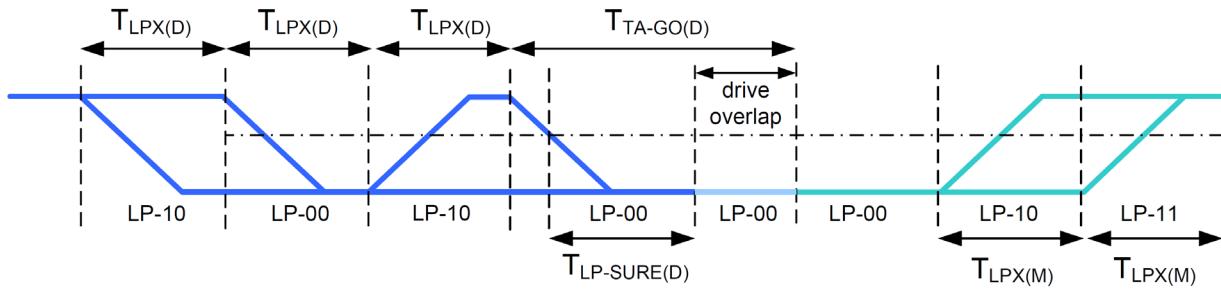
Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns + 4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE} + \text{time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.}$	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

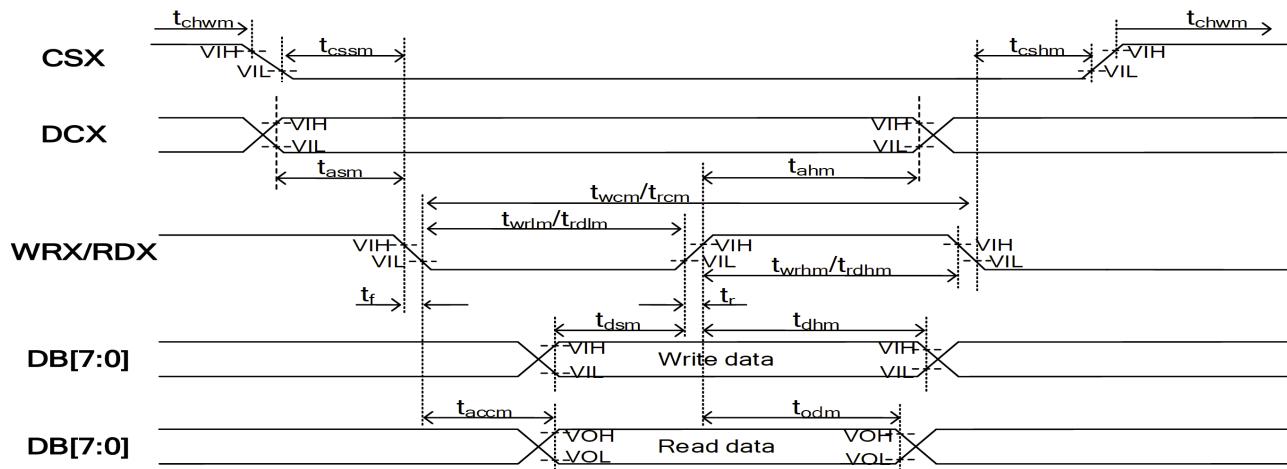
Low Power Mode :

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

NOTE:

1. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

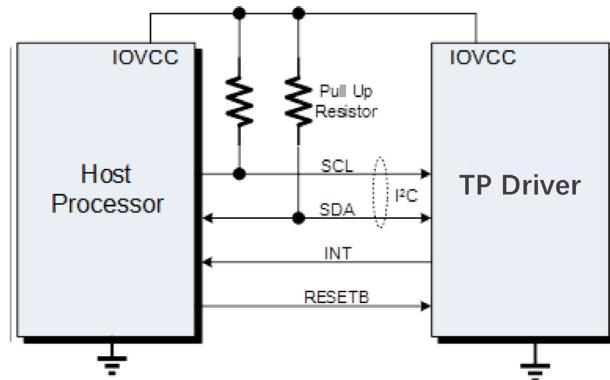
7-5 i8080-8Bits Interface Characteristics



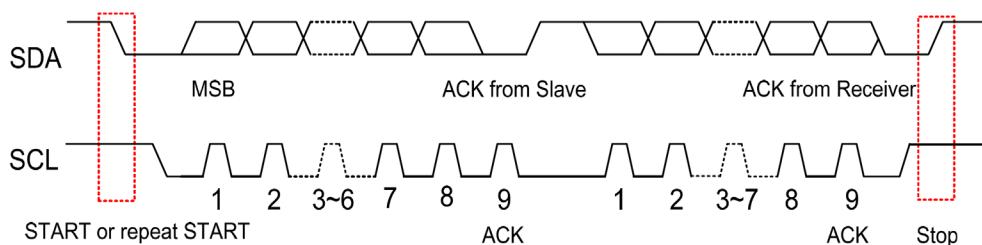
Characteristic	Symbol	Specification		Unit
		Min.	Max.	
Chip select setup time	CSX	t_{cssm}	10	–
Chip select hold time		t_{cshm}	10	–
Chip select “High” pulse width		t_{chwm}	20	–
Address setup time	DCX	t_{asm}	10	–
Address hold time(Write/Read)		t_{ahm}	10	–
Write cycle time	WRX (Write)	t_{wcm}	20	–
WRX “High” period (Write)		t_{wrhm}	10	–
WRX “Low” period (Write)		t_{wrilm}	10	–
Read cycle time (Register Read)	RDX (Register Read)	t_{rcm}	100	–
RDX “High” period (Register Read)		t_{rdhm}	50	–
RDX “Low” period (Register Read)		t_{rdlm}	50	–
Read cycle time (Memory Read)	RDX (Memory Read)	t_{rcm}	200	–
RDX “High” period (Memory Read)		t_{rdhm}	100	–
RDX “Low” period (Memory Read)		t_{rdlm}	100	–
Data setup time	DB[7:0]	t_{dsm}	10	–
Data hold time		t_{dhn}	10	–
Access time	DB[7:0]	t_{acm}	–	40
Output disable time		t_{odm}	20	–
Rise/Fall time	-	t_r/t_f	–	1

7-6 Touch Panel(TP) IIC Timing Characteristics

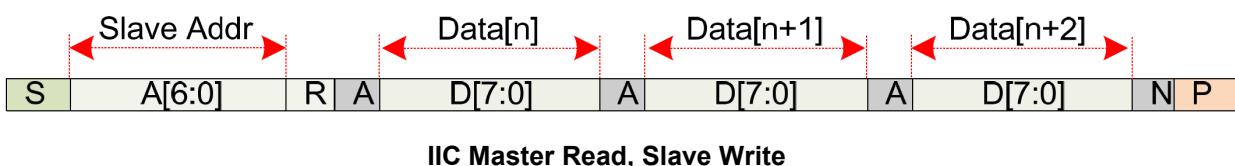
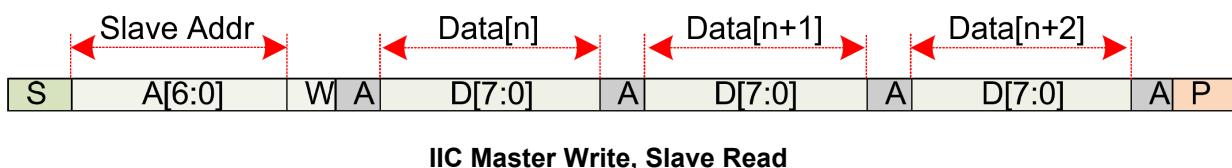
The TP driver communicates to the host through the IIC interface and follows the IIC protocol. IIC bus utilize the SCL and SDA, a two-wire synchronous communication interface and can operate at a maximum bit rate of 400kbps.



IIC Serial Data Transfer Format



IIC Interface Timing



TP Driver IC Slave Addr A[6:0]---0X38

Mnemonics	Description
S	I ² C Start or I ² C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0' for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I²C Timing Characteristics

Parameter	Standard Mode		Fast Mode		Unit
	Min	Max	Min	Max	
SCL frequency (fast mode support)	0	100	0	400	KHz
Clock low period	4.7	-	1.3	-	us
Clock high period	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	4.7	-	1.3	-	us
Hold time (repeated) START condition	4.0	-	0.6	-	us
Data setup time	250	-	100	-	ns
Setup time for a repeated START condition	4.7	-	0.6	-	us
Setup Time for STOP condition	4.0	-	0.6	-	us

TP I/O Communication Voltage follow IOVCC

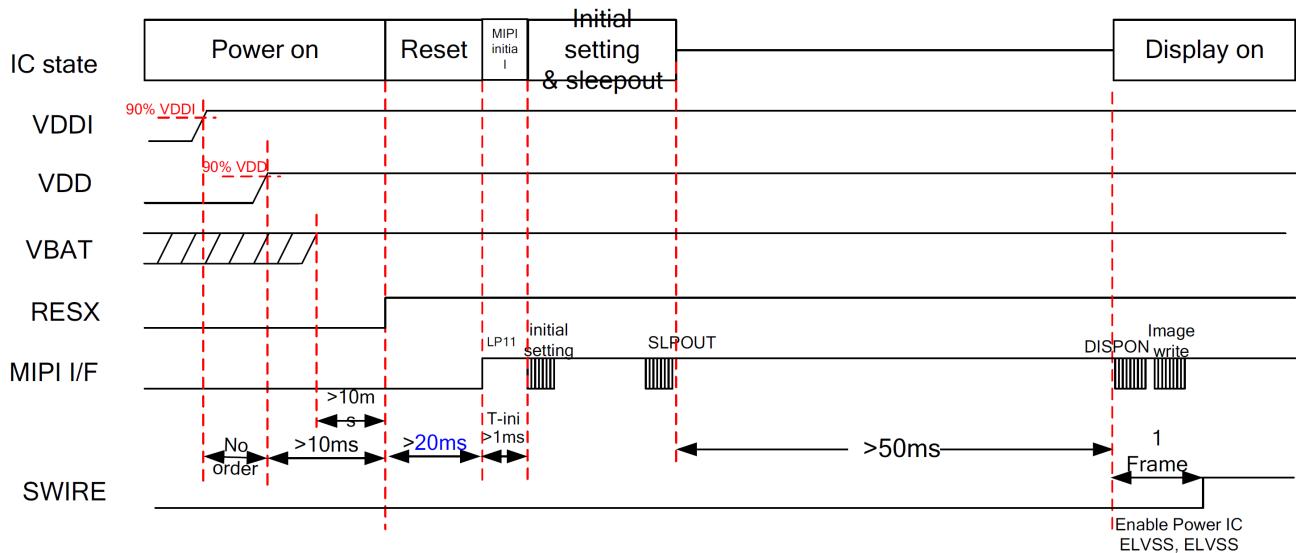
TP DC Characteristics

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Input high-level voltage	VIH		0.7 × IOVCC	-	IOVCC	V	
Input low -level voltage	VIL		-0.3	-	0.3 × IOVCC	V	
Output high -level voltage	VOH	IOH= -0.1mA	0.7 × IOVCC	-	-	V	
Output low -level voltage	VOL	IOH=0.1mA	-	-	0.3 × IOVCC	V	
I/O leakage current	ILI	Vin=0~AVDD	-1	-	1	µA	
Current consumption (Normal operation mode)	Iopr	AVDD=2.8V Ta=25°C MCLK=15MHz	-	1.5	-	mA	
Current consumption (Monitor mode)	Imon	AVDD=2.8V Ta=25°C MCLK=15MHz	-	30	-	µA	
Current consumption (Sleep mode)	Islp	AVDD=2.8V Ta=25°C	-	10	-	µA	
Power Supply voltage	AVDD		2.8	-	3.6	V	

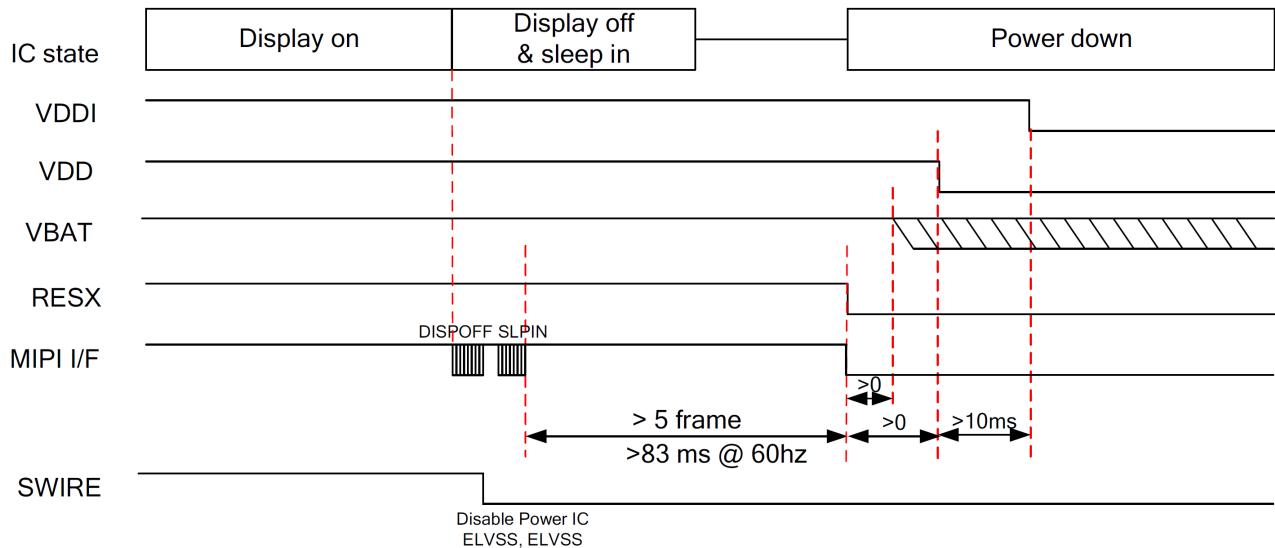
8.Recommended Operating Sequence

8.1 Power on/off sequence and timing

Power On sequence

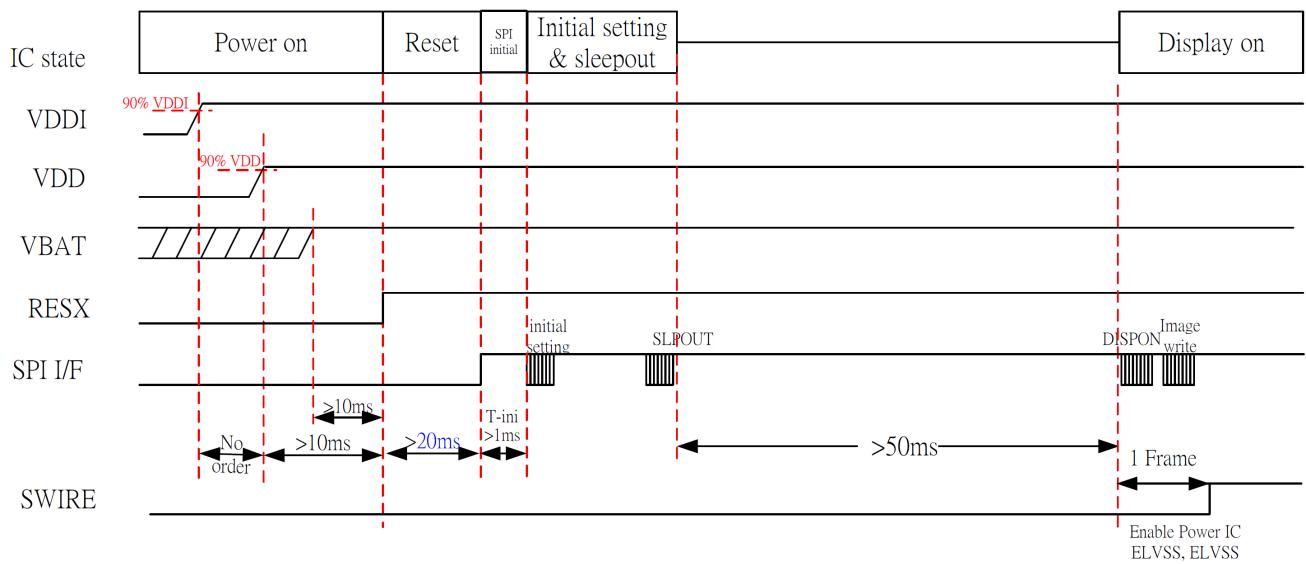


Power Off sequence



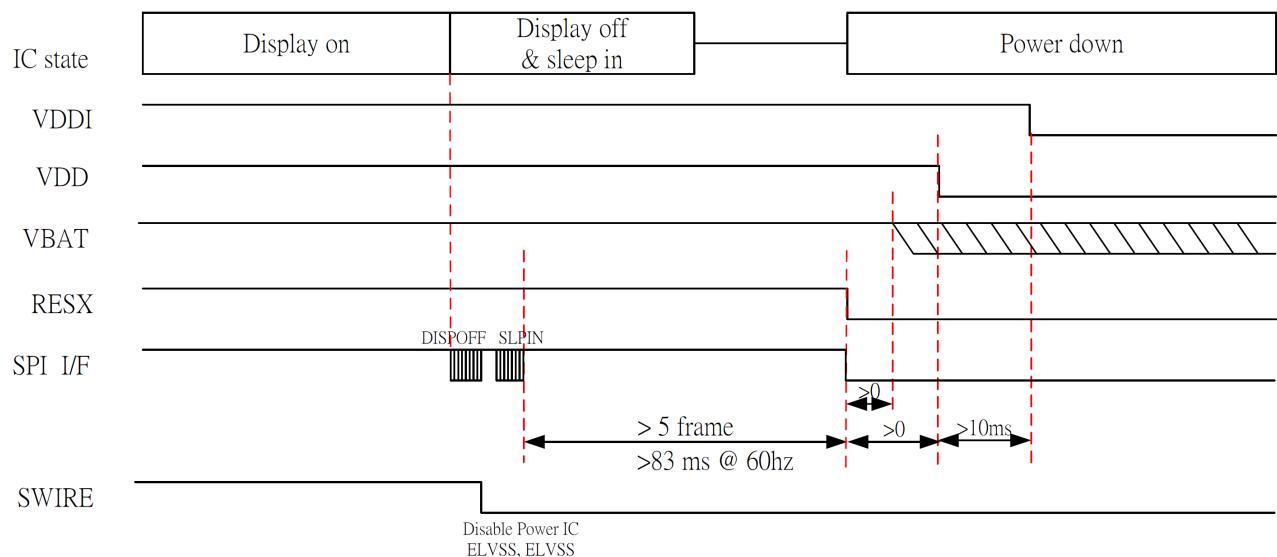
Power On sequence

SPI Interface



Power Off sequence

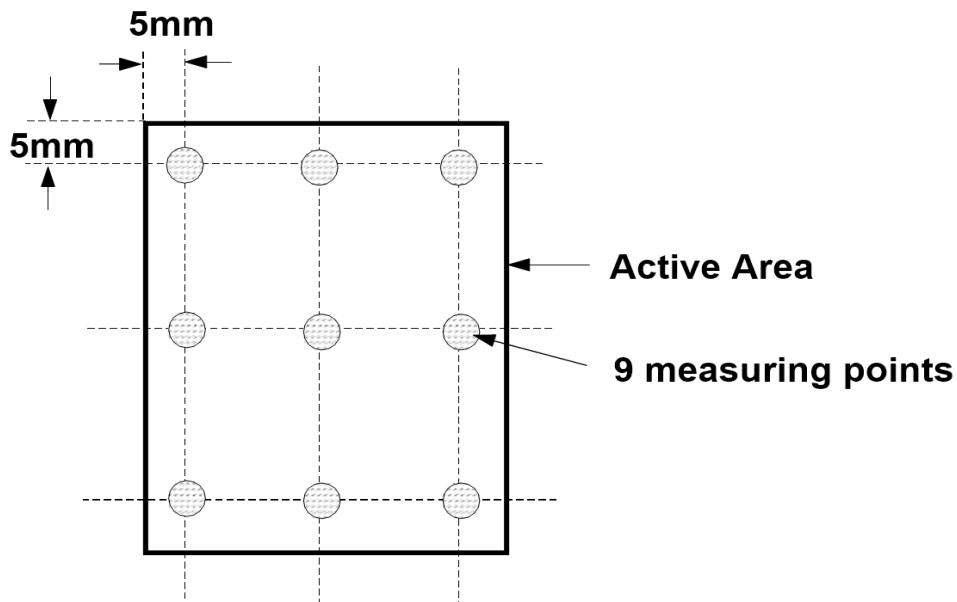
SPI Interface



9.Electro-optical characteristics

Item	Symbol	Temp	Condition	Min.	Typ.	Max.	Unit	Note		
Brightness		25°C	Normal (White Mode)	TBD	350	TBD	cd/m ²	Center brightness		
Uniformity		25°C	Normal (White Mode)	85	90	-	%	(1)		
Contrast ratio	K	25°C	Φ=0°,θ=0°	60,000		-	-	(1),(2)		
Color of CIE coordinate	White	25°C	Φ=0° θ=0°	0.275	0.295	0.315	-	(1),(2),(3)		
				0.295	0.315	0.335	-			
	Red			0.630	0.660	0.690	-			
				0.310	0.340	0.370	-			
	Green			0.170	0.220	0.270	-			
				0.680	0.730	0.780	-			
	Blue			0.115	0.140	0.165	-			
				0.025	0.050	0.075	-			
Color Gamut		25°C	vs. NTSC	85	100	-	%			
Life Time(5)		25°C	50% Brightness drop @250cd/m ² , Full White	-	30,000	-	Hr	(4)		

Note 1): Uniformity Measuring Point

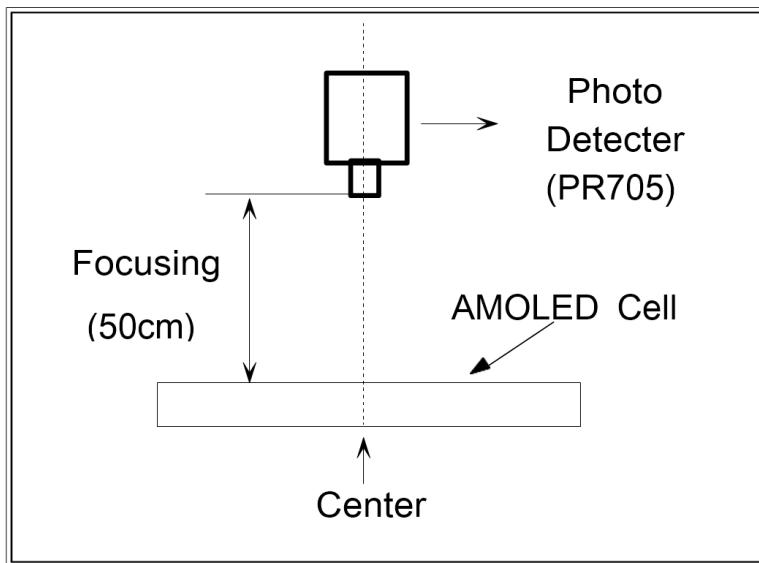


$$\text{Uniformity} = \frac{L_{\min}}{L_{\max}} * 100 \ [\%]$$

Note 2): Definition of contrast ratio (K)

$$\text{Contrast Ratio(K)} = \frac{\text{Brightness of selected dot} \\ (\text{White patterned area}) \text{ at } 250\text{cd/m}^2}{\text{Brightness of non-selected dot} \\ (\text{Black patterned area}) \text{ at } 250\text{cd/m}^2}$$

Note 3): Optical measuring system : temperature regulated chamber



Note 4): Life Time

The elapsed time that the full white brightness decreases to the half of initial value

10. Standard Specification For Reliability

No	Item	Condition	Cycles	Judgment Criterion
1	High Temperature Operation	80°C/ 240hours	10	
2	Low Temperature Operation	-30°C/ 240hours	10	
3	High Temperature Storage	85°C/ 240hours	5	1. No clearly visible defects or remarkable deterioration of display quality. However, any polarizer's deteriorations by the high temperature/ High humidity Storage test and the High temperature/ High humidity Operation test are permitted. 2. No function-related abnormalities.
4	Low Temperature Storage	-40°C/ 240hours	5	
5	High Temperature Humidity Operation	60°C/90%RH/ 240hours	5	
6	Thermal Shock	-40°C~85°C / 100cycles	5	

Note: The results must be measured after 2 hours later under room temperature keeping.

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