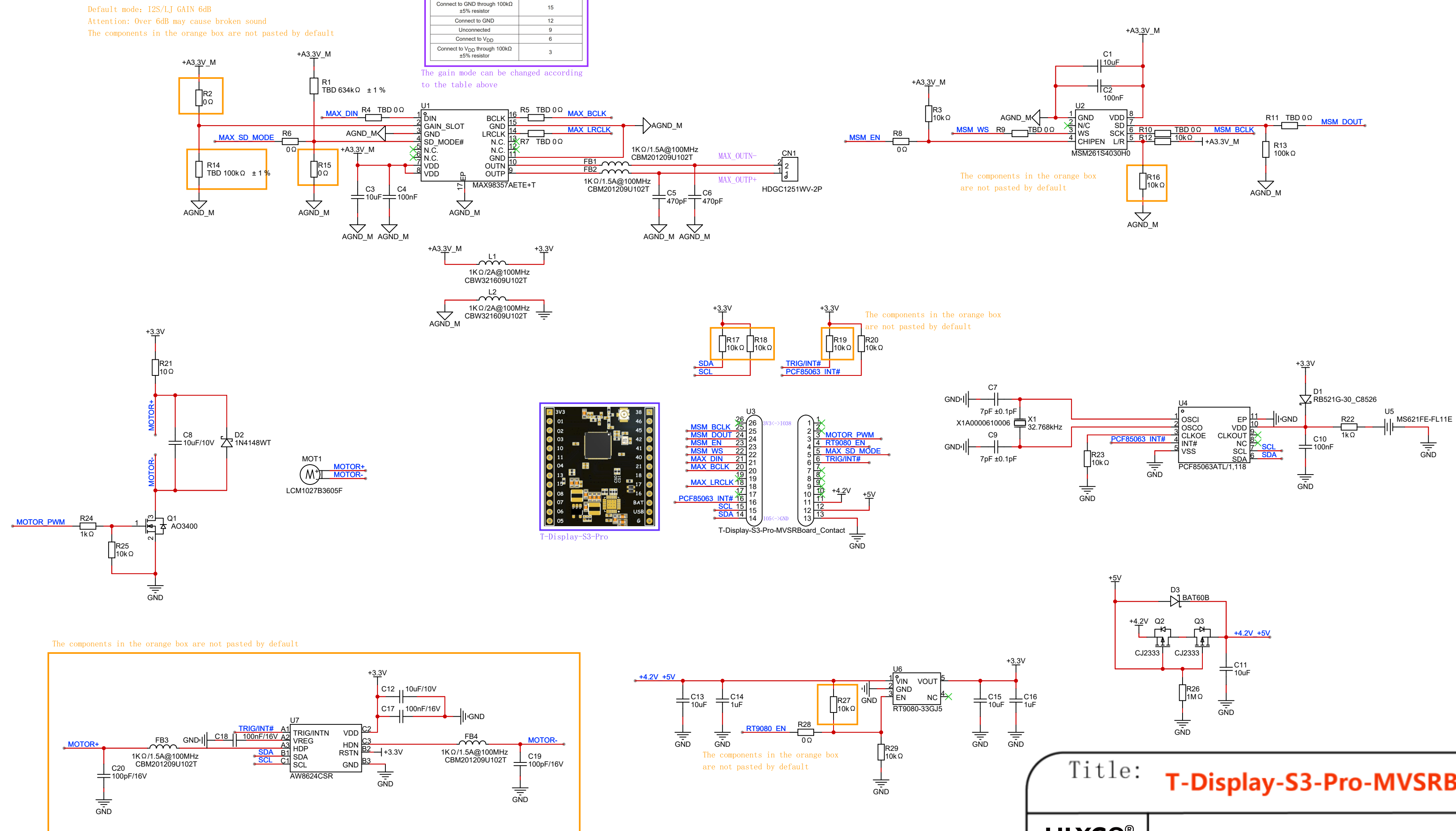


	SD_MODE STATUS	SELECTED CHANNEL
High	$V_{IC_MODE} > R2$ trip point	Left
Pulup through R_{PULL1}	$R2$ trip point $> V_{IC_MODE} > B1$ trip point	Right
Pulup through R_{PULL2}	$B1$ trip point $> V_{IC_MODE} > B0$ trip point	(Left2 & right2)
Low	$B0$ trip point $> V_{IC_MODE}$	Shutdown

LOGIC VOLTAGE LEVEL ($V_{DDIO}(V)$)	$R_{PULL1}(k\Omega)$	$R_{PULL2}(k\Omega)$
1.8	69.8	300
3.3	215.2	634

GAIN_SLOT	I²S/LJ GAIN (dB)
Connect to GND through 100kΩ ±5% resistor	15
Connect to GND	12
Unconnected	9
Connect to V _{DD}	6
Connect to V _{DD} through 100kΩ ±5% resistor	3

The gain mode can be changed according to the table above



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	Company: LILYGO	License: GPL 3.0
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