Micro-32 Plus

Technical specification

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1. Overview

The micro-32 plus is a general-purpose wi-fi +BT+BLE MCU module that is powerful and versatile for low-power sensor networks and demanding tasks such as speech encoding, audio streaming, and MP3 decoding.

The micro-32 plus comes in two modules, one with a ceramic antenna and the other with an IPEX antenna. The micro-32 is configured with 8 MB SPI flash and 2MB PSRAM

The ordering information of micro-32 plus is shown in the following table:

Table 1: Micro-32 plus information

Module	Built-in chip	Flash	PSRAM	module size (mm)
Ceramic Ant.	ESP32-PICO-V3-02	8 MB	2 MB	(13.00)x(18.90)x(2.80)
IPEX				

U. FL seat sizes are described in section 10. The information provided in this document applies to both modules.

Micro-32 USES ESP32-PICO-V3-02 chip*. ESP32-PICO-V3-02 chip has extensible, adaptive features. Two CPU cores can be controlled separately. Clock rates range from 80 MHz to 240 MHz. The user can turn off the power to the CPU and use the low-power coprocessor to monitor changes in the state of the peripheral or whether certain analog quantities exceed the threshold.

ESP32 also integrates a wealth of peripherals, including capacitive touch sensors, hall sensors, low-noise sensor amplifiers, SD card interfaces, Ethernet interfaces, high-speed SPI, UART, I2S, and I2C.。

Description：
* Please refer to the ESP32 specification for product model description of ESP32 series

The module integrates traditional Bluetooth, low-power Bluetooth and wi-fi, and has a wide range of USES: wi-fi supports a wide range of communication connections, as well as direct Internet connections via routers; Bluetooth allows users to connect to their mobile phones or broadcast BLE beacons for easy signal detection.ESP32 has A sleep current of less than 5 A, making it suitable for battery-powered wearable devices The module supports data transmission rate up to 150 Mbps, antenna output power up to 20 dBm, can achieve the maximum range of wireline communication. Therefore,

This module has industry-leading technical specifications and excellent performance in terms of high integration, wireless transmission distance, power consumption and network connectivity.

ESP32's operating system is freeRTOS with LwIP and TLS 1.2 with hardware acceleration. The chip supports OTA encryption updates at the same time, allowing developers to continue upgrading after the product launch.

Table 2 lists the product specifications for the micro-32 Plus。

Table 2: micro-32 plus product specifications

Categories	Items	Specifications
Certification	Bluetooth certification	BQB
Wi-Fi	Protocols	802.11 b/g/n (802.11n up to 150 Mbps)
		A-MPDU and A-MSDU aggregation and 0.4 μs guard interval support
	Center frequency range of operating channel	2412 ~ 2484 MHz
Bluetooth	Protocols	Bluetooth V4.2 BR/EDR and Bluetooth LE specification
	Radio	NZIF receiver with –97 dBm sensitivity
		Class-1, class-2 and class-3 transmitter
		AFH
	Audio	CVSD and SBC
Hardware	Module interfaces	ADC, DAC, touch sensor, SD/SDIO/MMC Host Controller, SPI, SDIO/SPI Slave Controller, EMAC, motor PWM, LED PWM, UART, I2C, I2S, infrared remote controller, GPIO, pulse counter, TWAI® (compatible with ISO 11898-1, i.e. CAN Specification 2.0)
	On-chip sensor	Hall sensor
	Integrated crystal	40 MHz crystal
	Integrated SPI flash	4 MB
	Operating voltage/Power supply	3.0 V ~ 3.6 V
	Operating current	Average: 80 mA
	Minimum current delivered by power supply	500 mA
	Operating ambient temperature	–40 °C ~ 85 °C
	Package size	(7.000±0.100) mm×(7.000±0.100) mm×(0.940±0.100) mm
	Moisture sensitivity level (MSL)	Level 3

2. Pin definition

2.1 pin layout

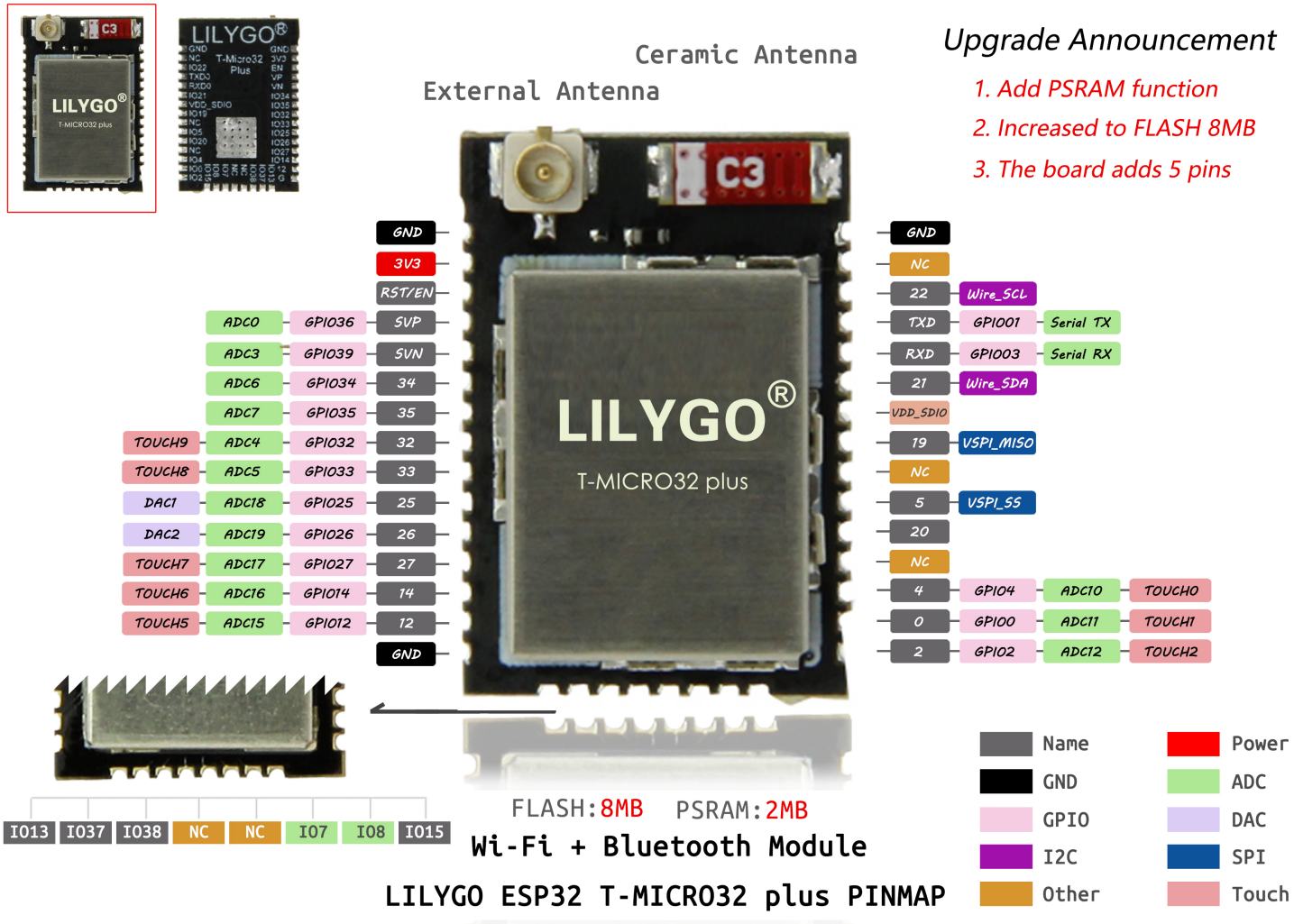

Table 1: Micro-32 Plus Pin Layout（TOP）

2.2 Pin description

Micro-32 has 38 pins in total, and the detailed description is shown in table 3

Table 3: pin definitions

Name	No.	Type	Function
GND	1	P	GND
3V3	2	P	Electricity supply
EN	3	I	Enable module, active high.
SENSOR_VP	4	I	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_VN	5	I	GPIO39, ADC1_CH3, RTC_GPIO3
IO34	6	I	GPIO34, ADC1_CH6, RTC_GPIO4
IO35	7	I	GPIO35, ADC1_CH7, RTC_GPIO5
IO32	8	I/O	GPIO32, XTAL_32K_P (32.768 kHz Crystal Input), ADC1_CH4, TOUCH9, RTC_GPIO9
IO33	9	I/O	GPIO33, XTAL_32K_N (32.768 kHz Crystal Output), ADC1_CH5, TOUCH8, RTC_GPIO8
IO25	10	I/O	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	11	I/O	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	12	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
IO14	13	I/O	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
IO12	14	I/O	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
GND	15	P	GND
IO13	16	I/O	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
SHD/SD2*	17	I/O	GPIO9, SD_DATA2, SPIHD, HS1_DATA2, U1RXD
SWP/SD3*	18	I/O	GPIO10, SD_DATA3, SPIWP, HS1_DATA3, U1TXD
SCS/CMD*	19	I/O	GPIO11, SD_CMD, SPICS0, HS1_CMD, U1RTS
SCK/CLK*	20	I/O	GPIO6, SD_CLK, SPICLK, HS1_CLK, U1CTS
SDO/SD0*	21	I/O	GPIO7, SD_DATA0, SPIQ, HS1_DATA0, U2RTS
SDI/SD1*	22	I/O	GPIO8, SD_DATA1, SPID, HS1_DATA1, U2CTS
IO15	23	I/O	GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0, RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3

IO2	24	I/O	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
IO0	25	I/O	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
IO4	26	I/O	GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
NC1	27	-	-
NC2	28	-	-
IO5	29	I/O	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
IO18	30	I/O	GPIO18, VSPICLK, HS1_DATA7
IO19	31	I/O	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
NC	32	-	-
IO21	33	I/O	GPIO21, VSPIHD, EMAC_TX_EN
RXD0	34	I/O	GPIO3, U0RXD, CLK_OUT2
TXD0	35	I/O	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
IO22	36	I/O	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
IO23	37	I/O	GPIO23, VSPID, HS1_STROBE
GND	38	P	GND

Note：

* pins SCK/CLK, SDO/SD0, SDI/SD1, SHD/SD2, SWP/SD3, and SCS/CMD, namely GPIO6 to GPIO11, are used to connect SPI flash integrated on modules, and are not recommended for other functions.。

2.3 Strapping

ESP32 has five Strapping pins, as described in chapter 6: • MTDI

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

The software can read the values of the five pins in the register "GPIO_STRAPPING".

During the system reset of the chip (power-on reset, RTC watchdog reset, undervoltage reset), the Strapping pin samples the level and stores it in the latch with a latch of "0" or "1", which remains until the chip loses power or closes.

Each Strapping leg connects the internal pull up/pull down. If a Strapping pin has no external connection or is connected to an external line in a high impedance state, the internal weak pull-up/pull-down determines the default value of the Strapping input level.

To vary Strapping values, you can apply external pull-down/pull-up resisters, or apply host MCU's GPIO to control Strapping pin levels for ESP32 recharging.

After resetting, the Strapping leg performs the same function as the conventional leg.

See table 4 for detailed boot modes for configuring Strapping pins.

Table 4: Strapping

Voltage of Internal LDO (VDD_SDIO)			
Pin	Default	3.3 V	1.8 V
MTDI	Pull-down	0	1
Booting Mode			
Pin	Default	SPI Boot	Download Boot
GPIO0	Pull-up	1	0
GPIO2	Pull-down	Don't-care	0
Enabling/Disabling Debugging Log Print over U0TXD During Booting			
Pin	Default	U0TXD Active	U0TXD Silent
MTDO	Pull-up	1	0
Timing of SDIO Slave			
Pin	Default	FE Sampling FE Output	FE Sampling RE Output	RE Sampling FE Output	RE Sampling RE Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

Note:

• the firmware can change the Settings of "built-in LDO (VDD_SDIO) voltage" and "SDIO slave signal input and output timing sequence" after startup by configuring some register bits.

• MTDI has been pulled up to high level (VDD_SDIO output 1.8v) inside the module since flash and SRAM of micro-32 module only support 1.8v.

3. Function description

This chapter describes the various modules and functions of the micro-32.。

3.1 CPU and memory

ESP32-PICO-V3-02 comes with two low-power Xtensa® 32-bit LX6 processors.On-chip storage includes: • 448 KB of ROM for program startup and kernel function calls:

• SRAM on 520 KB chips for data and instruction storage

• RTC fast memory, with 8 KB of SRAM, can be used for data storage and access by main CPU when RTC starts up in deep-sleep mode

• RTC slow memory, 8 KB SRAM, can be accessed by coprocessors in deep-sleep mode

• 1 Kbit eFuse, where 256 bits are dedicated to the system (MAC address and chip Settings); The remaining 768 bits are reserved for user programs, which include flash encryption and chip ids

3.2 external Flash and SRAM

ESP32 supports multiple external QSPI flash and static random access memory (SRAM). Refer to the SPI chapter of the ESP32 technical reference manual for details. ESP32 also supports AES based hardware encryption and decryption to protect applications and data in developer flash.

ESP32 can access external QSPI flash and SRAM via cache:

• external flash can map to both CPU instructions and read-only data Spaces.

-- when mapped to the CPU instruction space, up to 11 MB+248 KB can be mapped at a time. If the mapping exceeds 3 MB+248 KB at a time, cache performance may be reduced by speculative reads from the CPU.

- when mapped to a read-only data space, up to 4 MB can be mapped at a time. Supports 8-bit, 16-bit, and 32-bit reads.

• external SRAM can be mapped to CPU data space. Up to 4 MB can be mapped at a time. Supports 8-bit, 16-bit, and 32-bit access.

The micro-32 integrates 4 MB SPI flash and 8 MB PSRAM.

3.3 crystal vibration

The module USES 40 MHz crystal oscillator

3.4 RTC and low power management

ESP32 USES advanced power management technology to switch between different power modes.

For the current consumption of ESP32 in different power modes, see section "RTC and low power management" in the ESP32 technical specification.

4. Peripheral interface and sensor

Please refer to the section of ESP32 technical specification for Chinese and foreign interface and sensor。

Description::

GPIO6-11 has been used to connect the integrated SPI flash on the module, gpio16-17 has been used to connect the integrated PSRAM on the module, and other peripherals can use any other GPIO, see the circuit schematic diagram in section 6 for details.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the recommended operating conditions.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	–0.3	3.6	V
I_{output} [1]	Cumulative IO output current	-	1,100	mA
T_{store}	Storage temperature	–40	150	°C

1. The module worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO) output high logic level to ground. Please note that pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.
2. Please see Appendix IO_MUX of *ESP32 Datasheet* for IO's power domain.

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	-	-	A
T	Operating temperature	–40	-	85	°C

5.3 DC Characteristics (3.3 V, 25 °C)

Table 6: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter		Min	Typ	Max	Unit
C_{IN}	Pin capacitance		-	2	-	pF
V_{IH}	High-level input voltage		0.75×VDD[1]	-	VDD[1]+0.3	V
V_{IL}	Low-level input voltage		–0.3	-	0.25×VDD[1]	V
I_{IH}	High-level input current		-	-	50	nA
I_{IL}	Low-level input current		-	-	50	nA
V_{OH}	High-level output voltage		0.8×VDD[1]	-	-	V
V_{OL}	Low-level output voltage		-	-	0.1×VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, output drive strength set to the maximum)	VDD3P3_CPU power domain [1, 2]	-	40	-	mA
		VDD3P3_RTC power domain [1, 2]	-	40	-	mA
		VDD_SDIO power domain [1, 3]	-	20	-	mA

Symbol	Parameter	Min	Typ	Max	Unit
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, output drive strength set to the maximum)	-	28	-	mA
R_{PU}	Resistance of internal pull-up resistor	-	45	-	kΩ
R_{PD}	Resistance of internal pull-down resistor	-	45	-	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP_PU to power off the chip	-	-	0.6	V

Notes:

1. Please see Appendix IO_MUX of *ESP32 Datasheet* for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.
2. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, V_{OH}>=2.64 V, as the number of current-source pins increases.
3. Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

5.4 Wi-Fi Radio

Table 7: Wi-Fi Radio Characteristics

Description	Min	Typical	Max	Unit
Operating frequency range ^{note1}	2412	-	2484	MHz
Output impedance ^{note2}	-	50	-	Ω
TX power ^{note3}				
Output power of PA for 72.2 Mbps	13	14	15	dBm
Output power of PA for 11b mode	19.5	20	20.5	dBm
Sensitivity				
DSSS, 1 Mbps	-	–98	-	dBm
CCK, 11 Mbps	-	–91	-	dBm
OFDM, 6 Mbps	-	–93	-	dBm
OFDM, 54 Mbps	-	–75	-	dBm
HT20, MCS0	-	–93	-	dBm
HT20, MCS7	-	–73	-	dBm
HT40, MCS0	-	–90	-	dBm
HT40, MCS7	-	–70	-	dBm
MCS32	-	–89	-	dBm
Adjacent channel rejection				
OFDM, 6 Mbps	-	37	-	dB
OFDM, 54 Mbps	-	21	-	dB
HT20, MCS0	-	37	-	dB
HT20, MCS7	-	20	-	dB

1. Device should operate in the frequency range allocated by regional regulatory authorities. Target operating frequency range is configurable by software.
2. For the modules that use IPEX antennas, the output impedance is 50 Ω. For other modules without IPEX antennas, users do not need to concern about the output impedance.
3. Target TX power is configurable based on device or certification requirements.

5.5 BLE Radio

5.5.1 Receiver

Table 8: Receiver Characteristics – BLE

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	-	-	–97	-	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel C/I	-	-	+10	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	–5	-	dB
	F = F0 – 1 MHz	-	–5	-	dB
	F = F0 + 2 MHz	-	–25	-	dB
	F = F0 – 2 MHz	-	–35	-	dB
	F = F0 + 3 MHz	-	–25	-	dB
	F = F0 – 3 MHz	-	–45	-	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	-	-	dBm
	2000 MHz ~ 2400 MHz	–27	-	-	dBm
	2500 MHz ~ 3000 MHz	–27	-	-	dBm
	3000 MHz ~ 12.5 GHz	–10	-	-	dBm
Intermodulation	-	–36	-	-	dBm

5.5.2 Transmitter

Table 9: Transmitter Characteristics – BLE

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	3	-	dBm
RF power control range	-	–12	-	+9	dBm
Adjacent channel transmit power	F = F0 ± 2 MHz	-	–52	-	dBm
	F = F0 ± 3 MHz	-	–58	-	dBm
	F = F0 ± > 3 MHz	-	–60	-	dBm
$\Delta f1_{avg}$	-	-	-	265	kHz
$\Delta f2_{max}$	-	247	-	-	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	-	-	–0.92	-	-
ICFT	-	-	–10	-	kHz
Drift rate	-	-	0.7	-	kHz/50 μs
Drift	-	-	2	-	kHz

5.6 Reflow Profile

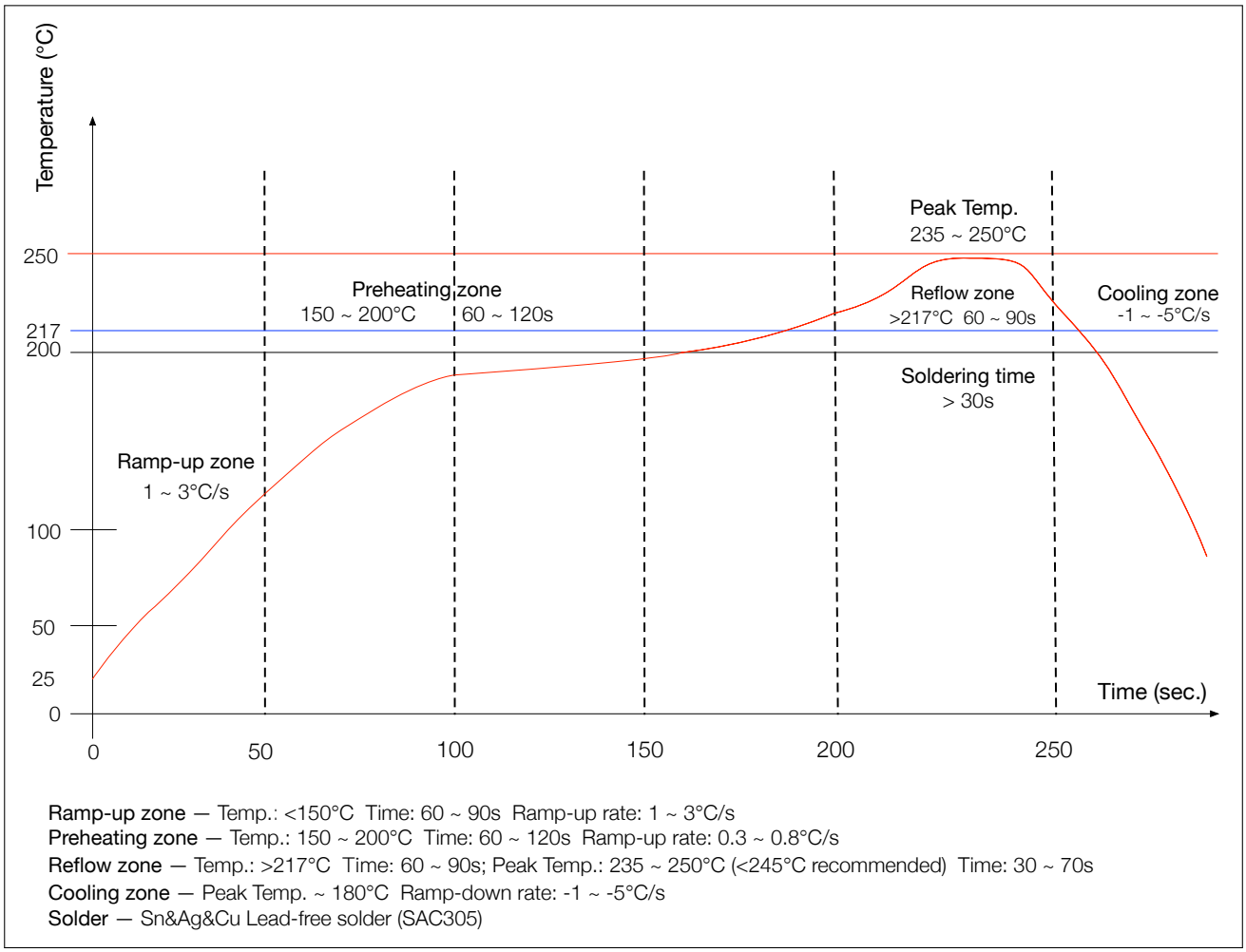

Figure 2: Reflow Profile

6. Circuit schematic diagram

Figure 3: micro-32 circuit schematic diagram

Description:
The discharge circuit is used in the case that VDD33 needs to be switched quickly and repeatedly, and the peripheral circuit of VDD33 has large capacitance. Please refer to the ESP32 specification for details

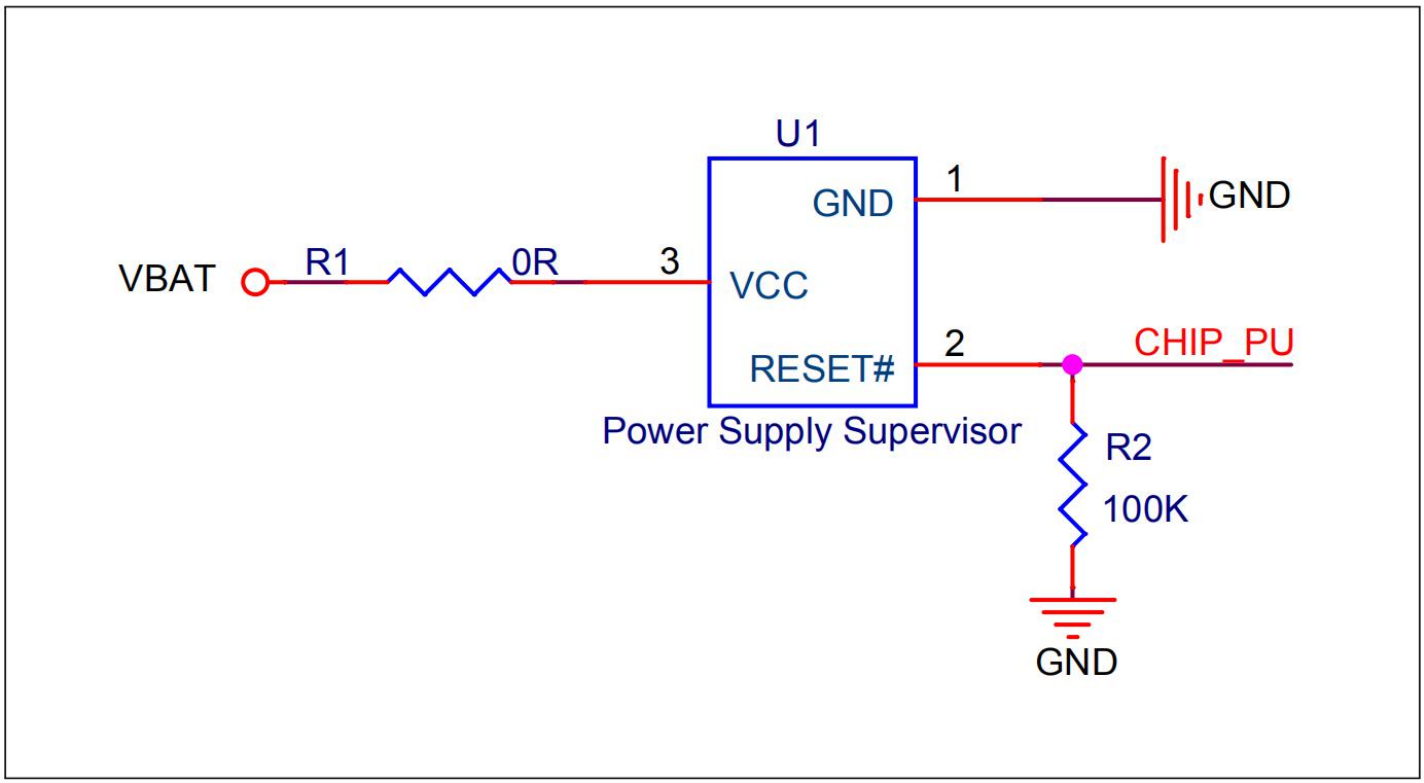

Figure 6: reset circuit

Description:
When the battery is used to Power the ESP32 series chips and modules, it is generally recommended to connect Power Supply Supervisor to the outside to avoid the abnormal state of the chips that cannot start normally due to the low battery voltage. It is recommended to lower the CHIP_PU feet of ESP32 when the

7. Module size

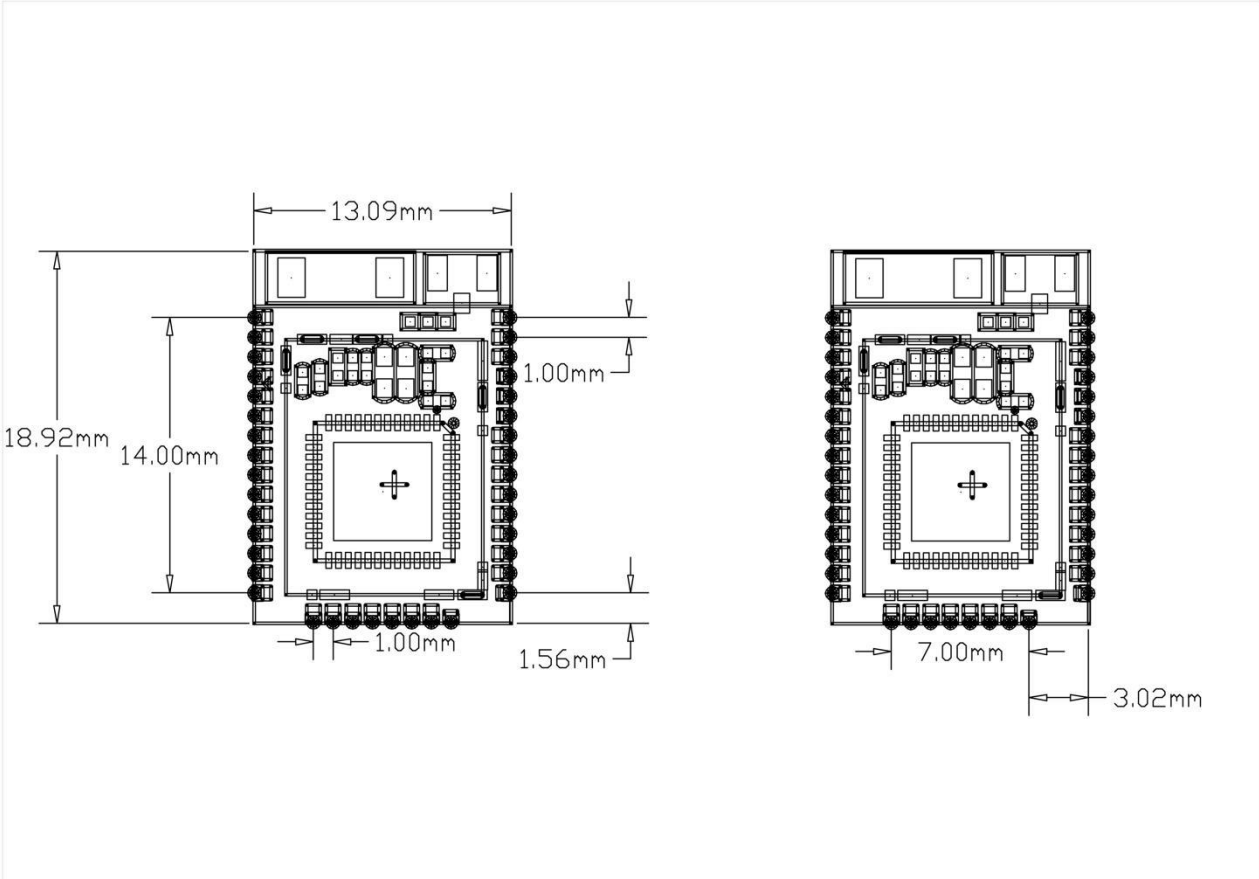

Figure 7: Micro-32 Plus(PCB/IPEX) dimension

8. PCB packaging graphics

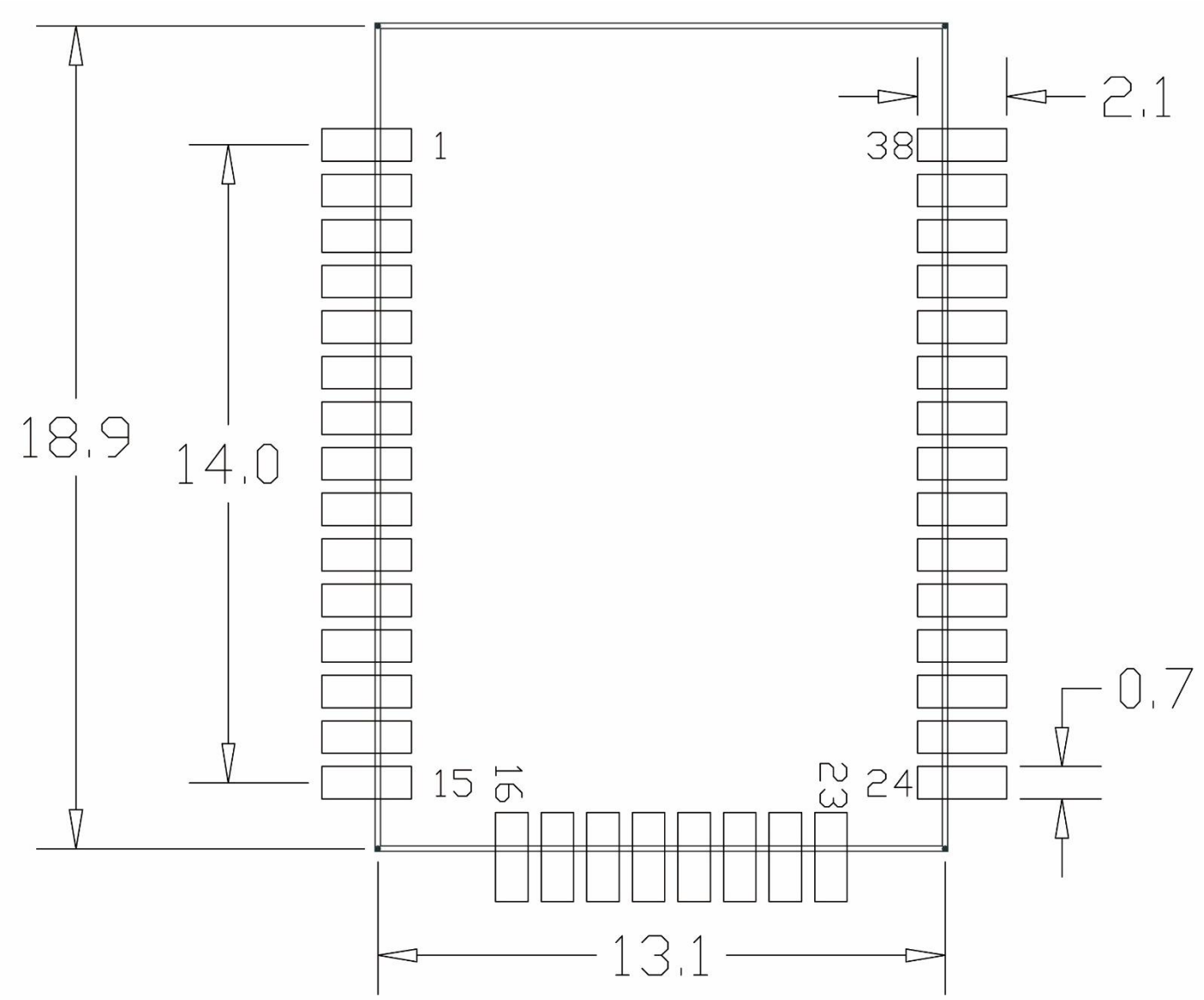

Figure 8: micro-32 encapsulates graphics

9. U.fl seat size

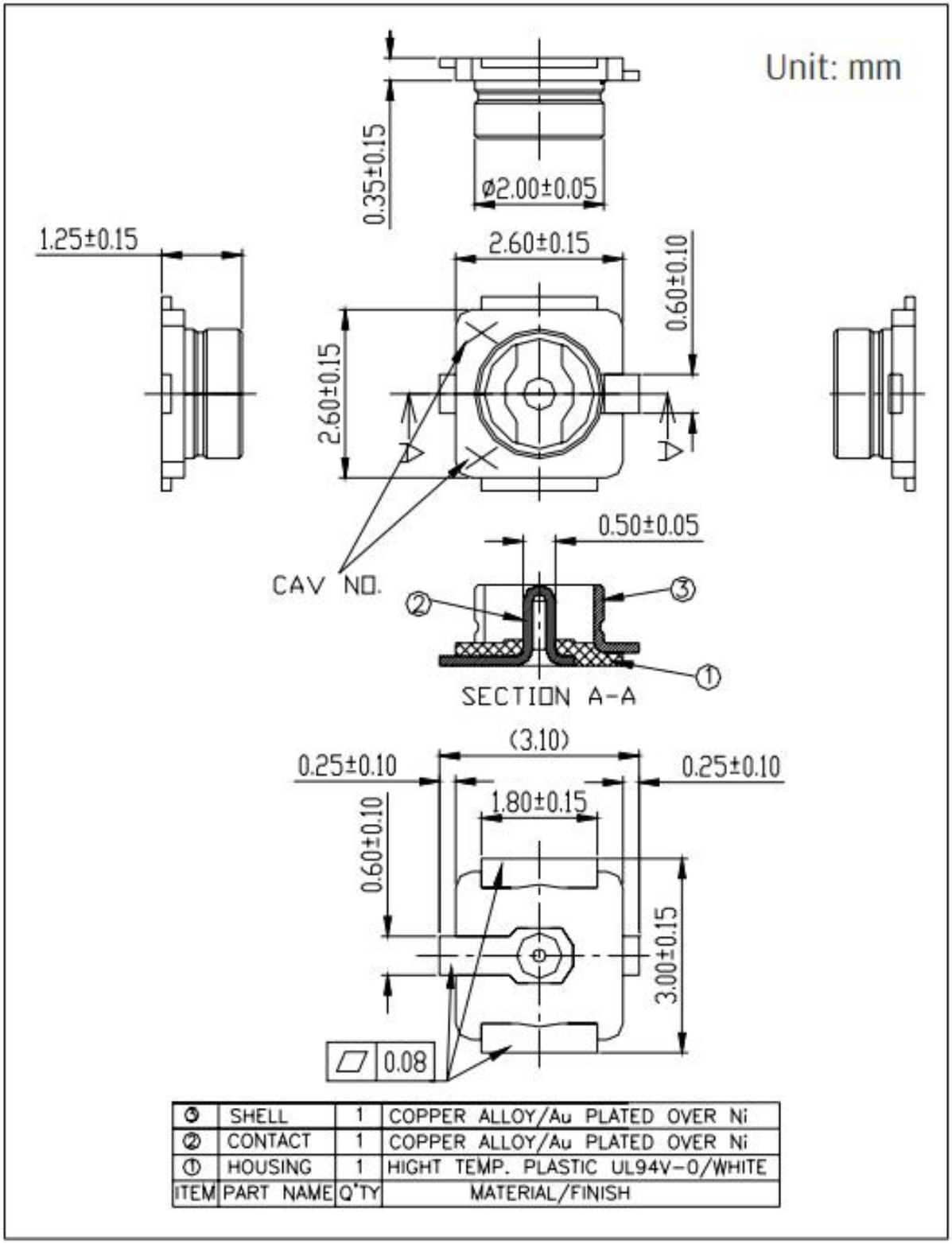

Figure 9: seat size diagram of u.fl