论文报告 2: IBM POWER7 multicore server processor

黄科乐 201828013229084

Time: 10-4

1 Introduction

The goal of POWER7 was to improve the socket-level, core-level, and thread-level performances significantly over POWER6 while achieving all of the following in one technology generation.
1.Reduce the core area and power to such an extent that four times as many cores can be placed on the processor chip in the same power envelope as that of POWER6.
2.Fit the POWER7 chip in the same socket as POWER6 and utilize the same SMP and I/O buses as in POWER6, which allows faster time to market and more continuity in POWER system designs.
3.Remove the external Level (L3) cache chips used in previous designs in order to reduce the system cost and power and power.
4.For significant performance improvement in high-performance computing(HPC), double the floating-point capability of each POWER7 core.

2 POWER7 core

POWER7 has advanced branch prediction and prefetching capabilities, as well as deep out-of-order execution capability for significant ST performance gain. Several POWER7 optimizations are focused on reducing core power and area. To reduce power and area, a partitioned approach to the SMT4 design was incorporated. With this approach, POWER7 can efficiently rename registers for twice as many threads with a total of physical GPR file entries that is less than that of POWER5*, which only supported SMT2. In erarlier out-of-order machines, the register rename structure for the GPR, FPR, VR was separate, which required a large number of entries. In POWER7, these were all merged into one unified rename structure with a total of 80 entries. In addition,the issue queues for FP instructios and FX have been combined to reduce the area and power.
As show in Fig.1:

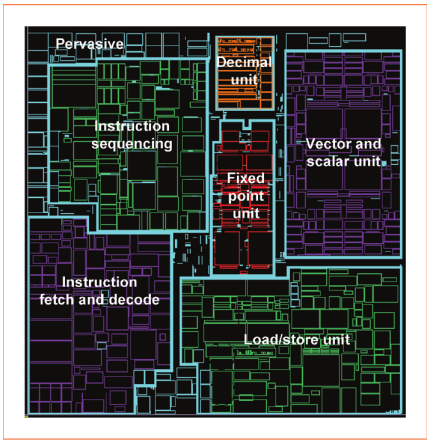

图 1: IBM POWER7 processor core floorplan

3 Instruction fetching

The IFU in POWER7 is based on a highly accurate branch-prediction mechanism, from each active thread well ahead of the point of execution. The IFU is also responsible for maintaining balance of instruction execution rates from the active threads based on software-specified threaad priorities, decoding and forming groups of instructions for the rest of the instruction pipeline, and executing branch instructions.

3.1 Branch prediction

The POWER7 IFU supports a three-cycle branch scan loop to fetch 8 instructions from the instruction cache, scan the fetched Ins for branches that have been predicted as taken, compute their target addresses, determine whether any of these branches are unconditional or predicted as taken, and if so, make the target address of the first such branch available for next fetch for the thread.

4 Data fetching

Data fetching is performed by the LSU, which contains two symmetric LS execution pipelines(LS0 and LS1), each capable to execute a load or a store operation in a cycle.

5 Fixed-point unit

The FXU comprises of two identical pipelines(FX0 and FX1). The most frequent FX instructions are executed in one cycle, and dependent operations may issue back to back to the same pipeline, if they are dispatched to the same UQ half.

6 Vector and scalar instruction execution

The POWER7 VSU implements the new VSX architecture introducing 64 architected registers. With dual issue of two-way SIMD floating-point DP instructions. the performance in FLOPs per cycle per core is doubled in comparison to POWER6.

7 Cache hierarchy

The cache hierarchy for POWER7 has been reoptimized with regard to the prior generation POWER6 processor in order to suit some changes in the core and at the chip.
1.Repipelining of the core from high-frequency design to the power/performance optimized design point.
2.Change from a primarily in-order to a primarily out-of-order instruction scheduling policy.
3.Reduction in L1 D-cache size from 64 to 32 KB along with reduction in L1 cache access time.
5.Growth from two cores to eight cores per die.

8 Reliability, availably, and serviceability

When an error is detected and reported by a core unit, the POWER7 core quickly blocks all instruction completion, along with blocking all instruction fetch and dispatch. To facilitate error detection and recovery in POWER7, the big register files are ECC protected, whereas the smaller register files are protected through parity.

9 Summary

POWER7 continues the tradition of innovation in POWER line of processors. This seventh-generation chip adds balanced multicore design, eDRAM technology, and SMT4 to the POWER innovation portfolio. The POWER7 chip has four times as many cores and eight times as many threads, compared with POWER6 chip, as well as eight times as many FLOPs per cycle. The balanced design allows the processor to scale from a single socket low-end blade to a high-end enterprise system with 32 sockets, 256 cores,

and 1024 threads. This new innovative design provides more than 4 times performance increase per chip, compared with the previous generation POWER6 processor.