论文报告 3: Intel's Haswell CPU Microarchitecture

黄科乐 201828013229084

Time: 10-11

1 Introduction

Haswell is the first family of SoCs that have been tailored to take advantage of Intel' s 22nm FinFET process technology. The Haswell family features a new CPU core, new graphics and substantial changes to the platform in terms of memory and power delivery and power management. All of these areas are significant from a technical and economic perspective and interact in various ways. However, the Haswell family represents a menu of options that are available for SoCs tailored to certain markets. Not every product requires graphics (e.g. servers), nor is a new power architecture desirable for cost optimized products (e.g. desktops). Architects will pick and choose from the menu of options, based on a variety of technical and business factors.The heart of the Haswell family is the eponymous CPU.

2 Haswell Instruction Set and Front-end

Haswell introduces a huge number of new instructions for the x86 ISA, that fall into four general families. The first is AVX2, which promotes integer SIMD instructions from 128-bits wide in SSE to 256-bits wide.AVX2 includes 16 new gather instructions, loads that can fetch 4 or 8 non-contiguous data elements using special vector addressing for both integer and floating point (FP) SIMD.Intel' s architects determined that MOV elimination with FMA3 provides about the same performance as FMA4, but using denser and easier to decode instructions; hence the abrupt about face in late 2008. The third extension is 15 scalar bit manipulation instructions (known as BMI) that operate on general integer registers. The last and most powerful of Intel' s ISA extensions is TSX, which has been extensively discussed in a previous article on Haswell' s transactional memory.

3 Haswell Out-of-Order Scheduling

Haswell' s out-of-order execution is where the microarchitecture becomes quite interesting and many changes are visible. Haswell is substantially wider than Sandy Bridge with more resources for dynamic

scheduling, although the overall design is fairly similar. The first part of out-of-order execution is renaming. The most performance critical resources in Haswell have all been expanded. The physical register files hold the actual input and output operands for uops. Gather instructions are microcoded and introduce additional complexity to the microarchitecture. The number of uops executed by gather instruction depend on the number of elements.

4 Haswell Memory Hierarchy

The most significant and comprehensive changes in Haswell are all in the memory hierarchy. At a high level, Haswell has twice the FLOP/s of Sandy Bridge. But raw compute power alone is rarely an interesting proposition; to take advantage of the new capabilities, the cache bandwidth for Haswell has also doubled. Moreover, the whole memory hierarchy must be adapted for gather instructions and transactional memory.

5 Conclusions and Analysis

Looking back over several generations of Intel microprocessors, the changes are remarkable. Merom marked Intel' s 'right hand turn' , acknowledging that the Pentium 4 was not a viable long term solution because power efficiency is crucial to success. Starting from Merom, Intel' s design teams embarked upon a relentless journey of continuous improvement with each major architectural change.