ShanghaiTech University
School of Information Science and Technology
Student name:
Student ID:

CS110: Computer Architecture
Spring, 2024

Assignment 4: Digital circuit

Attention: Recommend using LaTeX to complete your work. You can use any tool, such as Logisim, Visio, Draw.io, PowerPoint, etc., to create diagrams. However, handwritten or hand-drawn content is not acceptable.

1 Combinational logic

The circuit shown in Figure. 1 is a 1-bit comparator. Answer the following questions.

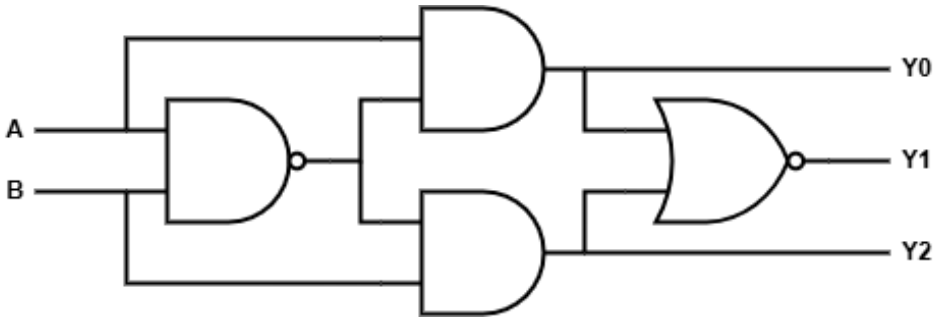


Figure 1: A 1-bit comparator circuit

(a) Write the un-simplified logic expressions for $Y0$, $Y1$ and $Y2$. [**6 pt**]

(b) Draw the truth table of this circuit in the following table.[**6 pt**]

(c) Write the sum of minterm for $Y0$, $Y1$ and $Y2$. [**6 pt**]

(d) What comparison do the outputs $Y0$, $Y1$ and $Y2$ represent respectively? e.g: $Y0 = 1$ represents $A = B$, $A < B$ or $A > B$ (one of the three cases). [**6 pt**]

(e) Draw the circuit of an unsigned 2-bit comparator using this 1-bit comparator and the following logic gates: 2-input AND, 2-input OR, and 1-input NOT. The 2-bit comparator has two 2-bit inputs $A1A0$ and $B1B0$, three outputs $Y0$, $Y1$ and $Y2$ with the same function as the 1-bit comparator. You can use the 1-bit comparator as a basic logic block as shown in Figure. 2. [**10 pt**]

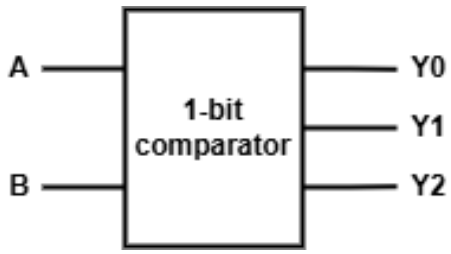


Figure 2: A 1-bit comparator diagram

Answer to Question 1

Your answer here.
(a) Un-simplified logic expressions:

$$Y0 = \overline{A}\overline{B} \cdot A$$
$$Y1 = \overline{(\overline{A}\overline{B} \cdot A) + (\overline{A}\overline{B} \cdot B)}$$
$$Y2 = \overline{A}\overline{B} \cdot B$$

(b) Do not modify the given values in the truth table.

A	B	Y2	Y1	Y0
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

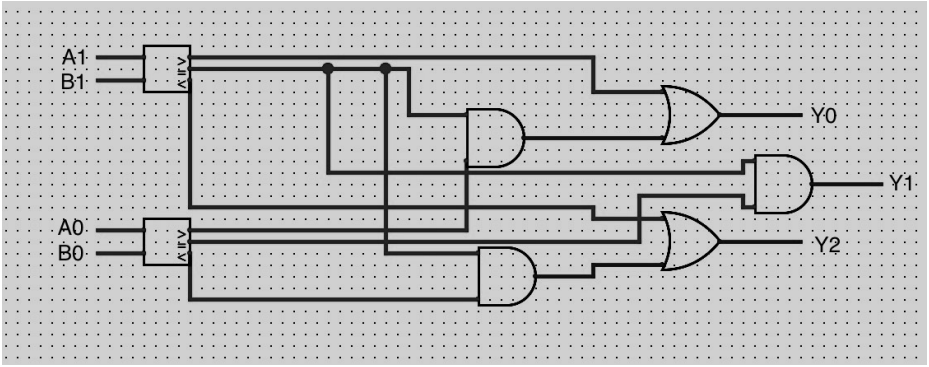
(c) Sum of minterms:

$$Y0 = A \cdot \overline{B}$$
$$Y1 = \overline{A} \cdot \overline{B} + A \cdot B$$
$$Y2 = \overline{A} \cdot B$$

(d) The outputs represent the following comparisons:

$$Y0 = A > B$$
$$Y1 = A = B$$
$$Y2 = A < B$$

(e) The circuit diagram of the 2-bit comparator is shown below



2 SDS

In the following circuit, NOT gates have a delay of 1ns, AND gates have a delay of 4ns, NAND gates have a delay of 3ns, OR gates have a delay of 4ns, NOR gates have a delay of 3ns. The registers have a clk-to-q delay of 2ns and setup time of 2ns. Assume the inputs come from registers. All the delays refer to propagation delay.

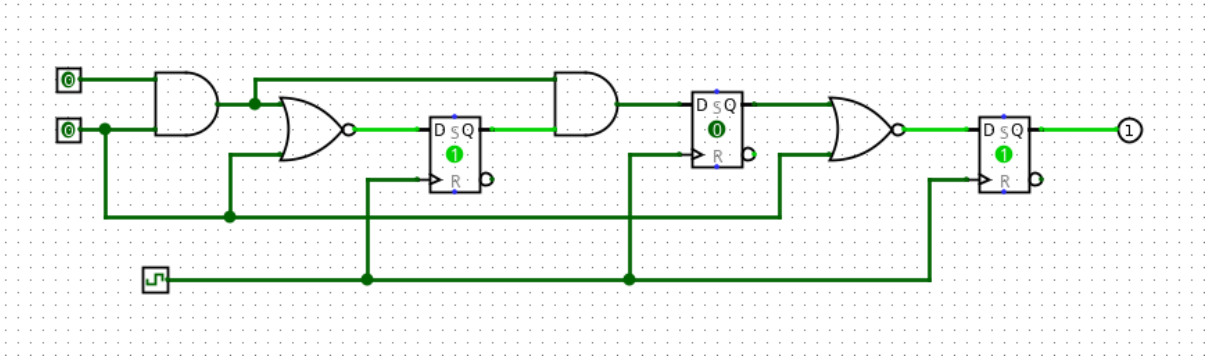


Figure 3: Circuit Diagram

What is the minimum acceptable clock cycle time for this circuit? What clock frequency does it correspond to? (please include enough explanation) **[16 pt]**

Answer to Question 2

Your answer here.
The minimum clock cycle time T_{min} is determined by the longest delay path between any two consecutive registers in the circuit. This delay must account for:
1. T_{clk-q} 2. T_{comb}: The maximum propagation delay through the combinational logic gates between the output of the first register and the input (D) of the second register.
3. T_{setup} $T_{min} = T_{clk-q} + T_{comb} + T_{setup}$
There are three paths in the circuit:
Path 1: Input Registers to Register 1 :
The path involves an AND gate followed by a NOR gate leading to the D input of the first register.
Delay = Delay(AND) + Delay(NOR) = 4 ns + 3 ns = 7 ns.(There's also a path from the bottom input through just the NOR gate: Delay(NOR) = 3 ns. We take the longer path).
Path 2: Register 1 to Register 2 :
The path involves the output of Register 1 going through two AND gates to the D input of Register 2.
Delay = 2 * Delay(AND) = 8 ns.
Path 3: Register 2 to Register 3 :
The path involves the output of Register 2 going through a NOR gate to the D input of Register 3.
Delay = Delay(NOR) = 3 ns.
So the longest path is Path 1, which has a delay of 7 ns.
Now, we can calculate the minimum clock cycle time:
$T_{min} = T_{clk-q} + T_{comb} + T_{setup}$
$T_{min} = 2 \text{ ns} + 8 \text{ ns} + 2 \text{ ns}$
$T_{min} = 12 \text{ ns}$
The clock frequency (f) is the reciprocal of the clock cycle time:
$f = 1/T_{min}$
$f = 1/12 \text{ ns}$
$f = 83.33 \text{ MHz}$
Therefore, the minimum acceptable clock cycle time for this circuit is 12 ns, which corresponds to a clock frequency of approximately 83.33 MHz.

3 Finite state machine

In this part, you need to implement a detector. When receiving two or more successive '0's or '1's, it outputs 1. For a bit sequence, it inputs one bit a period from left to right. e.g: input='11101001', output='01100010'.

(a) Draw the FSM (Moore machine) for this detector in five states: {start}, {10}(discrete '0'), {01}(discrete '1'), {00}(successive '0's), {11}(successive '1's).
e.g: input='011001', state={start}→{10}→{01}→{11}→{10}→{00}→{01} **[10 pt]**

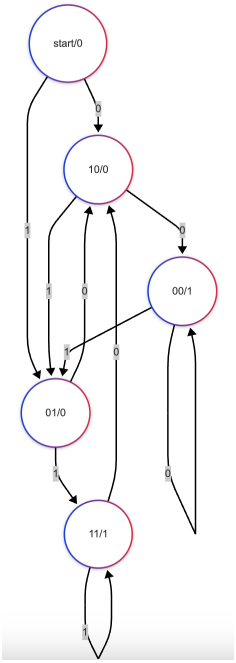
(b) Draw the FSM (Mealy machine) for this detector in no more than three states.**[10 pt]**

(c) Assign '000' to represent state {start}, '110' to represent {10}, '101' to represent {01}, '100' to represent {00}, '111' to represent {11}. We use 'CS' to represent current state and 'NS' for next state. Fill the truth table for the next-state and output logic based on the Moore FSM. **[15 pt]**

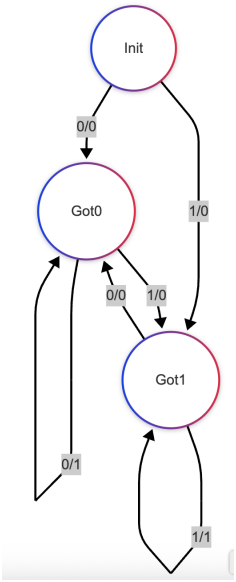
(d) Draw the circuit diagram for NS and output. **[15 pt]**

Answer to Question 3

Your answer here.
(a) The FSM (Moore machine) is shown below.



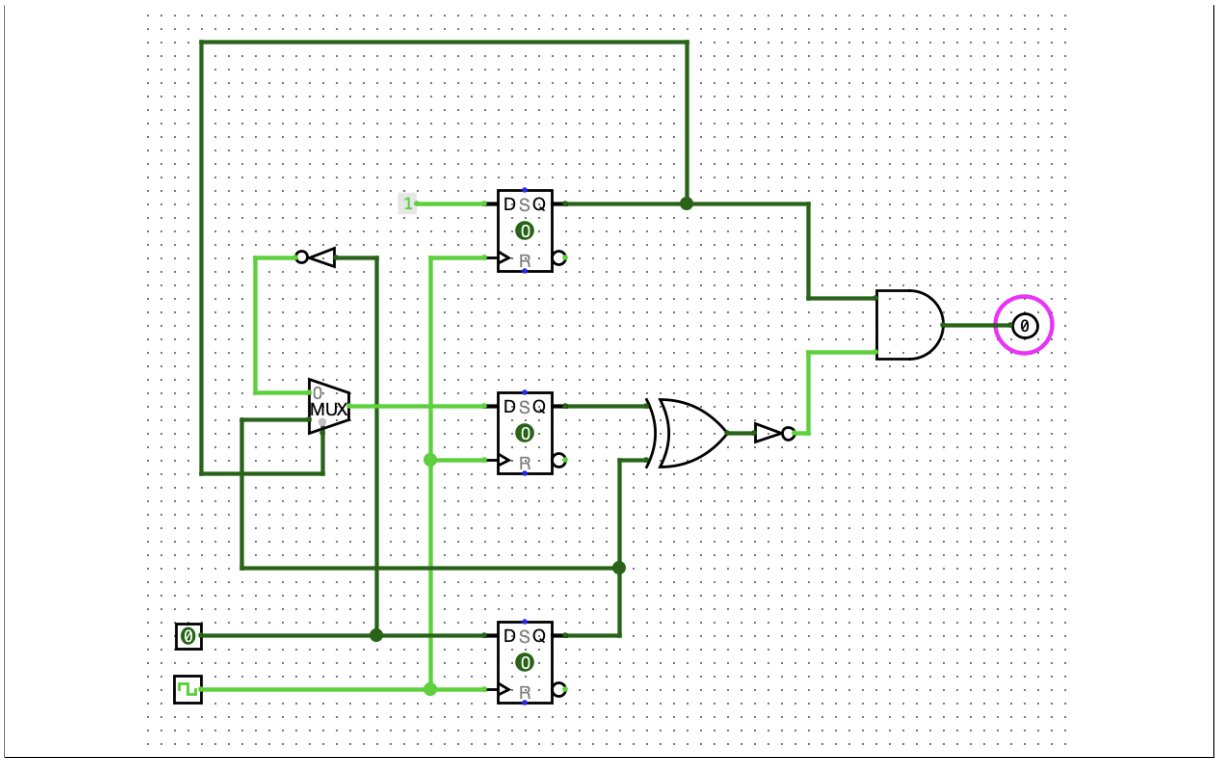
(b) The FSM (Mealy machine) is shown below.



(c) Do not modify the given values in the truth table.

CS[2]	CS[1]	CS[0]	input	NS[2]	NS[1]	NS[0]	output
0	0	0	0	1	1	0	0
0	0	0	1	1	0	1	0
1	1	0	0	1	0	0	0
1	1	0	1	1	0	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	1	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	1
1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1

(d) The circuit diagram for NS and output is shown below.


1
D S Q
0
R
0
MUX
D S Q
0
R
0
D S Q
0
R
0