26th IFIP/IEEE International Conference on Very Large Scale Integration

VLSI-SoC 2018

October 8-10, 2018
Verona, Italy
Roseo Hotel Leon d'Oro

VLSI-SoC 2018 is the 26th in a series of international conferences sponsored by the International Federation for Information Processing Technical Committee 10 Working Group 5, IEEE CEDA and IEEE CASS, which explore the state-of-the-art in the areas of Very Large Scale Integration (VLSI) and System-on-Chip (SoC) design. The purpose of VLSI-SoC is to provide a forum to exchange ideas and showcase academic as well as industrial research in architectures, circuits, devices, design automation, verification, test, and security, w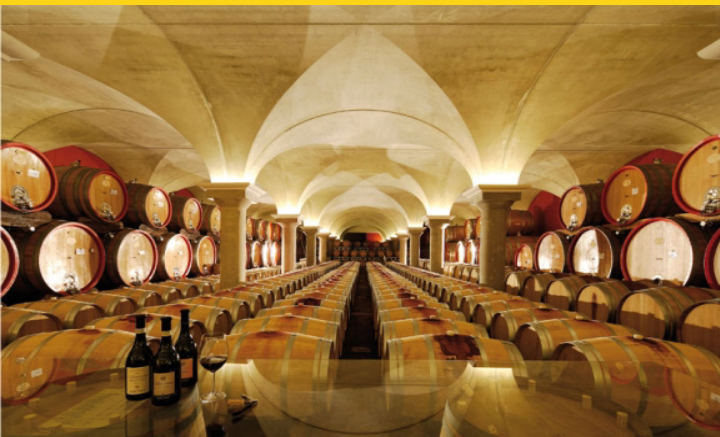ithin digital, analog, and mixed-signal systems. **VLSI-SoC 2018 will be held under the theme "Design and engineering of electronics systems based on new computing paradigms" by addressing cutting-edge research fields like heterogeneous, neuromorphic and brain-inspired, biologically-inspired, approximate computing systems.** VLSI-SoC 2018 will be held in Verona, Italy. Verona, which has been awarded World Heritage Site status by UNESCO because of its urban structure and architecture, is the set of the Shakespeare's Romeo and Juliet play, one of the most visited Roman imperial city in Northern Italy, the capital of the opera lyrics with its Arena roman amphitheater, the land of the Amarone della Valpolicella vineyards.

Paper Submission: Papers should present original research and industrial results not published or submitted for publication in other forums. Electronic submission in PDF format to http://www.vlsi-soc.com website is required. The proceedings will be published by IEEE and will be made available through IEEE Xplore.

A selection of the conference best papers will be invited to submit extended version to be included as chapters of a book to be published by Springer.

Paper Format: Papers should not exceed 6 pages (single-spaced, 2 columns, 10pt font). Submissions should be camera-ready, following the IEEE proceedings specifications.

Paper Publication and Presenter Registration: Papers will be accepted for regular or poster presentation at the conference. Every accepted paper MUST have at least one author registered at the conference by the time the camera-ready paper is submitted; the registered author is also expected to attend the conference and present the paper. A limited number of travel grants are available to needy PhD students from emerging countries.

PhD Forum and PhD School: A PhD Forum with a dedicated poster session will be included in the technical program, and PhD school on design and engineering of electronics systems will be co-located with the main conference.

Topics of interest include, but are not limited to:
- Analog, mixed-signal, and sensor architectures
- Digital architectures: NoC, multi- and many-core, hybrid, and reconfigurable
- CAD: Synthesis and analysis
- Prototyping, verification, modeling, and simulation
- Circuits and systems for signal processing and communications
- IoT, Embedded and Cyberphysical Systems: Architecture, design, and software
- Low-power and thermal-aware IC design
- Emerging devices and semiconductor technologies
- Variability, reliability, and test
- Hardware security
- Machine learning for SoC design and for electronic design automation

General chairs: Graziano Pravadelli (University of Verona, IT), Todd Austin (University of Michigan, USA)

Program chairs: Nicola Bombieri (University of Verona, IT), Masahiro Fujita (University of Tokyo, JP)

Special session chairs: Srinivas Katkoori (University of South Florida, USA), Katell Morin-Allory (TIMA Laboratory, FR)

PhD forum chairs: Kiyoung Choi (Seoul National University, KOR), Sara Vinco (Politecnico di Torino, IT)

Industrial chair: Yervant Zorian (Synopsys, USA)

Local chair: Franco Fummi (University of Verona, IT)

Publicity chairs: Ricardo Reis (UFRGS, BR), Matteo Sonza Reorda (Politecnico di Torino, IT)

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Abstract registration: April 20, 2018
Full paper submission: April 27, 2018
Special session proposal: April 27, 2018
Notification of acceptance: June 22, 2018
Camera ready: July 13, 2018