EECS240 – Spring 2010

Lecture 4: Design-Driven Small Signal Models

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MOSFET Models for Design

- SPICE (BSIM)
  - For verification
  - Device variations
- Hand analysis
  - Velocity-sat model (good mostly for intuition)
  - Small-signal model
- Challenge
  - How to accurately design when hand analysis models may be way off?

Parameters Designers Care About

- Layout designer:
  - Mostly care about just W and L
- Circuit designer:
  - Gain → g_m, r_o
  - Bandwidth → g_m, C_{GS}, C_{GD}, …
  - Power → I_D
  - Voltage swing → minimum V_{DS}
  - Noise
- Can get many of the circuit parameters without resorting to BSIM
  - Or rather, by just using BSIM as a look-up table

Small Signal Model

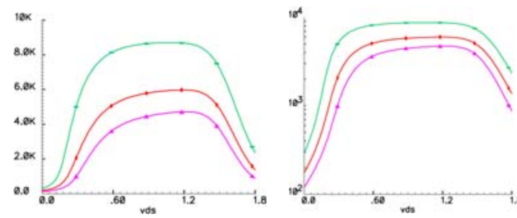
- Never really changes:

$$i_{ds} = \frac{\partial I_{ds}}{\partial V_{gs}} v_{gs} + \frac{\partial I_{ds}}{\partial V_{bs}} v_{bs} + \frac{\partial I_{ds}}{\partial V_{ds}} v_{ds}$$

$$i_{ds} = g_m V_{gs} + g_{mb} V_{bs} + g_{ds} V_{ds}$$

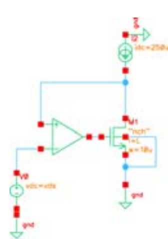
- Just need to know the coefficients…
  - Look at design-driven methods to figure out what r_o, g_m, etc. are
    - And what values you want to choose for them

Output Resistance r_o



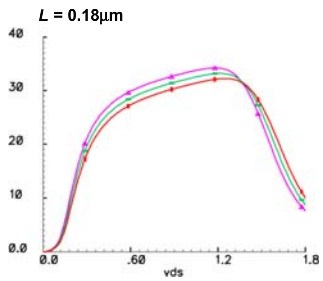
Hopeless to model this with a simple equation (e.g. $g_{ds} = \lambda I_D$)

What You Really Care About: Gain a_{v0}



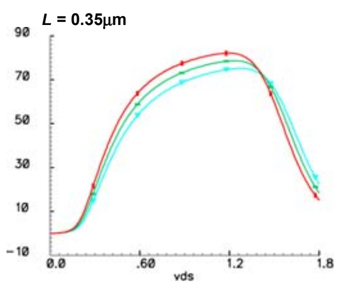
- Represents maximum attainable gain from a transistor
  - Often more useful than r_o
- Simulation Notes:
  - Bias current i_{dc} sets V_{GS} - V_T
  - Use feedback to find correct V_{GS} while sweeping V_{DS}
  - Use relatively small gain (100) for fast DC convergence

Gain, $a_{v0} = g_m r_o$



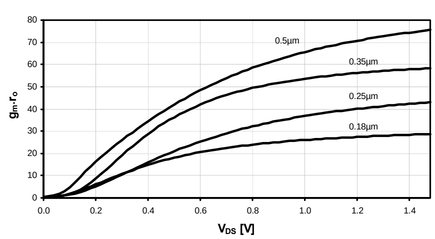
- Strong tradeoff: a_{v0} versus V_{DS} range
- *Create plots for several device lengths*

Long Channel Gain



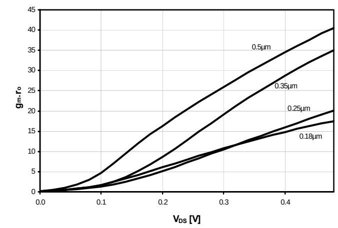
$L \uparrow \rightarrow a_{v0} \uparrow$

Technology Trend



Short channel devices usually have lower peak gain

Transistor Gain Detail



For practical V_{DS} gain penalty is less severe (remember: worst case V_{DS} is what matters!)

g_m: Square Law Model

- In saturation:

$$g_m = \mu C_{ox}\frac{W}{L}\sqrt{\frac{2I_{ds}}{\mu C_{ox}\frac{W}{L}}}$$

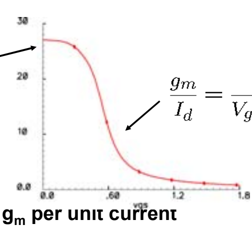
$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_{ds}} \propto \sqrt{I_{ds}}$$

$$g_m = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs}-V_T)^2\frac{1}{\frac{1}{2}(V_{gs}-V_T)}$$

$$g_m = \frac{2I_{ds}}{V_{gs}-V_T} = \frac{2I_{ds}}{\boldsymbol{V_{od}}}$$

Figure of Merit: g_m/I_D

$$\frac{g_m}{I_d} = ?$$



$$\frac{g_m}{I_d} = \frac{2}{V_{gs}-V_T} = \frac{2}{V_{dsat}}$$

- How much g_m per unit current
- Purely a DC metric
  - Will look at dynamic implications later
- Why does g_m/I_D flatten out at low V_{gs}?

Weak Inversion g_m

- In weak inversion we have bipolar behavior

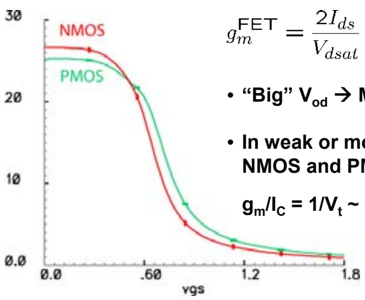
$$I_{ds} \approx \frac{W}{L} I_{ds,0} e^{\frac{q(V_{gs}-V_T)}{nkT}}$$

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\frac{W}{L} I_{ds,0} e^{\frac{q(V_{gs}-V_T)}{nkT}}}{n\frac{kT}{q}}$$

- Good model if transistor is actually used in weak inversion

$$g_m = \frac{I_{DS}}{n\frac{kT}{q}} \propto I_{DS}$$

Efficiency g_m/I_D



$$g_m^{\text{FET}} = \frac{2I_{ds}}{V_{dsat}} \quad \text{vs.} \quad g_m^{\text{BJT}} = \frac{I_C}{V_t}$$

- "Big" V_{od} → MOS has worse g_m/I_d
- In weak or moderate inversion, NMOS and PMOS approach BJT

$g_m/I_C = 1/V_t \sim 40\ V^{-1}$

Efficiency as a Design Parameter

- Why not use g_m/I_D for design?
- Can always determine value (from I_D and g_m)
  - Can do this "independently" of short channel effects (using simulator)
- Units (V^{-1}) and physical interpretation a little strange
  - But we'll just redefine things slightly to fix this

Substitute for g_m/I_D: V*

- Define:

$$\boxed{V^* = \frac{2I_D}{g_m} \quad \Leftrightarrow \quad \frac{g_m}{I_D} = \frac{2}{V^*}}$$

e.g. V* = 200mV → $g_m/I_D = 10\ V^{-1}$

- Square-law devices: $V^* = V_{GS}-V_{TH} = V_{od}$

$$\text{Square law}: \quad g_m = \frac{2I_D}{V_{GS}-V_{TH}} = \frac{2I_D}{V^*}$$

- Remember: real devices do not obey the square law!

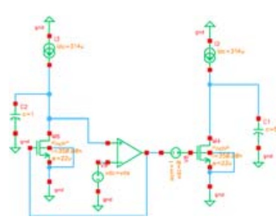
V_{od} vs V*

• Overdrive voltage V_{od}
  • Cannot be measured
  • Complex equations
	• $V^* = 2I_D/g_m$
	  • Measure (simulate) easily
	  • Complex equations

• "Long channel" devices:
  • $V_{od} = V_{dsat} = V^*$
  • $I_D \sim V^{*2}$
  • Boundary between triode and saturation
  • r_o "large" for $V_{DS} > V^*$
  • C_{GS}, C_{GD} change
	• "Short channel" devices:
	  • All interpretations of V* are *approximations*
	  • Except $V^* = 2\ I_D / g_m$ (but $V^* \neq V_{dsat}$)

Design Example

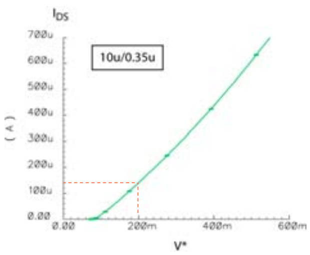
<u>Example</u>: Common-source amp
$a_{v0} > 70$, f_u = 100MHz for C_L = 5pF



- $a_{v0} > 70$ → L = 0.35µm
- $g_m \approx 2\pi f_u C_L = 3.14\text{mS}$
- Pick V* = 200mV

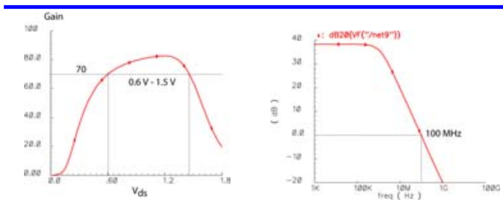
$$I_D = \frac{g_m V^*}{2} = 314\mu\text{A}$$

Device Sizing



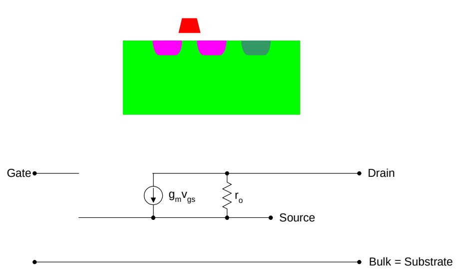
- Pick L 0.35µm
- Pick V* 200mV
- Determine g_m 3.14mS
- $I_D = 0.5\ g_m\ V^* = 314\mu A$
- W from graph (generate with SPICE)
  - → W = 10µm (314µA /141µA) = <u>22µm</u>
- *Create these graphs for several device lengths and flavors*

Common Source Verification

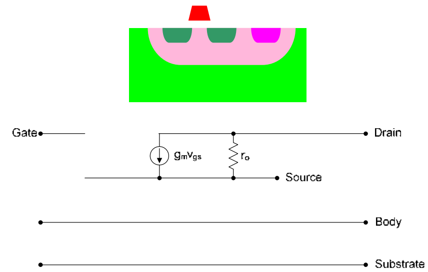


- Amplifier gain > 70; gain-bandwidth "dead on"
- Output range to 0.6V – 1.5V for gain (about ±0.45V swing)
- How did we pick V* = 200mV? Why not 75mV?
  - Need to look at AC model…

Small-Signal AC Model



PMOS AC Model



SPICE Charge Model

- Charge conservation
- MOSFET:
  - 4 terminals: S, G, D, B
  - 4 charges: $Q_S + Q_G + Q_D + Q_B = 0$ (3 free variables)
  - 3 independent voltages: V_{GS}, V_{DS}, V_{SB}
  - 9 derivatives: $C_{ij} = dQ_i / dV_j$, e.g. $C_{G,GS} \sim C_{GS}$
  - C_{ij} != C_{ji}

Ref: HSPICE manual, "Introduction to Transcapacitance", pp. 15:42, Metasoft, 1996.

Small Signal Capacitances

	Weak inversion	Strong inversion linear	Strong inversion saturation
C_{GS}	C_{ol}	$C_{GC}/2 + C_{ol}$	$2/3\ C_{GC} + C_{ol}$
C_{GD}	C_{ol}	$C_{GC}/2 + C_{ol}$	C_{ol}
C_{GB}	$C_{GC} \parallel C_{CB}$	0	0
C_{SB}	C_{jSB}	$C_{jSB} + C_{CB}/2$	$C_{jSB} + 2/3\ C_{CB}$
C_{DB}	C_{jDB}	$C_{jDB} + C_{CB}/2$	C_{jDB}

$$C_{GC} = C_{ox} WL$$

$$C_{CB} = \frac{\varepsilon_{Si}}{x_d} WL$$

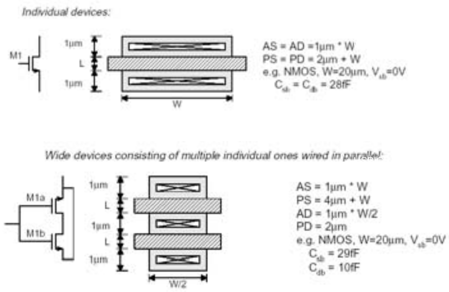
0.35u Process

$$C_{ox} = 5.3\ \text{fF}/\mu\text{m}^2$$

$$C_{olN} = 0.24\ \text{fF}/\mu\text{m}$$

$$C_{olP} = 0.48\ \text{fF}/\mu\text{m}$$

Layout



Source/drain Parasitics and HSPICE

- **ACM=3 model (not in our current library)**
  - **HDIF = half of heavily doped diffusion length**

  - **GEO = 0: No sharing**
  - **GEO = 1: Drain shared**
  - **GEO = 2: Source shared**
  - **GEO = 3: Both shared**

Dynamic Figure of Merit

- **Unity current-gain bandwidth**

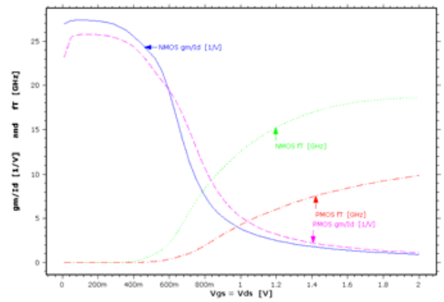
$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}}$$

$$\omega_T = \frac{3}{2}\frac{\mu V_{od}}{L^2} = \frac{3}{2}\omega_0 \quad \text{(Long channel model, } C_{gd}\text{=0)}$$

- **For degenerate short channel device**

$$\omega_T = \frac{3}{2}\frac{\nu_{sat}}{L} = \frac{3}{2}\frac{1}{\tau_{sat}}$$

Efficiency g_m/I_D versus f_T

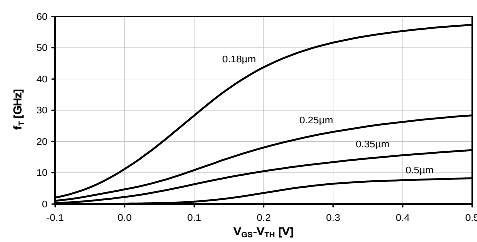


Speed-Efficiency Tradeoff

NMOS faster than PMOS

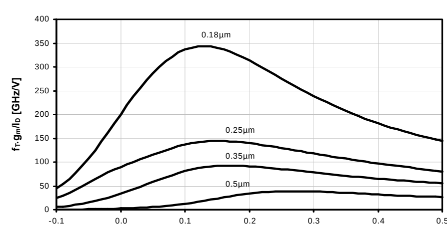
0.35u Process

Device Scaling



Short channel devices significantly faster

Composite Figure-of-Merit: $f_T \cdot g_m/I_D$



Peak performance for low V_{GS}-V_{TH} (implies low V*)

- **Guides choice of V*: if in doubt,**

Small Signal Design Summary

- Determine g_m (from design objectives)
- Pick L
  - Short channel → high f_T
  - Long channel → high r_o, a_{v0}, better matching
- Pick $V^* = 2I_D/g_m$ based on qualitative interpretation
  - Small V* → large signal swing, high current efficiency
  - High V* → high f_T, lower device parasitics
  - Also affects noise (see later)
- Determine I_D (from g_m and V*)
- Determine W (SPICE / plot) ← takes care of short channel effects, etc.
- Accurate for short channel devices → key for design