TSMC 0.18um MM/RF PDK Reference Manual

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Shanghai IC Tech. &Ind. Promotion Center
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This document gives important information and notice regarding this release of PDK. Users who want or plan to use this PDK should read the entire document first.

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1. Important switches for RF devices (in CDF)

This section introduce some important switches contains in RF device's CDFs which may significantly affect the simulation accuracy or LVS.

A. Hard_constrains : default is ON (checked)

This switch provides the flexibility to enable/disable the lower-bond and upper-bond checks for each user-specified parameter in CDF (for example, the W/L of a MOSFET). The lower-bond and upper-bond values for each parameter are usually set according to the parameter valid range described in spice model card or design rule manual. Once the 'Hard_constrains' switch is checked (switch ON), the user-input value for each parameter will be checked with its lower-bond and upper-bond. If the user-input value is smaller than the lower-bond value for a parameter, PDK will issue an error message in the CIW window and reset the value back to the lower-bond value. On the other hand, if the user-input value is greater than the upper-bond value of a parameter, PDK will also issue an error message in the CIW window and reset the value of that parameter back to the upper-bond value. Sometimes, customers may wish to use a special device with its parameter value outside the valid range (for example, a very large MOSFET with W greater than 1000um). At this time, they can switch OFF the 'Hard_constrain' to disable the lower-bond and upper-bond checks and input the W parameter value to '1000um'. Since the 'Hard_constrains' is OFF, the input value wouldn't be set back to the upper-bond value, but PDK will still issue a 'Warnning' message to tell users the input value is outside the valid range and they have to take the risk themselves.

Note: *With 'Hard_constrains' OFF, TSMC wouldn't guarantee the model accuracy and other possible risks that may occurred. Users have to specially take care at this situation and use it with their own risk.*

B. Create_Dummy_Poly : default is ON (checked)

The 'Create_dummy_Poly' switch provides the flexibility to allow users to enable or disable the 'dummy polys' in RF MOSFETs. Once the 'Create_Dummy_Poly' is ON (be checked), the corresponding Pcell layout will contain the 'dummy_poly'. While if it is OFF, the 'dummy polys' on RF MOSFET Pcell layouts will be removed. Please be aware of that: *disable the 'dummy poly' may also affect the accuracy of spice model, users have to take the risk themselves.*

C. Create_Guard_Ring : default is ON (checked)

The 'Create_Guard_Ring' switch provides the flexibility to allow users to enable or disable the NW/DNW guard-ring in Pcell layout (existed in some devices only). If the 'Create_Guard_Ring' switch is ON (be checked), the corresponding

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Pcell layout will contain the NW/DNW guard-ring. But if the 'Crete_Guard_Ring' is OFF, the corresponding Pcell layout wouldn't contain the guard-ring. *For RF devices, the guard-ring may significant affect the accuracy of spice model. Please see the "RF devices special note section" for detail.*

Note: After removing the guard-ring of RF devices, users may still need to create an outer guard-ring to enclose those RF devices. Otherwise, the LVS deck may not be able to recognize those RF devices. For the detail information to create an outer guard-ring, please refer to the document of "RF Devices GuardRing Drawn Guidelines" in directory "<pdk_install_directory/PDK_doc/>".

2. RF devices special note

RF/high frequency application is quite different from the regular baseband designs. Models are strongly layout dependent. Arbitrary changing sample layout can lead to significant design errors. The end results may be substandard circuit performance, or even the designed circuit will fail the design spec. Taking the RF resistors as an example, the DNW guard ring is used to define the substrate network, which is important for high frequency applications. Design frequency or clock rate plays an important factor. In general, if the frequency is lower than 1 GHz, the substrate network is not important. Our recent study indicates the high end may be able to push up to 1.9 GHz. But further verification is required.

In conclusion, high frequency guard ring layout cannot be arbitrary removed. *High frequency circuit simulation accuracy is only guaranteed that circuit is composed with untempered sample layout. Even minor changes to the sample layout may lead to significant simulation errors".*

3. FAQ

i.) The mimcap_rf cell with the metal shield under it doesn't have the DNW guard ring around it but the mimcap_rf without the shield does. Why the difference?

Ans: mimcap_rf with shield, the model can apply for different well (NW, PW, DNW...), however, a little higher parasitical capacitance is shown due to short distance between shield and CBM (capacitor bottom plate). This model also support different metal option applications (1P6M, 1P5M and 1P4M). For without shield case, model only guarantee for DNW underneath. The major difference between these two models is the substrate network.

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ii.) How can I add my own customized devices (or 3rd party IPs) into this PDK?
Ans: Please refer to the document of “Application note for customized cells” located in <pdk_install_direcotry/PDK_doc/>.

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