EECS240 – Spring 2010

Lecture 23: MOS Sample and Hold

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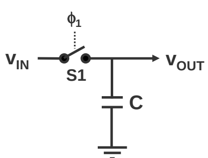
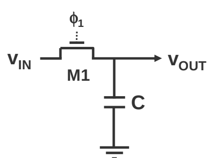
MOS Sample & Hold

Ideal Sampling



- Grab exact value of V_{in} when switch opens

Practical Sampling

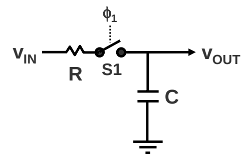


- kT/C noise
- Limited bandwidth
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection
- Clock jitter

Switch Resistance

Acquisition Bandwidth

- Finite switch R → finite bandwidth
- Assuming constant V_{in} and C starts at 0V:



$$v_{out}(t) = v_{in}\left(1 - e^{-t/\tau}\right)$$

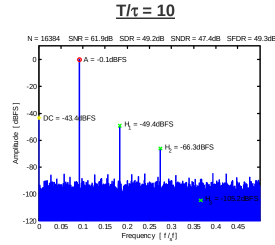
- Leads to min. switch size for given bandwidth, resolution
  - Linear settling calc. – remember may only get T/2
- (Will C always start at 0V?)

Switch R_{on} Non-Linearity

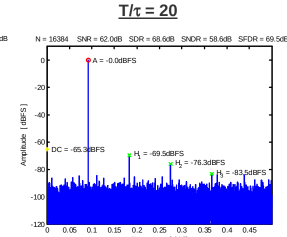
Sampling Distortion

$$v_{out} = v_{in}\left(1 - e^{-\frac{T}{2\tau}\left(1-\frac{v_{in}}{V_{DD}-V_{TH}}\right)}\right)$$

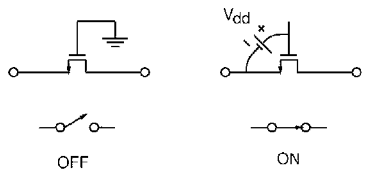
T/τ = 10



T/τ = 20



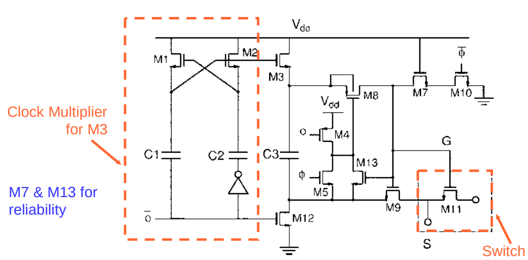
Constant V_{GS} Sampling



- Switch overdrive voltage is independent of signal
- Error from finite R_{ON} is linear (to first order)

Constant V_{GS} Sampling Circuit

Complete Circuit

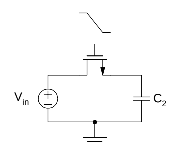


Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

Charge Injection

- "Extra" charge dumped onto holding capacitor
  - Channel charge has to go somewhere
  - (Also get injection through C_{ov})
- Problems:
  - Offset
  - Distortion (error charge is function of V_{IN})

Worst-Case Error Example



channel charge:

$$Q_{CH} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$

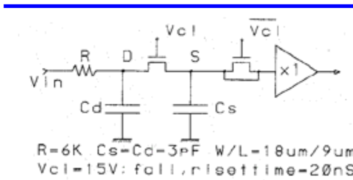
max pedestal error: $V_{in} = V_{SS}$

$$\Delta V = \frac{Q_{CH}}{C_2} = \frac{WLC_{ox}}{C_2}(V_{DD} - V_{SS} - V_{TH})$$

Example:

$$\Delta V = \frac{10 \times 0.35 \times 5}{1000}(3 - 0.6) = \underline{42\text{mV}}$$

Dummy Switch



Vin	UNCOMPENSATED SWITCH	COMPENSATED WITH DUMMY	BALANCED SWITCH
0v	-160mV	-45mV	6mV
5v	-105mV	-30mV	1mV
10v	-40mV	-11mV	0.5mV

- Dummy switch is half width
- Depends on equal split between source and drain
- Is split equal?

Ref: Bienstman et al, JSSC 12/1980, pp. 1051.

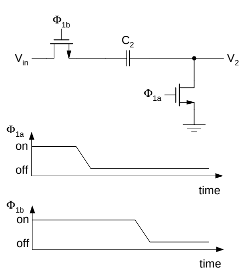
Eichenberger et al, JSSC 8/1989, pp. 1143.

Charge Injection Analysis

- Can perform more detailed, distributed analysis
  - See e.g. Wegmann et al, “Charge Injection in Analog MOS Switches,” IEEE J. Solid-state Circuits, Dec. 1987.
  - Results depend on how fast switch is turned off
- Note that SPICE doesn’t do this (lumped model) – uses “XPART” parameter instead:
  - XPART = 0: Source 60%, Drain 40%
  - XPART = 0.5: equal split
  - XPART = 1: 100% Drain

Rejecting Injection Error

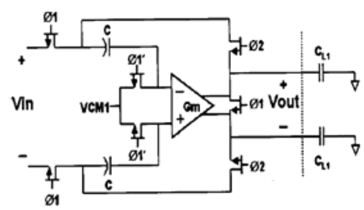
Bottom-Plate Sampling



- Turn off Φ_{1a} first
  - Injected charge is constant
  - Removed in differential output
- Switch Φ_{1b} opens later
  - C_2 disconnected → “zero” charge injected
- Is this useful?
  - V2 = 0V…

Using Bottom-Plate Sampling

Using Bottom-Plate Sampling



Ref: W. Yang, D. Kelly, I. Mehr, M. T. Sayuk, and L. Singer, "A 3-V 340mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE Journal of Solid-State Circuits,* vol. 36, pp. 1931 - 1936, December 2001.