



TSMC18 PDK usage guide:

An introduction on the usage of TSMC process design kits (PDK)

PDK Version: v1.0a Jan .07



Introduction:

- This document describes the TSMC process design kits (PDK) parameterized cell (Pcell) software, which provides a graphical user interface that lets user create parameterized cells for placement in design layout.
- It is assumed that the user is familiar with the development and design of integrated circuits and with the cadence Virtuoso Layout Editor.
- All the information and data contained hereunder constitute TSMC's proprietary and confidential information. Unless TSMC agrees otherwise in writing, you can only use the information contained herein for evaluation purpose. Further, you should treat the information as confidential information and exercise due care to prevent its disclosure to any persons, provided you may disclose it to your employees on a need to know basis in case they agree to similar duty of confidentiality to protect the information herein. You cannot disclose such information to any third party unless TSMC agrees in advance by writing. However, requirements hereunder shall not serve to supersede or change any existing contracts regulating similar issues between you and TSMC.



Overview:

The Symbol Display Information.

This section describes the symbol display information include four terminal NMOS symble, four terminal PMOS symbol, three terminal NMOS symbol, three terminal PMOS symbol, three terminal npn BJT symbol, two terminal diode symbol, two terminal resister symbol, three terminal resister symbol and two terminal varactor symbol.

Device Table

This section show the total device in this PDK. The user can check the page number in the device table to find out the CDF parameter and Pcell function.

- MOS Parameterized Cell Function Introduction
- BJT Parameterized Cell Function Introduction
- Diode Parameterized Cell Function Introduction
- Resistance Parameterized Cell Function Introduction
- Inductor Parameterized Cell Function Introduction
- Varactor Parameterized Cell Function Introduction
- Capacitor Parameterized Cell Function Introduction
- CDF Parameter Description
- Appendix

Appendix A – Stretch Handles Fast link

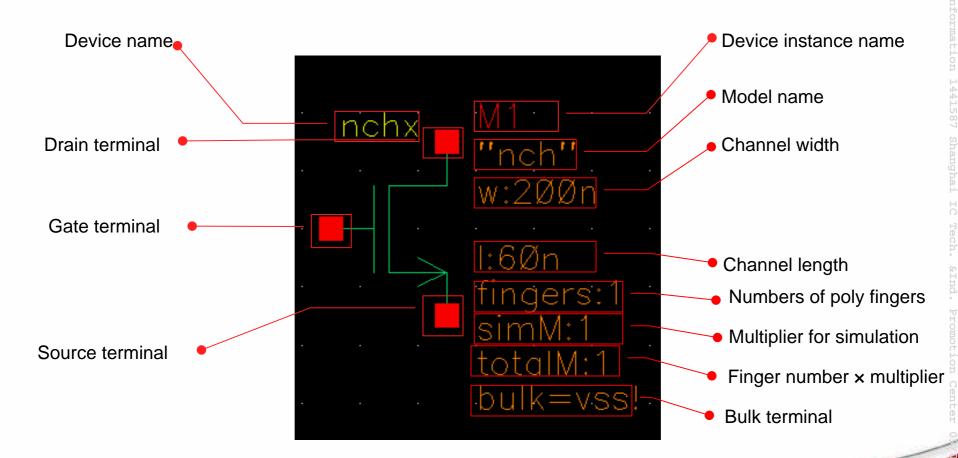
Appendix B – The three terminal MOS substrate pin Fast link

Appendix C – AS AD PS PD NRS NRD methodology Fast link

Appendix D – SA SB methodology Fast link

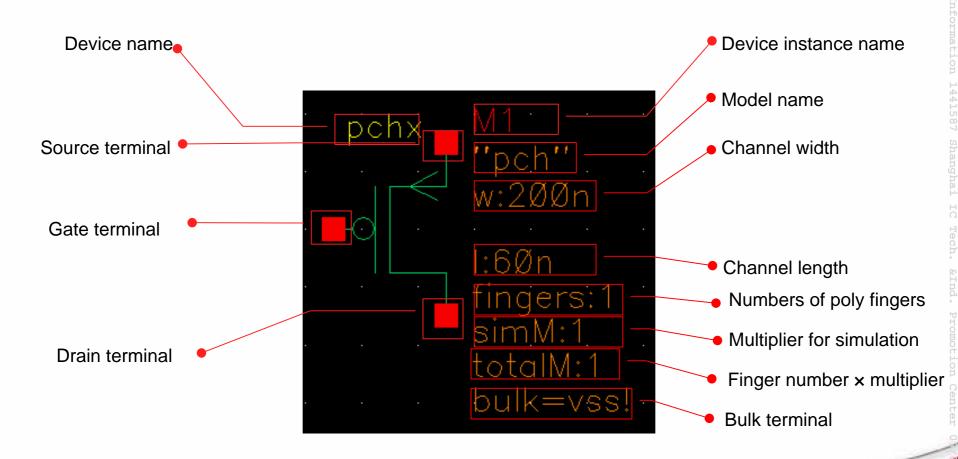


- The Symbol Display Information:
 - The following figure shows the symbol for a 3 terminal NMOS:



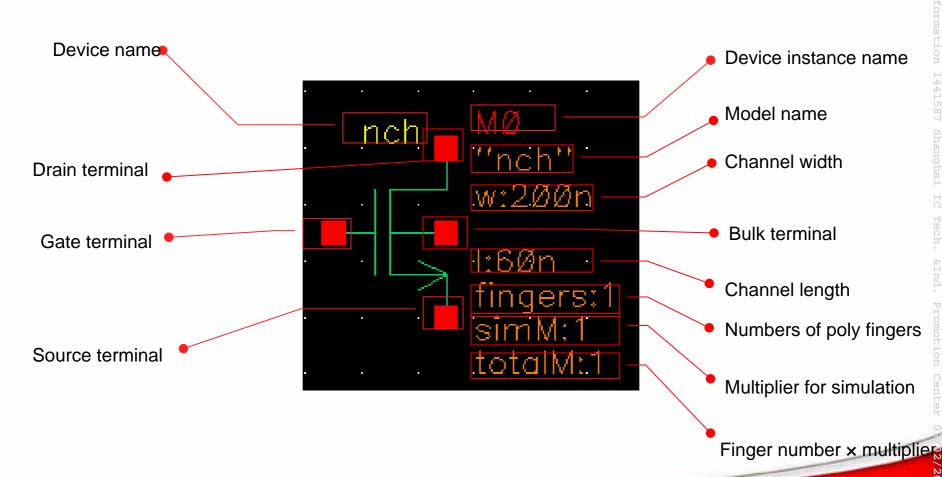


- The Symbol Display Information:
 - The following figure shows the symbol for a 3 terminal PMOS:



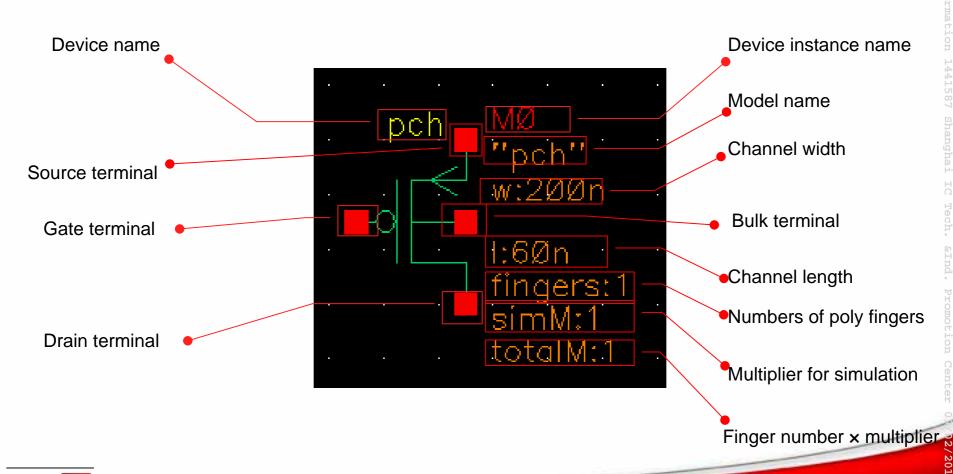


- The Symbol Display Information:
 - The following figure shows the symbol for a 4 terminal NMOS:



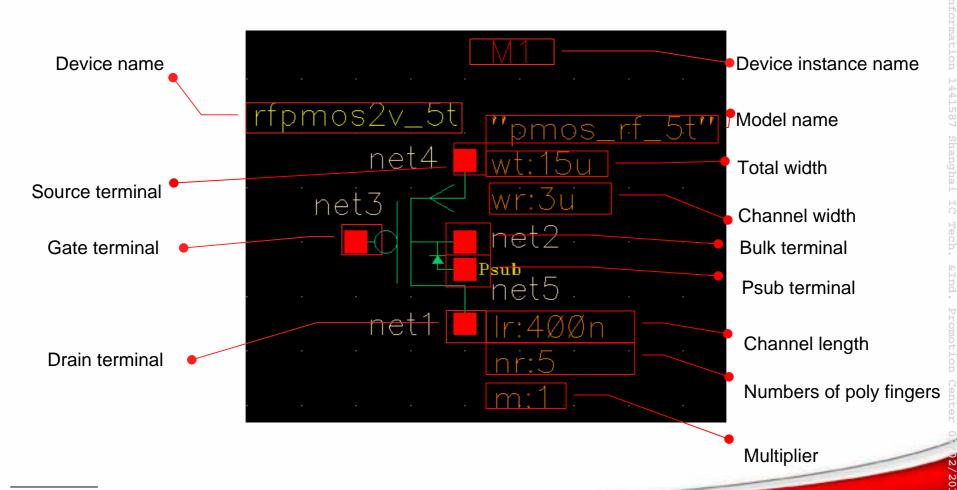


- The Symbol Display Information:
 - The following figure shows the symbol for a 4 terminal PMOS:



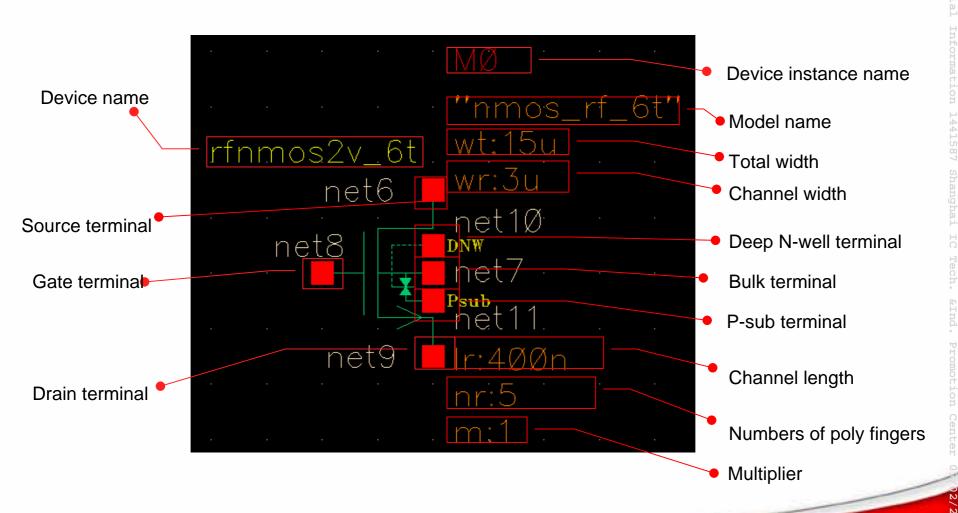


- The Symbol Display Information:
 - The following figure shows the symbol for a 5 terminal RF_PMOS:



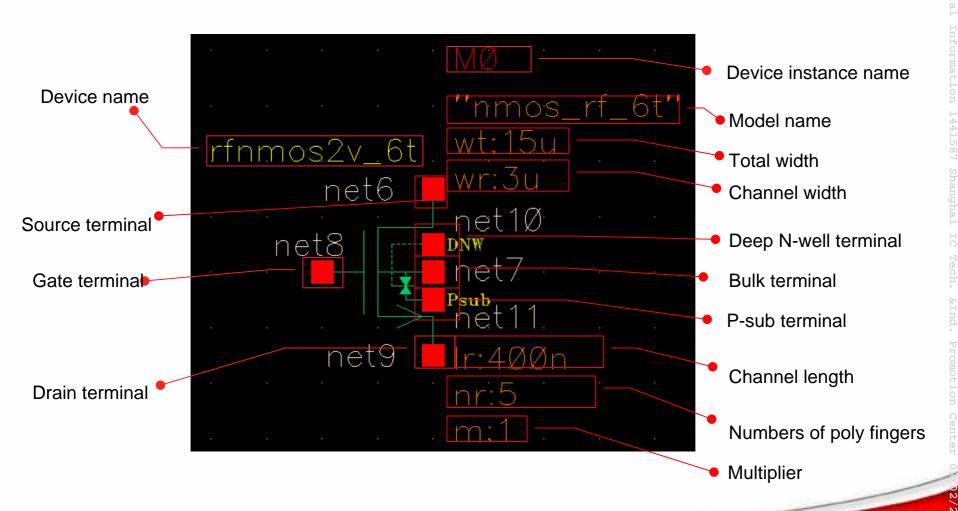


- The Symbol Display Information:
 - The following figure shows the symbol for a 6 terminal RF_PMOS:



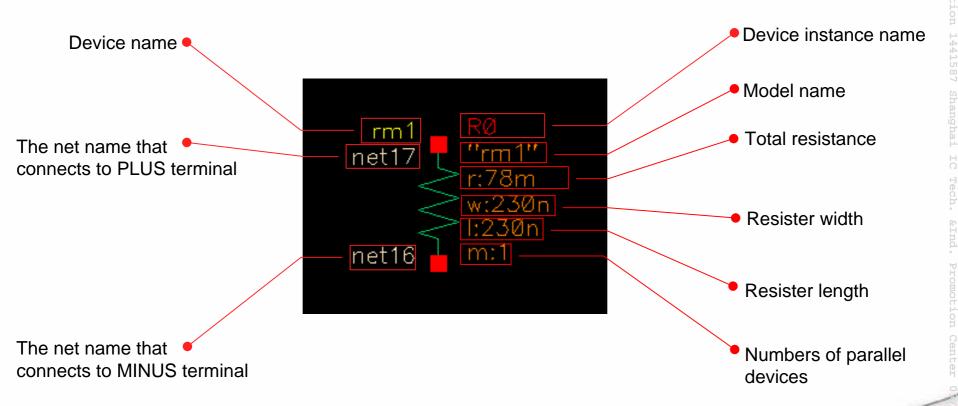


- The Symbol Display Information:
 - The following figure shows the symbol for a 6 terminal RF_PMOS:



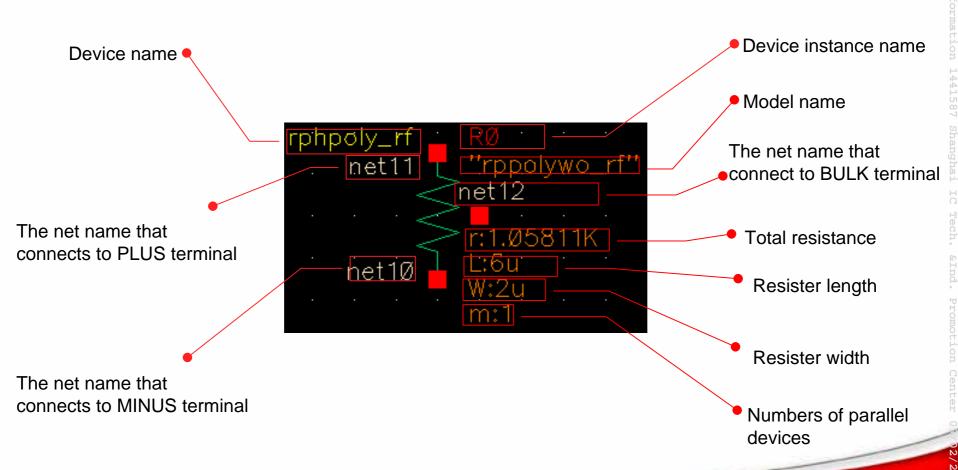


- The Symbol Display Information:
 - The following figure shows the symbol for a 2 terminal resister



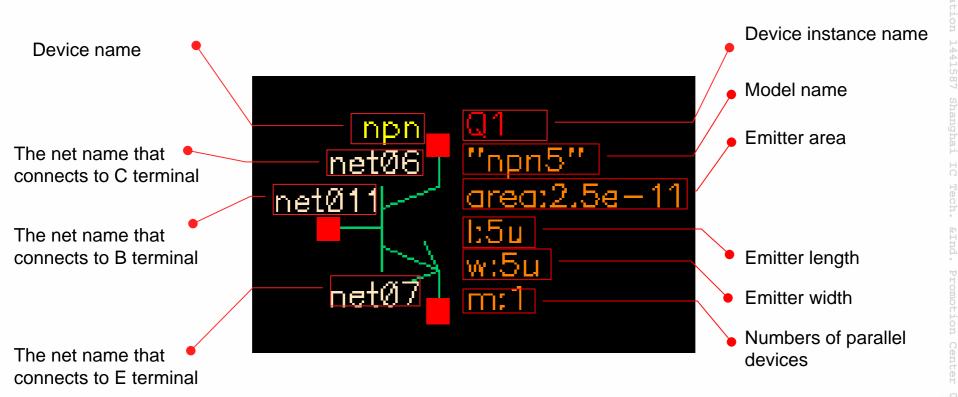


- The Symbol Display Information:
 - The following figure shows the symbol for a 3 terminal resister



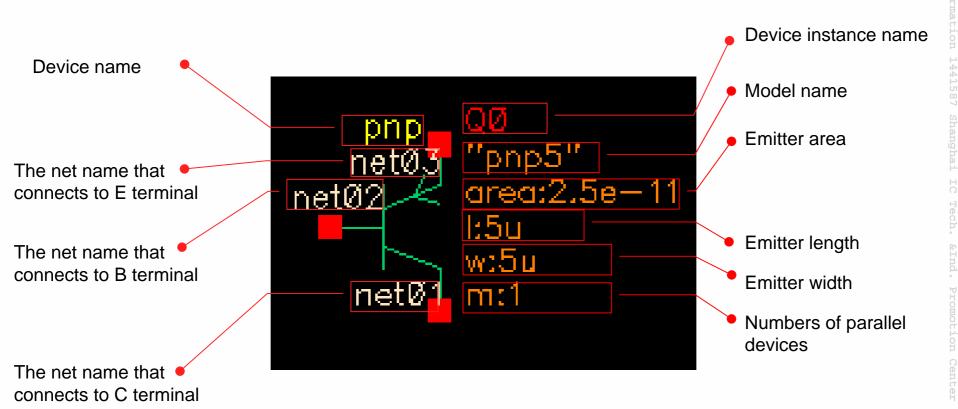


- The Symbol Display Information:
 - The following figure shows the symbol for a 3 terminal npn BJT:



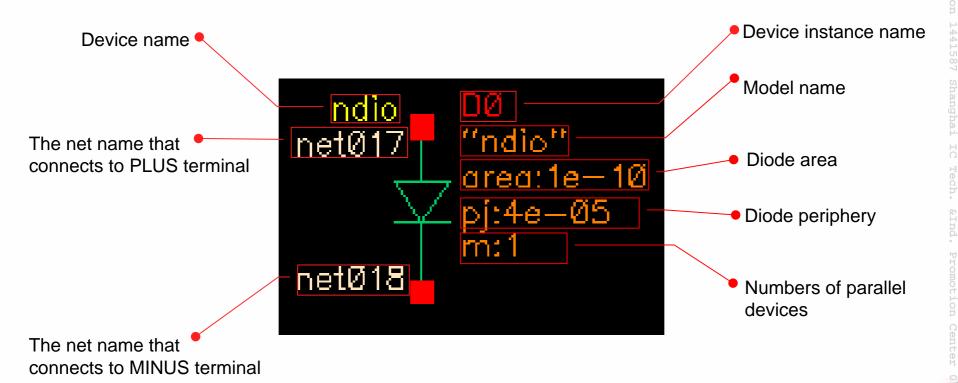


- The Symbol Display Information:
 - The following figure shows the symbol for a 3 terminal pnp BJT:



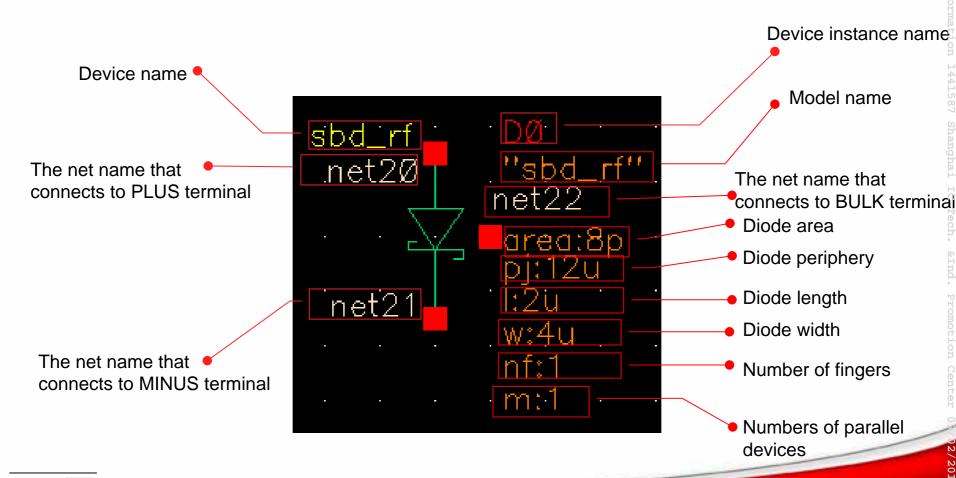


- The Symbol Display Information:
 - The following figure shows the symbol for a 2 terminal diode:



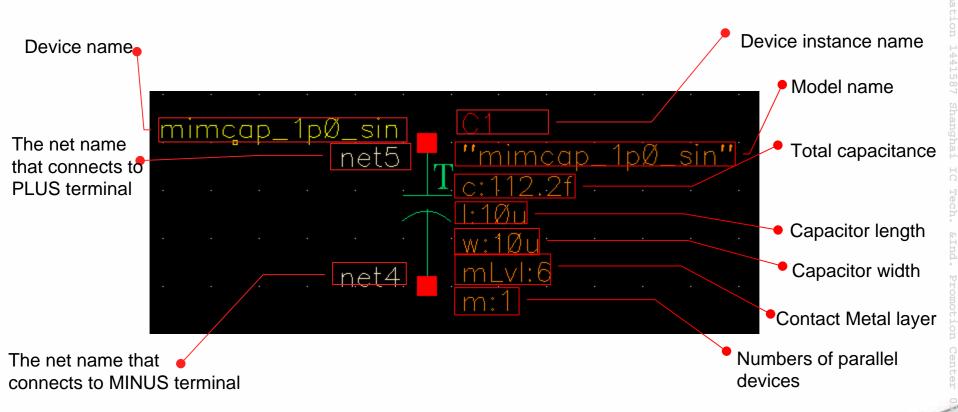


- The Symbol Display Information:
 - The following figure shows the symbol for a 3 terminal diode:



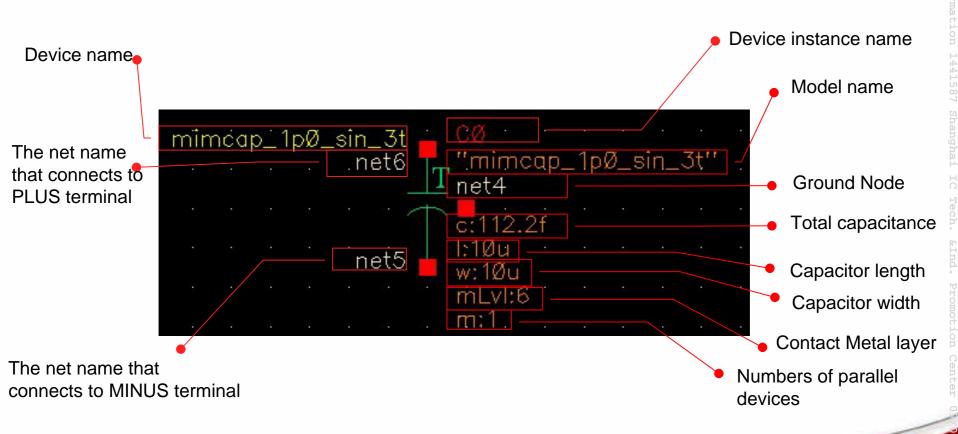


- The Symbol Display Information:
 - The following figure shows the symbol for a 2 terminal capacitor:



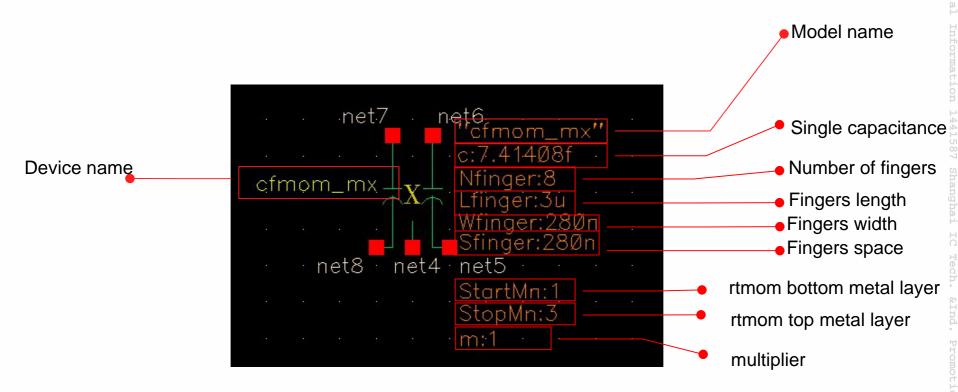


- The Symbol Display Information:
 - The following figure shows the symbol for a 3 terminal capacitor:



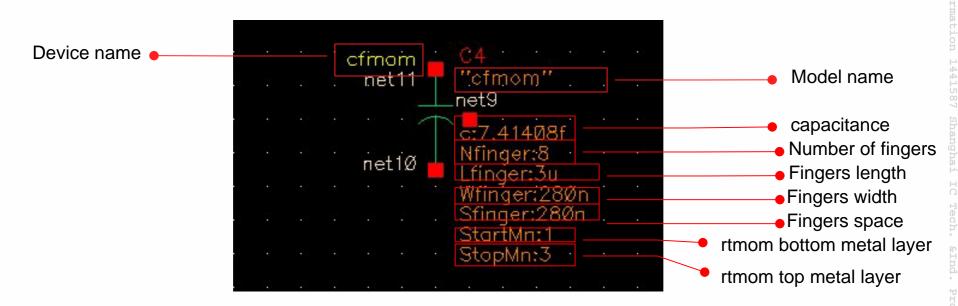


- The Symbol Display Information:
 - The following figure shows the symbol for a 5 terminal capacitor:



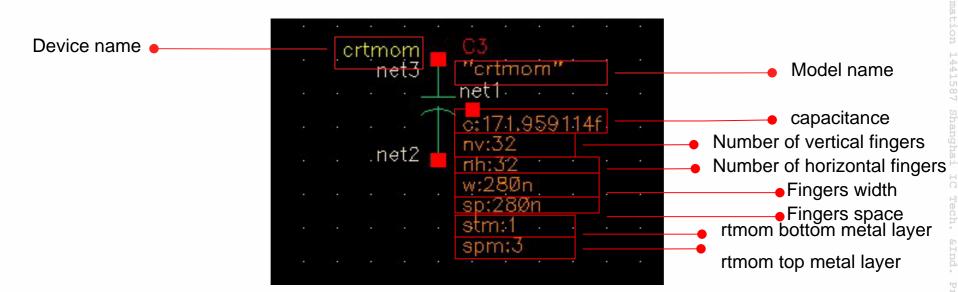


- The Symbol Display Information:
 - The following figure shows the symbol for a 3 terminal capacitor:



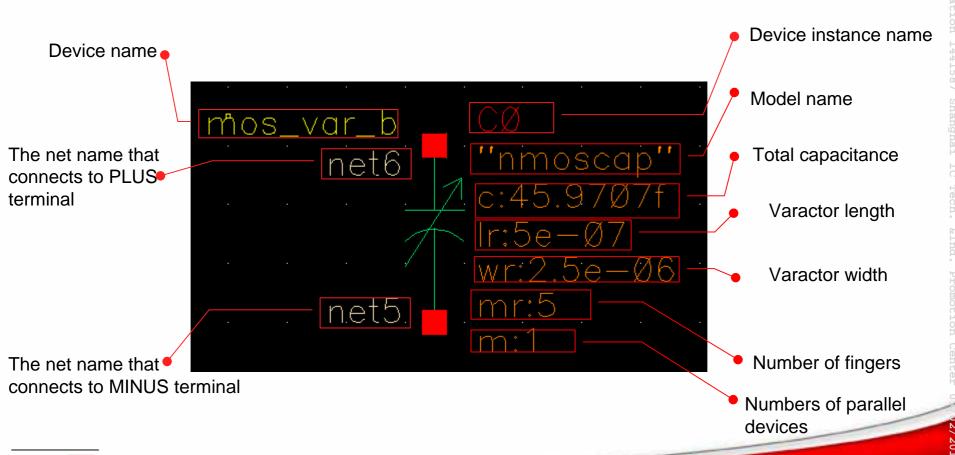


- The Symbol Display Information:
 - The following figure shows the symbol for a 3 terminal capacitor:



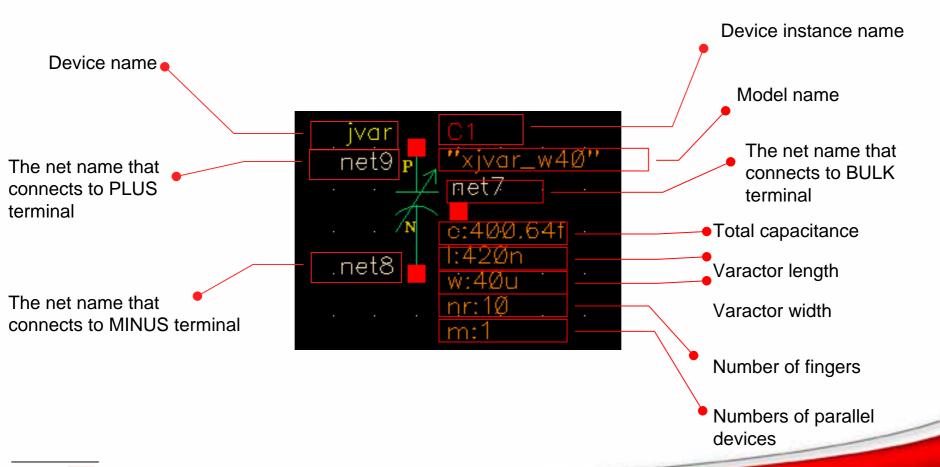


- The Symbol Display Information:
 - The following figure shows the symbol for a 2 terminal varactor:



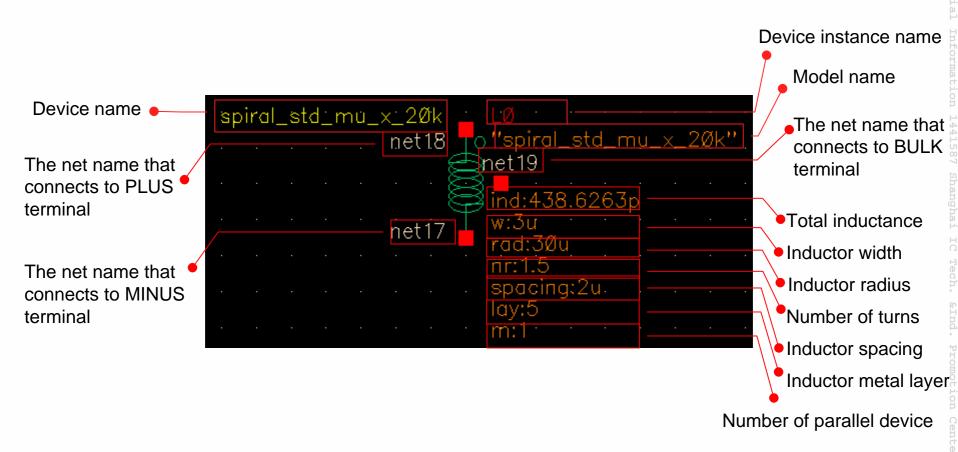


- The Symbol Display Information:
 - The following figure shows the symbol for a 3 terminal varactor:



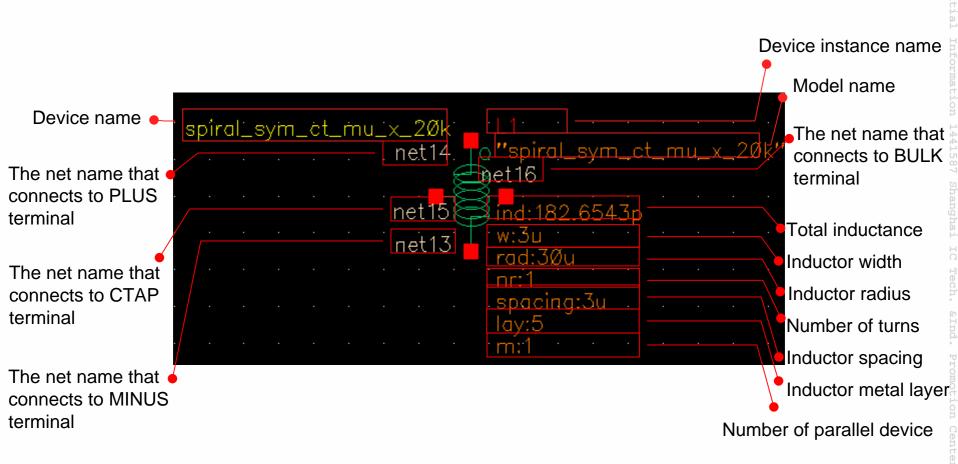


- The Symbol Display Information:
 - The following figure shows the symbol for a 3 terminal inductor:



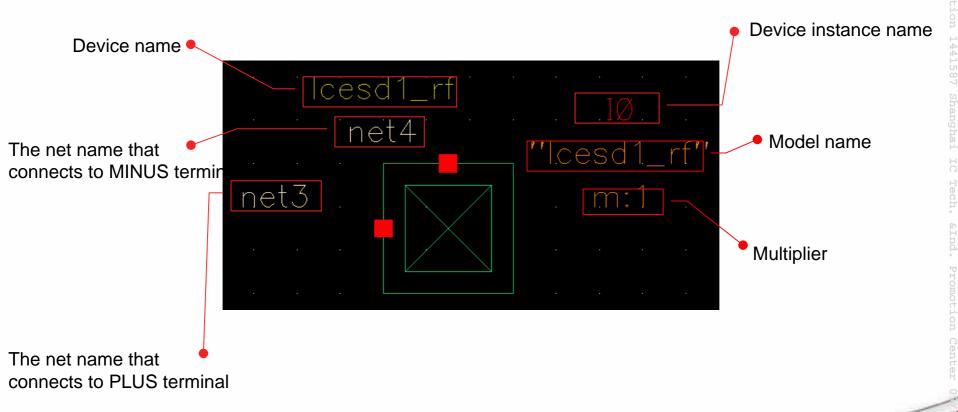


- The Symbol Display Information:
 - The following figure shows the symbol for a 4 terminal inductor:



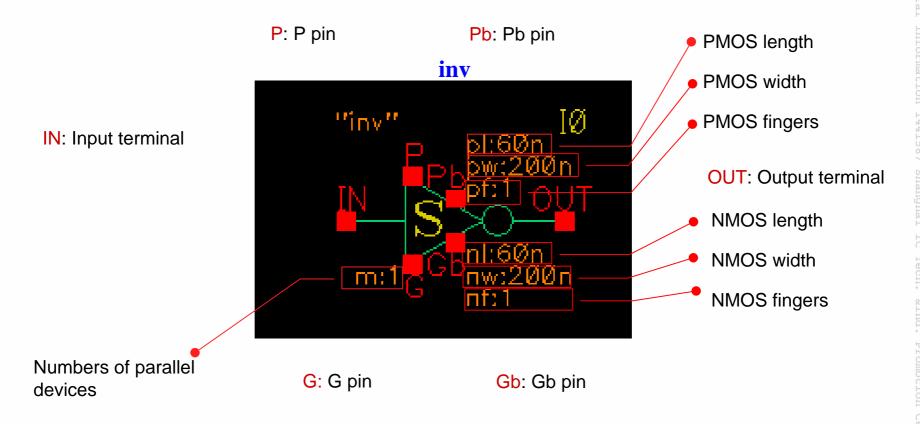


- The Symbol Display Information:
 - The following figure shows the symbol for a 2 terminal pad_device:



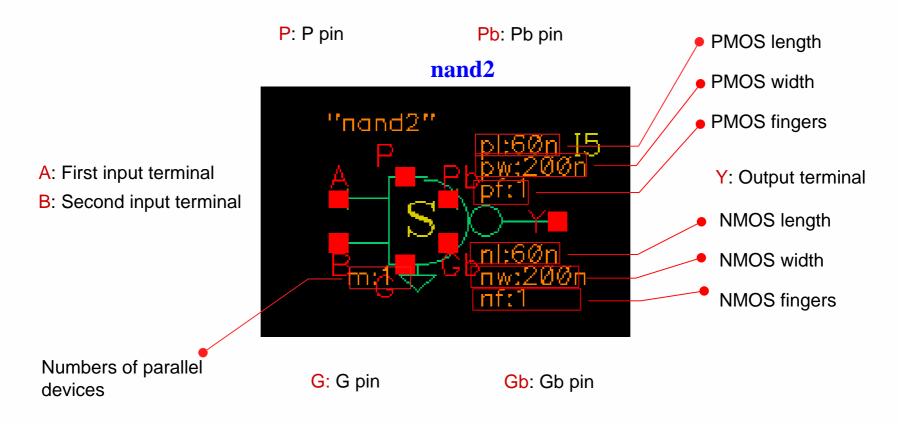


- The Symbol Display Information:
 - The following figure shows the symbol for an inverter gate :



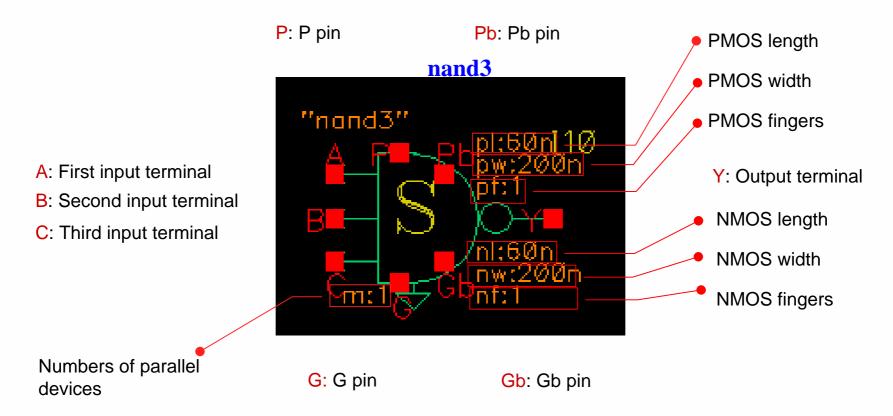


- The Symbol Display Information:
 - The following figure shows the symbol for a nand-2T gate :





- The Symbol Display Information:
 - The following figure shows the symbol for a nand-3T gate :





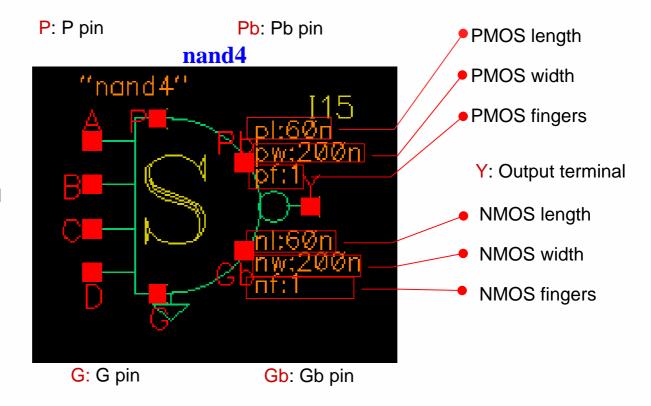
- The Symbol Display Information:
 - The following figure shows the symbol for a nand-4T gate :

A: First input terminal

B: Second input terminal

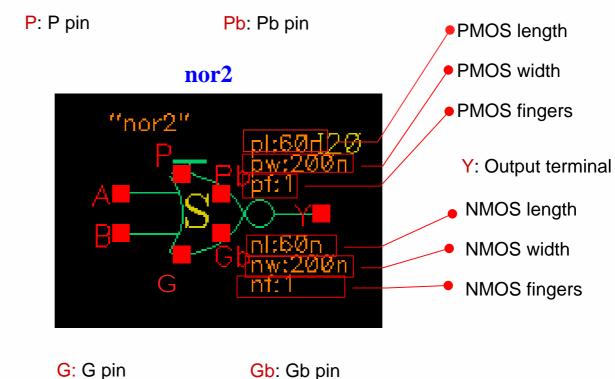
C: Third input terminal

D: Fourth input terminal





- The Symbol Display Information:
 - The following figure shows the symbol for a nor-2T gate :



A: First input terminal

B: Second input terminal



- **The Symbol Display Information:**
 - The following figure shows the symbol for a nor-3T gate:

P: P pin Pb: Pb pin PMOS length nor3 PMOS width PMOS fingers "nor<u>3</u> Y: Output terminal NMOS length NMOS width NMOS fingers

B: Second input terminal

A: First input terminal

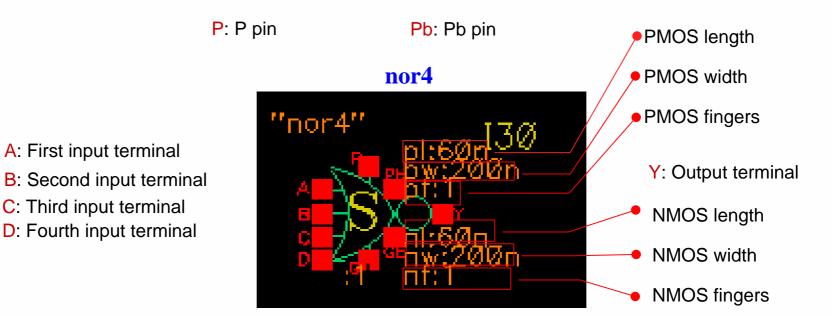
C: Third input terminal

G: G pin

Gb: Gb pin



- The Symbol Display Information:
 - The following figure shows the symbol for a nor-4T gate :

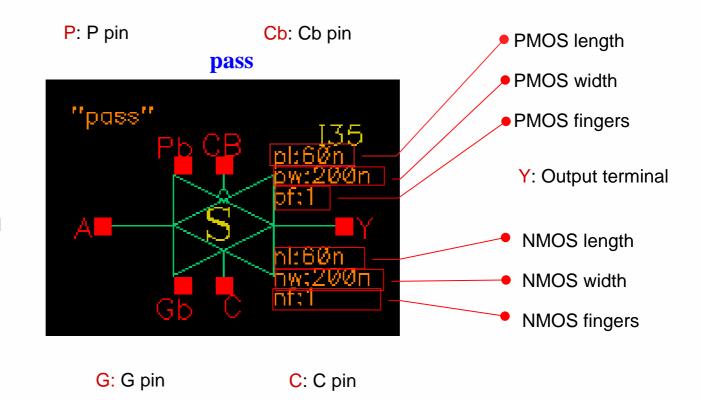


G: G pin

Gb: Gb pin



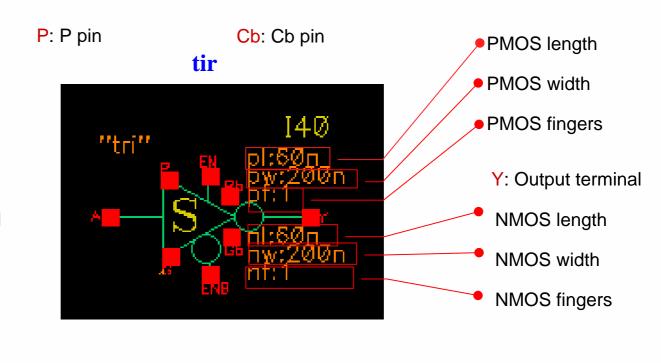
- The Symbol Display Information:
 - The following figure shows the symbol for a pass gate :



A: First input terminal



- The Symbol Display Information:
 - The following figure shows the symbol for a Tri state inverter gate:



A: First input terminal

G: G pin

C: C pin

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Device Table:

The devices in this PDK are list as below table:

Categories	Device
Bipolar	npn, npn_mis, vpnp, vpnp3, vpnp_mis
Capacitor_BB	crtmom, cfmom, cfmom_mx, mimcap_1p0_sin_3t, mimcap_1p0_sin,
	mimcap_2p0_sin_3t, mimcap_2p0_sin
Capacitor_rf	mimcap_rf_2p0, mimcap_rf_40k_2p0, cfmom_rf
Diode	dioden, dioden3v, diodenw, diodenw3v, diodep, diodep3v, ndio_m, ndio_3m, pdio_m
	sbd_rf, sbd_rf_nw
Mos	nmos2vx, nmos2vdnwx, nmos3vx, nmos3vdnwx, nmosmvt2vx, nmosmvt3vx,
	nmosnvt2vx, nmosnvt3vx, pmos2vx, pmos3vx, pmosmvt2vx, nmos2v_macx,
	nmos3v_macx, nmosmvt2v_macx, pmos3v_macx, pmosmvt2v_macx,
	nmosmvt3v_macx, nmosnvt2v_macx, nmosnvt3v_macx, pmos2v_macx,
	nmos2v, nmos2vdnw, nmos3v, nmos3vdnw,
	nmosmvt2v, nmosmvt3v, nmosnvt2v, nmosnvt3v, pmos2v, pmos3v, pmosmvt2v
Mos_rf	rfnmos2v, rfnmos3v, rfpmos2v, rfpmos2v_nw, rfpmos3v_nw,
	rfpmos2v_5t, rfpmos2v_nw_5t, rfpmos3v_5t, rfpmos3v_nw_5t,
	rfnmos2v_6t, rfnmos3v_6t,
Mos_mac	pmosmvt2v_mac, nmos2v_mac, nmos3v_mac, nmosmvt2v_mac, nmosmvt3v_mac,
	nmosnvt2v_mac, nmosnvt3v_mac, pmos2v_mac, pmos3v_mac
Res	rm1, rm2, rm3, rm4, rm5, rmt, rmu_40k
	rnhpoly, rpplus_2t, rphpoly, rnlplus_2t, rnlpoly,
	rnplus_2t, rnwell, rnwod_2t, rphripoly, rplplus_2t, rplpoly,
	rnhpoly_dis, rnlplus, rnlpoly_dis, rnplus, rnwod, rnwsti_m, rphpoly_dis, rphripoly_dis,
	rphripoly_rf, rplpoly_rf, rphpoly_rf, rplplus, rplpoly_dis, rpplus
Special divice	dio_dnwpsub, dio_pwdnw, diodesd3v
Varactor	mos_var_b, mos_var_b3, jvar, moscap_rf, moscap_rf_nw, moscap_rf33, moscap_rf33_nv



Device Table:

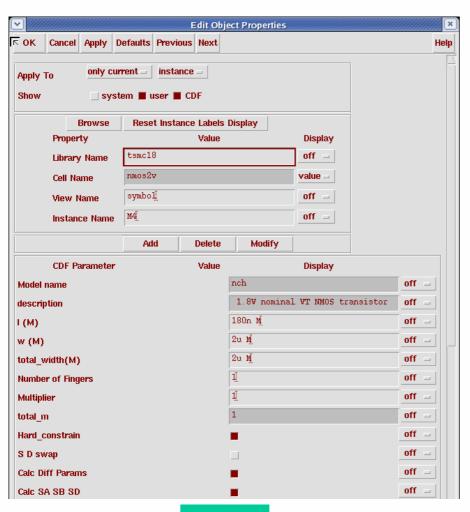
■ The devices in this PDK are list as below table:

Logic Gates	Device
pass	pass_2v, pass_3v, pass_mvt2v, pass_2v_mac, pass_3v_mac, pass_mvt2v_mac,
Tri	tri_2v, tri_3v, tri_mvt2v, tri_2v_mac, tri_3v_mac, tri_mvt2v_mac,
Nor	nor2_2v, nor2_3v, nor2_mvt2v, nor3_2v, nor3_3v, nor3_mvt2v, nor4_2v, nor4_3v,
	nor4_mvt2v, nor2_2v_mac, nor2_3v_mac, nor2_mvt2v_mac, nor3_2v_mac,
	nor3_3v_mac, nor3_mvt2v_mac, nor4_2v_mac, nor4_3v_mac, nor4_mvt2v_mac
Nand	nand2_2v, nand2_3v, nand2_mvt2v, nand3_2v, nand3_3v, nand3_mvt2v, nand4_2v,
	nand4_3v, nand4_mvt2v, nand2_2v_mac, nand2_3v_mac, nand2_mvt2v_mac,
	nand3_2v_mac, nand3_3v_mac, nand3_mvt2v_mac, nand4_2v_mac, nand4_3v_mac,
	nand4_mvt2v_mac
Inv	inv_2v, inv_3v, inv_mvt2v, inv_2v_mac, inv_3v_mac, inv_mvt2v_mac
	Device
PAD	lcesd1_rf, lcesd2_rf
Inductor	spiral_std_mu_x_20k, spiral_sym_mu_x_20k, spiral_sym_ct_mu_x_20k,
	spiral_std_mu_x_40k, spiral_sym_mu_x_40k, spiral_sym_ct_mu_x_40k



MOS Parameterized Cell Function Introduction:

■ The schematic component description format (CDF) parameter in MOS are list as below:



◆ Model name: Display Model name information.

(These parameters can't be modify in CDF form)

◆ **Description:** Display device description.

(These parameters can't be modify in CDF form)

- ◆L (M): Channel length of the device.
- ♦W (M): Channel width of the device.
- ◆Total_width(M): Total channel width of this device, equal to width x fingers.
- ◆ Number of Fingers_(N): Numbers of poly fingers.

Check here for more information

◆ Multiplier: Numbers of parallel MOS device.

Check here for more information

◆Total_m: Display numbers of parallel MOS device.

(This parameter can't be modify in CDF form)

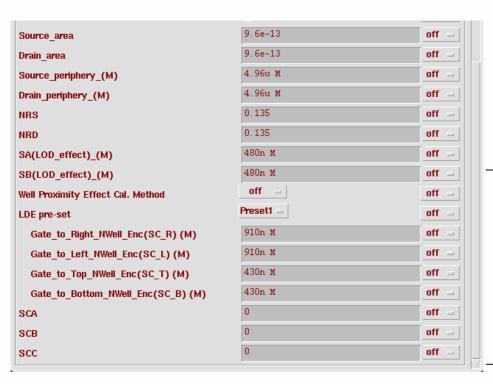
- ◆ Hard_constrain: This function provides an option to constrain the value for each parameter in this device.
- ◆S D swap: Enable this function to swap source and drain terminal
- **◆Calc Diff Params:** The switch provide to modify simulation parameters.
- ◆Calc SA SB SD: The switch provide to modify simulation SA, SB and SB.



MOS Parameterized Cell Function Introduction:

The schematic component description format (CDF) parameter in MOS are list as below:

Front page

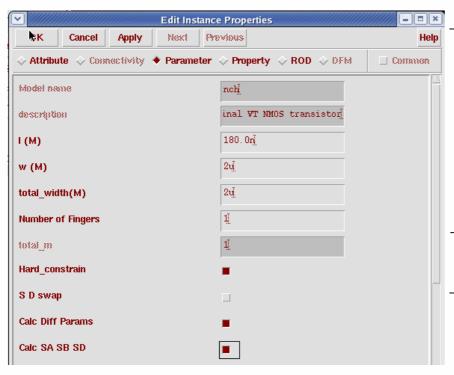


- ◆Source_area: Source area (AS) for simulate use.
- ◆Drain_area: Drain area (AD) for simulate use.
- ◆Source_periphery: Source periphery (PS) for simulate use.
- ◆ **Drain_periphery:** Drain periphery (PD) for simulate use.
- ◆NRS: Number of squares source resistance for simulate use.
- ◆NRD: Number of squares drain resistance for simulate use.
- ◆SA(LOD_effect)_(M): LOD effect parameter for simulate use.
- ◆SA(LOD_effect)_(M): LOD effect parameter for simulate use.
- ◆LDE pre-set: MOS LDE effect pre-set parameter, Gate to
 N-well enclosure distance for simulate use.
- ◆SCA (M): WPE SCA parameter. for simulate use
- ◆SCB (M): WPE SCB parameter. for simulate use
- ◆SCC (M): WPE SCC parameter. for simulate use

Check here for more information



- MOS Parameterized Cell Function Introduction:
 - The **layout** component description format (CDF) parameter in MOS are list as below:



Next page

◆ Model name: Display Model name information.

(These parameters can't be modify in CDF form)

- **◆Description:** Display device description.
- (These parameters can't be modify in CDF form)
- ◆L (M): Channel length of the device.
- ◆W (M): Channel width of the device.
- ◆Total_width(M): Total channel width of this device, equal to width x fingers.
- ◆ Number of Fingers_(N): Numbers of poly fingers.

Check here for more information

◆Total_m: Display numbers of parallel MOS device.

(This parameter can't be modify in CDF form)

- ◆ Hard_constrain: This function provides an option to constrain the value for each parameter in this device.
- S D swap: Enable this function to swap source and drain terminal.
- ◆ Calc Diff Params: The switch provide to modify simulation parameters. Check here for more information
- ◆Calc SA SB SD: The switch provide to modify simulation SA, SB and SB.



MOS Parameterized Cell Function Introduction:

The layout component description format (CDF) parameter in MOS are list as below:

Front page

Source_area	9. 6e-13i
Drain_area	9. 6e-13 <u>̃</u>
Source_periphery_(M)	4.96 <u>u</u> į
Drabi_Jierijihery_(M)	4.96 <u>u</u> į
HRS	0.135
NRD	0.135
SA(LOD_effect)_(M)	480.0r <u>i</u>
SB(LOD_effect)_(M)	480. 0r <u>i</u>
Well Proximity Effect Cal. Method	off =
LDE pre-set	Preset1 =
Gate_to_Right_MWe8_Enc(SC_R) (M)	910r <u>i</u>
Gate_to_Leff_NV/ell_Enc(SC_L) (M)	910r <u>i</u>
Gate_to_Top_HWell_Enc(SC_T) (M)	430r <u>i</u>
Gate_to_Bottom_NVell_Enc(SC_B) (M)	430r <u>i</u>

- ◆Source area: Source area (AS) for simulate use.
- ◆ Drain_area: Drain area (AD) for simulate use.
- ◆Source_periphery: Source periphery (PS) for simulate use.
- ◆ **Drain_periphery:** Drain periphery (PD) for simulate use.
- ◆NRS: Number of squares source resistance for simulate use.
- ◆NRD: Number of squares drain resistance for simulate use.
- ◆SA(LOD_effect)_(M): LOD effect parameter for simulate use. □
- ◆SB(LOD_effect)_(M): LOD effect parameter for simulate use.

♦Well Proximity Effect Cal. Method:

two entry methods for WPE parameters:

off => use model default values.

custom => user input desire value by self.

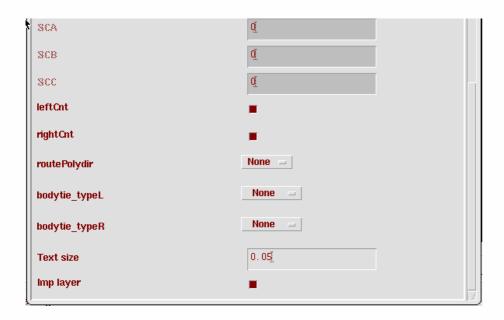
◆LDE pre-set: MOS LDE effect pre-set parameter, Gate to

N-well enclosure distance - for simulate use.



- MOS Parameterized Cell function Introduction:
 - The layout component description format (CDF) parameter in MOS are list as below:





- ◆SCA (M): WPE SCA parameter. for simulate use
- ◆SCB (M): WPE SCB parameter. for simulate use
- ◆SCC (M): WPE SCC parameter. for simulate use
- ◆leftCnt: A option for drawing poly-left diffusion area metal1 connection.
- rigthCnt: A option for drawing poly-right diffusion area metal1 connection.
- routePolydir:(None, Top, Bottom, Both) A option for drawing poly gate connection.

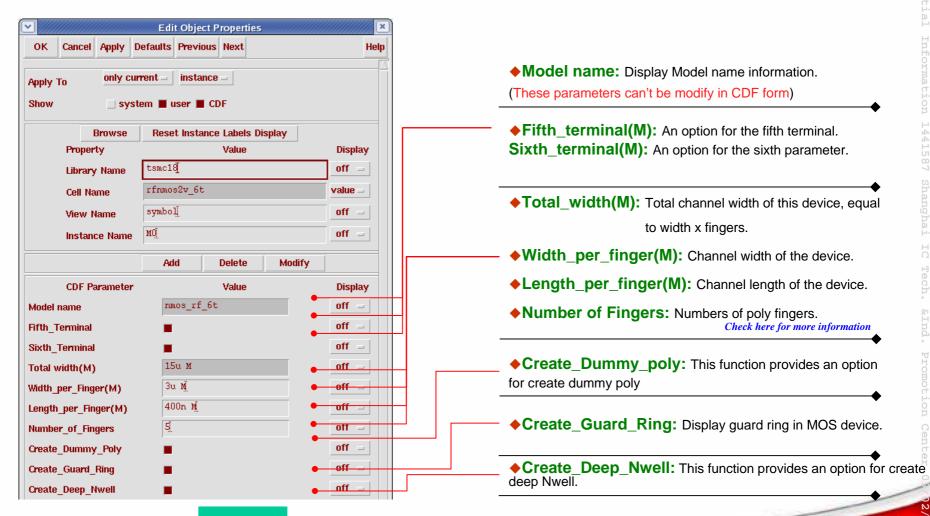
Check here for more information

- bodytie_typeL: (None, Integred, Detached) A option for drawing body connection.
- ◆bodytie_typeR: (None, Integred, Detached) A option for drawing body connection. Check here for more information
- ◆Text size: The function can modify the font value in layout view.
- ◆Imp layer: The function provide a option for well implant.



MOS Parameterized Cell Function Introduction:

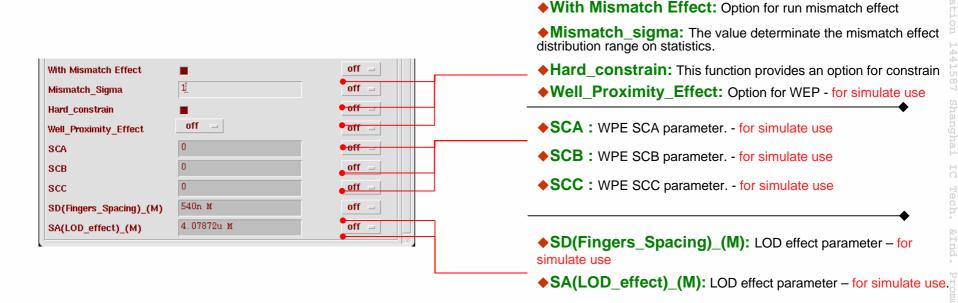
The schematic component description format (CDF) parameter in rf_MOS are list as below:





MOS Parameterized Cell Function Introduction:

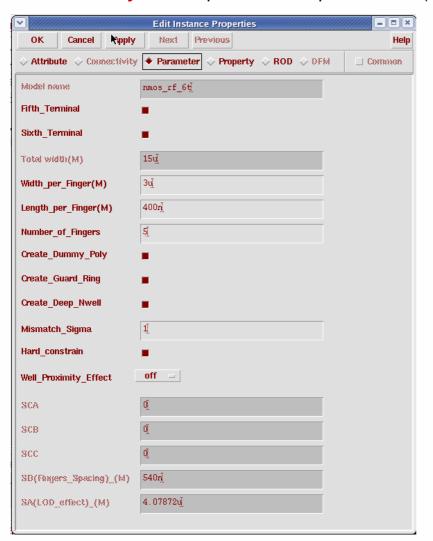
The schematic component description format (CDF) parameter in rf_MOS are list as below:



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MOS Parameterized Cell Function Introduction:

The layout component description format (CDF) parameter in MOS are list as below:



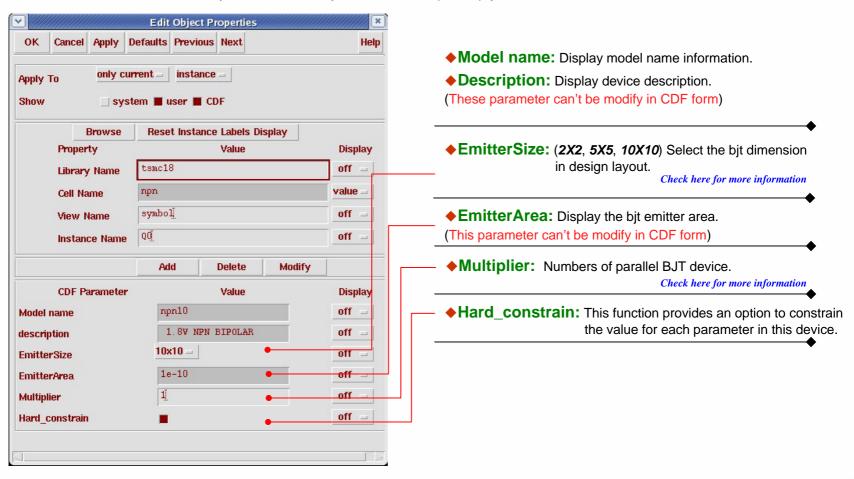
- ◆ Model name: Display Model name information.
- ◆Fifth_terminal(M): An option for the fifth terminal.
- ◆Sixth_terminal(M): An option for the sixth terminal.
- ◆Total_width(M): Total channel width of this device, equal to width x fingers.
- ◆Width_per_finger(M): Channel width of the device.
- ◆Length_per_finger(M): Channel length of the device.
- ◆Number of Fingers: Numbers of poly fingers.
- **◆Create_Dummy_poly:** This function provides an option for create dummy poly
- ◆Create_Guard_Ring: Display guard ring in MOS device.
- ◆Create_Deep_Nwell: An option for create deep Nwell
- ♦ With Mismatch Effect: An option for run mismatch effect
- ◆Mismatch_sigma: The value determinate the mismatch effect distribution range on statistics.
- ◆ Hard_constrain: This function provides an option to constrain
- ♦ Well Proximity Effect: Option for WEP for simulate use
- ◆SCA/SCB/SCC: WPE SCA parameter. for simulate use
- ◆SD(Fingers_Spacing)_(M): LOD effect parameter
- ◆SA(LOD_effect)_(M): LOD effect parameter for simulate use.

(Parameters with pale hue can't be modify in CDF form)



BJT Parameterized Cell Function Introduction:

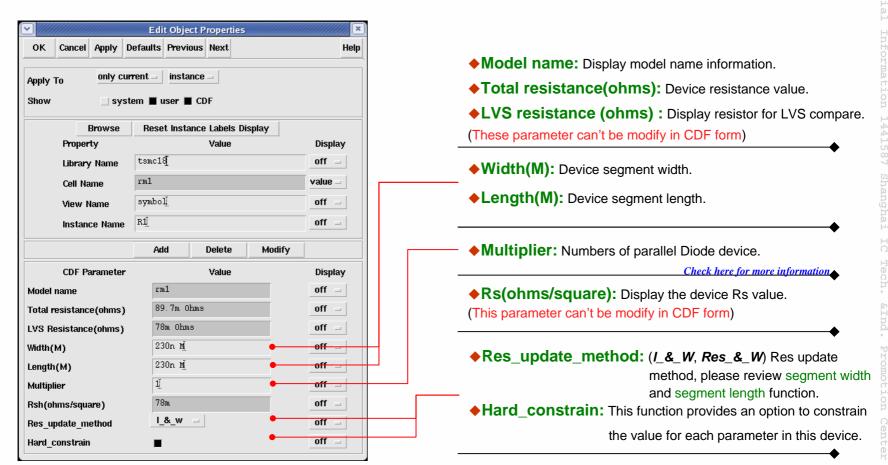
■ The schematic component description format (CDF) parameters in BJT are list as below:





Resistance (1) Parameterized Cell Function Introduction:

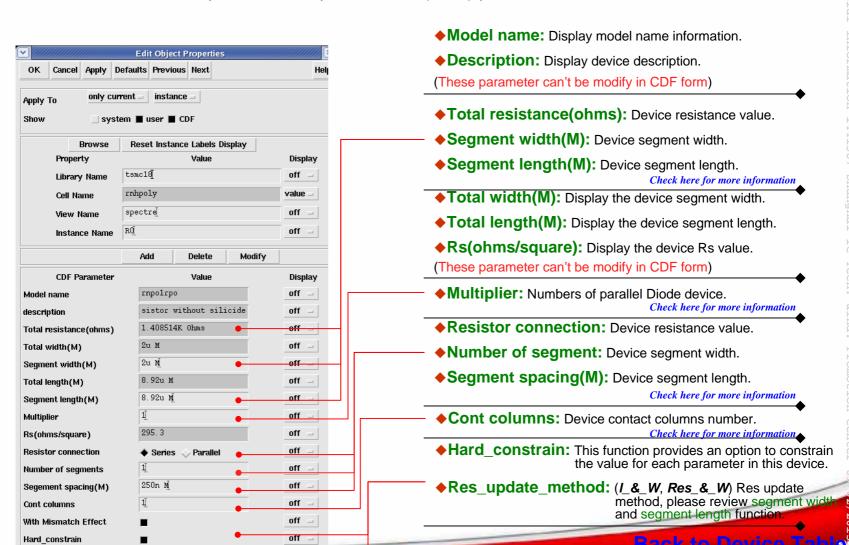
■ The schematic component description format (CDF) parameter in resistance are list as below:





Resistance(2) Parameterized Cell Function Introduction:

■ The schematic component description format (CDF) parameter in resistance are list as below:



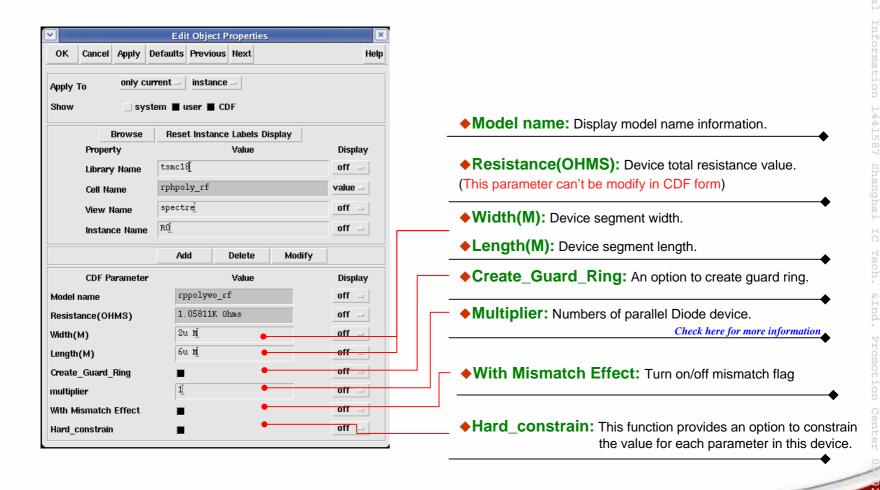
Res update method

1 & w

off =



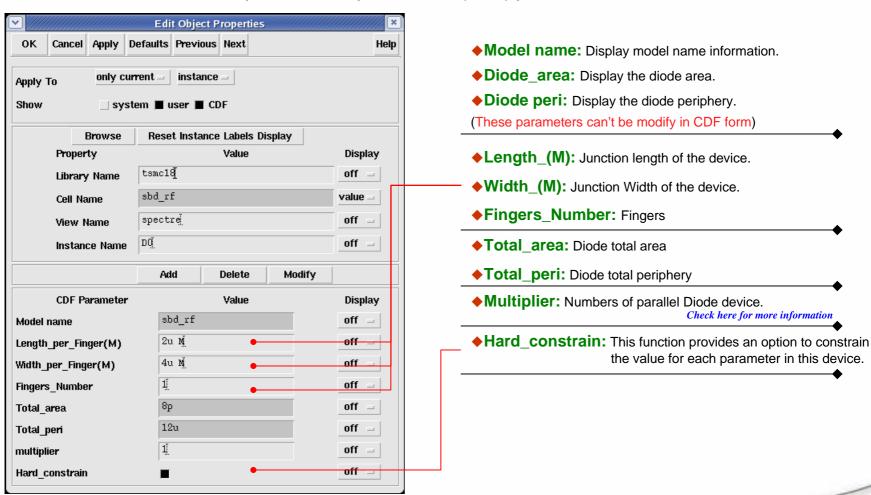
- Resistance(3) Parameterized Cell Function Introduction:
 - The schematic component description format (CDF) parameter in resistance are list as below:





Diode Parameterized Cell Function Introduction:

■ The schematic component description format (CDF) parameters in Diode are list as below:

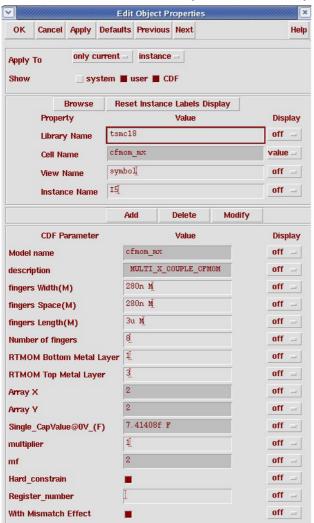




Capacitor(1) Parameterized Cell Function Introduction:

The schematic component description format (CDF) parameters in cfmom_mx are list as below:

layout view.



◆Model name: Display model name information.
◆ Description: Display device description.
(These parameters can't be modify in CDF form)
◆Fingers width: width for each finger
◆Fingers space: space between each finger
◆Fingers length: length for each finger
◆Number of fingers: total numbers of fingers
◆RTMOM Bottom metal layer: set up the bottom metal layer
◆RTMOM TOP metal layer: set up the top metal layer
◆Array X: Numbers of layout blocks in x direction.
Array Y: Numbers of layout blocks in y direction.
◆Single_CapValue@0V(F): Device capacitance information
(This parameter can't be modify in CDF form)
◆ Multiplier: Numbers of parallel cfmom_mx devices. Check here for more information
◆mf: (Array X * Array Y) / 2. (This parameter can't be modify in CDF form)
◆Hard_constrain: This function provides an option to constrain the value for each parameter in this device.

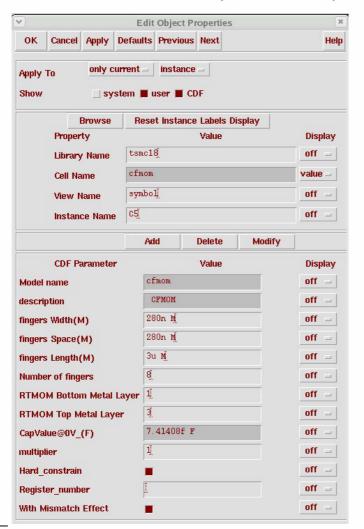
◆ Register number: Need a key from TSMC to display the

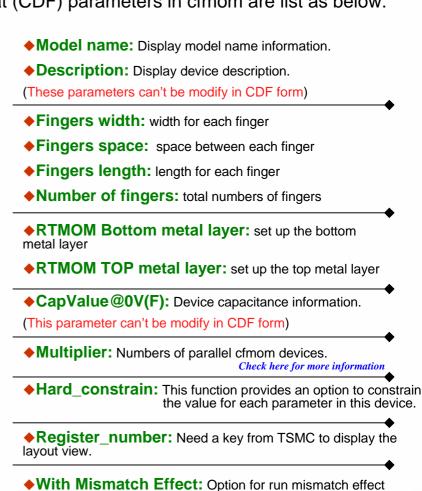
♦ With Mismatch Effect: Option for run mismatch effect.



Capacitor(2) Parameterized Cell Function Introduction:

■ The schematic component description format (CDF) parameters in cfmom are list as below:

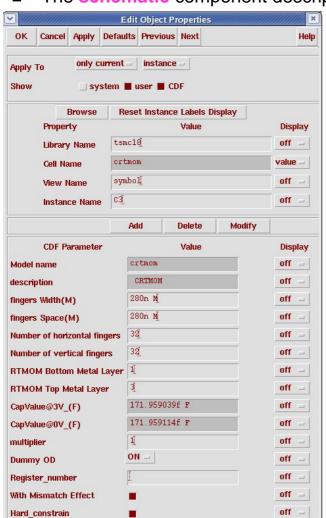






Capacitor(3) Parameterized Cell Function Introduction:

■ The schematic component description format (CDF) parameters in crtmom are list as below:



◆ Model name: Display model name information. **◆ Description:** Display device description. (These parameters can't be modify in CDF form) ◆Fingers width: width for each finger **♦Fingers space:** space between each finger ◆Number of horizontal fingers: total fingers in the horizontal direction ◆ Number of vertical fingers: total fingers in the vertical direction ◆RTMOM Bottom metal layer: set up the bottom metal laver ◆RTMOM TOP metal layer: set up the top metal layer ◆CapValue@3V(F): Device capacitance information. ◆CapValue@0V(F): Device capacitance information. (This parameter can't be modify in CDF form) ◆Multiplier: Numbers of parallel crtmom devices. Check here for more information ◆ **Dummy OD:** Create shading OD to prevent from parasitic effects

layout view.

◆Hard_constrain: This function provides an option to constrain the value for each parameter in this device.

◆ Register number: Need a key from TSMC to display the



Capacitor(4) Parameterized Cell Function Introduction:

■ The schematic component description format (CDF) parameters in mimcap are list as below:

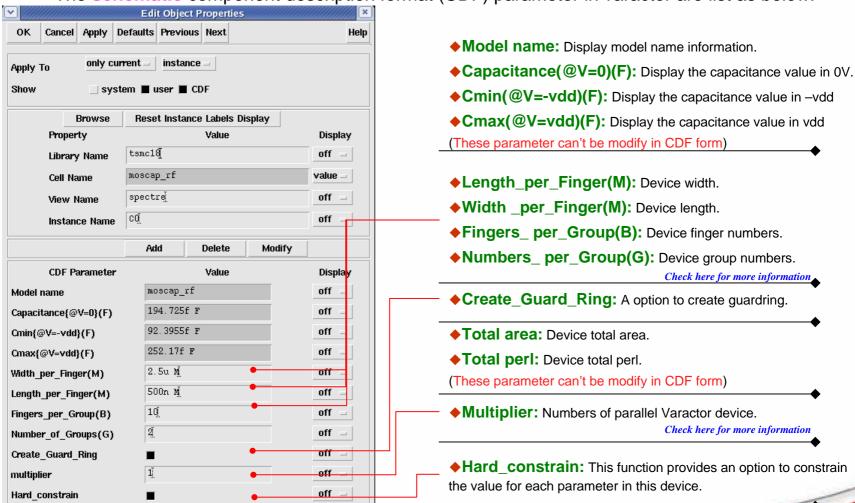


◆ Model name: Display model (This parameter can't be modify in	
◆Entry_method: (<i>I</i> _&_ <i>W</i> , _ <i>c</i> _	 _ , c_&_W) capacitor update
method.	Check here for more information
◆Capacitance: Capacitance in	*
(This parameter can't be modify in	CDF form)
◆Width_(M): Input capacitor m	etal width.
◆Length_(M): Input capacitor	metal length.
◆Create_Leading_terminal	ls: A option to create
	leading terminals.
♦ Leading_terminals_Widtl	h(M): This parameter can be
modify in layout CDF form, use o	can modify the terminal width.
◆Leading_terminals_lengt	:h(M): This parameter can be
modify in layout CDF form, use of	can modify the terminal length. Check here for more information
◆Multiplier: Numbers of paralle	el Capacitor device.
	Check here for more information
♦With Mismatch Effect : Op	tion for run mismatch effect
◆Hard_constrain: This function	on provides an option to constrai
the value f	or each parameter in this device
◆Circuit_under_pad: By add can recognize the device below the	ding dummy layer on mimcap, L\ is mimcap if this switch is turned



Varactor Parameterized Cell Function Introduction:

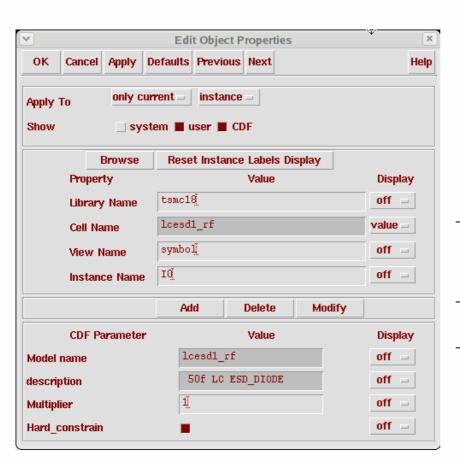
The **schematic** component description format (CDF) parameter in varactor are list as below:





Pad Parameterized Cell Function Introduction:

■ The schematic component description format (CDF) parameter in pad_device are list as below:



- ◆ Model name: Display model name information.
- **◆Description:** Display device description.

(These parameter can't be modify in CDF form)

♦ Multiplier: Numbers of parallel Varactor device.

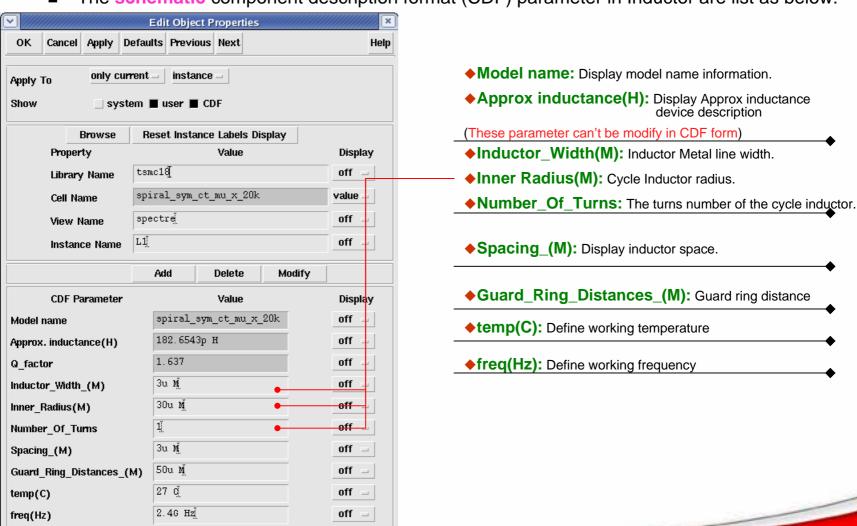
Check here for more information

◆Hard_constrain: This function provides an option to constrain the value for each parameter in this device.



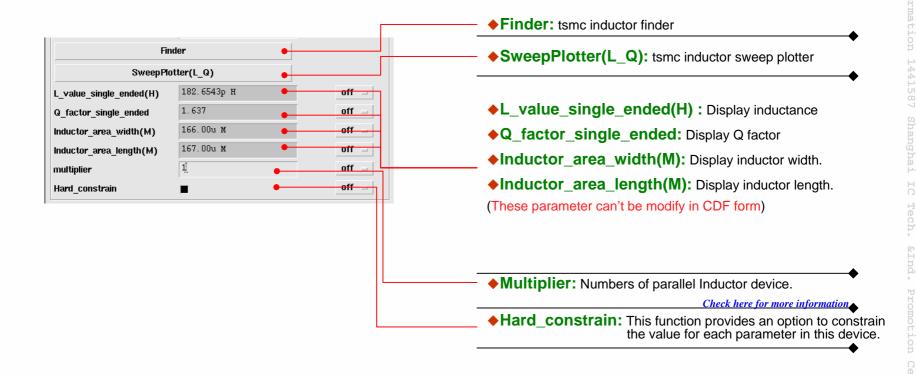
Inductor Parameterized Cell Function Introduction:

The schematic component description format (CDF) parameter in Inductor are list as below:





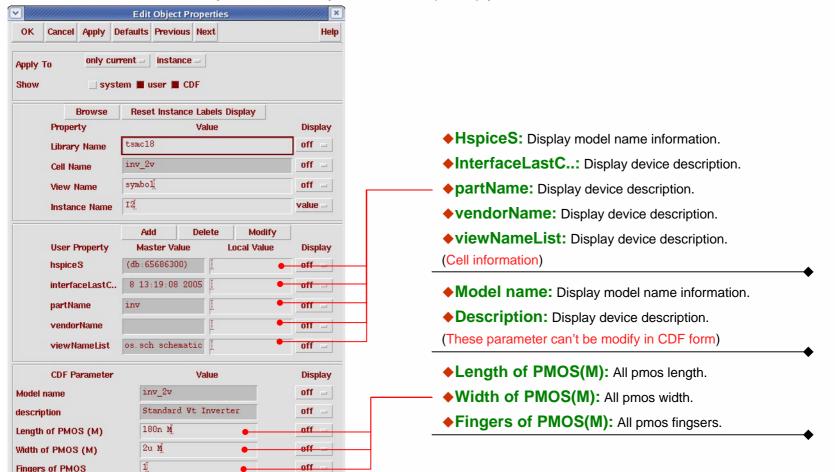
- Inductor Parameterized Cell Function Introduction:
 - The schematic component description format (CDF) parameter in Inductor are list as below:





LogicGate Parameterized Cell Function Introduction:

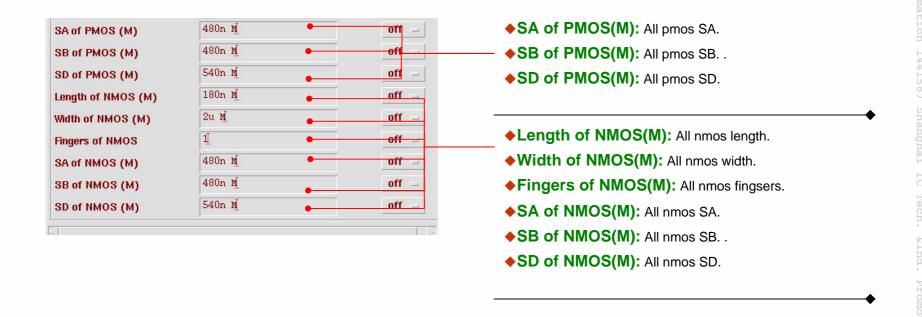
■ The schematic component description format (CDF) parameters in inverter are list as below:





LogicGate Parameterized Cell Function Introduction:

■ The schematic component description format (CDF) parameters in inverter are list as below:





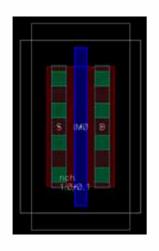
CDF Parameter Description

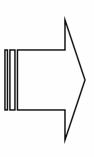
Confidential Security C

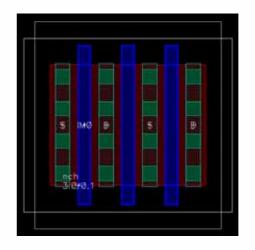
- The function of Number of Fingers_(N)
 - This parameter provide user to increment the poly finger numbers.

Number of Fingers_(N)=1

Number of Fingers_(N) =3

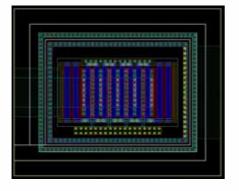


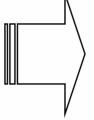


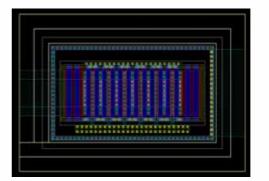


Number of Fingers_(N)=8







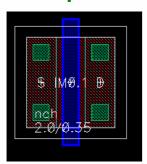


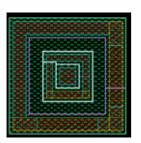
Confidential Security C

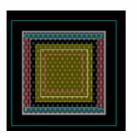
The function of Multiplier

■ This parameter provide user to increment the parallel device.

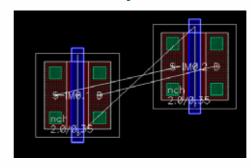
Multiplier = 1

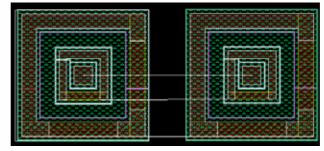


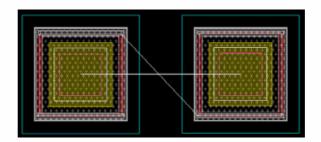




Multiplier = 2







Check here to back to MOS

Check here to back to BJT

Check here to back to Diode

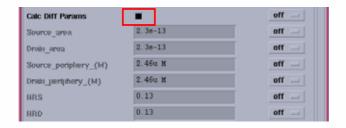
Check here to back to Resistance(1)
Check here to back to Resistance(2)
Check here to back to Varaetor



The function of Calc Diff Params and Calc SA SB SD

■ It's a switch for input simulation parameter that include area of source (AS), area of drain (AD), periphery of source (PS), periphery of drain (PD), number of squares source resistance (NRS), number of squares drain resistance (NRD) and LOD effect parameter- SA, SB and SD. Modify those parameters only influence simulation conditions, the design layout will not have any different.

Calc Diff Params is enable



Parameters can't be modify

Calc Diff Params is disable



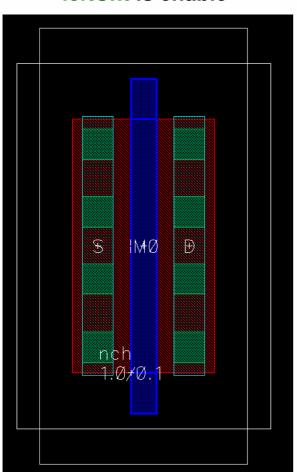
Parameters can be modify



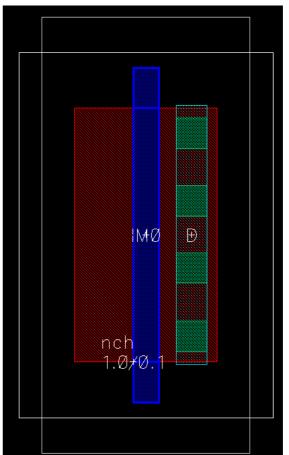
The function of leftCnt, RightCnt

■ The function provide a option for drawing poly-left (right) diffusion area metal1 connect

leftCnt is enable



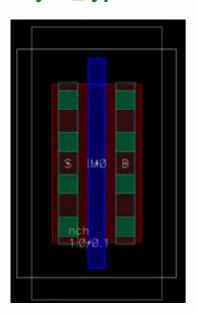
leftCnt is Disable





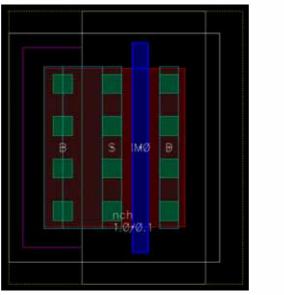
- The function of bodytie_typeL and bodytie_typeR
 - The function provide a option for drawing body connection at the device left (bodytie_typeL) or device right (bodytie_typeR).

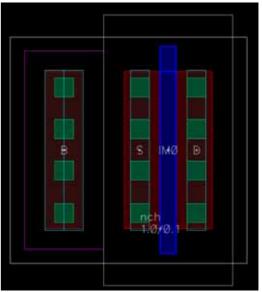
bodytie_typeL is *None*



bodytie_typeL is Integred





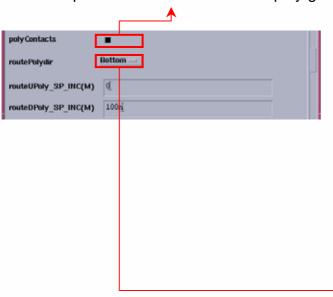


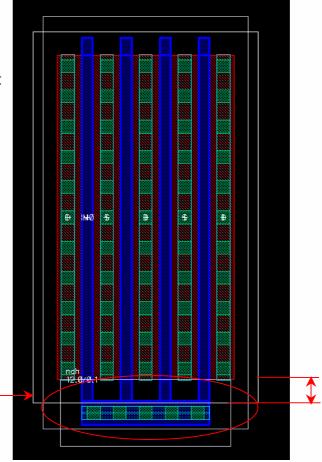


The function of routePolydir

The function is provided to drawing poly gate connection. The space of poly gate connection to the diffusion area can be modify by routeUPoly_SP_INC(M) and routeDPoly_SP_INC(M) ².

The **poly Contacts** will appear when **routPolydir** doesn't None. It is an option to draw contact on the poly gate.





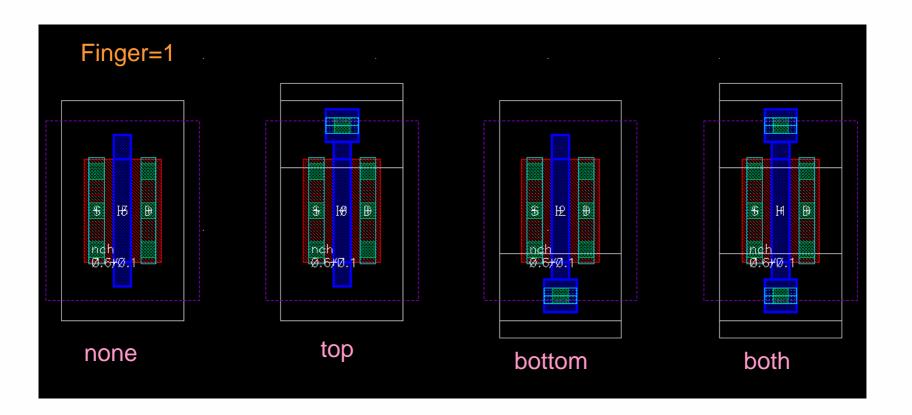
PO.S.6(design rule) + routeDPoly_SP_INC

² The routeUPoly_SP_INC(M) and routeDPoly_SP_INC(M) only appear when routePolydir doesn't *None*.

TSMC018 PDK Usage Guide The function of routePolydir



- - The function is suggest to use in multi-finger. If customer use only one finger and turn on the routePolydir none/top/bottom/both direction. It will shows the following layout.

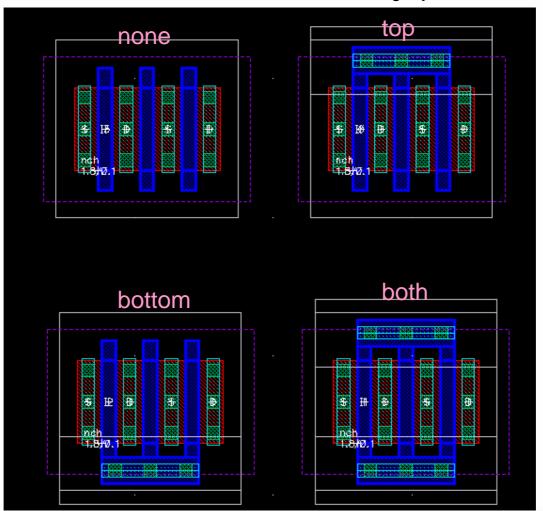


TSMC018 PDK Usage Guide The function of routePolydir

Confidential Security C

- - Finger number=3. If customer use finger number=3 and turn on the routePolydir none/top/bottom/both direction. It will shows the following layout.

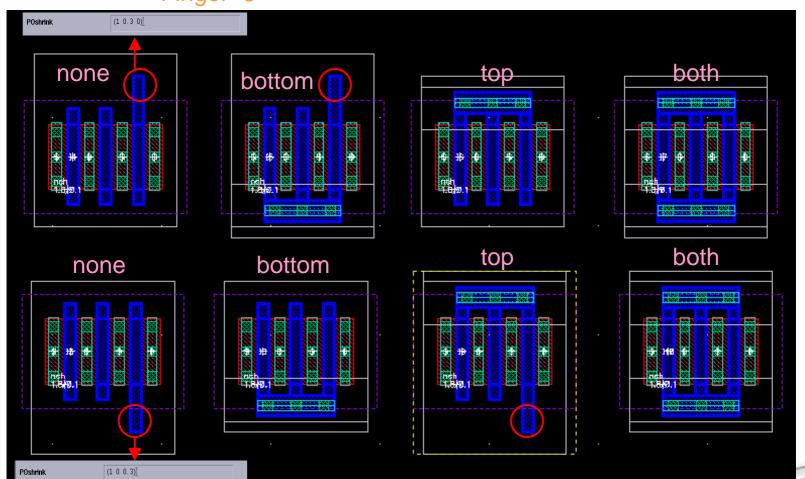
Finger=3



TSMC018 PDK Usage Guide The function of routePolydir



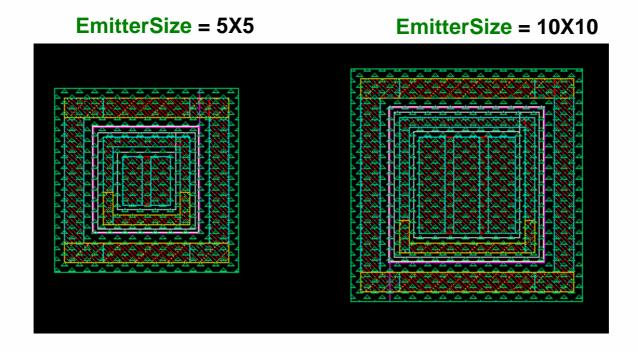
Finger number=3. Customer use finger number=3 and turn on the routePolydir none/top/bottom/both direction. At the same time customer uses Poshrink option as following: Finger=3





The function of EmitterSize

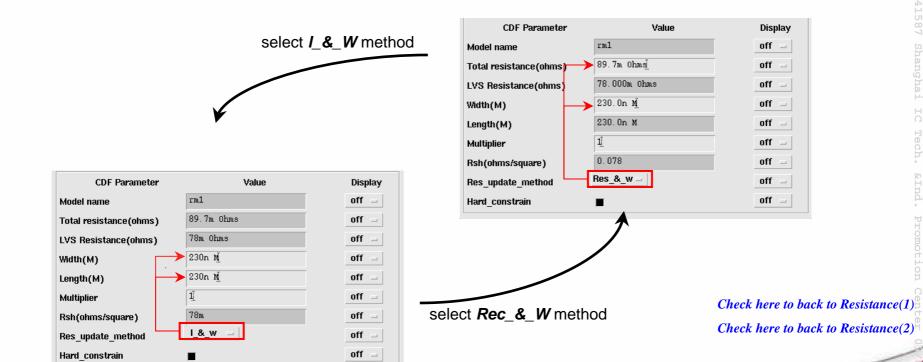
■ There are three dimension of pnp and npn are provided in this PDK, user can use this function to choose those device layout.



Check here to back to BJT

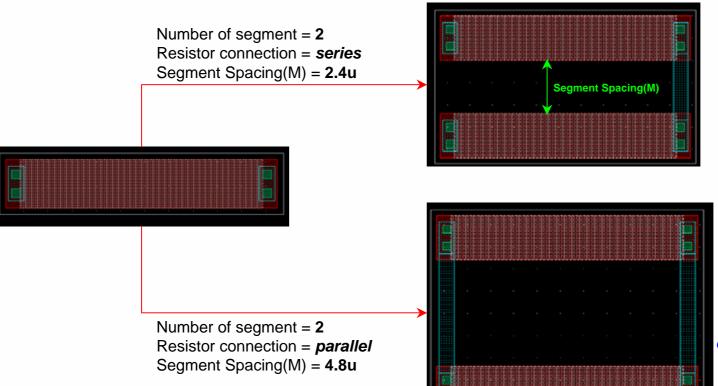


- The function of Total resistance(ohms), Width(M), Length(M) and Res_update_method
 - In the resistance cell, we provide user two kinds of input method *I_&_W* and *Rec_&_W* to modify the device resistance. When the user select *I_&_W* method, the input parameter will be length(M) and width(M), the other one is total resistance(ohms) and width(M).





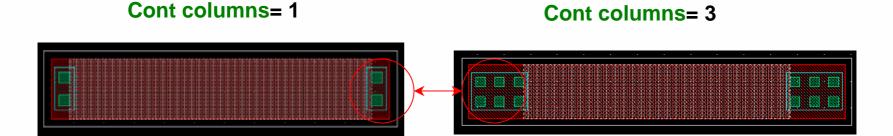
- The function of Resistor connection, Number of segment, Segment spacing(M)
 - Number of segment provide user a function to Increment the number of segment resistance, user can use Resistor connection and Segment spacing(M) to modify connection type **series** or **parallel** and segment spacing.



Check here to back to Resistance(2)



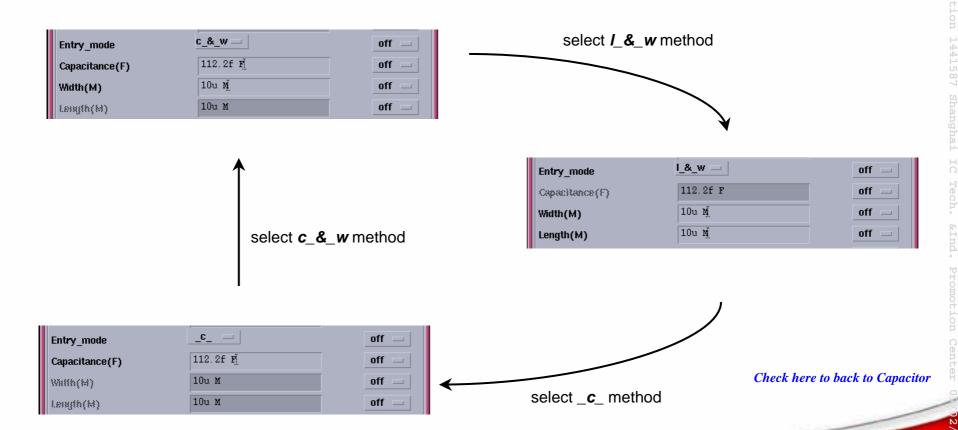
- The function of Cont columns
 - This function provide user to modify the contact columns.



Check here to back to Resistance(2)



- The function of Entry_method, Length_(M) and Width_(M).
 - In the capacitor cell, we provide user three kinds of input method *I_&_W*, _*c*_ and *c_&_W* to modify the device capacitance.

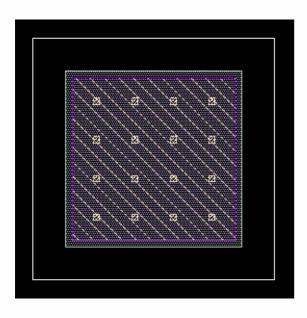


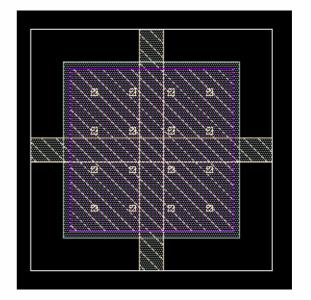


- The function of Create_Leading_terminals.
 - In the capacitor cell, we provide user a option to create leading terminals.

Create_Leading_terminals= Disable

Create_Leading_terminals= Enable

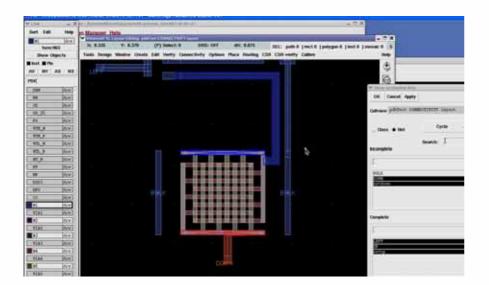




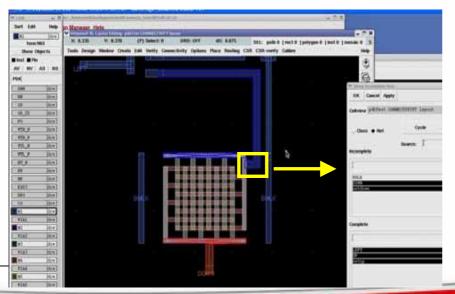
Check here to back to Capacitor



The function of CRTMOM



- No problem to add different metal layer connection flexibility.
- 2. Allow right&left side for connection but need to consider improper metal routing caused additional parasitic capacitances.

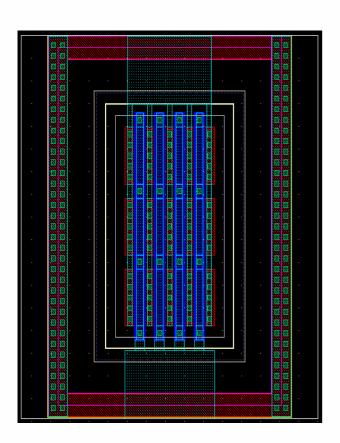


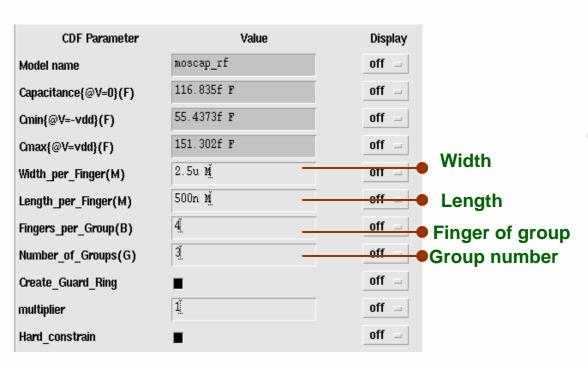
Extra Parasitic devices will be extracted in yellow mark region. Need to consider very careful.

TSMC don't recommend this kind connection.



- The function of PMOSCAP_RF
 - This function provide user to modify the device layout





Check here to back to Varactor

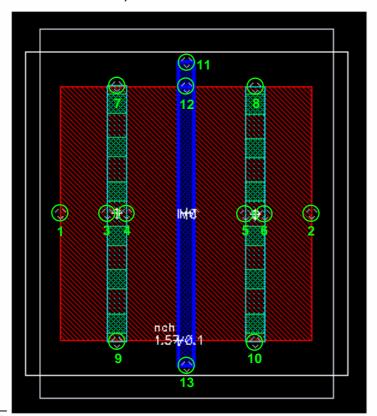


Appendix



Appendix A – Stretch Handles

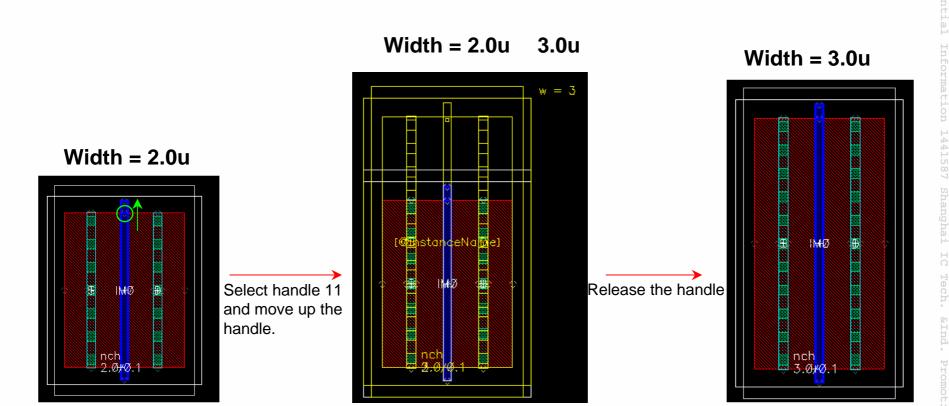
- This function lets user graphically change the value of those parameter for Pcell instances after user place them. The only one device MOS is a stretchable Pcell in this PDK.
- The system default is not show out the stretch handles, user must be enable the function manually. (Direct: in the layout view Options Display option Stretch Handles)



Stretch Handles number	Stretch direction
1	
2	
3, 5	
4, 6	
7, 8	
9, 10	
11	
13	
12	



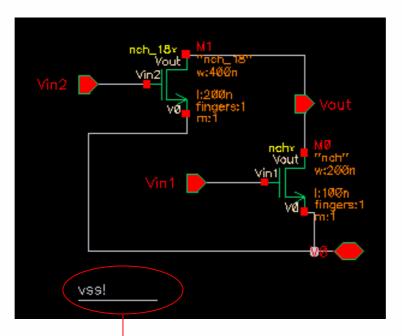
■ A example to show out the stretch case when the user stretch the handle 12.





Appendix B – The three terminal MOS substrate pin

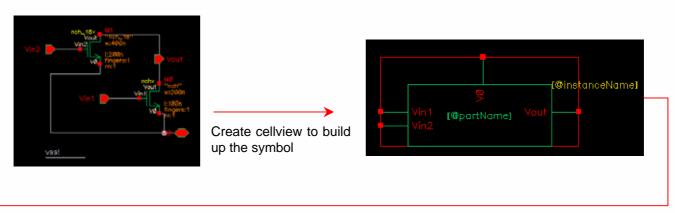
■ In three terminal MOS, we create a parameter for substrate pin. The pin name is vss_sub in NMOS and vdd_sub in PMOS. When user instances the three terminal MOS, all of the devices substrate terminal will connect to vss_sub or vdd_sub. User doesn't need to draw the wire to link the device. In the hierarchy structure, user can add a parameter in CDF form to assign the substrate terminal name.



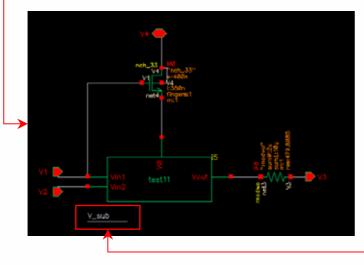
When user instances the nchx and nch_18x (three terminal MOS), all of the devices substrate terminal will connect to vss_sub (VSS!)

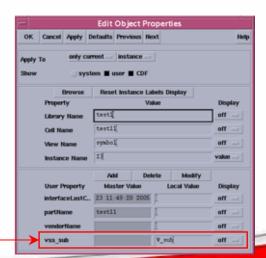


■ In the hierarchy structure, user can add a parameter in CDF form to assign the substrate terminal name.



Instance the symbol to other schematic view and assign the vss_sub to V_sub





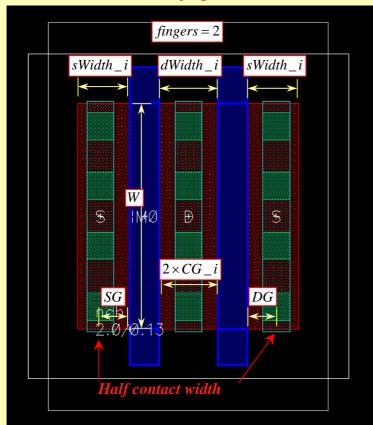


Appendix C – AS AD PS PD NRS NRD methodology

■ In this section, we will description that the PDK how to calculate as, ad, ps, pd, nrs and nrd.

Case I

• Normal MOS with multi fingers



$$S_{Area_total} = \sum_{i=1}^{s} sWidth_i \times w \qquad AS = S_{Area_total} / fingers$$

$$S_{Peri_total} = \sum_{i=1}^{s} (sWidth_i + w \times N_s) \times 2 \quad PS = S_{Peri_total} / fingers$$

$$D_{Area_total} = \sum_{i=1}^{s} dWidth_i \times w \qquad AD = D_{Area_total} / fingers$$

$$D_{Peri_total} = \sum_{i=1}^{s} (dWidth_i + w \times N_d) \times 2 \quad PD = D_{Peri_total} / fingers$$

$$N_s : \text{Number of Source} \qquad N_d : \text{Number of Drain}$$

$$NRS = (\sum_{i=1}^{s} CG_i_s + SG_s + DG_s) / fingers / w$$

$$NRD = (\sum_{i=1}^{s} CG_i_d + SG_d + DG_d) / fingers / w$$

CG_i_d: *CG_i* in Drain diffusion area

CG i $s: CG_i$ in Source diffusion area

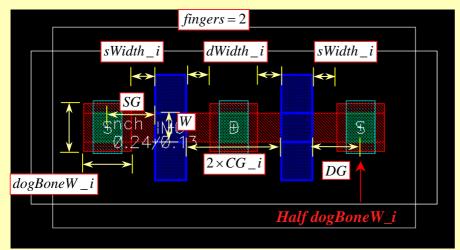
 $SG_d(SG_s): SG$ in Drain(Source) diffusion area

 $DG_d(DG_s)$: DG in Drain(Source) diffusion area



Case II

• Dog Bone MOS with multi fingers



$$S_{Area_total} = \sum_{i=1} sWidth_i \times w + dogBoneW_i \times dogBoneW_i \times N_s$$

$$D_{Area_total} = \sum_{i=1} dWidth_i \times w + dogBoneW_i \times dogBoneW_i \times N_d$$

$$S_{Peri_total} = \sum_{i=1} sWidth_i \times 2 + dogBoneW_i \times 4 \times N_s$$

$$D_{Peri_total} = \sum_{i=1}^{n} dWidth_i \times 2 + dogBoneW_i \times 4 \times N_d$$

 N_s : Number of Source N_d : Number of Drain

$$AS = S_{Area total} / fingers$$

$$PS = S_{Peri\ total} / fingers$$

$$AD = D_{Area_total} / fingers$$

$$PD = D_{Peri\ total} / fingers$$

$$NRS = (\sum_{i=1}^{n} CG_i s + SG_s + DG_s) / fingers / w$$

$$NRD = (\sum_{i=1} CG_i - d + SG_d + DG_d) / fingers / w$$

$$CG_i_d: CG_i$$
 in Drain diffusion area

$$CG_i_s: CG_i$$
 in Source diffusion area

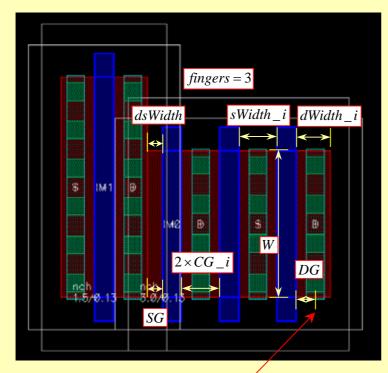
$$SG_d(SG_s) : SG$$
 in Drain(Source) diffusion area

$$DG_d(DG_s)$$
: DG in Drain(Source) diffusion area



Case III

• Normal MOS with multi fingers after abut



Half contact width

$$S_{Area_total} = (\sum_{i=1} sWidth_i + dsWidth) \times w$$

$$S_{Peri_total} = (\sum_{i=1} sWidth_i + dsWidth + w \times N_s) \times 2$$

$$D_{Area_total} = (\sum_{i=1}^{n} dWidth_i + ddWidth) \times w$$

$$D_{Peri_total} = (\sum_{i=1}^{n} dWidth_i + ddWidth + w \times N_d) \times 2$$

$$N_s$$
: Number of Source N_d : Number of Drain

$$AS = S_{Area\ total} / fingers$$
 $PS = S_{Peri\ total} / fingers$

$$AD = D_{Area_total} / fingers$$
 $PD = D_{Peri_total} / fingers$

$$NRS = (\sum_{i=1}^{n} CG_i s + SG_s + DG_s) / fingers / w$$

$$NRD = (\sum_{i=1} CG_i d + SG_d + DG_d) / fingers / w$$

$$CG_i - d : CG_i$$
 in Drain diffusion area

$$CG$$
 i $s: CG_i$ in Source diffusion area

$$SG_d(SG_s): SG$$
 in Drain(Source) diffusion area

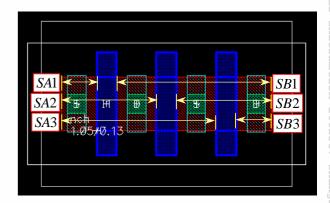
$$DG _d(DG _s) : DG$$
 in Drain(Source) diffusion area



■ Appendix D – SA SB SD methodology

- In this section, we will description that the PDK how to calculate sa and sb.
- For post-layout simulation (netlists extracted from the layout): Treat each finger of devices as an independent MOS. And thus PDK assigns different SA/SB to each independent MOS. So the netlist will look like (if finger_number=3):

m1 d g s b w=channel width I =channel length SA=SA1 SB=SB1 m2 d g s b w=channel width I =channel length SA=SA2 SB=SB2 m3 d g s b w=channel width I =channel length SA=SA3 SB=SB3



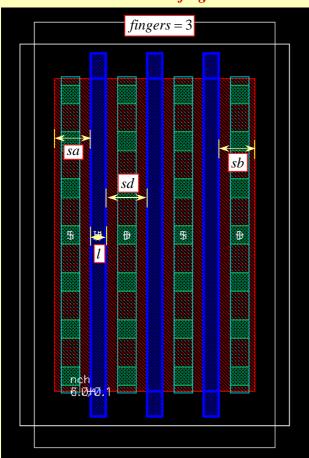
For pre-layout simultation (netlists estimated from schematic diagram): PDK sets m=finger_number, SA=SA, SB=SB and SD=SD. So the netlist will look like m0 d g s b w=channel width I =channel length m=1 SA=SA SB=SB SD=SD Please refer next two page to understand the SA, SB and SD in layout



■ In this page, we will description that the PDK how to calculate SA, SB and SD.

Case I

• Normal MOS with multi fingers



SA = sa: In the netlist, SA equal to sa

SB = sb: In the netlist, SB equal to sb

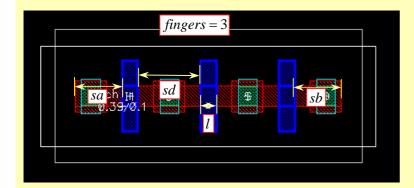
SB = sd: In the netlist, SB equal to sd



■ In this page, we will description that the PDK how to calculate SA, SB and SD.

Case II

• Dog Bone MOS with multi fingers



SA = sa: In the netlist, SA equal to sa

SB = sb: In the netlist, SB equal to sb

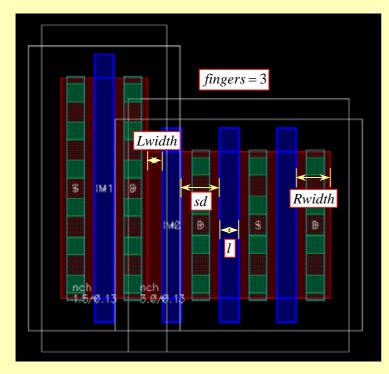
SB = sd: In the netlist, SB equal to sd



■ In this page, we will description that the PDK how to calculate SAeff and SBeff.

Case III

• Normal MOS with multi fingers after abut



$$Sum1_i = 1/(Lwidth + i \times (sd + l) + 0.5 \times l)$$

$$SAeff = fingers / \sum_{i=0}^{fingers-1} Sum1_i - 0.5 \times l$$

$$Sum2_i = 1/(Rwidth + i \times (sd + l) + 0.5 \times l)$$

$$SBeff = fingers / \sum_{i=0}^{fingers-1} Sum 2_i - 0.5 \times l$$

$$SAeff = SAeff$$

$$SBeff = SBeff$$

SA = SAeff: In the netlist, SA equal to SAeff

SB = SBeff: In the netlist, SB equal to SBeff

SA = sa: In the netlist, SA equal to sa

SB = sb: In the netlist, SB equal to sb

SB = sd: In the netlist, SB equal to sd