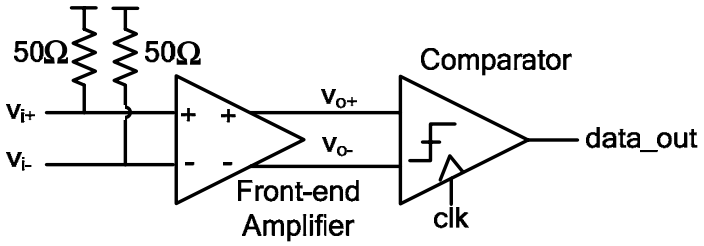
UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

E. Alon **Project Part I** **EECS 240**
Due Thursday, Apr. 15, 2010

For this phase of the project, you should use the EECS240 90nm CMOS process with the typical (tt) device parameters.

In this first phase of the project, we will be exploring the design of a front-end amplifier suitable for a high-speed, low-swing serial link. Below is a conceptual schematic showing how this amplifier is used.



Unlike previous homeworks, you will not be provided with many specifications on the amplifier itself. Rather, you will need to use higher-level specs (e.g., data-rate and required BER) in order to guide the design of your amplifier. As always, your goal will be to meet the required performance at minimum power consumption.

The specifications and constraints for your design are:

- Data-rate: 3 Gb/s
- BER: $< 10^{-12}$
- Input swing amplitude: 5 mV differential
- Comparator C_{in}: 30 fF (i.e., the comparator loads both v_{o+} and v_{o-} with 30fF of capacitance)
- Comparator offset: 20 mV

Some additional notes and guidelines:

- You can use ideal current sources in the bias circuitry for your amplifier, but any current source loads must be implemented with real transistors.
- You are allowed to use ideal resistors, but any capacitors in your circuit must be implemented out of MOS devices or MOM structures. For MOM capacitors, you can use the parameters of either vertical or horizontal parallel plates from HW#1.
- If your design requires common-mode feedback, for this phase of the project you can use an ideal amplifier to implement this feedback. You should however include the common-mode sensing network (and be sure to include any of its possible loading effects).
- You are free to set the common-mode at the input of your amplifier to any level you'd like.
- Don't forget to include the thermal noise of the input termination resistors. This will most likely require you to create the input voltages (i.e. v_{i+}, v_{i-}) to the amplifier using current sources.
- You also shouldn't forget to include the source and drain perimeters and areas for each of your devices.

Your final submission should include:

1. A clearly labeled schematic of your design including device sizes and nominal bias currents.

2. A concise, clear description of the procedure you followed to design the amplifier. How did you set the required gain, output noise, bandwidth, etc.?
3. Simulations plots and printouts verifying that your amplifier meets the gain, noise, and bandwidth specifications you calculated in 2.
4. A text or Excel file listing the simulated voltage outputs of your amplifier vs. time for the input waveforms provided in eye_input.sp (which is posted on the project section of the course web-site). Note that you do not need to print this out – just submit it electronically by email.
5. The HSPICE netlist of your amplifier.