ERC usage

LVS/RC section

Version 1.2

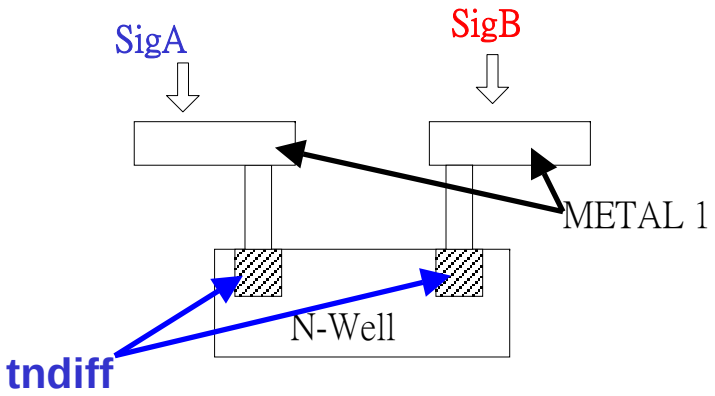
June 07, 2007

What is ERC (Electrical Rule Checking)

- ERC is a special option for designers. Some errors can be waived, but others may be deadly errors. So, designers must review every error or warning for LVS/ERC report.
- Some ERC rules are included in TSMC standard LVS command files.
  - Soft connect checking
  - Path checking
  - ptap/ntap checking
  - MOS s/d power&ground checking
  - Gate directly connects to power or ground.
  - Floating gate
  - Floating well

Soft connect and soft check

- N-well and P-well are high resistor material, so



1. Treat as Short
Sig A connect to Sig B
--> If Sig A is a power line and Sig B connect to a IP power.
--> The IP get a high resistor power, it means IR drop is very serious.
----> **ERROR**

2. Treat as open
Sig A does not connect to Sig B
--> If Sig A is a power signal and sig B is ground signal
--> power and ground short
--->**ERROR**

There are two methods to solve this problem

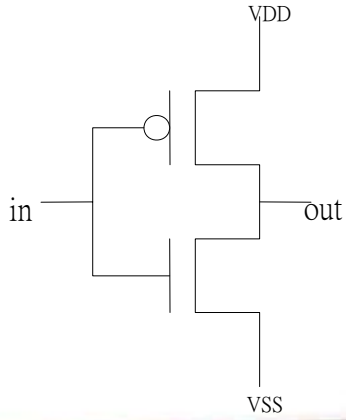
1. **Run two LVS command file, one is " treat as short", the other is "treat as open".**
2. **Use soft connect and soft check!!!**

What is soft connect and soft checking ?

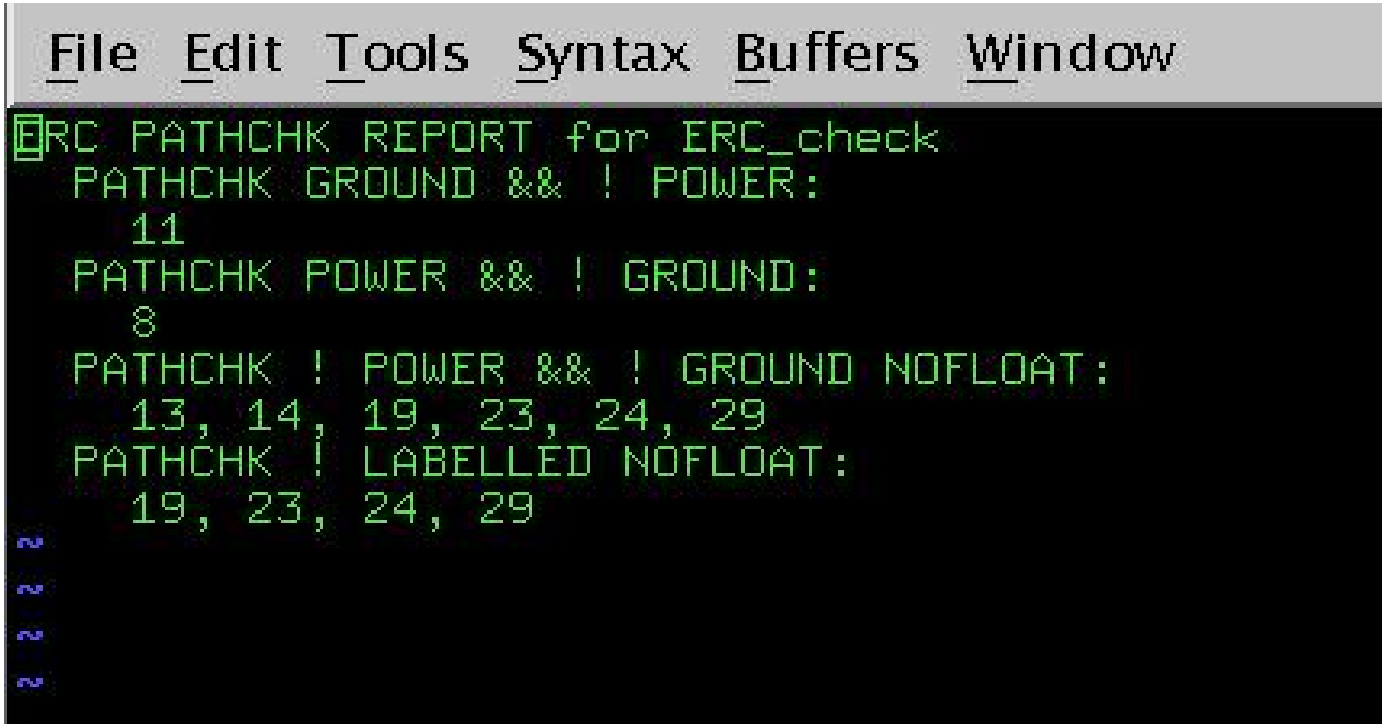
- *Sconnect definition*: **Passes established connectivity from the upper layer polygons onto the specified lower layer polygons (one-directional) < calibre manu.>**
- *Softchk* **: Help to search which contact connect to WELL.**
- **TSMC LVS/ERC command file contain those option, and those errors/warnings are report in lvs.rep or lvs.rep.ext .**
- **Please confirm every error or warning of those three file ~.rep ~.rep.ext svdb/~.rep .**
- **Give user a warning on the lvs.rep.ext file. User can debug this error by “calibre -rve” and open the svdb/~.softchk file .**

Path Checking

- 4 kinds of path checking
  - 1.Nodes with a path to power but not ground
  - 2.Nodes with a path to ground but not power
  - 3.Nodes without a path to both path and groundout
  - 4.Nodes without a path to pin
- Purpose
  - Help designer to check if the circuit miss something.



Pathchk Report (svdb/~.Rep)

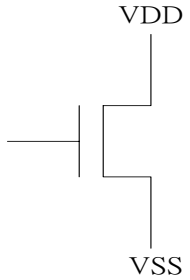


ERC Report

- Get ERC report in LVS stage.
- Calibre : %calibre –lvs –spi layout.net lvs_command_file
  - Calibre please check the “calibre_erc.db” and “calibre_erc.sum” files.
- Hercules : %hercules lvs_command_file
  - Hercules please check the “Top.LAYOUT_ERRORS” file.
- Assura : %assura LVS.rsf
  - Assura please check the “Top.err” file.

PTAP/NTAP and Special MOS Connectivity Checking

- **PTAP connect to power/ NTAP connect to ground**
  - Check ERC errors “PPVDD49” for PTAP
  - Check ERC errors “NPVSS49” for NTAP
- **N/P MOS source/drain one connect to POWER the other connect to GROUND**
  - Check ERC errors “mppg” for PMOS.
  - Check ERC errors “mnpg” for NMOS.



- **Calibre please check the “calibre_erc.db” and “calibre_erc.sum” files.**
- **Hercules please check the “Top.LAYOUT_ERRORS” file.**
- **Assura please check the “Top.err” file.**

Gate directly connects to power or ground

- PMOS gate directly connects to power without the 2.5v and 3.3v IO devices.
  - For ESD protection, if core or 1.8v PMOS gate directly connect power node, gate will be damaged.
  - Check ERC errors “ppvdd150” for PMOS gate.
- NMOS gate directly connects to ground without the 2.5v and 3.3v IO devices.
  - For ESD protection, if core or 1.8v NMOS gate directly connects ground node, gate will be damaged.
  - Check ERC errors “npvss150” for NMOS gate.
- Calibre please check the “calibre_erc.db” and “calibre_erc.sum” files.
- Hercules please check the “Top.LAYOUT_ERRORS” file.
- Assura please check the “Top.err” file.

Floating gate

- There is no any Contact interact with the poly gate.
  - Check ERC errors “floating” for all gate.

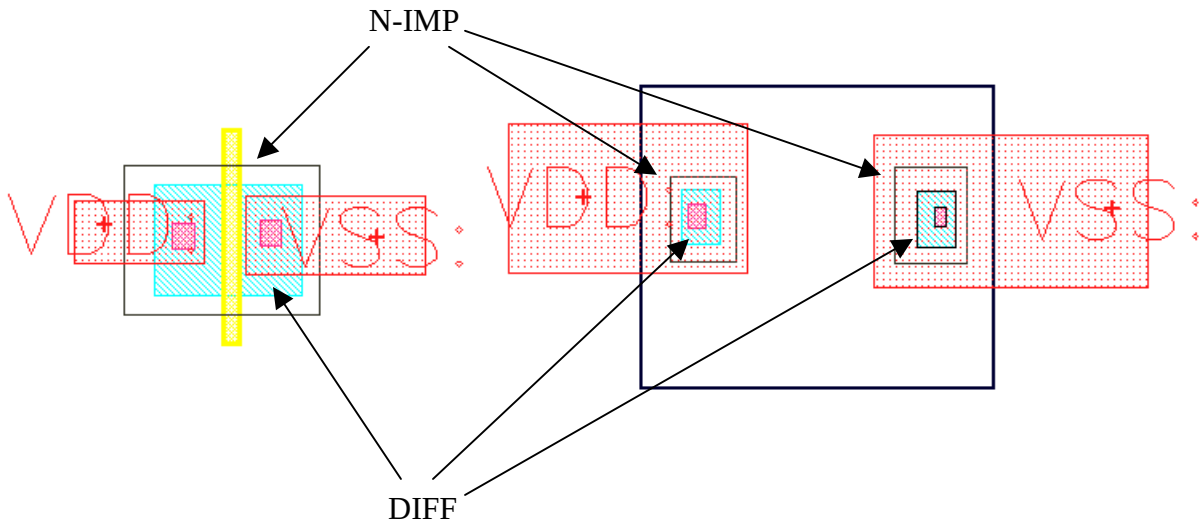
- Calibre please check the “calibre_erc.db” and “calibre_erc.sum” files.
- Hercules please check the “Top.LAYOUT_ERRORS” file.
- Assura please check the “Top.err” file.

Floating well

- There is no any power or ground connect to NWEL or PSUB.
  - Check ERC errors “floating.nxwell” for NWEL.
  - Check ERC errors “floating.psub” for PSUB.

- Calibre please check the “calibre_erc.db” and “calibre_erc.sum” files.
- Hercules please check the “Top.LAYOUT_ERRORS” file.
- Assura please check the “Top.err” file.

A Layout Example



~.sum

```
---------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK mppg .... TOTAL Result Count = 1
RULECHECK mnpg .... TOTAL Result Count = 0
RULECHECK ppvdd49 ... TOTAL Result Count = 0
RULECHECK npvss49 ... TOTAL Result Count = 1
---------------------------------------------------------------------------
```

~.ext

WARNING: Stamping conflict in SCONNECT - Multiple source nets stamp one target net.
Use LVS REPORT OPTION S or LVS SOFTCHK statement to obtain detailed information.

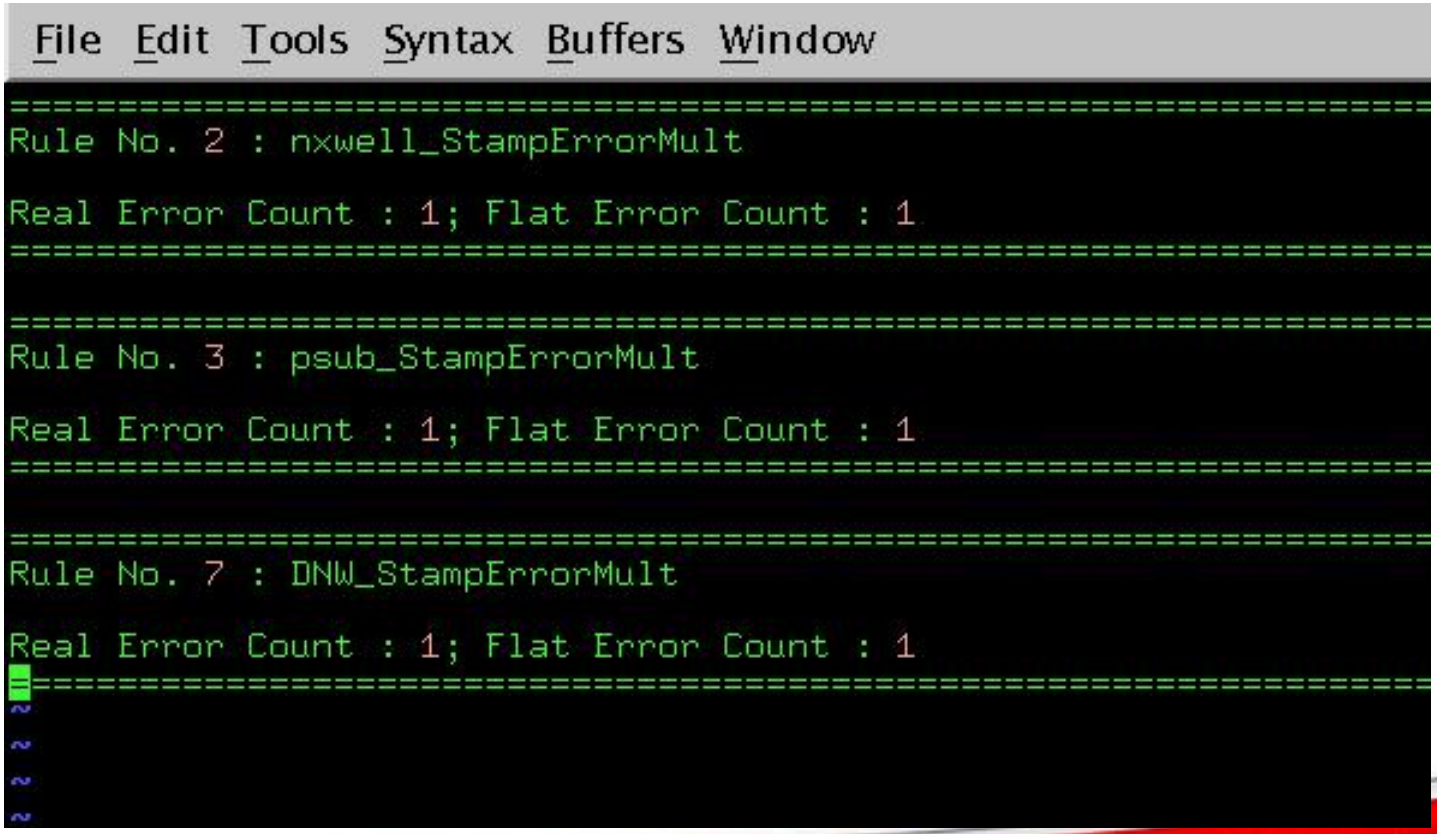
Hercules ERC Check Error File

- **Please check the Top.LAYOUT_ERRORS file.**

```
File  Edit  Tools  Syntax  Buffers  Window
Structure name:  ERC_check

                        ERROR SUMMARY

No Comment
 ERR_TEXT_SHORT_DISCARD ................................ 2 violations found.

No Comment
 C_THRU nplug INSIDE nxwell { } (1;0) ................... 2 violations found.

No Comment
 C_THRU pplug INSIDE psub_term { } (1;1) ................ 2 violations found.

No Comment
 C_THRU pplug INSIDE psub { } (1;2) ..................... 2 violations found.

No Comment
 C_THRU n_pplug INSIDE n_psub { } (1;4) ................. 2 violations found.

No Comment
 C_THRU dnwc INSIDE DNW { } (1;6) ....................... 2 violations found.

No Comment
 ERR_TEXT_SHORT_DISCARD ................................ 2 violations found.

No Comment
 ERR_TEXT_SHORT_DISCARD ................................ 2 violations found.

No Comment
 NET_PATH_CHECK { } PERM=path1_Out(1;13) ............... 13 violations found.

No Comment
 NET_PATH_CHECK { } PERM=path3_Out(1;15) ............... 16 violations found.

No Comment
 NET_PATH_CHECK { } PERM=path4_Out(1;16) ............... 16 violations found.
```

Assura ERC Check Error File

- Please check the Top.err file.
- Currently the Assura can not support the net-path check function.



Summary for ERC checker

- Please confirm every error or warning of these three files --- “~.rep” “~.rep.ext” “svdb/~.rep” for Calibre.
- Please confirm the Top.LAYOUT_ERRORS file for Hercules.
- Please confirm the Top.err file for Assura.
- Every soft connect error must be fixed.
- Other ERC errors/warnings need to be reviewed by circuit designer.