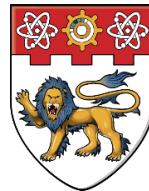




Technische Universität München



**NANYANG
TECHNOLOGICAL
UNIVERSITY**

NM6007

Analog IC Laboratory Course

Individual Assignment Class-AB Audio Amplifier with Translinear Loop

Report By:
Bian Wenxuan

2023/24 NTU-TUM MSC
Integrated Circuit Design
Matriculation No: G2303988L

Table of Contents:

1. Amplifier Design Background.....	9
1.1. Audio Amplifier Application Scenarios	9
1.2. Audio Amplifier System Architecture.....	9
1.3. Class-AB Audio Amplifier Design Requirements.....	13
2. Amplifier Circuit Analysis	14
2.1. Operational Amplifier Topology Selection.....	14
2.2. Key Parameter Analysis	15
2.2.1. Total Harmonic Distortion	15
2.2.2. Power Supply Rejection Ratio.....	17
2.2.3. Output Swing	18
2.3. Bias Circuit Structure Analysis	19
2.3.1. Star-up Circuit.....	19
2.3.2. Dobkin Current Source.....	20
2.3.3. Self-biased Wide-swing Cascode Current Mirror.....	23
2.4. Amplifier Circuit Structure Analysis.....	28
2.4.1. Input Stage.....	29
2.4.2. Gain Stage and Compensation.....	30
2.4.3. Output Stage	36
3. Design Process.....	38
3.1. MOSFET Characterizations	39
3.1.1. K'	39
3.1.2. V_{TH}.....	40
3.1.3. γ	41
3.1.4. λ	42
3.1.5. r_o & R_{ON}	43
3.2. Distribution of Current and V_{overdrive}.....	45
3.3. Adjustment of the Dimensions of Special MOS Transistors.....	46
3.3.1. Dobkin Current Source	46
3.3.2. Output Transistors.....	47

3.3.3. Translinear Loop.....	48
3.3.4. Input transistors of the First and Second Stages.....	49
3.3.5. Aspect Ratio of All the Transistors with Capacitor and Resistor Size.....	50
4. Pre-simulation.....	53
 4.1. Transistors Region and Power Consumption.....	54
 4.2. Closed-Loop Gain and Closed Loop Unity Gain Bandwidth.....	54
 4.3. Common-mode Gain.....	56
 4.4. Feed-back Loop Gain and Phase Margin.....	56
 4.5. Power Supply Rejection Ratio	57
 4.6. Output Swing.....	58
 4.7. Total Harmonic Distortion	58
 4.8. Settling Time	59
 4.9. Slew Rate.....	60
 4.10. First Stage Gain.....	61
 4.11. Equivalent Input Noise	62
 4.12. Complete PVT Corner Simulation Results.....	63
5. Layout Design	64
 5.1. First Version.....	64
 5.1.1. Full Layout Overview of First Version	64
 5.1.2. Bias in First Layout Version.....	65
 5.1.3. Amp in First Layout Version.....	66
 5.2. Second Version	67
 5.2.1. Full Layout Overview of Second Version	67
 5.2.2. Bias in Second Layout Version.....	68
 5.2.3. Amp in Second Layout Version.....	68
 5.2.4. Input Pair in Second Layout Version	69
 5.2.5. Other Parts in Second Layout Version	70
 5.2.6. Output Transistors in Second Layout Version	70
6. Post-simulation	71
 6.1. Power Consumption	72
 6.2. Closed-Loop Gain and Closed Loop Unity Gain Bandwidth.....	72

NM6007 Assignment: Class-AB Audio Amplifier

6.3. Common-mode Gain.....	73
6.4. Feed-back Loop Gain and Phase Margin.....	73
6.5. Power Supply Rejection Ratio	75
6.6. Output Swing.....	76
6.7. Total Harmonic Distortion	76
6.8. Settling Time	77
6.9. Slew Rate.....	79
6.10. Complete PVT Corner Simulation Results.....	80
7. Don't-s and Do-s.....	81
7.1. Don't-s.....	81
7.2. Do-s	81

List of Figures:

Figure 1 Audio System	9
Figure 2 Non-inverting Configuration	10
Figure 3 Inverting Configuration	10
Figure 4 System Diagrams of the Two Configurations	11
Figure 5 Ideal Frequency Response	12
Figure 6 Complete Operational Amplifier System Structure	13
Figure 7 Amplifier Circuit	15
Figure 8 Stabilizing Effect of the M30's V_{GS} on the Folding Point Voltage	17
Figure 9 All Transistors that may Affect the PSRR	18
Figure 10 Bias Circuit.....	19
Figure 11 Start-up Circuit	20
Figure 12 Remove Start-up with a Resistor	20
Figure 13 Simulation Curve of the Current Generated by Dobkin as V_{DD} Varies	22
Figure 14 Input Pair Gm Variation with PVT Changes.....	22
Figure 15 Self-biased Wide-swing Cascode Current Mirror	23
Figure 16 Conventional Cascode Current Mirror	24
Figure 17 Wide Swing Structure.....	24
Figure 18 Self-biasing Cascode Current Mirror	25
Figure 19 Two Types of Feedback Mechanisms	26
Figure 20 Loop Stability Mechanism	27
Figure 21 DC with Regulation Transistor and C0	27
Figure 22 DC when Removing Regulation.....	28
Figure 23 Amp Structure	28
Figure 24 Input Stage.....	29
Figure 25 Gain Stage	30
Figure 26 A Simple Feedback System.....	31
Figure 27 Peaking and Ringing.....	33
Figure 28 Miller Effect	33
Figure 29 AC Ground	35
Figure 30 Miller and Ahuja.....	35
Figure 31 Current Replication in the Translinear Loop	36
Figure 32 Output Stage with Translinear Loop	37
Figure 33 Loop Frequency Response of Pre-simulation with and without Load Capacitance	38
Figure 34 MOSFET Characterizations Testbench	39
Figure 35 Transfer Characteristic Curve and K' Calculation	40
Figure 36 V_{TH} Measurement	41
Figure 37 γ Measurement.....	41
Figure 38 Output Characteristic Curve	43
Figure 39 r_o & R_{ON}	44

NM6007 Assignment: Class-AB Audio Amplifier

Figure 40 DC Simulation Result.....	45
Figure 41 Distribution of Bias Current	45
Figure 42 Distribution of Amp Current	46
Figure 43 NMOS Translinear Loop	48
Figure 44 Transistor Sizing of Bias	50
Figure 45 Transistor Sizing of Amp	52
Figure 46 Transistors Region and DC Current in Pre-simulation.....	54
Figure 47 Common Testbench.....	54
Figure 48 Closed-Loop Gain and Closed Loop Unity Gain Bandwidth in Pre-simulation.....	55
Figure 49 Common-mode Gain in Pre-simulation.....	56
Figure 50 Feed-back Loop Stb Testbench with C_L	56
Figure 51 Feed-back Loop Stb Testbench without C_L	56
Figure 52 Feed-back Loop Gain and Phase Margin with or without C_L in Pre-simulation.....	57
Figure 53 Power Supply Rejection Ratio in Pre-simulation.....	57
Figure 54 Output Swing in Pre-simulation	58
Figure 55 THD 1k in Pre-simulation	58
Figure 56 THD 10k in Pre-simulation	59
Figure 57 Settling Time for Charging in Pre-simulation	59
Figure 58 Settling Time for Discharging in Pre-simulation	60
Figure 59 Slew Rate for Charging in Pre-simulation.....	60
Figure 60 Slew Rate for Discharging in Pre-simulation	61
Figure 61 First Stage Gain in Pre-simulation	61
Figure 62 Noise Testbench	62
Figure 63 Equivalent Input Noise in Pre-simulation	62
Figure 64 Complete PVT Corner Simulation Results in Pre-simulation.....	63
Figure 65 Swing for Temperature Variation in Pre-simulation	64
Figure 66 First Layout Version.....	64
Figure 67 Bias in First Layout Version.....	65
Figure 68 Amp in First Layout Version.....	66
Figure 69 Input Pair in First Layout Version.....	66
Figure 70 Second Layout Version	67
Figure 71 Bias in Second Layout Version	68
Figure 72 Amp in Second Layout Version	68
Figure 73 Common Centroid Symmetry Interdigititation Input Pair Reference.....	69
Figure 74 Input Pair in Second Layout Version	69
Figure 75 Other Parts in Second Layout Version	70
Figure 76 Output Transistors in Second Layout Version	70
Figure 77 Output Transistors Structure in Second Layout Version.....	71
Figure 78 DC Current in Post-simulation	72

NM6007 Assignment: Class-AB Audio Amplifier

Figure 79 Closed-Loop Gain and Closed Loop Unity Gain Bandwidth in Post-simulation.....	72
Figure 80 Common-mode Gain in Post-simulation.....	73
Figure 81 FB Loop Gain Difference between Pre and Post with C_L	73
Figure 82 Feed-back Loop Gain and Phase Margin with or without C_L in Post-simulation.....	74
Figure 83 Feed-back Loop LC Testbench with C_L	74
Figure 84 Feed-back Loop LC Test Result in Post-simulation.....	75
Figure 85 Power Supply Rejection Ratio in Post-simulation	75
Figure 86 Output Swing in Post-simulation.....	76
Figure 87 THD 1k in Post-simulation.....	76
Figure 88 THD 10k in Post-simulation.....	77
Figure 89 Settling Time for Charging in Post-simulation	77
Figure 90 Settling Time for Discharging in Post-simulation.....	78
Figure 91 Unusual Response Occurring during the Discharging Process	78
Figure 92 Slew Rate for Charging in Post-simulation.....	79
Figure 93 Slew Rate for Discharging in Post-simulation	79
Figure 94 Complete PVT Corner Simulation Results in Post-simulation	80
Figure 95 Swing for Temperature Variation in Post-simulation	80

List of Tables:

Table 1. Specification Table (@ VDD = 1.6V and @ 60°C)	13
Table 2. K'	40
Table 3 Transistor Sizing of Bias.....	50
Table 4 Transistor Sizing of Amp.....	52

1. Amplifier Design Background

1.1. Audio Amplifier Application Scenarios

In an audio output system, the signal is initially read from a CD and processed by a digital audio system before being transferred to the analog output circuitry. This typically includes pre-processing circuits like filtering and de-emphasis, along with audio operational amplifiers. The op-amp amplifies the signal by a factor of 4 and enhances its current driving capability. In the subsequent stage, a Zobel network is often added to the power amplifier system to counteract the inductive load of the amplifier by introducing an RC series network, which ensures a constant resistive load. The amplified signal drives the speaker, which can be regarded as a coil consisting of an inductance in series with a small resistor, simplified to a 16Ω resistor. When energized, the coil produces a magnetic field that interacts with a magnet, driving mechanical components that push air to vibrate, thereby generating sound. The audio system is illustrated in the accompanying figure.

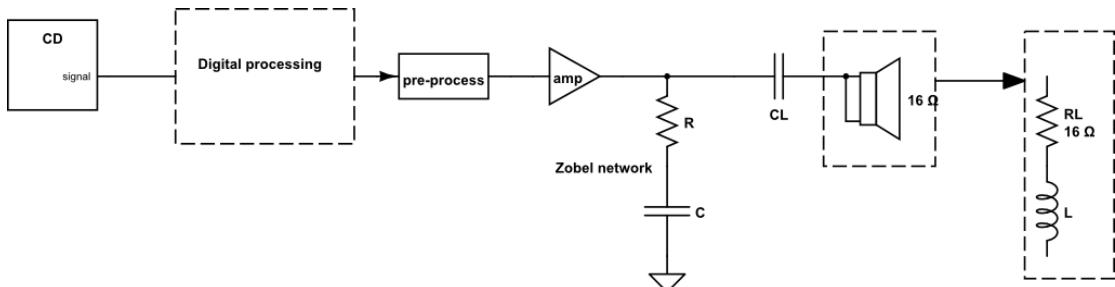


Figure 1 Audio System

1.2. Audio Amplifier System Architecture

In this system, the operational amplifier is a standalone IC chip, while other external components on the PCB are discrete components, which can be replaced with ideal components in simulations. The system architecture offers two configurations: inverting and non-inverting, both with a closed-loop AC gain of 4.

The non-inverting configuration configures the op-amp as a non-inverting proportional amplifier, as illustrated below.

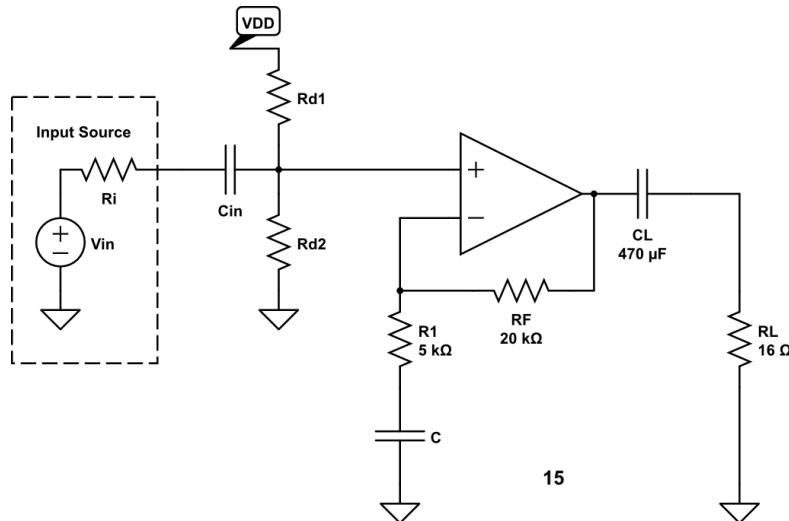


Figure 2 Non-inverting Configuration

This structure incorporates a capacitor to ground in the feedback loop, cutting off the DC current, thus the DC gain is 1, which does not amplify the offset. Additionally, the input voltage source's internal resistance does not affect the ratio calculation of the feedback resistors, significantly enhancing the accuracy of the closed-loop.

The inverting configuration sets the op-amp as an inverting proportional amplifier, as shown below.

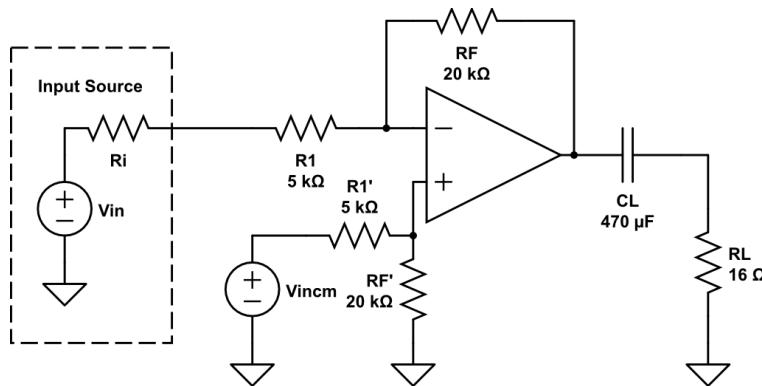


Figure 3 Inverting Configuration

Since the signal is input from the negative terminal of the operational amplifier, and the input and feedback paths are interconnected, the resistance value of R1 is in series with the internal resistance of the input voltage source, which adversely affects the precision of the op-amp's closed-loop gain. Before the signal enters the feedback loop, it first undergoes attenuation through R1. Because the gain-bandwidth product (GBW) is the product of $f(-3\text{dB})$ and A_v , and a reduction in A_v results in a decreased GBW, the bandwidth will be slightly smaller than that of a non-inverting configuration. However, as the system is primarily intended for low-frequency operations, the impact is minimal.

NM6007 Assignment: Class-AB Audio Amplifier

The system diagrams of the two configurations are distinctly different, as shown below. This design utilizes an inverting structure, with an R1/RF ratio of 1:4 and a closed-loop gain of 4.

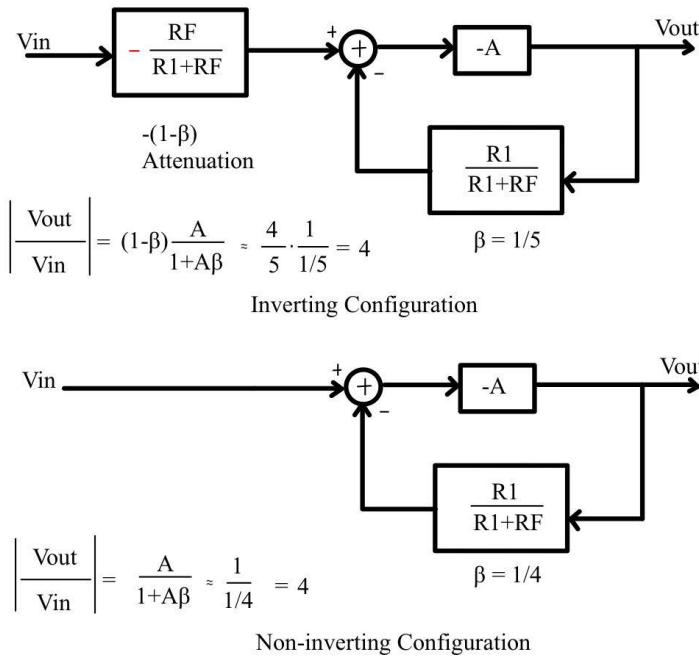


Figure 4 System Diagrams of the Two Configurations

This audio system processes signals at relatively low frequencies, primarily operating within the 20 - 44.1 kHz range. The human ear can hear frequencies from 20 to 20.05 kHz, and after sampling, the Nyquist frequency is twice the highest frequency, necessitating a bandpass from 20 to 44.1 kHz. To output low-frequency signals down to 20 Hz, a large capacitor is coupled at the output to allow low frequencies to pass while blocking the DC path, which can set the DC voltage at the top of the resistor to zero, centering the speaker's position to prevent initial displacement from limiting the dynamic range and causing distortion. The coupling capacitor is set at $470\mu F$, which can be implemented using discrete electrolytic capacitors. The system's maximum frequency is 44 kHz, which is significantly lower than the op-amp's gain-bandwidth product (GBW), allowing the inclusion of an RC series to limit bandwidth and shield against high-frequency noise. As the frequency increases, the capacitor acts as a short circuit, and the smaller resistor in parallel with the original resistor reduces the closed-loop gain at high frequencies, achieving the desired bandpass effect. The ideal frequency response of the operational amplifier system is shown in the figure. Because the specifications require a loop gain above 80 dB, the open-loop gain of the operational amplifier have to exceed 92 dB.

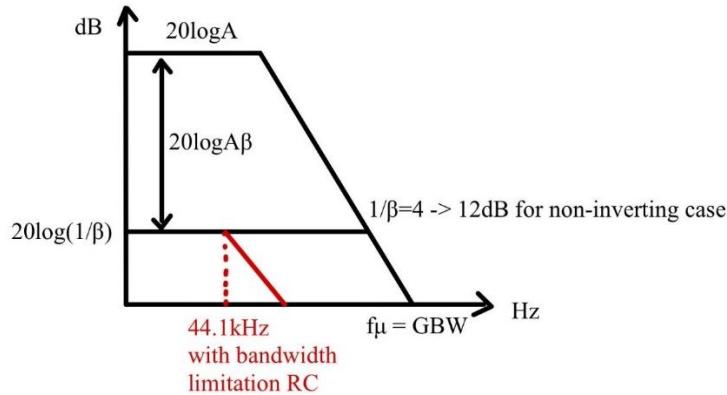


Figure 5 Ideal Frequency Response

The DC voltage at the output point is targeted at 0.8V, half of the supply voltage, ensuring that the output MOSFETs operate within their saturation or subthreshold regions, thereby facilitating larger signal swings. To set this DC voltage, based on the 1:4 voltage division ratio of R1 and RF, the common-mode voltage level at input terminals VP and VN should be established at 160mV, stabilized via negative feedback: in an inverting configuration, the AC signal is input through VN, while VP is used only for setting the DC voltage. Under deep negative feedback conditions, the common-mode voltage at VP is transferred to VN due to the virtual short condition. Then, the common-mode voltage is transferred to the output point proportionally through the voltage drop across the resistors, caused by the feedback current.

However, considering potential offset issues, assume leakage current at the input transistors' gate due to tunneling or other mechanisms. If the impedances seen from the VP and VN inputs are mismatched, this current could create different voltages at the two inputs, leading to offset. An impedance matching network could be added, replicating the external components seen at N on the P side, using the superposition theorem to zero the inputs and the output point.

The role of negative feedback is not limited to setting static input and output DC operating points, its influence on this circuit will be elaborated upon further in the discussion. The operational amplifier system structure, including the described circuit components, is illustrated in the accompanying figure.

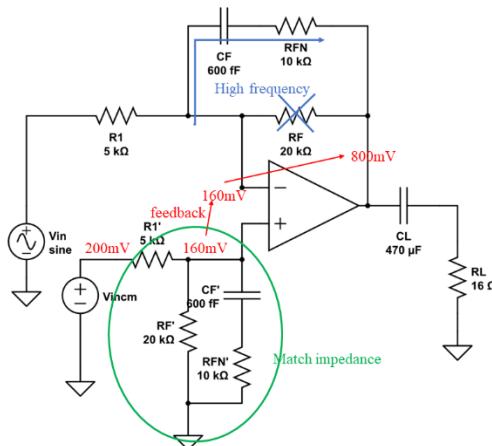


Figure 6 Complete Operational Amplifier System Structure

1.3. Class-AB Audio Amplifier Design Requirements

The operational amplifier to be designed includes a Class-AB audio amplifier with translinear loop control and a constant-gm biasing circuit with start-up circuitry, using the CSM 0.18 μ m CMOS process.

The typical temperature is 60°C, the range of operating temperature is from -40°C to 100°C. The typical supply voltage is 1.6V, the range of V_{DD} is from 1.5V to 1.8V. The load resistance R_L is 16Ω.

The key parameters include Closed-Loop Gain, Common-mode Gain, Total Harmonic Distortion, which should be satisfied for all the fs/sf/ff/ss transistors models in process corner simulation, temperature variation and voltage supply variation. Below are all the specifications.

Table 1. Specification Table (@ VDD = 1.6V and @ 60°C)

Specification	Units		Pre-Simulation	Post-Simulation
Closed Loop Gain ($\times 4$)	dB	-	12 ($\pm 5\%$)	12 ($\pm 5\%$)
Closed Loop <u>Unity</u> Gain Bandwidth	kHz	\geq	300	300
Common-mode Gain	dB	\leq	-75	-73
Feedback Loop Gain	dB	\geq	80	75

Feedback Loop Phase Margin	degree	\geq	60	60
Power Supply Rejection Ratio	dB	\leq	-70	-65
Quiescent Current Consumption	mA	\leq	2	2
Output Swing (@VDD = 1.5V)	V	-	$0.1 \leq V_o \leq 1.4$	$0.1 \leq V_o \leq 1.4$
Total Harmonic Distortion	dB	\leq	-80	-77
Settling Time	μs	\leq	0.45	0.50
Slew Rate	V/ μs	\geq	4	4
Chip Area	μm^2	\leq	-	250 x 200

2. Amplifier Circuit Analysis

2.1. Operational Amplifier Topology Selection

To accurately amplify audio signals while driving low-resistance loads, the operational amplifier should have a high open-loop gain to ensure precision in closed-loop amplification and possess substantial current driving capabilities. A three-stage structure is chosen: the first stage as the input stage, the second as the gain stage, and the third as the output stage. A PMOS folded cascode configuration is selected for the input stage to achieve an open-loop gain of over 60dB. The second stage utilizes a cascode configuration as the gain stage which offers more than 30dB gain, and the output stage employs a Class-AB configuration to enhance the output current capability. The overall circuit is depicted in the accompanying diagram.

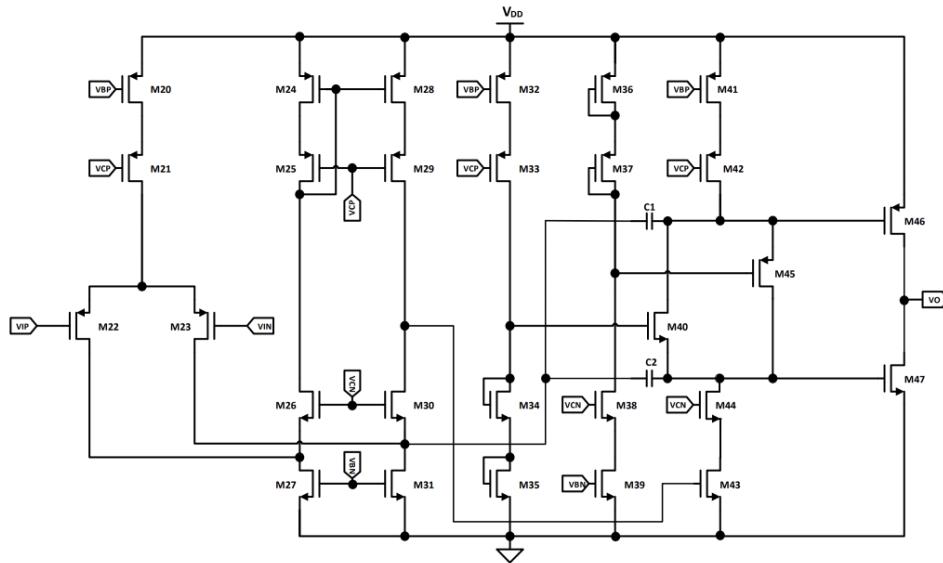


Figure 7 Amplifier Circuit

2.2. Key Parameter Analysis

The primary parameters of concern for this audio operational amplifier are Total Harmonic Distortion (THD), Power Supply Rejection Ratio (PSRR), and output voltage swing.

2.2.1. Total Harmonic Distortion

This metric represents the linearity of the system. While only the fundamental frequency signal in speakers is the original sound signal, the components of the system are inherently non-linear, making the system imperfectly linear. Therefore, after processing through the system, based on the fundamental frequency signal of the original sound wave, multiple harmonics are generated, ultimately resulting in an output sound signal that includes not only the fundamental frequency but also harmonics and their multiples, leading to distortion. So THD can be defined by:

$$THD = 10 \log \frac{\sum P_{harmonic}}{P_{fundamental frequency}} = 20 \log \sqrt{\frac{V_2^2 + V_3^2 + \dots}{V_1^2}}$$

For non-linear devices like MOSFETs, linearity is only assumed within a specific input range to disregard non-linear components and enable small-signal model analysis. Beyond this range, distortion occurs. For MOSFETs operating in saturation and subthreshold regions, derivations can be made respectively.

For saturation region:

$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} + v_{gs} - V_{TH})^2$$

$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} ((V_{GS} - V_{TH})^2 + 2v_{gs}(V_{GS} - V_{TH}) + v_{gs}^2)$$

$$i_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (2v_{gs}(V_{GS} - V_{TH}) + v_{gs}^2)$$

$$v_{gs}^2 \ll 2v_{gs}(V_{GS} - V_{TH})$$

$$v_{gs} \ll 2(V_{GS} - V_{TH})$$

For subthreshold region:

$$I_d = I_s e^{\frac{V_{GS} + v_{gs}}{nV_T}} = I_s e^{\frac{V_{GS}}{nV_T}} e^{\frac{v_{gs}}{nV_T}} = I_s e^{\frac{V_{GS}}{nV_T}} \left(1 + \frac{v_{gs}}{nV_T} + \frac{\left(\frac{v_{gs}}{nV_T}\right)^2}{2!} + \dots\right)$$

$$\frac{\left(\frac{v_{gs}}{nV_T}\right)^2}{2!} \ll \frac{v_{gs}}{nV_T}$$

$$\frac{v_{gs}}{nV_T} \ll 2$$

$$v_{gs} \ll 2nV_T$$

Generally, configuring the op-amp with negative feedback can significantly reduce THD. If the feedback depth is 1+AF, then adding negative feedback reduces distortion to 1/(1+AF) of the open-loop condition. However, negative feedback also reduces gain and can introduce stability issues, producing Transient Intermodulation Distortion (when the input signal's speed exceeds the amplifier's transient response capacity, the circuit's capacitors prevent the output from immediately achieving the correct voltage, and the negative feedback circuit cannot respond promptly, placing the amplifier in an open-loop condition momentarily, causing the amplification circuit to overload and clip).

In practical simulations, I discovered that THD is inversely related to the capacitance of the Ahuja capacitor and directly related to the output stage current, i.e., power consumption. This suggests a trade-off must be made between phase margin, THD, and power consumption. It is speculated that since the left side of the Ahuja capacitor is not an ideal AC ground, changing its capacitance impacts the front part of the circuit. Improvements might be achievable by altering the current distribution ratio for the cascode branches, increasing the upper current to enhance the stabilizing effect of

the M30's V_{GS} on the folding point voltage which is shown in the figure, or switching from Ahuja compensation to Miller compensation with a nulling resistor, which would also enhance the overall system stability. Increasing the static output current may also improve THD by reducing the relative proportion of harmonic components.

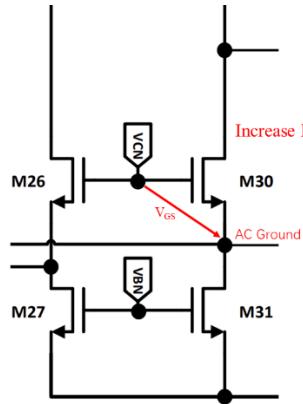


Figure 8 Stabilizing Effect of the M30's V_{GS} on the Folding Point Voltage

2.2.2. Power Supply Rejection Ratio

PSRR is a key parameter for audio operational amplifiers, and it can be expressed as:

$$PSRR = 20 \log \frac{\Delta V_{out}}{\Delta V_{dd}}$$

This parameter describes how the output signal is influenced by power supply ripple. For audio amplifiers, it is essential to suppress noise generated by the power supply at audio output stages such as headphone amplifiers. Noise from the power lines may couple into the signal path via p-channel transistors.

However, the use of a differential input structure in the amplifier naturally minimizes the impact of input-stage noise with low common mode gain, and cascode structure also make the tail current source more ideal. Additionally, negative feedback can help reduce feedback errors by increasing open-loop gain. The gain achieved through the two-stage cascode configuration significantly enhances the accuracy of the closed-loop output.

In practical simulations, I found that increasing the width of the common-source transistors in the current mirror load of the first stage can improve the PSRR. This enhancement is likely due to reducing the overdrive voltage, thus providing more voltage headroom for the transistors below, which optimizes the DC operating point.

Furthermore, the current mirror that converts differential input to single-ended output is inherently asymmetrical, potentially introducing some asymmetry in power supply disturbances. But increasing the L of these transistors to create higher impedance may also reduce PSRR.

The third stage also significantly influences the PSRR. In the P-channel section, the MOS transistors in the translinear loop configured as two diodes might introduce power supply noise to the second stage output point through their V_{GS} , leading to a degradation in PSRR. Increasing the length of the output transistors could also help suppress PSRR, but due to considerations regarding layout area, it has been decided to keep this unchanged. All transistors that may affect the PSRR are indicated in the figure.

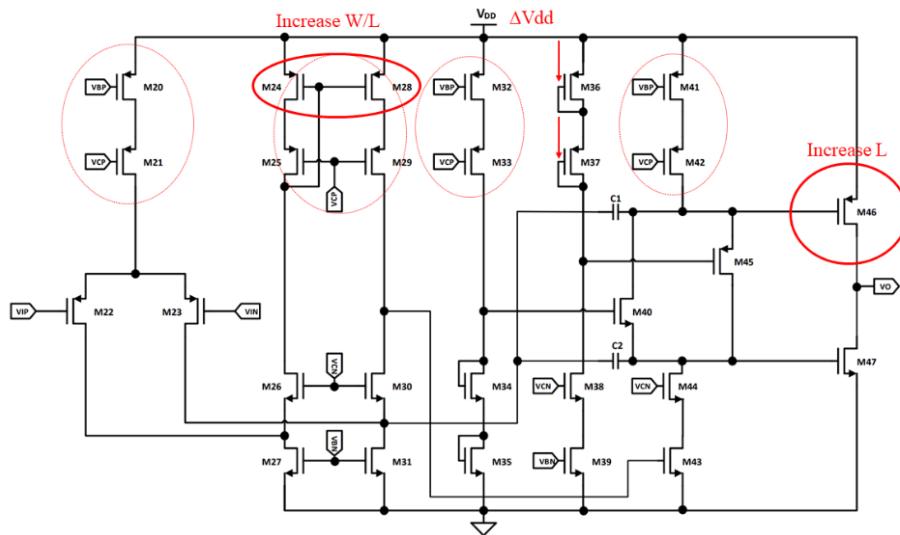


Figure 9 All Transistors that may Affect the PSRR

2.2.3. Output Swing

Output voltage swing represents the upper and lower limits of the output voltage of an operational amplifier. For the output stage, the range of voltage output is only between one overdrive voltage for NMOS and the supply voltage minus one overdrive voltage for PMOS, as the transistors require at least one overdrive voltage to maintain normal operation at the boundary of the saturation region. If the swing is insufficient, the output will be clipped off. When driving a 16Ω load, the voltage swing also helps evaluate the current driving capability limits of the operational amplifier.

In this circuit, with a 1.5V supply and a 16Ω load, the required voltage swing between 0.1V and 1.4V would result in a maximum output current that can be calculated as follows:

$$\Delta V = 0.1$$

$$I_{max} = \frac{\frac{1.6}{2} - 0.1}{16} = 43.75mA @ VDD = 1.6V$$

$$I_{max} = \frac{\frac{1.5}{2} - 0.1}{16} = 40.625mA @ VDD = 1.5V$$

This is also the starting point of our design. By calculating the swing, we can determine the size of the output transistors, and then design the other transistors accordingly.

2.3. Bias Circuit Structure Analysis

The bias circuit consists of a startup circuit, a Dobkin current source, and a self-biased wide-swing cascode current mirror. The circuit diagram is as shown.

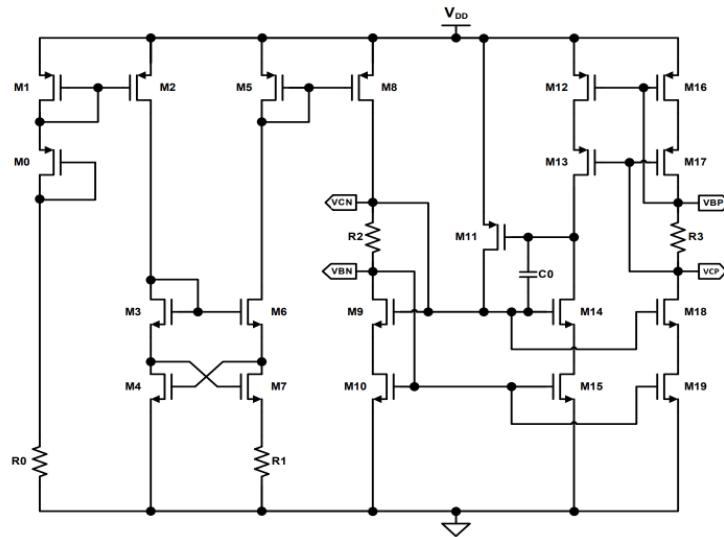


Figure 10 Bias Circuit

2.3.1. Star-up Circuit

The start-up circuit comprises two MOS transistors configured as diodes and a resistor, with M1 responsible for the initial startup. The circuit diagram for this part is shown below.

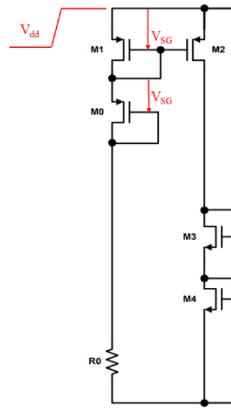


Figure 11 Start-up Circuit

Due to the diode structure, M1's V_{SG} spans between VDD and GND (before power-up, all voltages in the circuit are zero), allowing its V_{SG} to monitor changes in VDD. Upon power-up, if VDD increases beyond M1's threshold voltage, M1 will conduct and generate current. However, without M0 and the resistor, the current in this branch would become excessively large due to the high V_{SG} , leading to power wastage. Therefore, M0 and a resistor are added to divide the voltage and limit the branch current. The current generated by the startup circuit is mirrored into the Dobkin current source by M2, biasing M3 and M4.

2.3.2. Dobkin Current Source

The Dobkin current source can generate a constant-gm current and has a high negative output impedance. In fact, this structure does not require an additional startup circuit: it could simply replace M2 and the left-side startup circuit with a resistor as shown in the figure.

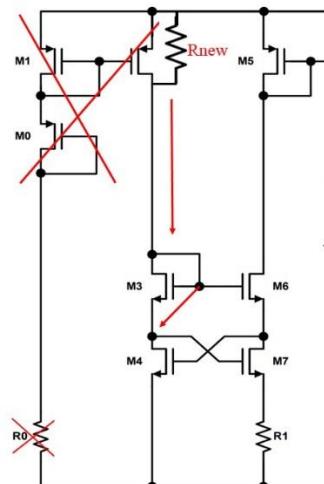


Figure 12 Remove Start-up with a Resistor

In this case, the voltage across resistor - $V_{GS, M3} - V_{GS, M7}$ - R_1 remains sandwiched between VDD and GND, allowing for self-starting. However, in this setup, the current in the left-side branch would be involved in the calculation of the constraints for current production in the Dobkin current source. Changing the parameters of the transistors would also affect the bias current value, complicating the design, hence a startup circuit is included to set the bias current value.

The transconductance of the transistors determines performance parameters such as noise, small-signal gain, and speed, and there is a desire to bias some transistors so that their transconductance does not depend on PVT (Process, Voltage, Temperature). When setting the width-to-length ratio of M7 to be four times that of M6, it can be derived that M6's transconductance equals the reciprocal of the resistance, independent of supply voltage and MOS transistor parameters. The derivation is shown as follows:

$$V_{GS3} + V_{GS7} + I_{out}R = V_{GS6} + V_{GS4}$$

$$V_{GS} = V_{TH} + \Delta V = V_{TH} + \sqrt{\frac{2I}{K' \frac{W}{L}}}$$

$$\text{Set } \frac{W}{L_{M7}} = 4 \frac{W}{L_{M6}}$$

$$\Delta V_7 = \frac{1}{2} \Delta V_6 \text{ @ same } I$$

$$I_{out}R = \frac{1}{2} \Delta V_6 + (V_{TH6} - V_{TH7}) + (V_{TH4} - V_{TH3})$$

$$gm_6 = \frac{2I_{out}}{\Delta V_6}$$

$$R = \frac{1}{2} \frac{\Delta V_6}{I_{out}} = \frac{1}{gm_6}$$

At this point, the current produced is called constant-gm current, which is independent of supply voltage but still a function of process and temperature. When this bias current is mirrored to the tail current source of the differential input transistors, if the temperature changes, the input transistors' gm changes, but the bias current also changes, compensating each other, thus keeping the input transistor gm constant.

In practical simulations scanning the current relationship with supply voltage changes and the input transistor gm variation with PVT changes, the current still depends on V_{DD} , and the input transistor gm is also changing.

NM6007 Assignment: Class-AB Audio Amplifier

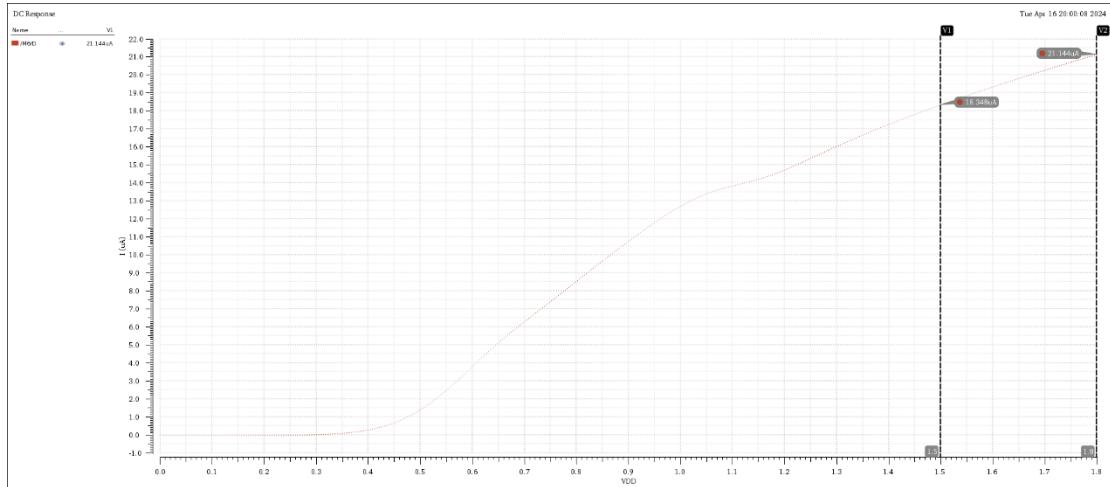


Figure 13 Simulation Curve of the Current Generated by Dobkin as V_{DD} Varies

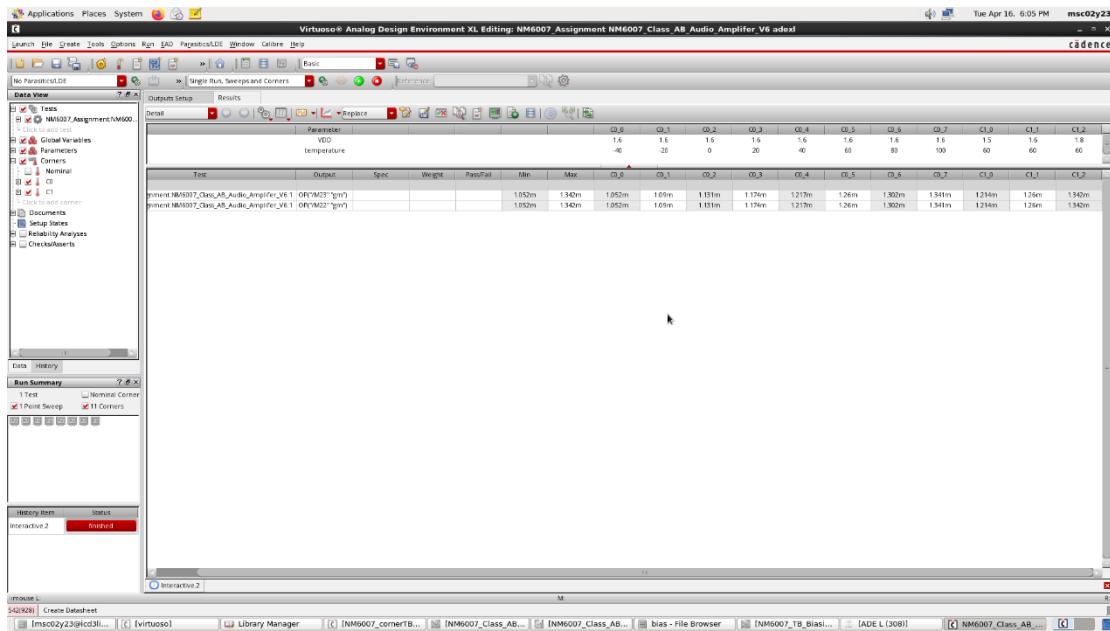


Figure 14 Input Pair G_m Variation with PVT Changes

This is presumed to be due to the resistance value changing with temperature and process, reducing g_m precision. Even when using a bandgap reference to eliminate the current's temperature dependency, process variations still affect precision. Additionally, transistor threshold voltage variations due to body effect can cause inaccuracies in the constraints, which can be mitigated by using a deep n-well to eliminate the effects of substrate bias at the cost of increased cost and area. It is also possible that the performance of MOS transistors in this configuration is not as good as that of BJTs.

2.3.3. Self-biased Wide-swing Cascode Current Mirror

The self-biased wide-swing cascode current mirror is composed of NMOS current mirror, PMOS current mirror, and a loop regulation component. It is capable of outputting four gate voltages: VCN, VBN, VBP, and VCP (or in other words, using multiplier to duplicate transistors, thereby mirroring the current into the main operational amplifier) to bias the cascode circuits within the main amplifier. The circuit diagram is shown below.

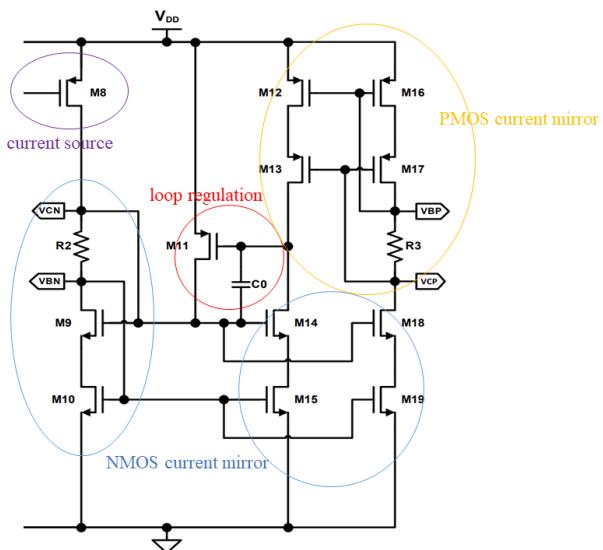


Figure 15 Self-biased Wide-swing Cascode Current Mirror

The cascode mirror trades off voltage swing for higher output impedance and more accurate current replication by increasing the number of transistor layers. This is achieved by the shielding effect of the common-gate transistors, which helps prevent changes in common-source transistors' V_{DS} from affecting the precision of current replication through channel length modulation effects.

Taking the NMOS current mirror as an example, a conventional cascode current mirror is shown as in diagram, where the gate voltage of M9 is equivalent to two V_{GS} , resulting in M18's swing being $V_{GS} + V_{ov}$, which exceeds the saturation maintenance requirement of two V_{ov} for two transistors, thus degrading the swing.

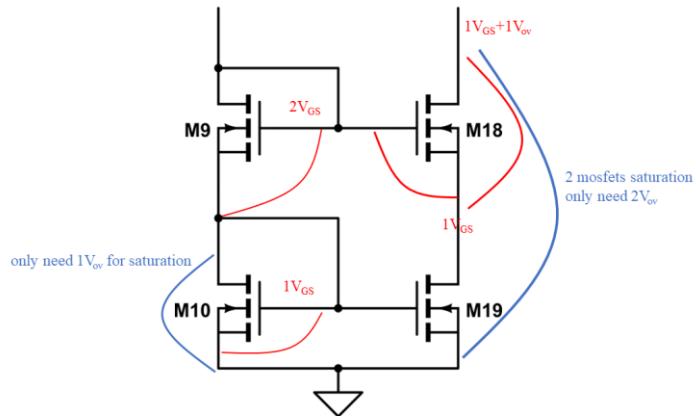


Figure 16 Conventional Cascode Current Mirror

It is evident that this voltage wastage occurs at M10, which to maintain saturation doesn't need a full V_{GS} but just a V_{ov} . Therefore, a high-swing structure can be adopted, as shown in diagram, by positioning M9 between the drain and gate of M10 to consume the excess voltage headroom at the drain of M10, which is shown as in figure.

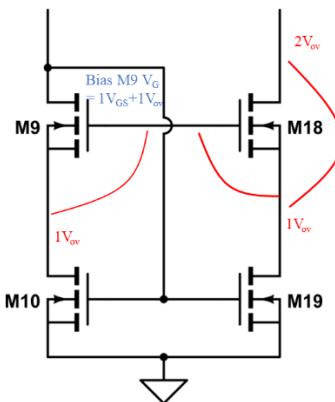


Figure 17 Wide Swing Structure

This configuration biases the gate voltage of M9 at $V_{GS} + V_{ov}$, compressing the drain voltage of M10 to just one V_{ov} . Consequently, M18's swing now matches the standard requirement of two V_{ov} for normal transistor operation, thus achieving a higher swing.

However, this structure necessitates an additional bias to generate the required gate voltage for M9. An option is to incorporate a resistor meticulously designed to have a voltage drop of one V_{ov} over it, given a fixed current from the preceding mirror, to ensure saturation of M10 and achieve self-biasing, which is shown as in diagram.

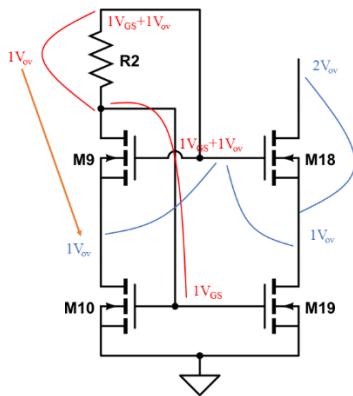


Figure 18 Self-biasing Cascode Current Mirror

This arrangement avoids the need for an additional biasing circuit, reducing power consumption and complexity, but comes with significant trade-offs. In low-power circuits, where the bias current is minimal, particularly at the nA level, the resistance easily reaches the $M\Omega$ range, occupying excessive layout area. Moreover, simulations have shown that because the resistance value is sensitive to PVT variations, the resulting V_{ov} can significantly fluctuate during corner variations, potentially causing M10 to struggle to achieve saturation. The resistance may need to be adjusted to approximately 240mV. Another strategy could be to increase the width-to-length ratio of M9 to reduce its V_{ov} , thereby providing more voltage headroom for M10, however, when the biasing transistors are replicated to the main operational amplifier, their aspect ratio may increase tens of times, resulting in a significant change in area. Additionally, the larger area leads to increased parasitic capacitance of the operational amplifier, affecting the pole positions and potentially deteriorating phase margin, thereby compromising stability.

Introducing M11 as the loop regulation transistor, and C0 as the compensation capacitor, along with M14, M15, M12, and M13 as the NMOS and PMOS current samplers, forms the loop adjustment component. Its operation principle is as follows: Assuming the inaccuracy during current replication results in a higher current through M12-M13 branch compared to M14-M15 branch, additional current flows into the gate capacitance of M11, raising its voltage. This reduces its V_{GS} , decreasing the current flowing into R2-M9-M10 branch and further reducing the current replicated to M14-M15 branch, thereby widening the difference between the upper and lower currents, constituting positive feedback.

However, at this point, the current replicated to M19-M18-R3-M17-M16 branch decreases, reducing the current replicated to M12-M13 branch, and diminishing the difference between the upper part current and lower part current, constituting negative feedback. The presence of this negative feedback reduces errors during current replication and regulates the static operating point of the circuit. The two types of feedback mechanisms are shown in the figure.

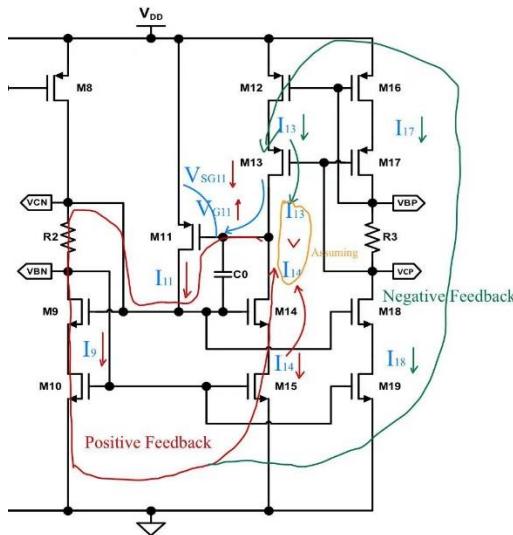


Figure 19 Two Types of Feedback Mechanisms

Ensuring stability of this loop requires that the loop gain of negative feedback is greater than that of positive feedback. When the signal propagates from the gate to the drain of M11, it can be regarded as passing through a common-source reverse amplifier with significant gain. At this point, when the signal passes through M14 in reverse amplification, it constitutes a positive feedback loop. Therefore, introducing a feedforward path C0, where the feedforward signal is phase-inverted with respect to the amplified signal from M11, counteracts each other, weakening the strength of positive feedback. Additionally, during circuit power-up, VDD can be seen as a square wave containing higher frequency components. In this scenario, C0 is considered a short circuit. M11 transitions from a common-source amplifier to diode-connected mode, significantly reducing the gain and ensuring loop stability. From a frequency-domain perspective, perhaps the pole generated at the drain of M11 compensated by the zero introduced by this capacitor in the feedforward path. The loop stability mechanism is depicted in the diagram.

NM6007 Assignment: Class-AB Audio Amplifier

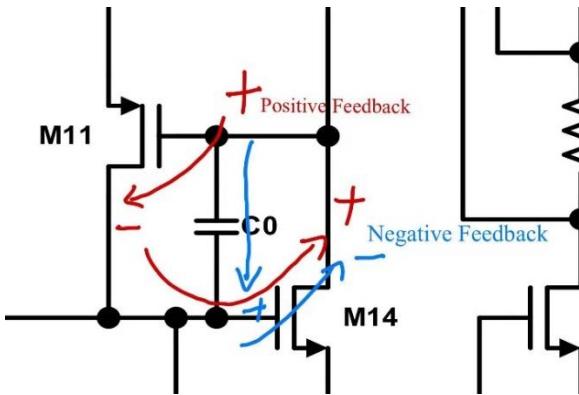


Figure 20 Loop Stability Mechanism

However, in practical simulations, even after removing the regulation transistor and C0, or the entire loop regulation section, the accuracy of current replication does not vary significantly, as shown in the figure. With regulation transistor and C0, the NMOS current is $19.7691\mu\text{A}$, PMOS current is $19.7748\mu\text{A}$.

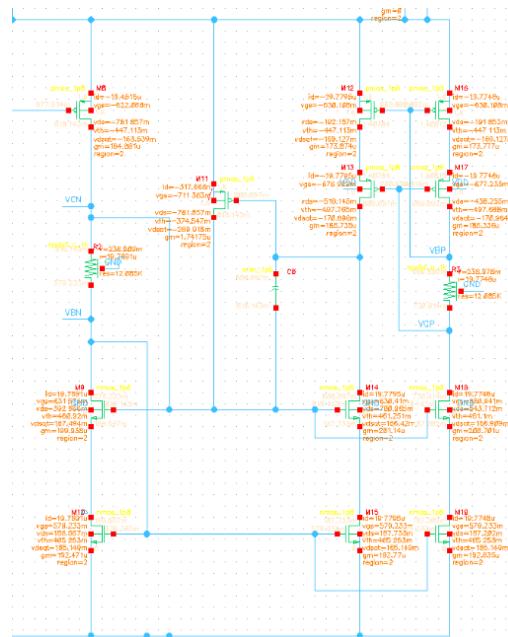


Figure 21 DC with Regulation Transistor and C0

Without the regulation transistor and C0, or by completely removing the middle branch, the DC current remains the same. the NMOS current is $19.4551\mu\text{A}$, PMOS current is $19.4612\mu\text{A}$.

NM6007 Assignment: Class-AB Audio Amplifier

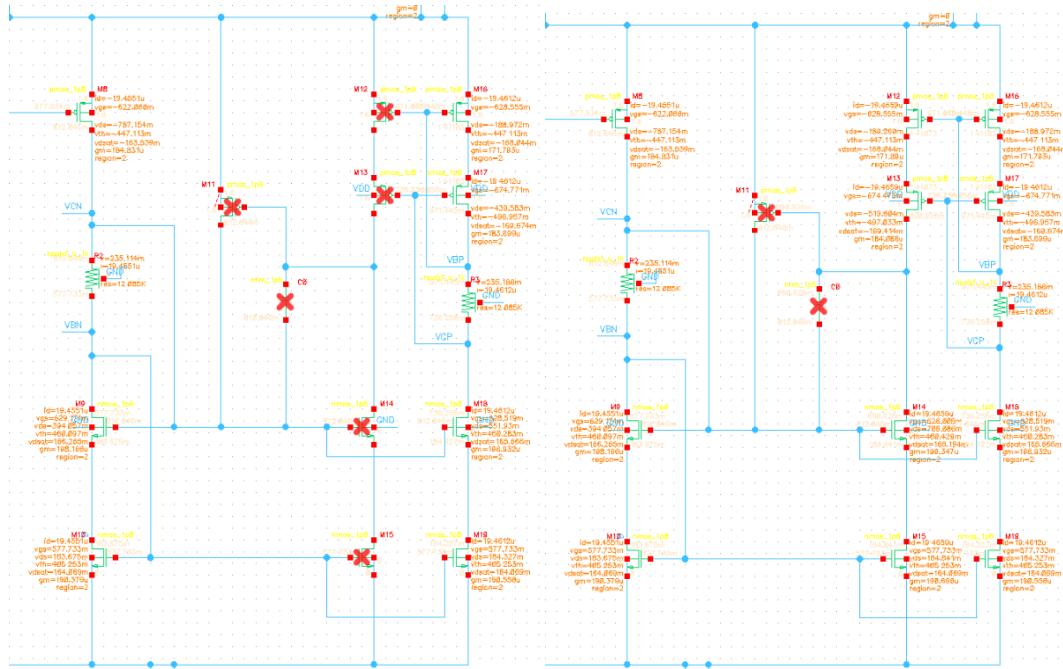


Figure 22 DC when Removing Regulation

2.4. Amplifier Circuit Structure Analysis

The operational amplifier consists of input stage, gain stage, and output stage as shown below. C1 and C2 are used for frequency compensation which will be discussed in 2.4.2.

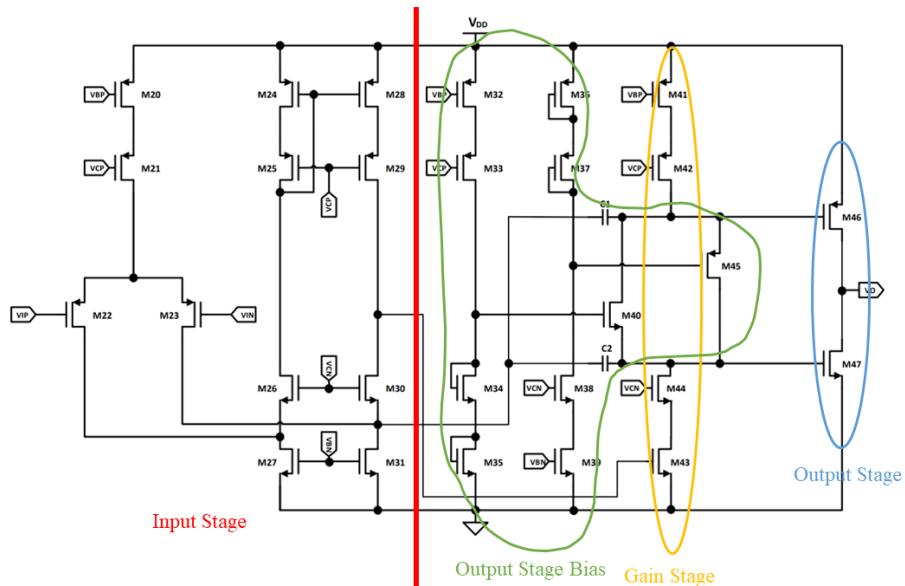


Figure 23 Amp Structure

2.4.1. Input Stage

The input stage adopts a folded cascode structure, load of the input stage is a wide-swing cascode current mirror, which converts the differential input into a single-ended output as the figure shown.

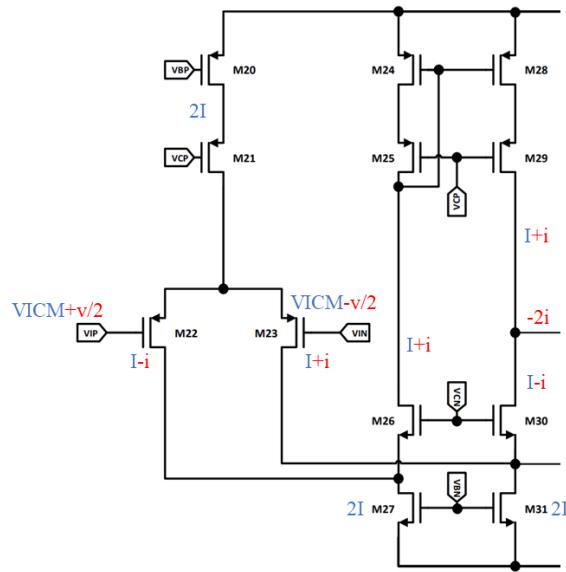


Figure 24 Input Stage

The gain of the input stage can be derived as:

$$\begin{aligned}
 i &= -gm \frac{v_{in}}{2} \\
 -2i &= gm v_{in} \\
 v_{out} &= (-2i) r_o = v_{in} g m r_o \\
 A_v &= \frac{v_{out}}{v_{in}} = gm_{23}(gm_{29}r_{o29}r_{o28}/gm_{30}r_{o30}(r_{o31}/r_{o23}))
 \end{aligned}$$

Since the common-mode point of the input voltage is at 160mV, P-type transistors are used for the input stage to meet the voltage input range around or below the ground, which can be derived as:

$$V_{in, max} = VDD - Vov - Vov - VGS = VDD - 3Vov - Vth \approx 500mV$$

$$V_{in, min} = Vov + Vov - VGS = Vov - Vth < 0$$

Moreover, P-type transistors have 2-5 times smaller 1/f noise compared to N-type transistors because $\overline{V^2} = \frac{K_F}{fC_{Ox}WL}$, where P-type transistors have both a larger area and smaller K_F . P-type transistors can be connected in the SB configuration, which eliminates the substrate bias and isolates the input transistors from VDD, optimizing PSRR. This is easily achieved for P-type transistors in the n-well process by using a

guard ring, but this configuration may reduce the lower limit of the voltage input due to lower V_{th} without body effect.

The principle of the folded cascode structure is to fold the input transistors of the telescopic cascode and introduce a new bias tail current source. This structure improves the output swing and optimizes the common-mode input range at the cost of a smaller bandwidth and gain, as well as larger noise and power consumption. The reason for the reduced gain compared to the telescopic cascode is that the output impedance of the common-source transistor and the input transistor are in parallel at the folding point, reducing the output impedance. The reason for the reduced bandwidth is that the folding point introduces new poles.

2.4.2. Gain Stage and Compensation

The second stage is the gain stage, employing a cascode structure with a gain of:

$$Av = gm_{43}(gm_{44}ro_{44}ro_{43}/gm_{42}ro_{42}ro_{41})$$

The gain stage is shown as:

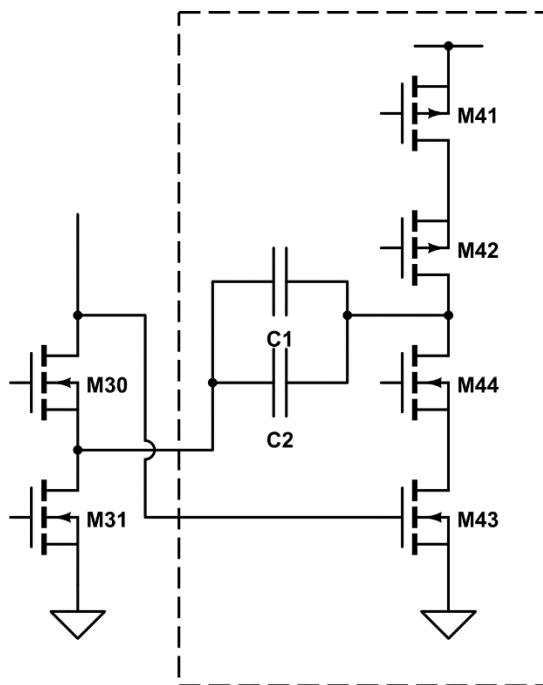


Figure 25 Gain Stage

However, in actual simulations, it was observed that the gain of the two-stage cascode configuration was too high, indicating some overdesign. The second stage can function without utilizing the cascode structure. A simple common-source structure can achieve the expected performance. Moreover, the transistors are more prone to saturation in the

latter case under PVT corner conditions, offering higher robustness. Otherwise, having five transistors in series on a single branch, if unsaturated, the output impedance becomes very low due to linear region, resulting in a much smaller gain even than that of a simple common-source configuration, thus compromising the functionality of the gain stage.

To ensure that the system's gain is determined more accurately by passive components rather than the op-amp itself, which may have imprecise open-loop gain due to significant variations with PVT, we operate the op-amp in a deep negative feedback state. Negative feedback stabilizes the DC operating point while altering the transfer function to achieve more ideal amplification. In a simple feedback system shown in the figure. This can be derived as:

$$\frac{Y}{X} = \frac{A}{1 + \beta A} \approx \frac{1}{\beta} \left(1 - \frac{1}{\beta A}\right)$$

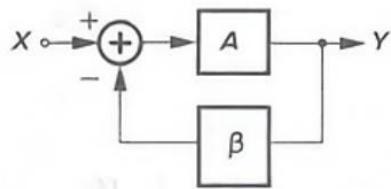


Figure 26 A Simple Feedback System

From the formula, it can be seen that when the loop gain is sufficiently large, the closed-loop gain is determined by the feedback factor, which can be derived from the ratio of two passive components. This ratio does not vary significantly with changes in PVT, allowing for more precise control of the gain.

However, the introduction of feedback can lead to stability issues. When the signal passes through the feedback loop and adds to the input, if the negative feedback becomes positive feedback due to phase shift in the system, it can cause oscillations. Therefore, the Barkhausen Criteria is introduced. When the loop gain is 1 (if greater than 1, the circuit is more easily to oscillate) and the phase shift is -360 degrees, meaning that negative feedback changes to positive feedback due to a phase shift of -180 degrees and the loop gain keeps the signal strength same within the feedback loop, the system reaches the lower limit of positive feedback oscillation. In this case, the circuit has two high-impedance nodes at the outputs of the first and second stages, resulting in two poles in the system. Two poles can provide a phase shift of -180 degrees, therefore, frequency compensation is necessary to maintain stability.

Additionally, because the feedback network is typically composed of passive components, where β is less than or equal to 1, the system's stability is worst when the feedback coefficient is 1 for maximum loop gain. In this case, the loop gain $A\beta$ degenerates to the open-loop gain A . Therefore, typically, the stability of the system can be judged by examining the zeros and poles of the open-loop gain function. In other words, simply observing the positions of the zeros and poles in the circuit diagram is sufficient, as closing the loop will reduce the loop gain, making the system inherently more stable.

Stability of the op-amp system is generally assessed by observing the locations of gain crossover frequency (G_X , gain = 1) and phase crossover frequency (P_X , phase = -180°) on the Bode plot. According to the change in phase, the location of the secondary pole corresponds to a phase shift of -135 degrees (the main pole already provides a phase shift of -90 degrees). After a decade in frequency, the phase shift becomes -180 degrees. That is to say, the frequency point that generates a -180 -degree phase shift, namely P_X , is related to the absolute position of the secondary pole.

The rule for the decrease in gain is that after passing through one pole, the rate of gain decrease is -20 dB/decade, and after passing through two poles, it becomes -40 dB/decade. The rate of gain reduction depends on the number of poles encountered. Typically, the rate of gain reduction, which determines the position of G_X , depends on the relative positions of the main pole and the secondary pole. In simple terms, when the two poles are close, the phase shift is mainly determined by the position of the secondary pole, leading to a rapid decrease. However, the gain drops slowly, as there is not much frequency range available for decrease, making it easy for the loop gain to remain above 1 at the -180 -degree phase shift position, resulting in the system becoming positive feedback and starting to oscillate.

It can be seen that to ensure system stability, it is necessary to ensure that P_X is greater than G_X . But how far should P_X be from G_X ? It is not only necessary to consider the requirements of margin for PVT variations but also to consider the circuit's response. Therefore, the angle difference between the phase corresponding to G_X and P_X is defined as phase margin, which represents the remaining margin before oscillation occurs. Based on experience, insufficient phase margin, such as 45 degrees, can lead to

underdamping phenomena. In this case, the transfer function exhibits a peak, known as frequency-domain Peaking. In the time domain, it results in ringing as shown in the figure, where the step response requires a long time of damped oscillation to stabilize.

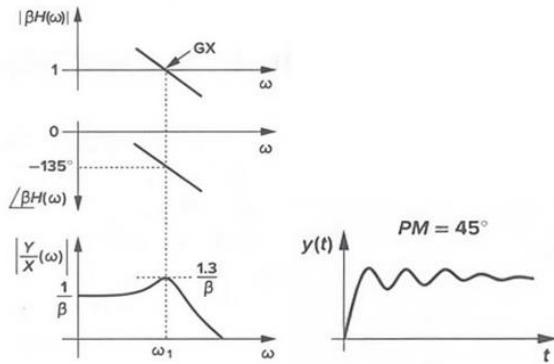


Figure 27 Peaking and Ringing

If the phase margin is too large, such as 90 degrees, the circuit exhibits overdamping, reducing response speed. A phase margin of around 60 degrees is considered appropriate. Therefore, it is necessary to design the position of the secondary pole reasonably. When the frequency corresponding to the secondary pole is the same as ω_u , the phase margin is 45 degrees. When $\omega_{p2} = 2\omega_u$, the phase margin is 63 degrees, and when $\omega_{p2} = 3\omega_u$, the phase margin is 72 degrees. Generally, setting ω_{p2} is equal to 2 or $3\omega_u$ is sufficient.

In addition to designing the location of the second dominant pole, we can also introduce capacitive compensation to adjust the position of the dominant pole, thereby achieving the required phase margin. By placing a capacitor across both sides of the second-stage amplifier, a large equivalent capacitance is generated using the Miller effect. The content of Miller effect is as follows:

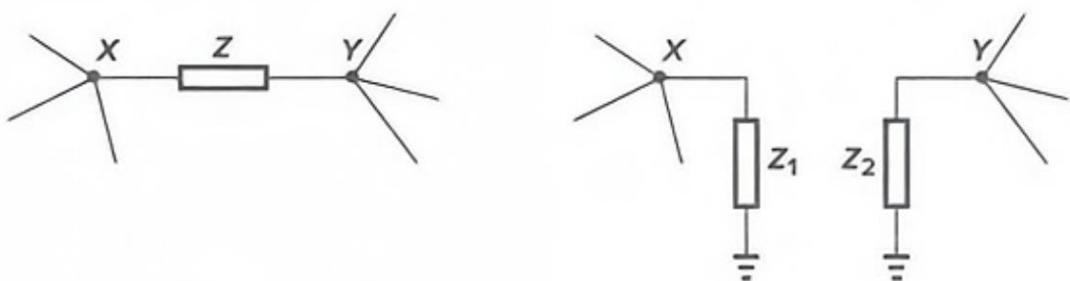


Figure 28 Miller Effect

$$\frac{V_X - V_Y}{Z} = \frac{V_X}{Z_1}$$

$$Z_1 = \frac{Z}{1 - \frac{V_Y}{V_X}} = \frac{Z}{1 - A_v}$$

$$Z_2 = \frac{Z}{1 - \frac{V_X}{V_Y}} = \frac{Z}{1 - \frac{1}{A_v}}$$

It can be observed that the Miller effect is caused by the inverter's reverse amplification increasing the voltage difference across the capacitor, which in turn increases the current flowing through the capacitor, effectively amplifying the capacitance.

Compared to directly adding a practical capacitor to ground, the Miller capacitor saves area and does not sacrifice much bandwidth. This equivalent capacitance mainly affects the main pole, increasing its capacitance and lowering its frequency, causing the gain to decrease earlier, and its impact on the phase shift at the secondary pole position is relatively small.

However, when using Miller compensation with an inserted capacitor, a right-half-plane zero is generated. This zero arises because the Miller capacitance introduces a feed-forward path across the second stage at high frequencies. Consequently, at the output of the second stage, because the gain decreases as the frequency increases, at a certain frequency, the signal output after being inverted by the second stage, and the feed-forward signal passing directly through the Miller capacitor, have the same amplitude but opposite phase. They cancel each other out, resulting in the creation of a zero.

This right-half-plane zero causes the phase to drop more rapidly while the gain decreases more slowly, shifting the PX to the left and the GX to the right, thereby worsening stability. This can be mitigated by inserting a nulling resistor in the feed-forward path to weaken it and shift the right-half-plane zero to the left half-plane, turning the negative phase shift positive.

To avoid the use of a nulling resistor, Ahuja compensation can be employed utilizing the characteristic of the folding node in a folded cascode structure, where that node acts as an AC ground. At this folding node, only small-signal currents flow in and out without a change in voltage, thus it is treated as an AC ground. Also, with a fixed DC

current, the V_{GS} of transistor M30 is determined by its gate voltage V_{CN} , making the source potential a fixed DC voltage, which for small signals is ground.

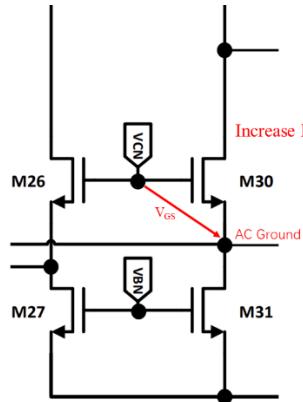


Figure 29 AC Ground

Analyzing from the small-signal perspective, the impedance looking downward from the drain of M30 can be simplified to gmr_o^2 for cascode, whereas from the drain of M31 it appears as only r_o . Hence, a voltage fluctuation Δv at the drain of M30 results in a response of $\frac{\Delta v}{gmr_o^2} r_o = \frac{\Delta v}{gmr_o}$ at the drain of M31. It can be seen that the voltage fluctuations are significantly reduced by the intrinsic gain of M30. In essence, this folding node can be considered as AC ground, allowing the compensation capacitor to be connected here, thereby removing the feed-forward path.

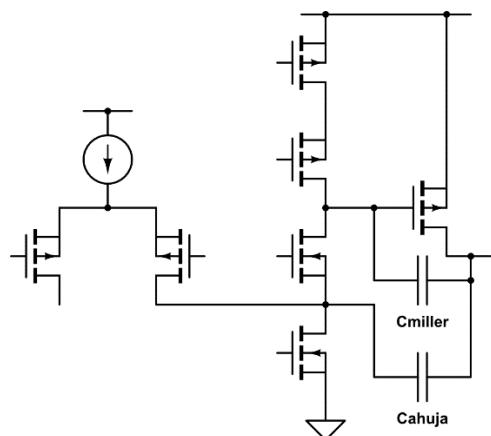


Figure 30 Miller and Ahuja

However, simulations have revealed that this point is not an ideal AC ground, leading to worsening THD and system stability. These issues might be improved by redistributing the current and increasing the I_D of M30 to stabilize its V_{GS} .

2.4.3. Output Stage

The third stage is the output stage, which requires the ability to drive a small resistor load and output a large current. If the second stage is directly connected to a small resistance, it will result in the output impedance being in parallel with this 16Ω resistor, causing the gain of the second stage to be lost. Therefore, a buffer stage with a voltage gain of 1 and a high current gain is used, specifically employing a Class-AB structure. The Class-AB structure resembles an inverter, with small signals input on the gates of both PMOS and NMOS transistors. This structure allows for very low static power consumption while providing high dynamic driving capability. Its push-pull output mode ensures that the current during large signal establishment is not limited by the quiescent current, enabling better slew rates, which is advantageous when driving heavy resistor loads.

Since both the P and N output transistors in a Class-AB configuration must be controlled by the signal from the preceding stage, in contrast, traditional output stages require only one type of transistor, either PMOS or NMOS, to be controlled by the input signal from the previous stage, the biasing circuit for a Class-AB amplifier is significantly more complex. In this case, a translinear loop structure is used to bias the output transistors. The essence of this approach is that the current is independent of V_{DD} and is proportionally replicated, shown in the figure.

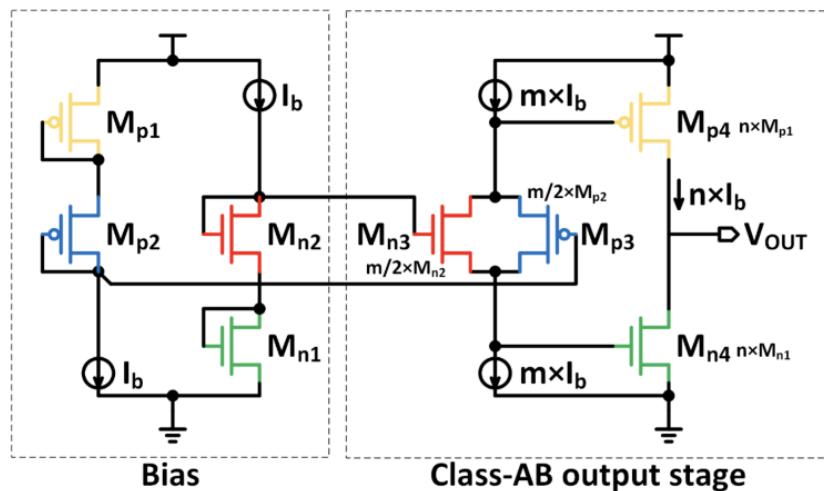


Figure 31 Current Replication in the Translinear Loop

For example, with N-type transistors, the principle of this structure involves connecting M35, M34, M40, and M42 into a translinear loop as the figure showing.

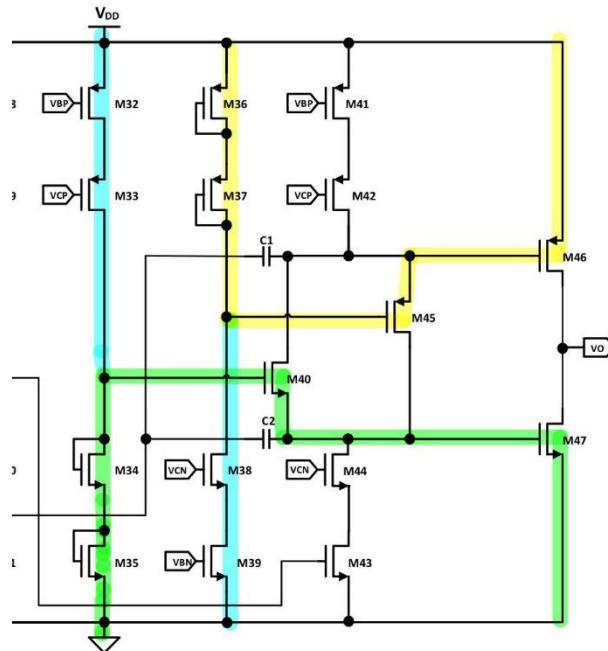


Figure 32 Output Stage with Translinear Loop

M35 and M34 provide a voltage of two V_{GS} under a fixed bias current, and then M40 and M42 distribute these two V_{GS} respectively. The same principle applies to the P-type transistor. M40 and M45, as adjusting transistors, distribute the bias current produced by M41 and M42, which can be designed to split the current evenly, making the total current equal to twice the bias current value of M35 and M34. Thus, the DC current flowing through M34 and M40 is the same, and setting their width to length ratio consistently, ignoring channel length modulation, results in $V_{GS,34}=V_{GS,40}$, hence $V_{GS,35}=V_{GS,42}$. Although the gates of M35 and M42 are not connected, they can be considered as a current mirror in static conditions, thus biasing the V_{GS} of the output transistors.

By adjusting the width-to-length ratio between M42 and M35 with the same V_{GS} , it is possible to set the quiescent current by adjusting the number of output transistor multipliers, which is determined by the bias current, reducing the circuit's sensitivity to PVT variations. When the circuit is dynamically operating, if there is a positive input voltage at the second stage input transistor, it will cause the voltage at the second stage output point to drop, i.e., the source voltage of M40 drops. With the gate voltage clamped by diodes M39 and M34, the V_{gs} of M40 increases, causing the V_{gs} of M42 to decrease, and the N-type output transistor enters the subthreshold region and turns off. At the same time, the increased V_{gs} of M40 enhances its current driving capability, increasing the current. With the total current fixed, the current through M45 decreases,

reducing its V_{gs} to the subthreshold region, thus M46's V_{gs} increases and enters the output state.

It can be seen that the translinear loop structure can provide reasonable gate voltages to the output transistors at DC, while M40 and M45 only distribute the current, so it does not affect the AC gain. Of course, all these are under the ideal condition of ignoring channel length modulation and Drain Induced Barrier Lowering, but when the operational amplifier is configured in a closed loop, the negative feedback automatically adjusts the DC operating point, allowing the system to overcome some non-ideal factors.

However, simulations have shown that although the voltage gain of the third stage is considered very small, in reality, due to the large coupling capacitance, the output stage can be seen as disconnected from the 16Ω load resistor at low frequencies, so the output impedance of this stage does not decrease, resulting in a significant voltage gain, which can affect the judgment of the actual amplifier gain. The output point of the third stage also introduces a zero-pole pair, although this does not affect the system's response at normal operating frequencies. The loop frequency response in the pre-simulation with and without load capacitance is shown in the figure.

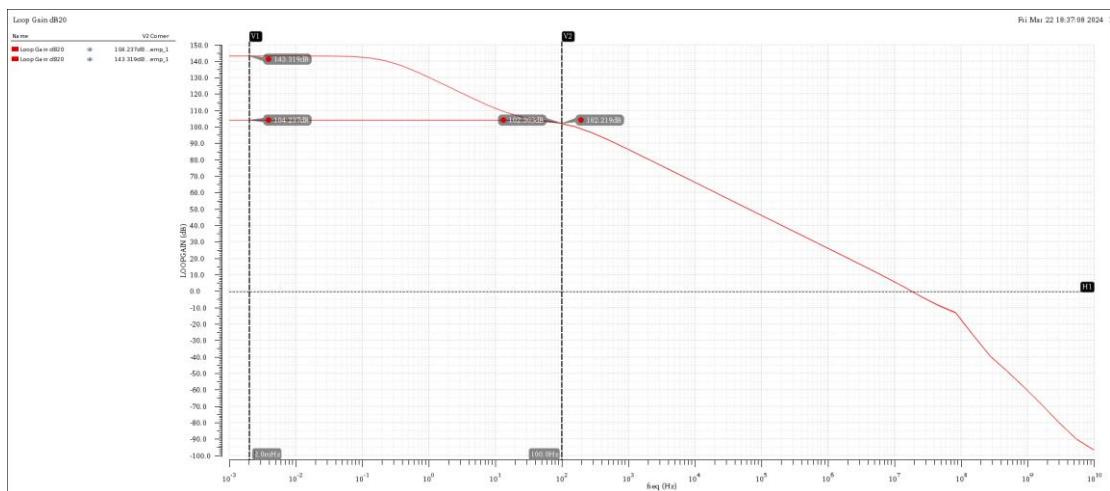


Figure 33 Loop Frequency Response of Pre-simulation with and without Load Capacitance

3. Design Process

The design process generally involves: measuring the parameters of MOS transistors, allocating branch currents based on power consumption, distributing overdrive

voltages for each branch, calculating the width-to-length ratio of general transistors. Based on the swing requirements, calculate the width-to-length ratio of the output transistors, determine the sizes of other transistors in the translinear loop using its formula, calculate the sizes of current source transistors and resistors in the bias circuit using the Dobkin structure constraint formula, set the width-to-length ratio of the input transistors, and fine-tune the sizes of transistors based on performance parameters.

3.1. MOSFET Characterizations

3.1.1. K'

Build the testbench circuit as shown in the figure, with the MOS transistor sizes using an NMOS width-to-length ratio of 5u/1u and PMOS of 20u/1u.

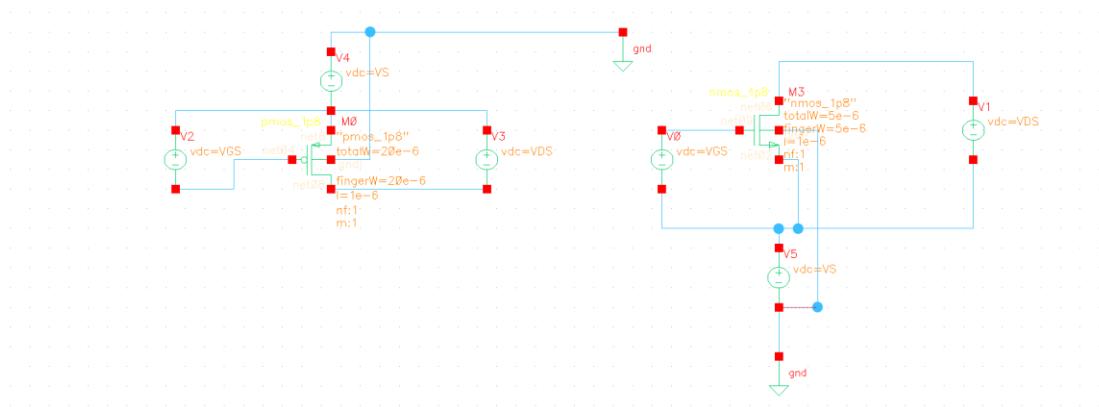


Figure 34 MOSFET Characterizations Testbench

Based on these equations:

$$I_D = \frac{1}{2} K' \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$\sqrt{2I_D} = \sqrt{K' \frac{W}{L} (V_{GS} - V_{TH})}$$

$$\frac{\partial \sqrt{2I_D}}{\partial V_{GS}} = \sqrt{K' \frac{W}{L}}$$

First, simulate the transfer characteristic curve of the MOS transistor. Then, use a calculator to multiply the result by 2 and take the square root. Finally, calculate the partial derivative with respect to V_{GS} . This process will produce a final graph that allows for the calculation of K' by substituting the width-to-length ratio. Choose the maximum value, 32.4m for NMOS, 30.18m for PMOS, from the curve to calculate K' .

NM6007 Assignment: Class-AB Audio Amplifier

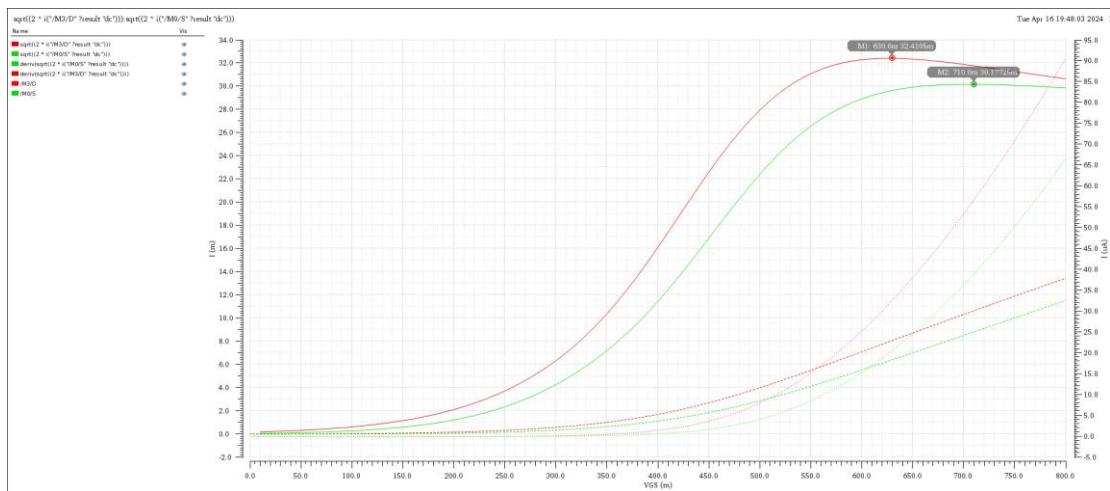


Figure 35 Transfer Characteristic Curve and K' Calculation

Table 2. K'

Type	K'
NMOS, 5u/1u	210u
NMOS, 5u/0.2u	160u
PMOS, 20u/1u	45.5u
PMOS, 20u/0.2u	55u

3.1.2. V_{TH}

$$I_D = \frac{1}{2} K' \frac{W}{L} (V_{GS} - V_{TH})^2$$

From this formula, it can be deduced that when I_D equals 0, $V_{GS} = V_{TH}$, which means the value at the intersection of the graph and the x-axis is V_{TH} . Fit a straight line within the range where the square law holds, and observe the value at the intersection. Estimate the threshold voltage of the N-channel transistor as 460 mV, and the threshold voltage of the P-channel transistor as 515 mV.

NM6007 Assignment: Class-AB Audio Amplifier

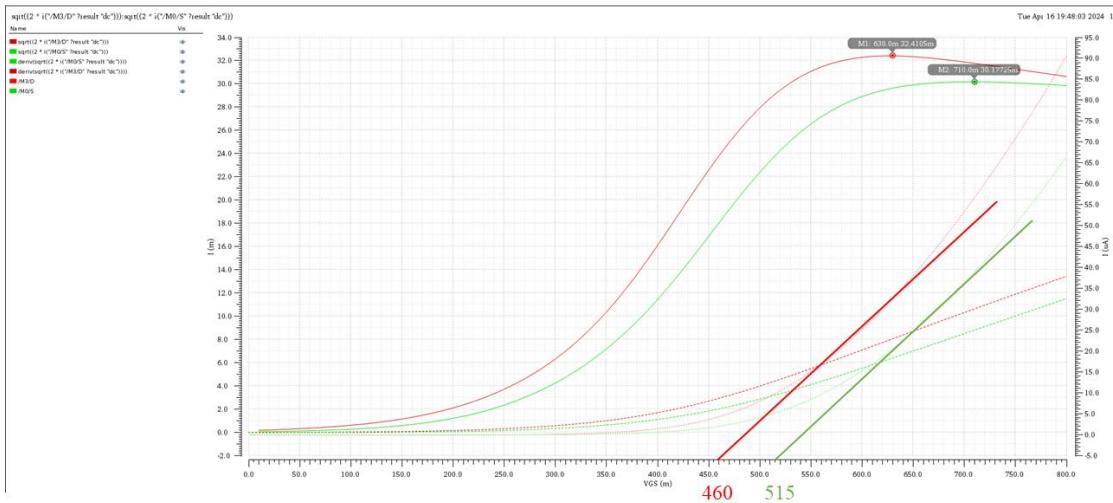


Figure 36 V_{TH} Measurement

3.1.3. γ

The parameter γ is related to the body effect. Therefore, while scanning the transfer characteristic curve to obtain the relationship between V_{GS} and I_D , use Parametric Analysis to scan V_{SB} .

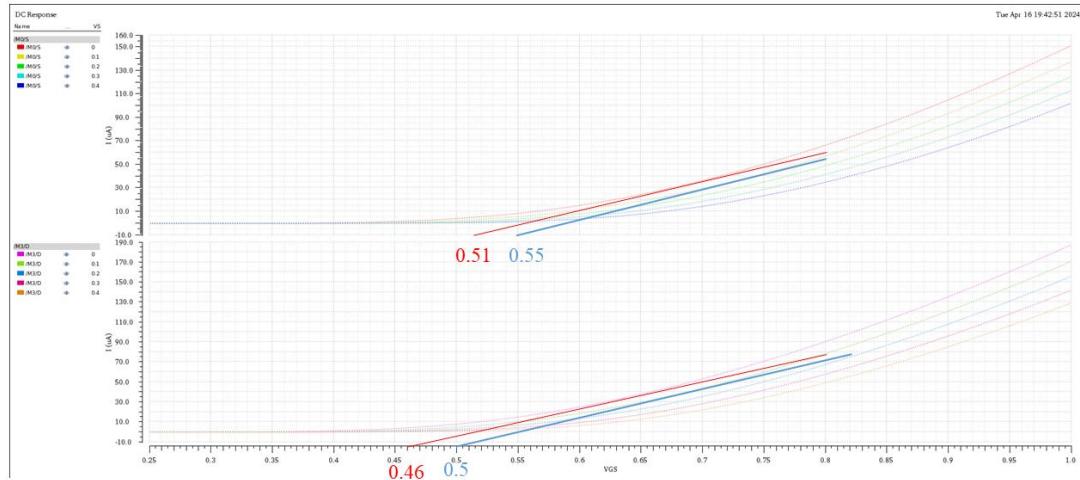


Figure 37 γ Measurement

According to the formula:

$$V'_{TH} = V_{TH0} + \gamma(\sqrt{2\varphi_F + V_{SB}} - \sqrt{2\varphi_F})$$

$2\varphi_F$ is usually set to 0.6V, and select two curves with $V_{SB} = 0\text{V}$ and $V_{SB} = 0.1\text{V}$ for calculation. The calculation shows that the γ values for both NMOS and PMOS are approximately $0.65\text{V}^{1/2}$.

3.1.4. λ

In an ideal scenario, the output current I_D of a MOSFET in the saturation region is independent of V_{DS} , meaning that increasing V_{DS} does not significantly change I_D , effectively acting as an ideal current source with infinite output impedance. However, the channel length modulation effect causes the length of the pinched-off region to increase with an increase in V_{DS} , which decreases the channel's length and its resistance, thereby increasing the current and resulting in a finite output impedance.

Therefore, a variable λ defined as the channel length modulation coefficient is introduced, with the formula similar to the Early voltage in BJTs, caused by base width modulation effects in BJTs. The formula for the channel length modulation coefficient λ can be derived as follows.

Actual channel length:

$$L' = L - \Delta L$$

Approximate treatment:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2 \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \left(1 + \frac{\Delta L}{L}\right)$$

Assume linear:

$$\frac{\Delta L}{L} = \lambda V_{DS}$$

Substitute zero for the current in the equation:

$$\begin{aligned} I_D &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \left(1 + \lambda V_{DS}\right) = 0 \\ 1 + \lambda V_{DS} &= 0 \\ V_{DS} &= -\frac{1}{\lambda} \end{aligned}$$

The actual meaning is to extend the saturation region curve of the output characteristic curve in reverse and find its intersection with the x-axis, which is the Early voltage. Therefore, simulate the output characteristic curve of the MOS transistor and substitute the numerical values from one of the points on the curve into the formula for calculation. Choose $V_{GS}=700\text{mV}$, $V_{DS}=600\text{mV}$, which are V2 with top curve. The calculation results in λ value are of 0.203 for the NMOS and 0.349 for the PMOS.

NM6007 Assignment: Class-AB Audio Amplifier

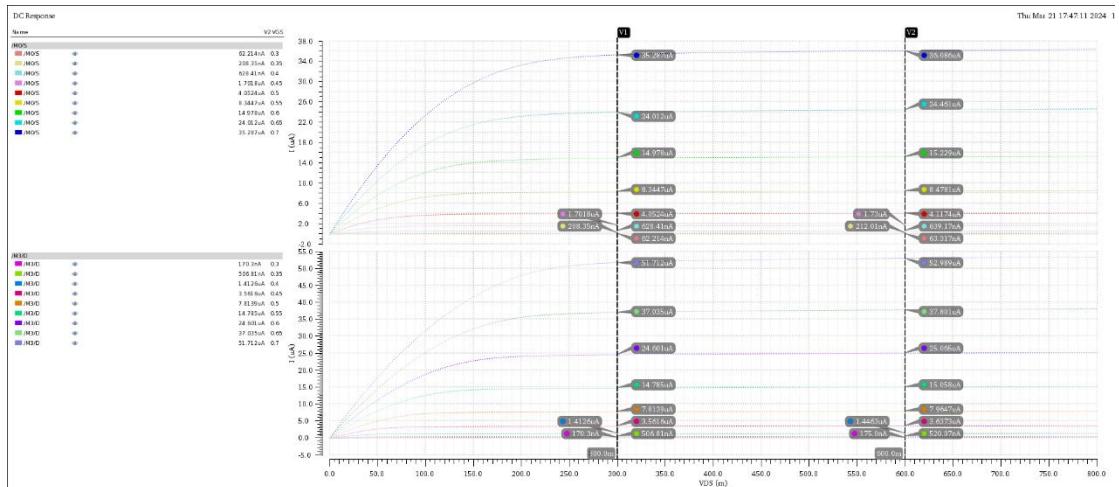


Figure 38 Output Characteristic Curve

3.1.5. r_o & R_{ON}

First, r_o is the AC impedance under small-signal conditions, resulting from channel length modulation effects and other short-channel effects. In an ideal scenario, the output current I_d does not change with variations in V_{ds} , which implies an infinite output impedance, akin to an ideal voltage-controlled current source. It is derived from the derivative of I_d with respect to V_{ds} , that is:

$$r_o = \frac{dV_{ds}}{dI_d} = \frac{1}{g_{ds}} \approx \frac{1}{\lambda I_D}$$

R_{ON} is the DC resistance or the conduction resistance under large signal conditions, which can be directly obtained by dividing the voltage across the device, V_{DS} , by the current flowing through the device, I_D , that is:

$$R_{ON} = \frac{V_{DS}}{I_D}$$

Specifically, when the MOS transistor operates in the linear region, it can be regarded as a voltage-controlled resistor, with the gate voltage controlling the resistance of the channel. At this time, the output characteristic formula is:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right)$$

If $V_{DS} \ll 2(V_{GS} - V_{TH})$, the MOS transistor enters the deep triode region, the formula can be approximated as:

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

Because the power transistor reaches the boundary between the saturation and linear regions at maximum swing, it can also be considered as a conduction resistance at this time. At the same time, these two types of impedance can also be distinguished from the image, as shown in the figure.

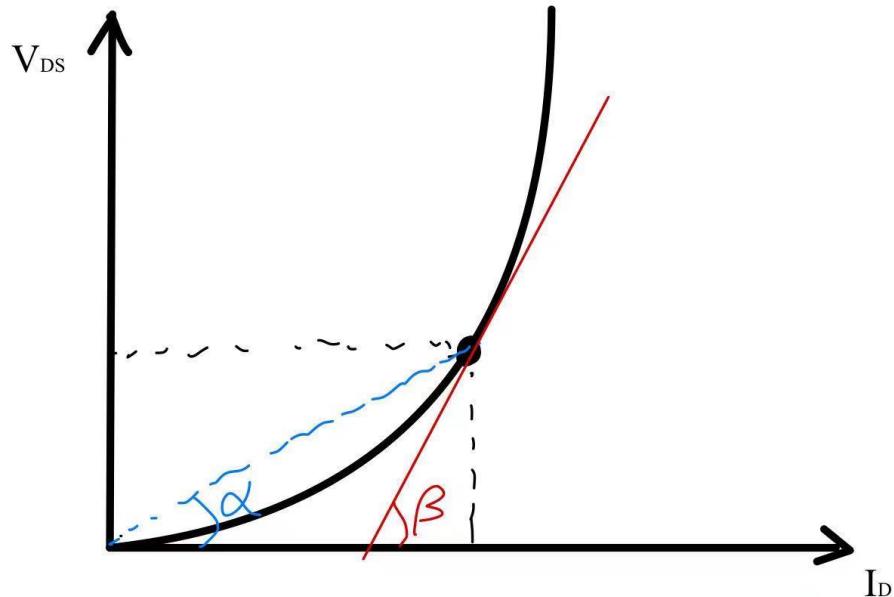


Figure 39 r_o & R_{ON}

$$r_o = \tan \beta$$

$$R_{ON} = \tan \alpha$$

Use $r_o \approx \frac{1}{\lambda I_D}$ to estimate r_o from 3.1.4, r_o for NMOS is $88\text{k}\Omega$, for PMOS is $79.7\text{k}\Omega$.

Use $R_{ON} = \frac{V_{DS}}{I_D}$ to calculate R_{ON} from 3.1.4, R_{ON} for NMOS is $15\text{k}\Omega$, for PMOS is $22\text{k}\Omega$.

The results from manual calculations are quite close to those from DC simulations, as shown in the figure. It should be noted that at this point, r_o should be: $r_o = \frac{1}{g_{ds}}$

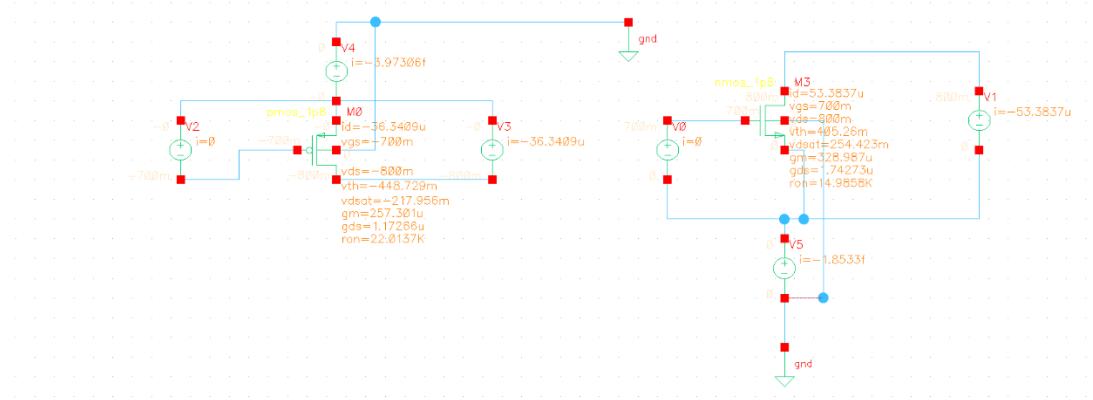


Figure 40 DC Simulation Result

3.2. Distribution of Current and $V_{overdrive}$

The bias circuit's base current is set at $20 \mu\text{A}$. By increasing the L of M11, the current is reduced to ensure precise replication by the current mirror. Since the startup circuit is not isolated from the main circuit after startup, its current is set to $10 \mu\text{A}$ to minimize power wastage.

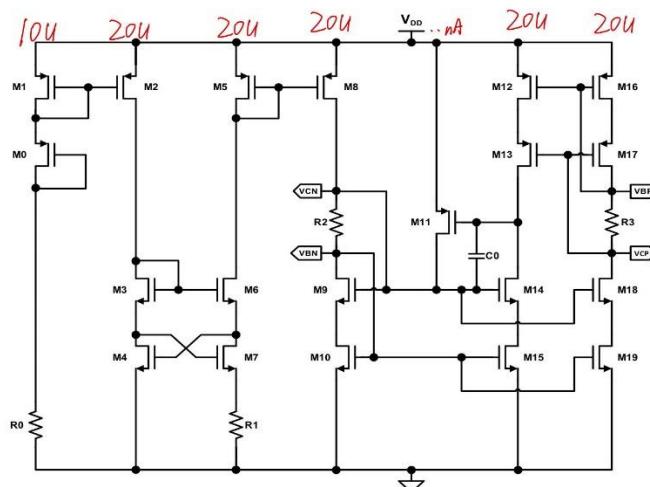


Figure 41 Distribution of Bias Current

Considering a quiescent current consumption of 2 mA and the translinear loop's ability to transition from static to dynamic current, 1 mA of quiescent current is allocated to the output transistors. The currents in the operational amplifier are set in multiples of $20 \mu\text{A}$, using Multiplier to ensure that the bias currents can be proportionally replicated from the bias circuit into the op-amp. A larger current is allocated to the first stage to meet performance specifications. M40 and M45 split the DC current equally, each receiving $20 \mu\text{A}$, the same as the current through M34, M35, M36, M37 to simplify calculations of translinear loop.

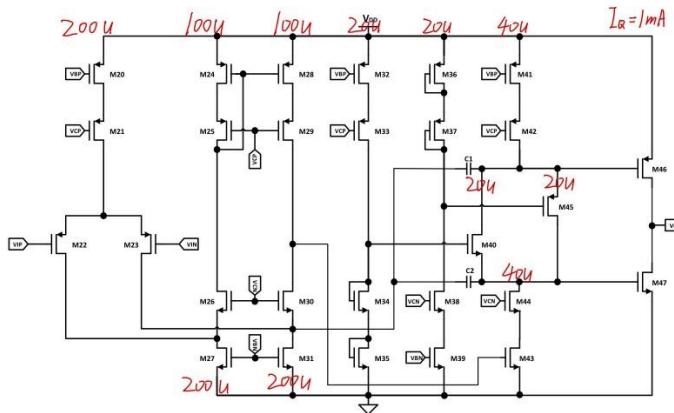


Figure 42 Distribution of Amp Current

At this point, the total power consumption of the circuit is approximately 1.6 mA, with a margin of 400 μ A reserved to accommodate variations in PVT.

Each MOS transistor is allocated a V_{ov} of 200 mV. Because in a 0.18 μ m process, this value maximizes the product of current density gain and bandwidth. Next, based on the base current of 20 μ A, K' , and V_{ov} , it is easy to calculate the basic width-to-length ratio of the transistor: NMOS 5u/1u, PMOS 20u/1u.

If the current needs to be increased, this can be achieved by increasing the Multiplier to enlarge the width-to-length ratio, while aiming to keep other device parameters unchanged. Separate adjustments may be required for transistors in different parts of the circuit, such as the input and output transistors, the Dobkin current source, and transistors within the translinear loop.

3.3. Adjustment of the Dimensions of Special MOS Transistors

3.3.1. Dobkin Current Source

As the currents of both sides are set to 20 μ A, and $\Delta V=200mV$, Resistance can be calculated in the following manner:

$$I_{out}R = \frac{1}{2}\Delta V_6 = 0.1$$

$$R = \frac{0.1}{20\mu} = 5k$$

To get W/L of M6, M3, M4, M7:

$$R = 5k = \frac{1}{gm_6} = \frac{1}{\sqrt{2\mu_n C_{ox} \frac{W}{L} I_{out}}}$$

$$\frac{W}{L_6} = \frac{W}{L_3} = \frac{W}{L_4} \approx \frac{5\mu}{1\mu}$$

$$\frac{W}{L_7} = 4 \frac{W}{L_6} = \frac{20\mu}{1\mu}$$

3.3.2. Output Transistors

Based on the requirements for swing, when the output transistor provides maximum swing, its own overdrive voltage is reduced to 0.1V. At this point, the MOS transistor is at the boundary between the saturation and linear regions, and its output characteristic curve can be described as:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2 \right)$$

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})V_{DS} = \mu_n C_{ox} \frac{W}{L} \Delta V^2$$

$$I_{Dmax} = \frac{\frac{1.5}{2} - 0.1}{16} = 40.625mA @ VDD = 1.5V \Delta V = 0.1V$$

$$\frac{W}{L} = 25.4k$$

Similarly, PMOS width-to-length ratio is 73.9k.

In simulations, it was observed that a width-to-length ratio of 10,000 for NMOS and 3,000 for PMOS could meet the swing requirements in the pre-simulation. However, post-simulation results showed that while the swing significantly deteriorated, there was still ample layout space to increase the width-to-length ratio of the output transistors, making it beneficial to do so.

But, if we increasing the width-to-length ratio of the output transistors, however, leads to higher static power consumption. This can only be balanced by adjusting the translinear loop and lowering their V_{GS} , but this adjustment risks leaving the cascode transistors in the gain stage unsaturated, as the V_{GS} of the output transistor is the sum of the V_{DS} of the cascode transistors, which was discussed in section 2.4.2 before.

3.3.3. Translinear Loop

Taking NMOS as an example, the translinear loop during DC is shown in the figure.

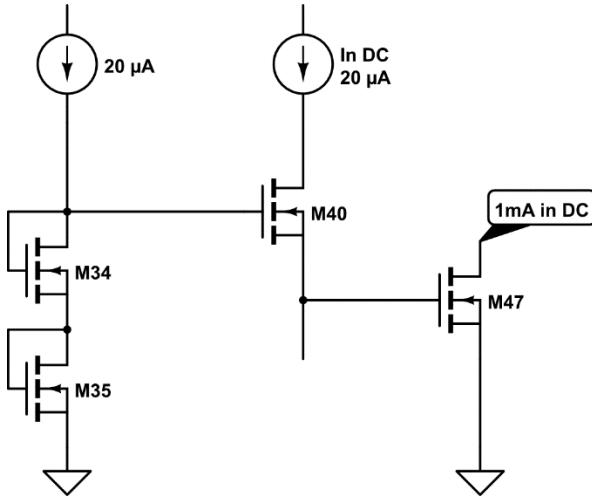


Figure 43 NMOS Translinear Loop

Setting M34 and M40 to the same width-to-length ratio because they both operate at same current of $20\mu\text{A}$, they have same V_{GS} . Therefore, it can be deduced:

$$V_{GS,35} + V_{GS,34} = V_{GS,40} + V_{GS,47}$$

$$V_{GS,34} = V_{GS,40}$$

$$V_{GS,35} = V_{GS,47}$$

This makes M35 and M47 appear as a current mirror. The desired quiescent current for M47 is 1 mA. Now, M35's quiescent current is provided by the bias current source, which is $20\mu\text{A}$. The ratio between these two is 50. Therefore, by setting the width-to-length ratio of M35 to 1/50 of M47's, the quiescent current of M47 can be set to 1 mA. As the size of M47 has been determined by the swing, the size of M35 can be directly derived. It is important to note that, to ensure accurate current replication, the gate lengths of both transistors are set to $0.2\mu\text{m}$.

The following is the setting for the sizes of M34 and M40. Since both during DC and AC, M34 and M35 provide a bias voltage of $2V_{GS}$, it can be listed as:

$$V_{GS,40,DC,20\mu\text{A}} + V_{GS,47,DC,1mA} = V_{GS,40,AC,sub} + V_{GS,47,AC,43.75mA}$$

Alternatively, simply estimating, assuming $2V_{GS} = 1.2\text{V}$, and $V_{GS,sub} = V_{TH} = 450\text{mV}$, the current-voltage equation for M40 can be listed as:

$$V_{GS,40,DC,20\mu\text{A}} = \sqrt{\frac{2I_{40\mu\text{A}}}{K' \frac{W}{L}}} + V_{TH} = 2V_{GS,34,35} - V_{GS,47,sub} = 0.75\text{V}$$

$$\frac{W}{L} \approx 4.44$$

In reality, the sizes of M40 and M34 need to be continuously adjusted through simulation to ensure that the quiescent current of the output transistor does not exceed the specifications. M40 and M34 equally share the DC current, and M41, M42, M43, M44 all need to be in saturation.

3.3.4. Input transistors of the First and Second Stages

Because the specifications require a loop gain above 80 dB, the open-loop gain of the operational amplifier have to exceed 92 dB, first stage should offer a gain of 60dB or more, second stage should offer 30dB. As the gain and gm is calculated as:

$$Av1 = \frac{v_{out}}{v_{in}} = gm_{23}(gm_{29}r_o_{29}r_o_{28}/(gm_{30}r_o_{30}(r_o_{31}/r_o_{23}))$$

$$Av2 = gm_{43}(gm_{44}r_o_{44}r_o_{43}/(gm_{42}r_o_{42}r_o_{41}))$$

$$gm = \sqrt{2I_D K' \frac{W}{L}}$$

Given that r_o is approximately between 600 kΩ to 1 MΩ, and the gm of the common-gate transistors in cascode structure is roughly above 700 μS, to meet the gain requirements, the gm of the input transistor of the first stage is estimated to be tens of μS. Based on the allocated current for the input transistor, the width-to-length ratio of the input transistor is found to be very small. Generally, the calculation of the gm of the input transistor is based on the GBW requirements specified in the specs.

However, as it is a low-frequency operational amplifier without speed-related requirements, the size of the input transistor is mainly determined by parameters such as PSRR and THD. Clearly, a larger open-loop gain can improve the quality of negative feedback and optimize performance parameters. Therefore, choosing a larger width-to-length ratio is necessary. However, larger sizes may introduce larger parasitic capacitances, requiring continuous iterative optimization in simulation.

For the second stage, since the allocated current is small, r_o is large, reaching levels of 1-2 MΩ. The gm of the common-gate transistor is approximately between three hundred to four hundred μS. This calculation yields a width-to-length ratio for the input transistor of the second stage of around 40 to 50. However, the transistors in the second stage always struggle to reach saturation persists. Altering the dimensions of the input transistor would affect the DC operating point in the middle, and because the

second stage and translinear loop are integrated, the DC operating point is greatly affected. Therefore, continuous adjustment is also required in simulation.

3.3.5. Aspect Ratio of All the Transistors with Capacitor and Resistor Size

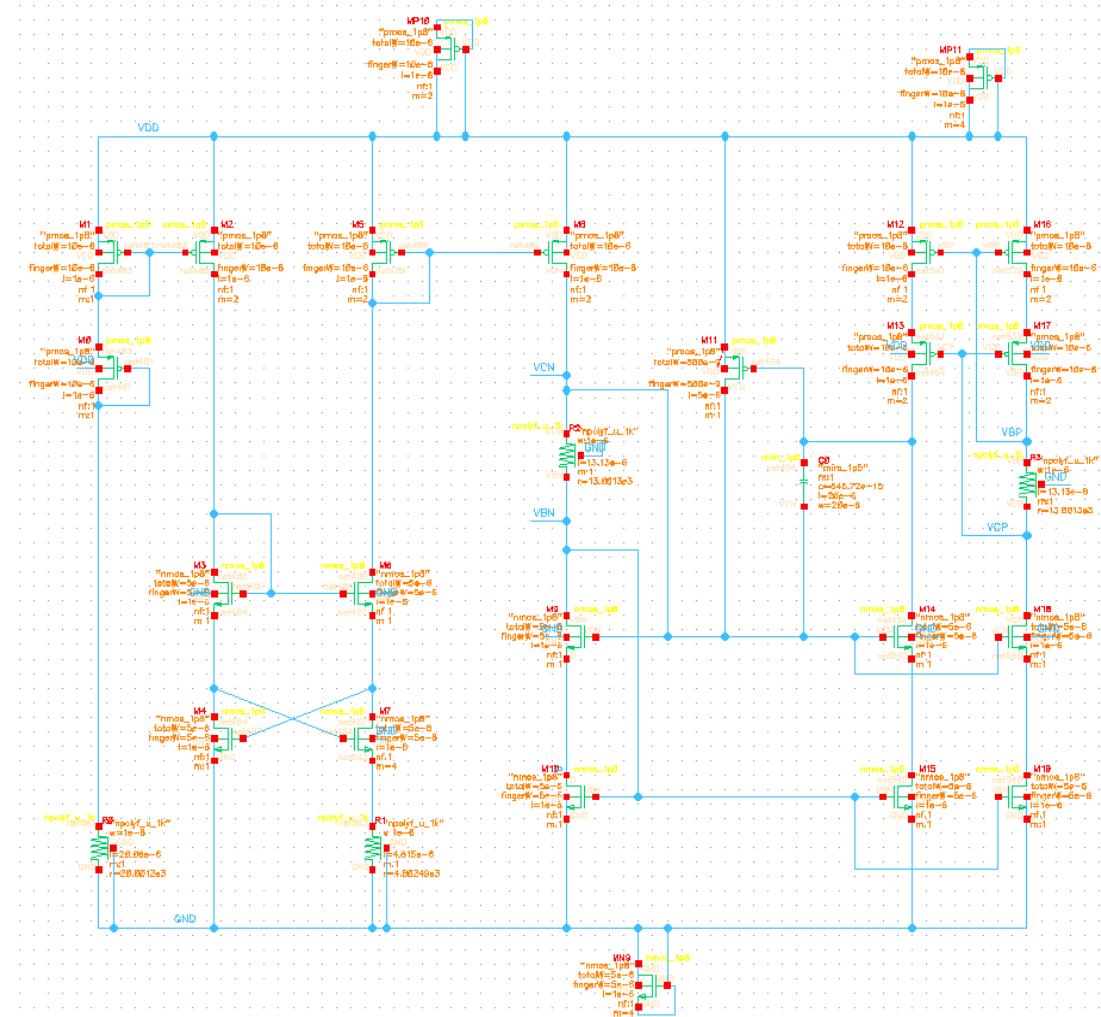


Figure 44 Transistor Sizing of Bias

Transistors with all ports connected to VDD or GND are dummy transistors.

Table 3 Transistor Sizing of Bias

Bias	W/L (um/um)	V _{dsat} (mV)	g _m (uS)
M0	10/1	-182	94
M1	10/1	-167	94.2
M2	10/1, M=2	-166.8	184
M3	5/1	173.8	201.8
M4	5/1	162.6	201
M5	10/1, M=2	-163.5	183.8

NM6007 Assignment: Class-AB Audio Amplifier

M6	5/1	173.2	197.8
M7	5/1, M=4	94.2	312.6
M8	10/1, M=2	-163.5	184.8
M9	5/1	167.5	199.9
M10	5/1	165.1	192.5
M11	0.5/5	-270	1.74
M12	10/1, M=2	-169	173.9
M13	10/1, M=2	-170.7	185.7
M14	5/1	166.4	201.1
M15	5/1	165.1	192.8
M16	10/1, M=2	-169.1	173.8
M17	10/1, M=2	-171	185.3
M18	5/1	167	200.7
M19	5/1	165.1	192.6
R0 (start-up)	1um*20um, 20kΩ, V=188mV		
R1 (Dobkin)	1um*4.815um, 4.6kΩ, V=82.5mV		
R2 (N-self)	1um*13.13um, 13kΩ, V=239mV		
R3 (P-self)	1um*13.13um, 13kΩ, V=239mV		
C0	20um*20um, 0.64672pF		

NM6007 Assignment: Class-AB Audio Amplifier

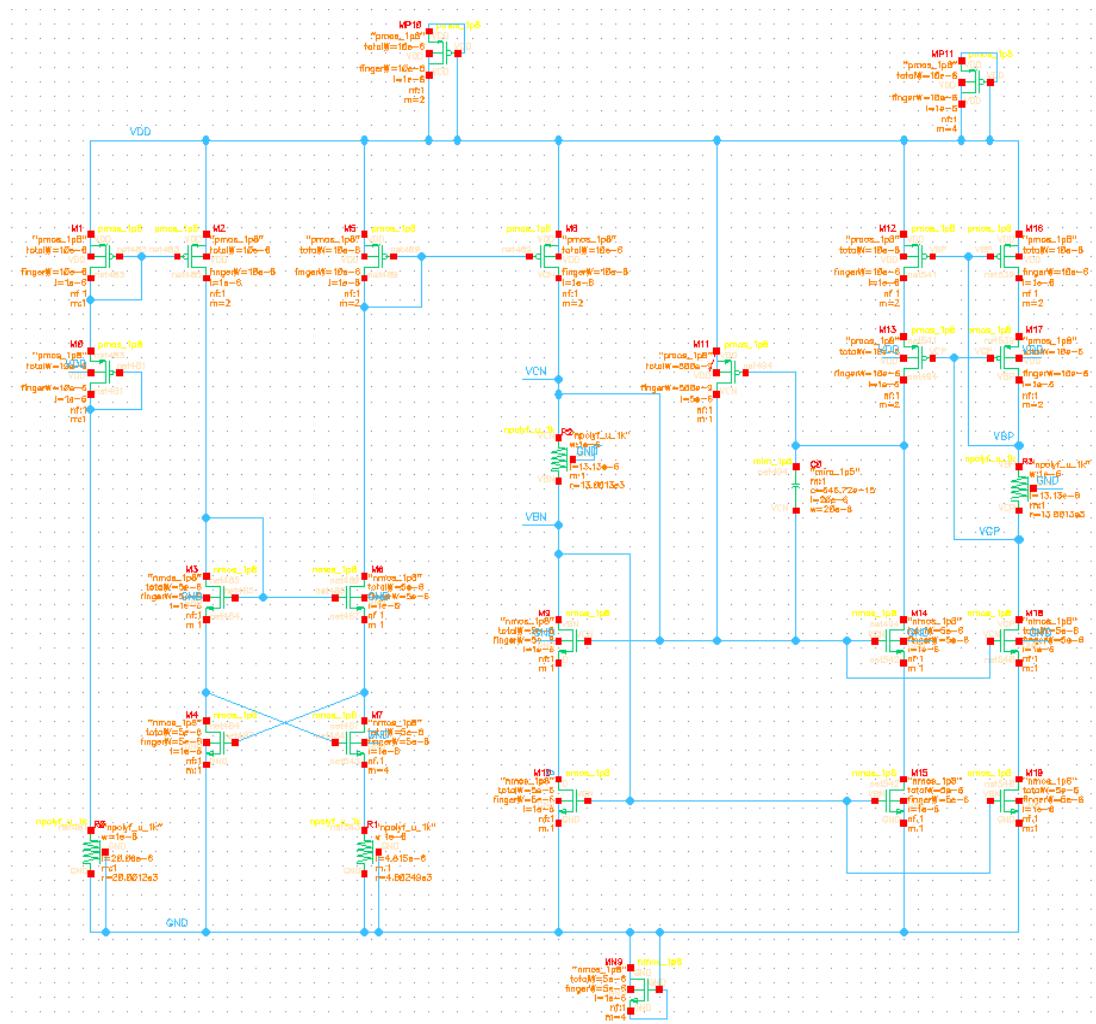


Figure 45 Transistor Sizing of Amp

Table 4 Transistor Sizing of Amp

Amp	W/L (um/um)	Vdsat (mV)	gm (S)
M20	10/1, M=20	-169.1	1.74m
M21	10/1, M=20	-170.6	1.86m
M22	10/0.4, M=8	-134.6	1.26m
M23	10/0.4, M=8	-134.5	1.26m
M24	10/1, M=16	-136.8	1.09m
M25	10/1, M=10	-171.1	924.7u
M26	5/1, M=5	166	1m
M27	5/1, M=10	165.1	1.93m
M28	10/1, M=16	-136.8	1.09m
M29	10/1, M=10	-170	933.5u
M30	5/1, M=5	168.1	994.3u

NM6007 Assignment: Class-AB Audio Amplifier

M31	5/1, M=10	165.1	1.92m
M32	10/1, M=2	169.1	173.6u
M33	10/1, M=2	-171.4	184.3u
M34	8/1	141	244u
M35	14/0.2	64.6	393.3u
M36	45/0.2	-67.4	371.9u
M37	24/1	-162.9	200.9u
M38	5/1	168.6	197u
M39	5/1	165.1	192.1u
M40	8/1	126.1	203.2u
M41	10/1, M=4	-169.1	346.6u
M42	10/1, M=4	-172.3	363.1u
M43	35/1	99.8	613.2u
M44	5/1, M=2	168.3	395.9u
M45	24/1	-178.9	227.2u
M46	237.5/0.2, M=8	-66.5	16.6m
M47	125/0.2, M=4	70	17m
C1	20um*16um, 0.52188pF		
C2	20um*16um, 0.52188pF		

4. Pre-simulation

Display the typical simulation results at 1.6V using the typical model at 60 degrees Celsius.

NM6007 Assignment: Class-AB Audio Amplifier

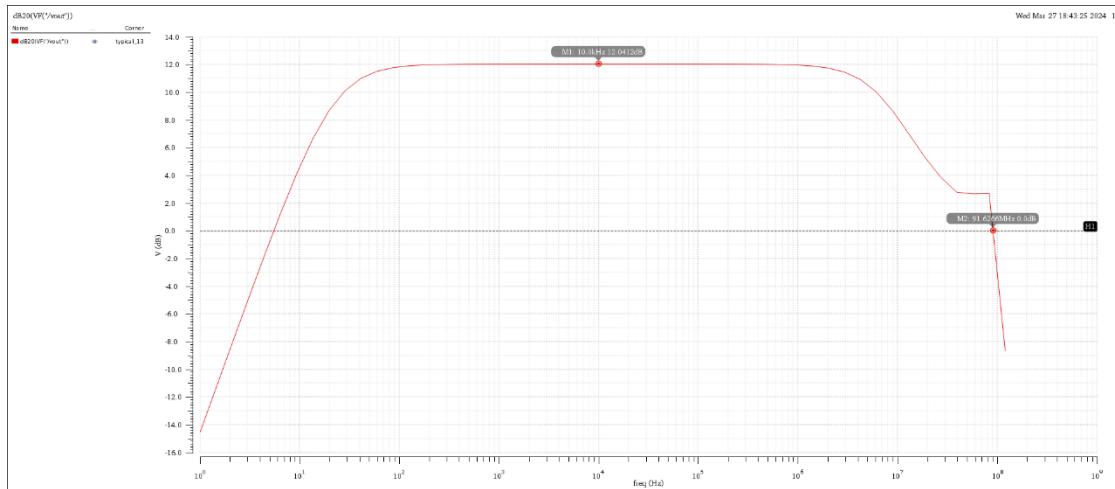


Figure 48 Closed-Loop Gain and Closed Loop Unity Gain Bandwidth in Pre-simulation

Closed loop gain is 12.04dB. Closed loop unity gain bandwidth is 91.6266MHz. This value is very large because the capacitance in the RC series network used to limit the bandwidth is very small. If I want to increase the capacitance, the output will oscillate in transient simulations with square waves. Therefore, I have to reduce the capacitance and give up its role in limiting the bandwidth.

Suspecting that the stability might be affected by the zeros and poles of the external circuit or the circuit architecture, or it could be an issue with Ahuja compensation. In the oscillation waveform, it's observed that the oscillation period is approximately 70ns, which corresponds to a frequency of around 14MHz, close to the 0dB point of the loop gain. However, at that point, the phase margin is still over 70 degrees. The relationship between these two factors is not clear yet. In the future, it would be necessary to find the charging and discharging loop corresponding to the oscillation frequency.

4.3. Common-mode Gain

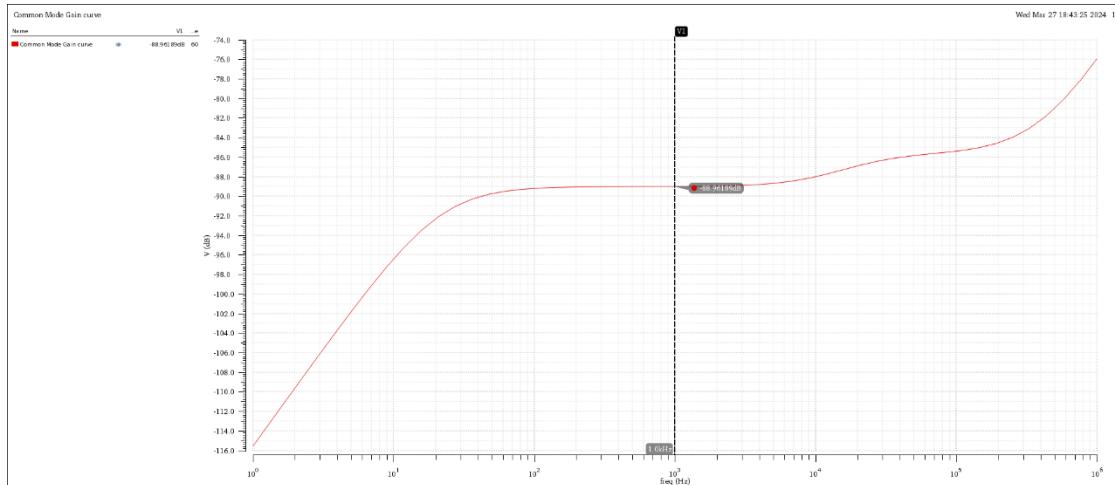


Figure 49 Common-mode Gain in Pre-simulation

Common-mode gain is -88.96189 dB at 1kHz. It can be seen that the differential input effectively suppresses common-mode noise.

4.4. Feed-back Loop Gain and Phase Margin

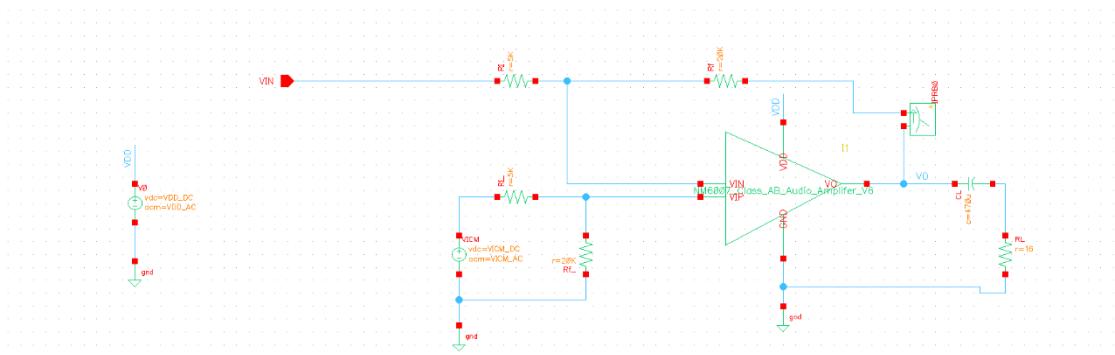


Figure 50 Feed-back Loop Stb Testbench with C_L

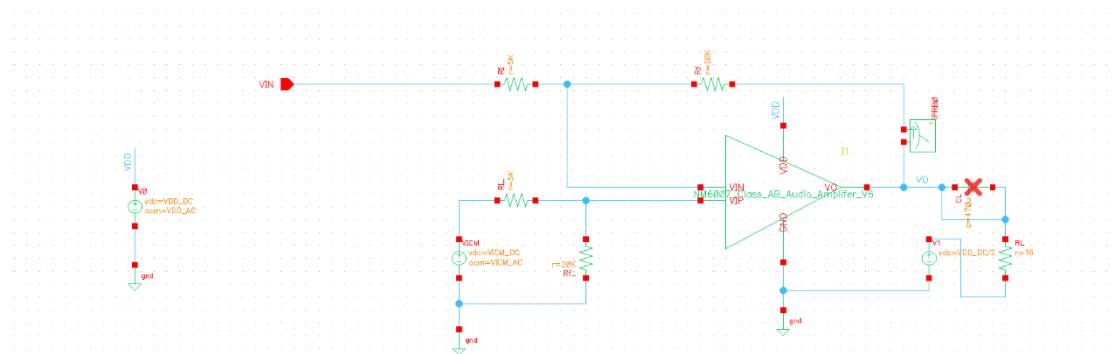


Figure 51 Feed-back Loop Stb Testbench without C_L

NM6007 Assignment: Class-AB Audio Amplifier

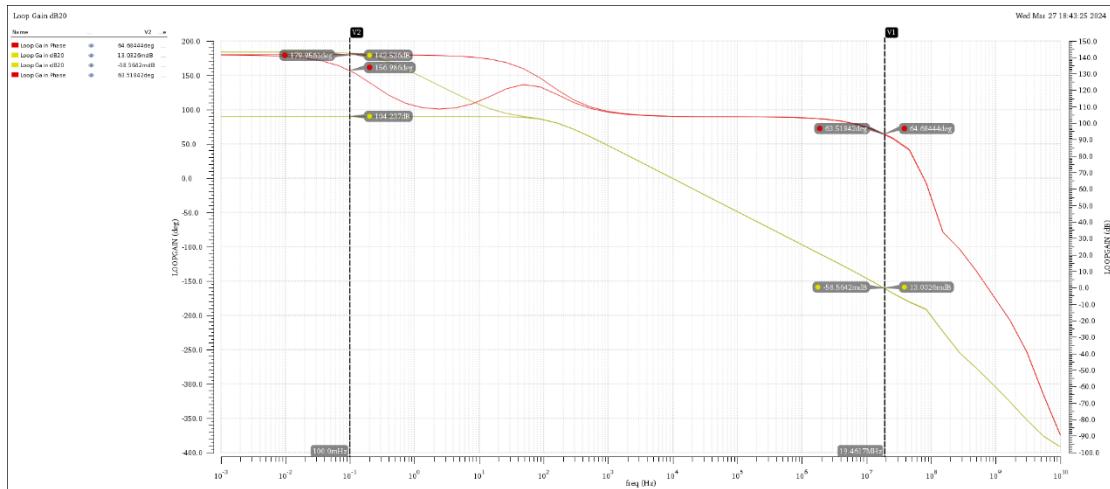


Figure 52 Feed-back Loop Gain and Phase Margin with or without C_L in Pre-simulation

Feed-back loop gain is 104dB without C_L , 142.5dB with C_L (yellow curve). Phase Margin is 64° . It can be observed that the addition of the load capacitance increases the low-frequency gain by 40dB. Additionally, it can be seen that the phase response curve passes through a zero-pole pair at low frequencies, and it overlaps with the curve without the load capacitance after 200Hz. Considering the frequency range of signals handled by the op-amp, the effect of the load capacitance is minimal.

4.5. Power Supply Rejection Ratio

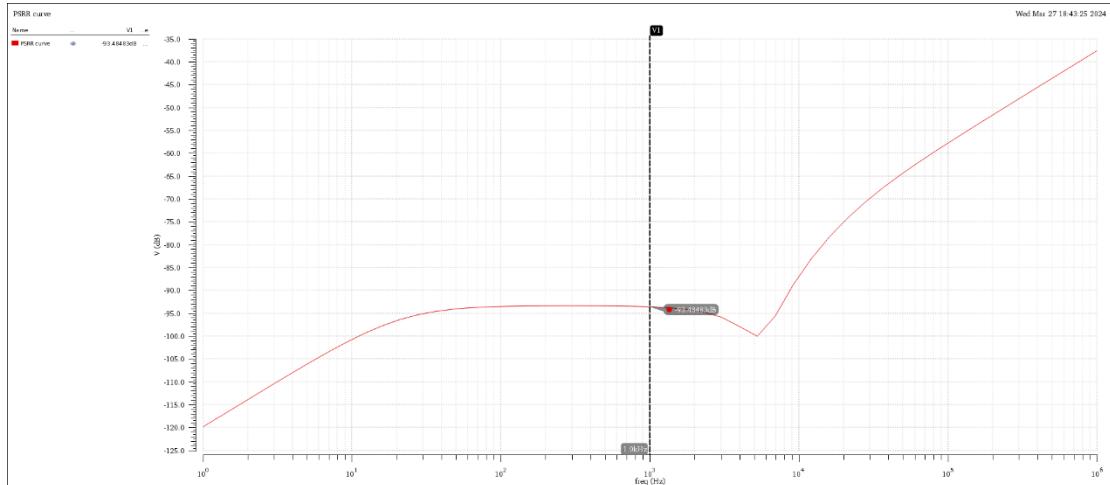


Figure 53 Power Supply Rejection Ratio in Pre-simulation

Power supply rejection ratio is -93.5dB at 1kHz. Since there are usually filtering capacitors on the power supply, the focus is mainly on the low-frequency PSRR.

4.6. Output Swing

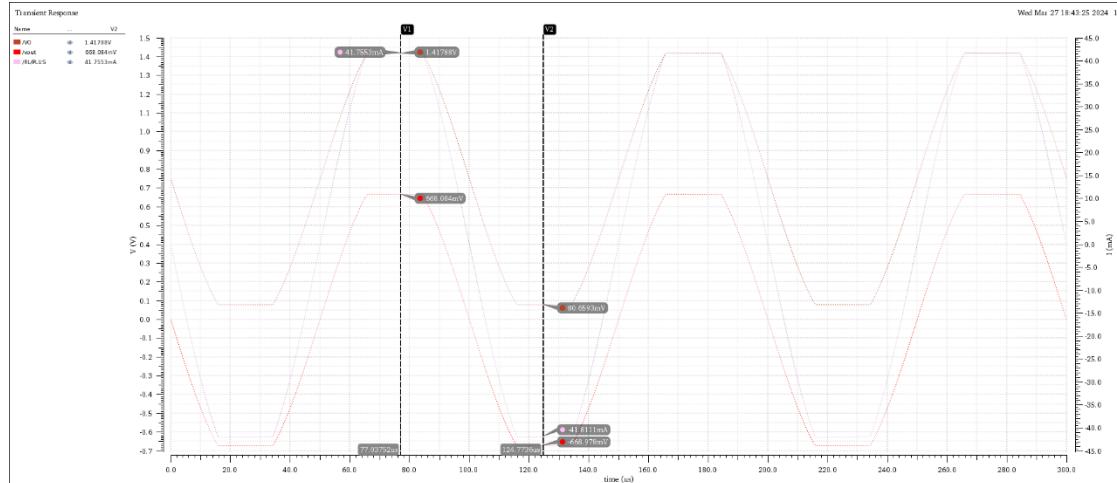


Figure 54 Output Swing in Pre-simulation

Apply a 200mV excitation signal to force the output to exhibit clipping distortion. Test the maximum output voltage swing and the corresponding output current. The output swing with 1.5V VDD is 80.6mV to 1.418V, and the output current is from -41.8mA to 41.75mA.

4.7. Total Harmonic Distortion

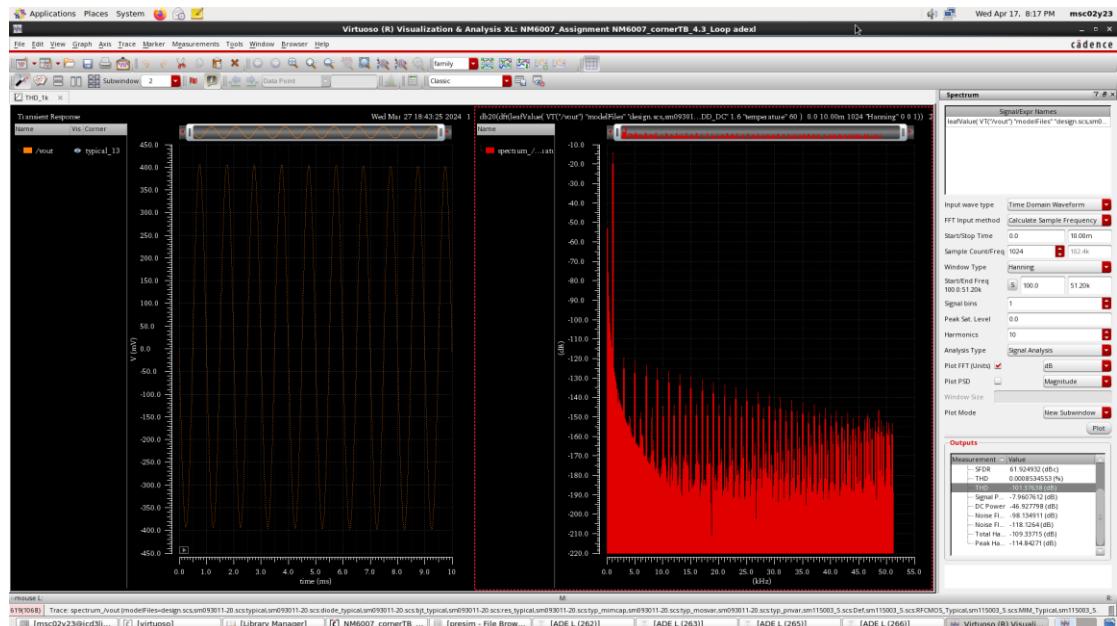


Figure 55 THD 1k in Pre-simulation

THD for 1kHz input using Hanning window is -101.4dB.

NM6007 Assignment: Class-AB Audio Amplifier

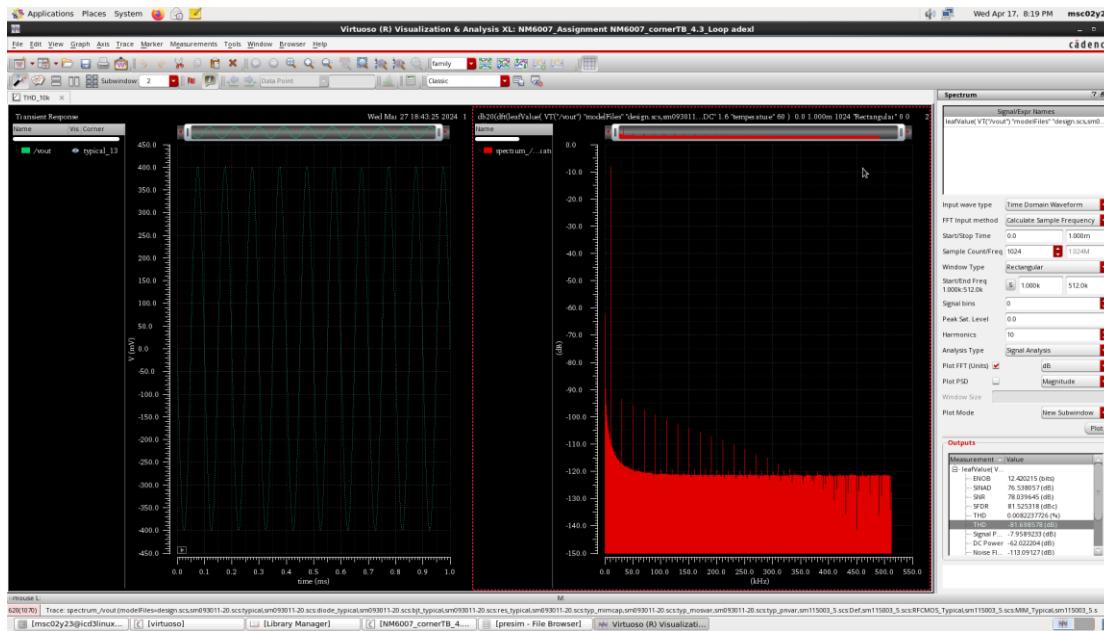


Figure 56 THD 10k in Pre-simulation

THD for 10kHz input using rectangular window is -81.7dB.

4.8. Settling Time

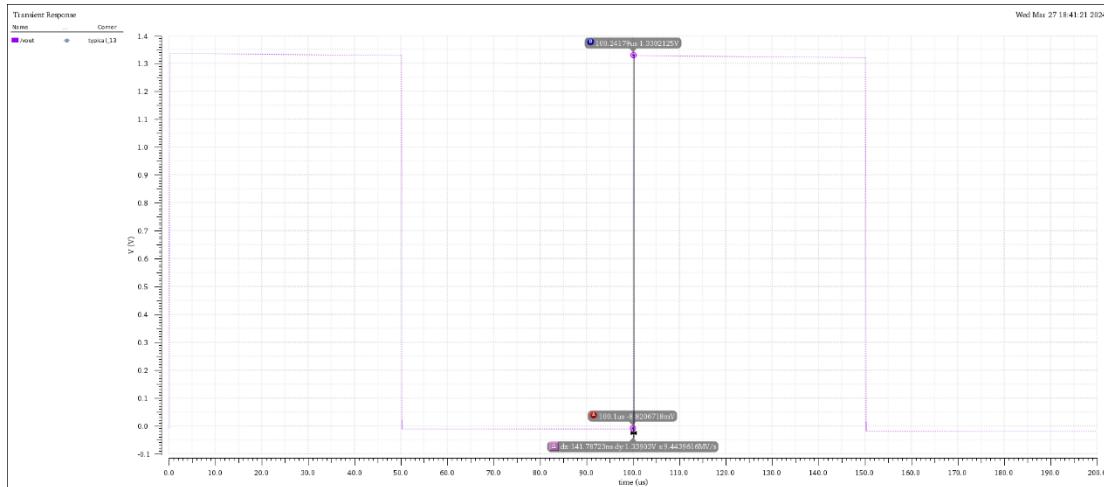


Figure 57 Settling Time for Charging in Pre-simulation

Settling time for charging is 142ns.

NM6007 Assignment: Class-AB Audio Amplifier

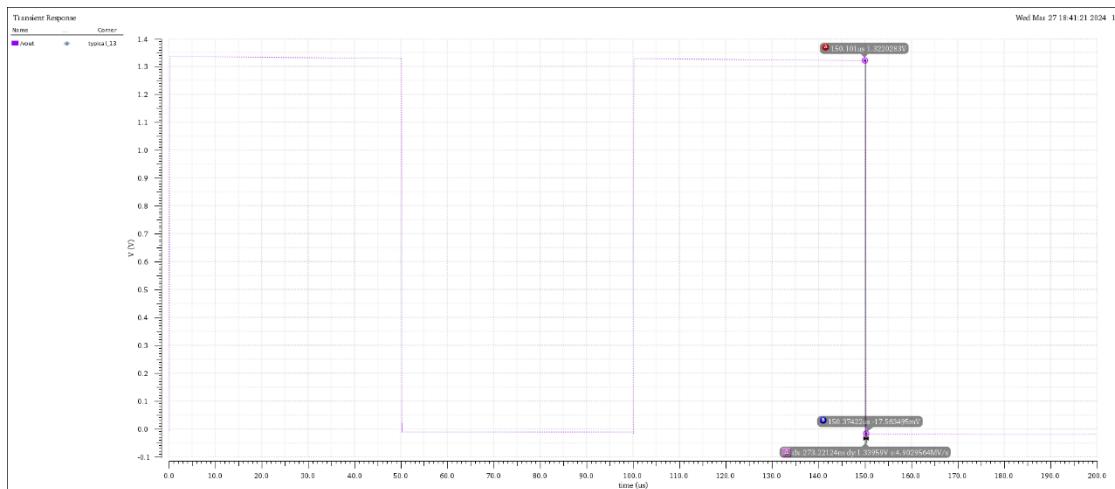


Figure 58 Settling Time for Discharging in Pre-simulation

Settling time for discharging is 273.2ns.

4.9. Slew Rate

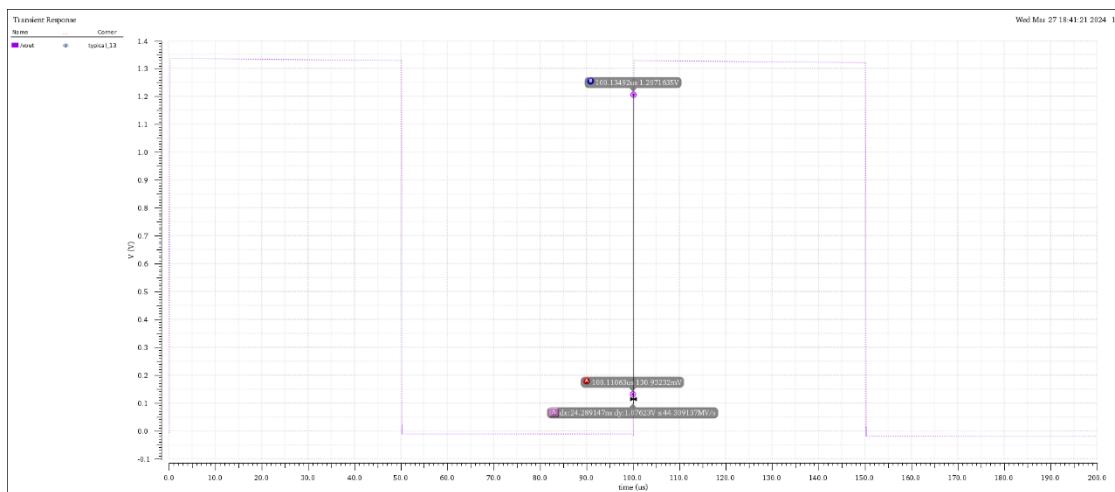


Figure 59 Slew Rate for Charging in Pre-simulation

Slew rate for charging is 44.4 V/ μ s.

NM6007 Assignment: Class-AB Audio Amplifier

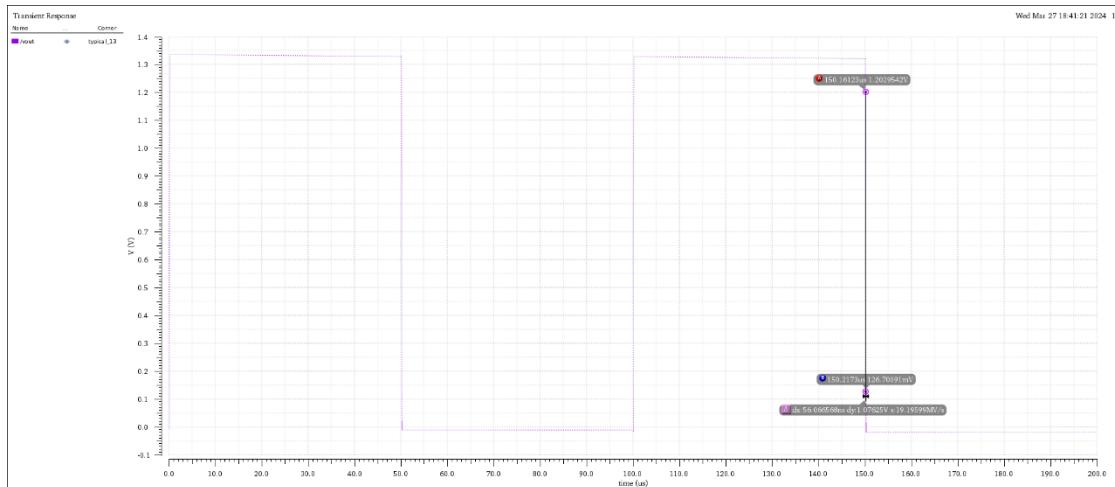


Figure 60 Slew Rate for Discharging in Pre-simulation

Slew rate for discharging is $19.2 \text{ V}/\mu\text{s}$.

4.10. First Stage Gain

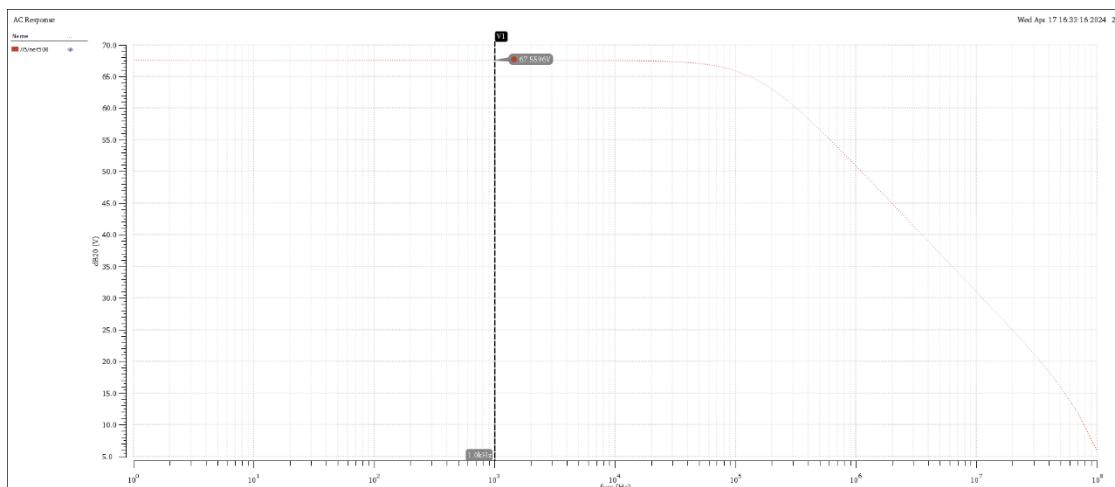


Figure 61 First Stage Gain in Pre-simulation

The first stage has a gain of 67dB. The gain of the first stage is measured in open loop. Meanwhile, attempts were made to measure the gain of the second stage, but since the second and third stages are merged together and the output node potential is determined by negative feedback, thereby determining the DC operating point of the preceding stage, it's not possible to measure the gain of the second stage independently in open loop. Instead, it can only be inferred from the loop gain measured through stability analysis and the open-loop gain of the first stage. In the future, it's advisable to research appropriate simulation methods for this purpose.

4.11. Equivalent Input Noise

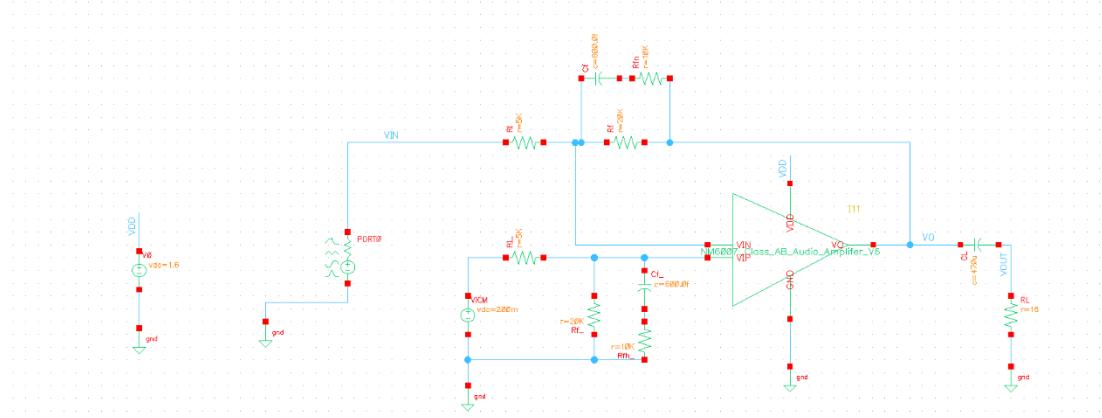


Figure 62 Noise Testbench

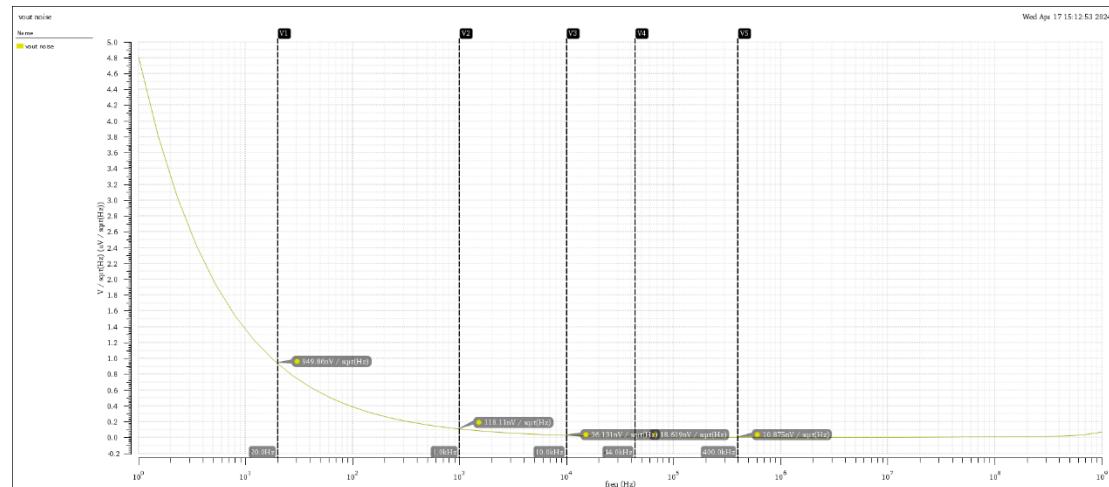


Figure 63 Equivalent Input Noise in Pre-simulation

Attempts were made to measure the equivalent input noise of the operational amplifier. However, the transition frequency of flicker noise falls within the operational amplifier's operating frequency range, and there is no filtering observed for high-frequency thermal noise. This could be related to the failure of the RC series network that limits the bandwidth.

NM6007 Assignment: Class-AB Audio Amplifier

Swing_0	Swing_1	Swing_2	Swing_3	Swing_4	Swing_5	Swing_6	Swing_7
typical							
1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
-40	20	0	20	40	60	80	100
Swing_0	Swing_1	Swing_2	Swing_3	Swing_4	Swing_5	Swing_6	Swing_7
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
disabled							
1.437	1.433	1.429	1.426	1.422	1.418	1.414	1.41
57.29m	62m	66.68m	71.34m	75.98m	80.61m	85.25m	89.95m
-48.2m	-42.91m	-42.62m	-42.34m	-42.06m	-41.78m	-41.52m	-41.26m
-43.01m	42.77m	42.54m	42.3m	42.05m	41.79m	41.51m	41.22m

Figure 65 Swing for Temperature Variation in Pre-simulation

5. Layout Design

5.1. First Version

5.1.1. Full Layout Overview of First Version

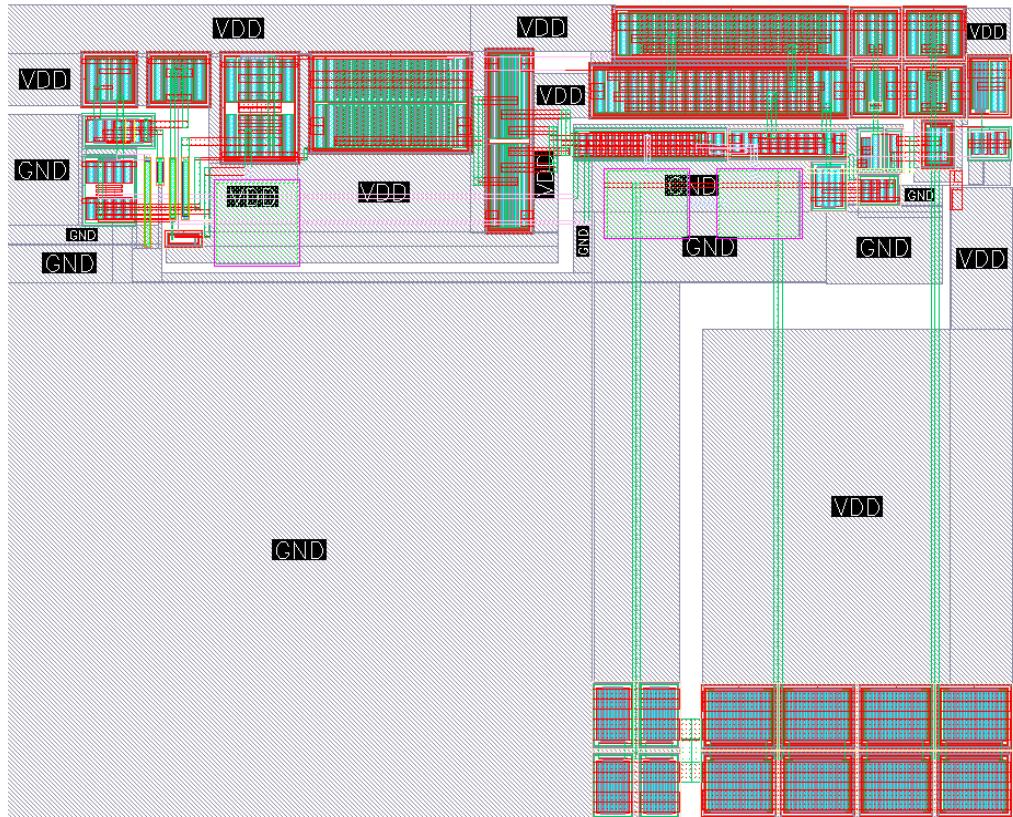


Figure 66 First Layout Version

In the first version of the layout, I placed the bias circuit in the upper left corner, the operational amplifier in the upper right corner, the input transistors in between them, and the output transistors in the lower right corner. The empty spaces were filled with metal for power and ground routing. Due to limited horizontal space, I couldn't align the input and output transistors, causing the asymmetric heat dissipation from the output transistors to affect the input transistors. The layout area is less than $250 \times 200 \mu\text{m}^2$ and has a significant margin, indicating the possibility of sacrificing area to improve other performance parameters.

5.1.2. Bias in First Layout Version

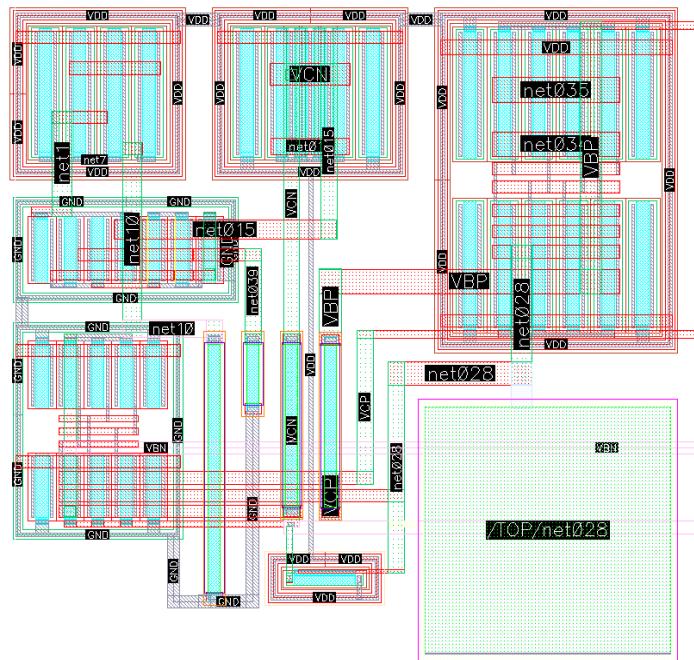


Figure 67 Bias in First Layout Version

I attempted to unify the gate orientation and placed resistors together, albeit at the cost of more complex wiring. MOS transistors sharing the same drain were merged together, and dummy transistors were added on both sides. Finally, four voltage outputs were extracted using high-level metal, as there is no current flowing through the gate. Therefore, the width of these four metal lines should be narrower than the other connections.

5.1.3. Amp in First Layout Version

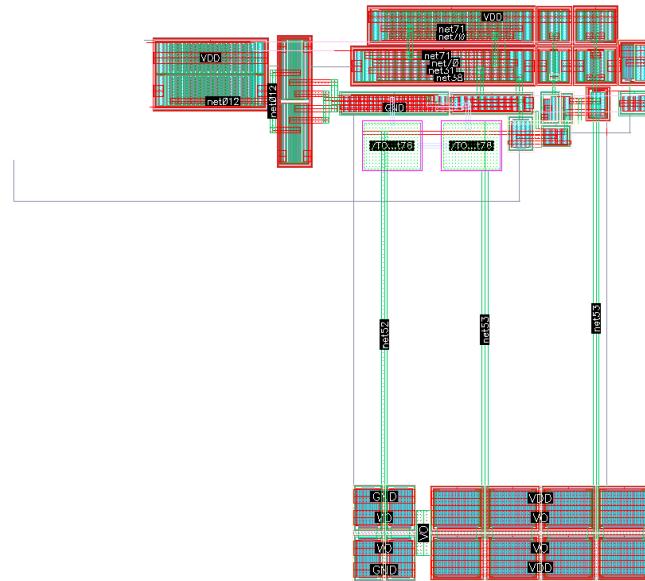


Figure 68 Amp in First Layout Version

In the operational amplifier, to minimize the use of interconnects and vias, I arranged the transistors as compactly as possible and used metal lines crossing over the gate. However, post-simulations demonstrated significant interference with the circuit's performance. The crosstalk from signals on the bottom metal lines to the gate cannot be ignored.

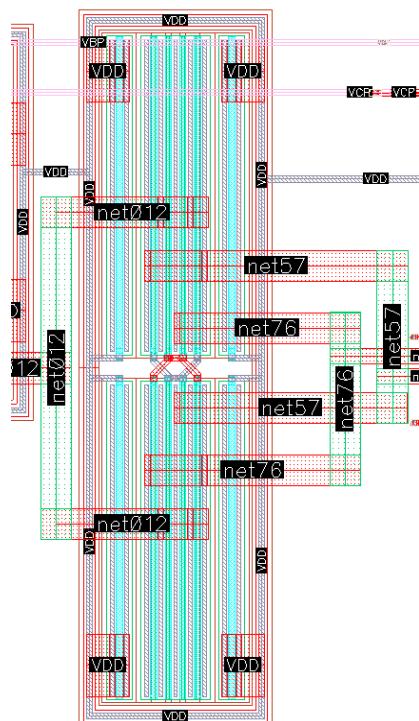


Figure 69 Input Pair in First Layout Version

I used a cross-coupled input gate, common-centroid differential pair, and dummy transistors to ensure the matching of the differential pairs as much as possible. However, it seems that the input transistors are a bit too wide.

5.2. Second Version

5.2.1. Full Layout Overview of Second Version



Figure 70 Second Layout Version

In the second version of the design, I used dedicated power and ground lines and optimized the connections between the bias and amplifier sections, allowing the four bias voltages to follow straight paths without bends. However, they still appear to be a bit too long, which could result in significant parasitic resistance and capacitance. The issue of thermal gradients from the output transistors affecting the input differential pair remains unresolved. The layout area is still less than $250 \times 200 \mu\text{m}^2$ and has a significant margin, indicating the possibility of sacrificing area to improve other performance parameters.

5.2.2. Bias in Second Layout Version

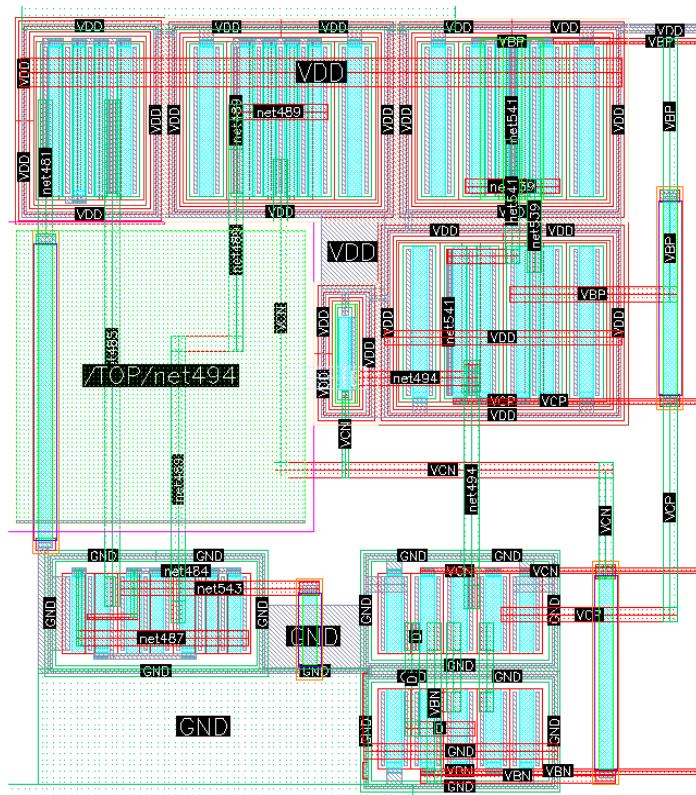


Figure 71 Bias in Second Layout Version

In the second version, to reduce parasitics on the interconnects, I dispersed the resistors to minimize the length of the traces, bends, and vias. However, in actual production, resistor mismatch may occur, leading to less precise resistance values. I also adjusted the orientation of the gates of the transistors to have a unified direction for all gates.

5.2.3. Amp in Second Layout Version

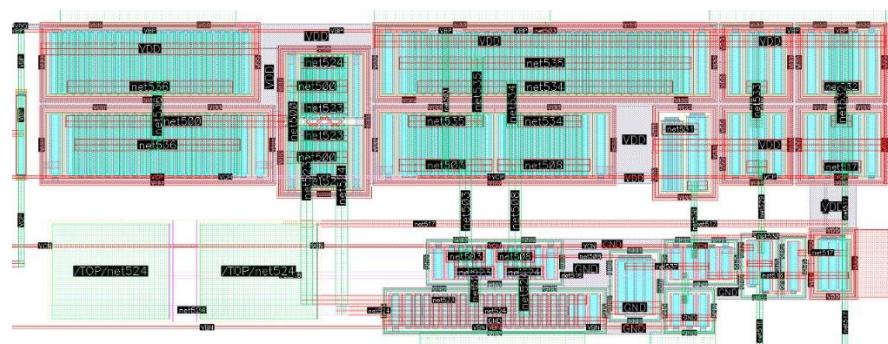


Figure 72 Amp in Second Layout Version

I optimized the layout of the operational amplifier, making the arrangement of the transistors more orderly. The gates of all transistors that require bias voltage are aligned on the same horizontal line.

5.2.4. Input Pair in Second Layout Version

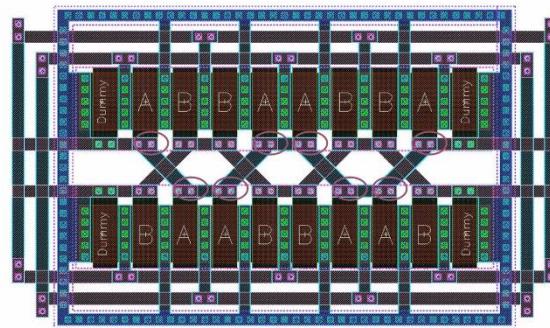


Figure 73 Common Centroid Symmetry Interdigitation Input Pair Reference

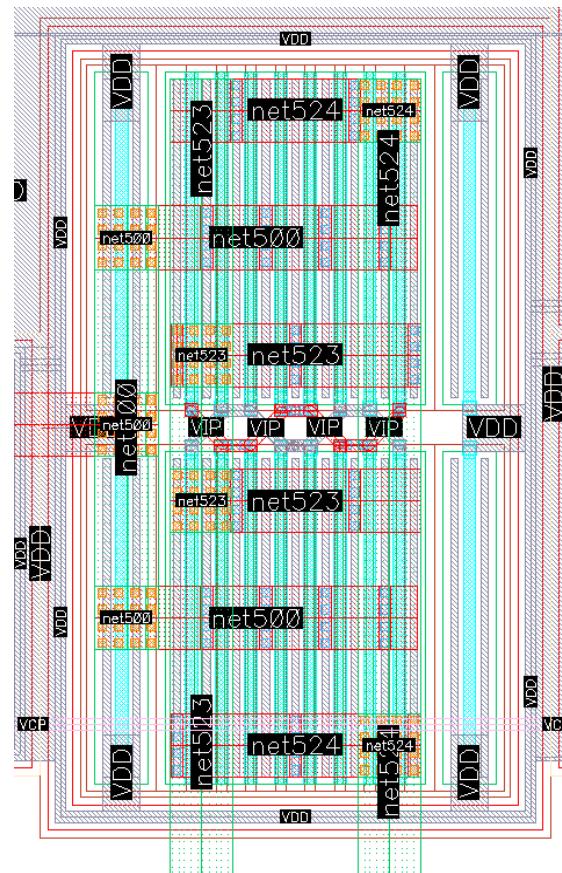


Figure 74 Input Pair in Second Layout Version

I increased the number of multipliers, making the layout of the input transistors more like a square. All the routing was also kept as symmetrical as possible.

5.2.5. Other Parts in Second Layout Version

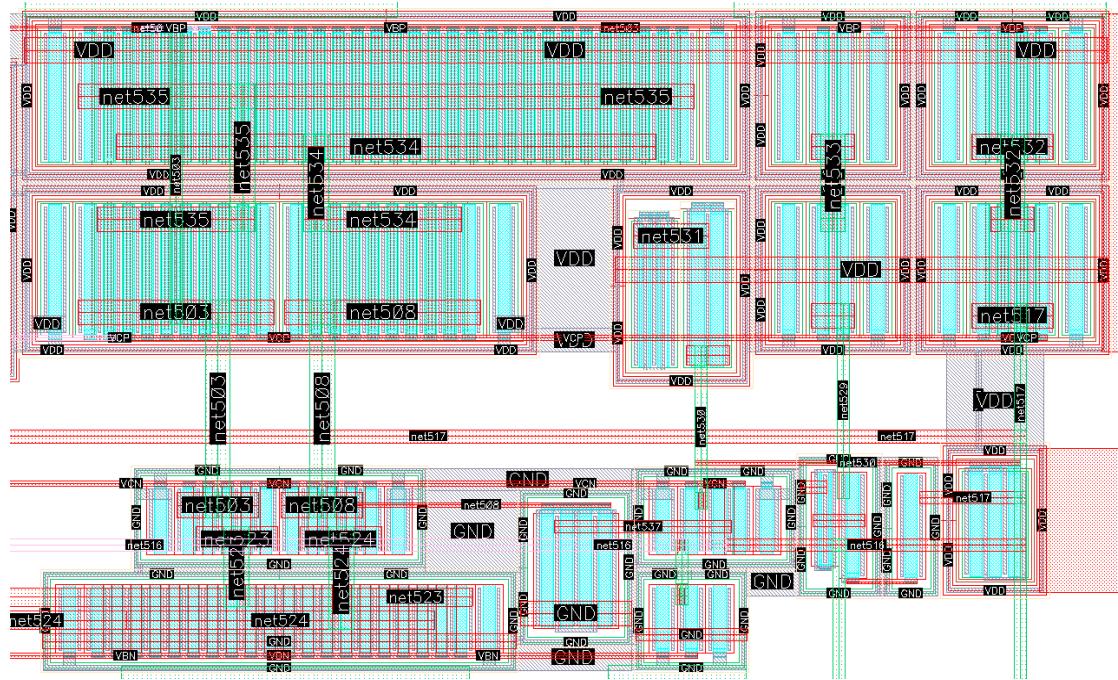


Figure 75 Other Parts in Second Layout Version

I ensured uniformity in wire widths and minimized the length of routing. However, the metal lines crossing over the gates caused crosstalk, and the distance between PMOS and NMOS was too far, wasting area and increasing the routing distance. Additionally, there were too many transistors in the guard ring, resulting in significant body effect, which needs improvement in future iterations.

5.2.6. Output Transistors in Second Layout Version

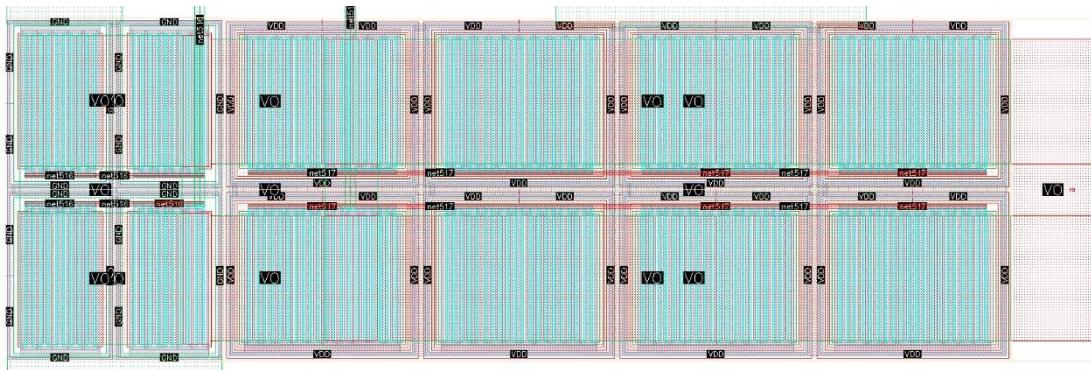


Figure 76 Output Transistors in Second Layout Version

I've attempted to use multipliers and fingers to cut the output transistors into squares as much as possible, but the size of this square is still somewhat large. I should continue to use guard rings to further divide it.

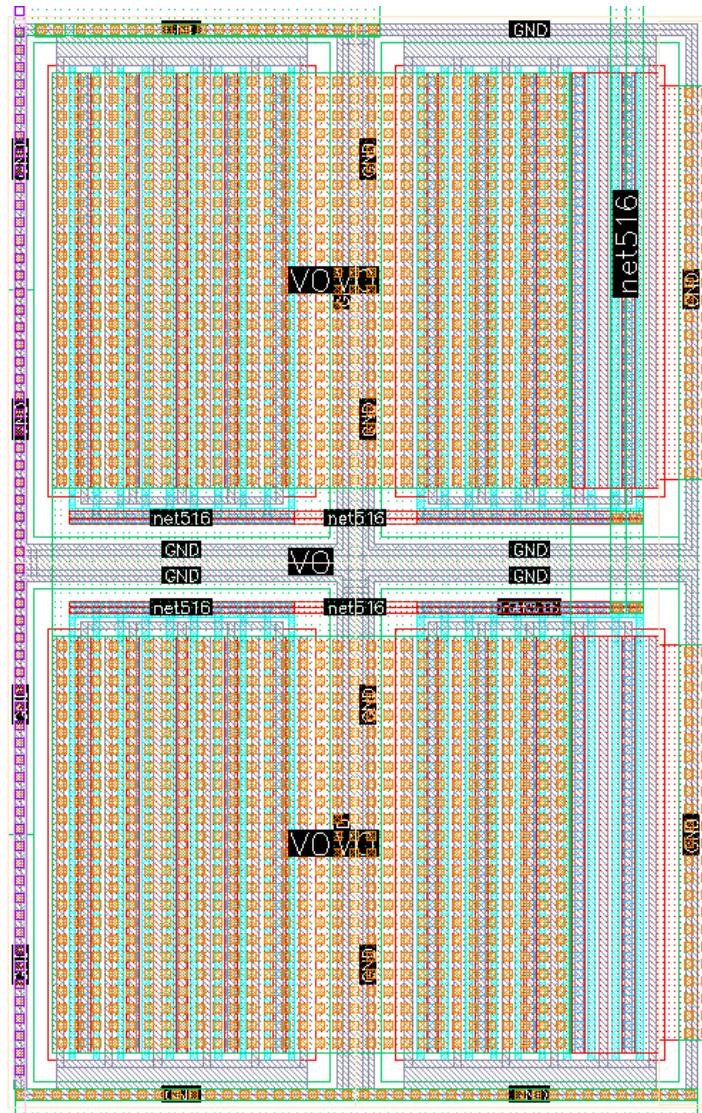


Figure 77 Output Transistors Structure in Second Layout Version

I've tried to maintain symmetry in the structure as much as possible, but due to the fact that the gates are only connected from one end, there is considerable parasitic resistance, which affects the swing in the post-simulation. In the future, I could try bringing out and connecting the gates from both ends, and reducing the number of MOS transistors in each guard ring.

6. Post-simulation

Display the typical post-simulation results at 1.6V using the extracted parasitic parameter netlist at 60 degrees Celsius.

6.1. Power Consumption

typical_0	typical_1	typical_2	typical_3	typical_4	typical_5	typical_6	typical_7	typical_8	typical_9	typical_10	typical_11
typical											
1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.6	1.6	1.6	1.6
-40	-20	0	20	40	60	80	100	-40	-20	0	20
typical_0	typical_1	typical_2	typical_3	typical_4	typical_5	typical_6	typical_7	typical_8	typical_9	typical_10	typical_11
747.1u	850.6u	962.4u	1.083m	1.212m	1.349m	1.492m	1.639m	814.9u	924.4u	1.043m	1.17m
typical_12	typical_13	typical_14	typical_15	typical_16	typical_17	typical_18	typical_19	typical_20	typical_21	typical_22	typical_23
typical											
1.6	1.6	1.6	1.6	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
40	60	80	100	-40	-20	0	20	40	60	80	100
typical_24	typical_13	typical_14	typical_15	typical_16	typical_17	typical_18	typical_19	typical_20	typical_21	typical_22	typical_23
1.307m	1.452m	1.604m	1.762m	944u	1.066m	1.197m	1.339m	1.489m	1.649m	1.817m	1.992m

Figure 78 DC Current in Post-simulation

DC current is less than that in pre-simulation with maximum 1.992mA.

6.2. Closed-Loop Gain and Closed Loop Unity Gain Bandwidth

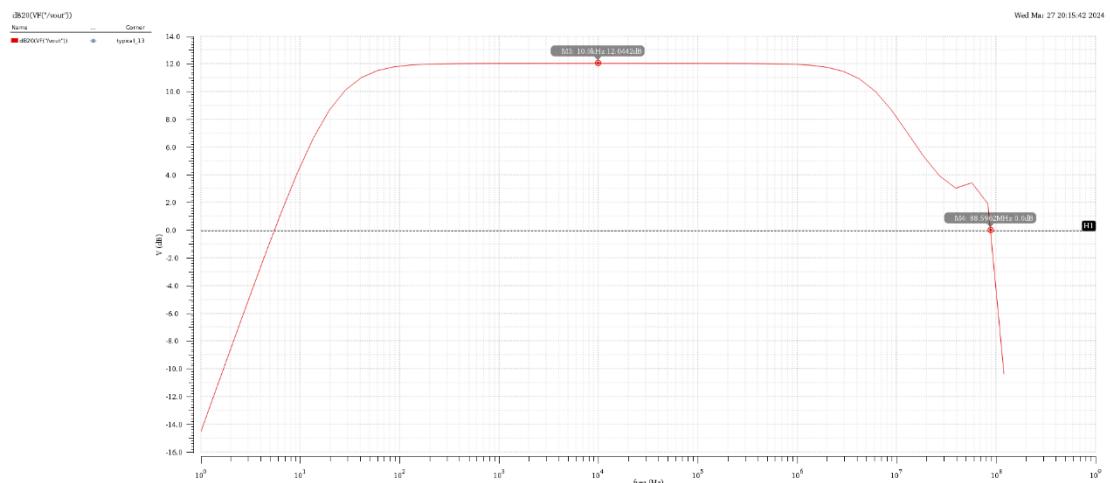


Figure 79 Closed-Loop Gain and Closed Loop Unity Gain Bandwidth in Post-simulation

Closed loop gain is still 12.04dB while the closed unity gain bandwidth drops to 88.6MHz compared to 91.6MHz in pre-simulation.

6.3. Common-mode Gain

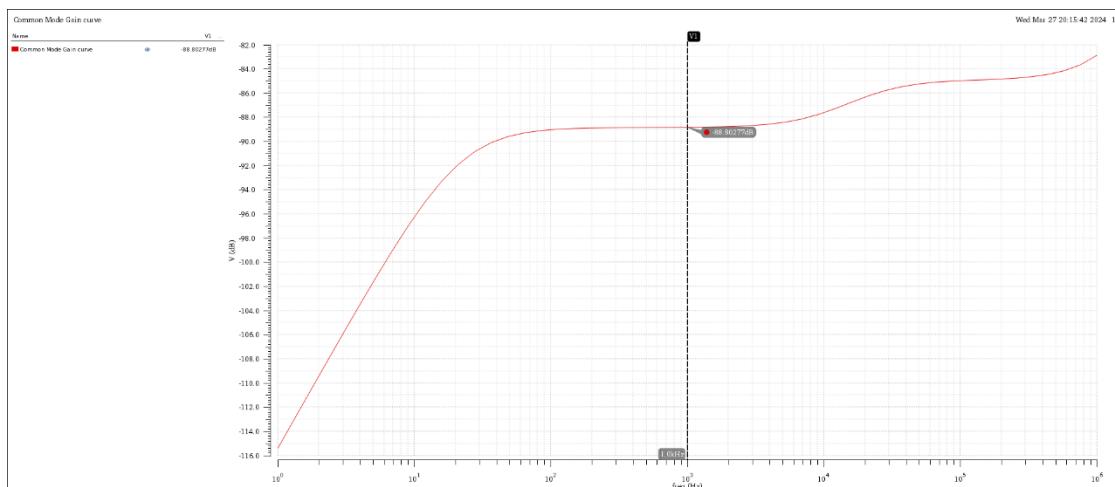


Figure 80 Common-mode Gain in Post-simulation

Common-mode gain is -88.8dB at 1kHz compared to -88.96189dB in pre-simulation, indicating that the differential pair is functioning properly.

6.4. Feed-back Loop Gain and Phase Margin

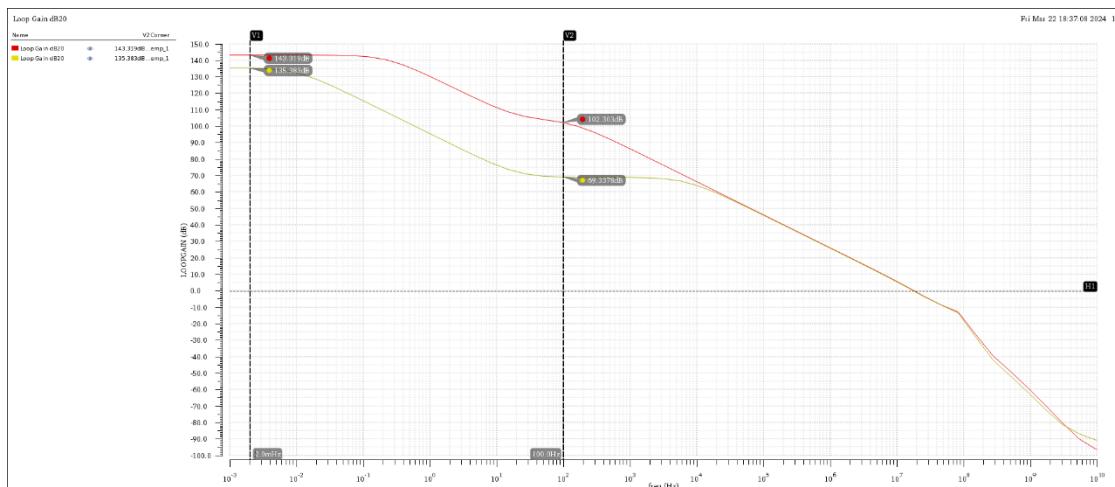


Figure 81 FB Loop Gain Difference between Pre and Post with C_L

NM6007 Assignment: Class-AB Audio Amplifier

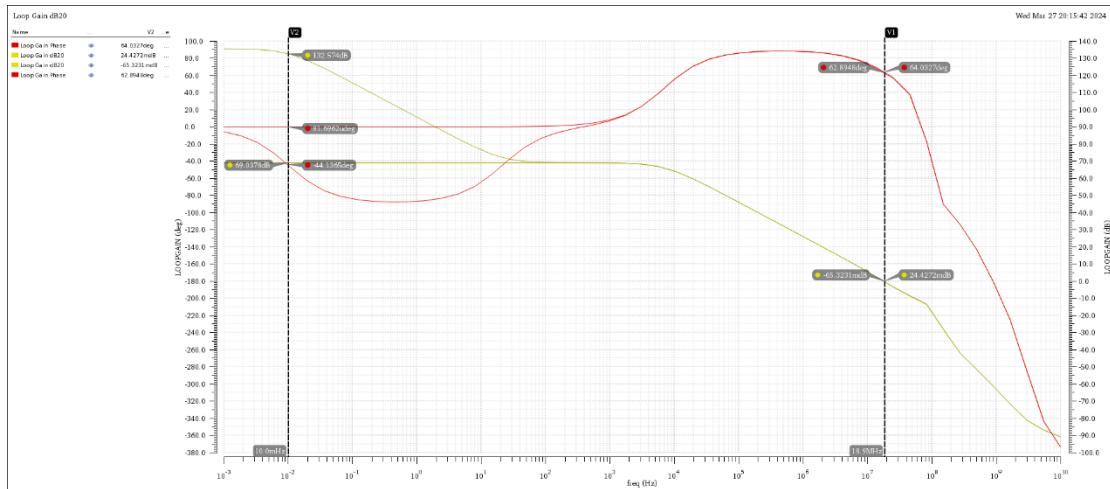


Figure 82 Feed-back Loop Gain and Phase Margin with or without C_L in Post-simulation

It can be observed that in the post-simulation, if there is no "fake gain" caused by the load capacitance (yellow curves), or a lower frequency point is not chosen as the dc gain, the loop gain cannot meet the specifications. which means the transistors in the gain stage are likely not saturated. The reason for non-saturation may be the influence of parasitic parameters in the layout, such as too many transistors in the guard ring, internal transistors not being turned on, indirectly reducing the aspect ratio of the devices, resulting in a need for a larger V_{dsat} to achieve saturation.

From the phase-frequency curve, it can be seen that the starting point of the phase changes, resulting in inconsistency with the pre-simulation phase-frequency response curve. However, the phase margin still meets the specifications. There is a suspicion that the stability in the post-simulation might not be functioning properly. Attempting to use large inductance and capacitance to cut off the feedback loop for testing.

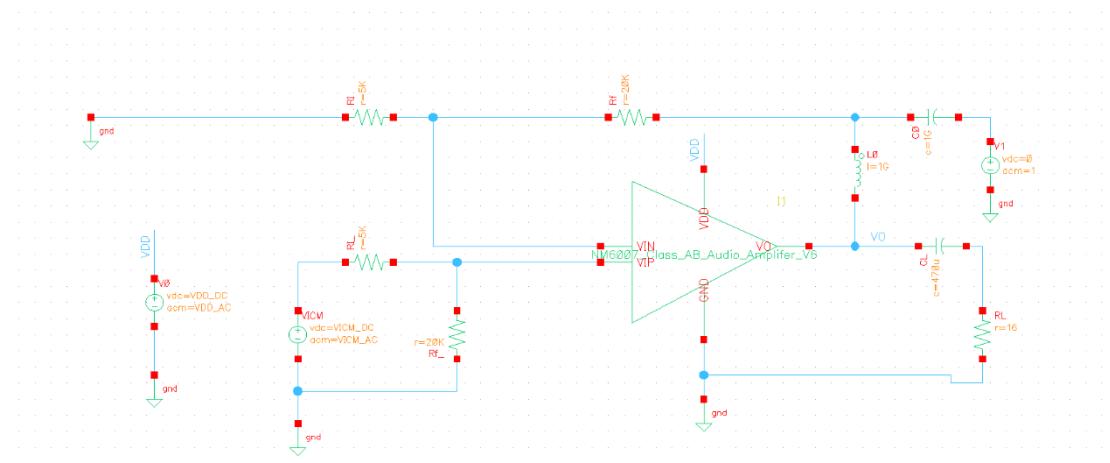


Figure 83 Feed-back Loop LC Testbench with C_L

NM6007 Assignment: Class-AB Audio Amplifier

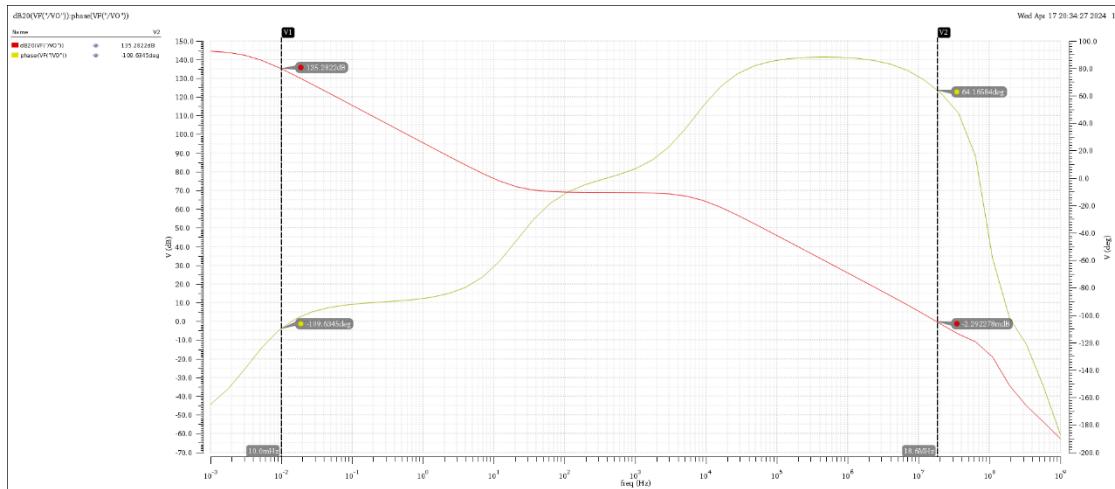


Figure 84 Feed-back Loop LC Test Result in Post-simulation

Despite replacing the test circuit, the phase still did not return to normal.

6.5. Power Supply Rejection Ratio

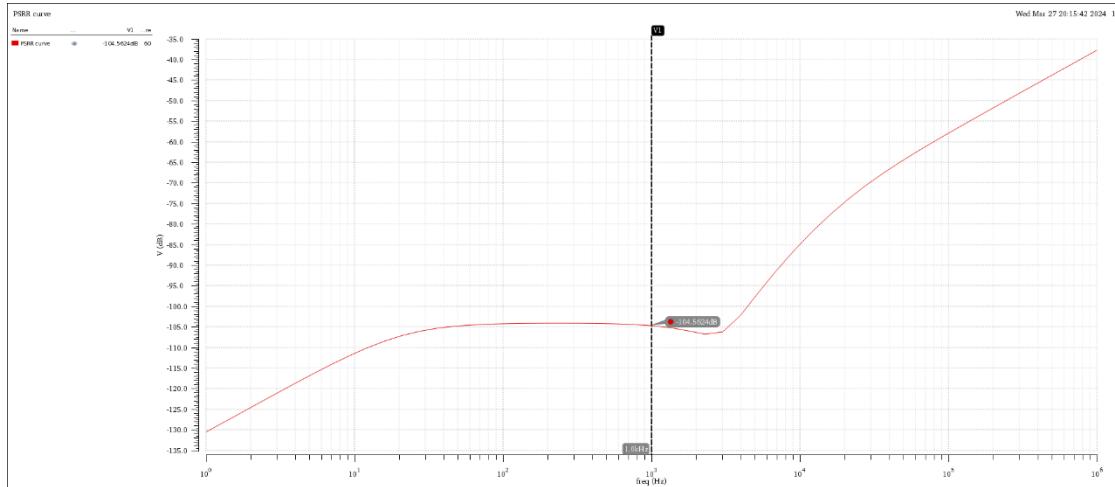


Figure 85 Power Supply Rejection Ratio in Post-simulation

The power supply rejection ratio in the post-simulation is -104.5dB in 1kHz, which is even better than the -93.5dB in the pre-simulation. Interesting.

6.6. Output Swing

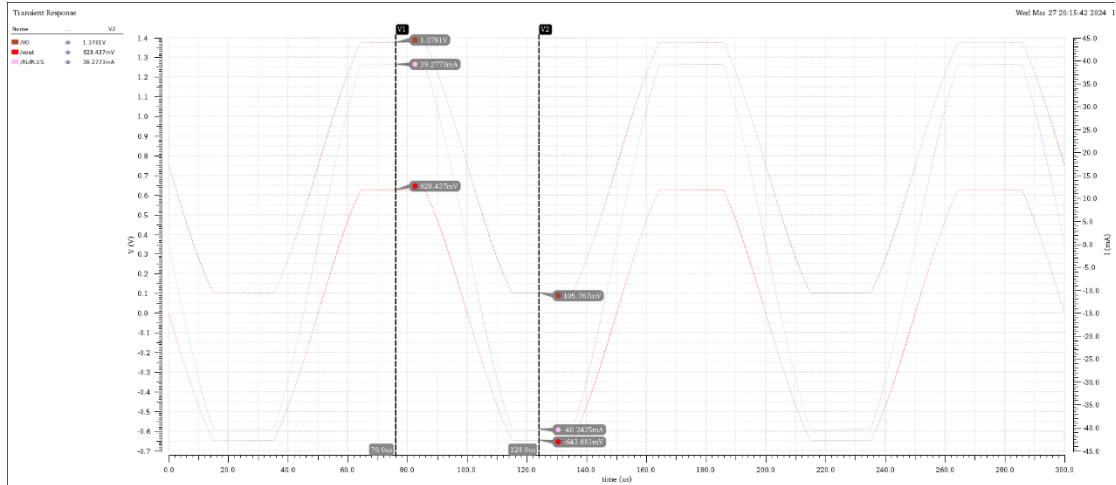


Figure 86 Output Swing in Post-simulation

The output swing with $1.5V$ V_{DD} is $105.8mV$ to $1.378V$ compared to $80.6mV$ to $1.418V$ in pre-simulation, and the output current is from $-40.24mA$ to $39.27mA$ compared to $-41.8mA$ to $41.75mA$.

6.7. Total Harmonic Distortion

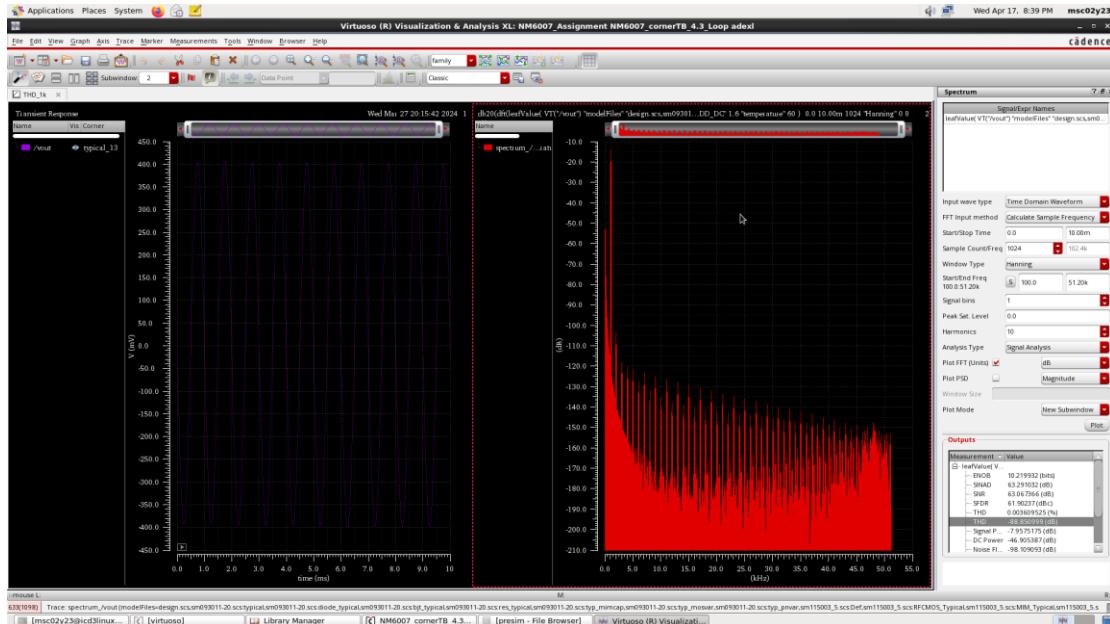


Figure 87 THD 1k in Post-simulation

NM6007 Assignment: Class-AB Audio Amplifier

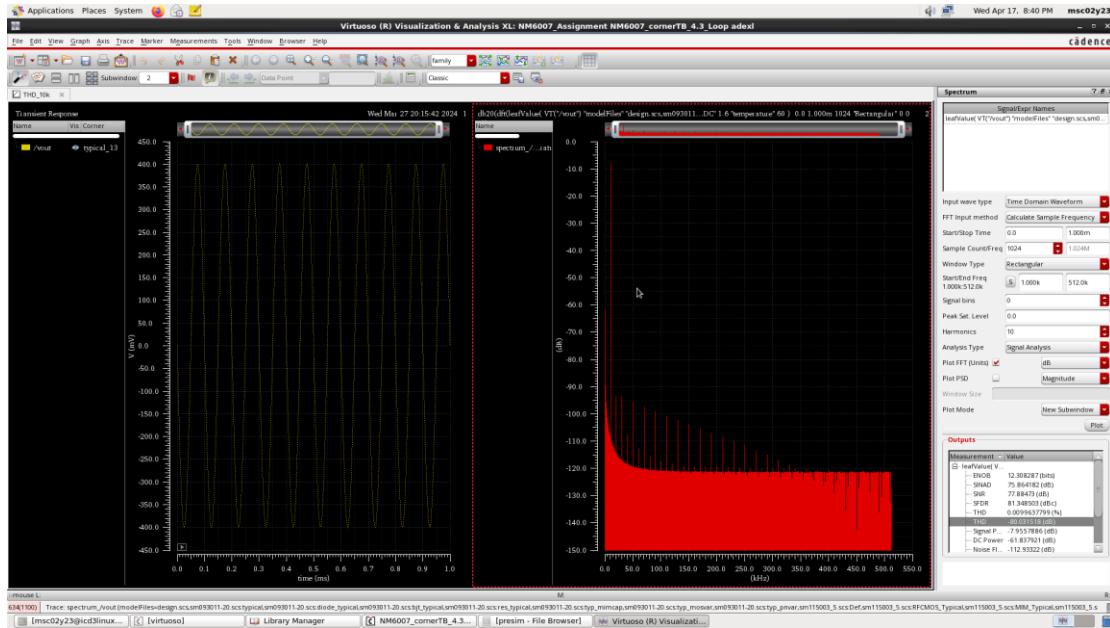


Figure 88 THD 10k in Post-simulation

THD is -88.85dB for 1kHz input and -80.03dB for 10kHz input, compared to -101.4dB and -81.7dB in pre-simulation. Performance has degraded but still meets the requirements.

6.8. Settling Time

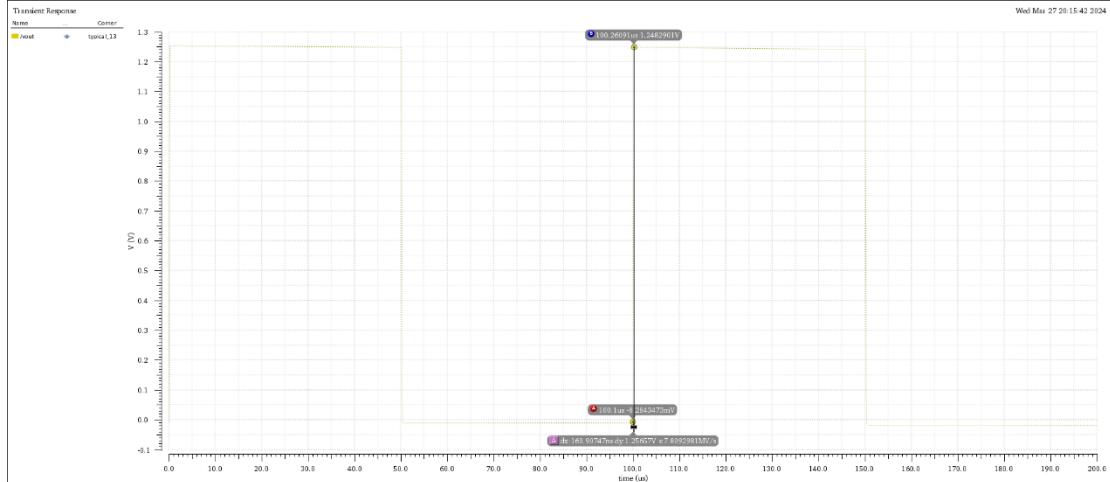


Figure 89 Settling Time for Charging in Post-simulation

Settling time for charging in post-simulation is 161ns.

However, there are still unclear aspects in the image. Within one period, the voltage continuously decreases after charging to its maximum. Comparing multiple periods, it

NM6007 Assignment: Class-AB Audio Amplifier

can also be seen that the maximum voltage is continuously decreasing. Moreover, the maximum voltage in the post-simulation is 1.24V, which has already decreased by 0.1V compared to the 1.33V in the pre-simulation. At this point, the simulation results should not be due to capacitor leakage. It's unclear why this circuit never stabilizes when a square wave input is applied.



Figure 90 Settling Time for Discharging in Post-simulation

Settling time for dis-charging in post-simulation is 299ns.

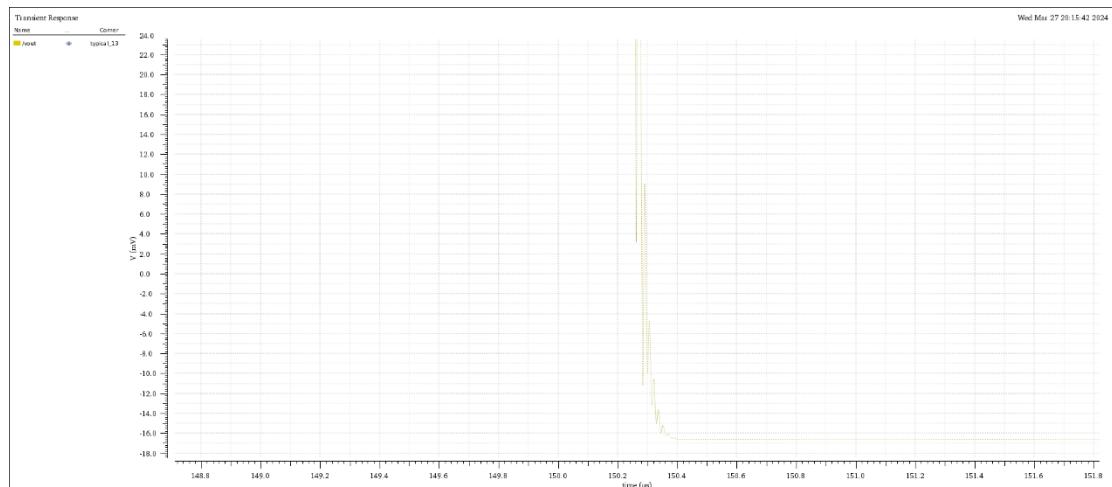


Figure 91 Unusual Response Occurring during the Discharging Process

From the image, it can be seen that the signal starts oscillating before it reaches the lowest point, which is completely different from the ringing phenomenon of overshoot and undershoot commonly seen in step responses. The reason for this phenomenon is currently unknown.

6.9. Slew Rate

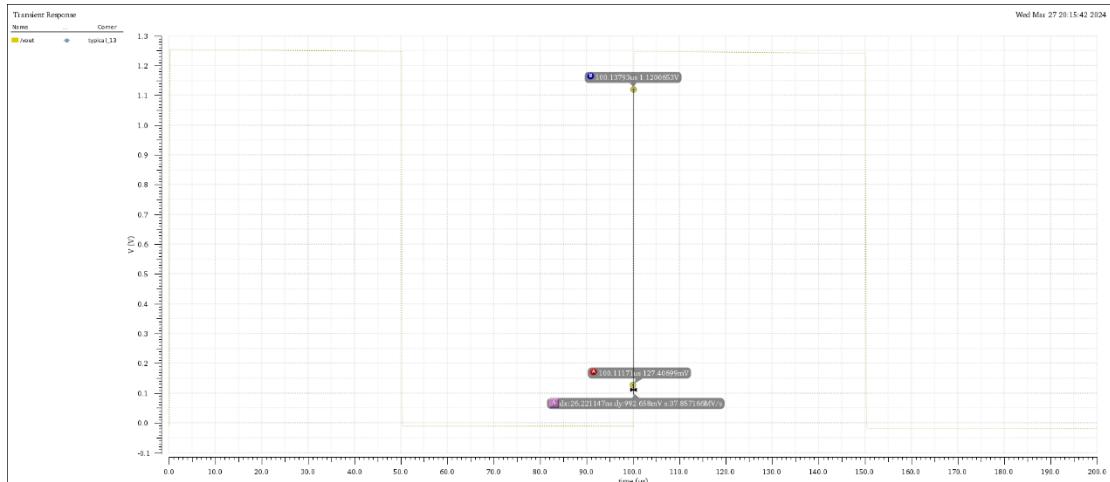


Figure 92 Slew Rate for Charging in Post-simulation

Slew rate for charging in post-simulation is $37.8 \text{ V/}\mu\text{s}$ compared to $44.4 \text{ V/}\mu\text{s}$ in pre-simulation. The decrease in slew rate may be due to the introduction of parasitic capacitances in the layout, which slow down the charging speed of the tail current source.



Figure 93 Slew Rate for Discharging in Post-simulation

Slew rate for discharging in post-simulation is $13.3 \text{ V/}\mu\text{s}$ compared to $19.2 \text{ V/}\mu\text{s}$ in post-simulation.

7. Don't-s and Do-s

7.1. Don't-s

1. When simulating operational amplifiers, open-loop simulation is rarely necessary. Operational amplifiers that require negative feedback to maintain a static operating point become comparators once open-looped, which is meaningless for this application.
2. In layout design, try not to use lower layer metals to cross over gate regions, as this will create significant parasitic capacitance and crosstalk. Comparatively, the parasitics from making the wiring more complex or using more vias are acceptable.
3. Do not overpopulate the guard ring with devices to prevent voltage drops due to substrate resistance or well resistance, which could cause the body effect.
4. The distance between NMOS and PMOS can be reduced. The resulting parasitic capacitance from VDD and GND is harmless, and might even help filter out power noise. Guard rings can also be merged together, provided they completely overlap, otherwise, DRC will flag an error.

7.2. Do-s

1. One needs to learn how to handle oscillations after they occur, try to find the charging and discharging loop corresponding to the oscillation frequency. And learn how to deal with convergence issues of simulator.
2. Practice analyzing and calculating small-signal models, like the output impedance of a Dobkin current source. Complete the exercises a of Razavi's book.
3. Practice calculating device dimensions based on specifications rather than being a spice monkey, one must at least understand why adjustments are made in this direction, including the calculation of compensation capacitor sizes in bias and amp, the calculation of the complex loop gain, the calculation of the width-to-length ratio of the input transistor from spec.
4. Practice analyzing and deriving the zeros and poles of a system from system block diagrams or signal flow graphs, differentiate various bandwidths like 3dB and GBW, open-loop frequency response, closed-loop frequency response, and loop frequency response and so on, and study Principle of Automatic Control to deepen the understanding of feedback, zeros and poles, as well as concepts like root locus, damping coefficient, and other related topics.

5. Deepen understanding of the correspondence and physical meanings between time domain, frequency domain, s-domain, and z-domain, and review signals and systems and digital signal processing.
6. Deepen understanding of small signals and large signals, large-signal response and small-signal response such as the state of other devices and internal signals when the output device reaches the swing limit. Practice determining the DC operating point by crossing I-V characteristic curves of different devices on the same branch.
7. Practice designing with the gm/I_d methodology.
8. Practice using EDA software, learn simulation methods for some circuit parameters, learn to set up environments and batch process scripts, thereby simplifying operations and improving efficiency.
9. Accumulate the advantages and value of actual metrics corresponding to different circuit topologies, and learn how to reasonably allocate current.
10. In layout, the line width should be determined based on the current density and parameters provided by the process library. Increasing line width reduces resistance but increases capacitance, and the impact on RC delay needs to be considered.
11. Further learning of overall layout and routing techniques is necessary, including the general parameters of the process library used and the specific impact of the layout on post-simulation.
12. Adapt to the logarithmic calculation method in dB units, but also have an approximate estimate of the corresponding linear values.

NM6007 Assignment: Class-AB Audio Amplifier

NM6007 Assignment: Class-AB Audio Amplifier

Personal Score Sheet

Name: Bian Wenzuan

Date: _____

Specification		Signature
12dB Closed Loop Gain	12.04	<u>J</u>
$\geq 200\text{kHz}$ Closed Loop Unity Gain Bandwidth	Max: 122.6M, typ. 1.8.82 Min: 31.93M, typ. 1.5.40	<u>A</u>
≤ -73 Common-mode Gain	Max: -80.35, typ. 1.8.60 Min: -108.5, typ. 1.5.40	<u>J</u>
$\geq 75\text{dB}$ Feedback Loop Gain	Max: 147.7, typ. 1.8.100 Min: 140.2, typ. 1.5.40	<u>J</u>
≥ 60 Feedback Loop Phase Margin	Max: 71.66, typ. 1.5.40 Min: 57.88, typ. 1.8.60	<u>A</u>
≤ -65 Power Supply Rejection Ratio	Max: -69.28, typ. 1.8.100 Min: -104, typ. 1.6.60	<u>J</u>
$\leq 2\text{mA}$ Current Consumption	Max: 1.992mA, typ. 1.8.100 Min: 1.472mA, typ. 1.5.40	<u>A</u>
≤ 77 Total Harmonic Distortion	Max: -76.97, fs, 1.6.60 Min: -80.93, typ. 1.8.40	<u>J</u>
$\leq 0.5\mu\text{s}$ Settling Time	F _s = 88.7054 ns F _r = 187.17 ns	<u>J</u>
$\geq 4\text{V/us}$ Slew Rate	F _s = 36.98 V/us F _r = 13.57 V/us	<u>J</u>
$\leq 250 \times 200 \mu\text{m}^2$ Chip Area	190.15 x 250 μm^2	<u>J</u>

Please scan a copy of this page which must be included in the appendix of the final report.