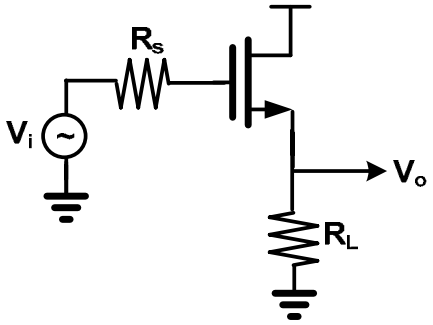
UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

E. Alon **Homework #1** **EECS 240**

Due Thursday, February 4, 2010

Use the EECS240 90nm CMOS process in all homeworks and projects unless otherwise noted. The SPICE model and instructions for running the simulator are available on the course website.

1. As a brief review of some of the basic analysis you learned in EE140, in this problem we will analyze the simple amplifier circuit shown below. You can assume that the small signal output resistance (r_o) of the transistor is infinite, and that the only parasitic capacitance associated with the transistor is its C_{gs}.



   a. Draw the small signal model of this circuit.
   b. As a function of the transistor's g_m and the resistor values R_s and R_L, what is the DC small signal gain (V_o/V_i) of the amplifier?
   c. What is the gain of the amplifier at very high frequencies?
   d. Sketch the magnitude of the transfer function of this amplifier vs. frequency and label the location of the amplifier's poles and zeros (as a function of R_s, R_L, g_m, and C_{gs}).

2. In this problem we will look at the design of MOM capacitors in our 7-level metal process. Unless otherwise noted, you should assume that all metal layers have a thickness T = 0.2μm, minimum width W = 0.14μm, minimum horizontal spacing S = 0.14μm, vertical spacing H = 0.2μm, and that the insulator is SiO_2. You can assume that the separation of the lowest layer of metal from the substrate is also H = 0.2μm, and that the inter-layer vias have the same width as the wires they are connected to. For simplicity, you can ignore fringing fields in all of these calculations.

   a. What is the maximum capacitance density (in fF/μm^2) you can achieve with a simple horizontal parallel plate? What is the ratio of capacitance to bottom plate parasitic?
   b. What is the maximum capacitance density (still in fF/μm^2) you can achieve with a vertical parallel plate? Now what is the ratio of capacitance to bottom plate parasitic?
   c. In many processes the upper layers of metal are thicker, but also have larger minimum width and spacing. For this part of the problem, let's assume that metal layers 1 through 5 have the same characteristics as before, but that metal layers 6 and 7 have T = 0.8μm, W = 0.56μm, S = 0.56μm, and H = 0.8μm. (Note that the vertical spacing from metal layer 5 to metal layer 6 is 0.2μm.) In this case (and still ignoring fringing fields), what structure gives you the highest capacitance density, and what is that density?

3. In this problem you will need to run HSPICE (or whatever your favorite simulator is). For some of the problems you should access internal device parameters such as g_m or V_{TH} – in HSPICE, you can access these with a statement like:

   .print m1_vth=par('lv9(m1)')

   (You can find the names of the various transistor parameters you might want to look at in the HSPICE manual, which can be accessed from the instructional machines – see the link on the course website.)

   For this problem, you should plot the results for all of the process corners provided in the library (i.e. *SS, TT, FF*). Unless otherwise specified, use minimum length transistors with $W=1\mu m$ and a maximum $|V_{GS}|$ and $|V_{DS}|$ of 1.2V.

   a. Plot the magnitude of the threshold voltage of an NFET and PFET as a function of channel length L. You should sweep L from 90nm to 500nm – be sure to use a step size small enough to measure a smooth curve.

   b. Plot the g_m versus V_{GS} of an NFET on a linear and log scale, biasing the transistor with $V_{GS} = V_{DS}$.

   c. Plot g_m/I_D as a function of $|V_{GS}|$ (still with $V_{GS} = V_{DS}$) for an NFET and PFET with L=90nm, 180nm, and 360nm. Then, use this data to plot $V^* = 2I_D/g_m$ as a function of $|V_{GS}|$.

   d. Still using the data from part c., plot I_D as a function of V^*.

   e. Plot the output resistance r_o and DC gain $g_m r_o$ versus V_{DS} for an NFET and PFET. You should bias the transistors with V^* = 200mV. What is the allowed output swing to maintain a DC gain of 80% of the peak value?

   f. Plot f_T and $f_T \cdot (g_m/I_D)$ as a function of $|V_{GS}-V_T|$ for L=90nm, 180nm, and 360nm. You should set $V_{DS} = V_{GS}$ and vary $|V_{GS}-V_T|$ from 0 to 500mV. What is the V^* that achieves the maximum $f_T \cdot (g_m/I_D)$ for each channel length?.

   Keep these results handy for future design work!