018/016 Calibre LVS/LPE Deck Usage

PDKD/TSMC

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Switch and Variable Setting

Calibre Switches(I)

- **#define RC_DECK – Calibre Flow**
  - Turn on this switch for Calibre XRC extraction.
  - For MOS devices, the properties w, l, as, ad, ps, pd, nrs, and nrd will be extracted.
- **#define CCI_DECK – CCI Flow**
  - Turn on this switch for Calibre+StarRCXT extraction in CCI deck.
  - For MOS devices, the properties w, l, as, ad, ps, pd, nrs, and nrd will be extracted.
- **#define LVS_DECK – CCI Flow**
  - Turn on this switch for Calibre LVS check in CCI deck.
- **#define ZERO_NRS_NRD**
  - Turn on this switch to set NRS=NRD=0.
  - XRC extracts NRS/NRD by default. In order to avoid double count in source and drain regions, please turn on this switch.

Calibre Switches(II)

- **#define extract_dnwdio**
  - Turn on this switch to extract RW/DNW and DNW/PSUB diodes.
- **#define extract_as_ad**
  - This switch is for TSMC internal library team using only.
- **#define NW_RING**
  - Turn on this switch to enable NW ring to separate the node from BULK.
- **#define Accuracy**
  - Resistance value variable setting

Calibre Variables

- **VARIABLE POWER_NAME**
  - Power name string setting.
- **VARIABLE GROUND_NAME**
  - Ground name string setting.
- **VARIABLE PRESCALE**
  - For 018 process, PRESCALE=1.0 ; for 016 process, PRESCALE=0.9. Scale factor can be found from spice model card.
  - Scale variable relates to the scale factor in shrink process. Please do not change the default value.

Calibre LVS/XRC Flow

Calibre LVS Flow

- **Run LVS deck(default):**
  - Include “source.added” file in your source netlist for subcircuits.
    - .include source.added
  - Comment the following line for LVS check.
    - //#define RC_DECK
  - Fill in the gds file name and top_cell name in the rule deck.
    - LAYOUT PRIMARY “top_cell”
    - LAYOUT PATH “top_cell.gds”
  - Fill in the source netlist name and top_cell name in the rule deck.
    - SOURCE PRIMARY “top_cell”
    - SOURCE PATH “top_cell.cdl”
  - Run Calibre
    - **% calibre –lvs –hier –spi layout.net calibre_rule_deck**
    - Files lvs.rep and lvs.rep.ext are LVS result and path check report.
  - It’s recommend to flatten dummy patterns for performance.
    - FLATTEN CELL top_cell_DM top_cell_DODDPO

Calibre XRC Extraction Flow

- **Prepare XRC technology file :**
  - Download the xCalibre RC technology file corresponding to the process you used from TSMC online.
    - For example, if your design is based on TSMC 0.18um MMRF 1P6M SALICIDE 1.8V/3.3V process(T-018-MM-SP-001-X1), you need to download the XRC technology file corresponding to this process.
  - Unzip the zip file and extract the capacitance rule statement file (rules) and resistor statement file(File name looks like "t018_mm_1p6m.res").
  - Use the Unix command 'cat' to combine these two files into a new rule file, and rename the new rule file "rules".
    - **% cat t018_mm_1p6m.res >> rules**
  - Finally, run RCX on your design. Make sure the "rules" file is located in the working directory.

Calibre XRC Extraction Flow

- **Run RC deck:**
  - Include “source.added” file in your source netlist for subcircuits.
    - .include source.added
  - Uncomment the following line for RC extraction flow.
    - #define RC_DECK
  - Fill in the gds file name and top_cell name in the rule deck.
    - LAYOUT PRIMARY “top_cell”
    - LAYOUT PATH “top_cell.gds”
  - Fill in the source netlist name and top_cell name in the rule deck.
    - SOURCE PRIMARY “top_cell”
    - SOURCE PATH “top_cell.cdl”
  - Run Calibre XRC
    - File “hcell” is used for RC cell blocking in RF devices.
    - **% calibre –xrc –phdb –hcell hcell calibre_rule_deck**
    - **% calibre –xrc –pdb –xcell hcell –rc calibre_rule_deck**
    - **% calibre –xrc –fmt –all calibre_rule_deck**
    - Files net.dist , net.dist.pex, and net.top_cell.pxi are created.

Calibre/StarRCXT LVS/CCI Flow

Calibre LVS/CCI Flow

- **Run LVS deck:**
  - Include “source.added” file in your source netlist for subcircuits.
    - .include source.added
  - Comment the following line for LVS check.
    - //#define CCI_DECK
  - Uncomment the following line for LVS check.
    - #define LVS_DECK
  - Fill in the gds file name and top_cell name in the rule deck.
    - LAYOUT PRIMARY “top_cell”
    - LAYOUT PATH “top_cell.gds”
  - Fill in the source netlist name and top_cell name in the rule deck.
    - SOURCE PRIMARY “top_cell”
    - SOURCE PATH “top_cell.cdl”
  - Run Calibre
    - **% calibre –lvs –hier –spi layout.net calibre_rule_deck**
    - Files lvs.rep and lvs.rep.ext are LVS result and path check report.
  - It’s recommend to flatten dummy patterns for performance.
    - FLATTEN CELL top_cell_DM top_cell_DODDPO

Calibre/StarRCXT CCI FLOW

- **Run CCI deck(default) :**
  - Include “source.added” file in your source netlist for subcircuits.
    - .include source.added
  - Comment the following line for CCI StarRCXT flow.
    - //#define LVS_DECK
  - Uncomment the following line for CCI StarRCXT flow.
    - #define CCI_DECK
  - Run Calibre
    - **% calibre -lvs –hier –spi layout.net calibre_rule_deck**
    - **% calibre -query svdb < query_cmd**
  - Run StarRCXT :
    - The StarRCXT mapping files with different metal scheme are put in CCI_FLOW/STAR_MAP catalog.
    - Download StarRCXT tech file(*.nxtgrd file) from TSMC online.
    - In order to get a correct spice model name for simulation in CCI flow, please add cross reference command “XREF: YES” in your star_cmd file.
    - Please add X_DEV.cmd behind star extraction command.

      % StarXtract -clean star_cmd RES_X.cmd

StarRCXT Mapping File Notice

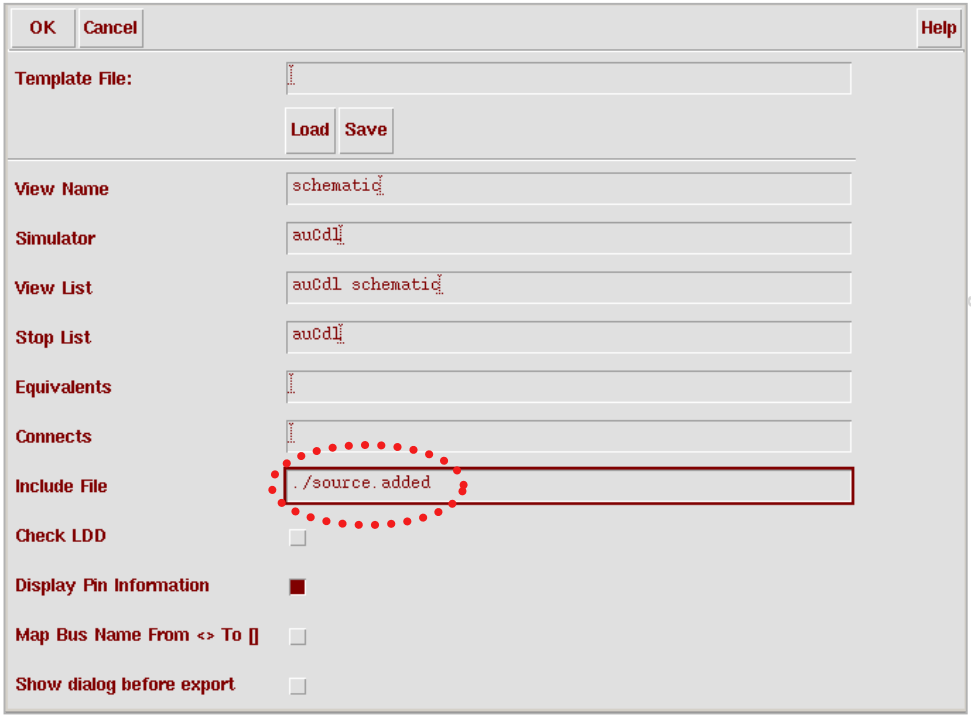
- When the switch "extract_dnwdio" is turn off, please move layer "psub_term" to remove layer.
- By default ZERO_NRS_NRS = 0, user has to set RPSQ of tndiff/tpdiff to zero (RPSQ=0.0000001) to avoid double count. Then NRS/NRD will be extracted by Calibre and output as device parameters.
  - tndiff OD RPSQ=0.0000001
  - tpdiff OD RPSQ=0.0000001
- If set ZERO_NRS_NRD = 1, users have to remove RPSQ=0.0000001 of tndiff/tpdiff. Then NRS/NRD will be extracted by StarRCXT and output as parasitic RC network.
  - tndiff OD
  - tpdiff OD
- Please ignore the warning message in StarRCXT CCI flow, it won't impact any accuracy.

Calibre LVS/XRC GUI Flow

Calibre LVS Flow(I)

1. Specify the “source.added” file as an include file for netlist export by click “Calibre->Setup->Netlist Export…”.

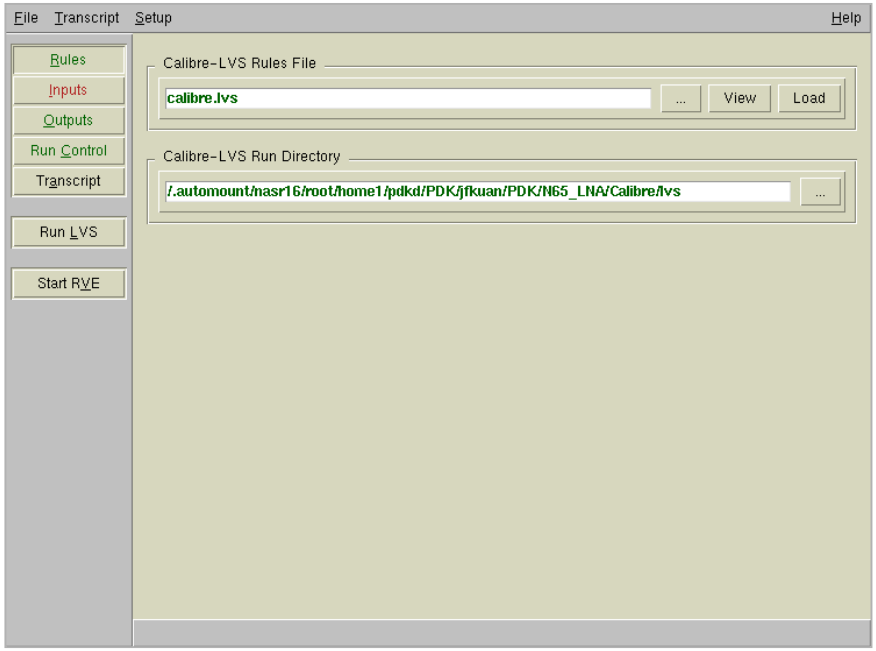
2. Click “Calibre->Run LVS” in layout window to invoke Calibre LVS graphic user interface.

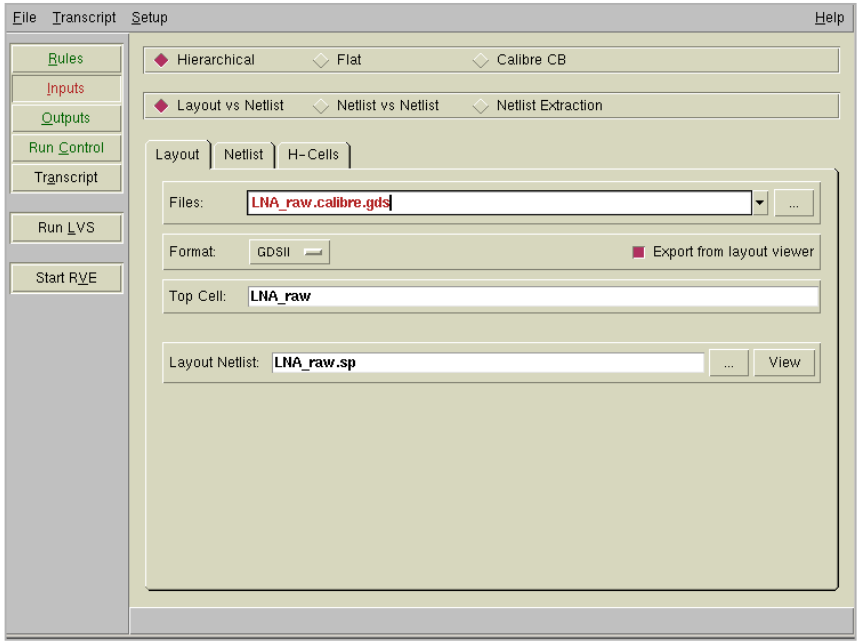


Calibre LVS Flow(II)

3. Specify the “Calibre-LVS rules file“, working directory and “Primary cell” in Calibre LVS window. If you need to change some LVS switches, you have to edit the Calibre LVS deck first.

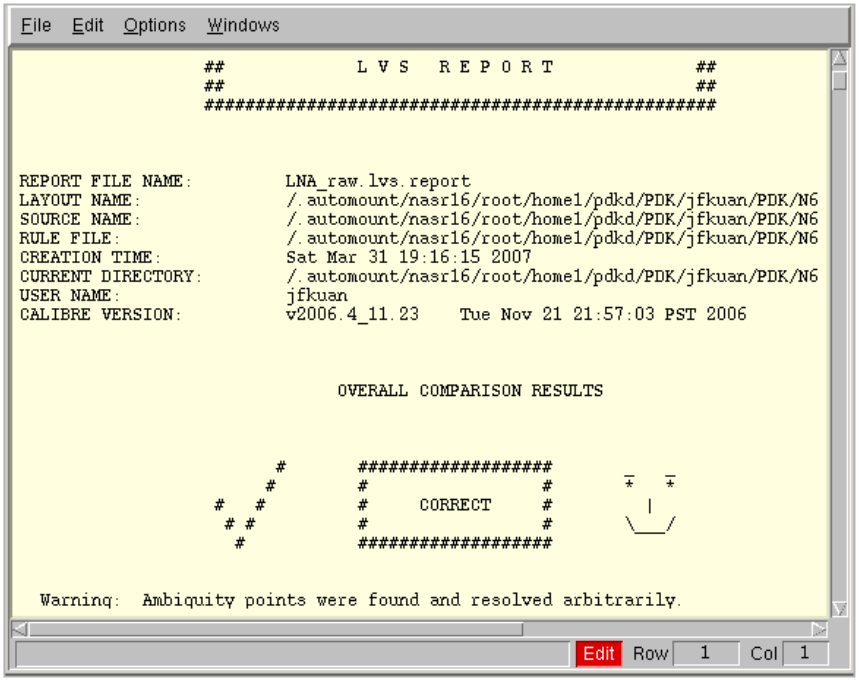
4. Click “OK” to run the Calibre GUI LVS and see the result. If the layout isn’t matched to schematic, you have to fix the layout and re-run the LVS check to make the LVS result matched.

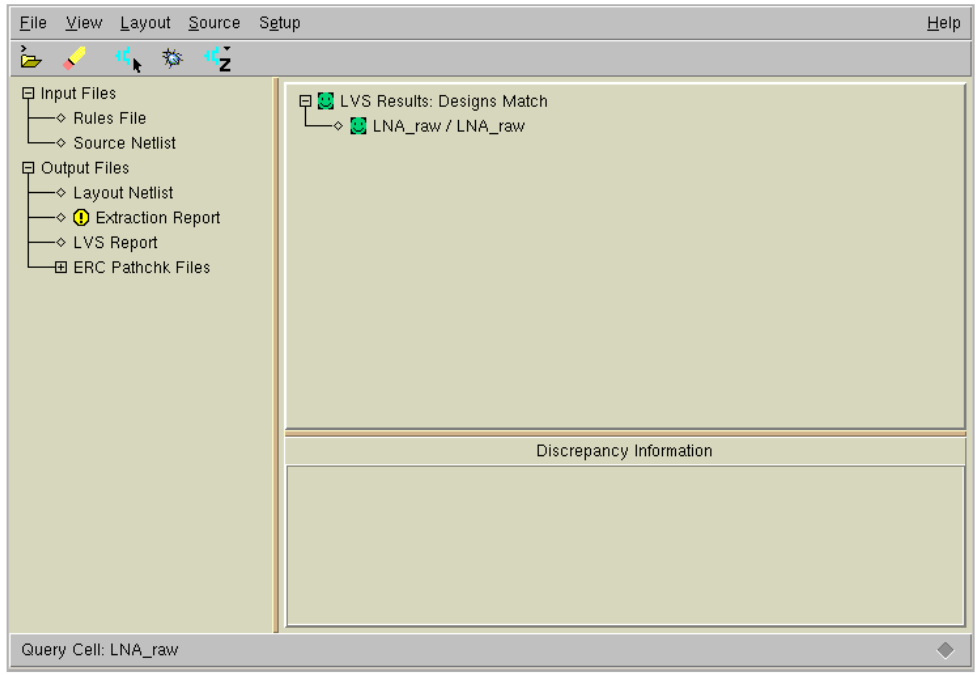




Calibre LVS Flow(III)

Below is the LVS result that shows good match between layout and schematic.





Calibre XRC Flow(I)

Before running XRC flow

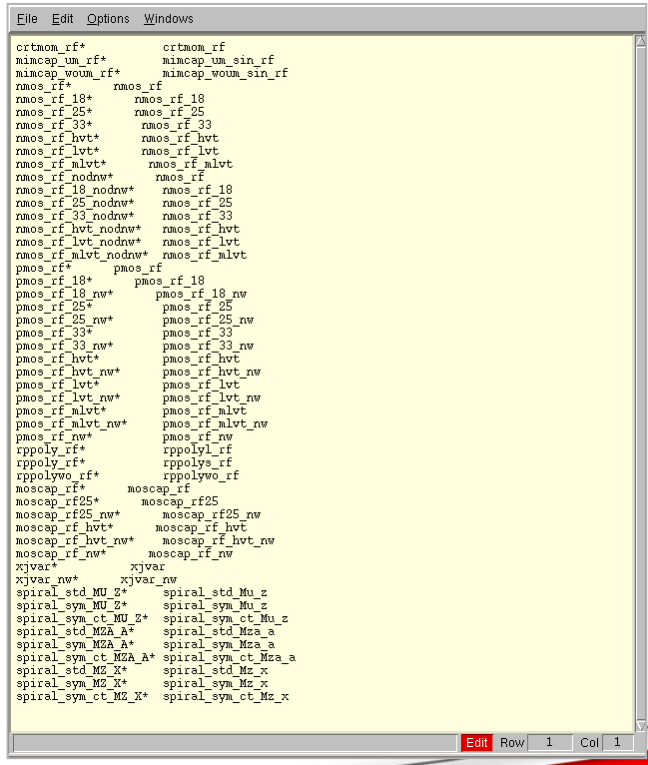
Since all of the parasitics in the P-cell have been accounted by RF PDK device model. The extraction tool must not extract parasitics inside the specified devices to avoid double counting. The following steps should be taken to run pre-characterized device (PCD) flow:

1. Add following statements in your XRC rule file:

   SOURCE CASE YES

   LVS COMPARE CASE NAMES

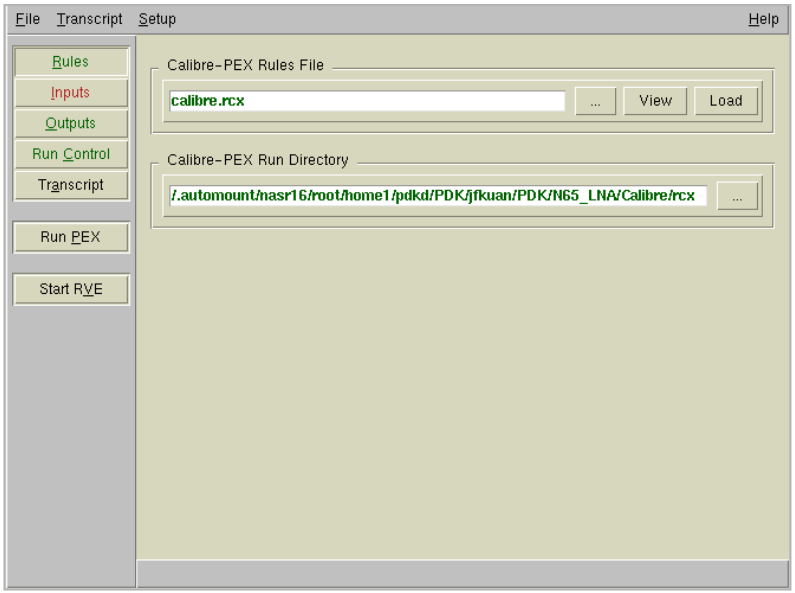
2. Add ***PEX IDEAL XCELL YES*** in your XRC rule file.
3. Prepare h-cell file for RC blocking in RF devices:

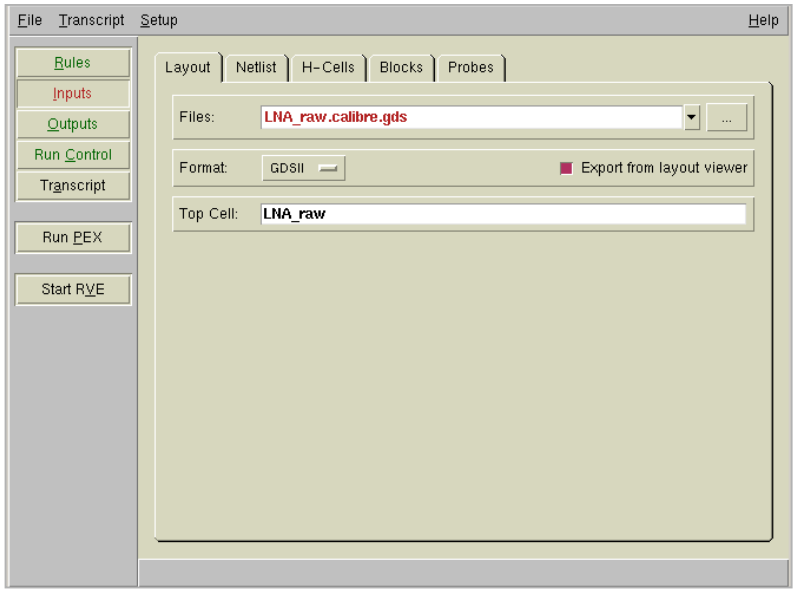


Calibre XRC Flow(II)

1. Click “Calibre->Run PEX” in layout window to invoke Calibre XRC graphic user interface.

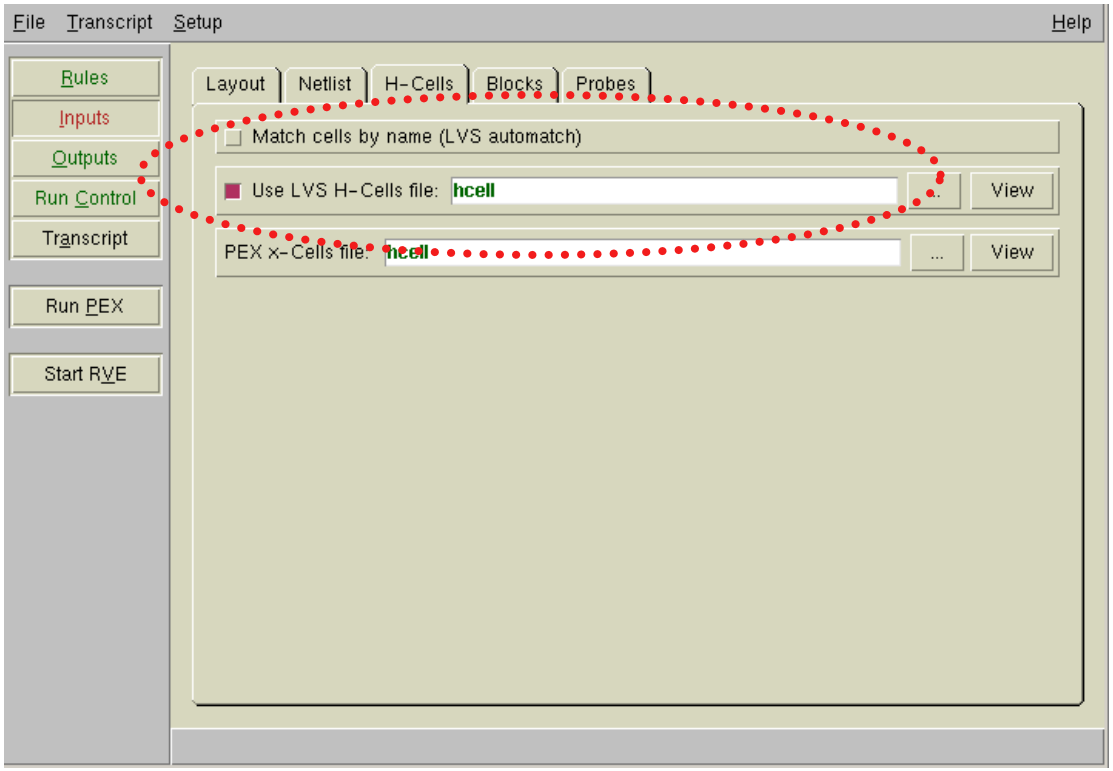
2. Specify the “Calibre-PEX rules file“, working directory and “Top cell” in Calibre XRC window. If you need to change some XRC switches, you have to edit the Calibre XRC deck first.





Calibre XRC Flow(III)

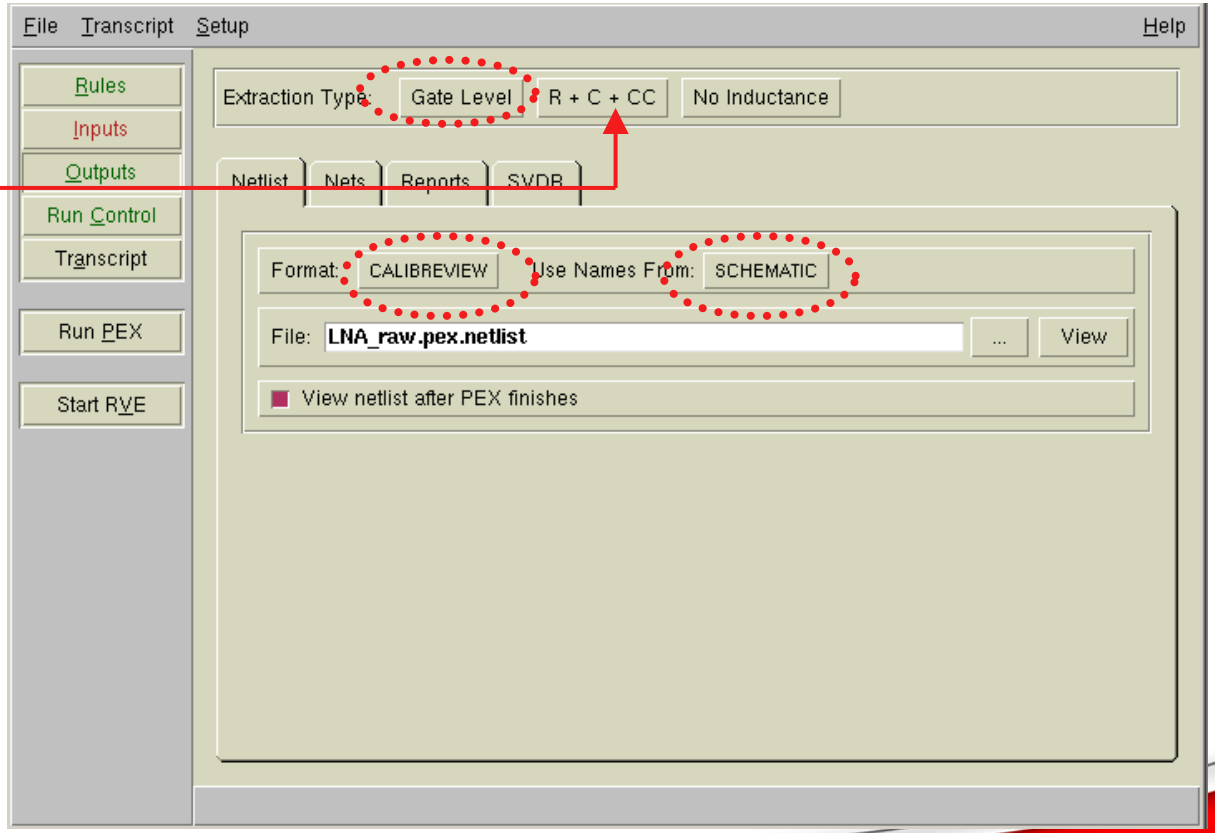
3. Enable "**Use LVS H-Cells file**" in" **Inputs->H-Cells**". Specify the H-cell file name and PEX x-Cell file name which is the hcell file that is included in LVS package.



Calibre XRC Flow(IV)

4. Select the "**Outputs**", set the "**Extraction Type**" to "**Gate Level**". Specify the output format to be "**CALIBREVIEW**" and "Use Names From" to be "**SCHEMATIC**".

Select the extraction type which you want to run.
(no parasitic, C+CC, R, R+C, R+C+CC)



Calibre XRC Flow(V)

4. Click “OK” to run the Calibre GUI RC extraction. When the extraction run is completed, a calibre view setup window will pop up. Specify the “Cellmap File”, “Magnify symbols by” .

5. Click “OK” in the Calibre view setup window to create the Calibre view.