E. Alon   **Project Part III**   **EECS 240**
Due Monday, May. 10, 2010

In this third and final phase of the project, you will be designing the complete analog front-end of a high-speed serial link. Although the only new circuit you will be dealing with is the comparator, there are several new effects you will need to take into account during this phase of the project.
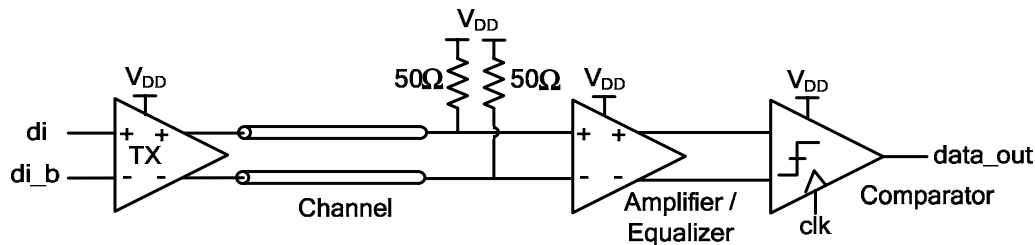
Once again, you will not be provided with a set of specifications on each of the components – figuring out the right specifications and tradeoffs is an integral part of the project. In fact, for this part of the project we will not even specify the target data-rate. Rather, as long as your data-rate is above the minimum required (3 Gb/s), you are free to explore the tradeoffs between data-rate and power consumption. However, no matter what data-rate you choose, you should be sure to minimize the power used to achieve this data-rate.

In order to give you a head-start on building the complete link, a SPICE netlist and Cadence schematic of a CML comparator have been posted on the course web-site. As long as your link functions correctly and meets the constraints provided below, you are free to modify any of the circuit components as you see fit. Note however that each one of the components has a nearly infinite number of different possible implementations, so don't just randomly tinker with the various elements. Instead, you should be sure to analyze which elements appear to be the most critical and will provide you the highest "return on investment" for the time you spend on them.

Instead of arbitrarily fixing the offsets of each of the components (e.g., the comparator) like in the previous phases of the project, we will be assuming that the offsets in our fully differential structures are dominated by V_{th} mismatch. Thus, you will be using Pelgrom's model with $A_{Vth} = 4$ mV·µm to calculate the σ of the V_{th} mismatch between each pair of matched transistors. As described in lecture, we will model this offset by including 3σ of mismatch in the worst-case direction between every pair of matched transistors.

In addition to including the actual offsets of the transistors, for this phase of the project we will also be including the fact that the power supplies of both the transmitter and the receiver will vary (i.e., are noisy). Even though supply noise is deterministic, we will model the variations on the TX and the RX as being random (just like thermal noise), but with a known power spectral density. Posted on the web is a subcircuit called nsgen that will create both supplies with a nominal DC value that you specify, but that will generate noise if you run a noise simulation in SPICE. (Note that you should look inside of this deck to figure out what the spectral densities are so that you can use them for your hand calculations.)

The specifications and constraints for your design are:

- Process: EE240 90 nm CMOS, tt corner
- Operating temperature: 25° C
- Data-rate: >3 Gb/s
- $V_{DD} = 1.2$V
- BER: < 10^{-12} with worst-case mismatch and supply noise
- Maximum input capacitance on di, di_b: 50 fF
- Capacitive load on data outputs: 50 fF

- Current mirror ratios: ≤ 20
- Maximum total capacitor area: $2000 \ \mu m^2$

Some additional notes and guidelines:

- For thermal and flicker noise calculations in SPICE, the limits of integration should be 1kHz to 100GHz.
- You can not change the value of the supply voltage V_{DD} (=1.2V). This means that if you want to e.g. lower the common-mode voltage at the output of your transmitter, you will need to modify the transmitter circuit to implement this.
- You can not assume that the data is DC-balanced – i.e., you can not use AC coupling between the transmitter and the receiver.
- You can use a total of two ideal current sources in your design: one for the transmitter, one for the receiver. Any current source loads in your signal path must be implemented with real transistors. Also, you must include the power dissipation of your biasing circuitry when you calculate the total power dissipated by your link.
- You are allowed to use ideal resistors, but any capacitors in your circuit must be implemented out of MOS devices or MOM structures. For MOM capacitors, you can use the parameters of either vertical or horizontal parallel plates from HW#1. For MOS capacitors, you can assume that the capacitance density is 6 fF/μm^2.
- Don't forget to include the source and drain perimeters and areas for each of your devices, or to implement common-mode feedback if it is required.
- Your link must function correctly over the same channel provided in Phase II.
- You can use as many digital bits as you'd like to implement offset correction circuitry.
- You should include the nsgen subcircuit when you simulate the noise performance of your circuit. However, you should separate out how much of the total noise you measure at the input to the comparator comes from the supply vs. from thermal and flicker noise.
- You can place your sampling clock anywhere within the data eye you'd like, as long as it is always at the same relative time within the bit. You can also use as many clock phases as you'd like. However, your clocks must be driven by real inverters, and you must include the power dissipated by these inverters when calculating your total power consumption.

Your final submission for the project will consist of two parts: 1) a written report including the items listed below, and 2) a 4 minute, 4 slide presentation about your design that you will give on May 7th (time/location TBD).

The written report should include:

1. A brief summary of the specifications you achieved:
   o Data-rate:
   o Total power consumption:
      ▪ TX:
      ▪ Equalizer:
      ▪ Comparator:
      ▪ Biasing:
      ▪ Other:
   o BER with worst-case offset:
      ▪ Min. eye opening at RX input:
      ▪ Total offset at comparator input:
      ▪ Total thermal + flicker noise at comparator input:
      ▪ Total supply noise at comparator input:
2. **Clearly** labeled schematics of any new components you designed, including device sizes and nominal bias currents. (You do not need to show the transmitter or comparator if you simply used the default designs.)
3. A **concise**, **clear** description of the procedure you followed to design the front-end. Some example questions you should aim to answer include: What were your main goals? (e.g., highest

speed or lowest power) How did you decide upon the equalizer topology? How did you choose which components to modify? How did you set the swing at the transmitter? How did you deal with the noise on the power supplies?

4. Hand analysis and simulations plots/printouts verifying that your design meets the specifications you provided in 1.

5. An electronic text or Excel file listing the simulated differential voltage at the input of your comparator and the digital output of the comparator vs. time for the data inputs provided in eye_input_final.sp (which will be posted on the course web-site).

6. The HSPICE netlist of your design (again, you do not need to include any of the "default" components you used).