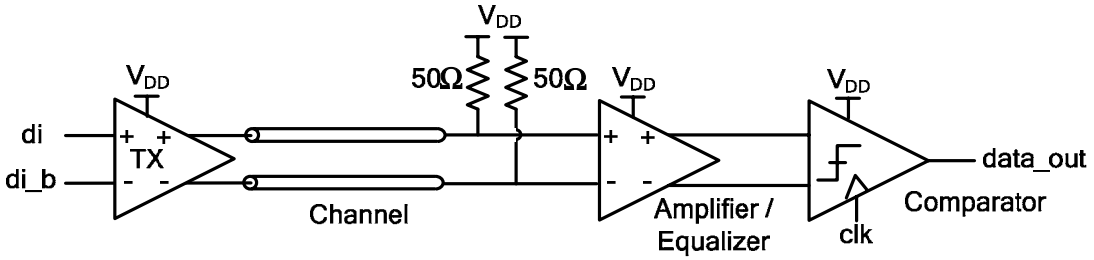
UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

E. Alon **Project Part II** **EECS 240**
Due Friday, Apr. 23, 2010

In this second phase of the project, we will be exploring how to modify the front-end amplifier in order to implement an equalizer for the analog front-end of a high-speed serial link. Below is a conceptual schematic highlighting the main components of the front-end.



Since in the final phase of the project you will not be provided with any specifications on the individual components themselves, in this phase we will start along this road by allowing you to change the swing at the transmitter. However, your main focus in this phase of the project should be to understand the design of the equalizer, so if you are unsure about what transmit swing to use, start with ~20mV. As usual, your overall goal is to minimize power consumption while meeting the performance specifications.

Since you can now change the transmit swing, you will use the actual transmitter circuits in this phase of the project. Therefore, a SPICE netlist and Cadence symbol for a "default" transmitter have been posted on the course website; we have also provided you with a model for the channel – see the additional notes below. You are free to modify the circuit topology of this transmitter, but this is by no means necessary (or even recommended) for this phase of the project.

The specifications and constraints for this phase of the project are:

- Data-rate: 3 Gb/s
- BER: $< 10^{-12}$
- $V_{DD} = 1.2V$
- Comparator C_{in}: 30 fF (i.e., the comparator loads both v_{o+} and v_{o-} with 60fF of capacitance)
- Comparator offset: 20 mV
- Maximum input capacitance on di, di_b: 50 fF
- Current mirror ratios: ≤ 20

Some additional notes and guidelines:

- You can use a total of two ideal current sources in your design: one for the transmitter, one for the receiver. Any current source loads in your signal path must be implemented with real transistors.
- You are allowed to use ideal resistors, but any capacitors in your circuit must be implemented out of MOS devices or MOM structures. For MOM capacitors, you can use the parameters of either vertical or horizontal parallel plates from HW#1.
- Don't forget to include the source and drain perimeters and areas for each of your devices, or to implement common-mode feedback if it is required.

- The "default" transmitter which has been provided to you in "tx.sp" is a "current-mode" design that is scalable in terms of the swing it provides at the output. For example, if you instantiate the transmitter with:

  xtx di di_b vp_t vn_t vdd tx sw=0.1

  then the swing at the output of the transmitter will have 100 mV of differential amplitude (i.e., 200 mV peak-to-peak).
- Your link must function correctly over the channel provided in the "chan.sp" file posted on the website.
- To simplify creating your schematics/netlists, the website also includes Cadence views of the transmitter and the channel model that you can instantiate as symbols. By using the "HspiceD" simulator in Analog Environment, you can use these symbols to generate netlists that include these components. You will however need to include the "tx.sp" and "chan.sp" files in your top-level deck in order for HSPICE to see what's inside of these symbols though.

The written report should include:

1. **Clearly** labeled schematics of your equalizer design (and transmitter, but only if you modified it) including device sizes and nominal bias currents.
2. A **concise**, **clear** description of the design procedure you followed. Examples of questions you should answer here include: How did you decide upon the equalizer topology and specifications? How did you set the swing of the transmitter?
3. Hand analysis (including noise analysis of your equalizer and BER of the overall link) and simulations plots/printouts verifying that your design meets the required specifications. If your description of the design procedure already includes the hand analysis you did (e.g. for noise), it does not need to be repeated here.
4. An electronic text or Excel file listing the simulated differential voltage at the output of your vs. time for the data inputs provided in eye_input_ph2.sp and eye_ph2.vec (both of which have been posted on the course web-site). Note that you do not need to print this out – just submit it electronically by email.
5. The HSPICE netlist of your equalizer along with the decks you used to test your design. This can also be submitted purely electronically by email.