A Fully Differential Transconductance Amplifier

--EE240 final project, Spring 2001

Shiying Xiong (xiongsy@eecs.berkeley.edu)
Min She(mshe@tft.eecs.berkeley.edu)

Department of Electrical Engineering and Computer Science
University of California at Berkeley, CA 94720

Abstract

In this project, we design a fully-differential operational transconductance amplifier to be used in the first stage of a high resolution pipelined A/D converter. The circuit is realized with a two-stage amplifier design. The first stage is a telescopic cascode stage, followed by a common source second stage. It's demonstrated that this circuit meets all the design specification while achieving low power consumption, which is less than 10mW. This OTA achieve a large DC gain and high swing output of above 2.2V. The circuit performance is summarized below:

Device model	slow	nominal	fast
Output swing Vo,max	±2.35V	±2.41V	±2.45V
Total noise Vo,noise (uV)	463.6	468.2	468.7
Dynamic range (dB)	71.1	71.22	71.36
Open loop peak gain	761K	882K	957K
Settling time	16.28ns	23.79ns	21.23ns
OTA power dissipation	8.292mW	8.294mW	8.295mW
CMFB power	3.59mW	3.59mW	3.58mW
Bias circuit power	8.996mW	8.996mW	8.996mW
Phase margin	67	60	62
Unit gain band width	513MHz	514MHz	567MHz

Table 1. circuit performance summary.

1. Introduction

The design specification of the OTA with 3V power supply is:

- Dynamic range at output, DR ≥70dB
- Settling Accuracy≤ 0.05%
- Setting time ≤25ns

The design should also minimize the power consumption while meeting all the requirements. When selecting an optimal circuit architecture, a number of fundamental issue and trade-off should be considered based on the design requirement.

First, There is choice between single-stage circuit and multi-stage circuit. In this amplifier, the feedback factor is very small (less than 1/16) due to the very small feedback capacitor. To meet the settling accuracy, we still need high DC gain which should be at least 40,000. A single-stage topology of either simple folded-cascode or telescopic cascode circuit might not achieve the desired DC gain. Although telescopic triple cascode circuit can meet the DC gain, 3V power supply may limit the output swing and then the dynamic range. Second, we completely eliminate the possibility of using three or more than three-stage amplifiers since the circuit will be both slow and power-consuming.

Although DC gain requirement seems to require a two-stage design, we should not eliminate the possibility of realizing the circuit with one-stage. Some analysis is done here to finalize the choice. In fact, we have several choices here: folded-cascode or telescopic topology, gain-boosted one stage or two-stage circuits.

If we use a two-stage design, the first stage can be realized using either a telescopic or folded-cascode topology. The topology with lower power

consumption and low noise should be chosen. The folded-cascode stage has 2 extra legs, which dissipate more static power than the telescopic counterpart. Also the folded-cascode stage has extra current source transistors, they directly add to the noise factor of the input stage. The main advantage of folded-cascode is that the output swing will be higher than that of telescopic topology since there are only four devices instead of five there. But in the two-stage design, the output swing is determined mainly by the second stage. Since a common-mode feedback is involved, common-mode input range is of less concern. Therefore, a telescopic first stage topology is the right choice for low-power, low noise two-stage OTA .

On the other hand, if we choose single-stage design. The folded-cascode is more favorable because there are only four devices, which leads to high output voltage range. Saving a voltage drop of one device is very important in our design. The output resistance of the MOSFET is a strong function of Vds. To achieve the high gain, Vds of each device should be much larger than Vdsat. Therefore some voltage margins need to be left across the source and drain to get a reasonable output resistance. In this point of view folded-cascode is better in single-stage OTA.

So now we have choice between: Regulated folded-cascode single-stage OTA and Two-stage OTA with telescopic first stage. Single-stage circuit is inherently faster than two-stage design. And theoretically speaking, single-stage will consume less power because of fewer current legs.

On the other hand, two-stage design allow high output swing, more noise can be allowed for the specified dynamic range. Therefore smaller capacitors can be used in two-stage design. Then for a fixed settling time, smaller current can be used due to smaller capacitor. That is also to say, for fixed current, two-stage can be even faster than one-stage design.

To finalize the choice, we tried both single-stage design and two-stage design to estimate the current and power consumption while meeting the specified design requirement. After some simple calculation, we find regulated single stage design need larger capacitors and therefore larger current to achieve the specified settling speed. Therefore, we conclude that two-stage OTA with telescopic first stage is the right choice for this project.

In the following section, schematic layout of the circuit will be shown first. Devices size and bias point for each transistor are summarized in table 2.

2. Amplifier design and analysis

The two-stage OTA is shown in Figure 1(next page). The second stage is made of a NMOS common-source amplifier.

The compensation technique is necessary in two-stage amplifier to maintain stability. Standard miller compensation use pole-splitting to move the dominant pole to lower frequency and the non-dominant pole to high frequency. Instead, cascode compensation is utilized here because higher bandwidth can be achieved with this technique.

In the signal path, we use NMOS transistor because they are about three times faster than PMOS device since the mobility of electrons is much larger than that of holes, although PMOS device may give less flicker noise.

The transistors size and bias point is shown in table 2. In the appendix, hand calculation is conducted first to estimate the capacitor size, bias current, transistor size and so on, then spice simulation is used to tune those parameters a little and the design is modified by better estimation. In this section, we present the results from the analysis and the trade-off on device size, capacitor size and bias current are also shown here.

Dynamic Range

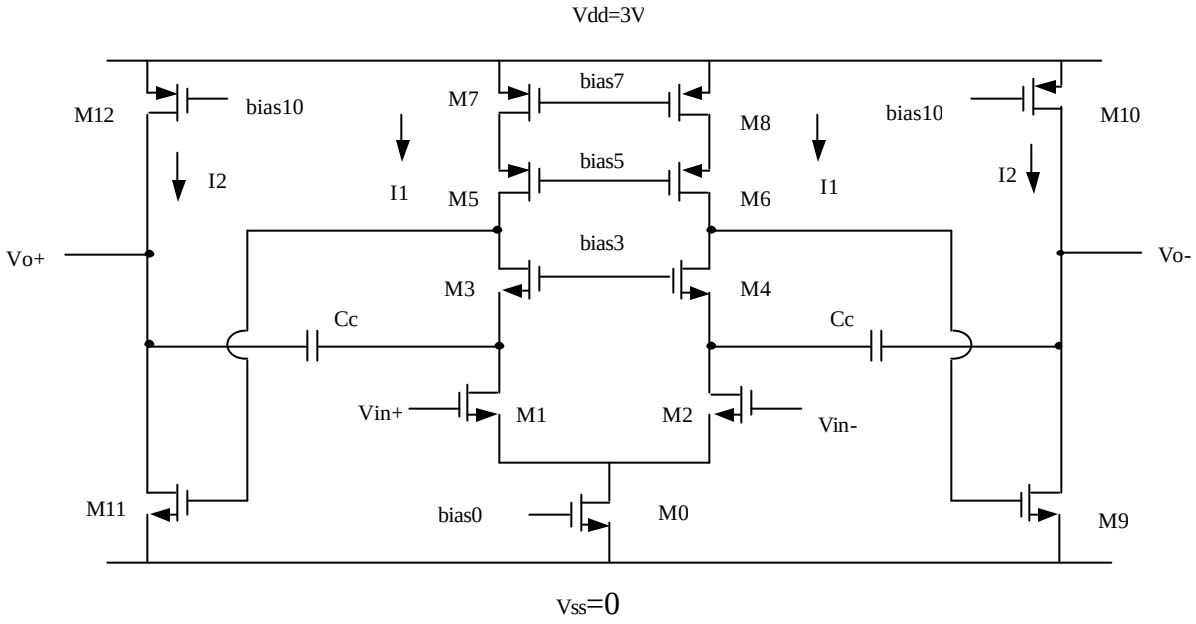


Figure 1 two-stage fully differential OTA

transistors	W/L (um/um)	I (mA)	Gm (mS)	Vdsat (mV)
M1, M2	266.3/0.35	0.575	10.05	85
M3, M4	532.6/0.7	0.575	9.94	91
M5, M6	1446/0.7	0.575	8.44	111
M7, M8	518.2/0.7	0.575	6.13	168
M9, M10	124.9/0.7	0.807	6.94	177
M11, M12	290.9/1.05	0.807	4.73	310
M0	200/0.7	1.15	10.01	172
Cc	1.0pF			
Cs	6.4pF			

Table 2 device size and bias point in OTA circuit.

The dynamic range at the output of the amplifier is given by the following equation:

$$DR = 10\log\frac{P_{signal}}{P_{noise}} \qquad (1)$$

The maximum output swing is determined by the saturation voltage and the necessary drain voltage margin of the transistors in the second stage. The total noise at the output should be less than $491.9uV$ rms assuming ±2.2V output swing. The total output noise is given by

$$P_{noise} \approx 2*\frac{2}{3}*\frac{kT}{Cc}*F*n_{f1} + \int_1^{\infty}\frac{2*n_{f2}*k_n}{C_{ox}W_1L_1 f}*H(s)df \qquad (2)$$

Here the first term is thermal noise contribution and the second term is the flicker noise from the input device. F and n_{f1} are feedback factor and noise factor in thermal noise calculation, respectively, they are given as:

$$F = \frac{C_s/16}{C_s + C_{gs1} + C_s/16}$$

$$n_{f1} = 1 + \frac{g_{m7}}{g_{m1}} = 1 + \frac{V_{dsat1}}{V_{dsat7}} \qquad (3)$$

$n_{f2} = 1 + \frac{k_p m_p}{k_n m_n}(\frac{L_1}{L_7})^2$ is the flicker noise factor. H(s) is a transfer function which can be found in the appendix.

When using equation (2), we already made some assumptions: first, we assume the noise from second stage is negligible, because it's attenuated by the square of the first stage gain when referring to the input. Second, it's assumed that the noise from the cascode device can be negligible.

It's necessary to minimize the ratio $\frac{g_{m7}}{g_{m1}}$ to reduce the noise. Therefore we had to reduce noise by increasing V_{dsat7}/V_{dsat1}. Regarding flicker noise contribution, it's often small since this design uses big device. Also increasing the length of M7 reduces the flicker noise factor, which also helps.

On the other hand, the feedback factor F needs to be maximized. Then C_{gs1} need to be minimized and hence the input device should have minimum gate length. At the beginning, we neglect the flicker noise and calculate the capacitor parameter. The compensation capacitor required to achieve 70dB dynamic range is 0.616 pF. To leave sufficient headroom for the flicker noise and also noise from the second stage at high frequency, we choose 1 pF for the Cc.

Settling time

The settling time consists of two parts: slew-rate limited settling and linear settling. During slew region, the capacitors at both first stage and second stage need to be charged. The slew rate limit can be reached in either stage and it's expressed as:

$$SR = \min\left(\frac{I_1}{C_c}, \frac{I_2}{C_c + C_{Leff}}\right) \qquad (4)$$

Here I_1 and I_2 are the current through first stage and second stage, respectively. C_{Leff} is the effective loading capacitor at the output.

Generally speaking, to minimize power consumption, these two terms need to be equal: $\frac{I_1}{C_c} = \frac{I_2}{C_c + C_{Leff}}$. The total settling time is $t_S = t_{SR} + t_{lin}$, we have

$$t_{SR} = \frac{V_{ostep} - V_{dsat1}/F}{I_1} \cdot C_C \qquad (5)$$

Here $V_{ostep} = 2.2V$, Let's take $V_{dsat1} = 150mV$, then $t_{SR} \approx 0$ since the feedback factor is so small. Hence in the settling time calculation, we don't consider the slew settling time. The linear settling time can be expressed as:

$$t_{lin} = -\frac{1}{Fw_u} \ln \frac{e \cdot F \cdot V_{ostep}}{V_{dsat1}} \qquad (6)$$

$$\text{with} w_u = \frac{g_{m1}}{C_C}$$

In the above analysis, we assume the system is stable, that is to say, the phase margin is guaranteed. In our miller cascode compensation scheme, there are two complex conjugate poles and one zero at the right plane and another zero on the left plane. The conjugate complex poles can be expressed as:

$$P_{2,3} = -w_n\left(1 \pm \sqrt{D}\right),$$

$$D = 1 - 4 \cdot \frac{g_{m9}}{g_{m3}}\left(\frac{C_C}{C_3} \cdot \frac{1}{2 + \frac{C_C}{C_{Leff}} + \frac{C_{Leff}}{C_C}}\right),$$

$$w_n = \frac{1}{2}\frac{g_{m3}}{C_C}\left(1+\frac{C_C}{C_{Leff}}\right)$$

The effect from M3 and M5 can be decoupled [1] so simplified expression can be obtained:

$$P_1 \approx \frac{g_{m1}}{C_C}F,\ p_2 = \frac{g_{m9}}{C_{Leff}},\ P_3 = \frac{g_{m3}}{C_C + C_{gs3} + C_{gd1}}$$

To maintain large phase margin we must have:

$$g_{m3} >> g_{m1}F,\ g_{m9} >> g_{m1}F\frac{C_{Leff}}{Cc},$$

which is easy to met and hence not a problem in our case since we have small F.

Open-loop Voltage gain

Although there is no explicit requirement for the open-loop gain, we still need a large low frequency DC gain if we want to meet the settling accuracy since the feedback factor is so small. The DC gain is the product of the first stage gain and second stage gain:

$$A_{dc} = \{g_{m1}.(g_{m3}r_{03}r_{01} \parallel g_{m5}r_{05}r_{07})\}\{g_{m9}.(r_{09} \parallel r_{011})\}$$

To maximize the output resistance and hence the DC gain, we can use long channel transistor for the device which is not in the signal path such as M7, M8, M10 and M12, since they do not capacitively load the signal path.

Bias Circuit

In this project, cascode high swing bias circuit is used to bias the two-stage OTA. The circuit is shown in Figure 2. The cascode topology is used to increase the matching of currents in different leg and the bias network will be less sensitive to process variation and power supply.

The Vdsat of the biasing devices are chosen to be same as those in the OTA to guarantee good matching. Generally speaking, the device in bias circuit can be scaled so less current and hence less power can be consumed by the bias circuit. The output of the first stage is biased at 782mV. During the design of the second stage the Vdsat for M9 and M10 were adjusted to a proper value so a level shifter between the two stages is unnecessary.

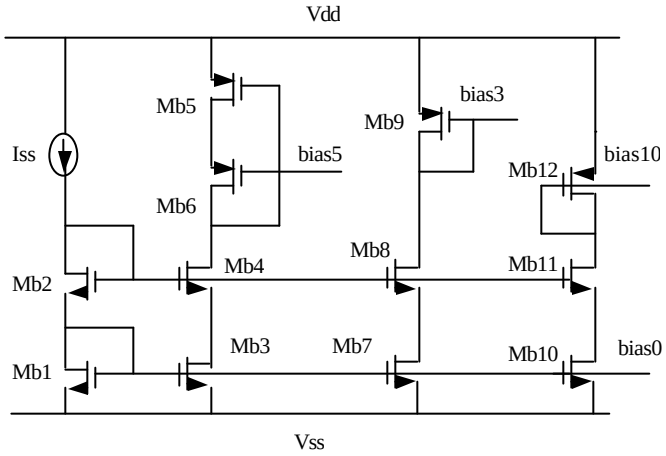


Figure 2: Bias circuit.

device	Width(um)	Length (um)	Ibias (mA)
Mb1,Mb3, Mb7	100	0.7	0.6
Mb2,Mb4, Mb8	133.2	0.7	0.6
Mb5	44	0.7	0.6
Mb6	1446	0.7	0.6
Mb9	18.2	0.7	0.6
Mb10, Mb11	200	0.7	1.2
Mb12	436.1	1.05	1.2
Mcm	200	0.7	1.2
Mcm1,Mcm2	518.2	0.7	0.6
Mcm3,Mcm4	518.2	0.7	0.6
Cm1,2	0.01pF		
Vref	1.5V		

Table 3. device size in bias circuit and CMFB circuit.

Common Mode feedback

Common mode feedback is necessary in a fully differential amplifier, otherwise the bias voltage at the output node will not be well defined. With CMFB the process of optimization will be less difficult. The circuit is shown in Figure 3. It's a differential pair with diode connected loads. The device size should be chosen in the way that the gain of CMFB circuit will not be large to make the phase margin worse, otherwise it will cause oscillation in the output wave.

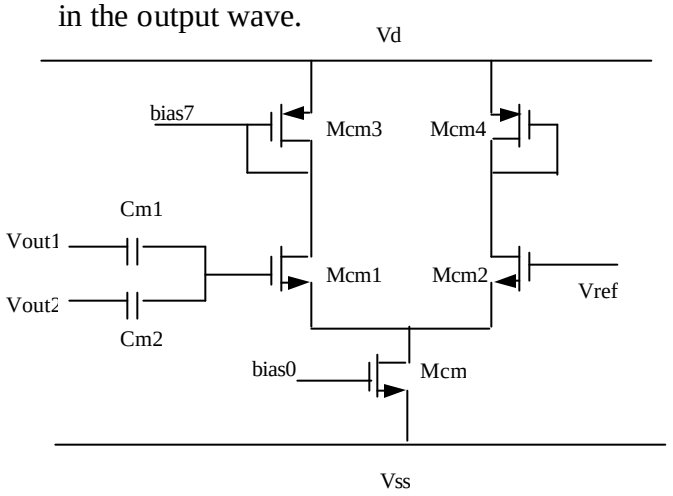


Figure 3. Common-mode feedback circuit.

Circuit Performance

Hspice simulation results and deck are attached at the end. Output swing, total noise, step response and ac transfer function are shown there. It's verified that the two-stage OTA meet all the design requirement. The results are summarized in table 1.

Output swing and dynamic range

The DC sweeps of the input signal with the corresponding output voltage for the slow, nominal and fast models are shown in Figure A. It's evident that the DC gain are higher than 40,000 for the output swing between –2.35 V and 2.35 V in the slow model. In the nominal and fast model, the output swing is even a little larger.

The dynamic range for all three models is above 70dB.

Noise

The output noise density is simulated by spice. The total output noise was calculated by integrating the noise density from 1Hz to 1000GHz. The total noise in the circuit is $468.7\,uV$ for the fast model, which is the worst case. Please refer to Figure B.

Frequency response

The frequency response is shown in Figure C. It's shown that phase margin is better than 60 in all three models.

Settling

The step response of the amplifier is shown in Figure D1 to Figure D3. There is very small settling time difference in the rising step and falling step. The settling time are 16.28ns, 23.78ns, 21.23ns for slow, nominal and fast model in the rising step, respectively, while they are 16.07ns, 23.79ns, 21.264ns in the falling step, respectively.

The settling time is fastest in the slow model. In fact, because the oscillation in slow model is largest, which helps the settling.

Power consumption:

It's summarized in table 1. The two-stage OTA consumes only 8.3mW power while common mode feedback circuit consume less than 3.6mW.

Conclusion

In this project, a fully differential OTA with EE240 0.35um technology is designed and optimized. The simulation results show all of the design requirement are met. The amplifier itself dissipate only 8.3mW of power. With 3V supply, the DC peak loop gain can be as high as

761K. The dynamic range is above 70dB. The settling time is 23.79 ns in the worst case.

Comments

The CMRR and PSRR in this circuit should be reasonable. Finite CMRR is due to the finite resistance of the tail current source. Both of them can be improved by cascading the tail current source. Due to time limit, we didn't do that.

Reference

[1] Feldman, Arnold, "High-speed, low-power Sigmal-delta modulators for RF baseband channel applications", Ph.D thesis, UCB, 1997.
[2]Nakamura, Katsufumi, "An 85mW, 10b, 40Msamples/s CMOS Parallel-Pipelines ADC", IEEE Journal of Solid-State Circuits, Vol.30, No.3, 1995.

Appendix: parameter calculation (hand analysis**)**

Estimate Cc from DR requirement:

At first, we don't take into account of the flicker noise, so the noise expression is

$$P_{noise} \approx 2 * \frac{2}{3} * \frac{kT}{Cc} * n_f / F \qquad (7)$$

Here we assume $F = \frac{Cs/16}{C_s + C_{gs1} + Cs/16} \approx \frac{1}{18}$

and $n_f = 1.5$, voltage swing is ±2.2V.

From DR>70dB requirement:

$$P_n < P_s \times 10^{-7} = 2.42 \times 10^{-7} V^2$$

$$\Rightarrow \sqrt{\overline{V_n^2}} < 491.9uV$$

Then from equation (7), we get Cc=0.616pF.

To make sure there is enough design margin for flicker noise and noise from second stage and so on, we choose Cc=1pF. But Cc can't be too large, otherwise we need large current to meet the settling time.

Bias current and input device size :

As we said before, the slew rate limited settling time is negligible. Here we only consider the linear settling time:

$$t_{lin} = \frac{1}{Fw_u} \ln \frac{e \cdot F \cdot V_{ostep}}{V_{dsat1}}, \text{with} w_u = \frac{g_{m1}}{C_C} \qquad (9)$$

$$-\ln \frac{e \cdot F \cdot V_{ostep}}{V_{dsat1}} = \ln \frac{0.0005 \times \frac{1}{18} \times 2.2}{0.10} = 7.4 \qquad (10)$$

$t_{lin} < 25n\sec \Rightarrow w_u > 5.328 \times 10^9 rad/s \Rightarrow$ $g_{m1} > 5.328mS$. Actually we choose $g_{m1} = 12mS$ to give enough headroom for the settling time. $I_1 = g_{m1} * V_{dsat1} / 2 = 0.6mA$. (Here we take $V_{dsat1} = 100mV$). Then

$$\left(\frac{W}{L}\right)_1 = \frac{g_{m1}}{k_n' \cdot V_{dsat1}} = \frac{12 * 10^{-3}}{190 * 10^{-6} * 0.1} = 631.6,$$

$$L_1 = 0.35um \Rightarrow W_1 = 221um$$

$$C_{gs1} = 5.3fF * 0.35 * 221 * 2/3 + 0.24 fF * 221$$

$$= 0.326 pF$$

As mentioned in the EE240 class, the feedback capacitor should not be less than C_{gs1}, so we take $C_f = 0.4 pF$, then

$C_s = 16 * C_f = 6.4pF$. The total capacitance seen at the output is $C = C_C + C_{Leff}$,

$$C_{Leff} = C_L + C_F(1-F) + C_{dtot} = 1.68pF$$

when assuming C_{dtot} at the output is about 1pF.

Phase margin consideration and second stage current:

The phase margin is expressed as:

$$\Phi_m = \arctan\left(\frac{P_2}{w_u}\right) = \arctan\left(\frac{\frac{g_{m9}}{2C_L} \times \frac{C_C + C_L}{C_L}}{w_u}\right)$$

we choose $\Phi_m = 60^O$, so $g_{m9} = 8mS$,

From swing consideration let $V_{dsat9} = 200mV$, then

$$I_2 = g_{m9} * V_{dsat9} / 2.0 = 0.8mA.$$

Estimate other transistor size:

The bias current in each stage is well defined now. After choosing the appropriate Vdsat for each device (subject to open loop gain requirement and output swing requirement), we can determine each transistor size.

We choose $V_{dsat,3} = 150mV$ and we get

$$(\frac{W}{L})_{3,4} = \frac{2 * I_1}{m_n C_{ox} V_{dsat,3}^2} = 701.8$$

$$V_{dsat,7} = \frac{V_{dsat,1}}{n_f - 1} = 0.2V, \text{ and}$$

$$(\frac{W}{L})_{7,8} = \frac{2 * I_1}{m_p C_{ox} V_{dsat,7}^2} = 512.86.$$

We choose $V_{dsat,5} = 100mV$, then

$$(\frac{W}{L})_{5,6} = \frac{2 * I_1}{m_p C_{ox} V_{dsat,5}^2} = 1333.$$

And in the same way, we can determine the size of the second stage as

$$(\frac{W}{L})_{9,10} = \frac{2 * I_2}{m_n C_{ox} * 0.2^2} = 210.5$$

$$(\frac{W}{L})_{11,12} = \frac{2 * I_2}{m_p C_{ox} * 0.3^2} = 197.53$$

The final design of those parameter used in spice is very close to the parameter determined from the hand calculation. Some of the main parameters are summarized in table 4.

parameter	Hand analysis	Spice value
I_1	0.6mA	0.575mA
I_2	0.8mA	0.807mA
$(W/L)_{1,2}$	631.6	760.9
$V_{dsat1,2}$	100mV	85mV
g_{m1}	12mS	10.05mS
$(W/L)_{7,8}$	333.3	740.3
$V_{dsat7,8}$	200mV	168mV
$(W/L)_{9,10}$	210.5	178.4
g_{m9}	8mS	6.94mS
$V_{dsat9,10}$	200mV	177mV
Cc	1pF	1pF
Cs	6.4pF	6.4pF

Table 4. hand calculation and spice parameter comparison.

Note: the transfer function in equation (2) can be expressed as

$$H(s) = \frac{1}{1 + \frac{sC_c}{g_{m1}F}}$$, since flicker noise in our design is very small and it's very difficult to calculate the flicker noise integration in equation (2) analytically, we didn't do detailed calculation for flicker noise. But we raised the Cc value to give enough margin for flicker noise.

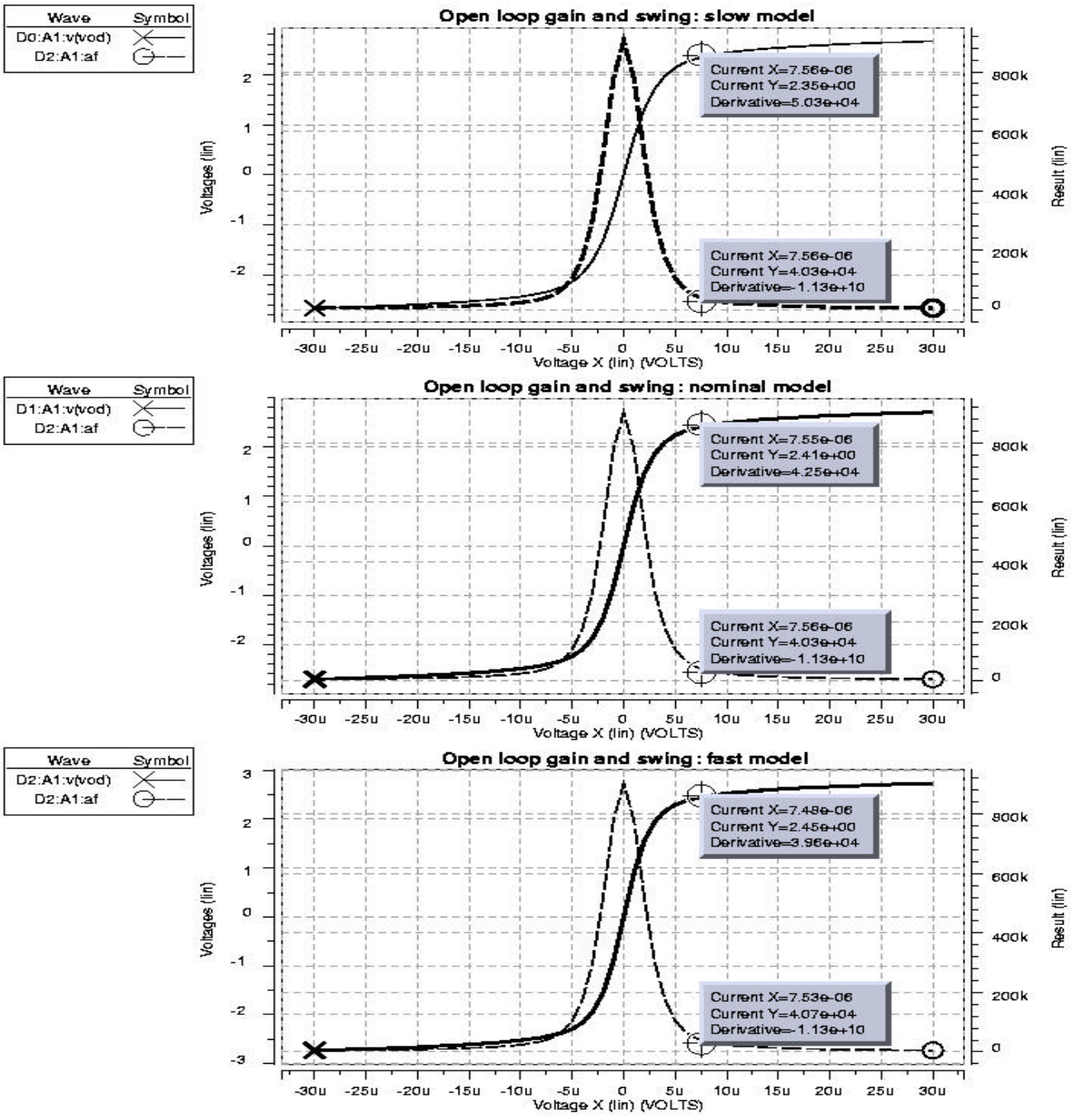


Figure A: Open-loop gain and output swing.

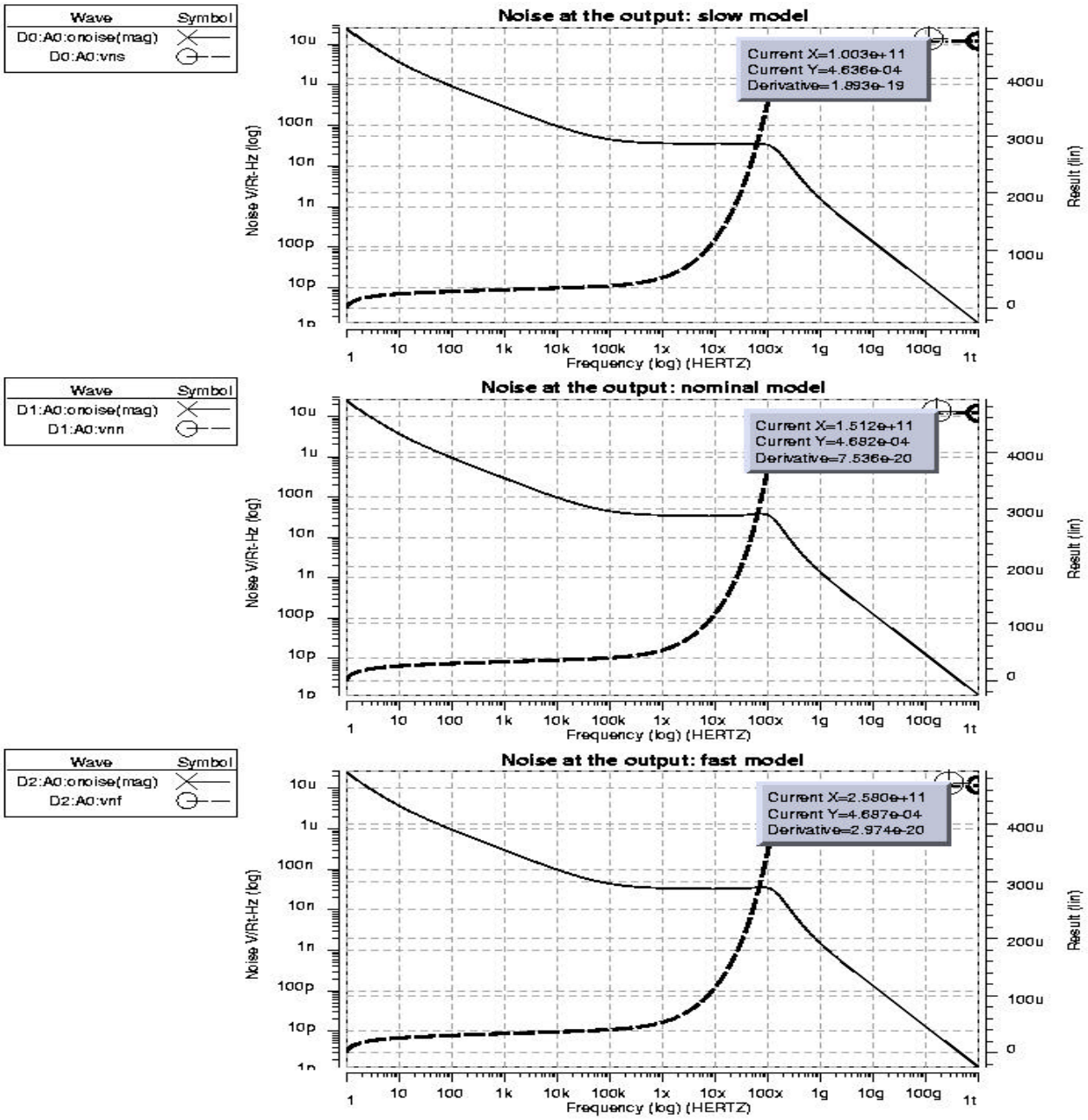
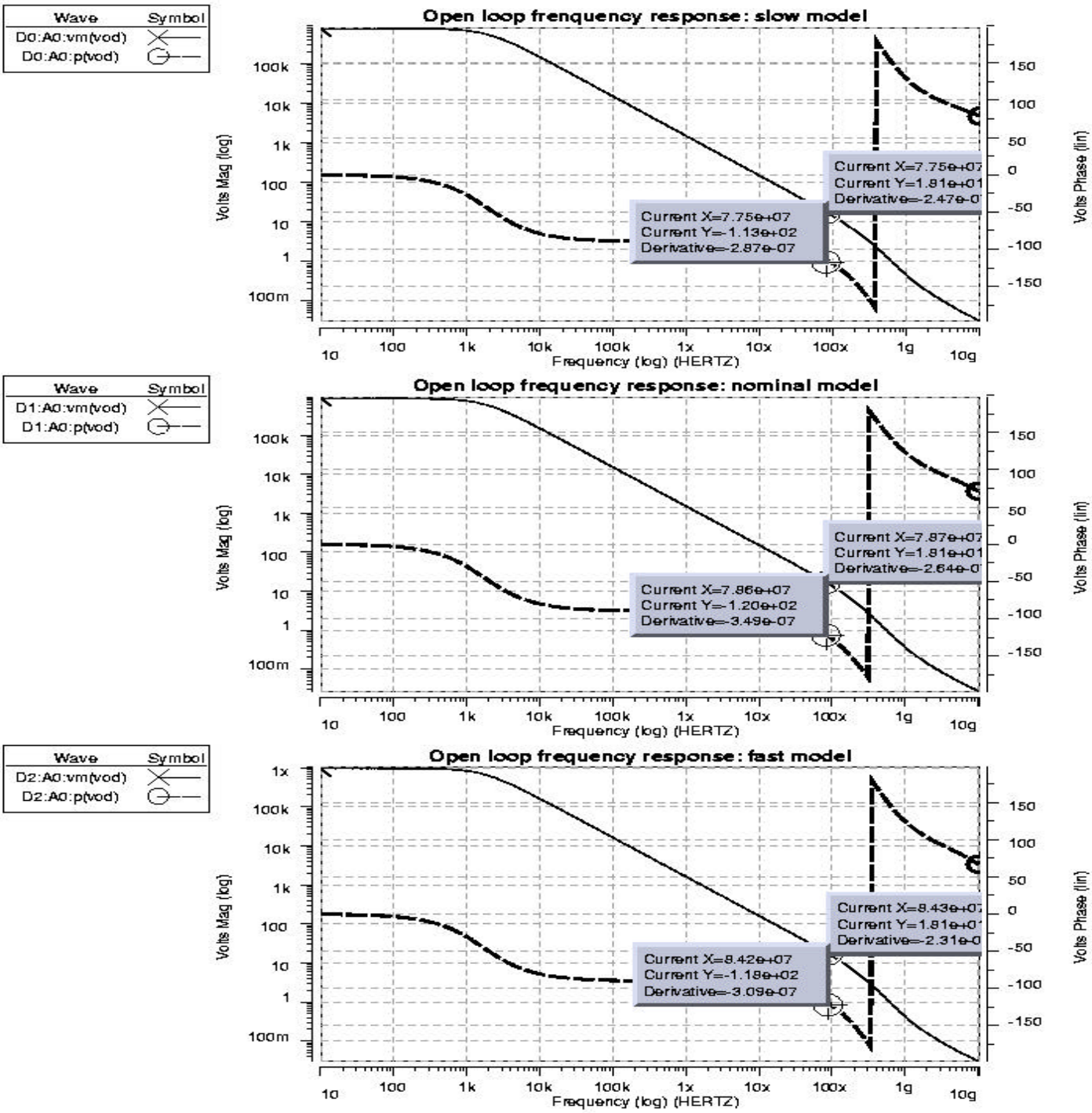
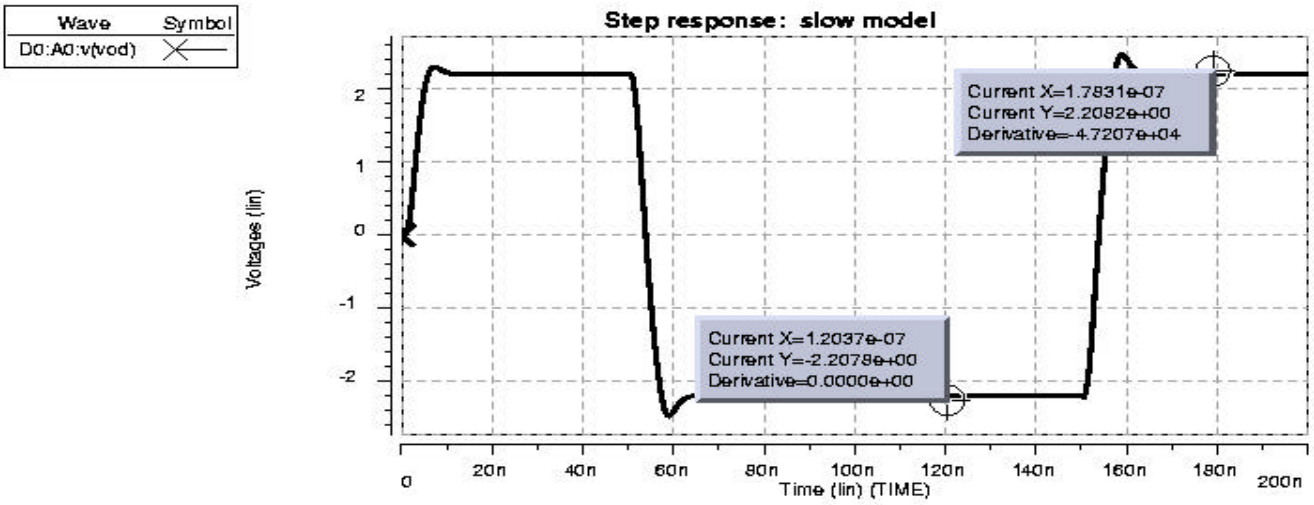
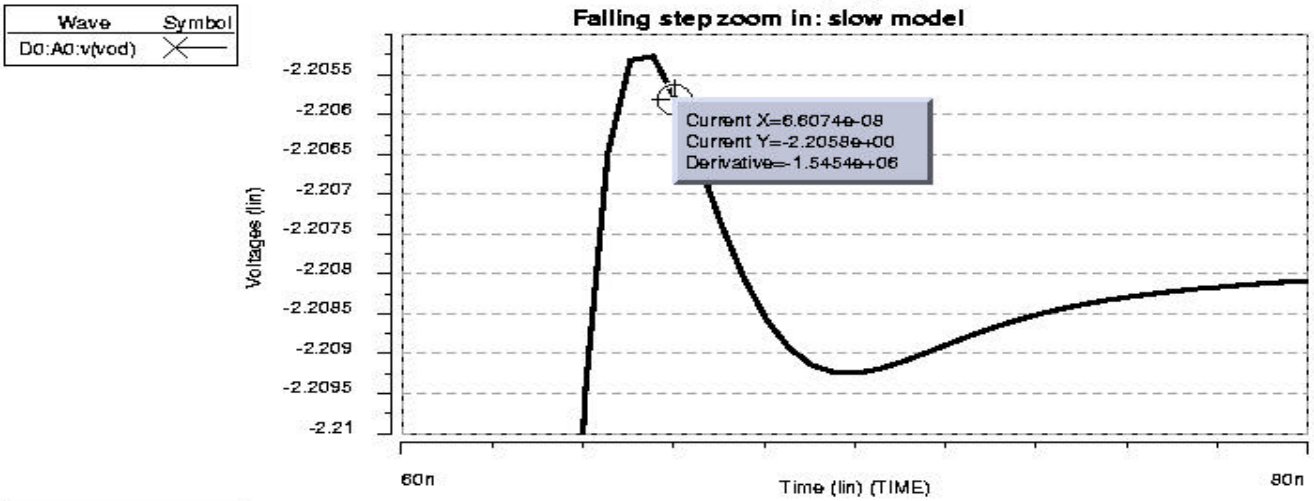


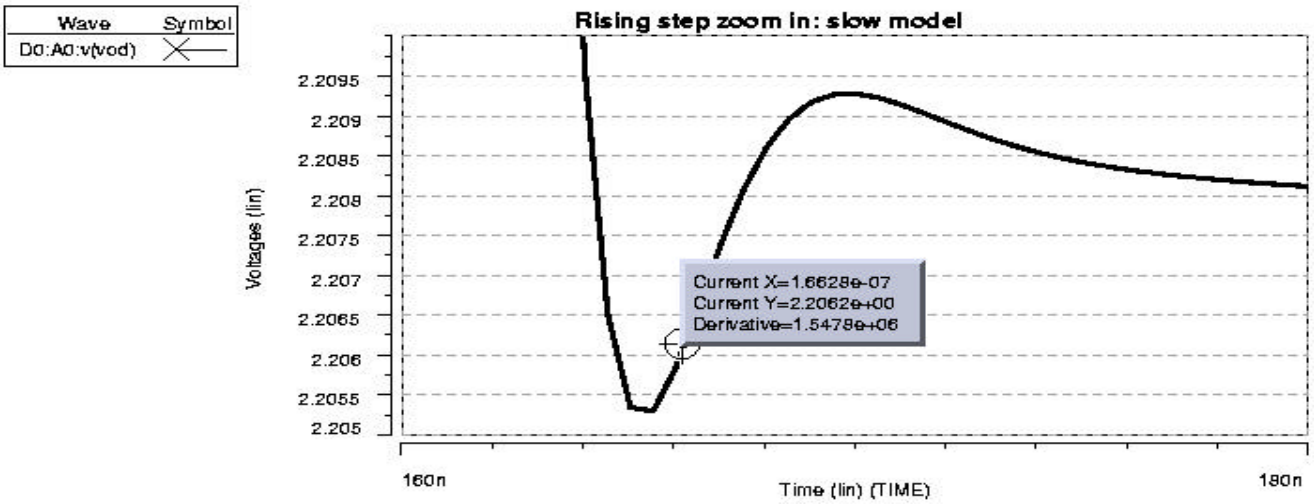
Figure B: noise density and total noise integration

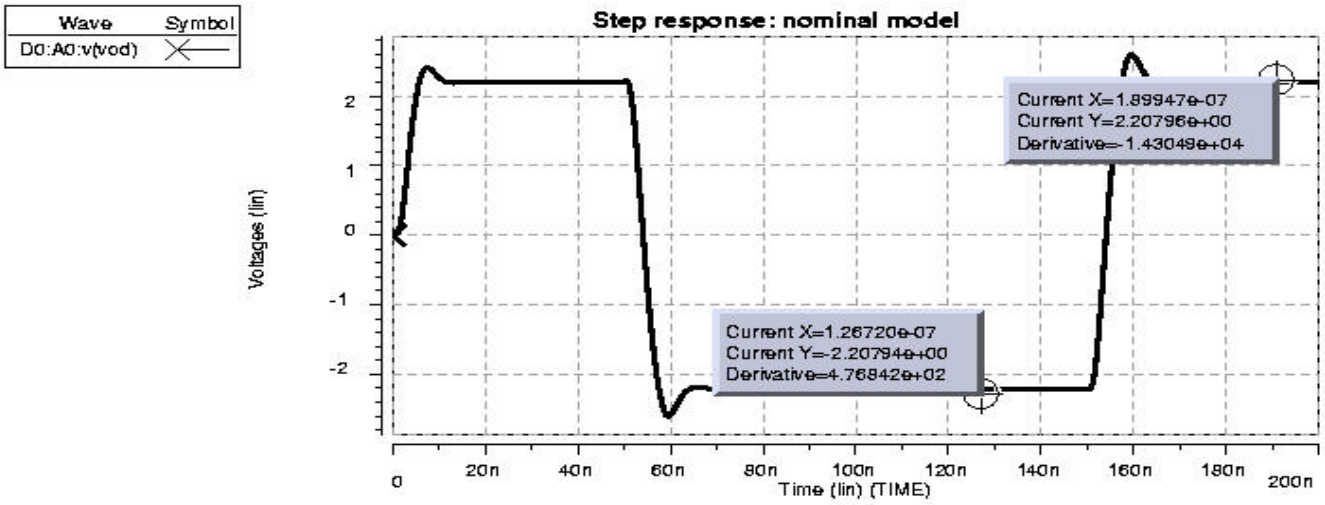
Figure C: Phase margin determination

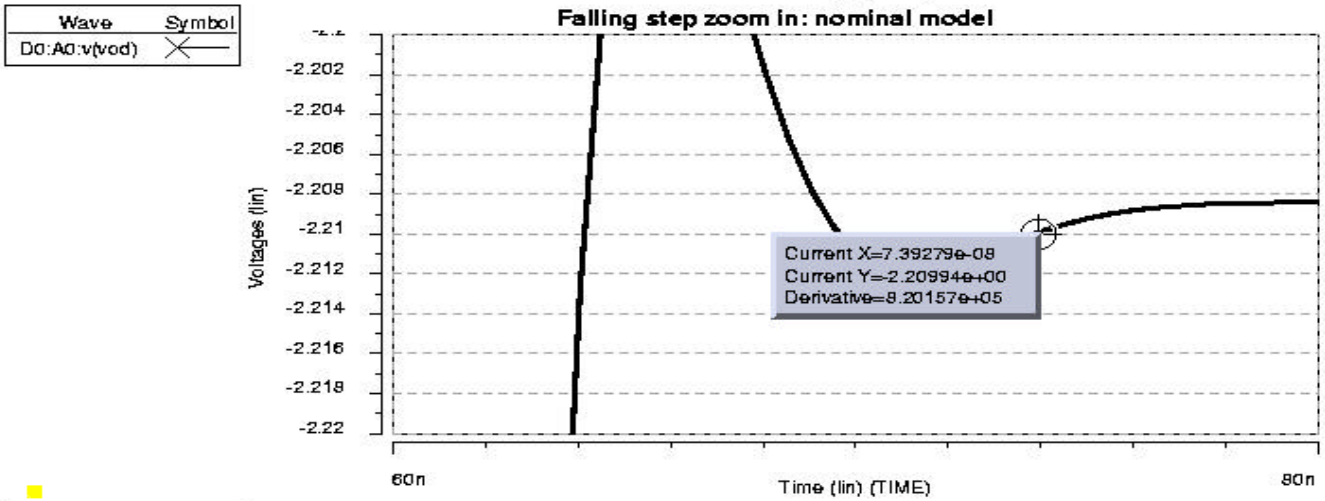


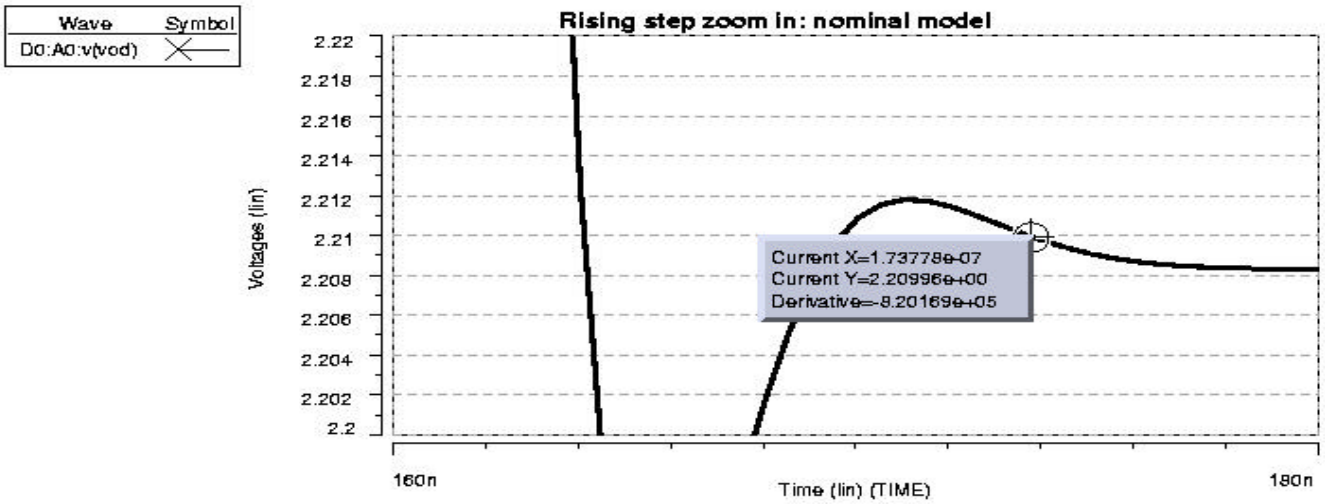

Wave
Symbol
D0:A0:v(vod)
Step response: slow model
Current X=1.7831e-07
Current Y=2.2082e+00
Derivative=-4.7207e+04
Current X=1.2037e-07
Current Y=-2.2078e+00
Derivative=0.0000e+00
Voltagee (lin)
Time (lin) (TIME)
2
1
0
-1
-2
0
20n
40n
60n
80n
100n
120n
140n
160n
180n
200n

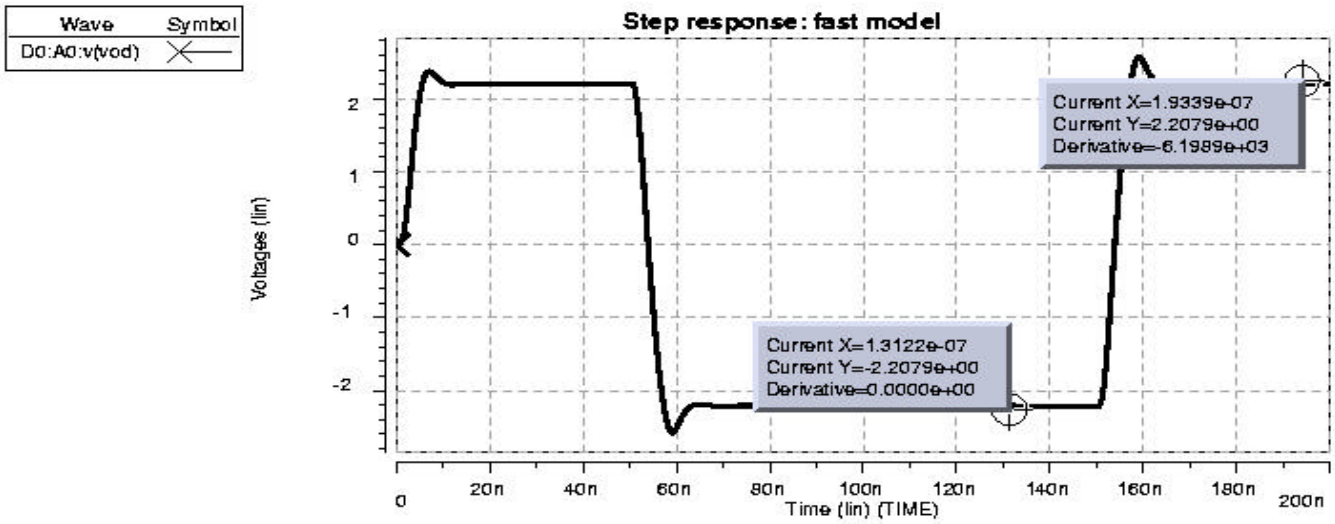

Wave
Symbol
D0:A0:v(vod)
Falling step zoom in: slow model
Current X=6.6074e-08
Current Y=-2.2058e+00
Derivative=-1.5454e+06
Voltagee (lin)
Time (lin) (TIME)
-2.2055
-2.206
-2.2065
-2.207
-2.2075
-2.208
-2.2085
-2.209
-2.2095
-2.21
60n
80n

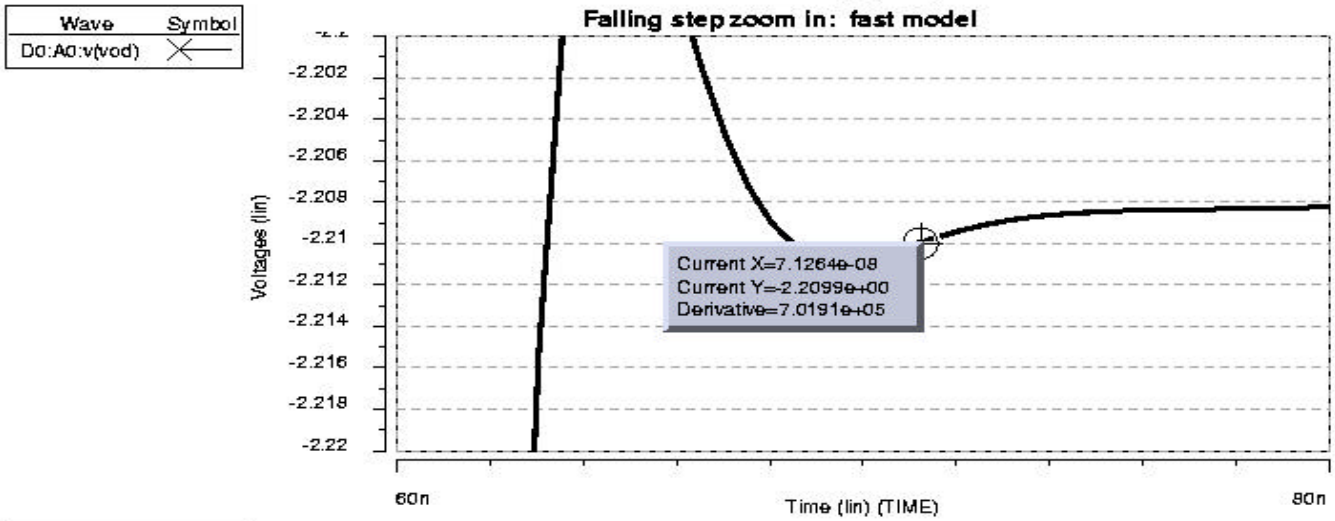

Wave
Symbol
D0:A0:v(vod)
Rising step zoom in: slow model
Current X=1.6628e-07
Current Y=2.2062e+00
Derivative=1.5479e+06
Voltagee (lin)
Time (lin) (TIME)
2.2095
2.209
2.2085
2.208
2.2075
2.207
2.2065
2.206
2.2055
2.205
160n
180n


Wave
Symbol
D0:A0:v(vod)
Step response: nominal model
Current X=1.89947e-07
Current Y=2.20796e+00
Derivative=-1.43049e+04
Current X=1.26720e-07
Current Y=-2.20794e+00
Derivative=4.76842e+02
Voltages (lin)
Time (lin) (TIME)
0
20n
40n
60n
80n
100n
120n
140n
160n
180n
200n
2
1
0
-1
-2


Wave
Symbol
D0:A0:v(vod)
Falling step zoom in: nominal model
Current X=7.39279e-08
Current Y=-2.20994e+00
Derivative=8.20157e+05
Voltages (lin)
Time (lin) (TIME)
60n
80n
-2.202
-2.204
-2.206
-2.208
-2.21
-2.212
-2.214
-2.216
-2.218
-2.22


Wave
Symbol
D0:A0:v(vod)
Rising step zoom in: nominal model
Current X=1.73778e-07
Current Y=2.20996e+00
Derivative=-8.20169e+05
Voltages (lin)
Time (lin) (TIME)
160n
180n
2.22
2.218
2.216
2.214
2.212
2.21
2.208
2.206
2.204
2.202
2.2


Wave
Symbol
D0:A0:v(vod)
Step response: fast model
Current X=1.9339e-07
Current Y=2.2079e+00
Derivative=-6.1989e+03
Current X=1.3122e-07
Current Y=-2.2079e+00
Derivative=0.0000e+00
Voltages (lin)
Time (lin) (TIME)
2
1
0
-1
-2
0
20n
40n
60n
80n
100n
120n
140n
160n
180n
200n


Wave
Symbol
D0:A0:v(vod)
Falling step zoom in: fast model
Current X=7.1264e-08
Current Y=-2.2099e+00
Derivative=7.0191e+05
Voltages (lin)
Time (lin) (TIME)
-2.202
-2.204
-2.206
-2.208
-2.21
-2.212
-2.214
-2.216
-2.218
-2.22
60n
80n

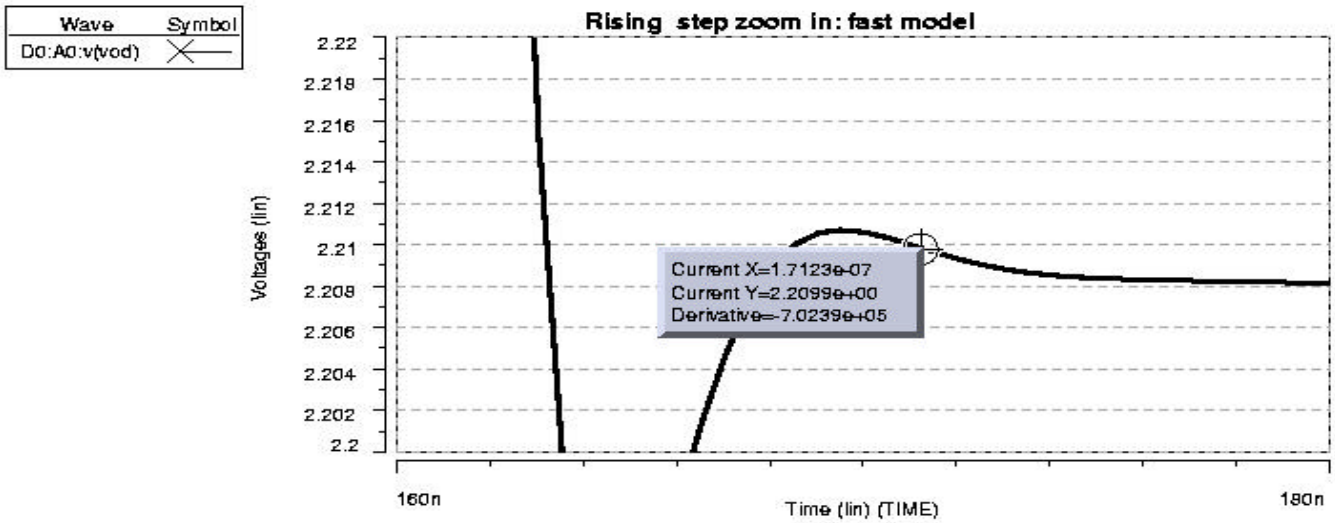
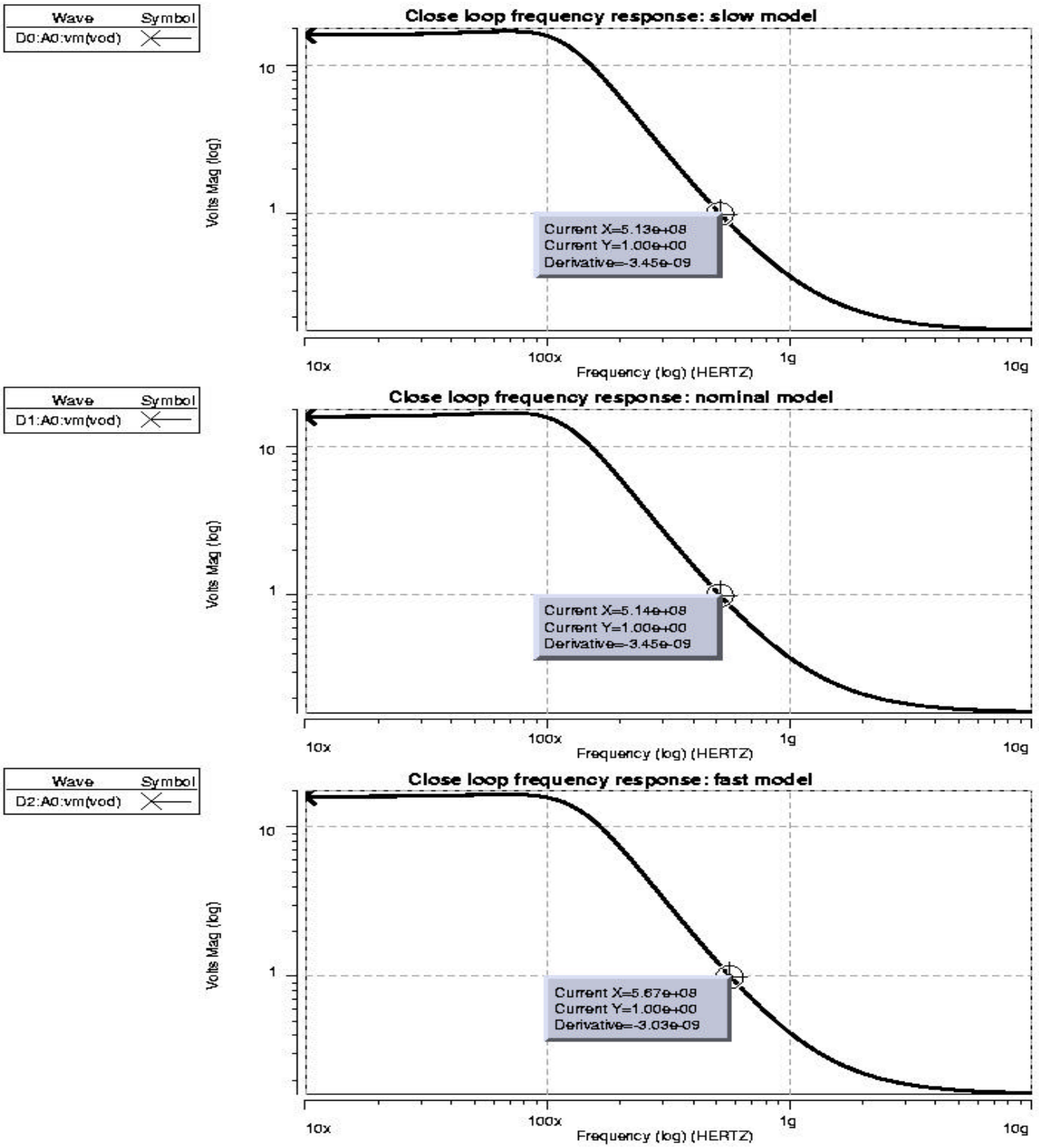

Wave
Symbol
D0:A0:v(vod)
Rising step zoom in: fast model
Current X=1.7123e-07
Current Y=2.2099e+00
Derivative=-7.0239e+05
Voltages (lin)
Time (lin) (TIME)
2.22
2.218
2.216
2.214
2.212
2.21
2.208
2.206
2.204
2.202
2.2
160n
180n

Figure E: close loop frequency response



EE240 Project: Fully-differential OTA

```
*model files
.include 'util.inc.txt'
.option post brief nomod reltol=1e-7
.lib 'cmos35.txt'  fast


*Parameters:
.param wn='266.3u'
.param wn1='200u'
.param ln='0.35u'
.param wp5='1446u'
.param wp7='518.2u'
.param lp='0.35u'
.param wp9='187.2u'
.param wp11='436.1u'
.param wpf='wp7'
.param b='0.667'

*Power supply
vdd vdd 0 3.0

* first stage OTA
x0    vs b00 0 0 ntype l='ln*2' w='wn1'

x1    vc1 vg+ vs 0 ntype l='ln' w='wn'
x2    vc2 vg- vs 0 ntype l='ln' w='wn'

x3    vo1  b3 vc1 0  ntype l='ln*2'  w='wn*2'
x4    vo2  b3 vc2 0  ntype l='ln*2'  w='wn*2'

x5    vo1  b5 vd7 vdd  ptype l='lp*2'  w='wp5'
x6    vo2  b5 vd8 vdd  ptype l='lp*2'  w='wp5'

x7    vd7 b7 vdd vdd  ptype l='lp*2'  w='wp7'
x8    vd8 b7 vdd vdd  ptype l='lp*2'  w='wp7'


* second stage OTA
x9    vout1 vo1 0 0  ntype l='ln*2'  w='wp9*b'
x10   vout2 vo2 0 0  ntype l='ln*2'  w='wp9*b'

x11   vout1 b10 vdd vdd ptype l='lp*3' w='wp11*b'
x12   vout2 b10 vdd vdd ptype l='lp*3' w='wp11*b'


* bias circuit
xb1 b00 b00 0 0  ntype l='ln*2' w='wn1/2.0'
xb2 iss iss b00 0 ntype l='ln*2' w='wn/2.0'
iss vdd iss '0.6m'
```

```
xb3 db3 b00 0 0 ntype l='ln*2' w='wn1/2'
xb4 b5 iss db3 0 ntype l='ln*2' w='wn/2'
xb5 db7 b5 vdd vdd ptype w='wp7*0.085' l='lp*2'
xb6 b5 b5 db7 vdd ptype w='wp5' l='lp*2'
xb7 db11 b00 0 0  ntype l='ln*2' w='wn1/2.0'
xb8 b3 iss db11 0 ntype w='wn/2.0' l='ln*2'
xb9 b3 b3 vdd vdd ptype w='26*lp*2' l='lp*2'
xb10 db14 b00 0 0 ntype l='ln*2' w='wn1'
xb11 b10 iss db14 0 ntype l='ln*2' w='wn1'
xb12 b10 b10 vdd vdd ptype l='lp*3' w='wp11'

* common mode feedback
xcm3  b7 b7 vdd vdd ptype w='wpf'   l='lp*2'
xcm4  node5 node5 vdd vdd ptype w='wpf'  l='lp*2'
xcm1  b7 vcm1  node6 0 ntype w='wpf'  l='ln*2'
xcm2  node5 vref node6 0 ntype w='wpf'  l='ln*2'
xcmc  node6 b00 0 0  ntype w='wn1' l='2*ln'
cfb+  vout1 vcm1 0.01p
cfb-  vout2 vcm1 0.01p
rc1 vout1 vcm1 10000g
rc2 vout2 vcm1 10000g
vref vref 0 dc 1.5v

*Cascade Miller compensation
cc+ vout1 vc1 1.0pF
cc- vout2 vc2 1.0pF

*Ouput Load Capacitors
cl+ vout1 0 0.3pF
cl- vout2 0 0.3pf

*Open loop gain analysis
x13 vid vc vg+ vg- balun
vc vc 0 1.0
vid vid 0 0 ac 1
x100 vod voc vout1 vout2 balun

.op
.dc vid  -30u 30u 1u
.tf v(vod) vid

*Stability analysis and phase margin:
ci+ vg+ 0 6.8pF
ci- vg- 0 6.8pF
co+ vout1 0 0.37647pF
co- vout1 0 0.37647pF

x13 vid vc vg+ vg- balun
vc vc 0 1.0
vid vid 0 0 ac 1
x100 vod voc vout1 vout2 balun
```

```
.ac dec 101 10 10g

*close loop
cf+ vout1 vg- 0.4pF
cf- vout2 vg+ 0.4pF

cs+ vin+ vg+ 6.4pF
cs- vin- vg- 6.4pF

x13 vid vc vin+ vin- balun
x100 vod voc vout1 vout2 balun

rg1 vc vg+ 10000g
rg2 vc vg- 10000g

*close loop freqency response
vc vc 0 1.0
vid vid 0 0 ac 1
.ac dec 101 1 1000g

*Settling analysis
vc vc 0 1.0
vstep vid 0 pwl 0 0 2n 0.138 50n 0.138 52n -0.138 150n -0.138 152n 0.138V 200n 0.138V
.tran 0.1n 200n

*noise analysis
vc vc 0 1.0
vid vid 0 0 ac 1

.ac dec 51 1 1000g
.noise v(vod) vid 10
.probe noise onoise


.end
```