EECS240 – Spring 2010

Lecture 2: CMOS Technology and Passive Devices

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Today's Lecture

- EE240 CMOS Technology
- Passive devices
  - Motivation
  - Resistors
  - Capacitors
  - (Inductors)
- Next time: MOS transistor modeling

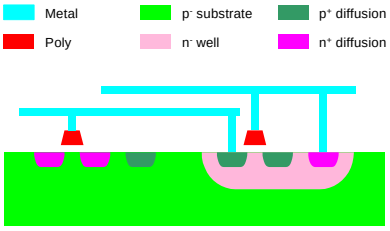
EE240 Process

- 90nm 1P7M CMOS
  - Minimum channel length: 90nm
  - 1 level of polysilicon
  - 7 levels of metal (Cu)
  - 1.2V supply
  - Models for this process not "real"
- Other processes you might see
  - Shorter channel length (45nm / 1V)
  - Bipolar, SiGe HBT
  - SOI

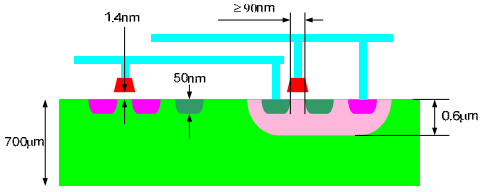
Process Options

- Available for many processes
- Add features to "baseline process"
- E.g.
  - Silicide block option
  - "High voltage" devices (2.5V & 3.3V, >10V)
  - Low V_{TH} devices
  - Capacitor option (2 level poly, MIM)
  - …

CMOS Cross Section



Dimensions



Why Talk About Passives?

Resistors

- No provisions in standard CMOS
- Resistors are bad for digital circuits →
  - Minimized in standard CMOS
  - But, often want big, well-controlled R for analog…
- Sheet resistance of available layers:

Layer	Sheet resistance
Aluminum	60 mΩ/□
Polysilicon	5 Ω/□
N+/P+ diffusion	5 Ω/□
N-well	1 kΩ/□

How about an N-Well Resistor?

Silicide Block Option

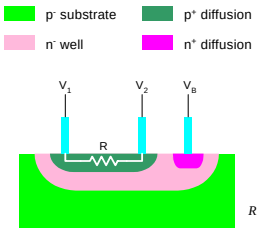
Layer	R/□ [Ω/□]	T_C [ppm/°C] @ T = 25 °C	V_C [ppm/V]	B_C [ppm/V]
N+ poly	100	-800	50	50
P+ poly	180	200	50	50
N+ diffusion	50	1500	500	-500
P+ diffusion	100	1600	500	-500
N-well	1000	-1500	20,000	30,000

- Non-silicided layers have significantly larger sheet resistance
- Even with silicide block, many non-idealities:
  - Temperature coefficient: R = f(T)
  - Voltage coefficient: R = f(V)
  - Manufacturing Variations

Resistor Temp-Co. Example

Voltage Dependence

Voltage Coefficient



Example:
Diffusion resistor

→ **Applied voltage modulates depletion width (cross-section of conductive channel)**

→ **Well acts as a shield**

$$R = \frac{V_1 - V_2}{I}$$
$$\approx R_0\left[1 + T_C\left(T - 25^\circ\right) + V_C\left(V_1 - V_2\right) + B_C\left(\frac{V_1 + V_2}{2} - V_B\right)\right]$$

Compensation

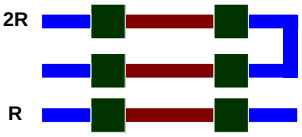
Resistor Matching

- **Types of mismatch:**
  - **Run-to-run variations**
    - **Global differences in thickness, doping, etc.**
  - **Systematic (e.g. contacts)**
  - **Random variations between devices**
- **Run-to-run variations in absolute R value: 20+%**
  - **Can be problematic for termination, bias current, etc.**
- **Best case: make circuit depend only on ratios**
  - **E.g., use feedback to control opamp gain**
  - **With careful layout, can get 0.1 – 1% matching**

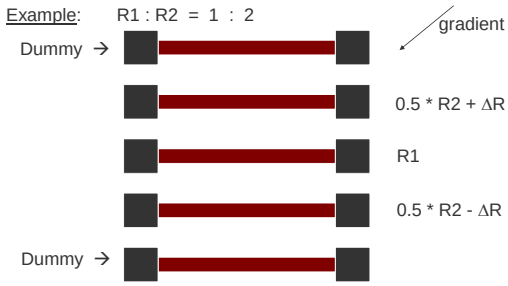
Systematic Variations from Layout

- **Example:**

- **Use unit element instead:**

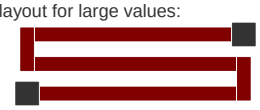


Common Centroid and Dummies

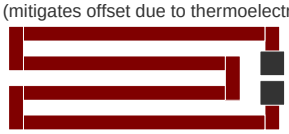


Resistor Layout (cont.)

Serpentine layout for large values:



Better layout (mitigates offset due to thermoelectric effects):



See Hastings, "The art of analog layout," Prentice Hall, 2001.

MOSFETs as Resistors

- **Triode region ("square law"):**

$$I_D = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS} \qquad \text{for} \quad V_{GS} - V_{TH} > V_{DS}$$

- **Small signal resistance:**

$$\frac{1}{R} = \frac{\partial I_D}{\partial V_{DS}} = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH} - V_{DS}\right)$$

$$R \approx \frac{1}{\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)} \qquad \text{for} \quad V_{GS} - V_{TH} >> V_{DS}$$

- **Voltage coefficient:**

$$V_C = \frac{1}{R}\frac{\partial R}{\partial V_{DS}} = \frac{1}{V_{GS} - V_{TH} - V_{DS}}$$

MOS Resistors

Example: R = 1 MΩ

$$R \approx \frac{1}{\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)}$$

$$\frac{W}{L} = \frac{1}{\mu C_{ox} R\left(V_{GS} - V_{TH}\right)}$$

$$= \frac{1}{100\frac{\mu A}{V^2} \times 1\text{M}\Omega \times 2\text{V}} = \frac{1}{200}$$

$$V_C\Big|_{V_{GS}-V_{TH}=0V} = \frac{1}{V_{GS} - V_{TH}}$$

$$= \frac{1}{2\text{V}} = 0.5\text{V}^{-1}$$

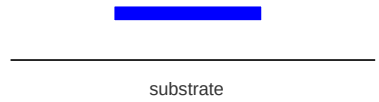
- **Large R-values realizable in small area**
- **Very large voltage coefficient**
- **Applications:**
  - ***MOSFET-C filters: (linearization)***
    Ref: Tsividis et al, "Continuous-Time MOSFET-C Filters in VLSI," JSSC, pp. 15-30, Feb. 1986.
  - ***Biasing: (>1GΩ)***
    Ref: Geen et al, "Single-Chip Surface-Micromachined Integrated Gyroscope with 50º/hour Root Allen Variance," ISSCC, pp. 426-7, Feb. 2002.

Resistor Summary

- **No or limited support in standard CMOS**
  - **Large area (compared to FETs)**
  - **Nonidealities:**
    - **Large run-to-run variations**
    - **Temperature coefficient**
    - **Voltage coefficients (nonlinear)**
- **Avoid them when you can**
  - **Especially in critical areas, e.g.**
    - **Amplifier feedback networks**
    - **Electronic filters**
    - **A/D converters**
  - **We will get back to this point**

Capacitors

- **Simplest capacitor:**



- **What's the problem with this?**

Capacitors

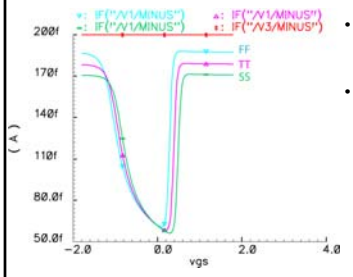
- **"Improved" capacitor:**

- **Is this only 1 capacitor?**

Capacitor Options

Type	C [aF/μm²]	V_C [ppm/V]	T_C [ppm/ºC]
Gate	10,000	Huge	Big
Poly-poly (option)	1000	10	25
Metal-metal	50	20	30
Metal-substrate	30		
Metal-poly	50		
Poly-substrate	120		
Junction caps	~ 1000	Big	Big

MOS Capacitor



- High non-linearity, temperature coefficient
- But, still useful in many applications, e.g.:
  - (Miller) compensation capacitor
  - Bypass capacitor (supply, bias)

Capacitor Layout

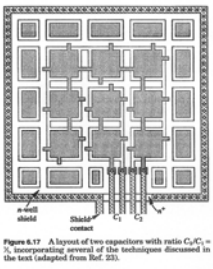


Figure 6.17 A layout of two capacitors with ratio $C_2/C_1 = \frac{1}{3}$, incorporating several of the techniques discussed in the text (adapted from Ref. 23).

- Unit elements
- Shields:
  - Etching
  - Fringing fields
- "Common-centroid"
- Wiring and interconnect parasitics

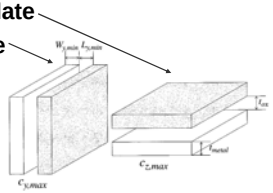
Ref.: Y. Tsividis, "Mixed Analog-Digital VLSI Design and Technology," McGraw-Hill, 1996.

MIM Capacitors

- Some processes have MIM cap as add-on option
  - Separation between metals is much thinner
  - Higher density
- Used to be fairly popular
  - But not as popular now that have many metal layers anyways

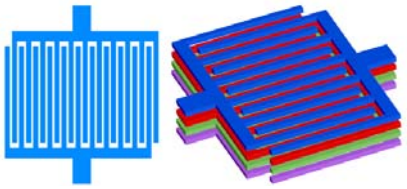
Capacitor Geometries

- Horizontal parallel plate
- Vertical parallel plate
- Combinations



Ref: R. Aparicio and A. Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors," JSSC March 2002, pp. 384-393.

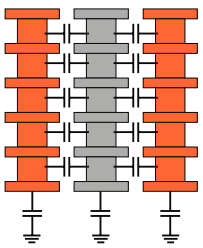
"MOM" Capacitors



- Metal-Oxide-Metal capacitor. Free with modern CMOS.
- Use lateral flux (~L_{min}) and multiple metal layers to realize high capacitance values

MOM Capacitor Cross Section

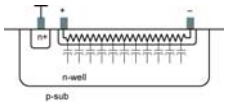
- Use a wall of metal and vias to realize high density
- More layers – higher density
  - May want to chop off lower layers to reduce C_{bot}
- Reasonably good matching and accuracy



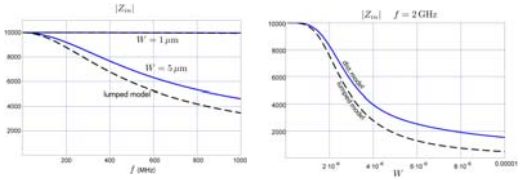
Distributed Effects

- Can model IC resistors as distributed RC circuits.
- Could use transmission line analysis to find equivalent 2-port parameters.
- Inductance negligible for small IC structures up to ~10GHz.

$$R \gg \omega L$$

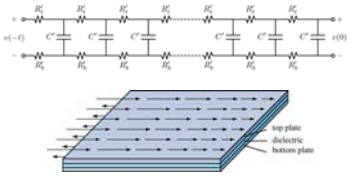


Effective Resistance



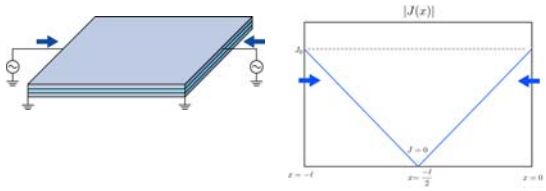
- High frequency resistance depends on W, e.g.:
  - W=1μ 10kΩ resistor works fine at 1GHz
  - W=5μ 10kΩ resistor drops to 5kΩ at 1 GHz
- May need distributed model for accurate freq response

Capacitor Q



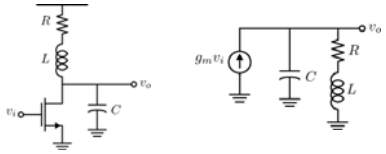
- Current density drops as you go farther from contact edge…

Double Contact Strucutre



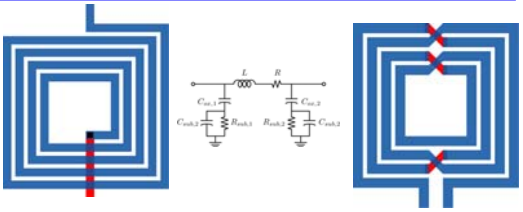
- If contact on both edges,
  - R drops 4X
  - Can be a good idea even if not hitting distributed effects

What About Inductors?



- Mostly not used in analog/mixed-signal design
  - Usually too big
  - More of a pain to model than R's and C's
  - But they do occasionally get used
- Example inductor app.: shunt peaking
  - Can boost bandwidth by up to 85%!
  - Q not that important (L in series with R)
  - But frequency response may not be flat

Spiral Inductors



- Used widely in RF circuits for small L (~1-10nH).
- Use top metal for Q and high self resonance frequencies.
  - Very good matching and accuracy – if you model them right