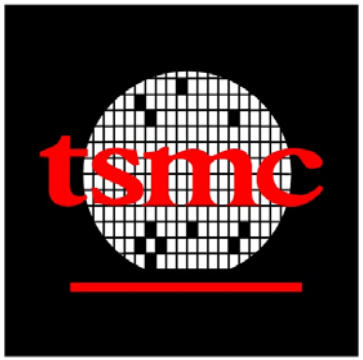

TSMC PDK RF Flow Guide:
A Low-Noise Amplifier (LNA) Design Flow Example of TSMC CRN90LP Process Design Kits (PDK)

DSDAD

Ver 0.2a

Apr. 2004

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Introduction

The major purpose of this user guide is to introduce the basic usage of a TSMC's PDK for those users who are completely new to TSMC PDK or never use TSMC's PDKs before as a reference. To ease the overall introduction, we use a simple LNA design as an example to go through the whole design flow: starting from the schematic capture and ending at the physical verification and post-layout simulation. We divide the whole flow into several phases below:

Schematic Capture

- **Environment setup**
- **Creating a library, design, symbol and test fixture**

Pre-layout Simulation

- **Using Spectre simulator**
- **LNA performance, corner, Monte Carlo**

Layout Creation

- **Schematic-drive-layout**
- **Components placement**
- **Manual routing**

Physical Verification

- **Assura flow**
- **Calibre flow**

Post-layout Simulation

- **Assura flow**
- **Calibre flow**

Contents

Schematic Capture

After you have finished the installation of the TSMC's PDK, we will start to create a new design based on the installed PDK

- **Environment setup**
- **Creating a library**
- **Creating a design**
- **Creating a symbol**
- **Creating a test fixture**

Environment setup

Before we start to create a new design, some environment setups should be done. First, we have to set the environment variable of “CDS_Netlisting_Mode” to “Analog”. This can be archived by the following UNIX command:

setenv CDS_Netlisting_Mode “Analog”

Then, go to the demo directory and enter Cadence environment by:

% cd <pdk_install_directory> /RF_flow
% icfb &

Note:

1. The installation procedures of the TSMC’s PDK can be found in the document of “TSMC PDK reference manual ” released along with the corresponding PDK.
2. The <pdk_install_directory> is referred to the path where the TSMC’s PDK was installed.

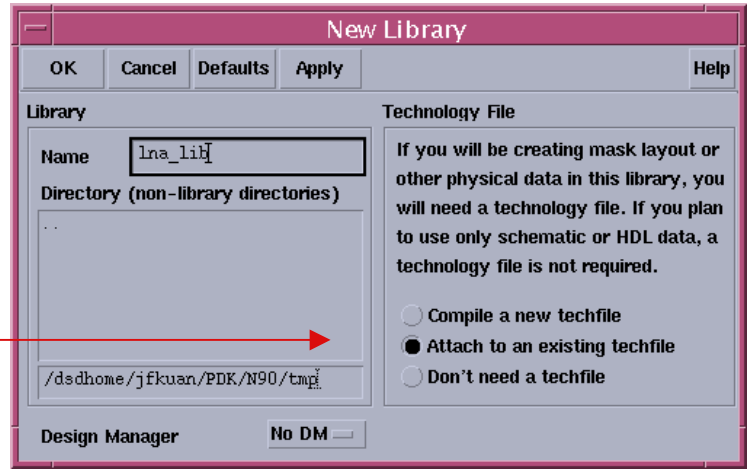
Creating a library

After completing the environment setup, we can start to create a new library.

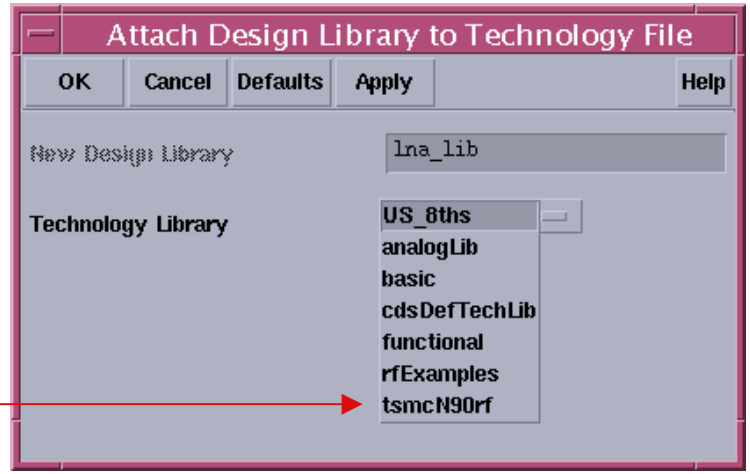
1. In the CIW, select “File->New->Library

Enter the new library name into the Name field

Select “Attach to an existing techfile”



2. In the Attach Design Library to Technology File form, select “tsmcN90rf”, then click OK.



Creating a design

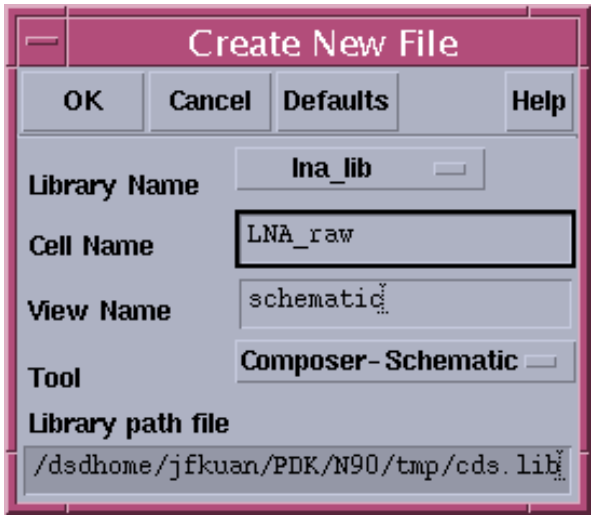
Creating a Schematic Cellview

1. In the CIW or Library Manger, select File->New->Cellview.

2.Set up the Create New File as follows:

Enter the new cell name into the Name field →

Select “Composer-Schematic” →

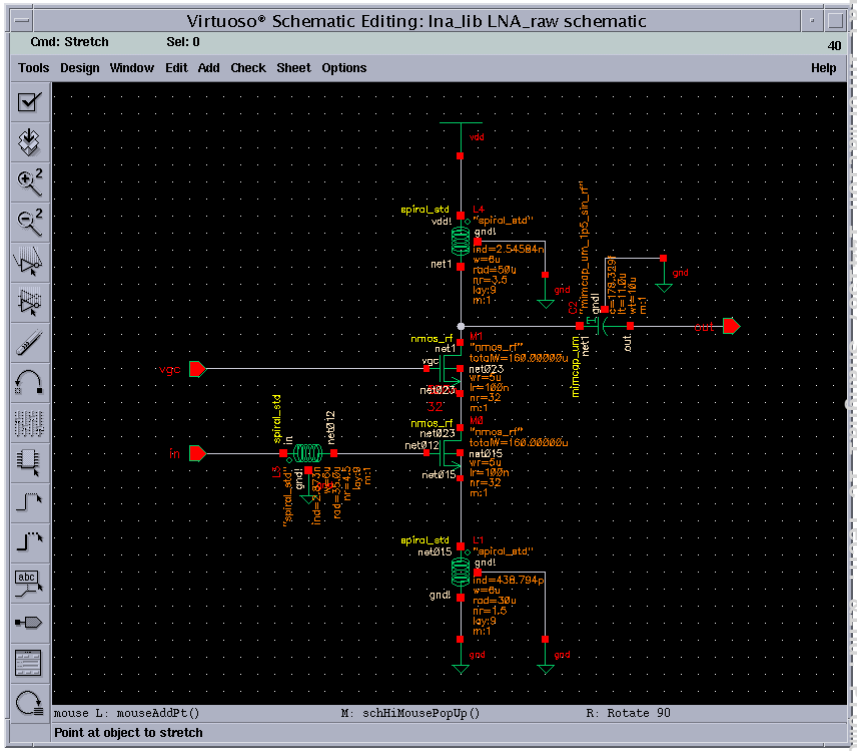


3. Click OK when done.

Creating a design

Adding Components to a Schematic

Build the lna_raw schematic shown below:



1. In the ***LNA_raw*** schematic window, click the **Instance** fixed menu icon to display the Add Instance form.

2. Make sure that the View Name field in the form is set to symbol. You will update the Library Name, Cell Name, and the property values given in the table as you place each component.

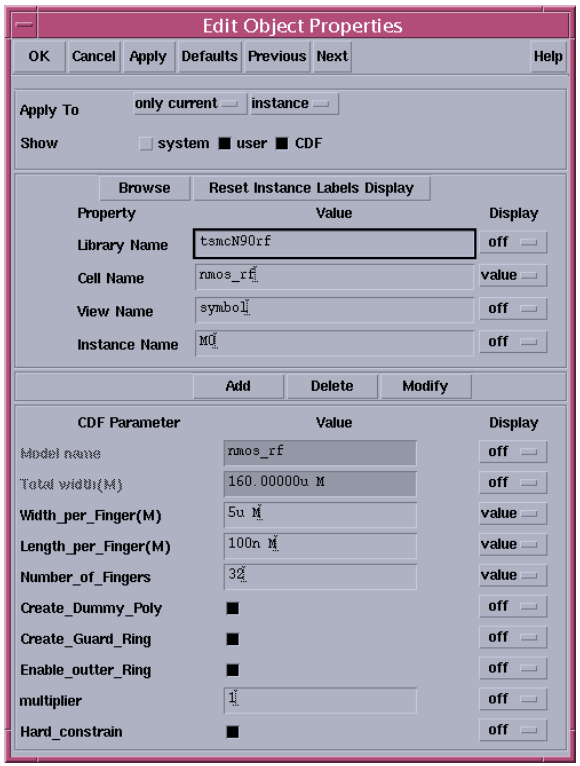
3. After you complete the Add Instance form, move your cursor to the schematic window and click **left** to place a component.

Another way to fill in the Add Instance form is to click on the **Browse** button. This button opens up a Library Browser from which you can select components to place your **left** mouse button.

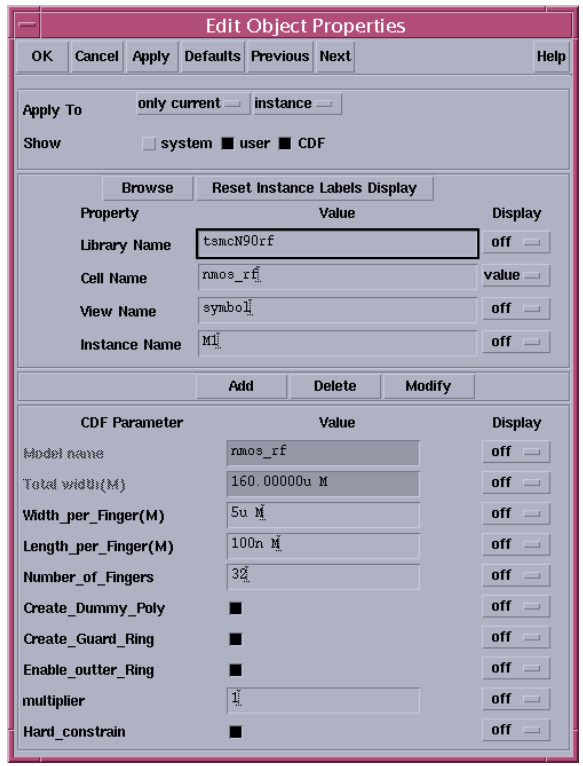
Library Name	Cell Name	Properties/comments
tsmcN90rf	nmos_rf	For M0: Model = "nmos_rf", wr=5u, lr=100n, nr=32,m=1
tsmcN90rf	nmos_rf	For M1: Model = "nmos_rf", wr=5u, lr=100n, nr=32,m=1
tsmcN90rf	spiral_std	For L1 : Model = "spiral_std", w=6u, rad=30u, nr=1.5, lay=9, m=1
tsmcN90rf	spiral_std	For L3 : Model = "spiral_std", w= 6u, rad=35u, nr=4.5, lay=9, m=1
tsmcN90rf	spiral_std	For L4 : Model = "spiral_std", w= 6u, rad=50u, nr=3.5, lay=9, m=1
tsmcN90rf	mimcap_um	For C2 : Model= "mimcap_um_1p5_sin_rf", lt =11u, wt=10u, m=1

Creating a design

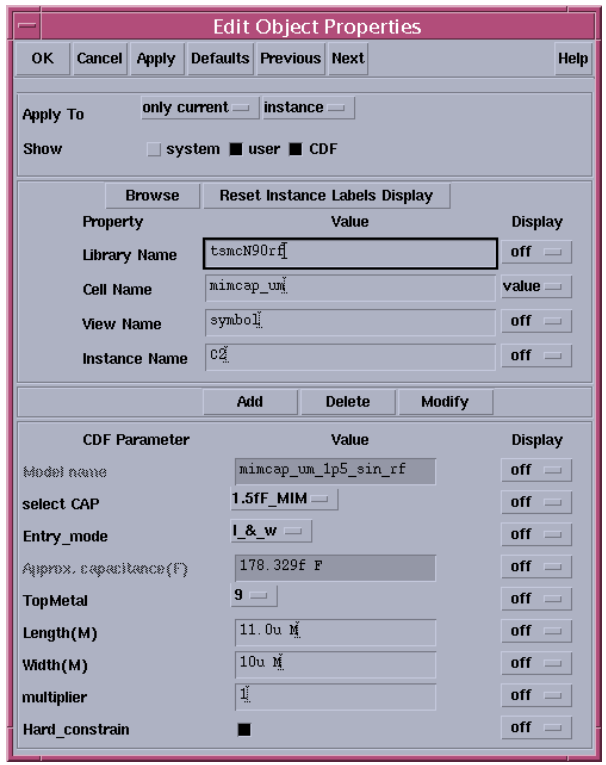
If you place a component with wrong parameter values, you can use the Edit->Properties->Objects command to change the parameters.
The properties of M0, M1, C2, L1, L3 and L4 should be made sure as follows:



M0

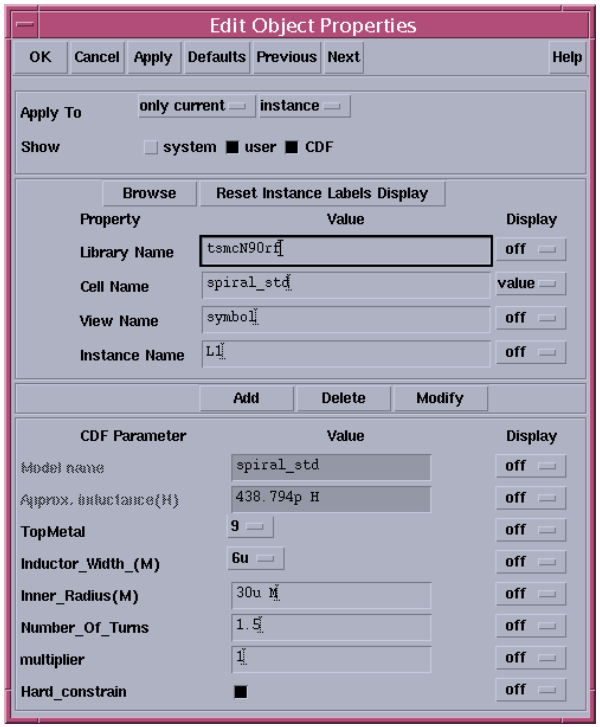


M1

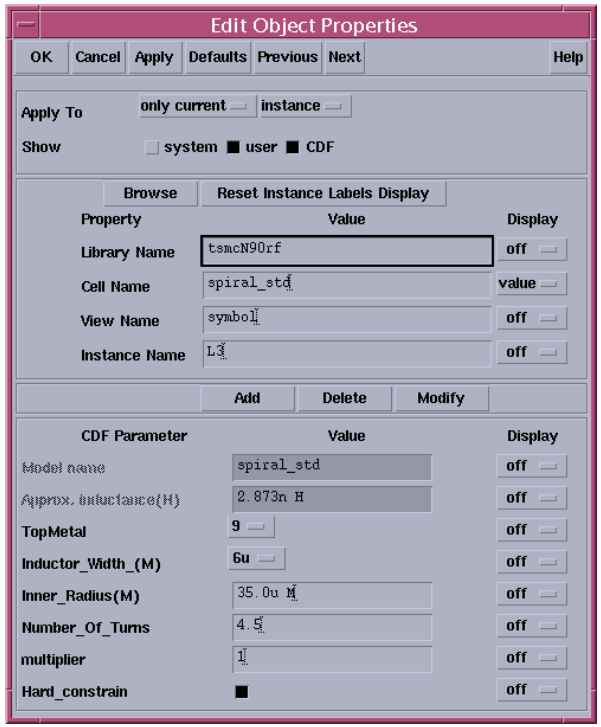


C2

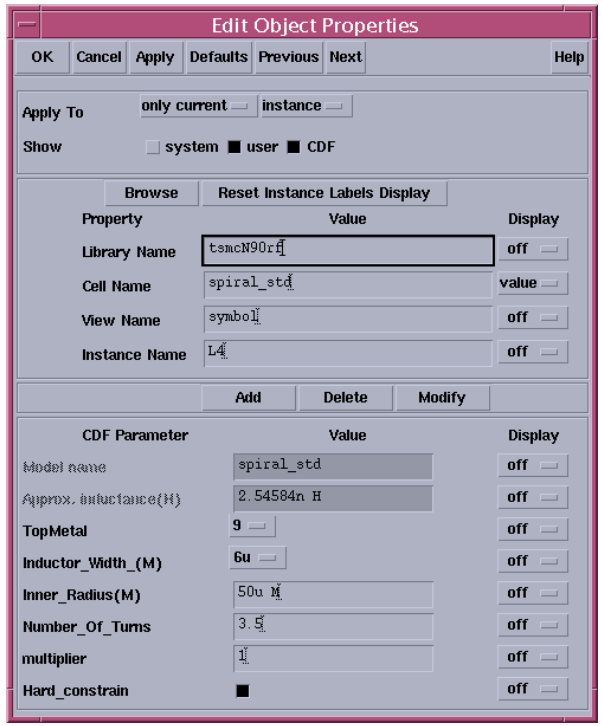
Creating a design



L1



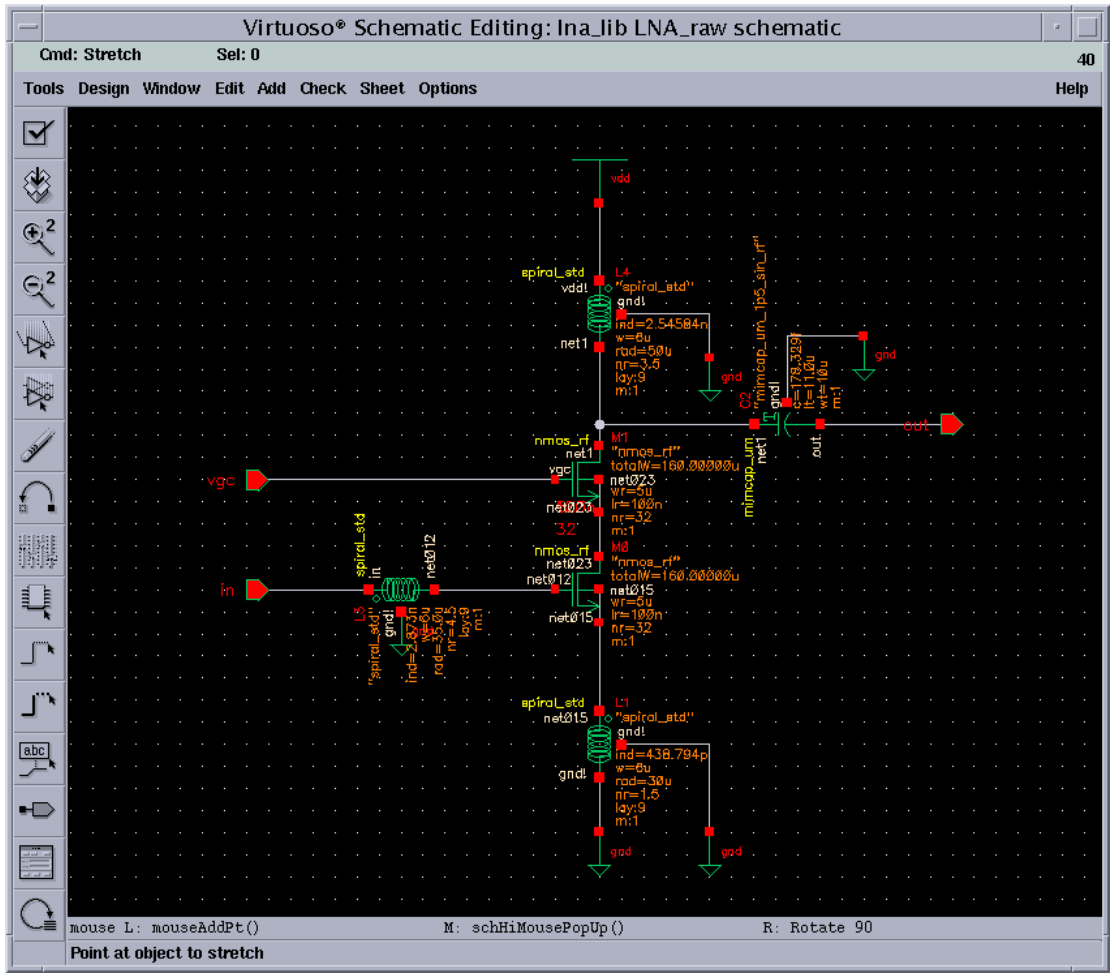
L3



L4

Creating a design

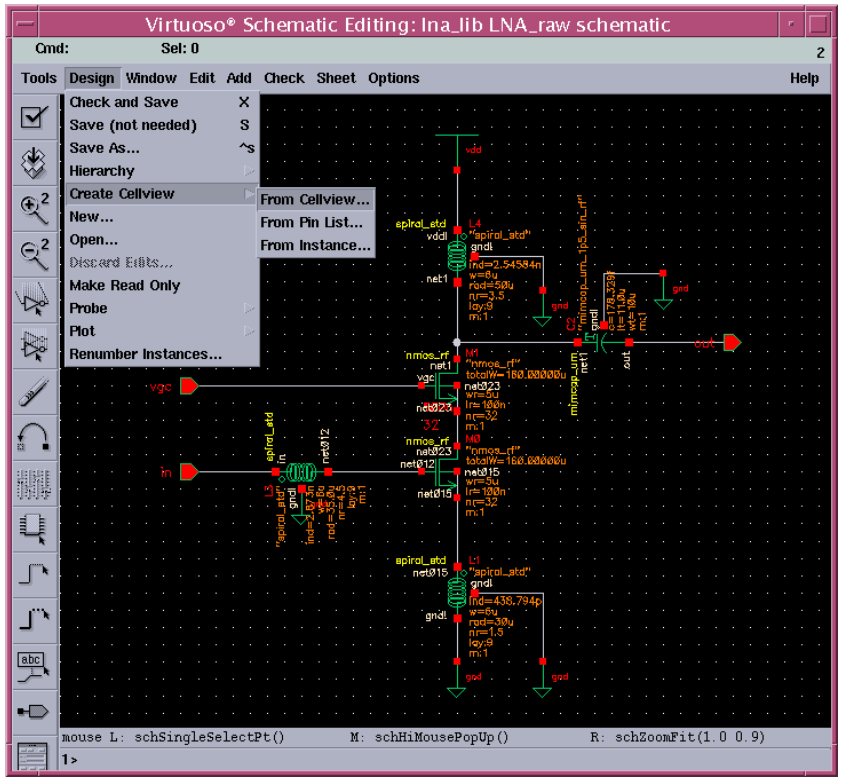
After entering components, add vdd, gnd,(from analogLib) Pins and wires to the schematic as follows:



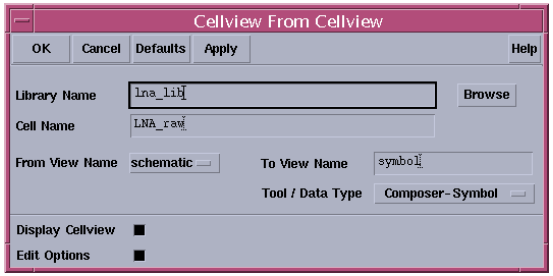
Creating a symbol

After completing the creation of schematic-capture, we have to create its corresponding symbol for the subsequence simulation steps.

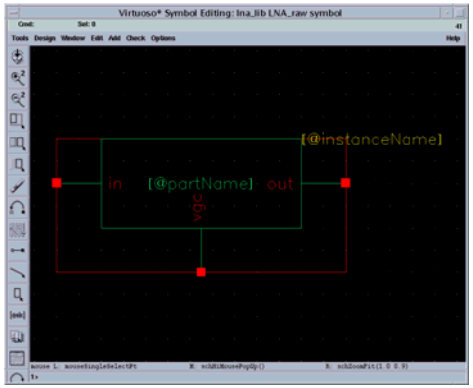
1. In the ***LNA_raw*** schematic window, select Design->Create Cellview->From Cellviw



2. Setup the Cellview From Cellview window as follows:



3. Click OK then the symbol view is created.



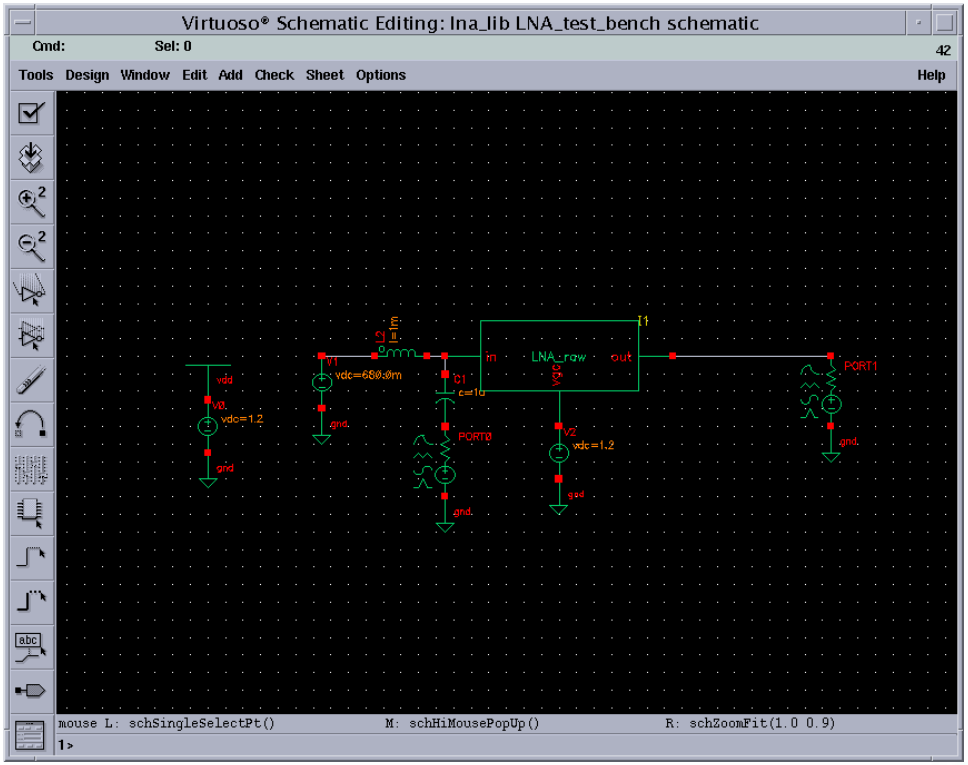
The symbo view

Creating a test fixture

The final step before we start the simulation is to create a test fixture for our design. The creation of test fixture is similar to the creation of a design. Furthermore, you also have to prepare the component table shown below to build the test fixture schematic.Generally, a test fixture will consist of the following components: a core design (the LNA_raw in our case), DC voltage source, ground, vdd, port, DC blocking capacitor and RF choke inductor. The test fixture that we used for our design namely “LNA_test_bench” is shown below:

Library Name	Cell Name	Properties/comments
analogLib	vdd	
analogLib	gnd	
analogLib	vdc	For vin : DC voltage =0.68 V
analogLib	vdc	For vgc : DC voltage =1.2 V
analogLib	vdc	For vdd : DC voltage =1.2 V
analogLib	port	For PORT0 : Resistance = 50 ohm
analogLib	port	For PORT1 : Resistance = 50 ohm
analogLib	ind	For L2 : L= 1m H
analogLib	cap	For C1 : C=1u F
lna_lib	LNA_raw	core design

Component table



LNA test bench

Contents

Pre-layout Simulation

After completing schematic capture, we have to verify the electrical performance and the functionality of our design using a simulation tool. In this chapter, we will use Spectre as simulators.

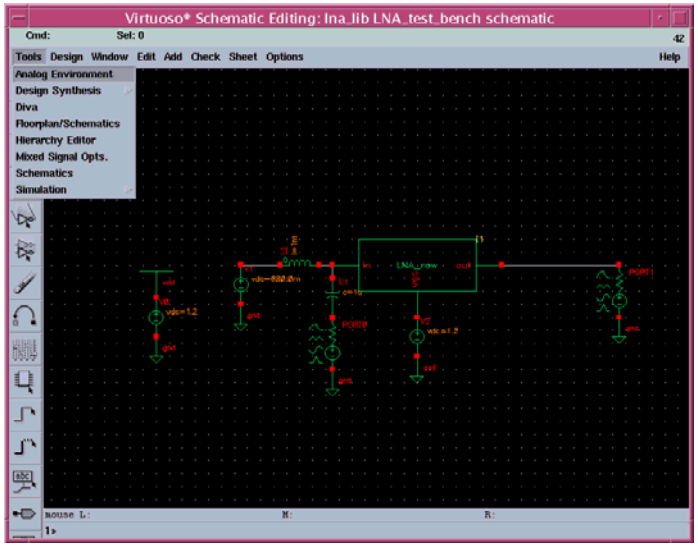
- **Using Spectre simulator**
- **LNA performance**
- **Corner simulation**
- **Monte Carlo (process) simulation**

Using Spectre simulator

In this section, we will start to simulate our design with spectre simulator under Analog Artist environment . The simulation steps of Spectre simulator are listed below :

1. Open Analog Artist window

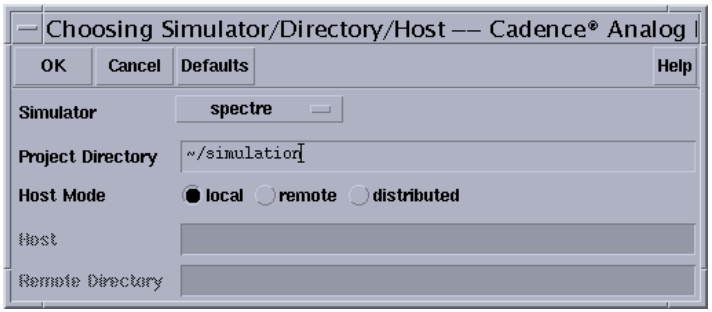
This can be archived by “Tools->Analog environment” in the menu banner of “LNA_test_bench” schematic view

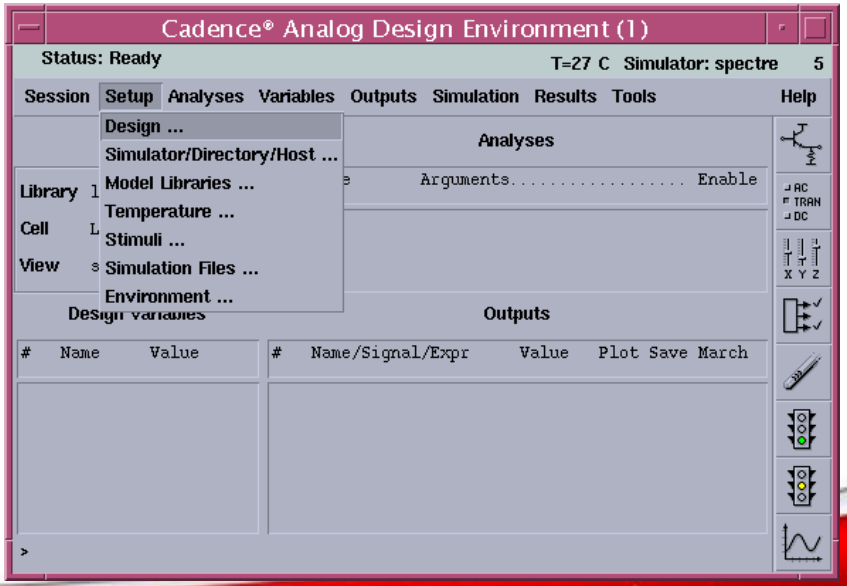


2. Select Simulator

In the Analog Artist window, select Setup->Simulator/Directory/Host.

Set Simulator to **spectre** and specify the “Project Directory”





Using Spectre simulator

3. Model Library Setup

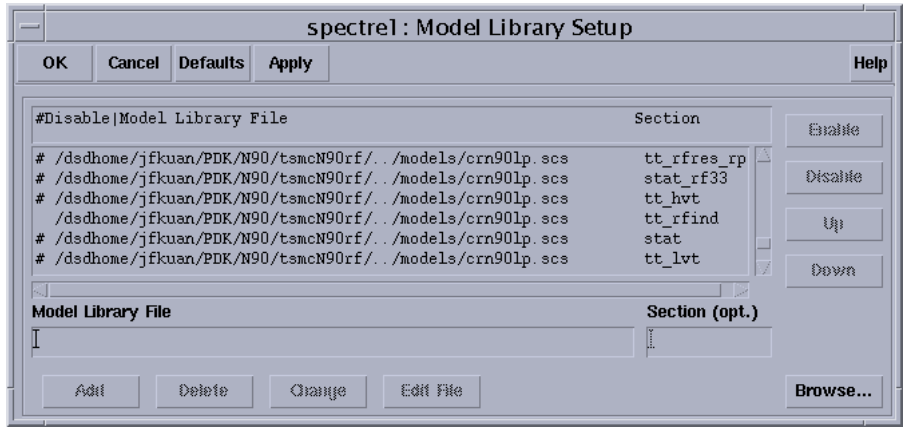
In the Analog Artist window, select Setup->Model Library.

In this case, below three section should be enabled

crn90lp.scs tt_rfmos

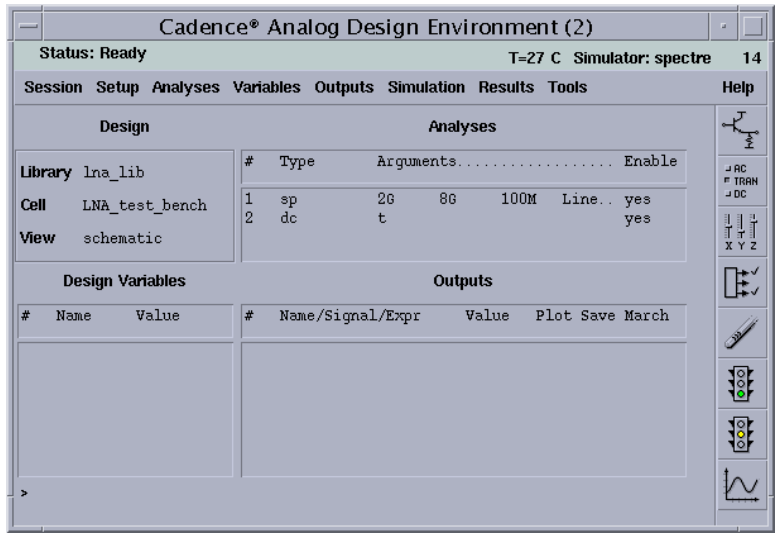
crn90lp.scs tt_rfind

crn90lp.scs tt_rfmim



4. Select analysis type and fill in parameters for simulation

In the Analog Artist window, there are many analysis options that you can choose. Since we want to analysis the S-parameter of our design, we choose the sp analysis for our design. Some designers may want to see the OP point and they can also include the DC op point analysis



Using Spectre simulator

5. Setup of sp analysis

In the Analysis section, select **sp.**

In the S-parameter Analysis section , click on the Select button, and select the ports of interest in schematic: **PORT0** and **PORT1** are selected in this case.

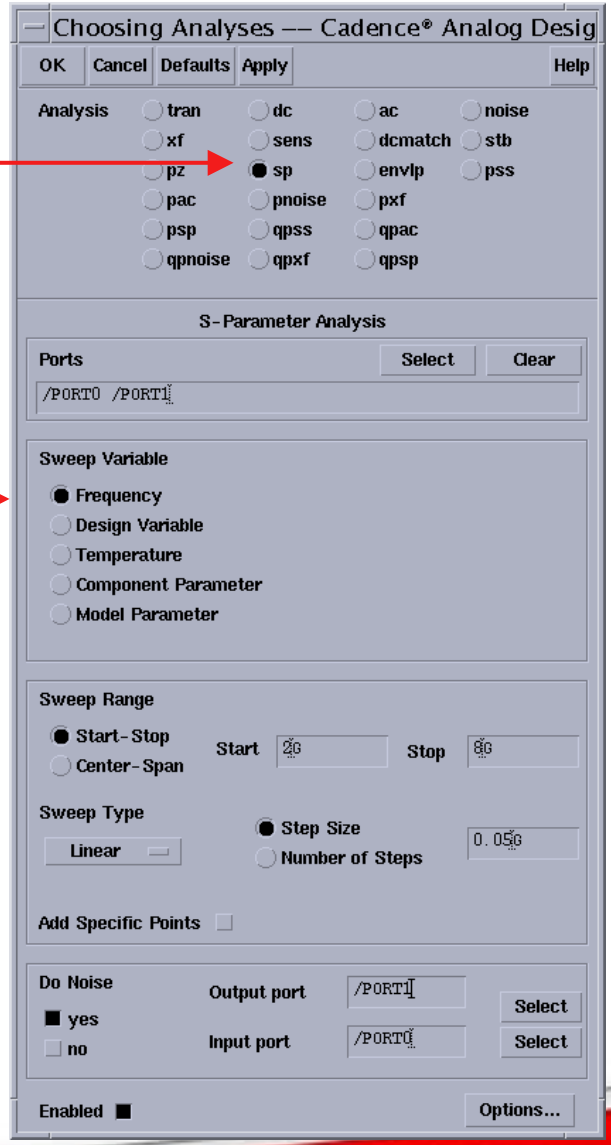
Set the Sweep Variable to **Frequency**

Set Start to **2G** and stop to **8G**

Set the sweep type to **Linear** with Step Size set to **0.05G**

Set **yes** to do noise simulation and select PORT1 as output port and PORT0 as input port in this case

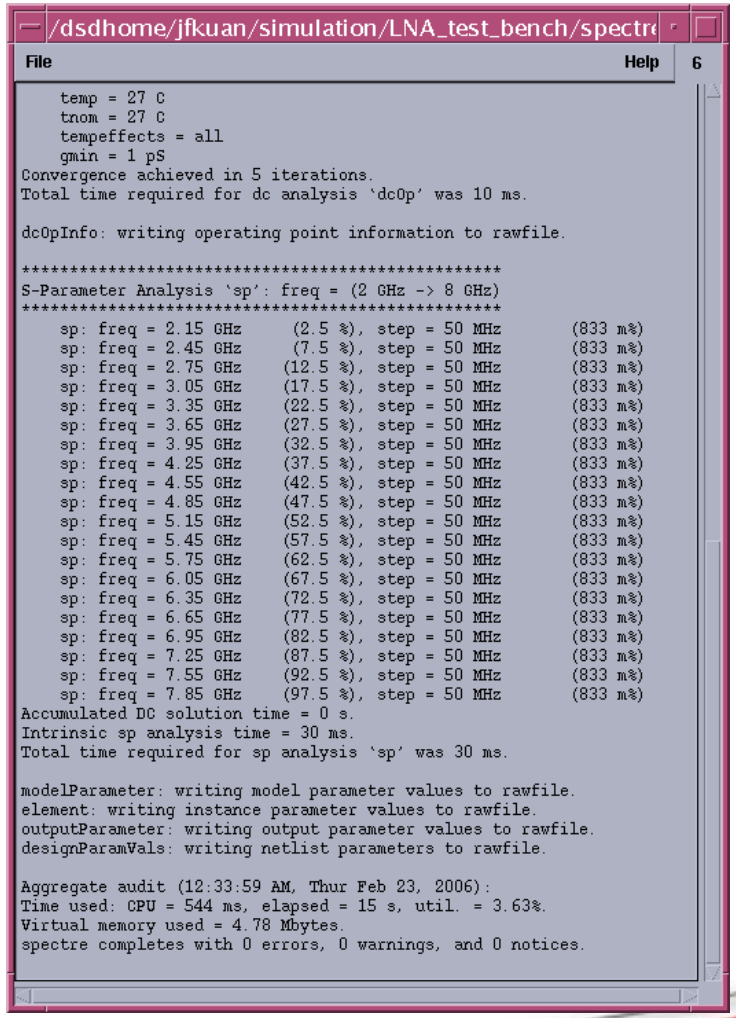
Turn on the Enabled field



Using Spectre simulator

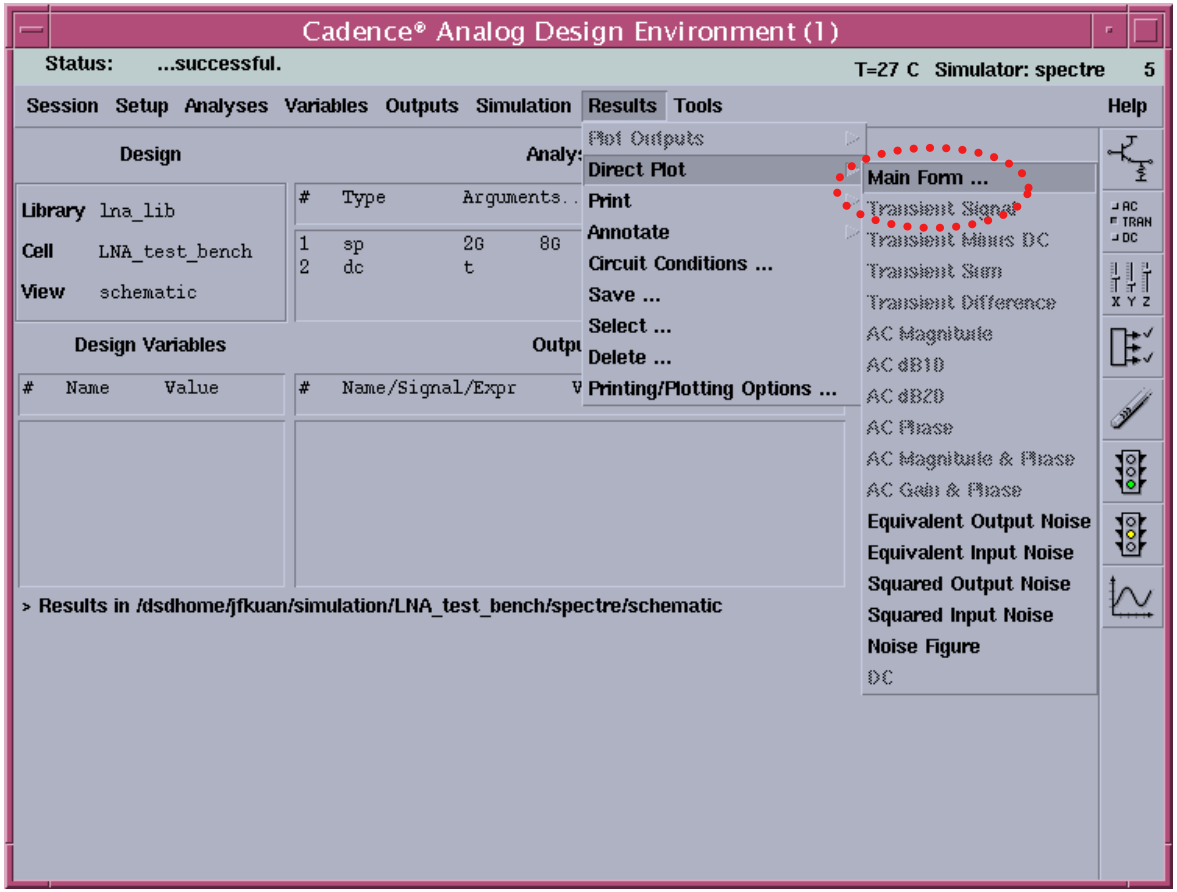
6. Run simulation

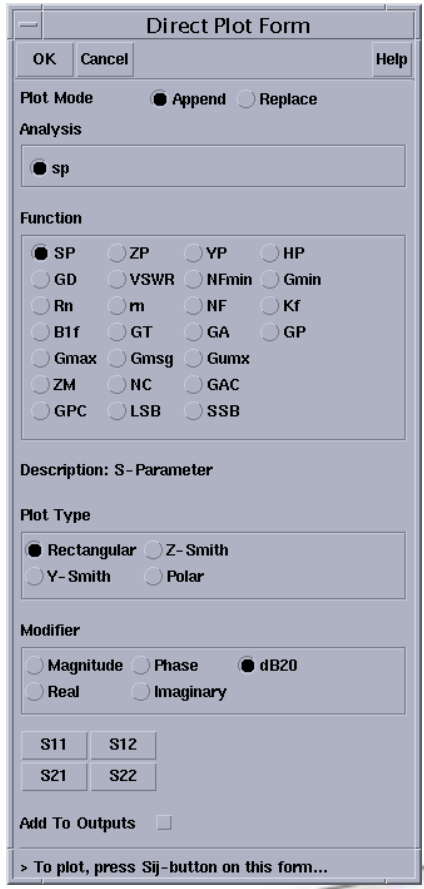
To start the simulation, you can click “simulation->netlist and run” from the Analog Artist menu banner.



LNA performance

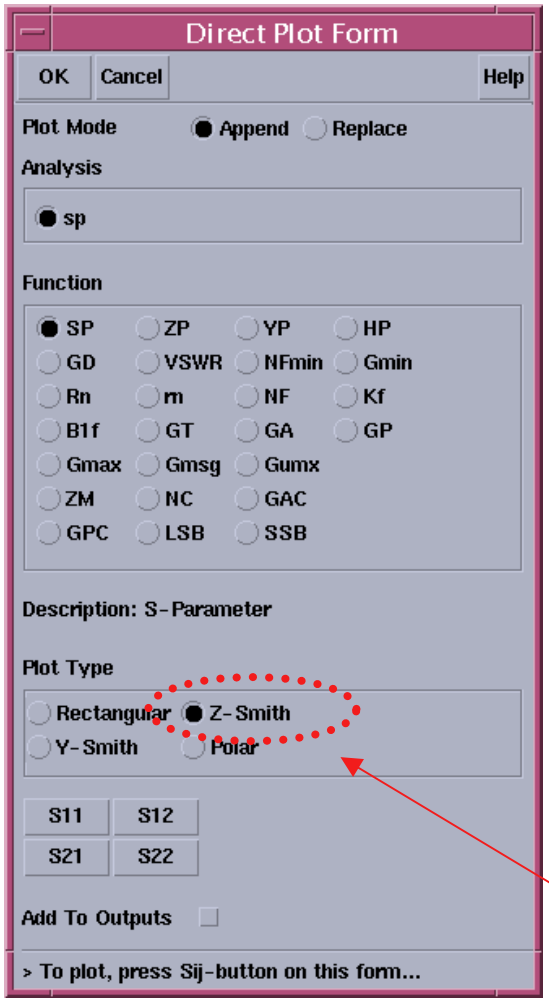
After running simulation, we can see the result and performance of our design from Results->Direct Plot->Main Form… :

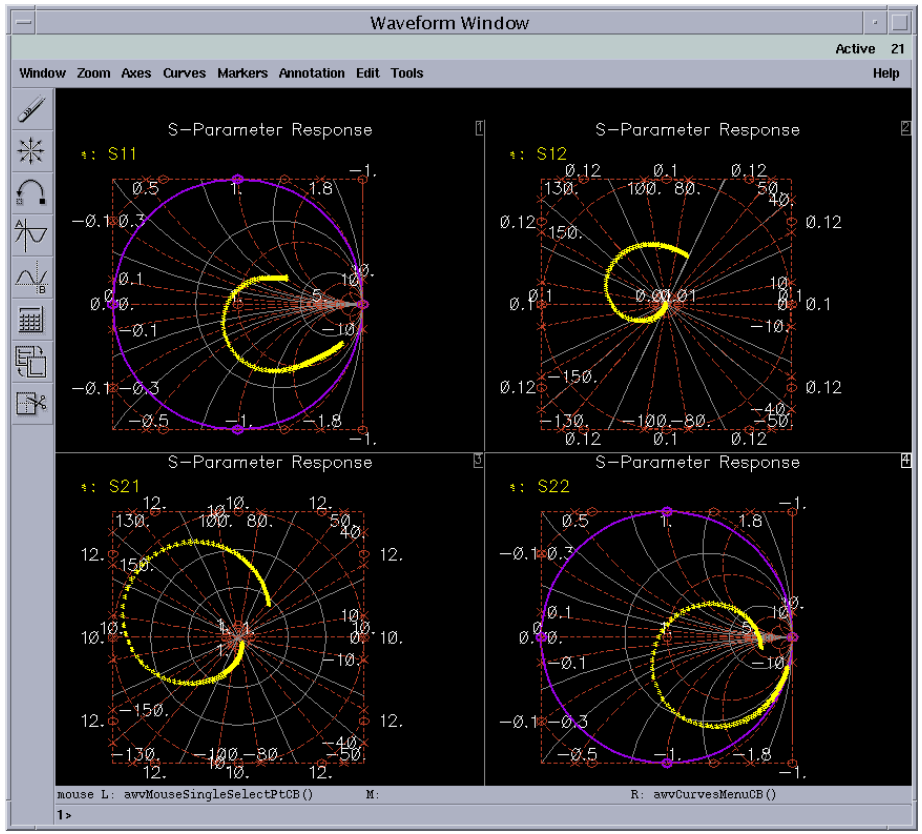




LNA performance

By setting Direct Plot Form shown below, we can see the S-parameter of our LNA design.





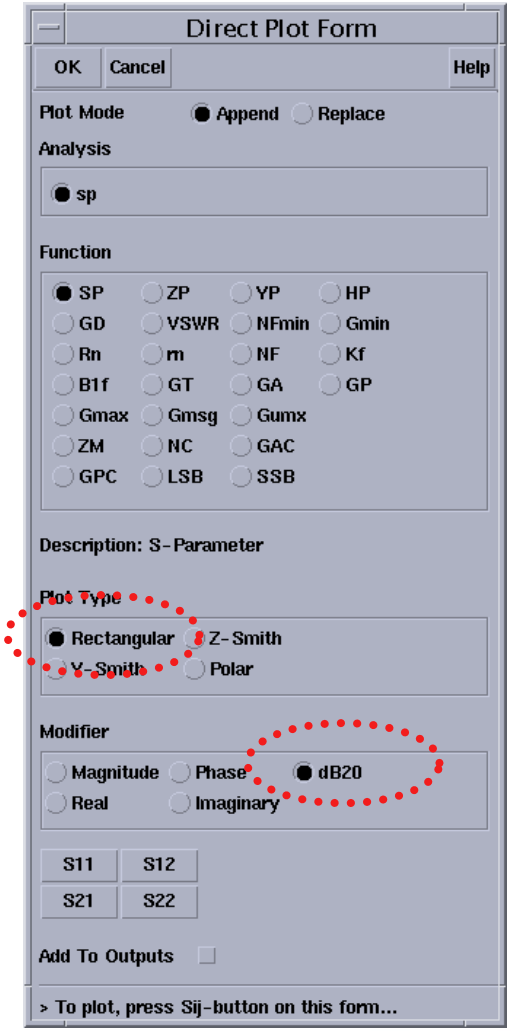
S-parameter

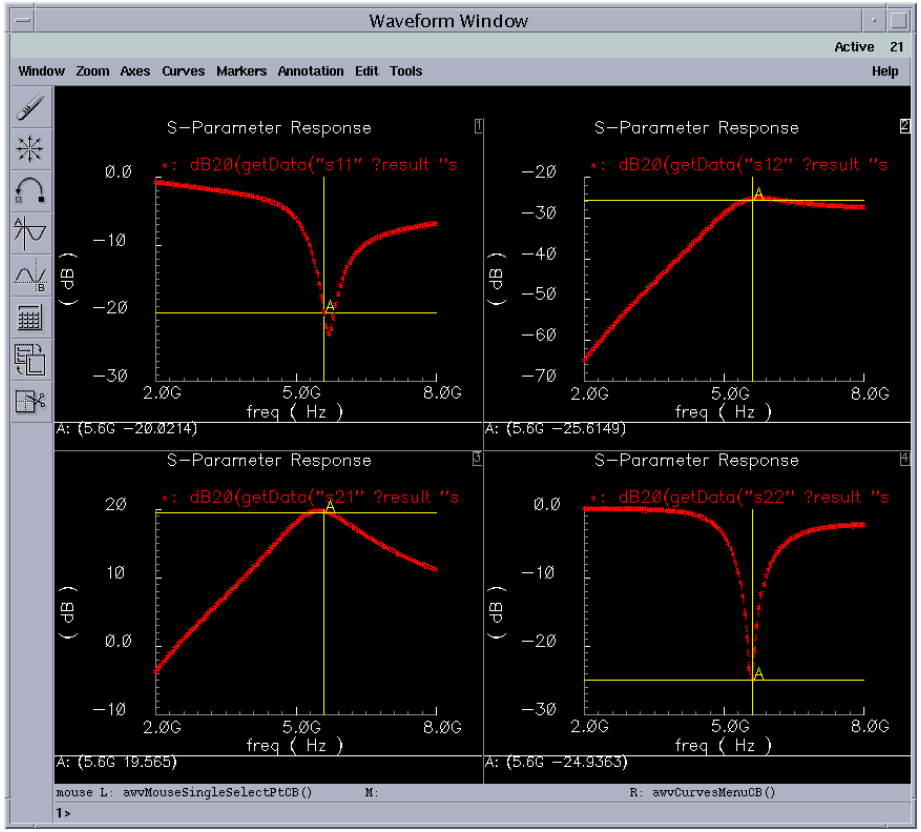
S11	S12
S21	S22

In this plot, "**Plot type**" is set to "**Polar**" on S12 and S21

LNA performance

By setting Direct Plot Form shown below, we can see the dB format S-parameter of our LNA design.

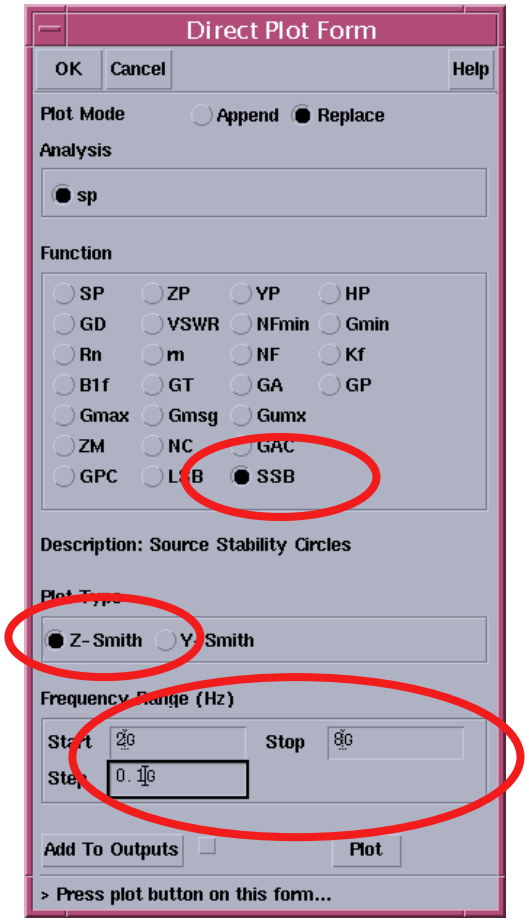


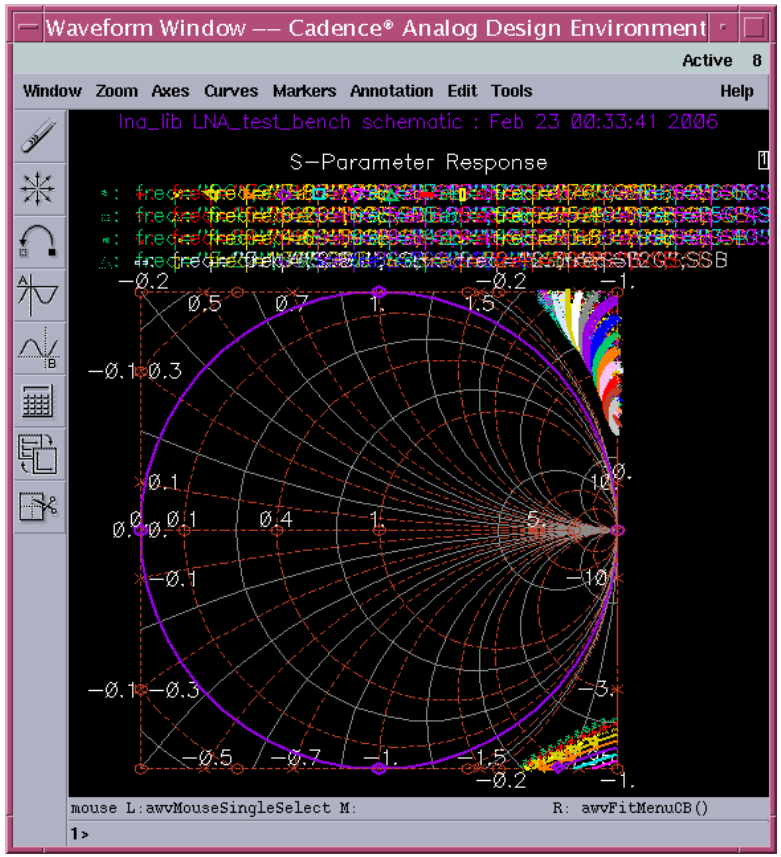


S21 = 19.6 dB @5.6GHz
S11 = -20.02dB @5.6GHz
S22 = -24.94 dB @5.6GHz

LNA Performance

By setting Direct Plot Form shown below, we can see the source stability circles of our LNA design.

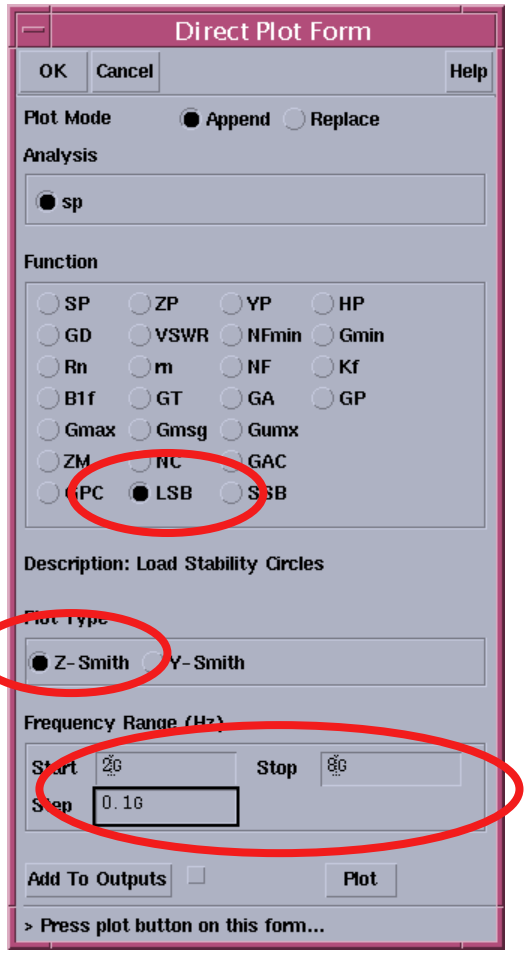


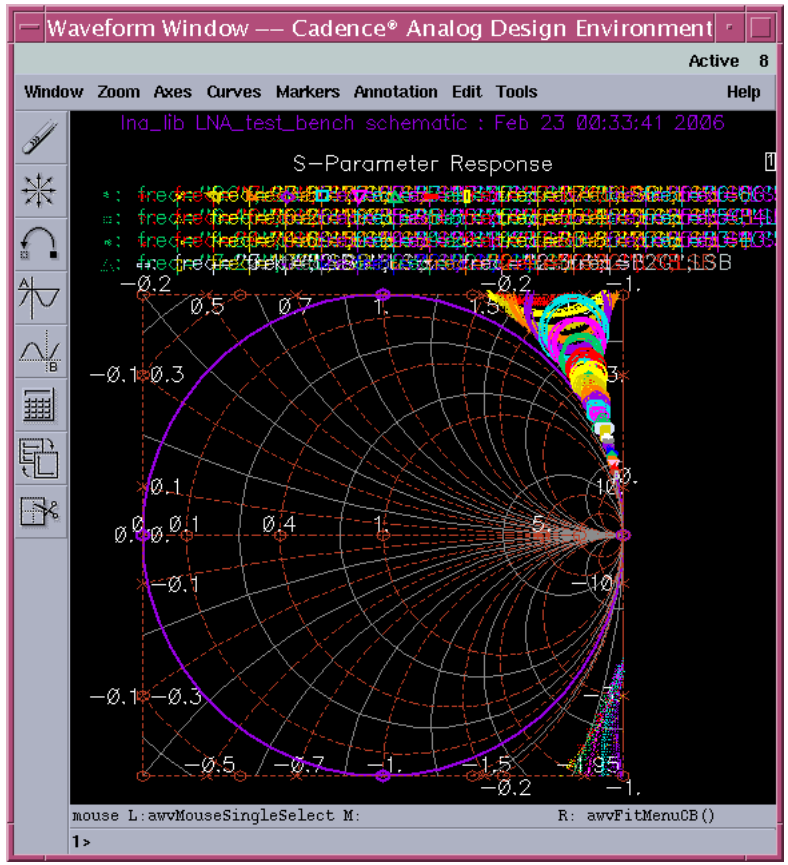


Source stability circle from 2GHz to 8GHz

LNA Performance

By setting Direct Plot Form shown below, we can see the load stability circles of our LNA design.

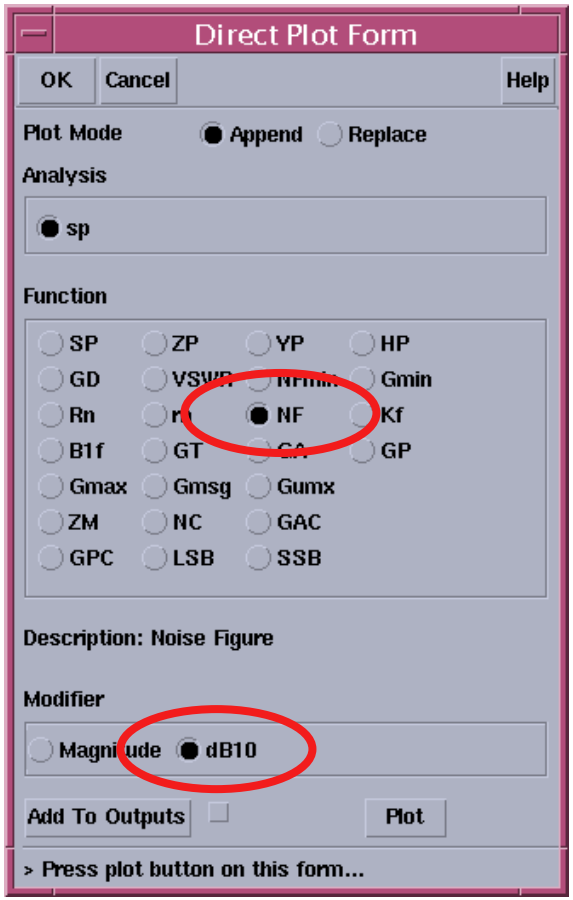


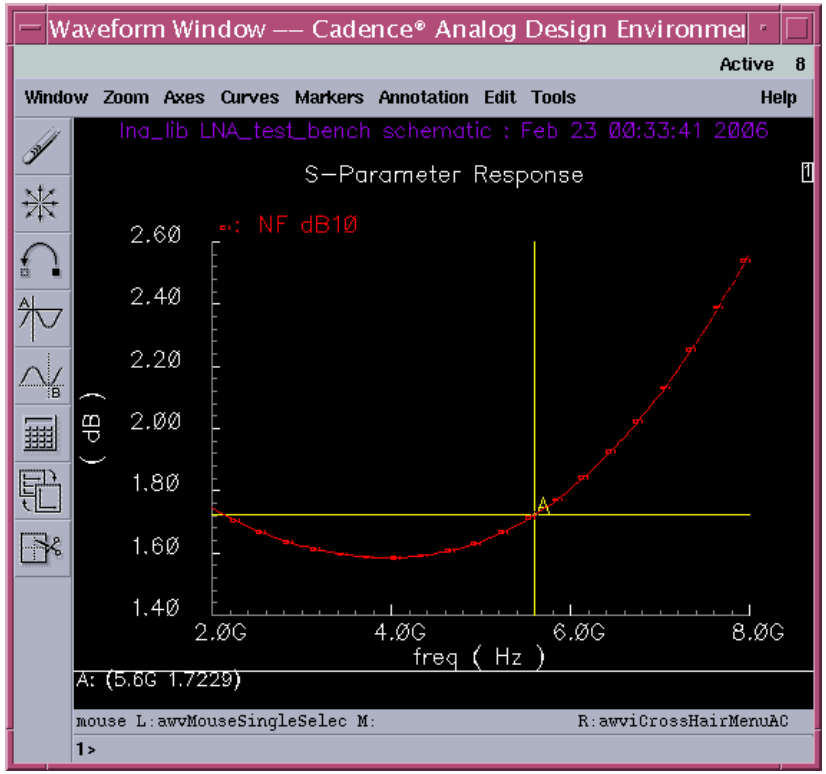


Load stability circle from 2GHz to 8GHz

LNA Performance

By setting Direct Plot Form shown below, we can see the Noise Figure of our LNA design.





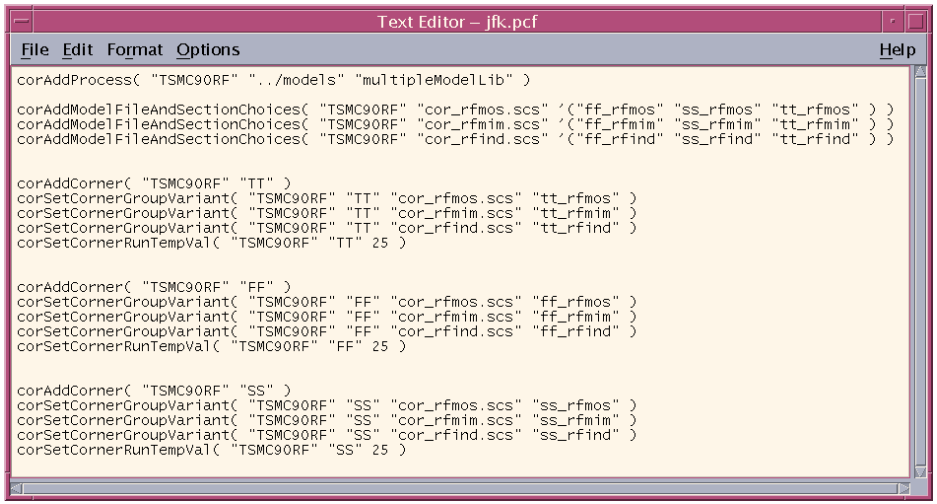
NF = 1.72 dB @5.6GHz

LNA performance summary

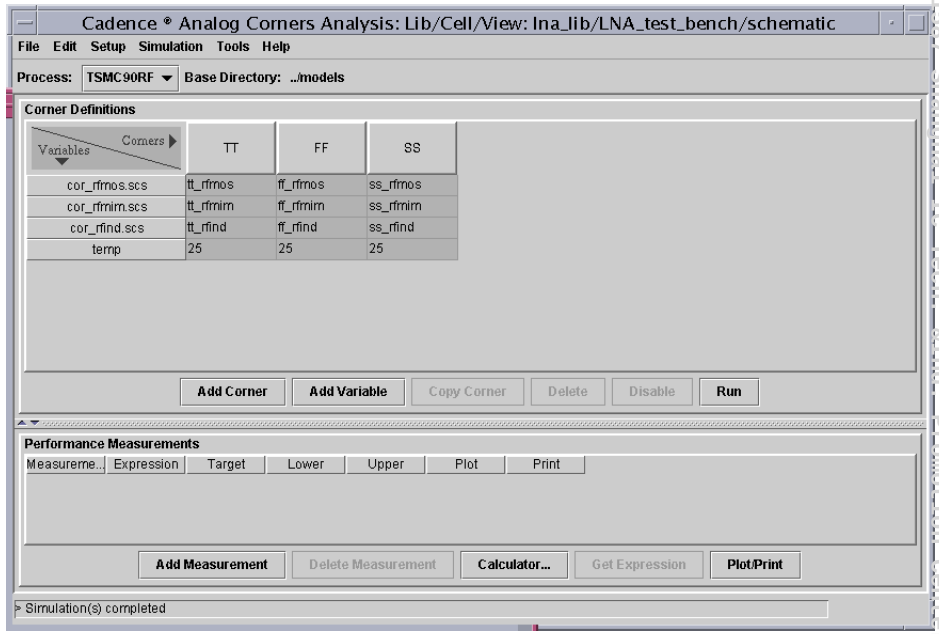
Sepcification	Simulation value
Center freqency	"5.6 GHz"
Gain	"19.6 dB"
Input return loss	"-20 dB"
Output return loss	"-24.9 dB"
Noise figure	"1.72 dB"
3dB bandwidth	">1.5 GHz"
Supply voltage	"1.2 V"
Supply current	"16.45 mA"

Corner simulation

In addition to cover the typical case, we may sometime want to simulate our design to cover the process variations in different corners. This can let us know whether the circuit performance specifications will still meet even when the process variation shift to different corner. Furthermore, this can also improve the product yield of our design. In our case, we simulate our design in three different corners: the typical case, the fast_best case (all devices in FF) and slow_worst (all devices in SS) case. By loading the well-defined PCF file released along with TSMC's PDK, you can find the corner analysis window shown below:



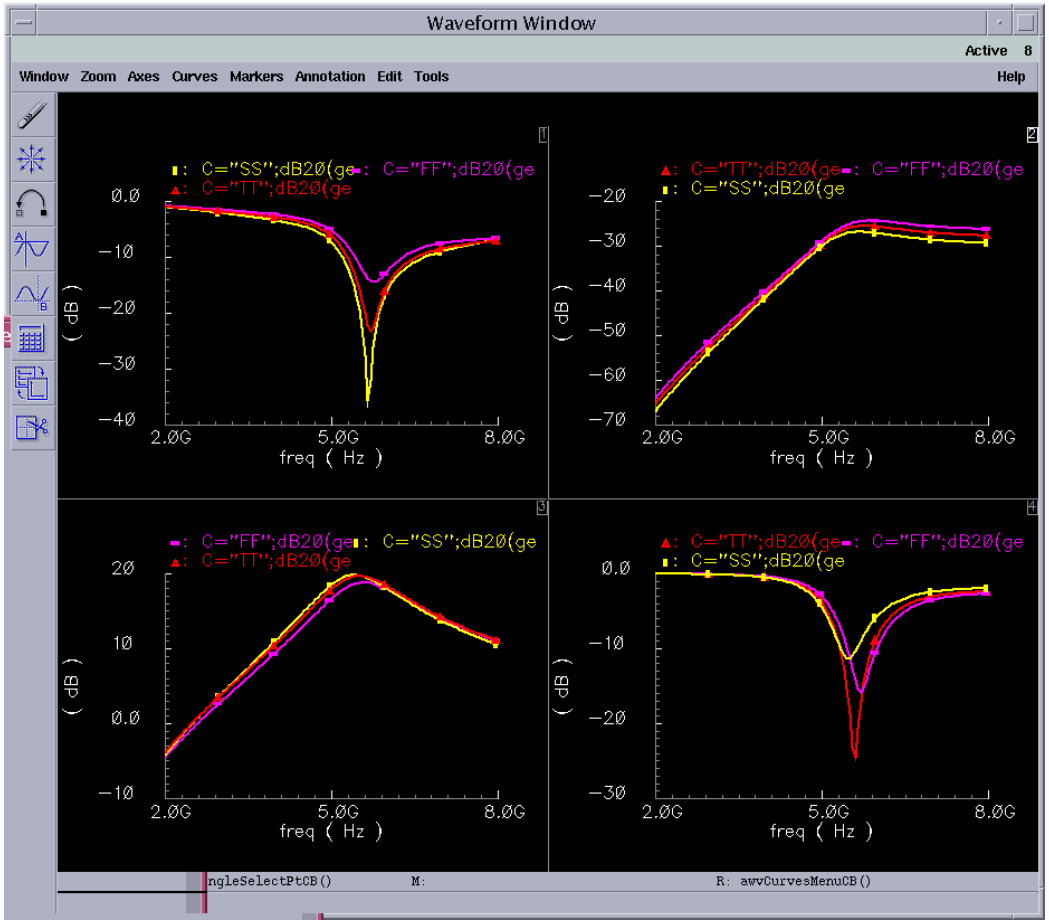
well-defined PCF file



Loading PCF file for corner analysis

Corner simulation

After finished the corner analysis, the s-parameters simulation results in different corners are shown below :



S11	S12
S21	S22

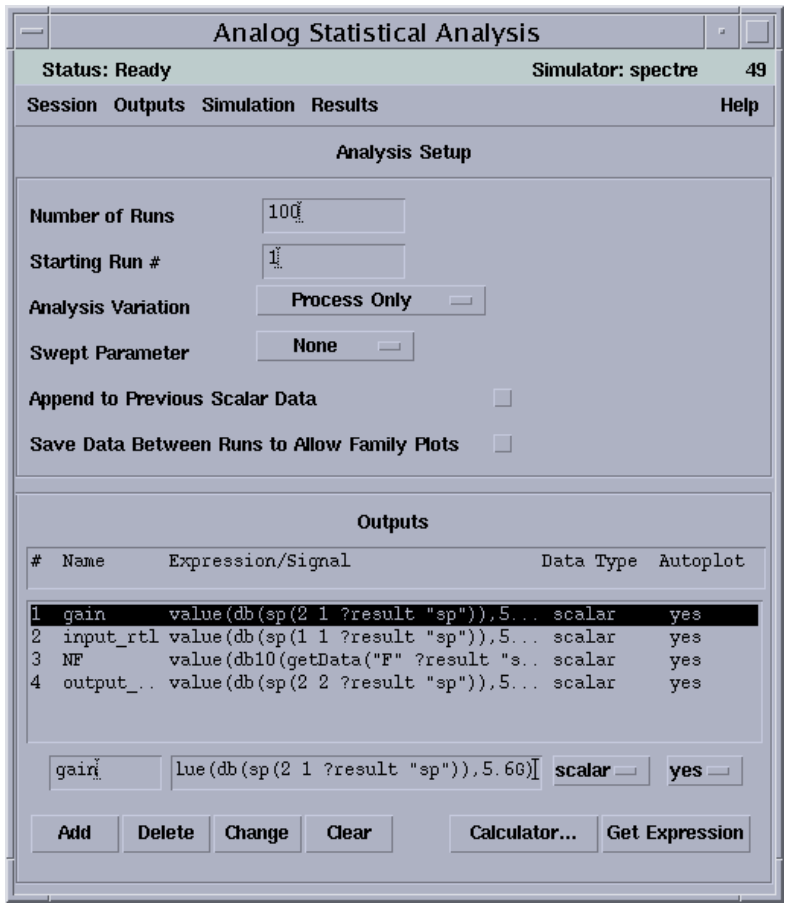
Red : TT
Pink : FF
Yellow : SS

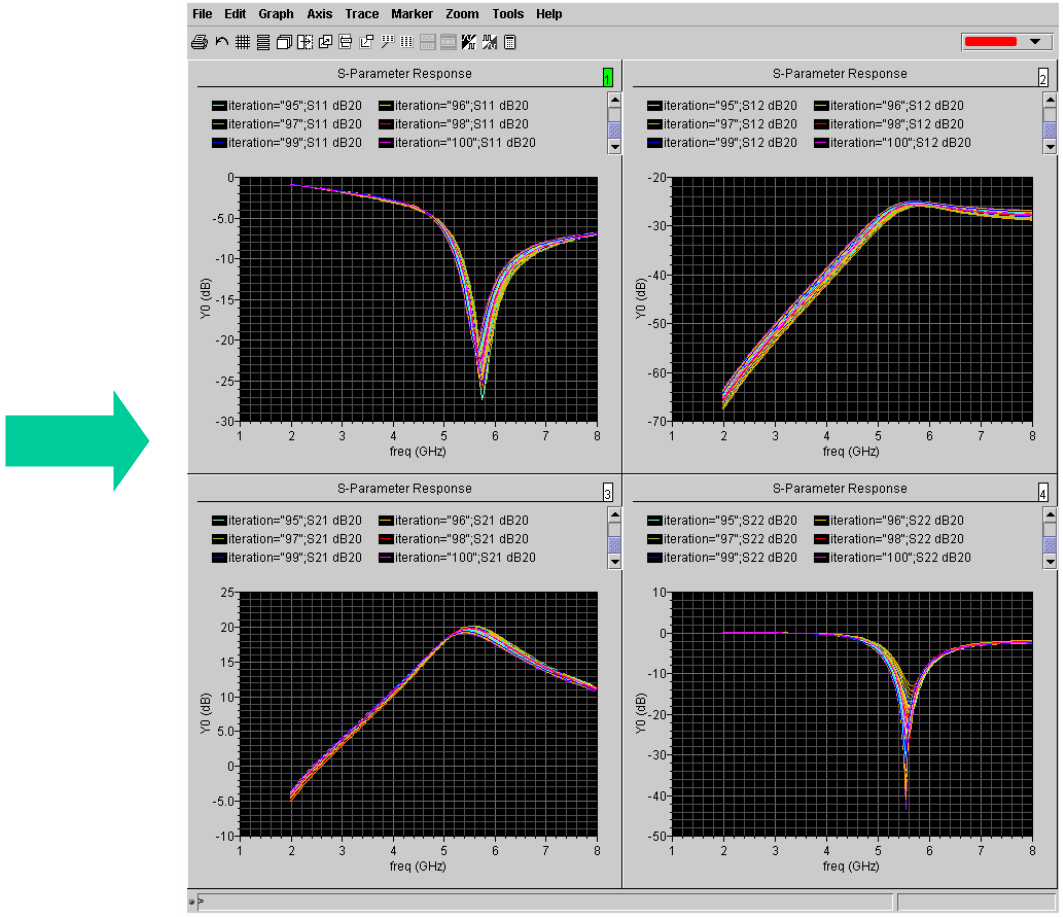
Monte Carlo simulation

By setting statistical analysis shown below,

we can see the Monte Carlo results.

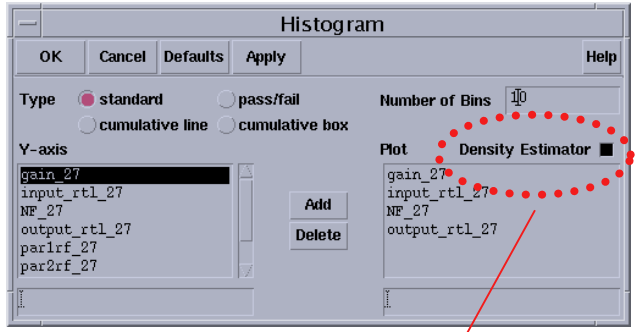
S11	S12
S21	S22



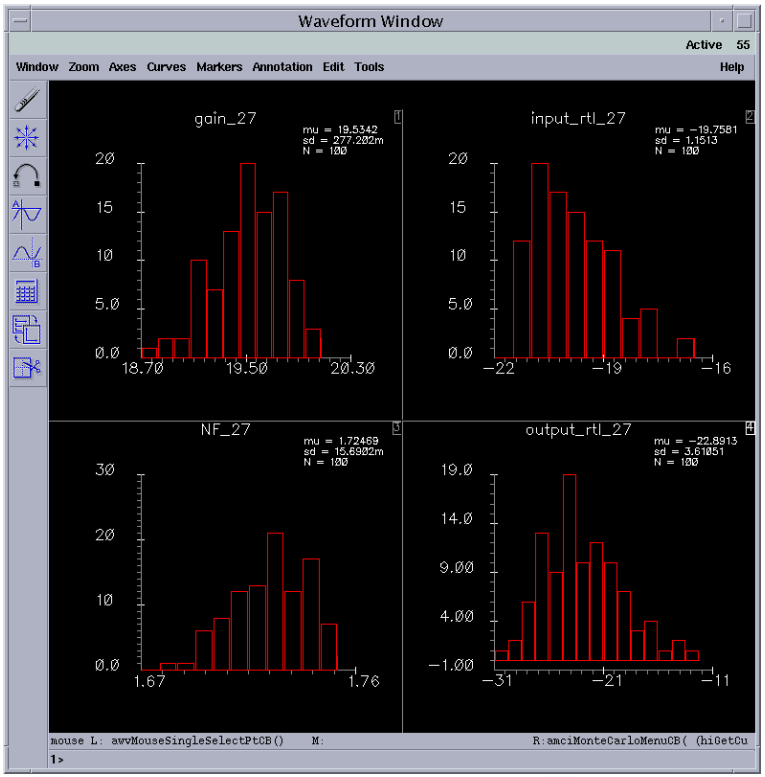


Monte Carlo simulation

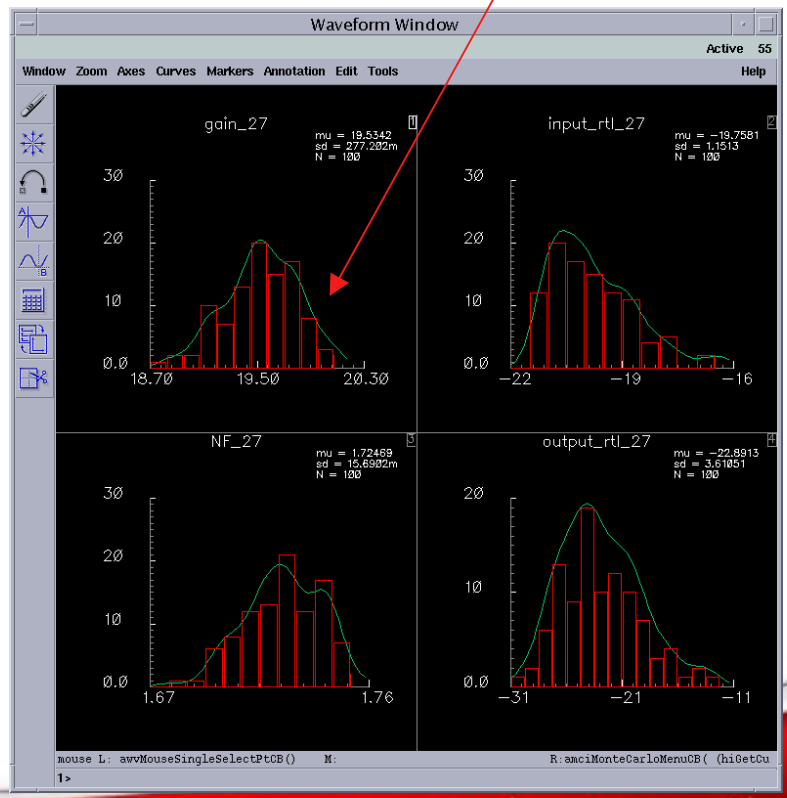
We can translate the Monte Carlo results into histogram by setting frequency to 5.6G :



With Density Estimator enabled (green line)

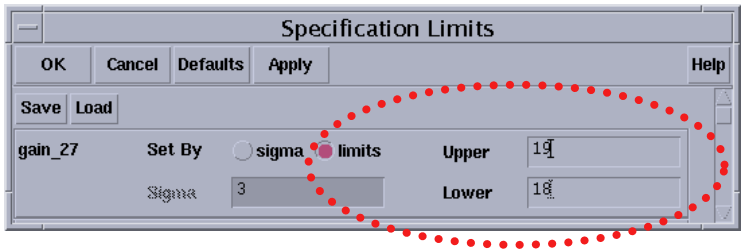


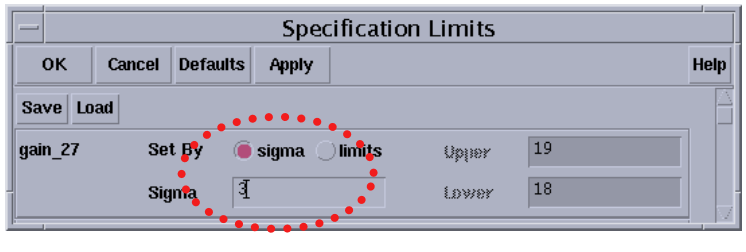
Gain	S11
NF	S22

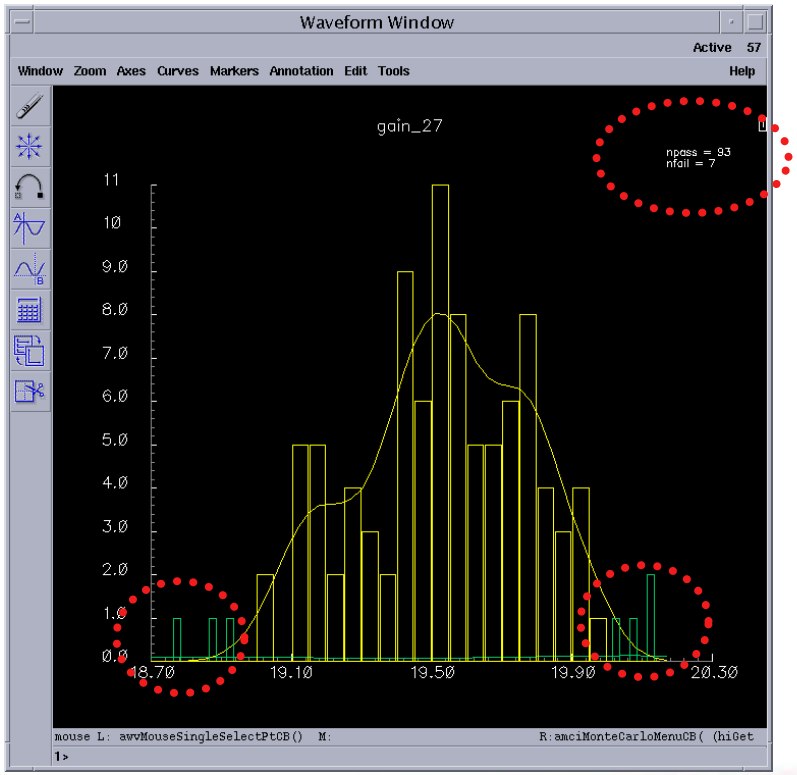


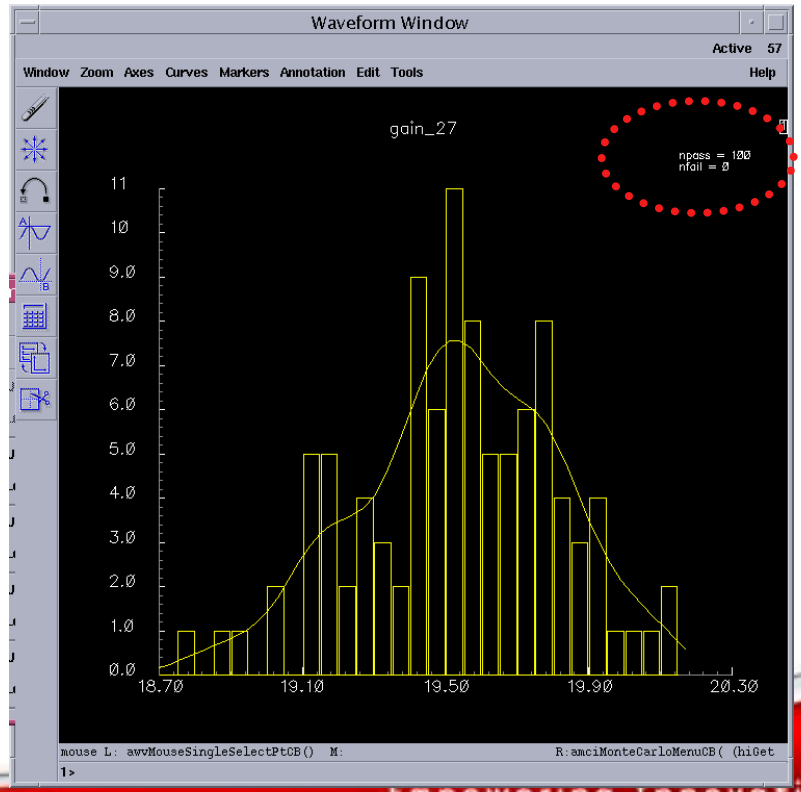
Monte Carlo simulation

Below are the specification limits results of the gain set by limits and sigma, respectively.









Contents

Layout Creation

After completed the pre-layout simulation and make sure the functionality and the circuit performance are all correct and in the design specifications, we can now start to create the corresponding layout for our design. The layout creation procedures are partitioned into three parts: “Schematic-Driven-Layout”, “Components Placement” and “Manual route”.

- **Schematic-driven-layout**
- **Components placement**
- **Manual routing**

Schematic-drive-layout

Steps for Schematic-Driven-Layout method:

1. Open the schematic view of our design

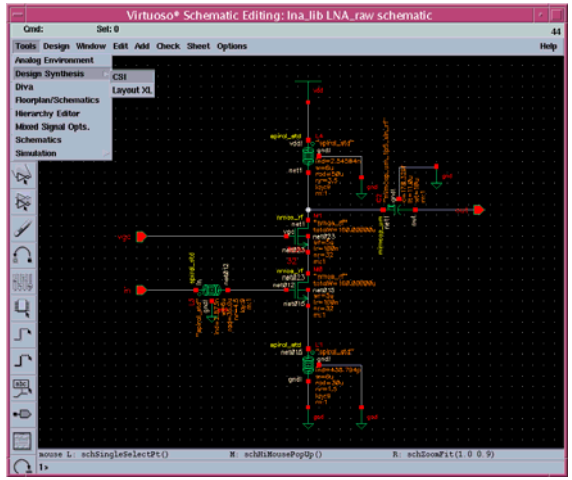
2. From the schematic menu select “Tools -> Design Synthesis -> Layout XL”

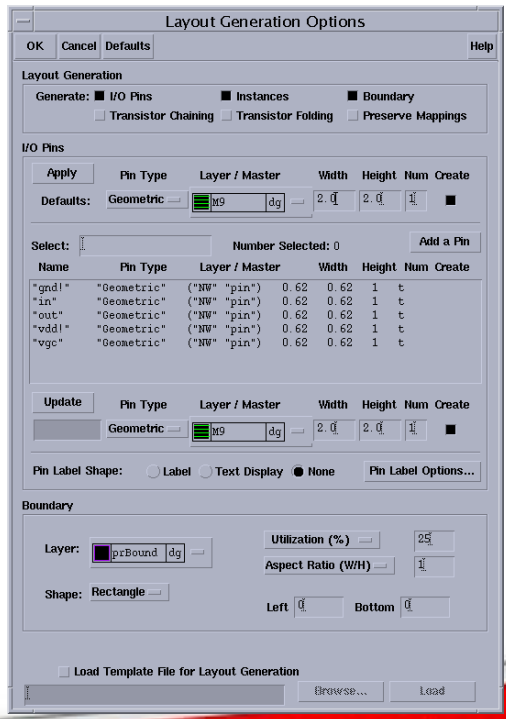
3. After selecting this option, a small dialog box will first open to let users select the cell name and view name for the layout. Upon finished the selection of the cell name and view name, a Virtuoso XL layout window popup for layout generation

4. From the Virtuoso XL layout menu, select “Design -> Gen from source …”

5. A layout generation options window appeared and prompts users to setup the pin layers, pin width, pin height, boundary layer …and so on for layout generation.

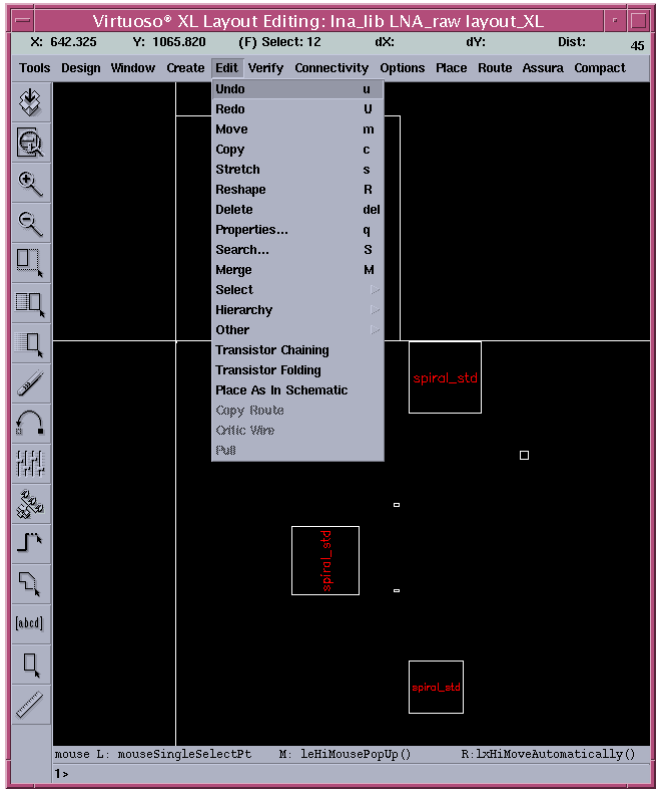
6. After finished the selection of above information, some rectangles that represent the components (transistor, inductor, capacitor and I/O pins will show up in the bottom of the layout window.

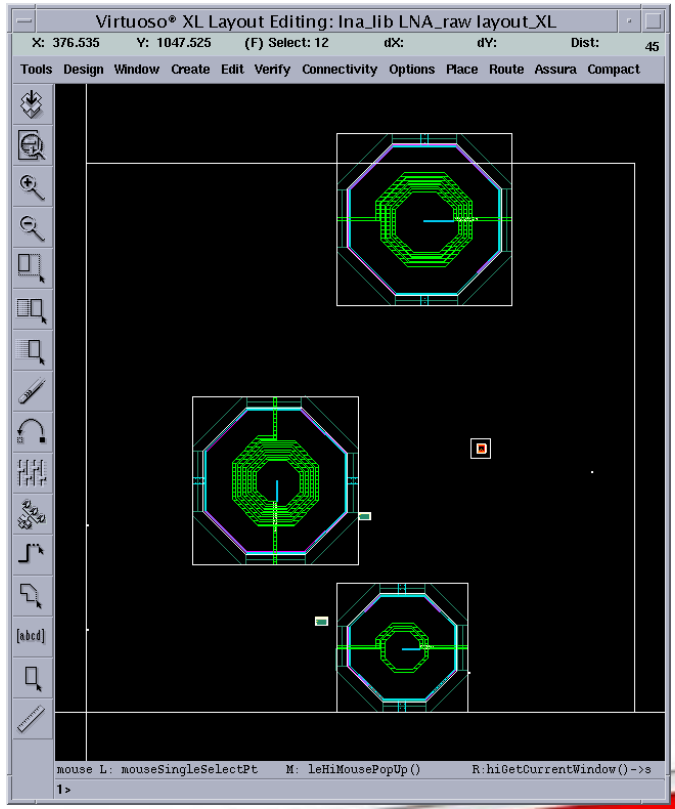




Components placement

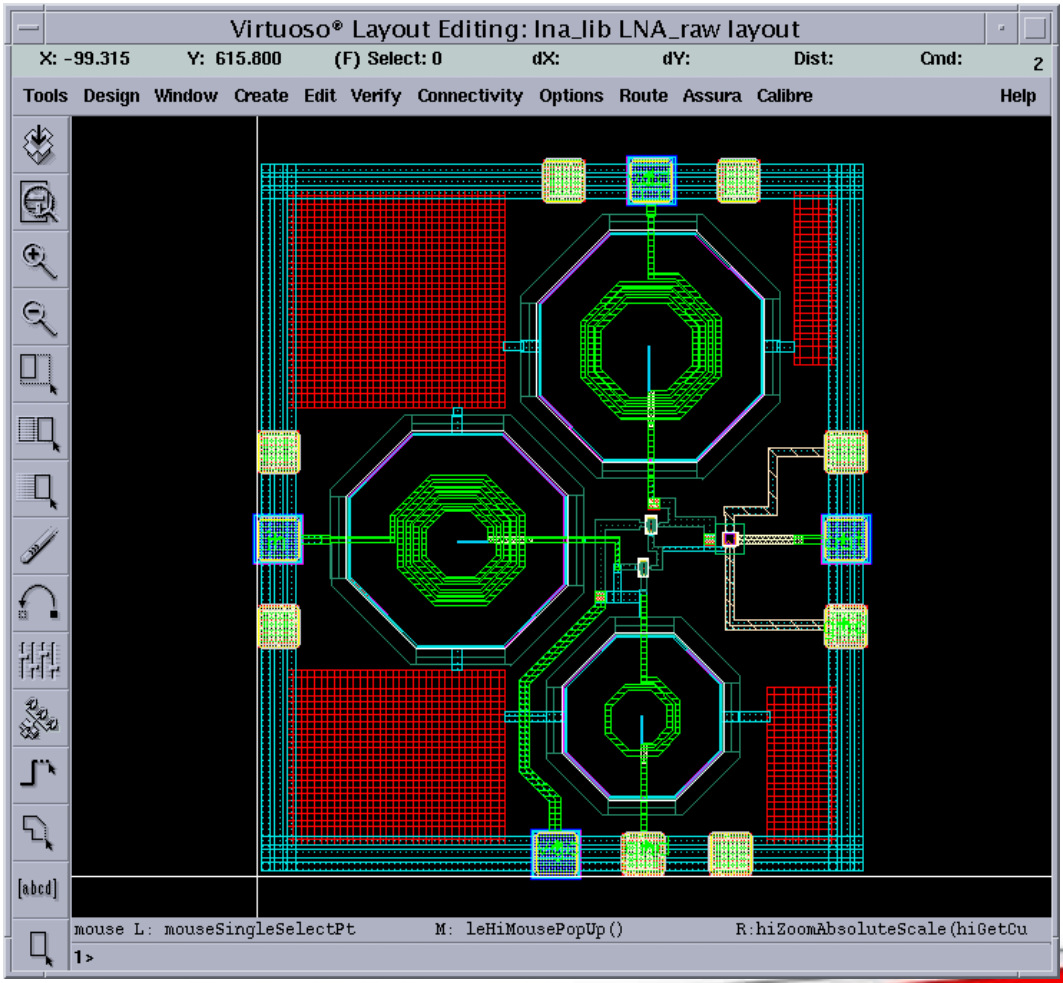
The next step is to do the device placement. The only one thing that you need to do is to place all the components and I/O pins in the layout window into the design area (cell boundary). You can use **Edit->Place As In Schematic** as your first placement reference. By selecting devices/IO pins and dragging them to proper locations inside the design area, we can complete the component placement. During the device movement and placement, the lines represent the connections of select object to other objects will show up. This can help you to decide where to properly locate the selected object.





Manual routing

For RFIC design, most designer prefer manual routing by themselves because the performance is layout-dependant. Different routing may cause different parasitics. Below is an layout example of the LNA_raw design.



Contents

Physical Verification

After the layout creation is completed, we have to start the physical verification to make sure this layout is DRC free and each device in the layout is completely match to its corresponding component in original schematic. After that, the parasitic extraction is necessary for post-layout simulation to make sure our design still work well after taking the parasitic R & C effects into account. Generally, the physical verification procedures can be divided into three parts: the design rule check (DRC), layout V.S. schematic check (LVS) and parasitic extraction (RCX or PEX). Furthermore, based on the differences in running methods and supported tools, they can be classified into different flows. TSMC's PDK supports varied kinds of decks to be used for different kinds of flows. In this application note, Assura DFII flow and Calibre GUI flow are demonstrated. In real design, users only need to choose one of these physical verification flows and have no need to go through all the flows.

- **Assura DFII Flow**
  - DRC
  - LVS
  - RCX
- **Calibre GUI Flow**
  - DRC
  - LVS
  - PEX

Assura DRC Flow

Currently TSMC has not supported Assura RF drc deck yet.
You can refer the procedure of Calibri drc flow.

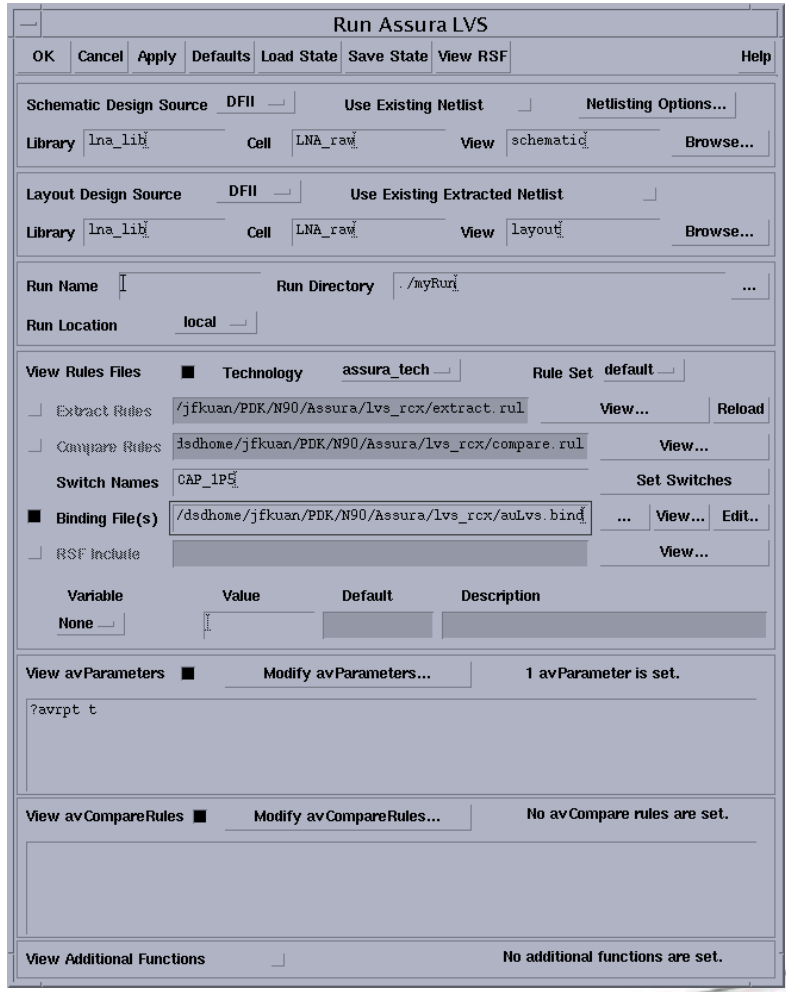
Assura LVS Flow

After the layout has no DRC violations (DRC free), the next step is to run the LVS check to make sure the layout is totally match to the schematic.

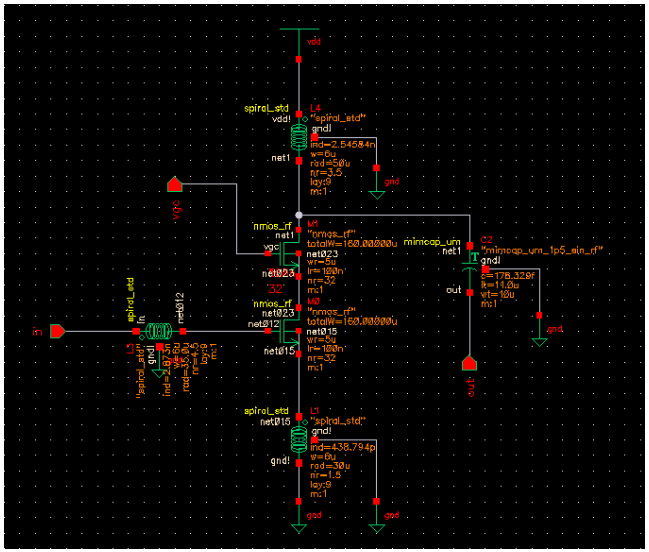
1. Click “Assura->Run LVS…” in layout window to invoke Assura LVS graphic user interface.

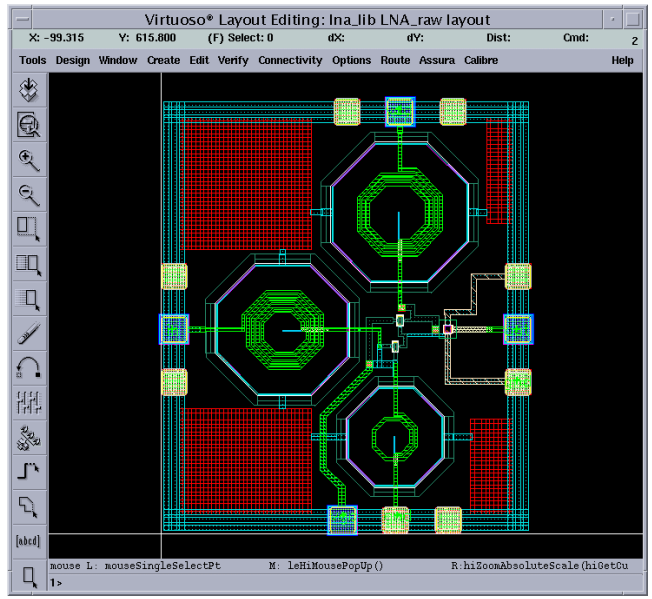
2. Fill in the “Assura run directory” and select the “Technology” field to “assura_tech” in Assura LVS window. You can also set the Assura LVS switches and other parameters if needed. In this case, we set the CAP_1P5 switch.

3. Click “OK” to run the Assura LVS and see the result. If the layout isn’t matched to schematic, you have to manually re-edit the layout and re-run the LVS check to make the LVS result matched.

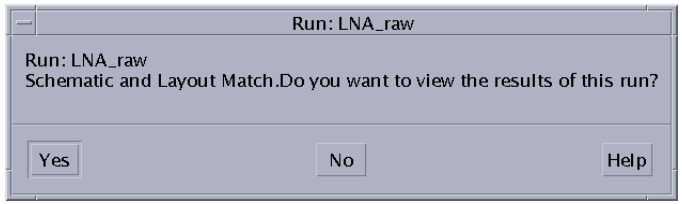


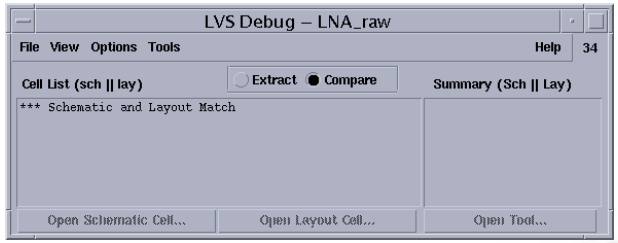
Assura LVS Flow





At this case, after running LVS, the result shows “Schematic and Layout Match”



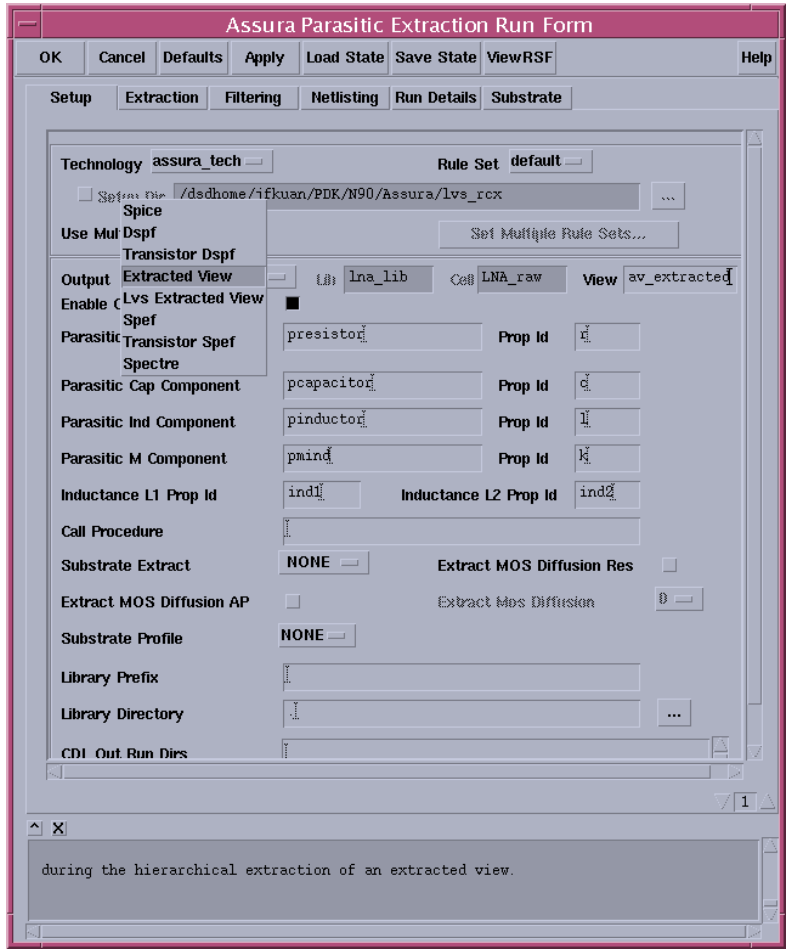


Assura RCX Flow

When the layout is DRC free and LVS clean, the next step is to perform the RC extraction. This step is to prepare the layout extracted netlist for post-layout simulation.

1. Click “Assura->Run RCX…” in layout window to invoke Assura RCX graphic user interface.

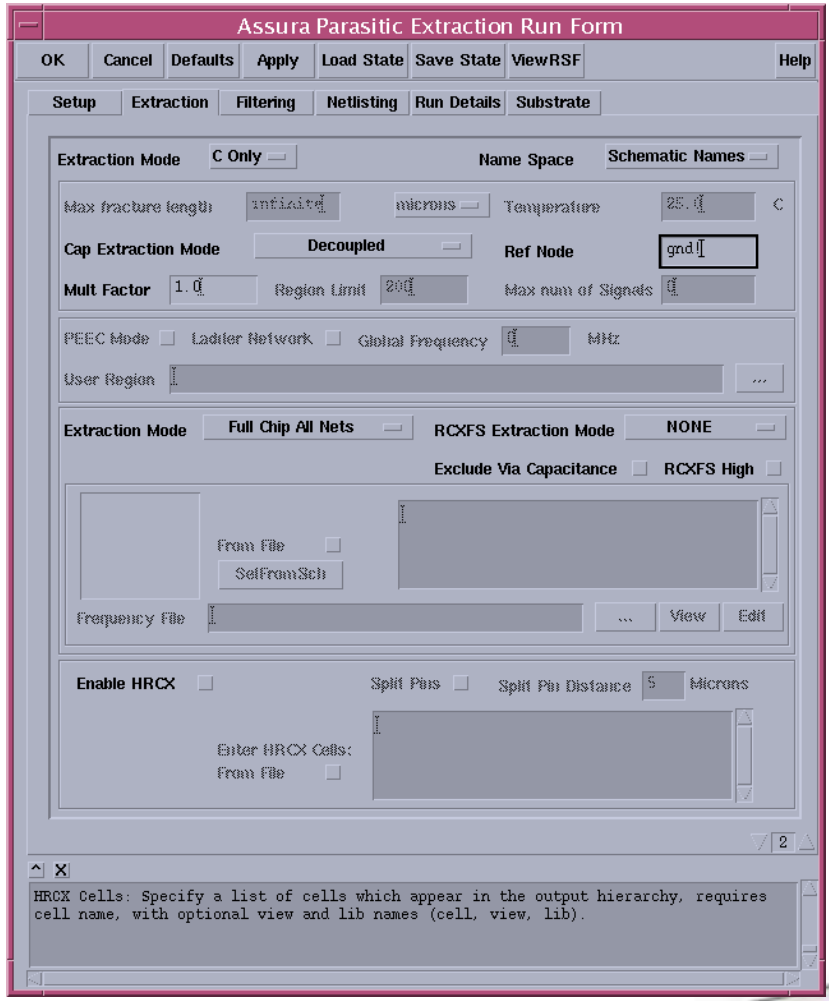
2. Select “Output” to “Extracted View” in “setup” folder of Assura RCX window to output extract result to “av_extracted” view.



Assura RCX Flow

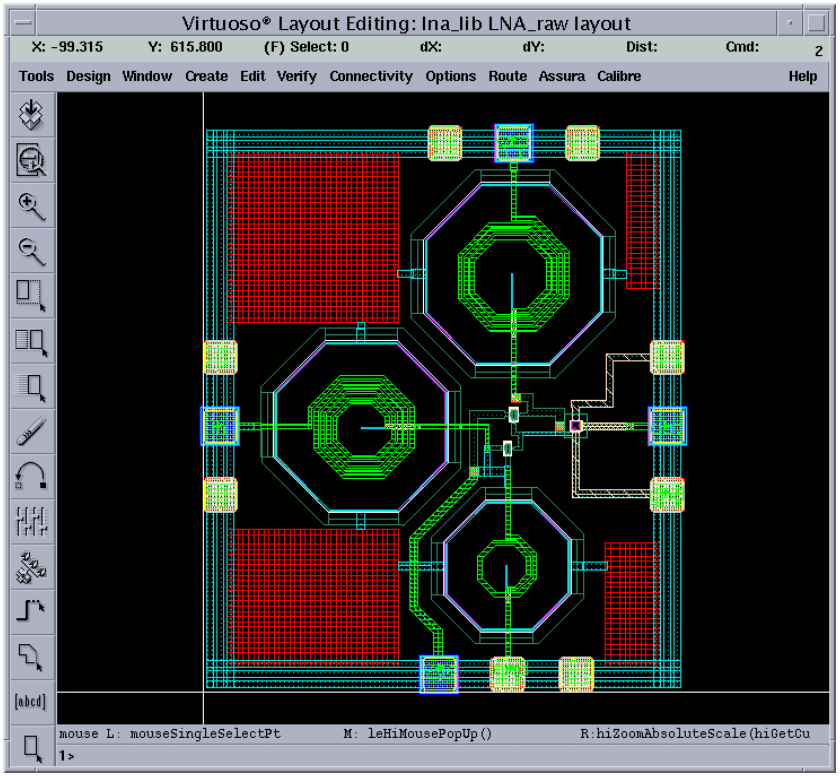
3. In the “Extraction” folder of Assura RCX window, select the “extraction mode” to “C only” (if you want to extract only C), set the “Name space” to “Schematic Names” and fill in the “Ref Node”(here we use “gnd!”).

4. Click “OK” to start the Assura RC extraction. After the RC extraction is completed, a new view (“av_extracted” view) which contains not only the original components but also the parasitic devices will be generated and then can be used for post-layout simulation.

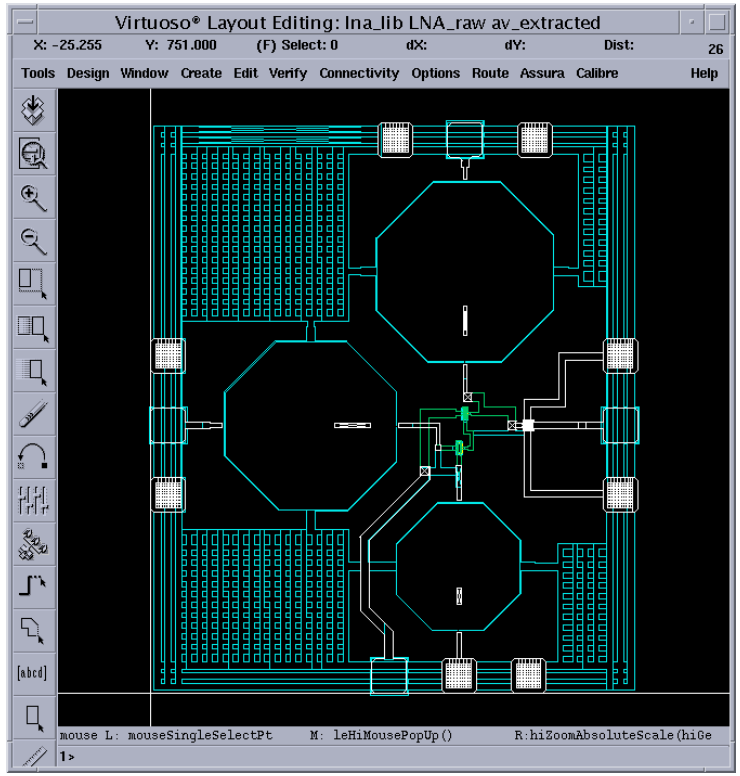


Assura RCX Flow

The av-extracted view by C-only mode is showed below:



Original layout



Av-extracted view by C-only mode

Calibre DRC Flow

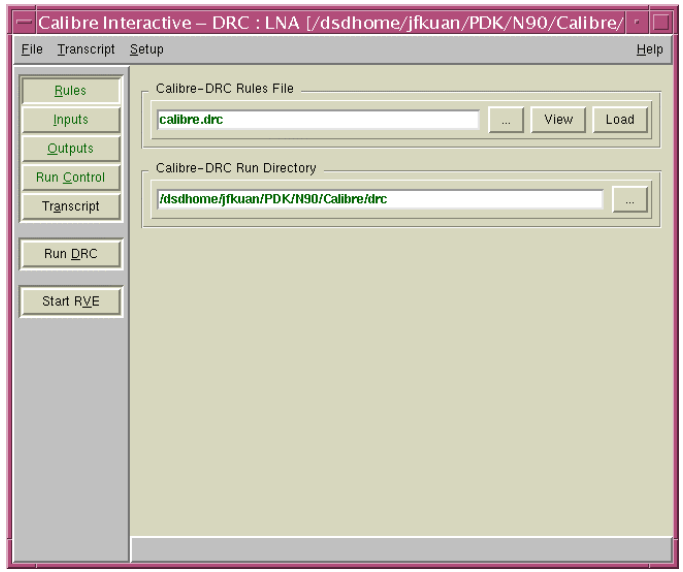
Calibre GUI mode flow is working under Cadence Virtuoso environment and its DRC verification procedures are listed below :

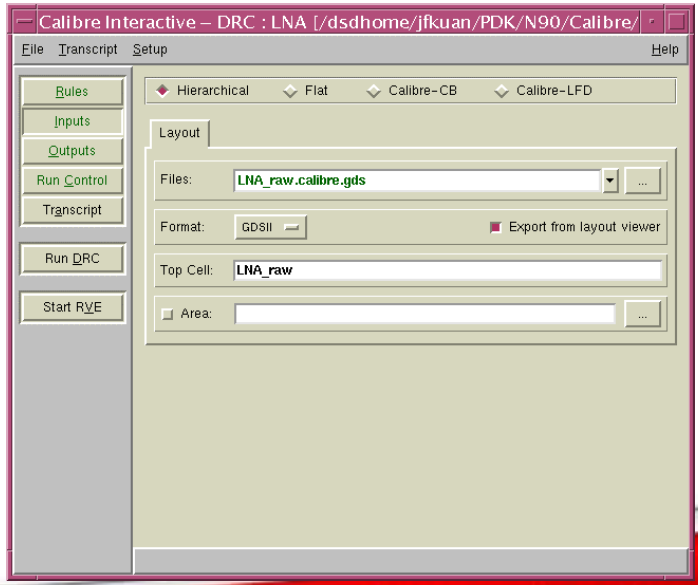
1. Click “Calibre->Run DRC” in layout window to invoke Calibre DRC graphic user interface.

2. Specify the “Calibre-DRC rules file” and the “Primary cell” in Calibre interactive-DRC window. If you need to change some DRC switches, you have to edit the Calibre DRC deck first.

3. Click “Run DRC” button to start the Calibre DRC verification and check the result in RVE.

4. If the layout isn’t DRC free, you have to re-edit the layout and re-run the DRC check to make it DRC free

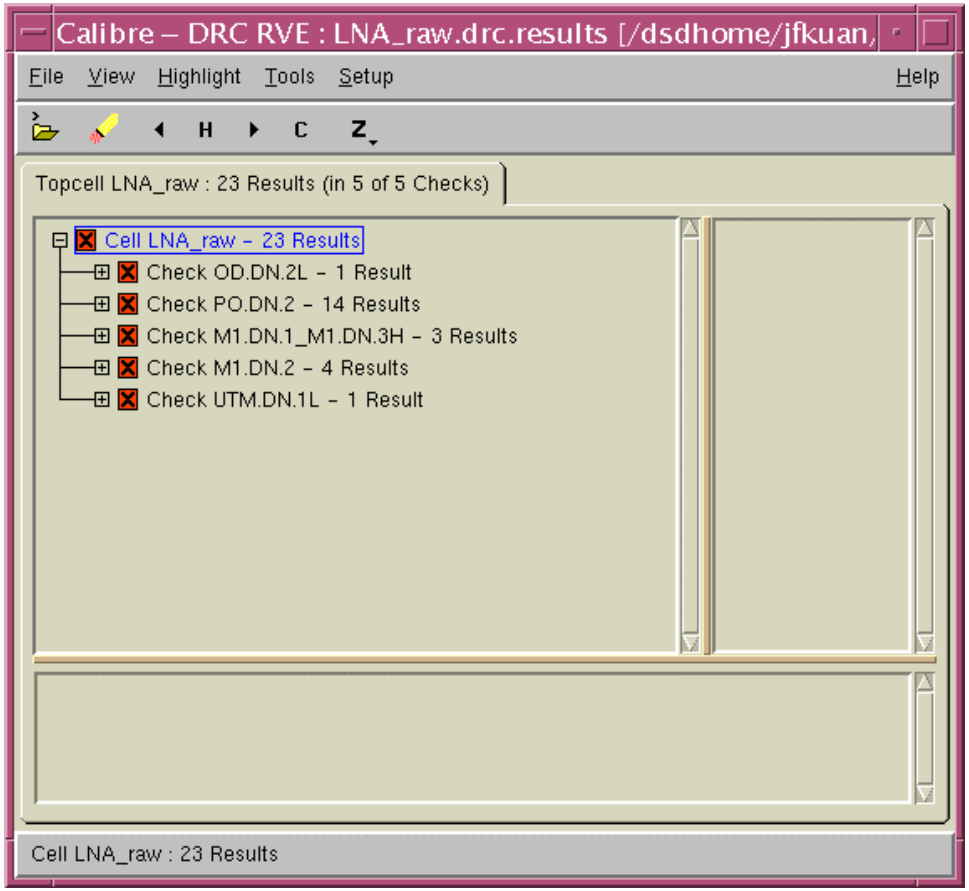




Calibre DRC Flow

We have disabled the "**fullchip**" option in the rule file because this case is just for a demonstration.

After running calibre drc, the results show that the layout is drc clean except some density rule.

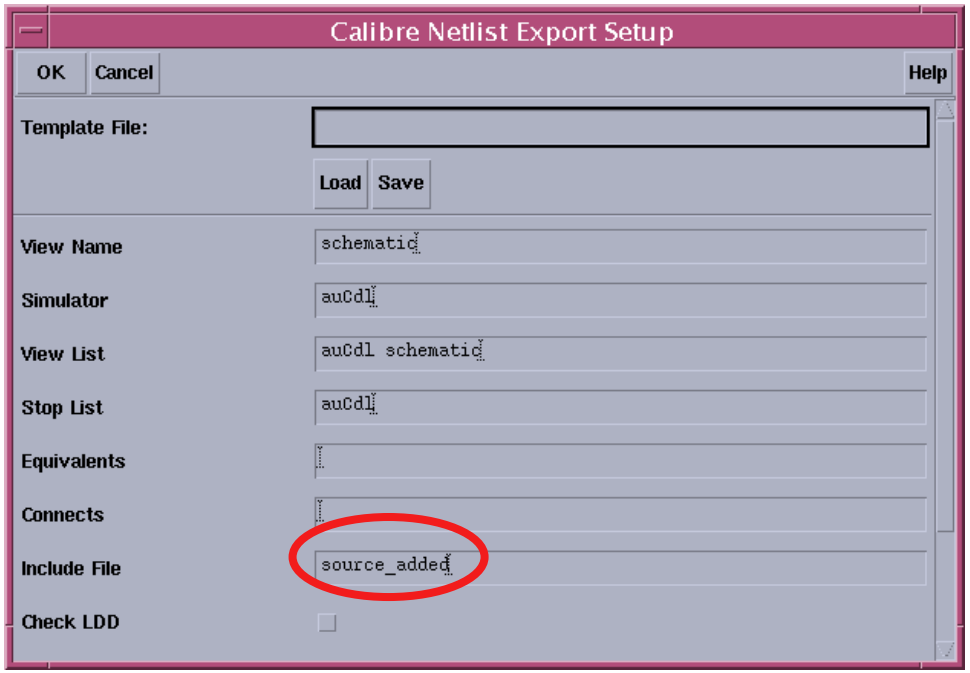


Calibre LVS Flow

After the layout has no DRC violations, the next step is to run the LVS check to make sure the layout is completely match to the schematic.

1. If the “source_added” file (empty sub-circuit file) is provided along with the LVS deck, you have to specify this file as an include file for netlist export by click “Calibre->Setup->Netlist Export…”.

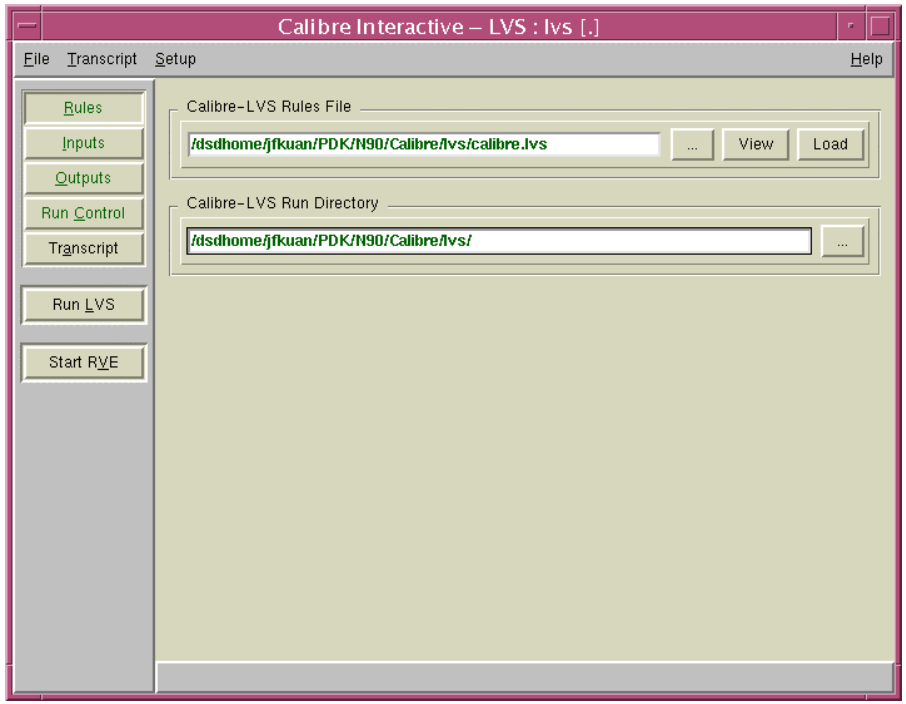
2. Click “Calibre->Run LVS” in layout window to invoke Calibre LVS graphic user interface.

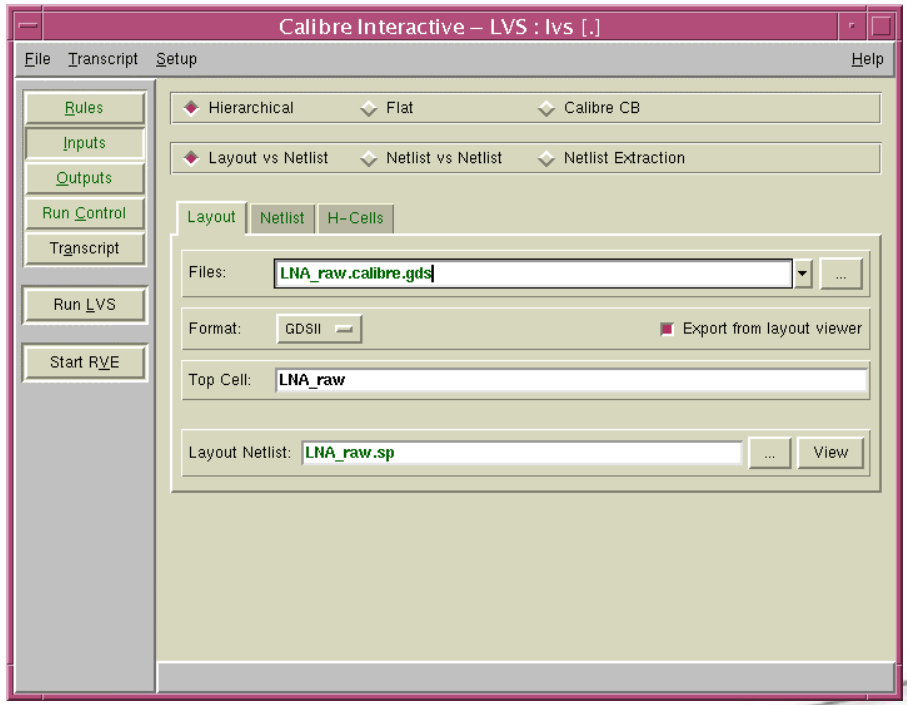


Calibre LVS Flow

3. Specify the “Calibre-LVS rules file“, working directory and “Primary cell” in Calibre LVS window. If you need to change some LVS switches, you have to edit the Calibre LVS deck first.

4. Click “OK” to run the Calibre GUI LVS and see the result. If the layout isn’t matched to schematic, you have to fix the layout and re-run the LVS check to make the LVS result matched.

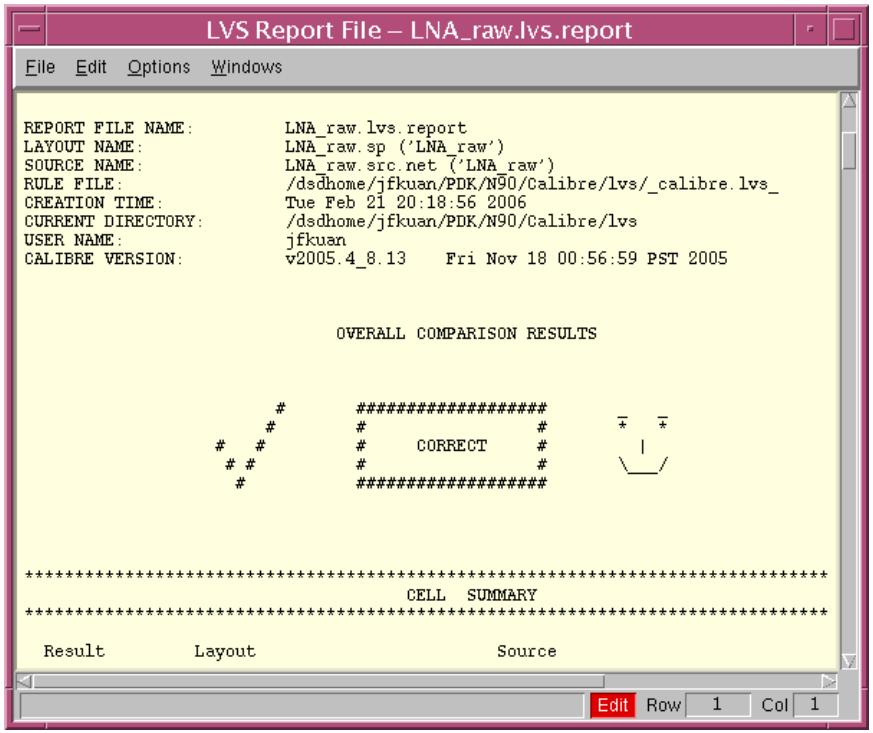


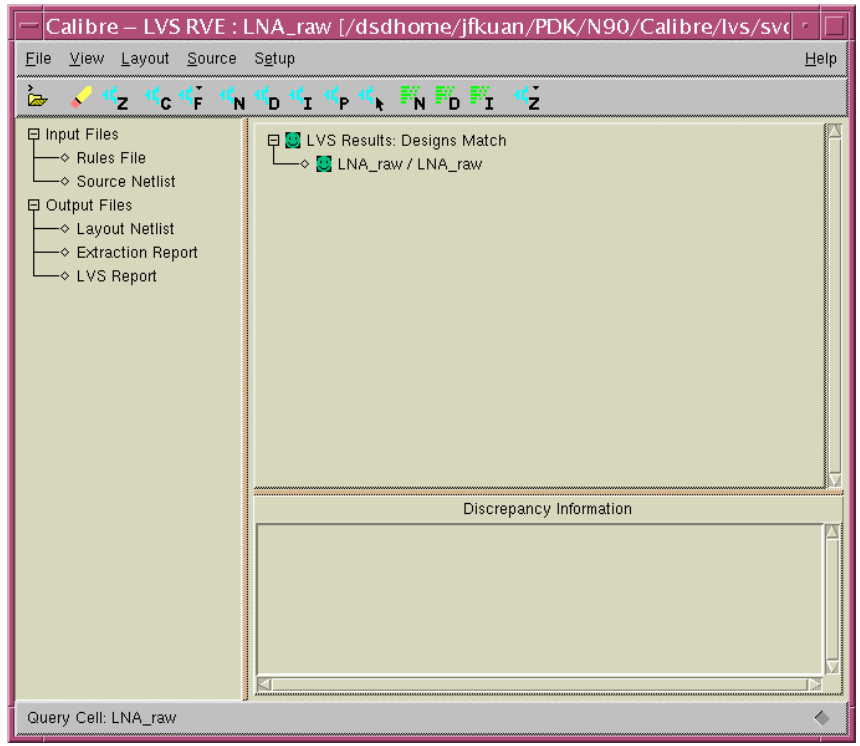


Calibre LVS Flow

Below is the LVS result that shows good match between layout and schematic

.





Calibre PEX Flow

When the layout is verified to be DRC free and LVS clean, the next step is to perform the RC extraction.

Before running PEX flow

Since all of the parasitics in the P-cell have been accounted by RF PDK device model. The extraction tool must not extract parsitics inside the specified devices to avoid double counting. The following steps should be taken to run pre-characterized device (PCD) flow:

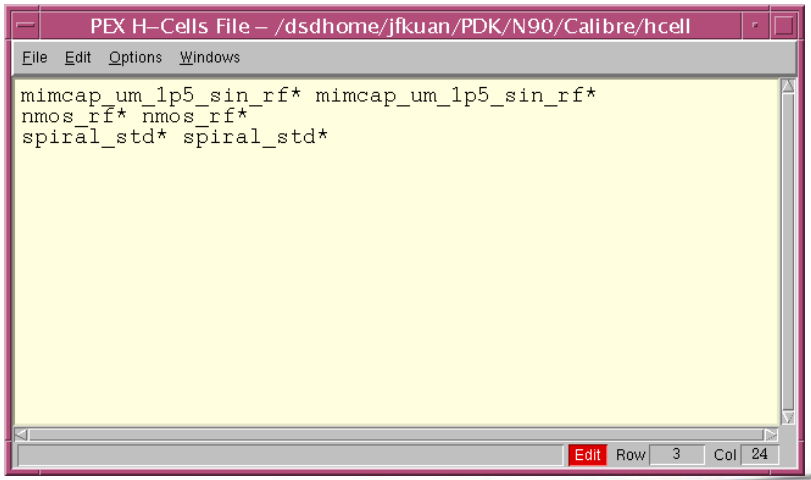
1. Add following statements in your LVS rule file:

   SOURCE CASE YES

   LVS COMPARE CASE NAMES

2. Add ***PEX IDEAL XCELL YES*** in your PEX rule file.

3. Prepare h-cell file as follows:

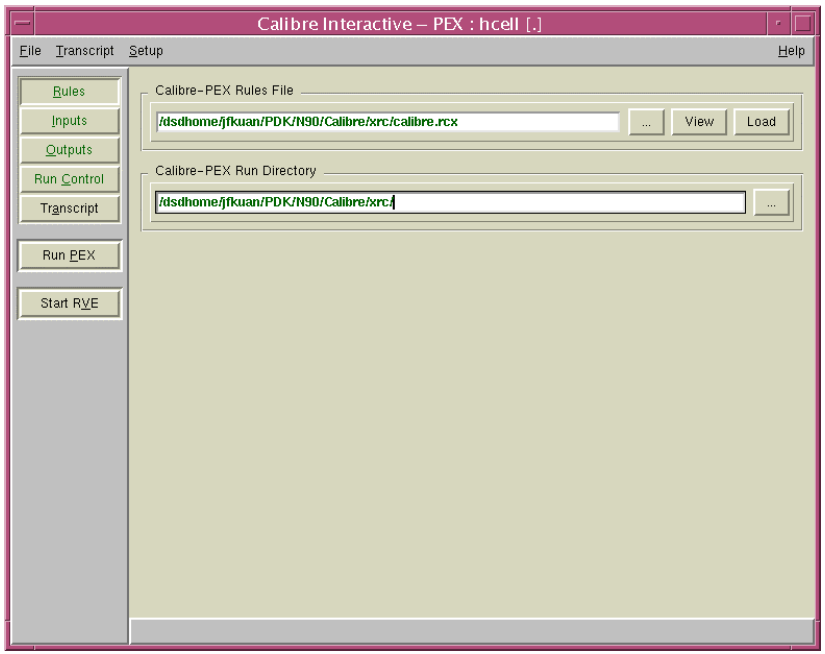


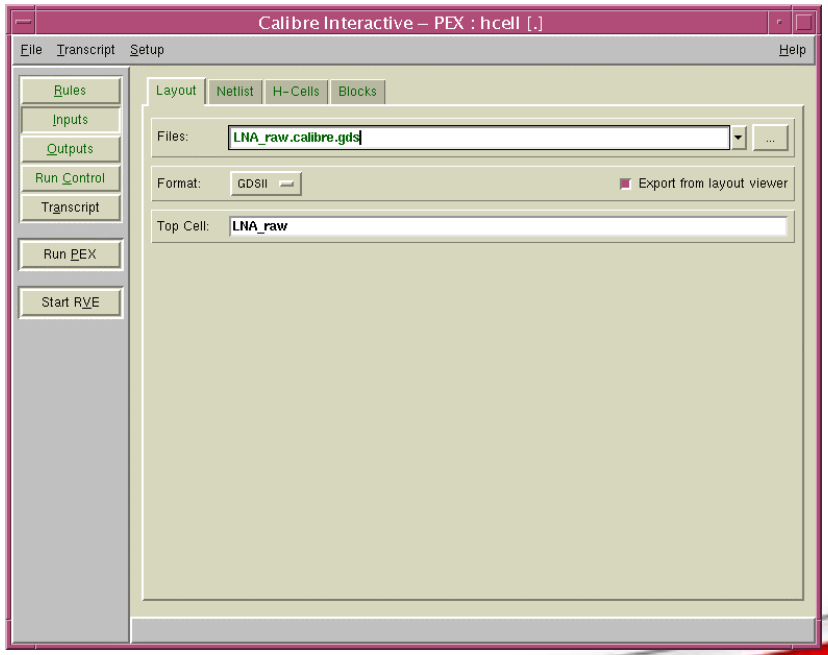
Calibre PEX Flow

In addition to directly obtain the ascii extracted netlist file from Calibre GUI mode extraction, you can also choose to obtain an extracted view 'calibre-view' which is somewhat like the Assura av_extracted view. In this calibre-view, you can see not only the original components and but also the parasitic devices and their connectivity. Furthermore, this calibre-view can also be used in Cadence Analog Artist environment for post-layout simulation.

1. Click "Calibre->Run PEX" in layout window to invoke Calibre PEX graphic user interface.

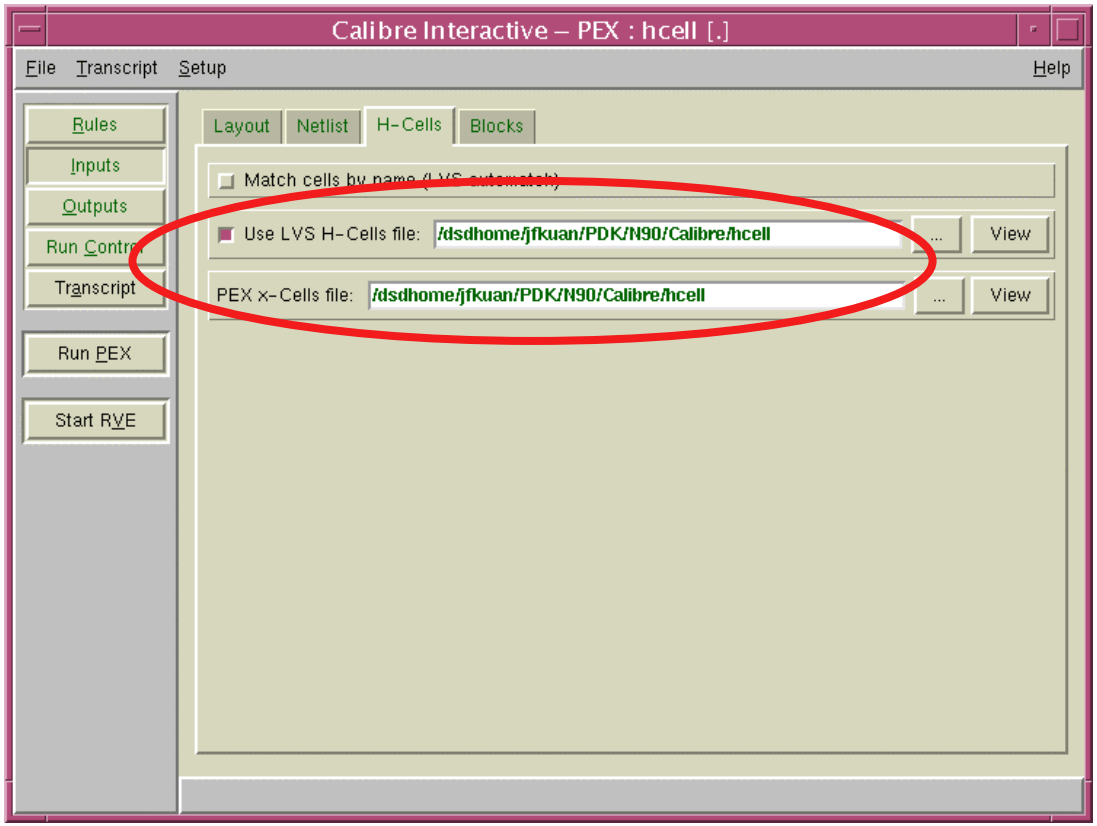
2. Specify the "Calibre-PEX rules file", working directory and "Top cell" in Calibre RCX window. If you need to change some RCX switches, you have to edit the Calibre RCX deck first.





Calibre PEX Flow

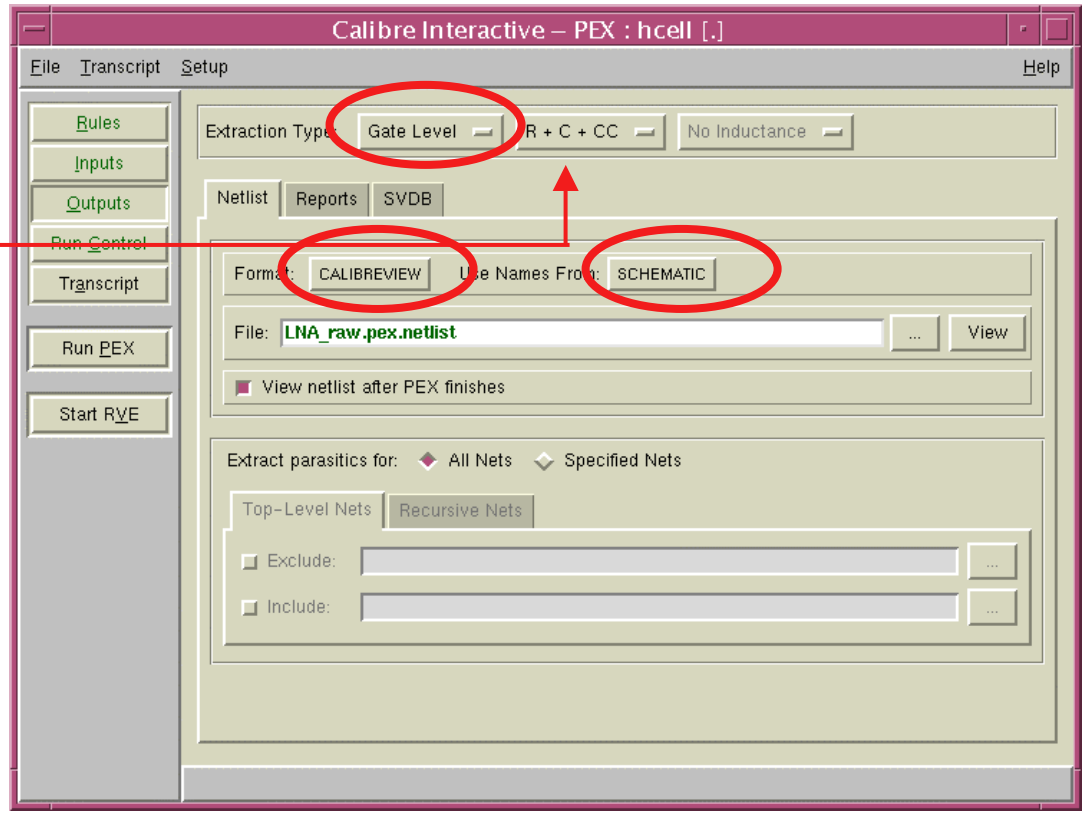
3. Enable "**Use LVS H-Cells file**" in" **Inputs->H-Cells**". Specify the H-cell file name and PEX x-Cell file name which is the h-cell file that we created before.



Calibre PEX Flow

4. Select the "**Outputs**", set the "**Extraction Type**" to "**Gate Level**". Specify the output format to be "**CALIBREVIEW**" and "Use Names From" to be "**SCHEMATIC**".

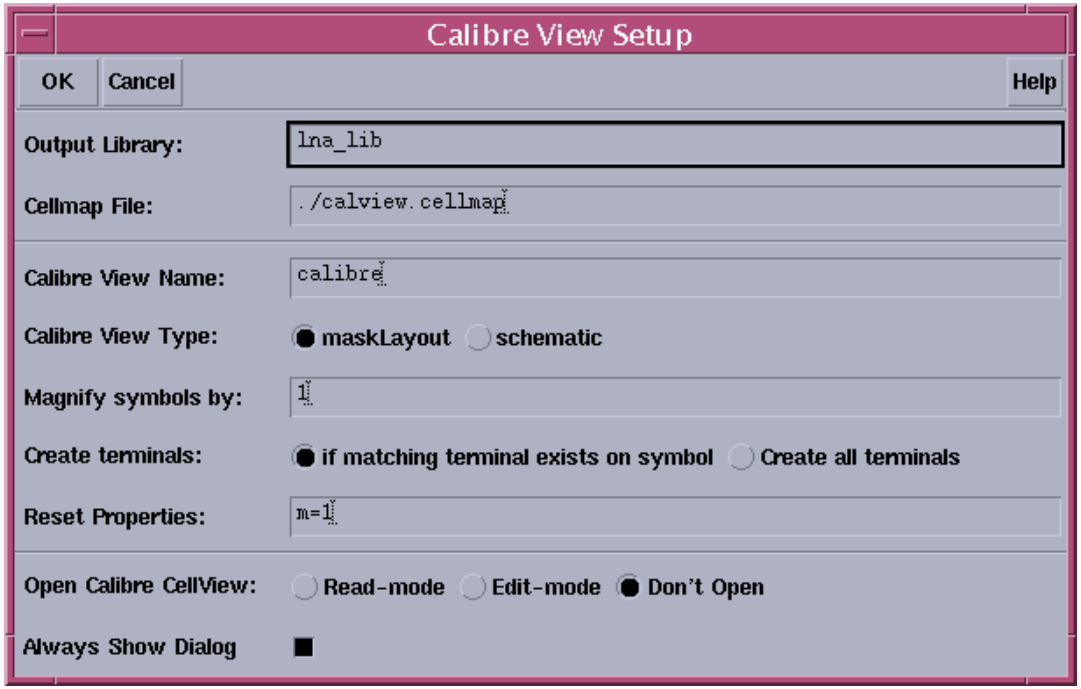
Select which extraction type you want to run.
(no parasitic, C+CC, R, R+C, R+C+CC)



Calibre PEX Flow

4. Click “OK” to run the Calibre GUI RC extraction. After the extraction run is completed, a calibre view setup window pops up. Specify the “Cellmap File”, “Magnify symbols by” .

5. Click “OK” in the Calibre view setup window to create the Calibre view.



Contents

Post-layout Simulation

When you accomplished the physical verification, the last step to tape-out is to perform the post-layout simulation on the extracted netlist/view. During the post-layout simulation, not only the original components but also the parasitic R & C (depends on what you have extracted in RCX stage) of the interconnections are taken into consideration. Therefore, we can say that the post-layout simulation result is much closer to the real silicon measurement data than the original pre-layout simulation result. Furthermore, base on the difference of RC extraction flows you chose you would run your post-layout simulation in different ways.

- **Assura RCX extracted view**
  - C-only mode
  - **RC mode**
- **Calibre XRC extracted view**
  - C+CC mode
  - R+C+CC mode

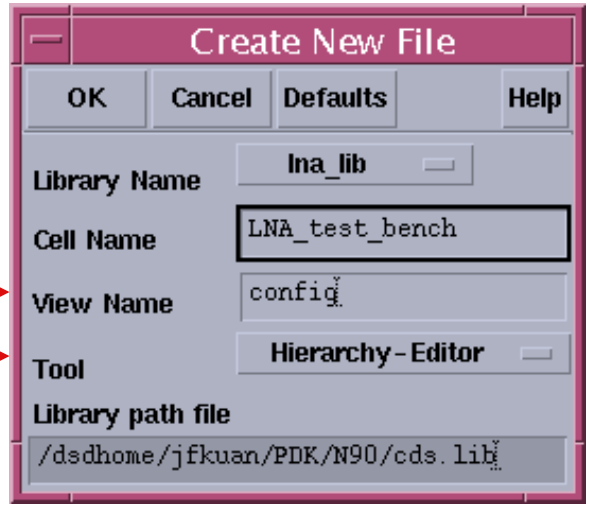
Post-layout Simulation

- **Creating a Configuration file for Post-layout simulation**

1. In the CIW or Library Manager, select File->New->Cellview.
2. Set up the Create New File form as follows:

Enter the new view name into the Name field →

Select “Hierarchy-Editor” →

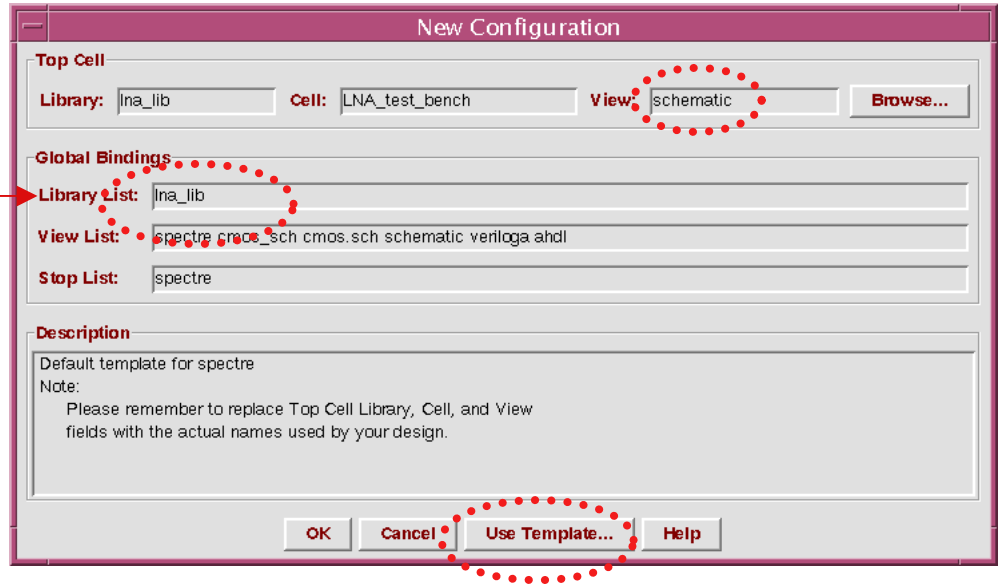


Post-layout Simulation

3. At the top the form enter the view to “schematic”, and at the bottom, click on the “Use Template…”.

4. The Use Template form opens; cycle the Name to spectre and click OK then the “New Configuration” form is like below:

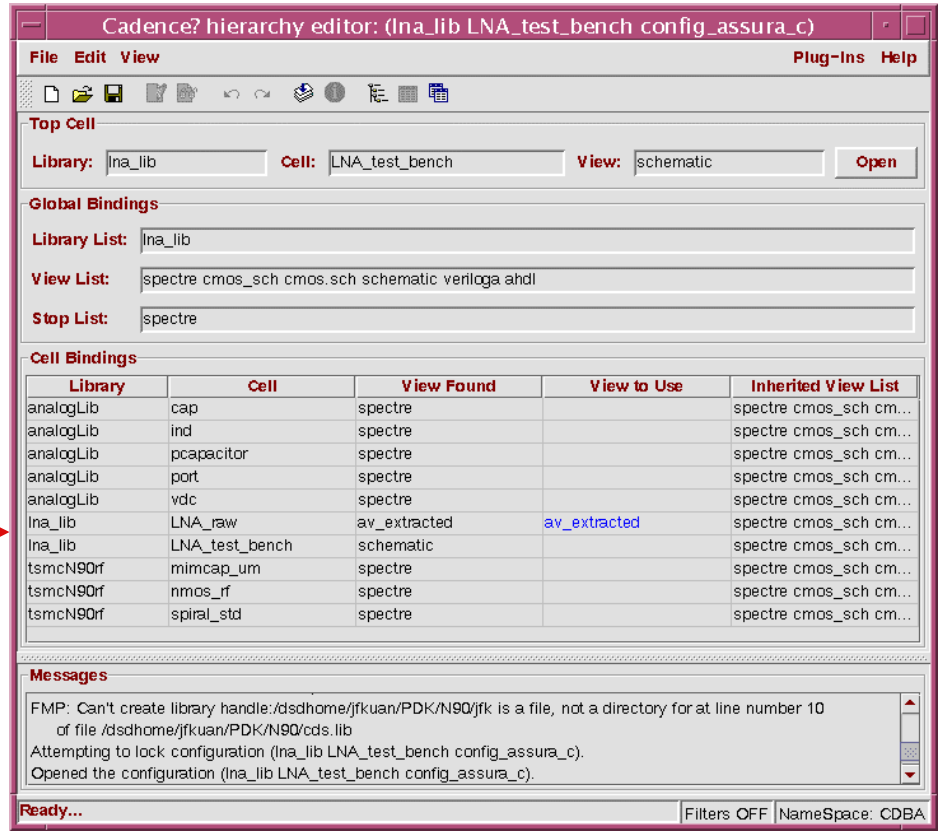
Make sure that you change the default name to “lna_lib”



Post-layout Simulation

5. Edit the hierarchy for the design:
   Change the “View to Use” to which you want at “LNA_raw” cell and save the file.

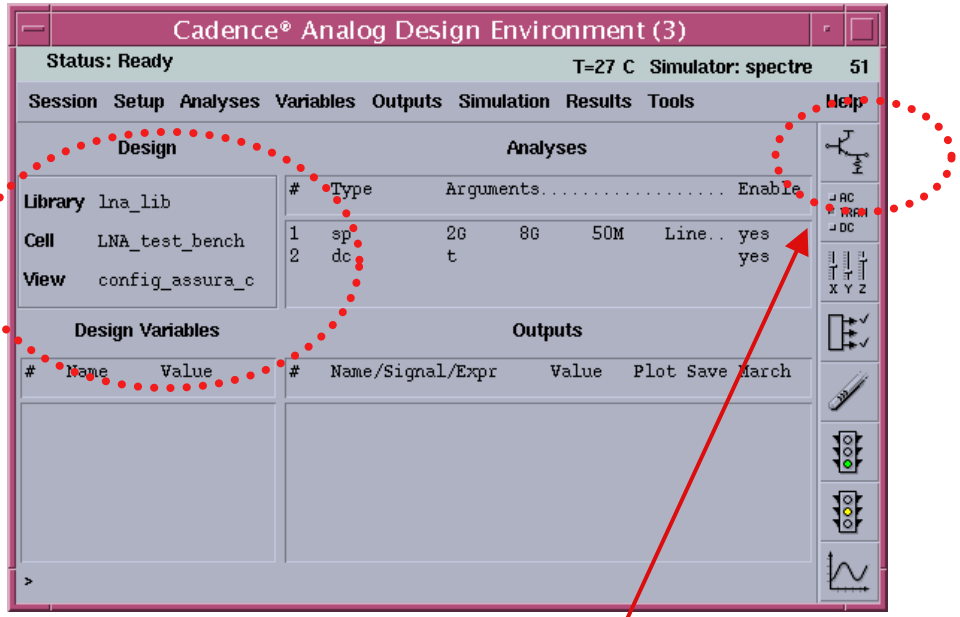
You can change the view that you have created by extraction tool.



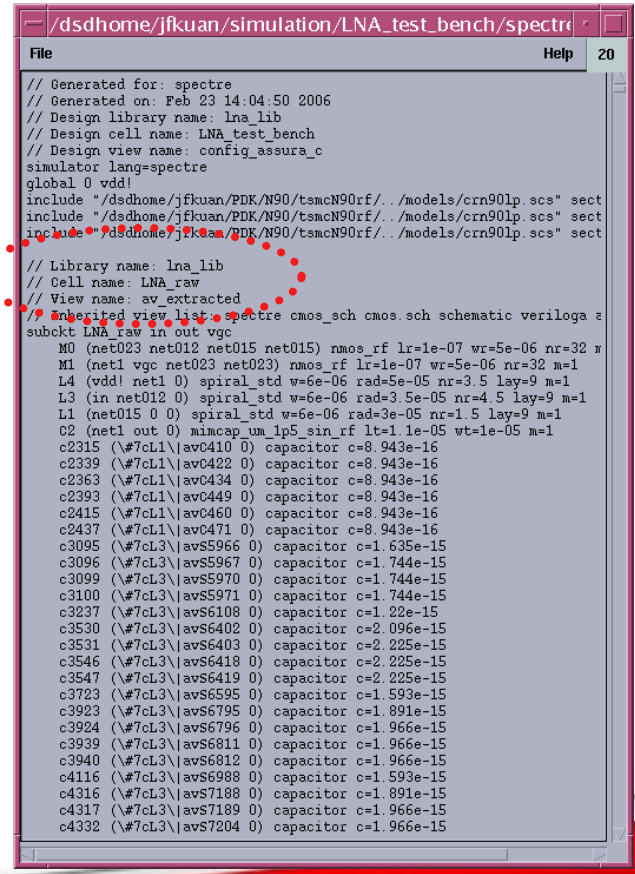
Post-layout Simulation

- **Run post-layout simulation with extracted view**

Now, you can run post-layout simulation by changing design setup to configuration created previously. You can output the netlist to make sure a correct view is used for post-layout simulation.



You can change the design setup by clicking this icon.

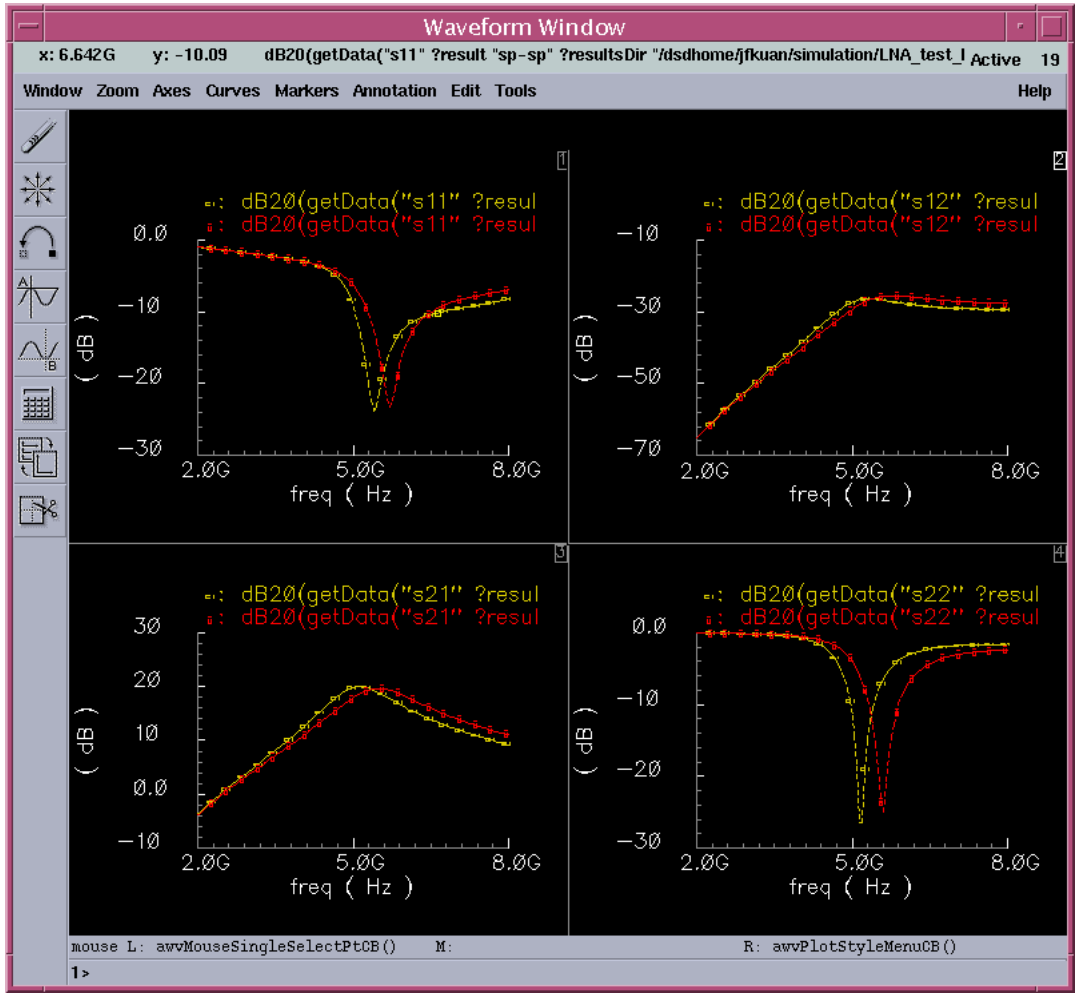


Post-layout Simulation Result

After completing the post-layout simulation. We will check the result between different RC extraction methods.

- **Assura RCX extracted view**
  - Assura C-only mode v.s. Pre-layout simulation
  - **Assura RC mode v.s. Pre-layout simulation**
- **Calibre XRC extracted view**
  - Calibre C+CC mode v.s. Pre-layout simulation
  - Calibre R+C+CC mode v.s. Pre-layout simulation
- **Comparison**
  - Assura C-only mode v.s. Calibre C+CC mode
  - Calibre C+CC mode v.s. Calibre R+C+CC mode
  - **Assura RC mode v.s. Calibre R+C+CC mode**

Assura C-only mode v.s. Pre-layout simulation

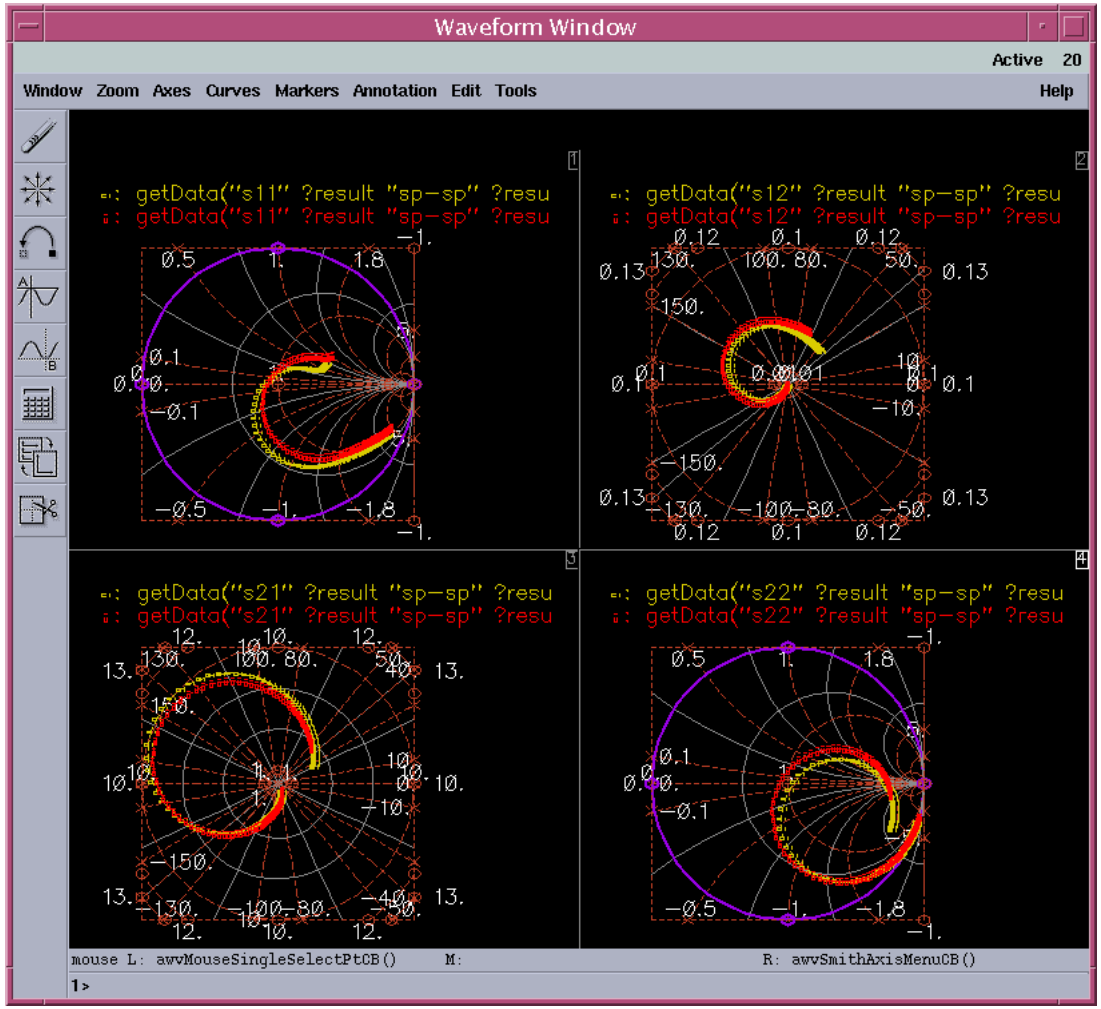


Red : Pre-layout simulation
Yellow : Assura C-only mode

S11	S12
S21	S22

S-paramter (20dB)

Assura C-only mode v.s. Pre-layout simulation

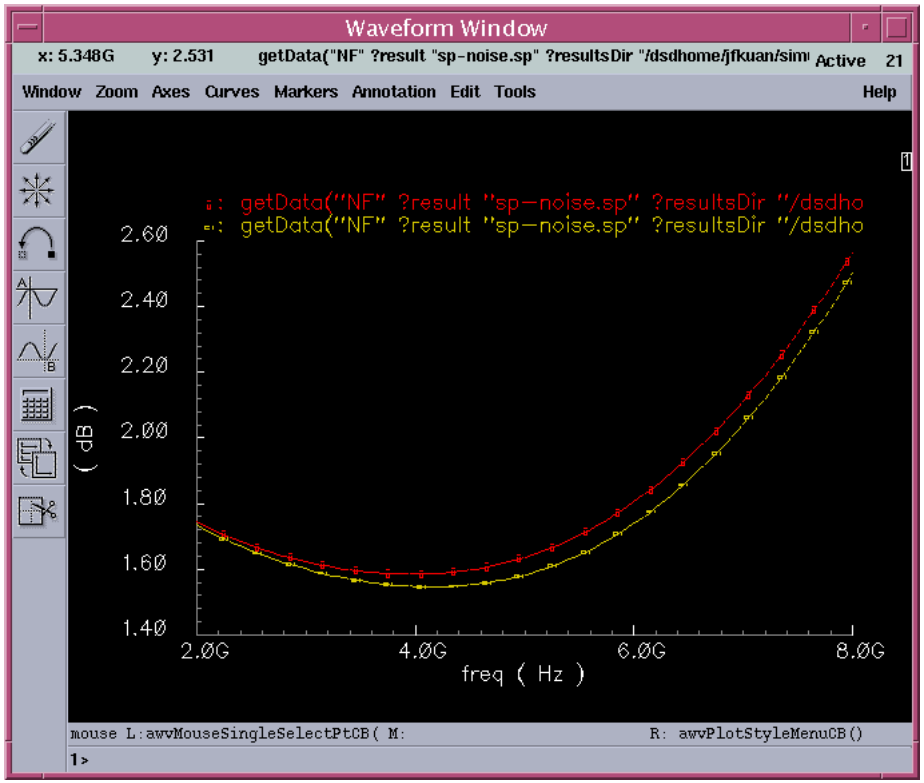


S-paramter

Red : Pre-layout simulation
Yellow : Assura C-only mode

S11	S12
S21	S22

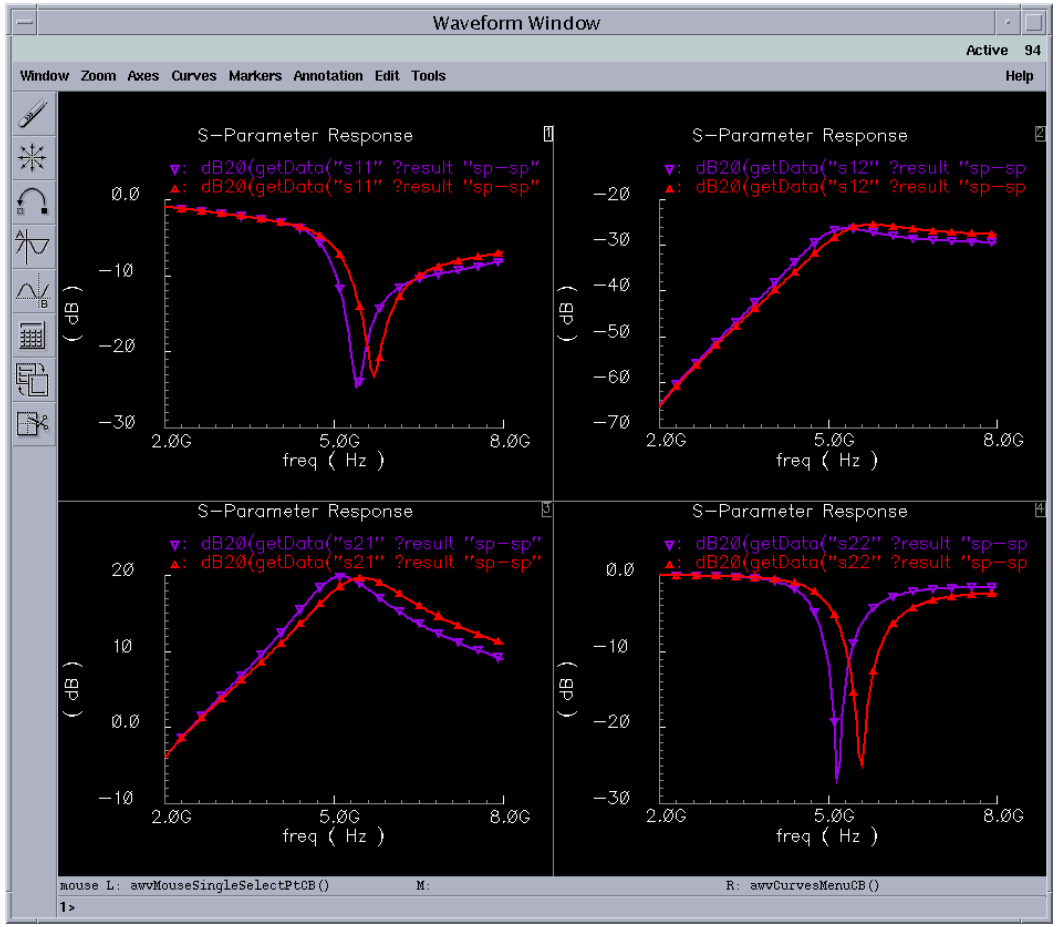
Assura C-only mode v.s. Pre-layout simulation



Red : Pre-layout simulation
Yellow : Assura C-only mode

Noise Figure

Assura RC mode v.s. Pre-layout simulation

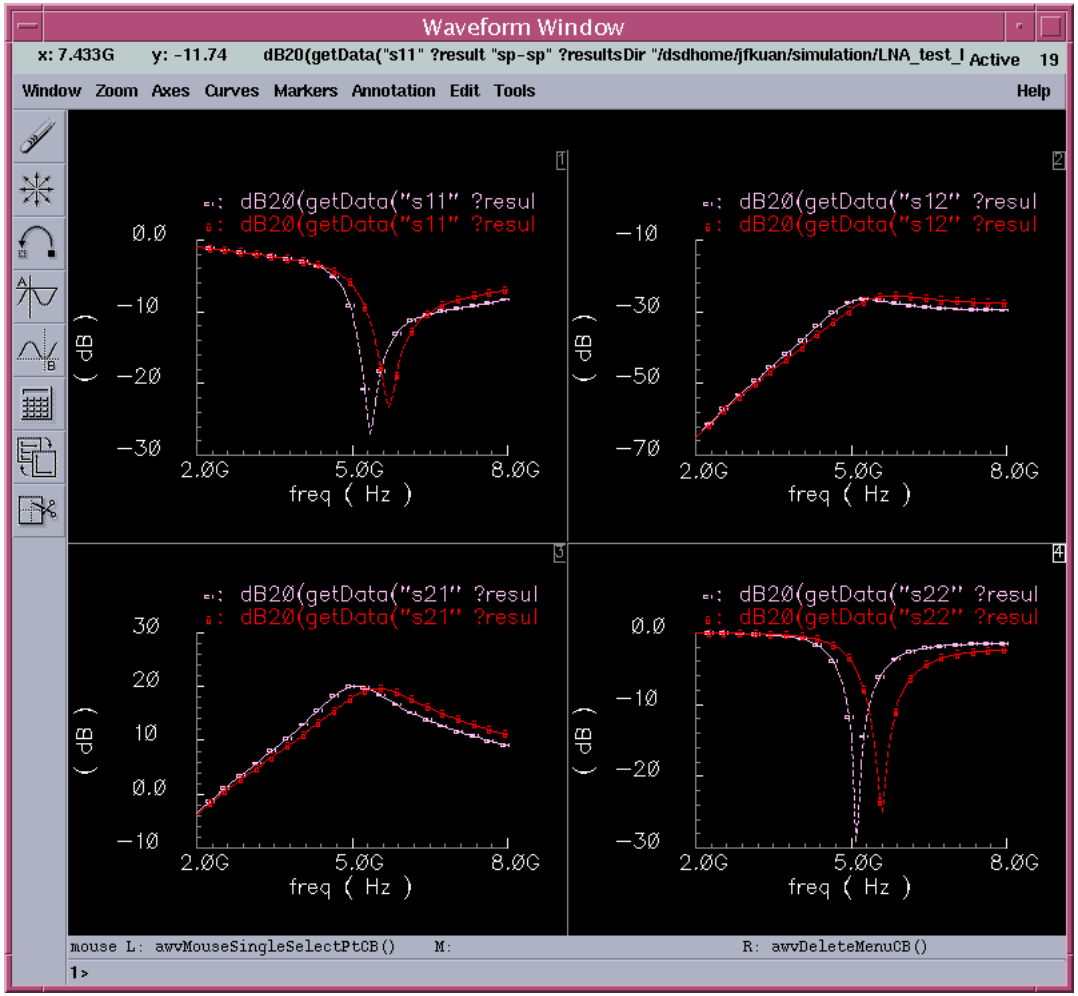


Red : Pre-layout simulation
Purple : Assura RC mode

S11	S12
S21	S22

S-paramter (20dB)

Calibre C+CC mode v.s. Pre-layout simulation

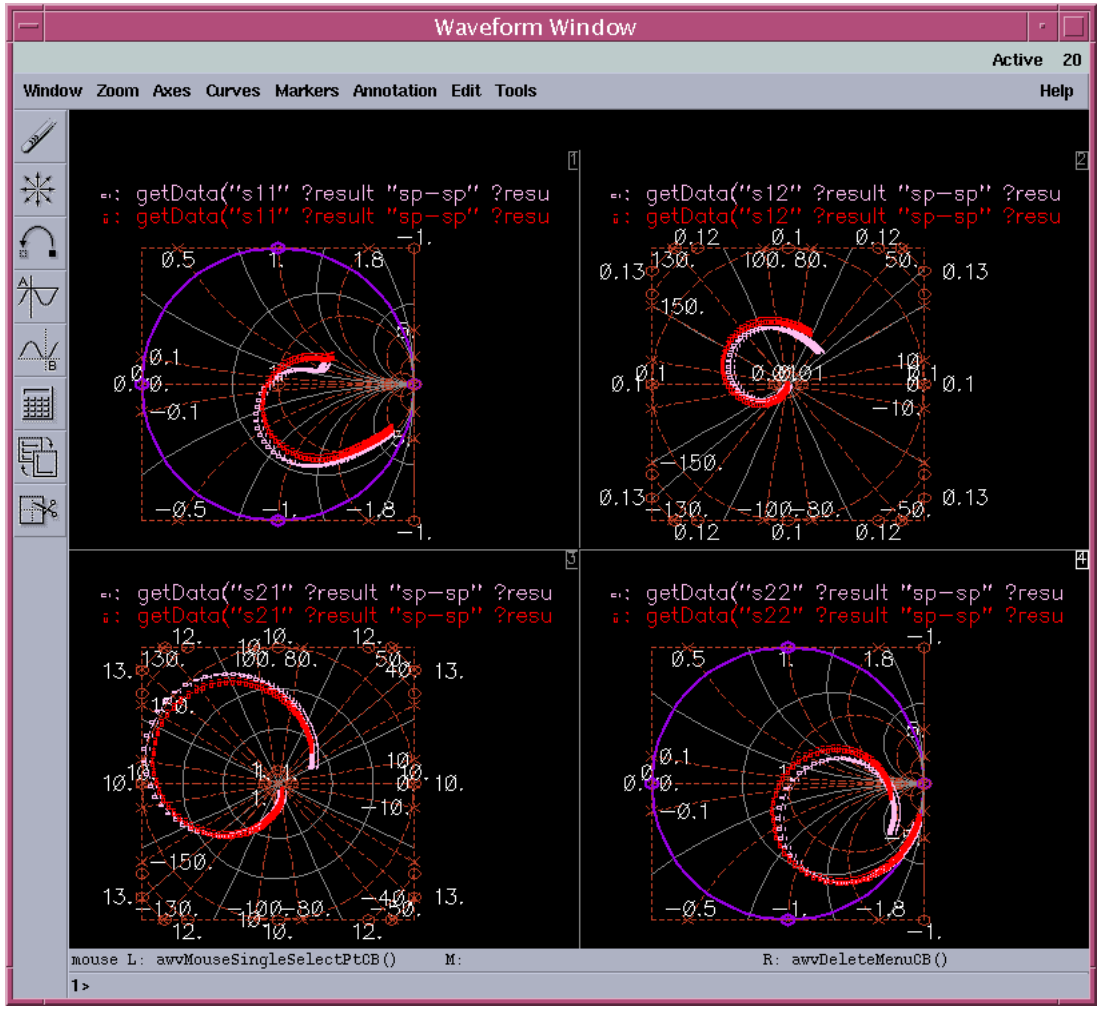


Red : Pre-layout simulation
Pink : Calibre C+CC mode

S11	S12
S21	S22

S-paramter (20dB)

Calibre C+CC mode v.s. Pre-layout simulation

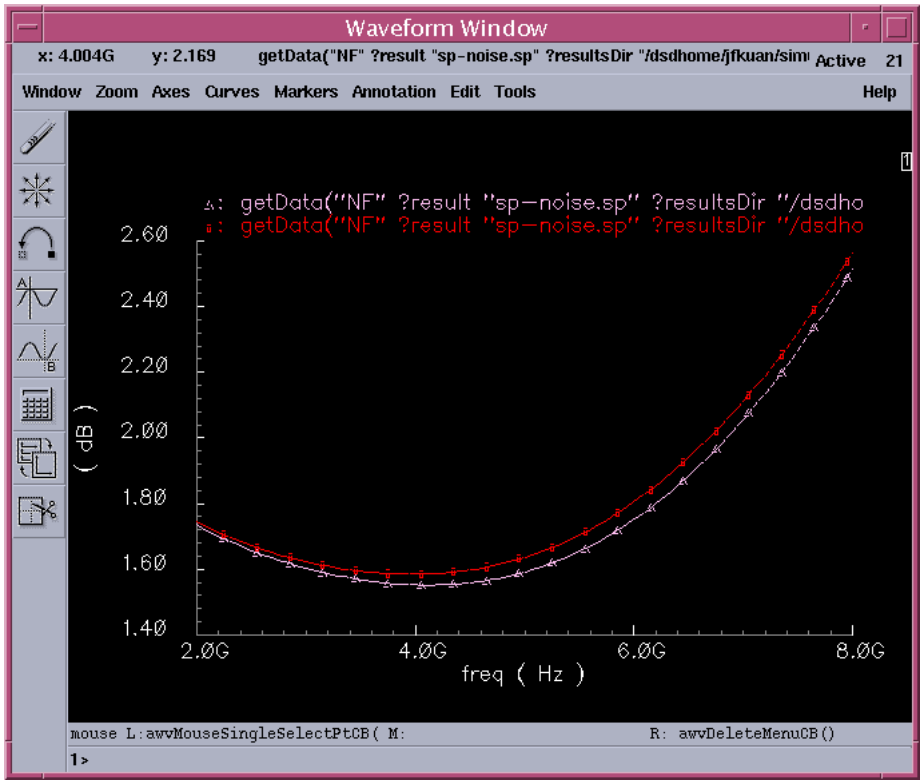


S-paramter

Red : Pre-layout simulation
Pink : Calibre C+CC mode

S11	S12
S21	S22

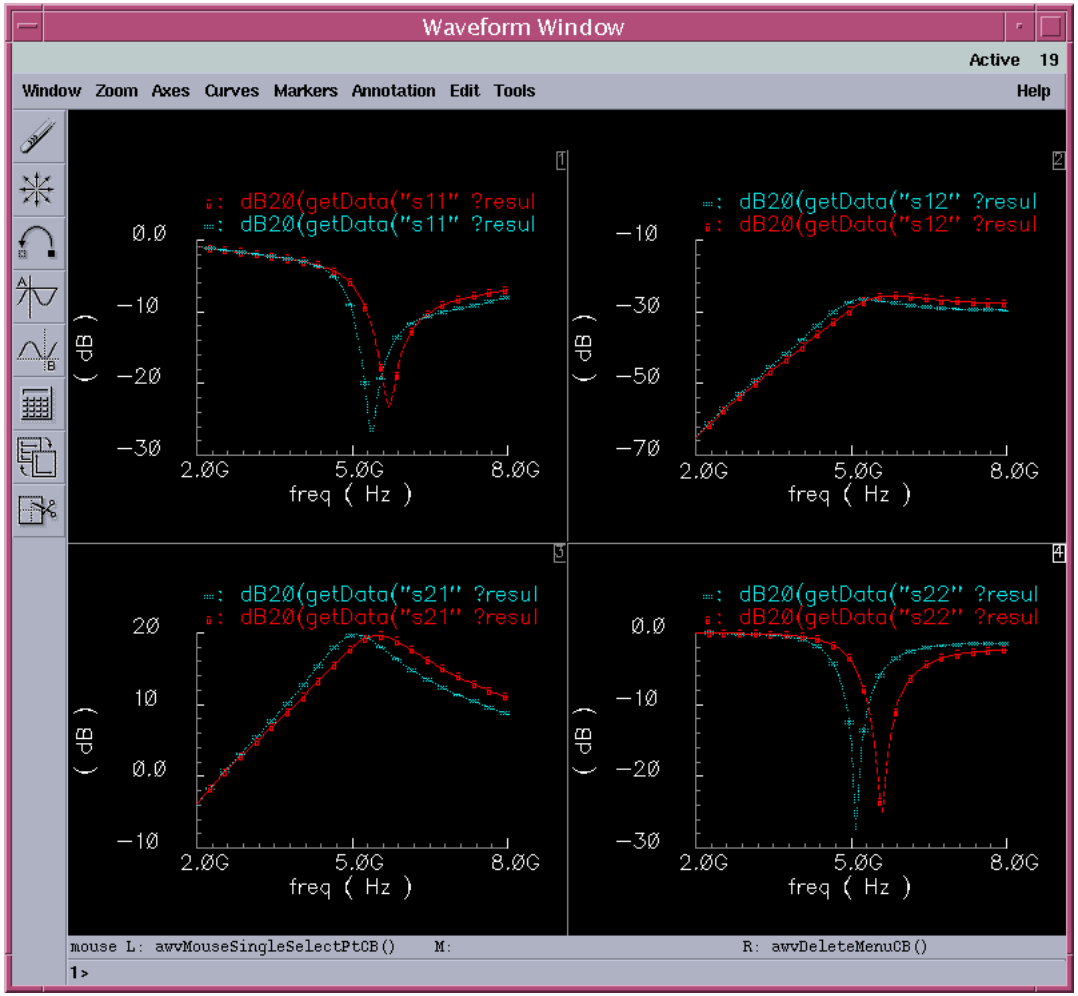
Calibre C+CC mode v.s. Pre-layout simulation



Red : Pre-layout simulation
Pink : Calibre C+CC mode

Noise Figure

Calibre R+C+CC mode v.s. Pre-layout simulation

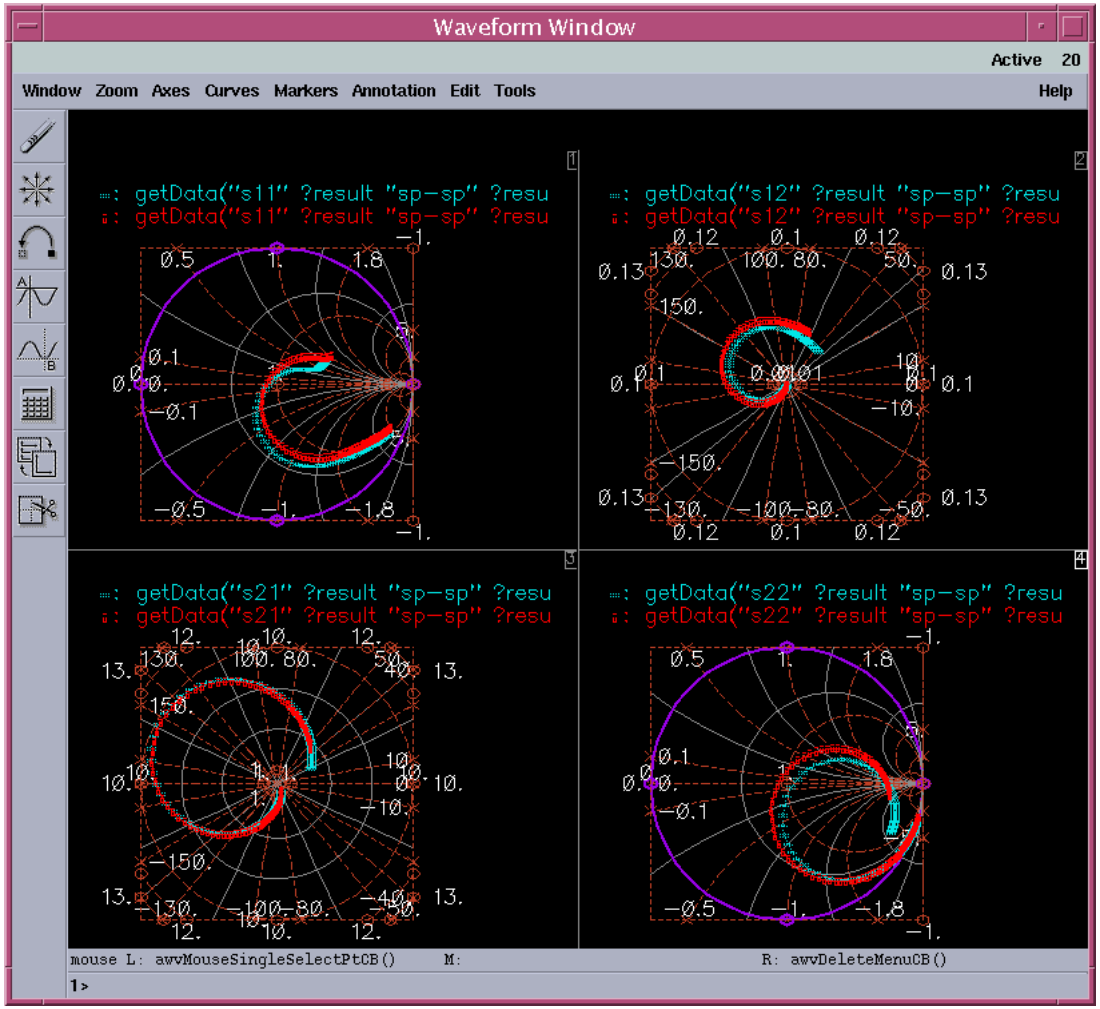


S-paramter (20dB)

Red : Pre-layout simulation
Blue : Calibre R+C+CC mode

S11	S12
S21	S22

Calibre R+C+CC mode v.s. Pre-layout simulation

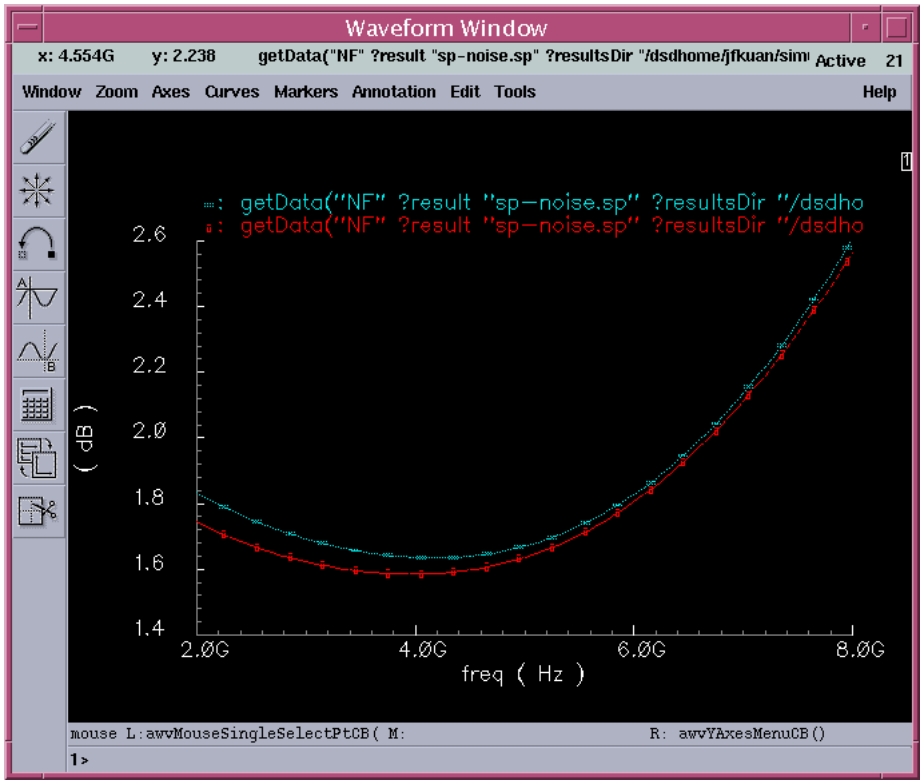


S-paramter

Red : Pre-layout simulation
Blue : Calibre R+C+CC mode

S11	S12
S21	S22

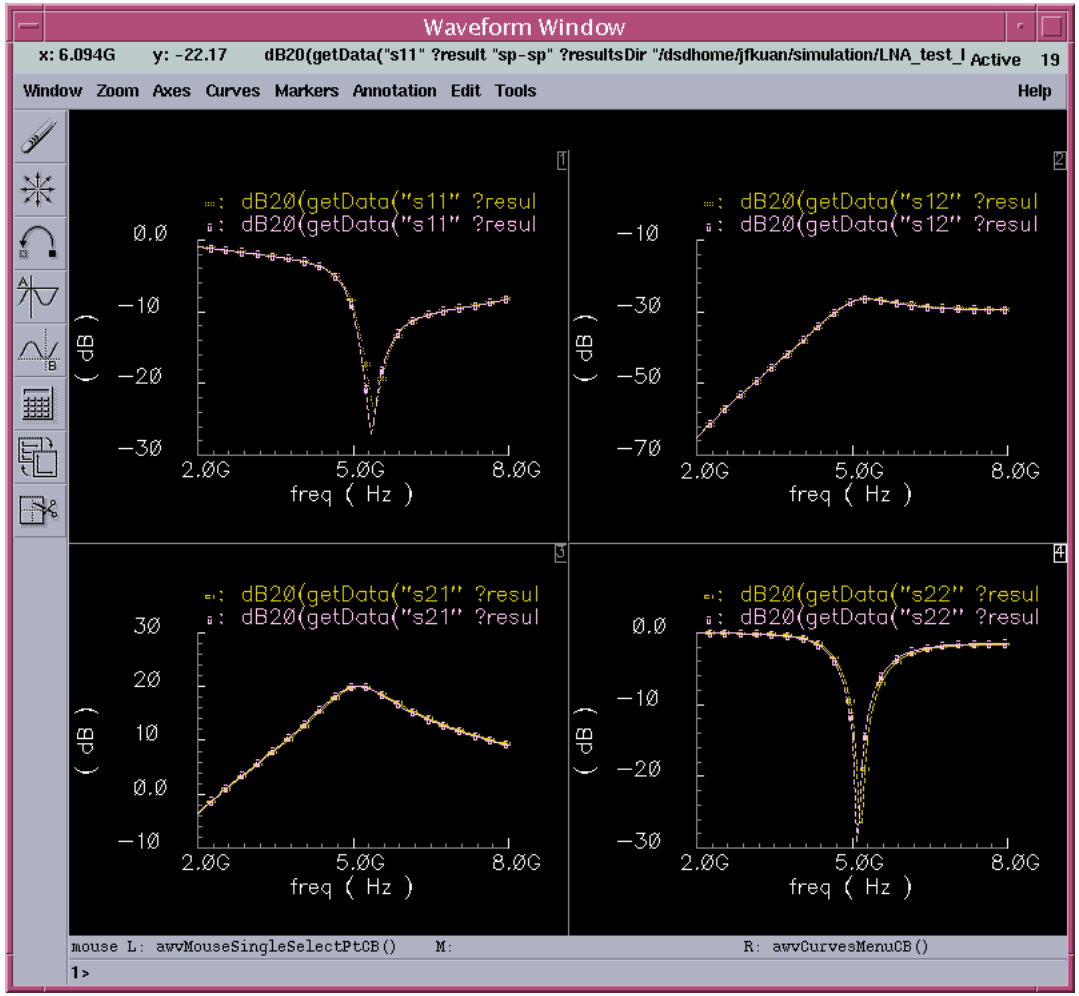
Calibre R+C+CC mode v.s. Pre-layout simulation



Red : Pre-layout simulation
Blue : Calibre R+C+CC mode

Noise Figure

Assura C-only mode v.s. Calibre C+CC mode

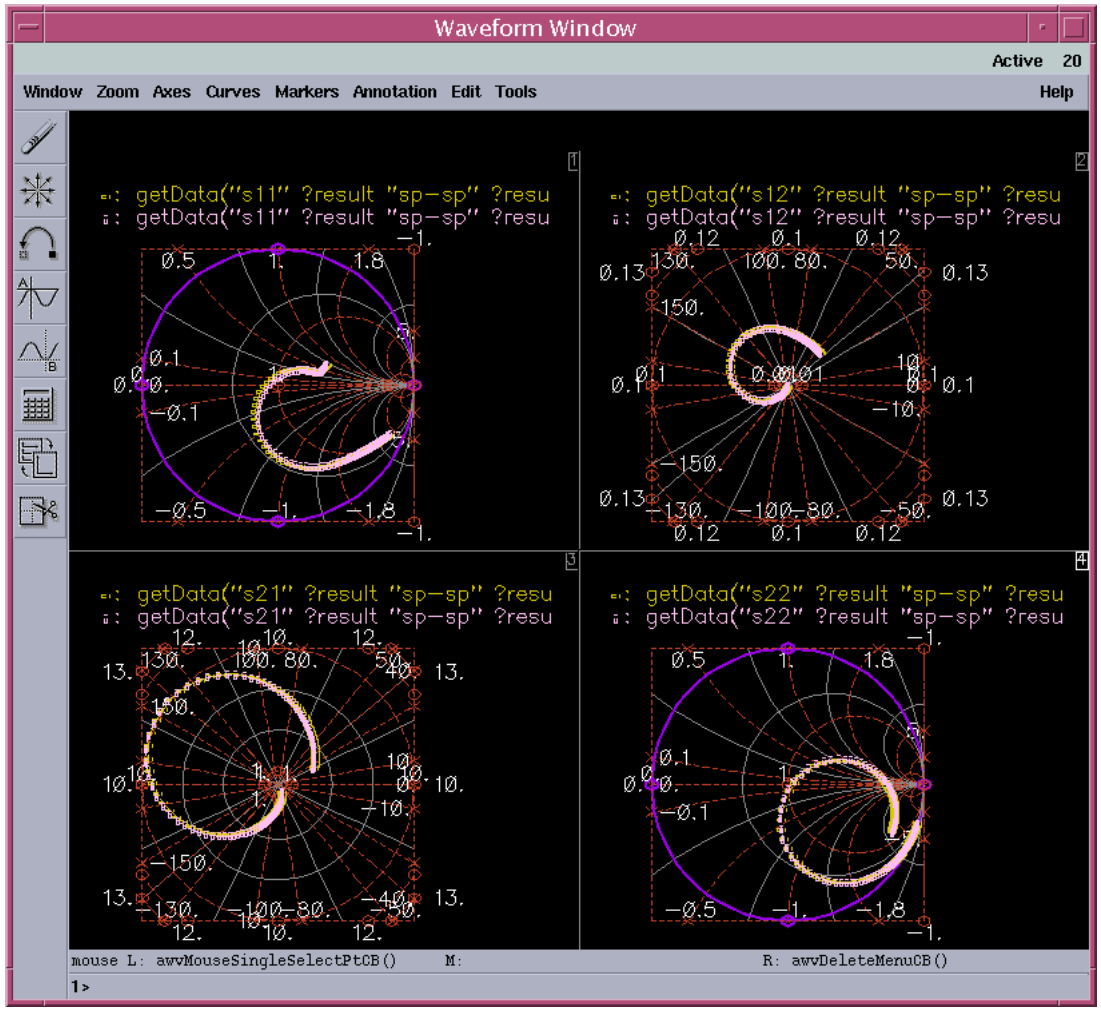


Yellow : Assuua C-only mode
Pink : Calibre C+CC mode

S11	S12
S21	S22

S-paramter (20dB)

Assura C-only mode v.s. Calibre C+CC mode

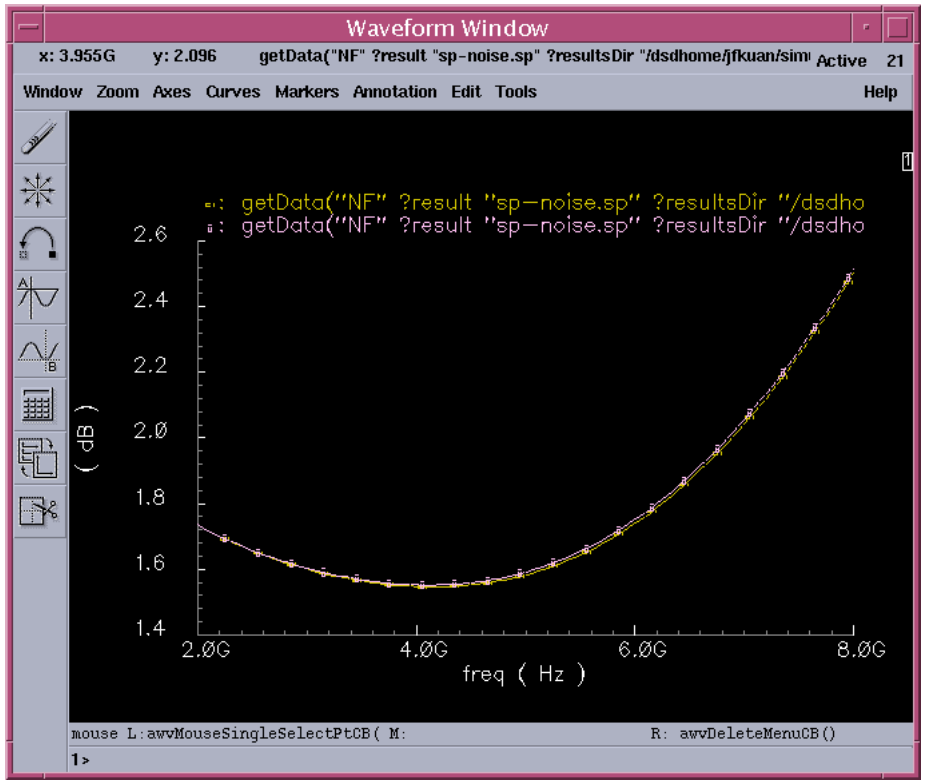


S-paramter

Yellow : Assuua C-only mode
Pink : Calibre C+CC mode

S11	S12
S21	S22

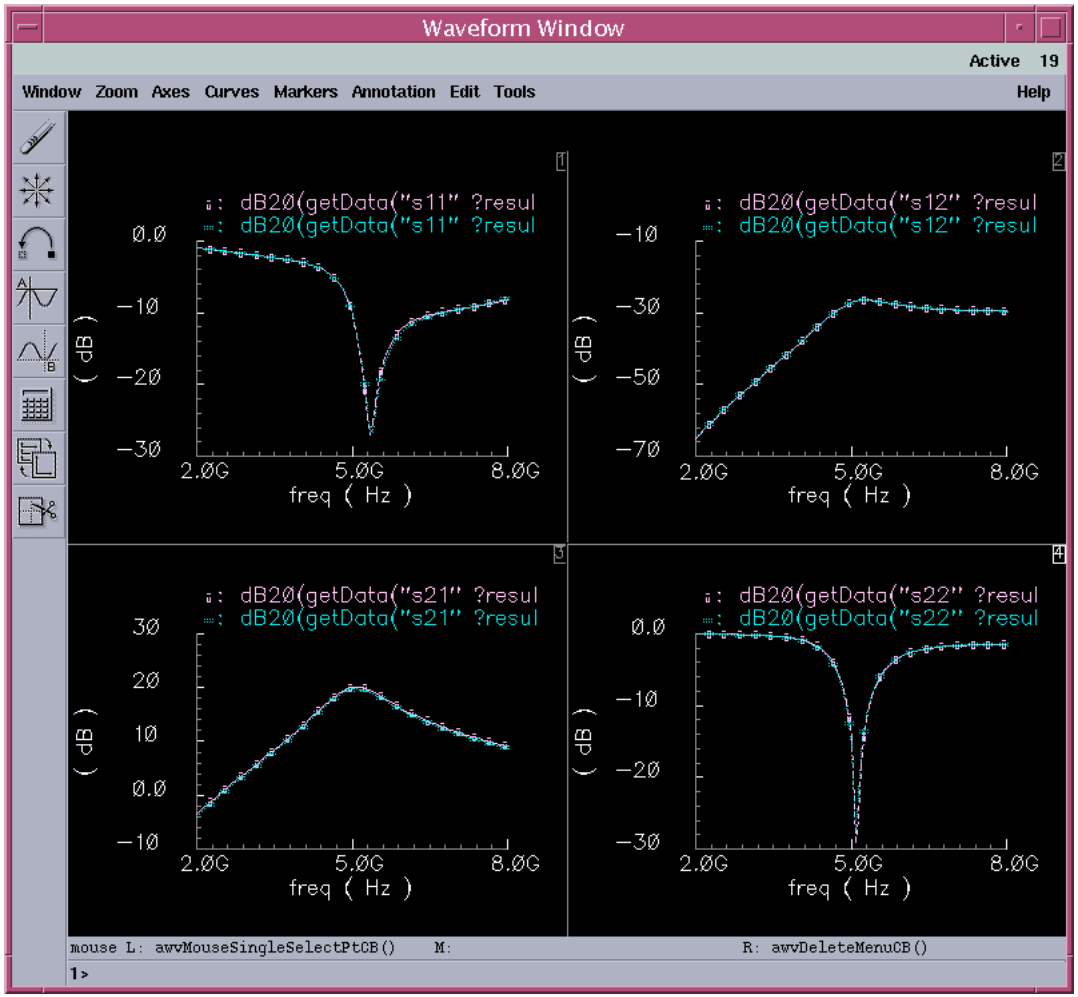
Assura C-only mode v.s. Calibre C+CC mode



Yellow : Assuua C-only mode
Pink : Calibre C+CC mode

Noise Figure

Calibre C+CC mode v.s. Calibre R+C+CC mode

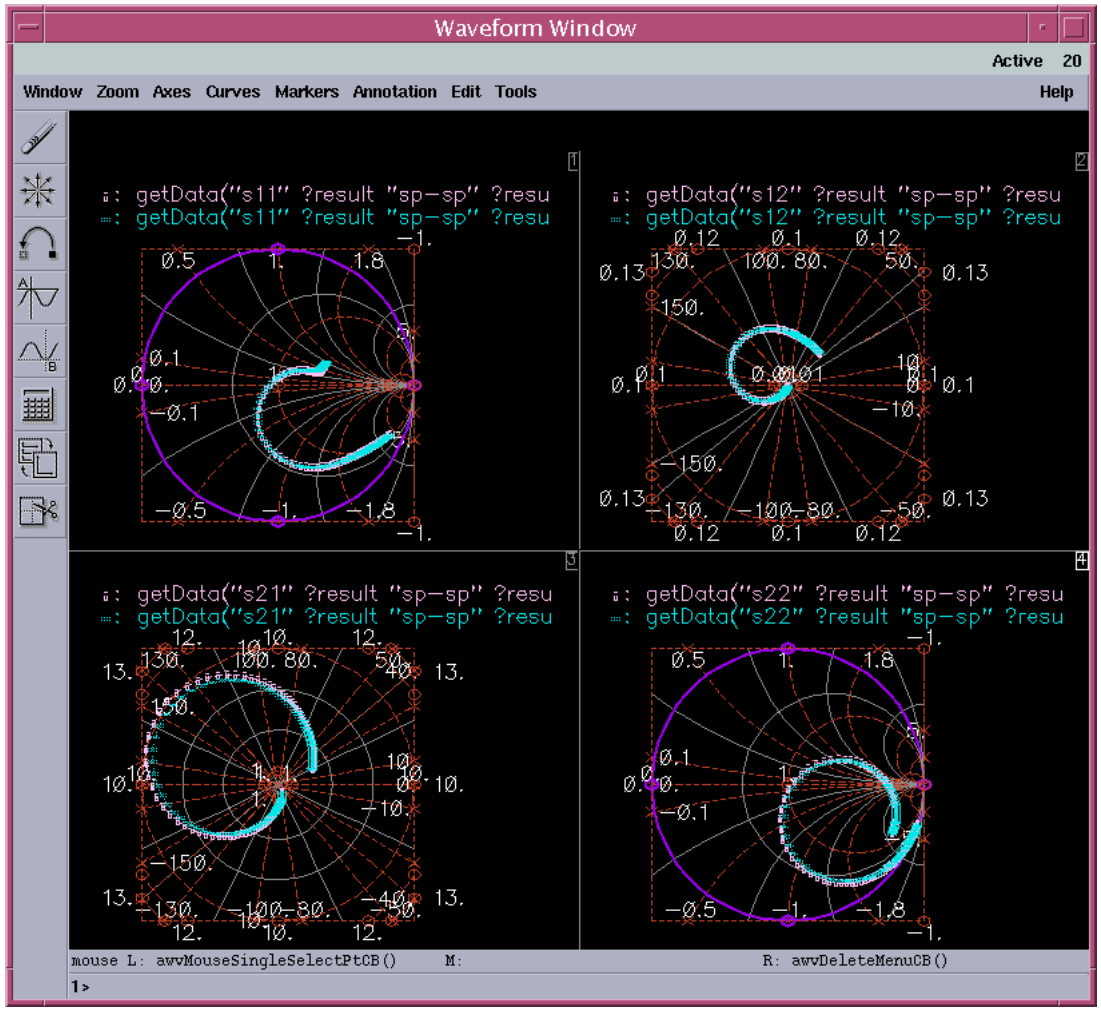


Pink : Calibre C+CC mode
Blue : Calibre R+C+CC mode

S11	S12
S21	S22

S-paramter (20dB)

Calibre C+CC mode v.s. Calibre R+C+CC mode

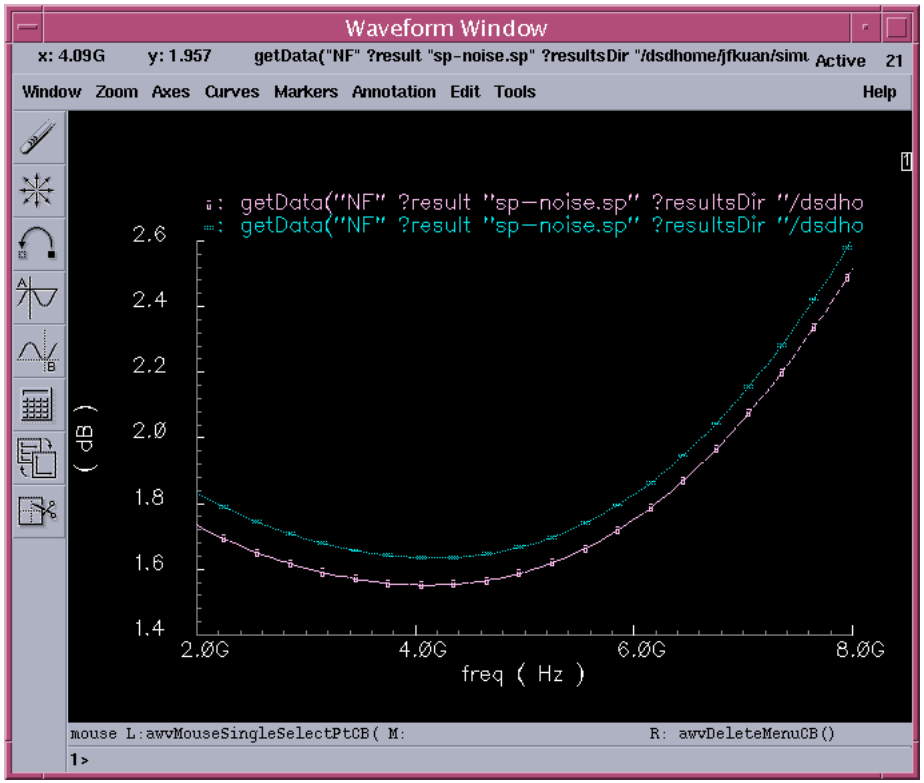


S-paramter

Pink : Calibre C+CC mode
Blue : Calibre R+C+CC mode

S11	S12
S21	S22

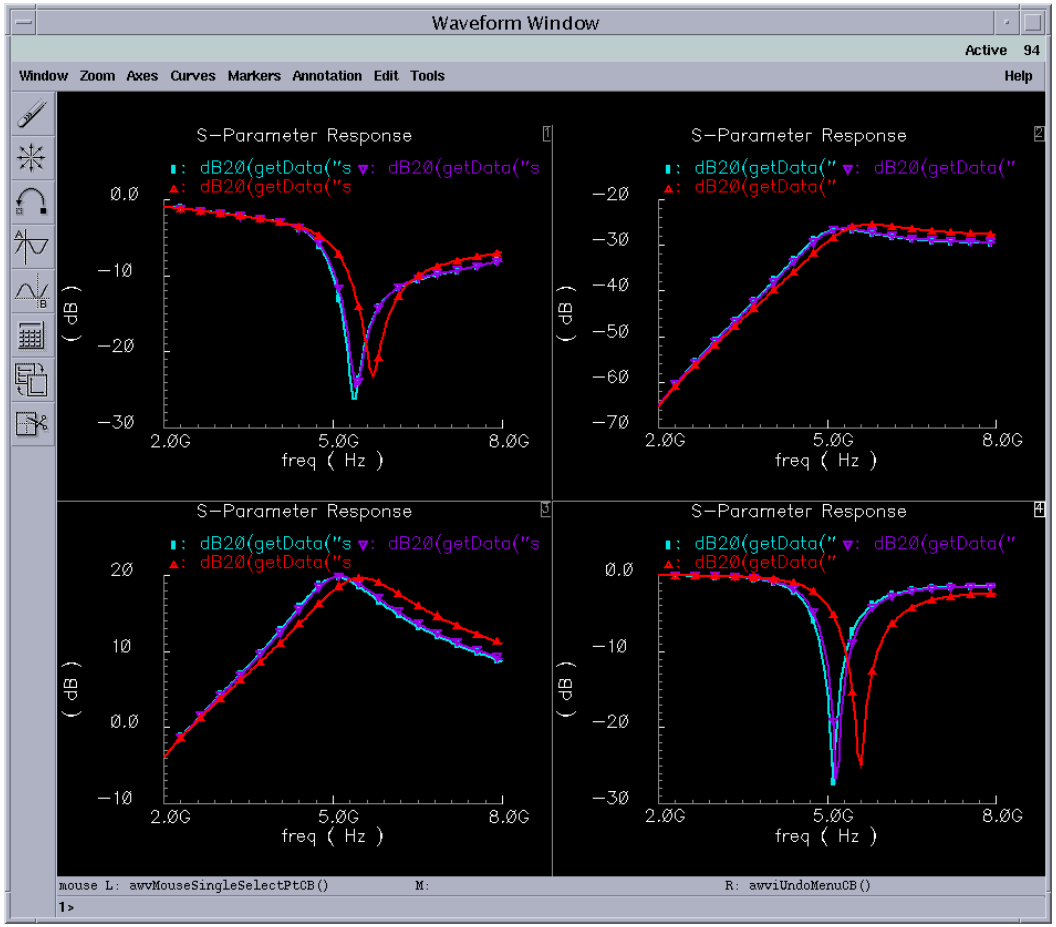
Calibre C+CC mode v.s. Calibre R+C+CC mode



Pink : Calibre C+CC mode
Blue : Calibre R+C+CC mode

Noise Figure

Assura RC mode v.s. Calibre R+C+CC mode

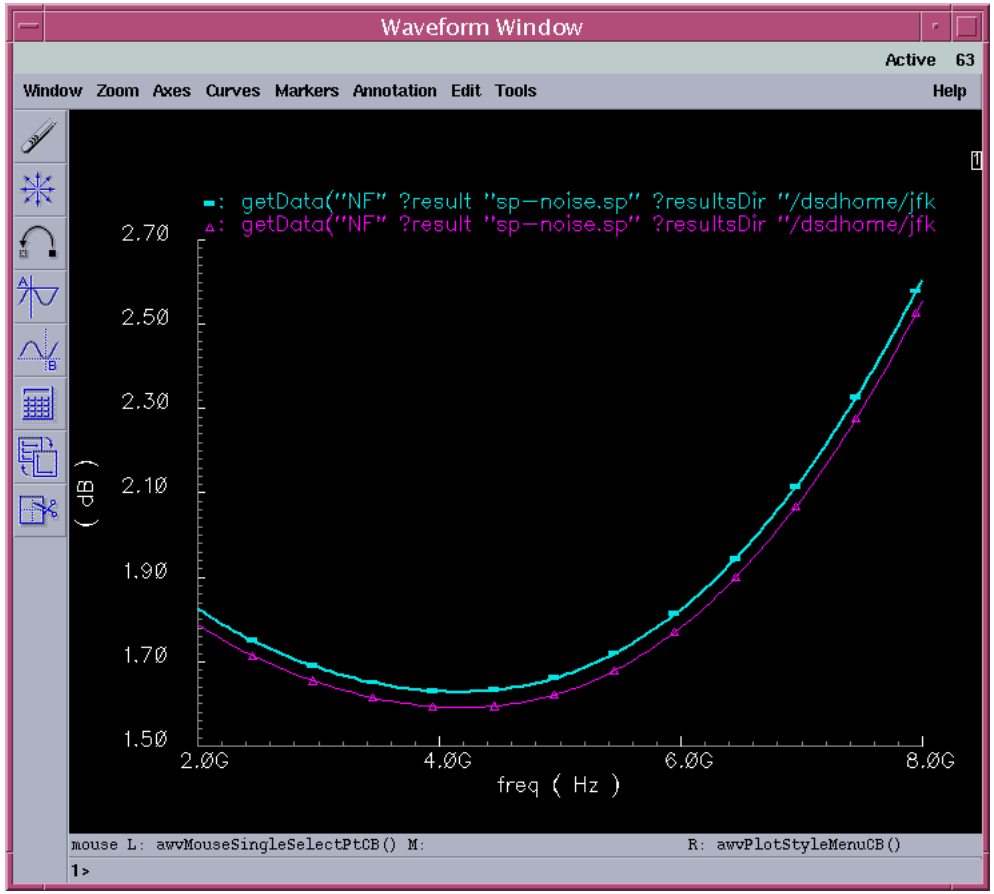


Red : Pre-layout simulation
Blue : Calibre R+C+CC mode
Purple : Assura RC mode

S11	S12
S21	S22

S-paramter (20dB)

Assura RC mode v.s. Calibre R+C+CC mode



Blue: Calibre R+C+CC mode
Purple : Assura RC mode

Noise Figure

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