# EECS240 – Spring 2010

**Lecture 24: PLL and CDR Overview**

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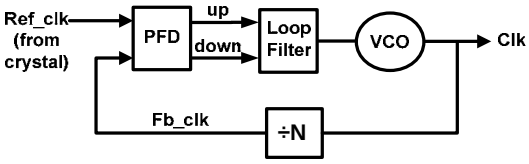
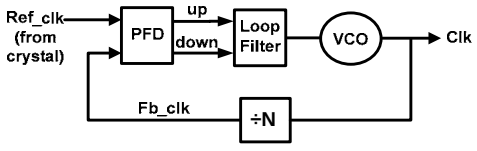
## Clock Generation




- **Typical (low-cost) crystals give <500 MHz clock**
  - **5 Gb/s link → where to get a 5 GHz clock?**
- **PLL: multiply frequency up, align phase**
  - **While maintaining low jitter, power**



## PLL: Linear Model






## Linear Model cont'd



## Stability and Loop Bandwidth



## Loop Components: Phase Detectors

- **Basic idea: create pulses with width $\alpha$ to phase difference**

## Loop Filter



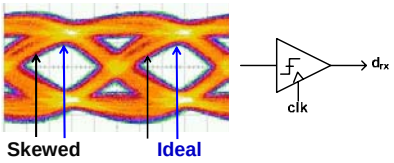
## VCOs



## Noise and Jitter



## Clock Recovery




- Voltage margin strongly dependent on exact sampling position
- How do we set the clock at the "best" place?

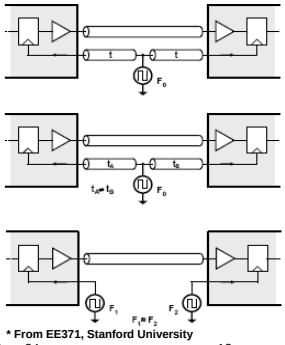


## Conceptual CDR



## System Types

- (Source) Synchronous
  - Same frequency & phase
- Mesochronous
  - Same frequency, unknown phase
- Plesiochronous
  - Almost same frequency

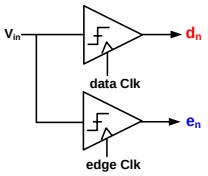


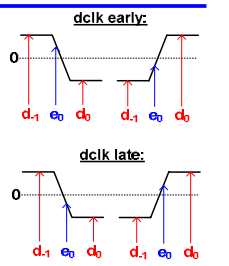
* From EE371, Stanford University

## Linear (Hogge) Phase Detector



## Bang-Bang (Alexander) Phase Detector




- Edge clock $T_{sym}/2$ away from data
- Derive early/late from data and edge samples:
  - Dn: $(d_n != e_n)$ & $(d_{n-1} != d_n)$
  - Up: $(d_n == e_n)$ & $(d_{n-1} != d_n)$

* LF can be analog or digital