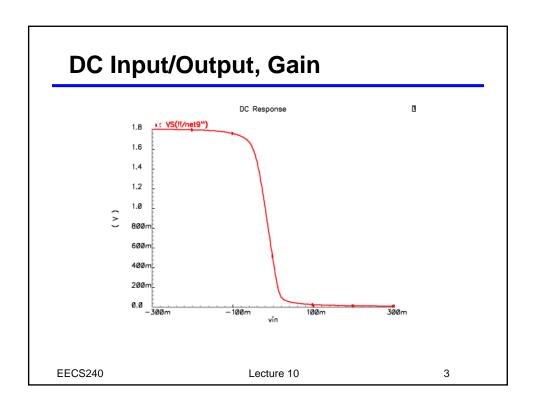
EECS240 – Spring 2010

Lecture 10: Single-Ended and Differential OTAs



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Simplest Single-Ended OTA



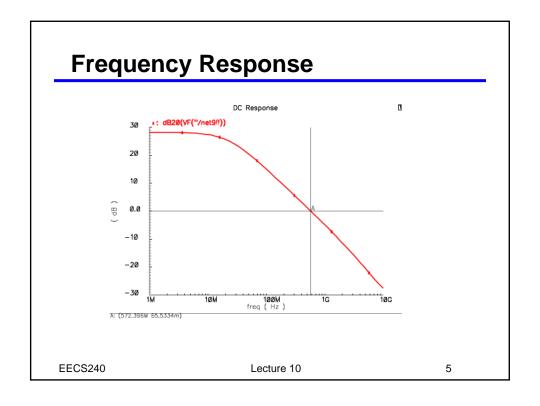
Gain, Output Range

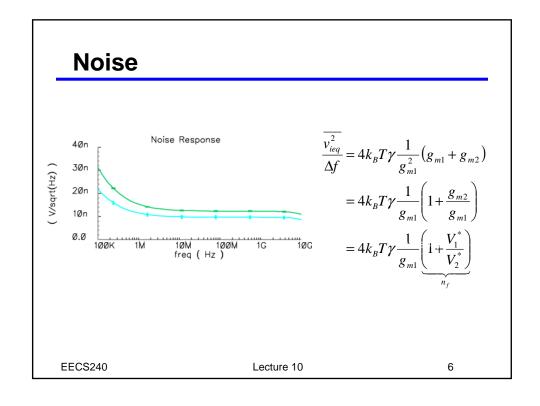
• Small Signal:

$$a_{vo} = \frac{dV_{out}}{dV_{in}}$$

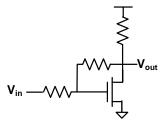
• Large Signal:

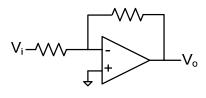
$$A_{vo} = \frac{V_{out} - V_{out_o}}{V_{in} - V_{in_o}}$$





Differential Input?

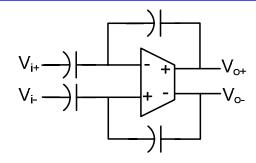




- Why use a differential input?
 - Diff. version has extra device(s) more power, noise, etc.
- Real reason is systematic offset
 - · All voltages are relative
- Inherent asymmetry to get single-ended Vout
 - "common-mode" sensitivity

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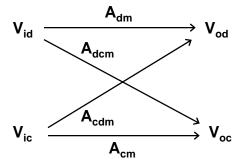
Fully Differential Circuits



- Fully differential circuits: complete symmetry
 - $V_{id} = V_{i+} V_{i-}$ $V_{ic} = (V_{i+} + V_{i-})/2$
 - $V_{od} = V_{o+} V_{o-}$ $V_{oc} = (V_{o+} + V_{o-})/2$
- · Still need to be careful with common mode

Fully Differential Amplifier Gains

Input Output



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PSRR, CMRR, ...

$$A_{dm} = \frac{v_{od}}{v_{id}} \to \infty \qquad A_{VDD} = \frac{v_{od}}{v_{DD}} \to 0 \qquad CMRR = \left| \frac{A_{dm}}{A_{cdm}} \right| \to \infty$$

$$A_{cm} = \frac{v_{oc}}{v_{ic}} \to 0 \qquad A_{VSS} = \frac{v_{od}}{v_{SS}} \to 0 \qquad PSRR_{VDD} = \left| \frac{A_{dm}}{A_{VDD}} \right| \to \infty$$

$$A_{cdm} = \frac{v_{od}}{v_{ic}} \to 0 \qquad PSRR_{VSS} = \left| \frac{A_{dm}}{A_{VSS}} \right| \to \infty$$

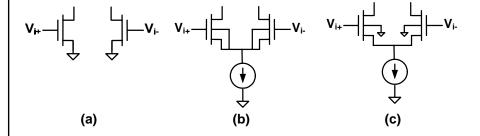
- · All "terminals" are inputs
 - May not be a node in the circuit could be e.g. temperature
- Typical metrics: CMRR, PSRR
 - · Careful with how you use these

CMRR Example

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Differential Input Stage Options



PSRR Example EECS240 Lecture 10 13

