DRC Violation that can be Waived

Date: 01/05/2010 1. Background:

There is DRC violation about the RPO (silicide block) size in this cell.

2. DRC Violation:

2.1 Rule: RPO.A.1

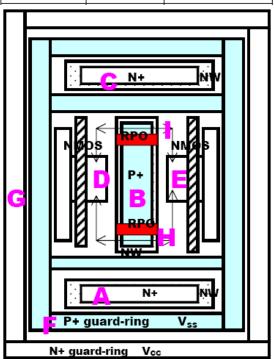
Description: Minimum area of RPO $\geq 2 \text{ um}^2$

Root Cause: This small RPO is used for creating small resistors to limit the drain

passing current.

anona, Waive Reason: There is silicon data on hand to prove the cell's performance.

Input Pad	Vss	Vcc
A, B, C	F	G



3. Action:

Please waive this DRC violation in the LCESD cell.

4. Question:

Please contact

jctsengc@tsmc.com Jen-Chou Tseng 03-5636688 ext.703-8650 ESD/EOS Technology Program **Design Technology Division TSMC**

thchangf@tsmc.com Tzu-Heng Chang ext. 703-8233