FABLESS SEMICONDUCTOR ASSOCIATION

RF PDK Checklist

Foundry - TSMC
Process – 0.18um RF
PDK Revision – Version 1.0a 01/07/2010

PDK Support Contact

E-mail pdk@tsmc.com

Foundry Process Documents

Design Manual (Devices)	T-018-LO-DR-001		2.8	07/16/09
Electrical Parameters				
Design Layout Rules	T-018-LO-DR-001		2.8	07/16/09
Spice Model	T-018-CM-SP-018		1.0	09/11/09
RF Parameters/Modeling	T-018-CM-SP-018		1.0	09/11/09
Noise Model	T-018-CM-SP-018		1.0	09/11/09
Matching Models	T-018-CM-SP-018		1.0	09/11/09
ESD Guidelines				
DRC	T-018-LO-DR-001-C1 T-018-LO-DR-001-U1		2.8a 2.8a	06/25/09 09/09/09
LVS	T-018-CM-SP-018-C1 T-018-CM-SP-018-U1		1.0c 1.0b	12/02/09 12/16/09
Parasitic Extraction	T-018-MM-SP-001-X1 T-018-MM-SP-001-V1		1.5c 1.5a	12/05/08 08/19/08
Layer Map	T-018-LO-LE-004		2.8b_pre1 10309	11/03/09

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EDA Tools Supported and Verified for Use with this PDK

Type	Vendor and Tool	Version	Version Date
Schematic	Cadence Design Systems, Inc / Composer	6.1.4.500.2	
Simulation Control	Cadence Design Systems, Inc / Analog Design Environment	6.1.4.500.2	
Layout Editor	Cadence Design Systems, Inc / Virtuoso VirtuosoXL	6.1.4.500.2	
Circuit Simulator (A)	Cadence Design Systems, Inc / Spectre	7.0.1.146	
Circuit Simulator (B)	Synopsys / Hspice – HspiceD	2009.09	
Circuit Simulator (C)	Cadence Design Systems, Inc / Verilog	08.20.004	
Circuit Simulator (D)	Mentor Graphics Corporation, Inc / Eldo	2009.2	
DRC Checker	Cadence Design Systems, Inc / Assura Mentor Graphics Corporation, Inc / Calibre	41 2009.2_18.12	
LVS Checker	Cadence Design Systems, Inc / Assura Mentor Graphics Corporation, Inc / Calibre	41 2009.2_18.12	
Parasitic Extractor	Cadence Design Systems, Inc / Assura Mentor Graphics Corporation, Inc / Calibre	41 2009.2_18.12	

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Device Type	Device Name	Comment	Terminals	Symbol	Spice-Mod	1/f Noise	HF Noise	Stat Mod	Sim-Net-A	Sim-Net-B	Sim-Net-C	Sim-Net-D	LVS Net	SDL Net	GDS	P-Params	Sim-Test-A	Sim-Test-B	Sim-Test-C	Sim-Test-D	DRC Test	LVS Test	Pcell Test
MOS	nmos2vx		3	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmos2v_macx		3	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmos2vdnwx		3	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmos3vx		3	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmos3v_macx		3	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmos3vdnwx		3	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmosmvt2vx		3	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmosmvt2v_macx		3	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmosmvt3vx		3	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmosmvt3v_macx		3	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmosnvt2vx		3	X	X				X	X	X	X	X	X	X	42	X	X	X	X	X	X	X
	nmosnvt2v_macx		3	X	X			X	X	X	X	X	X	X	X	42	X	X	X	X	X	X	X
	nmosnvt3vx		3	X	X				X	X	X	X	X	X	X	42	X	X	X	X	X	X	X
	nmosnvt3v_macx		3	X	X			X	X	X	X	X	X	X	X	42	X	X	X	X	X	X	X
	pmos2vx		3	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	pmos2v_macx		3	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	pmos3vx		3	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	pmos3v_macx		3	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	pmosmvt2vx		3	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	pmosmvt2v_macx		3	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	rfnmos2v		4	X	X				X	X	X	X	X	X	X	12	X	X	X	X	X	X	X
	rfpmos2v		4	X	X				X	X	X	X	X	X	X	11	X	X	X	X	X	X	X
	rfnmos3v		4	X	X				X	X	X	X	X	X	X	12	X	X	X	X	X	X	X
	rfpmos3v		4	X	X				X	X	X	X	X	X	X	11	X	X	X	X	X	X	X
	rfnmos2v_6t		6	X	X				X	X	X	X	X	X	X	14	X	X	X	X	X	X	X
	rfnmos3v_6t		6	X	X				X	X	X	X	X	X	X	14	X	X	X	X	X	X	X
	rfpmos2v_5t		5	X	X				X	X	X	X	X	X	X	12	X	X	X	X	X	X	X
	rfpmos2v_nw		4	X	X				X	X	X	X	X	X	X	11	X	X	X	X	X	X	X
	rfpmos2v_nw_5t		5	X	X			X	X	X	X	X	X	X	X	12	X	X	X	X	X	X	X
	rfpmos3v_5t		5	X	X				X	X	X	X	X	X	X	12	X	X	X	X	X	X	X
	rfpmos3v_nw		4	X	X				X	X	X	X	X	X	X	11	X	X	X	X	X	X	X
	rfpmos3v_nw_5t		5	X	X			X	X	X	X	X	X	X	X	12	X	X	X	X	X	X	X
	nmos2v		4	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmos2v_mac		4	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmos2vdnw		4	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmos3v		4	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmos3v_mac		4	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmos3vdnw		4	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X

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	nmosmvt2v		4	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmosmvt2v_mac		4	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmosnvt2v		4	X	X				X	X	X	X	X	X	X	42	X	X	X	X	X	X	X
	nmosnvt2v_mac		4	X	X			X	X	X	X	X	X	X	X	42	X	X	X	X	X	X	X
	nmosnvt3v		4	X	X				X	X	X	X	X	X	X	42	X	X	X	X	X	X	X
	nmosnvt3v_mac		4	X	X			X	X	X	X	X	X	X	X	42	X	X	X	X	X	X	X
	nmosmvt3v		4	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	nmosmvt3v_mac		4	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	pmos2v		4	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	pmos2v_mac		4	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	pmos3v		4	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	pmos3v_mac		4	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	pmosmvt2v		4	X	X				X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
	pmosmvt2v_mac		4	X	X			X	X	X	X	X	X	X	X	51	X	X	X	X	X	X	X
PAD	lcesd1_rf		2	X	X				X	X	X	X	X	X	X	1	X	X	X	X	X	X	X
	lcesd2_rf		2	X	X				X	X	X	X	X	X	X	1	X	X	X	X	X	X	X
VAR	jvar		3	X	X				X	X	X	X	X	X	X	5	X	X	X	X	X	X	X
	moscap_rf		3	X	X				X	X	X	X	X	X	X	6	X	X	X	X	X	X	X
	moscap_rf33		3	X	X				X	X	X	X	X	X	X	6	X	X	X	X	X	X	X
	moscap_rf33_nw		3	X	X				X	X	X	X	X	X	X	6	X	X	X	X	X	X	X
	moscap_rf_nw		3	X	X				X	X	X	X	X	X	X	6	X	X	X	X	X	X	X
	mos_var_b		2	X	X				X	X	X	X	X	X	X	4	X	X	X	X	X	X	X
	mos_var_b3		2	X	X				X	X	X	X	X	X	X	4	X	X	X	X	X	X	X
DIO	dioden		2	X	X				X	X	X	X	X	X	X	3	X	X	X	X	X	X	X
	dioden3v		2	X	X				X	X	X	X	X	X	X	2	X	X	X	X	X	X	X
	diodenw		2	X	X				X	X	X	X	X	X	X	3	X	X	X	X	X	X	X
	diodenw3v		2	X	X				X	X	X	X	X	X	X	3	X	X	X	X	X	X	X
	diodep		2	X	X				X	X	X	X	X	X	X	3	X	X	X	X	X	X	X
	diodep3v		2	X	X				X	X	X	X	X	X	X	2	X	X	X	X	X	X	X
	ndio_3m		2	X	X				X	X	X	X	X	X	X	3	X	X	X	X	X	X	X
	ndio_m		2	X	X				X	X	X	X	X	X	X	3	X	X	X	X	X	X	X
	pdio_m		2	X	X				X	X	X	X	X	X	X	3	X	X	X	X	X	X	X
	sbd_rf		3	X	X				X	X	X	X	X	X	X	4	X	X	X	X	X	X	X
	sbd_rf_nw		3	X	X				X	X	X	X	X	X	X	4	X	X	X	X	X	X	X
CAP	crtmom		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	cfmom		3	X	X			X	X	X	X	X	X	X	X	8	X	X	X	X	X	X	X
	cfmom_rf		3	X	X			X	X	X	X	X	X	X	X	13	X	X	X	X	X	X	X
	cfmom_mx		5	X	X			X	X	X	X	X	X	X	X	8	X	X	X	X	X	X	X
	mimcap_1p0_sin		2	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	mimcap_1p0_sin_3t		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	mimcap_2p0_sin		2	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	mimcap_2p0_sin_3t		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	mimcap_rf_40k_2p0		3	X	X			X	X	X	X	X	X	X	X	8	X	X	X	X	X	X	X
	mimcap_rf_2p0		3	X	X			X	X	X	X	X	X	X	X	8	X	X	X	X	X	X	X
BJT	npn	1	3	X	X				X	X	X	X	X	X	X	2	X	X	X	X	X	X	X
	npn_mis	1	3	X	X			X	X	X	X	X	X	X	X	2	X	X	X	X	X	X	X
	vpnp	1	3	X	X				X	X	X	X	X	X	X	2	X	X	X	X	X	X	X
	vpnp3	1	3	X	X				X	X	X	X	X	X	X	2	X	X	X	X	X	X	X
	vpnp_mis	1	3	X	X			X	X	X	X	X	X	X	X	2	X	X	X	X	X	X	X

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RES	rm1		2	X	X				X	X	X	X	X	X	X	5	X	X	X	X	X	X	X
	rm2		2	X	X				X	X	X	X	X	X	X	5	X	X	X	X	X	X	X
	rm3		2	X	X				X	X	X	X	X	X	X	5	X	X	X	X	X	X	X
	rm4		2	X	X				X	X	X	X	X	X	X	5	X	X	X	X	X	X	X
	rm5		2	X	X				X	X	X	X	X	X	X	5	X	X	X	X	X	X	X
	rmt		2	X	X				X	X	X	X	X	X	X	5	X	X	X	X	X	X	X
	rmu_40k		2	X	X				X	X	X	X	X	X	X	5	X	X	X	X	X	X	X
	rnhpoly		2	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rnhpoly_dis		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rnlplus		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rnlplus_2t		2	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rnlpoly		2	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rnlpoly_dis		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rnplus		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rnplus_2t		2	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rnwell		2	X	X				X	X	X	X	X	X	X	6	X	X	X	X	X	X	X
	rnwod		3	X	X				X	X	X	X	X	X	X	6	X	X	X	X	X	X	X
	rnwod_2t		2	X	X				X	X	X	X	X	X	X	6	X	X	X	X	X	X	X
	rnwsti_m		3	X	X				X	X	X	X	X	X	X	6	X	X	X	X	X	X	X
	rphpoly		2	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rphpoly_dis		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rphripoly		2	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rphripoly_dis		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rplplus		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rplplus_2t		2	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rplpoly_dis		2	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rplpoly_dis		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rpplus		3	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rpplus_2t		2	X	X			X	X	X	X	X	X	X	X	9	X	X	X	X	X	X	X
	rphpoly_rf		3	X	X			X	X	X	X	X	X	X	X	6	X	X	X	X	X	X	X
	rphripoly_rf		3	X	X			X	X	X	X	X	X	X	X	6	X	X	X	X	X	X	X
	rplpoly_rf		3	X	X			X	X	X	X	X	X	X	X	6	X	X	X	X	X	X	X
IND	spiral_std_mu_x_20k		3	X	X				X	X	X	X	X	X	X	10	X	X	X	X	X	X	X
	spiral_sym_ct_mu_x_20k		3	X	X				X	X	X	X	X	X	X	10	X	X	X	X	X	X	X
	spiral_std_mu_x_20k		3	X	X				X	X	X	X	X	X	X	10	X	X	X	X	X	X	X
	spiral_std_mu_x_40k		3	X	X				X	X	X	X	X	X	X	10	X	X	X	X	X	X	X
	spiral_sym_ct_mu_x_40k		3	X	X				X	X	X	X	X	X	X	10	X	X	X	X	X	X	X
	spiral_std_mu_x_40k		3	X	X				X	X	X	X	X	X	X	10	X	X	X	X	X	X	X
SPE	dio_dnwpsub	2	2	X	X				X	X	X	X	X			0	X	X	X	X			
	dio_pwdnw	2	2	X	X				X	X	X	X	X			0	X	X	X	X			
	diodesd3v	2	2	X	X				X	X	X	X	X			0	X	X	X	X			

Comments

1. The npn/vpnp/vpnp3 cells don't have the layout view. It will be automatically generated during the schematic driven layout procedures.
2. This PDK only provides front-end information for these devices. Users have to provide the layouts and set those parameters manually depending on the layouts wanted.
3. This PDK only provide front-end information for these devices. These devices are designed for designers to take the RC substrate network effect into consideration during the design phase. Users have to pre prepare the corresponding models for those devices and incorporate them into TSMC's spice model before running the simulation.

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