EE 214 Project Report Fall 2007

A 3V Gain-Boosted Fast Settling 4.95 mW 90 dB Dynamic Range CMOS OTA design

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Outline:

1, Design Approach and Decisions

2, OTA Schematics

3, Design process and Equations

4, Simulation Plots

* Modified from Saihua Lin, Hai Wei, "A 3V Gain-Boosted Fast Settling 5.52 mW 91.09 dB Dynamic Range CMOS OTA design", EE214 project report, fall 2007

1, Design Approach and Decisions

The static error of 0.025% requires the open loop gain to be larger than about 16000. To satisfy this requirement, we need to build an amplifier with at least 3 transistor stages in its signal path or by using gain-boosting techniques. For those with only 2 transistor stages in path, it is hard to meet the specs. For example, we have tried to modify the project example to meet the spec by using L = 1.1 μm for PMOS transistors and L = 0.65 μm for NMOS transistors. However, the static error is still 0.05% with power 27.56 mW and settling time 39.5 ns.

There are mainly two options to implement the desired OTA in order to meet the specs. One is the two-stage circuit with the first stage telescopic to provide high gain and the second stage common source to provide high swing. The other one is the gain boosted OTA. The other topologies such as folded cascode OTA can also be considered. However, generally it is worse than the two-stage OTA in terms of output swing. It is still worse than the gain boosted OTA in terms of power.

Table 1, Amplifier comparison between two-stage circuit and gain boosted circuit

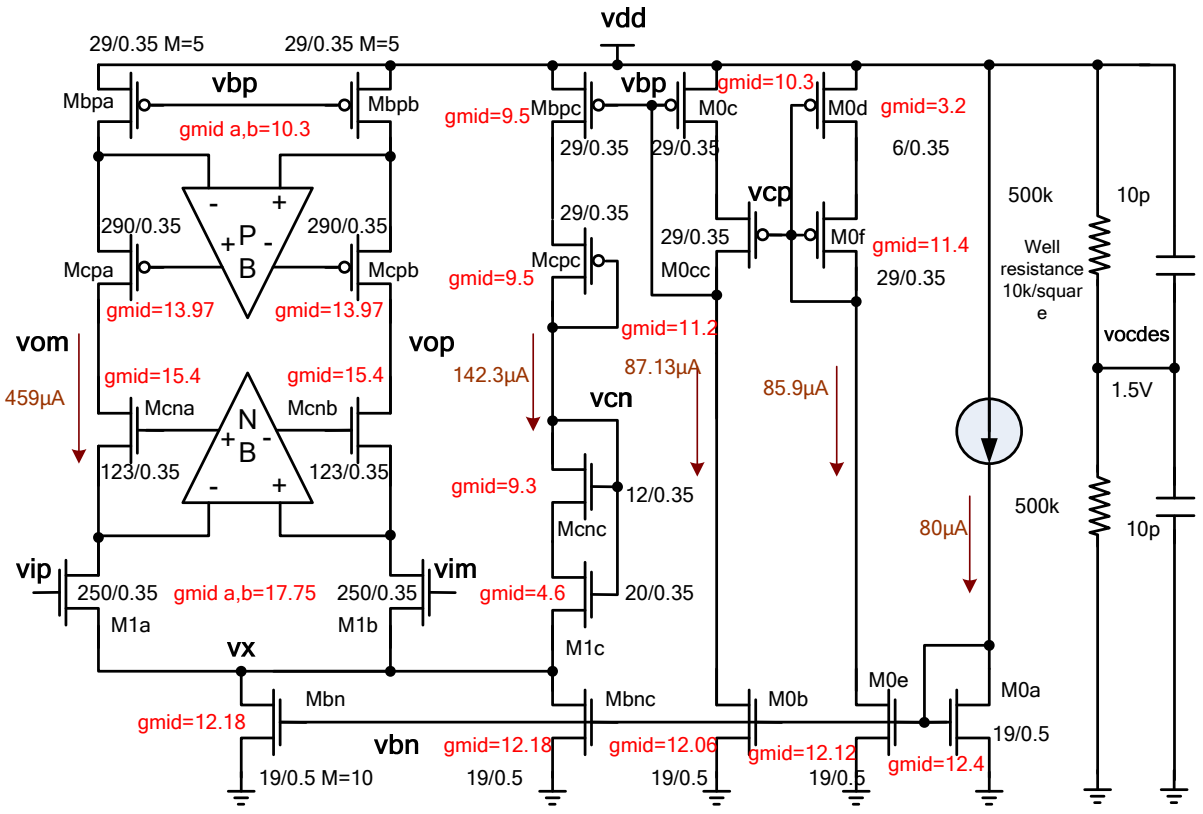
Amplifier Topology Comparison							
Topology	Gain	Output Swing	NF	DR	Procedure	Power	Linear Settling
two-stage	gmro^3	VDD-2Vdsat	>1.3	Large	Easy	Large	Fast
gain boost	gmro^3-4	VDD-5Vdsat	~1.3	Small	Complex	Small	Slow

Table 1 summarizes our observations of these two topologies. Two-stage amplifier design is easy especially we can use MATHCAD, MATLAB, and HSPICE extensively to find the minimum power consumption point without much “SPICE Monkeying”. If offers a large output swing and thus the dynamic range can be made quite high. In addition, the linear settling speed is generally faster than the gain boosted OTA. This is an important consideration though many designers may ignore [1]. For 0.025% dynamic settling error, the linear settling time of the two-stage amplifier with 75 degree phase margin is 41% smaller than that of the gain boosted amplifier whose phase margin is typically around 90 degree [2]. If slew is not considered, this means the current of the main amplifier of the gain boosted circuit has to be increased by 2.78X. From this standpoint, the two-stage amplifier is still comparable to or even better than the gain boosted amplifier in terms of power consumption.

However, in reality slew does happen and even plays a very important role for power reduction. We can find that with more slew, the total power can be reduced more, thereby making the faster linear settling speed effect of the two-stage OTA negligible. As a result, the drawback of two-stage amplifier is still the large power consumption problem. Compared to the gain boosted telescopic amplifier, it has 4 current legs while the gain boosted telescopic amplifier has only 2 current legs. As a result, the power of two-stage amplifier is often larger than the gain boosted amplifier. Actually we have designed a two-stage OTA that meets all the specifications (DR = 90.08 dB, settling time = 39.94 ns, settling accuracy < 0.01%). The power consumption is as large as 12.17 mW. We can further show that the minimum power consumption of two-stage OTA is around 12 mW qualitatively.

Yet gain boosted amplifier design is complex. We have to manage the inherent doublet [3][4] and the optimization procedure is not quite clear. As a result, we may end up with lots of manual circuit tweaking. In this project, however, we still chose to design a gain boosted OTA because of low power consideration. Since the gain-boosting techniques decouples the DC gain and frequency response of the amplifier. It allows us to attain very high gain while maintaining the bandwidth, which is crucial to the small settling time. Finally, by combining MATHCAD optimization and circuit tweaking, we achieved a 5.52 mW gain boosted OTA in nominal corner. We can further show qualitatively that the minimum power consumption is around 6 mW under single pole approximation.

2, OTA Schematics



- CMFB circuits are not shown. For the main amplifier, g is 35 mS ; for the booster amplifiers, g is 1.06 mS. They are designed not to pull any current from the ground.
- The maximum current mirror ratio is 17
- The maximum gm/id is 18.8, occurring in P-Booster differential pair
- Use only NMOS, PMOS, ideal capacitors, ideal resistors, single current source, and controlled sources in CMFB circuit. Vocdes is generated by resistor divider like in Flash ADC way.

3, Design process and Equations

3.1 Specification and Considerations

In this section, we give out the project specification and our design considerations on the OTA design.

- Prepare .bat or script files that are used for HSPICE files and MATLAB files respectively. This would help accelerate the simulation procedure.
- Prepare MATHCAD tables and all kinds of technology related functions.
- gm/ID > 20 is assumed to be impractical throughout the design because then the circuit would be too sensitive to process variations.

Reference:N:\mos\tables.xmcd

Dynamic Range	$DRdB := 90$	Static Settling Error	$\varepsilon_s := 0.025\%$
Supply voltage	$V_{DD} := 3V$	Dynamic Settling Error	$\varepsilon_d := 0.025\%$
Close Loop Gain	$A_{cl} := 1$	Settling Time	$t_s := 40 \cdot 10^{-9} s$
Temperature	$T_r := 300K$	Total Settling Error	$\varepsilon_{tot} := \varepsilon_s + \varepsilon_d$
Boltzman Constant	$k_B := 1.38 \cdot 10^{-23} \frac{J}{K}$	Noise factor	$\gamma := \frac{2}{3}$

3.2 Dynamic Range Consideration

Here, we choose the maximum output swing is 2.0 V. It's reasonable for a telescopic gain-boosted circuit since there are 5 transistors stacking on one vdd to ground path.

Dynamic Range	$DR := 10^{\frac{DRdB}{10}}$	$DR = 1 \times 10^{9}$	
Output swing	$V_{omax} := 2V$	Signal Power	$P_s := 0.5 \cdot V_{omax}^{2}$
Noise Power	$P_n := \frac{P_s}{DR}$	$\sqrt{P_n} = 4.472 \times 10^{-5}\ V$	

3.3 Capacitances

In order to minimize noise effect of the active loads, the $V_{dsat,loads}/V_{dsat,in}$ should be maximized. However, this value can not be too large because of output swing limitation. In telescopic gain-boosted circuit, the output swing is very cherishing.

Suppose $V_{dsat1} := 100mV$ $V_{dsat2} := 300mV$ $\beta_{est} = 0.333$

$$N_{tot} := 2 \cdot \left(\frac{V_{dsat1}}{V_{dsat2}} + 1 \right) \cdot \gamma \cdot \frac{1}{\beta_{est}} \cdot \frac{k_B \cdot T_r}{C_L} \qquad C_{Lmin} := \frac{8}{3} \cdot \gamma \cdot \frac{1}{\beta_{est}} \frac{k_B \cdot T_r}{P_n} \qquad C_{Lmin} = 1.104 \times 10^{-11}\ F$$

Considering the noise contribution of boost amplifier and cascode transistor, we set C_L = 12.5 pF to give margin. Then the feedback capacitance is chosen as 5 pF by considering the DR margin and feed forward effect:

$$\frac{V_{odstep}}{V_{idstep}} = \frac{1}{1 + \frac{C_{in}}{C_f} + \frac{C_L / C_f}{1 + C_L / C_f}} \cdot \frac{1}{1 + C_L / C_f} \quad \text{should be small}$$

We can calculate the loop gain is 4000 and the open loop gain is about 16000. This means we need one stage gain about 178 in signal path. Since small length can offer higher speed, therefore in the main amplifier the input differential pair and the cascode transistors are chosen to have the minimum lengths. Although this would reduce

the intrinsic gain, the gain boost amplifier can effectively cope with this not-enough-gain problem (~gmro^4).

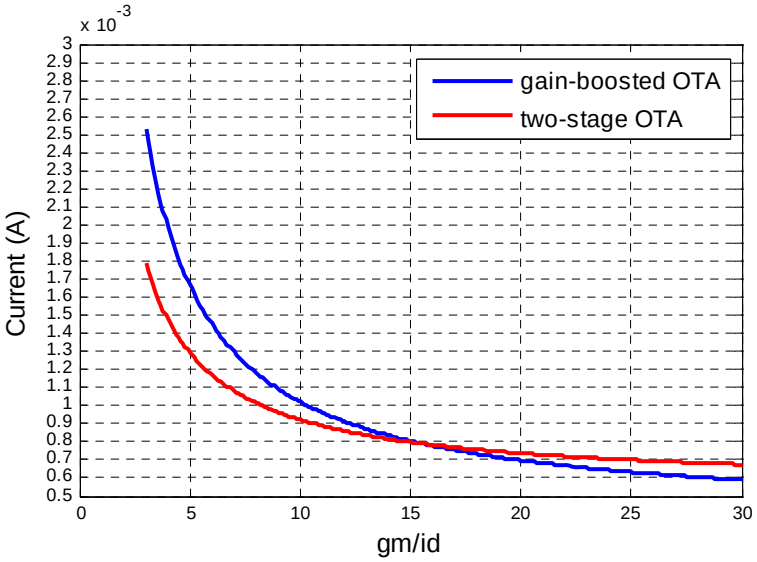
3.4 Main Stage Current Selection

This would be the most important part to design a low power gain boosted OTA. By using the equation $t_s = \frac{|V_{xstep}| - 2.8/(g_m/I_D)}{\beta \cdot SR} - \tau \ln(\varepsilon_d)$ we can derive:

$$I_D = \frac{1}{t_s}\left(\frac{|V_{xstep}| - 2.8/(g_m/I_D)}{2\beta} C_{Leff} - \frac{\ln(\varepsilon_d)}{\beta(g_m/I_D)} C_{Leff}\right)$$ for gain boosted circuit single pole analysis

$$I_D = \frac{1}{t_s}\left(\frac{|V_{xstep}| - 2.8/(g_m/I_D)}{2\beta} C_c - 0.574 \times \frac{\ln(\varepsilon_d)}{\beta(g_m/I_D)} C_c\right)$$ for two-stage circuit (PM = 75 degree)

By choosing gm/ID in the range 15-20, we can find the minimum current required by gain boosted circuit is about 700 µA. For two-stage circuit, the corresponding minimum current is about 780 µA. The second stage current is about 800 µA×(1+C_{Leff}/C_c)=1.13 mA. So the minimum power consumption for two-stage OTA should be about 12 mW. This prediction is very close to our MATHCAD optimization and final implementation of the two-stage amplifier. So we can predict that the minimum power of the gain boosted circuit under single pole analysis is only around 6 mW, half of that of the two-stage circuit.



Suppose ID is 750 µA, and choose the different gm/id or V_{dsat} to satisfy the output swing limitation:

Active Load 210 mV, gmid=9.5 $W_4 := \frac{I_D}{pidwfuc(L_p, gmid4)}$ $W_4 = 1.493 \times 10^{-4}$ m

PMOS cascode 167 mV, gmid=12 $W3 := \frac{I_D}{pidwfuc\left(L_p, \frac{12}{V}\right)}$ $W3 = 2.794 \times 10^{-4}$ m

NMOS cascode 150 mV, gmid=13 $W2 := \frac{I_D}{nidwfuc\left(L_n, \frac{13}{V}\right)}$ $W2 = 1.297 \times 10^{-4}$ m

Input pair 120 mV, gmid=16 $W_1 := \frac{I_D}{nidwfuc(L_n, gmid1)}$ $W_1 = 2.416 \times 10^{-4}$ m

Tail current source 210 mV, gmid=9.5 $W5 := 2 \cdot \frac{I_D}{nidwfuc\left(0.5\mu m, \frac{9.5}{V}\right)}$ $W5 = 1.972 \times 10^{-4}$ m

Similarly we can calculate all the other width and length by using MATHCAD functions and lookup tables.

3.5 Settling Time Consideration and Booster Decision

$V_{istep} := 2V$

$$V_{xstep} := V_{istep} \cdot \frac{C_s}{C_s + C_{gg1} + \frac{C_f C_L}{C_f + C_L}}$$

$$t_{slew} := \frac{V_{xstep} - \frac{2.8}{gmid1}}{\beta \cdot 2 \frac{I_D}{C_{Leff}}}$$

$t_{slew} = 1.954 \times 10^{-8}\ s$ $V_{xstep} = 1.114\,V$

$t_{lin} := 40\,10^{-9}\,s - t_{slew}$ $f_{ca} := \frac{-\ln(\varepsilon_d)}{2\pi t_{lin}}$ $f_c = 6.453 \times 10^7\ \frac{1}{s}$

For booster design, we choose folded cascode differential pair circuit because it can provide large common mode input range. In addition, since the local feedback can introduce doublet effect, the bandwidth of the amplifier should be optimized according to $\beta\omega_{u,main} \le \omega_{booster} \le \omega_{p2,main}$ [3].

3.6 Common Feed Back Consideration

The CMFB unity-gain bandwidth should be *A* times larger than the differential unit gain bandwidth. We can derive: $g_{mcfb} >= A*2*\beta*g_{m1}$, where *A* is a coefficient and is generally larger than 0.5. In the final version, we choose g_{mcfb}=17 mS (corresponding to *A* = 2.4, PM=88) for the main amplifier, g_{mcfb}=0.725 mS for the booster amplifiers. With a large *A*, the common mode output voltage can be settled very fast. However, *A* can not be too large. Otherwise, the phase margin will not be enough, thereby causing ringing effect (equation see corner analysis part).

3.7 Performance Summary

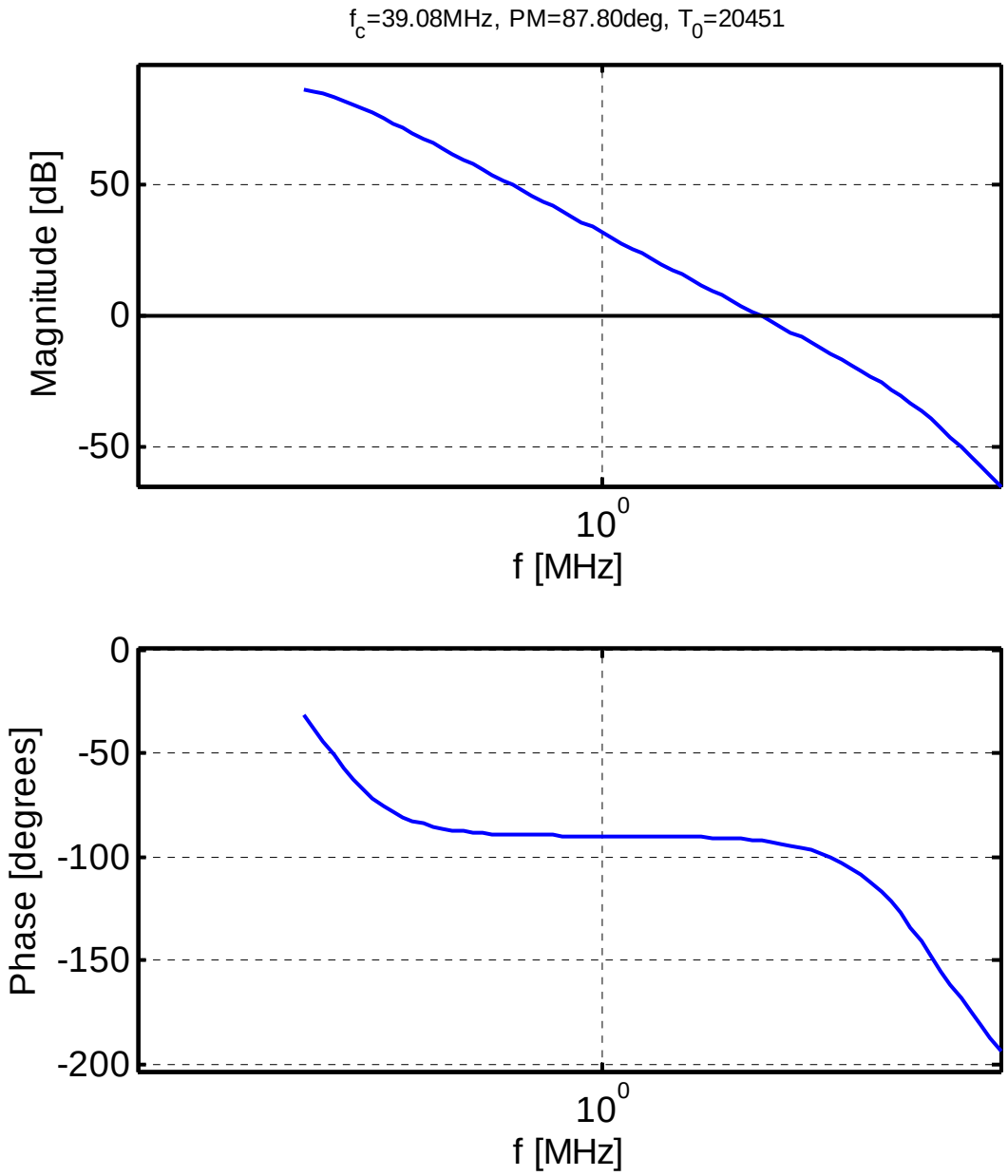
Performance parameter	First Run*	Hand 1st	Error of first run	Final Run**
ID1(μA)	812	750	8.27%	459
DR (dB) at Vomax	92.59	90	2.88%	90.01
PM (degree)	87.96	90	-2.27%	87.8
Loop gain	15217	>4000	-	20451
Unit gain bandwidth f_c(MHz)	68.44	64.5	6.1%	39.08
Total output noise (μV)	34.86	44.7	-22.01%	37.95
Settling time (ns)	37.86	40	-5.35%	38.65
Static Settling accuracy	<0.01%	0.025%	-	<0.01%
Power without bias (mW)	7.12	6.3	13.2%	3.76
Total Power (mW)	8.95	-	-	4.95

** First run means we implement the circuit according to the above W/L and I parameters without any tweaking*

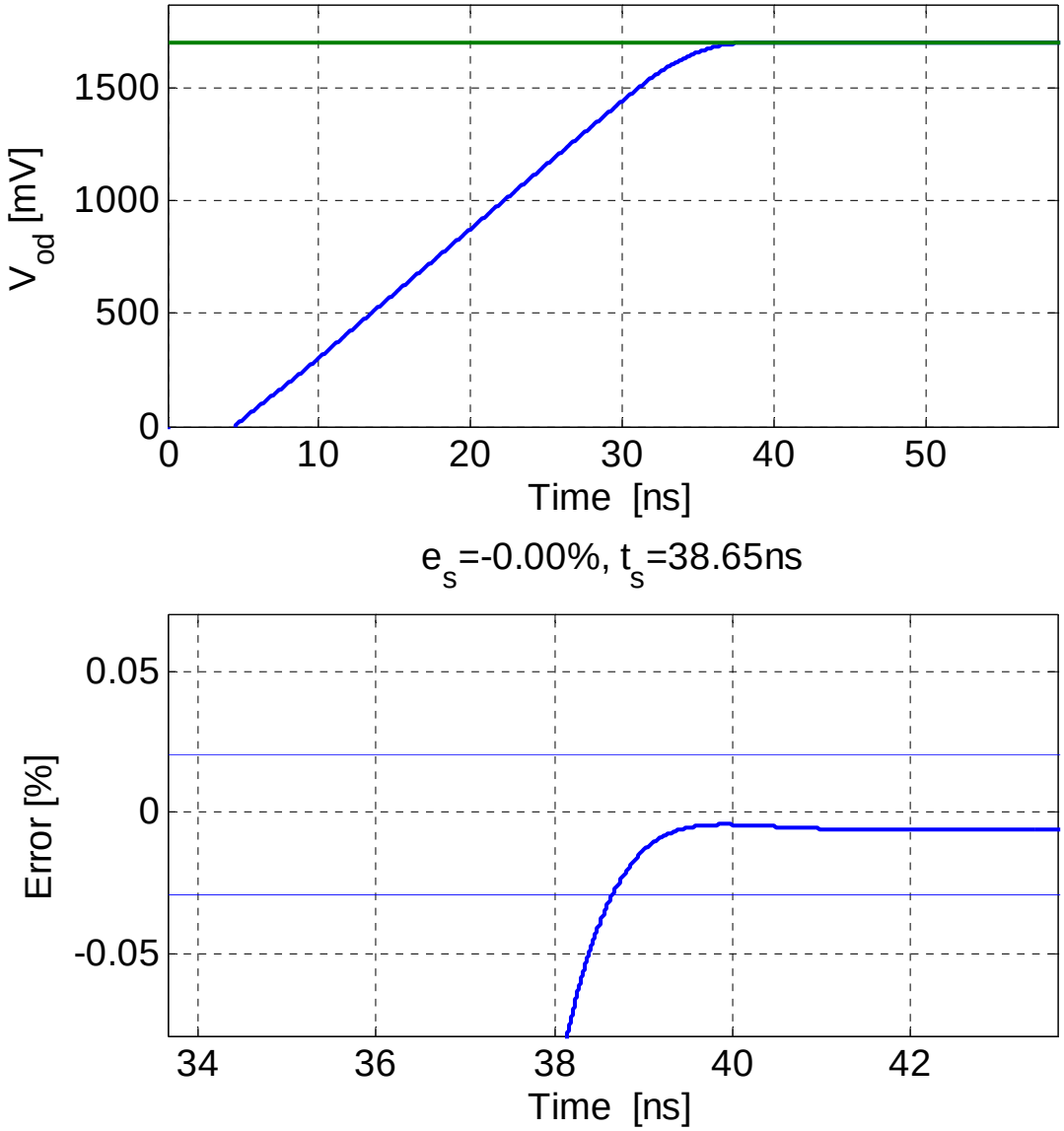
*** Final run means we reduce the bias current to reduce power(this implies gm/id of transistors can be increased)*

The reason why the ID1 and DR are larger in the first run is understandable. This is due to channel length modulation and our over selection of the load capacitance (40% larger than minimum). As a result, the total noise is 34.86 μV, 22% smaller than the initial calculation. This also implies the cascode transistor and the gain boosting amplifiers contribute some noise. From the table we can see f_c is 6.1% larger than the calculation. This is mainly due to the current increase of the differential pair (8.27% increases) and the W/L increase (we choose 250/0.35, 4.2% larger than calculated 241.6/0.35). As a result, the linear settling time is smaller than 40 ns (5.35% reduction). Another reason why the linear settling time is reduced from the calculation is the effect of the non-dominant pole. Since the phase margin is 87.96 degree, the linear settling time speed up is 0.967×. Thus linear settling time can be reduced by 3.3%. Finally, the three methods to obtain an ultra low power OTA used are: 1, use relatively large gm/ID; 2, enhance slew settling time; 3, optimize the common mode loop effect.

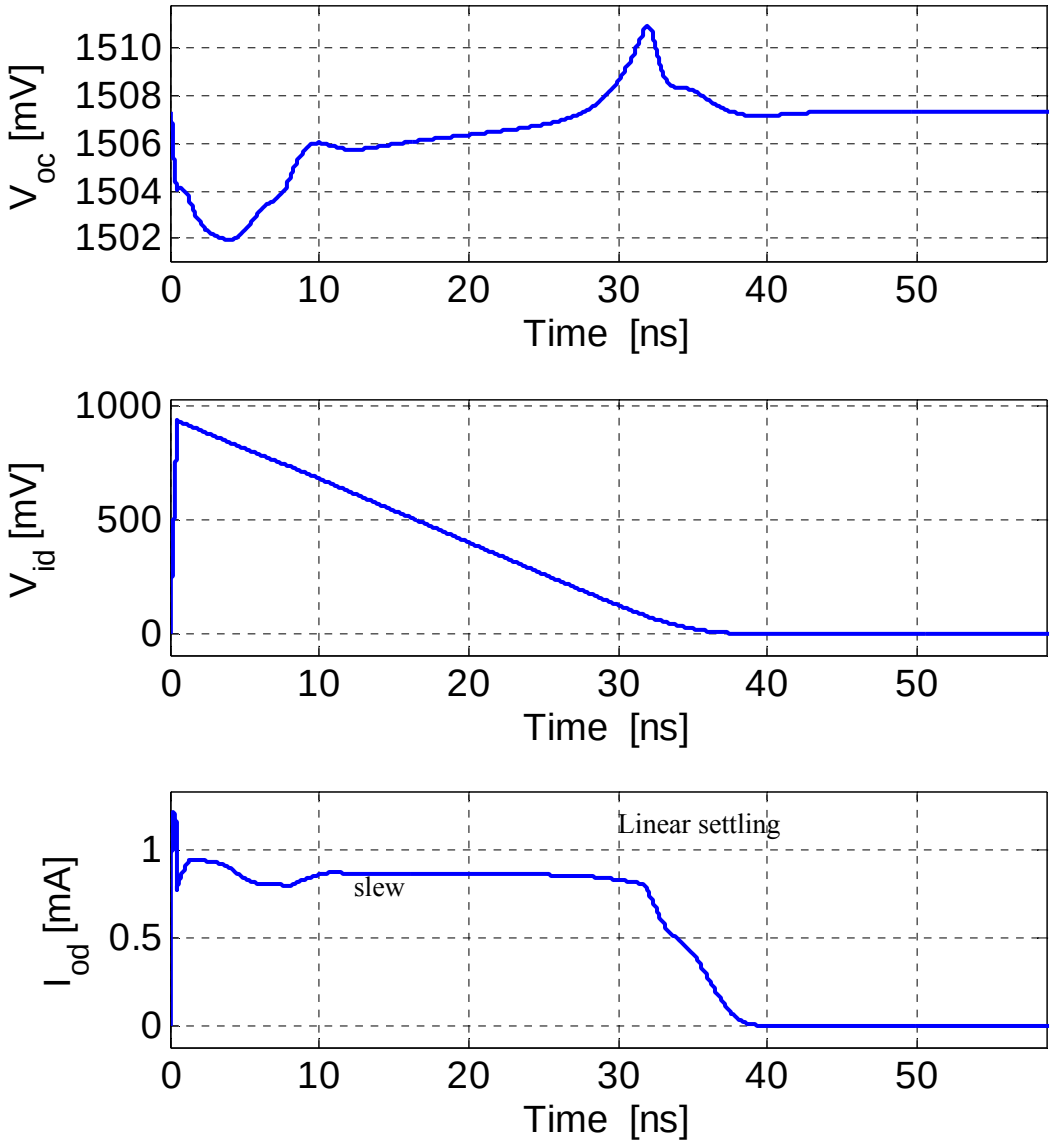
4, Differential AC loop frequency Response



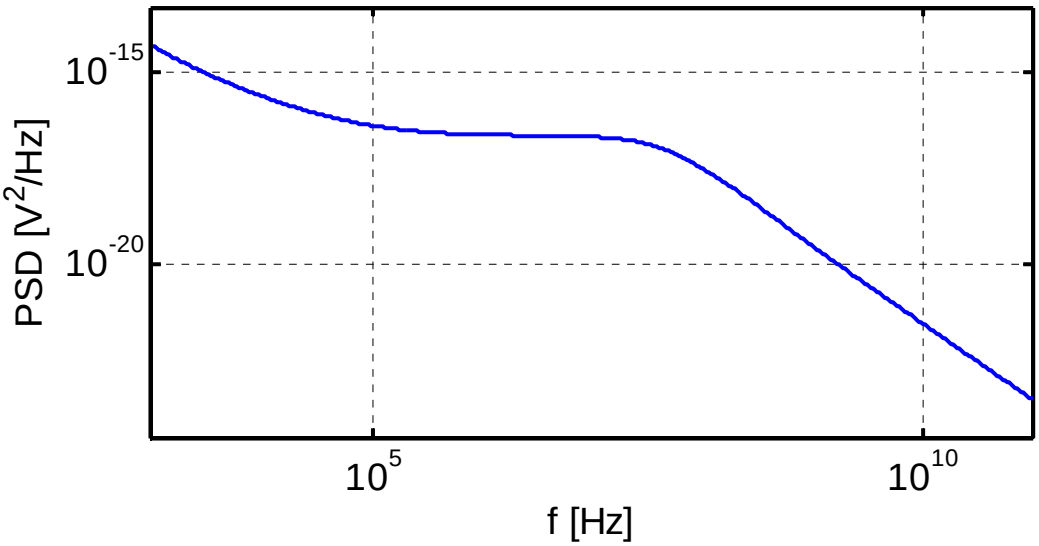
5, Vod Response and Settling Time



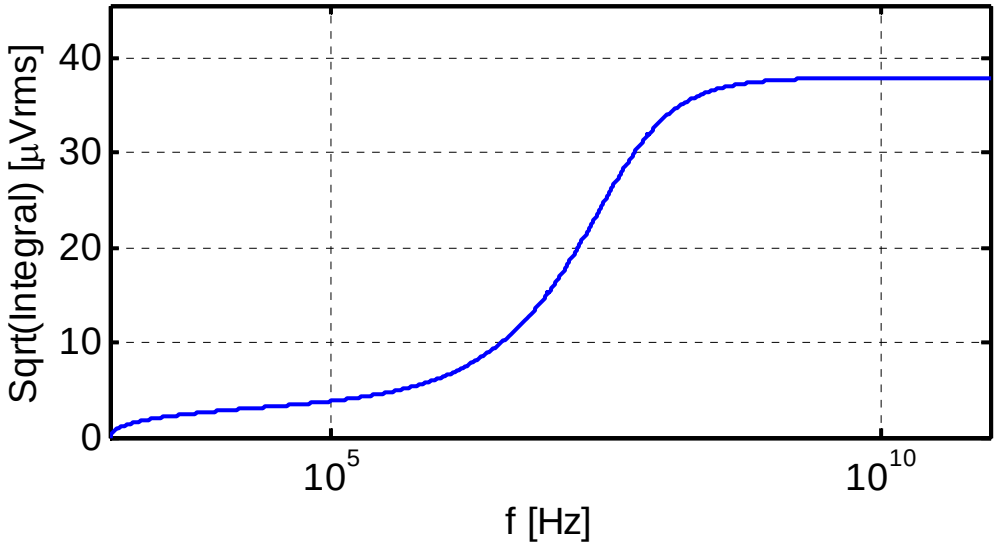
6, Common Mode Output and Differential Voltage and Current



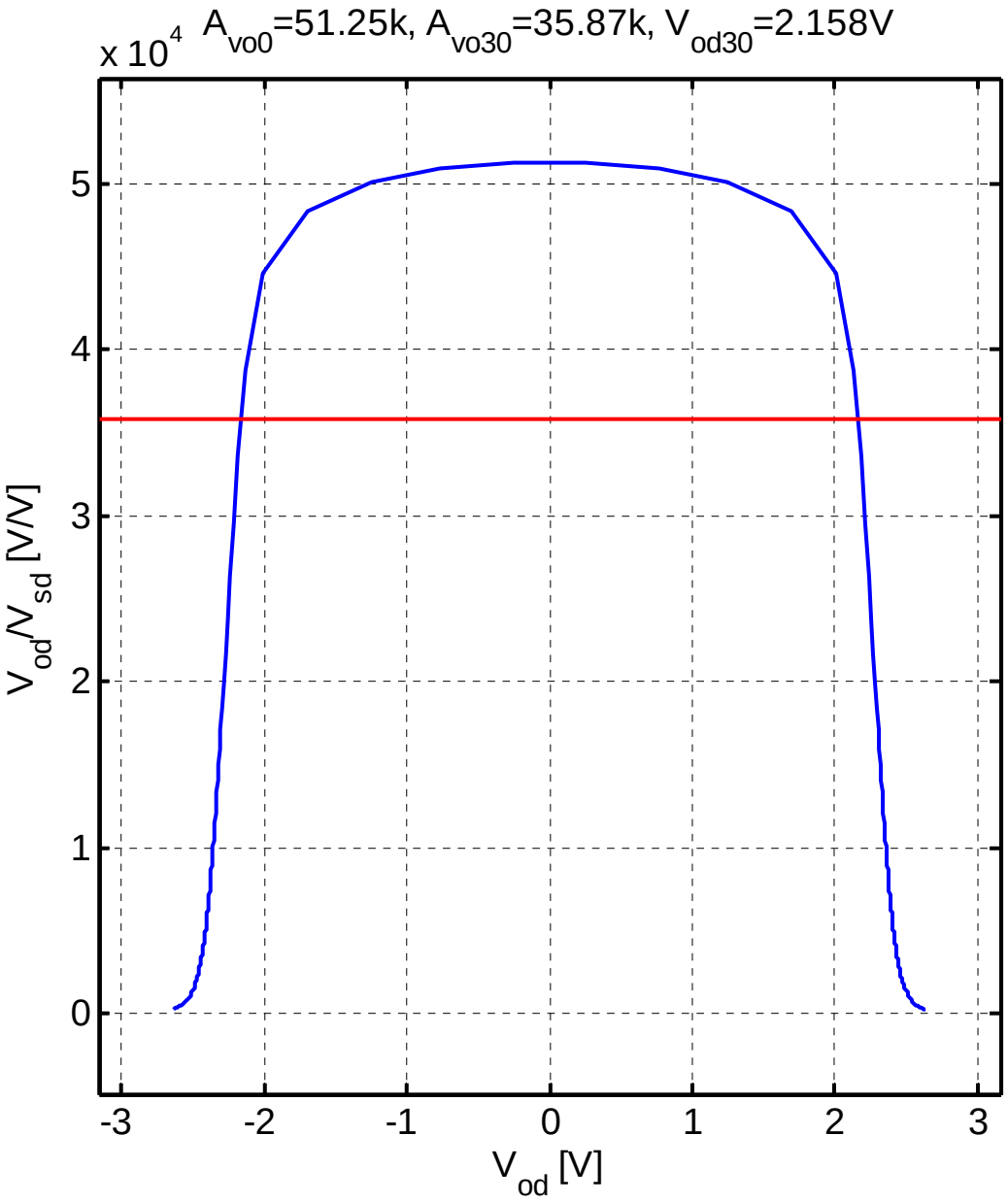
7, Noise Performance



Integral=37.95uVrms, DR=90.01dB (for V_{odmax}=1.70V)



8, Output Range



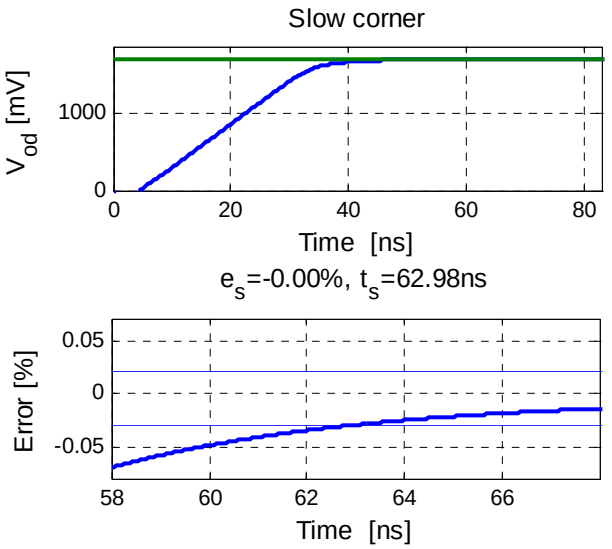
9, Corner Analysis

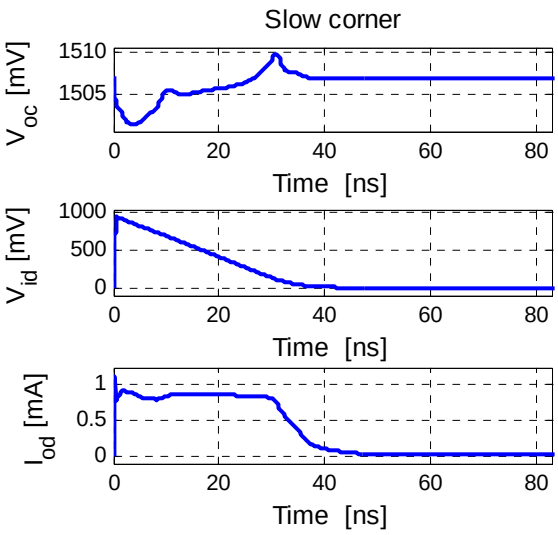
Performance parameter	Nominal	Slow,125℃	Error (%)	Fast, 0℃	Error (%)
ID1(μA)	459	451.4	-1.6558	475	3.4858
DR (dB) at Vomax=1.9	90.01	**88.58**	-1.5887	90.41	0.4444
PM (degree)	87.8	87.95	0.1708	87.7	-0.1139
Loop gain	20451	19532	-4.4937	15038	-26.4681
Open loop gain at Vod=0 ($\times 10^3$)	51.25	54.86	7.0439	34.44	-32.8000
Unit gain bandwidth fc(MHz)	39.08	29.6	-24.2579	45.53	16.5046
Total noise (μV)	37.95	44.75	17.9183	36.26	-4.4532
Settling time (ns)	38.65	**62.98**	**62.9495**	**50.48**	**30.6080**
Static settling accuracy	<0.01%	<0.01%	-	<0.01%	-
Total Power (mW)	4.95	4.84	-2.2222	5.17	4.4444

From above table we can find in fast corner and slow corner, the settling time increased largely from the nominal corner. This may due to 1: corner effect (process variation effect); 2, the doublet effect; 3 the common mode feedback effect. We first investigate the common mode feedback effect. In nominal corner, the g_m of the input differential pair is 8.15 mS and the main stage common mode feedback g is 35 mS, so

$$\frac{g_{mcfb}}{2\beta g_{m1}} \approx 5.36\,, \quad PM = \arctan\left(\frac{4C_L g_{m1}}{2C_{gs1}+C_{db,bn}+C_{gd,bn}} \cdot \frac{1}{g_{mcfb}}\right) = 89°$$

In fast corner, this factor is reduced to 4.6 and in slow corner this factor is increased to 7.2 (89 degree). So we can see clearly that this factor is large enough in slow corner. This implies the common mode feedback circuit should have not much impact on the time response. The figure shown below confirms our guess, i.e. there is no more ringing on Voc. So we have to consider another reason: the corner effect. This means the transistor parameters are different in different corners (process variations), like mobility, threshold voltage etc. By using .OP analysis, we find that the tail current source of the main amplifier is in linear region. In addition, since the unit gain bandwidth is also low compared to the nominal corner, the linear settling time is increased and the slew time is reduced. As a result, the total settling time is increased.

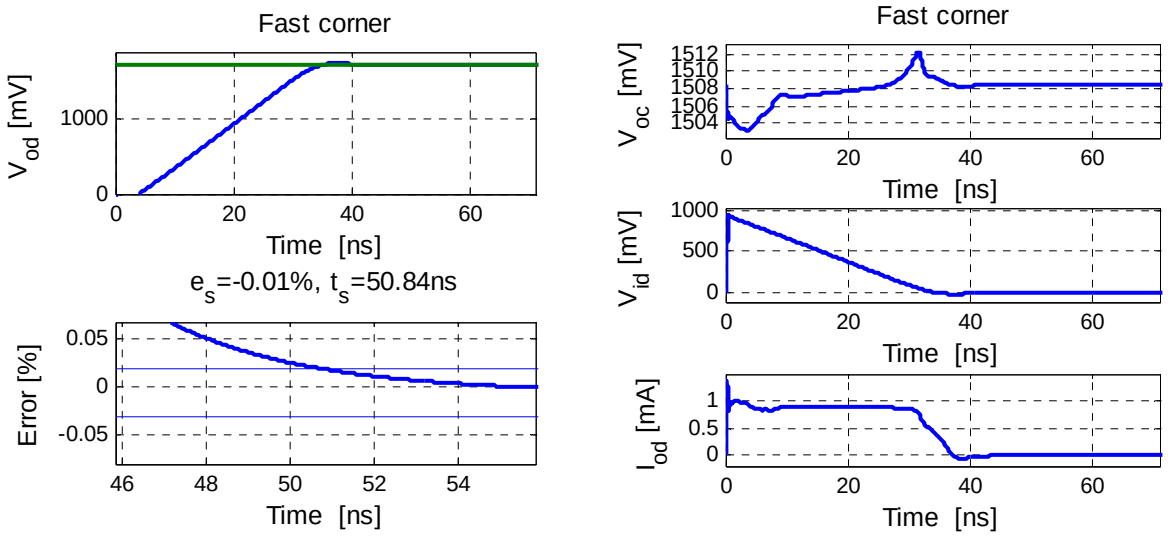




In order to solve/mitigate this problem, it would be better to design a CMOS circuit that provides the input common mode voltage so that the input common mode voltage can change corresponding to different corners. As

a result, the input differential pair and the tail current source transistor can operate in the active region.

When turning to the fast corner analysis, the above analysis is not true since all the transistors operates correctly and the unit gain bandwidth is larger than that in the nominal corner. The common feedback loop bandwidth is also large enough. Since gm input is larger, the phase margin is also larger (about 89 degree). However, from the transient waveform, we can find there is overshoot. This is the reason why the settling time is increased.



The reason can be the pole-zero double effect. As has been analyzed in [2][3], a pole-zero doublet can degrade the settling performance and can also cause overshoot. In order to solve this problem, we can add compensation capacitances to push the doublet frequency beyond the close-loop dominant pole frequency of the amplifier. So $\beta\omega_{u,main} \le \omega_{booster} \le \omega_{p2,main}$. This technique is originally proposed by K. Bult and G. Geelen [4].

From the above table, we can also find that the dynamic range does not satisfy the spec in slow corner situation where the noise is increased by 17.9%. Given the expression:

$$N_{tot} := 2\cdot\left(\frac{V_{dsat1}}{V_{dsat2}} + 1\right)\cdot\gamma\cdot\frac{1}{\beta_{est}}\cdot\frac{k_B\cdot T_r}{C_L}$$

We can see that noise is related to temperature. So we can calculate that the temperature contribution of the noise voltage is about 5.8%. The other 12.1% noise is mainly attenuated by the 40% over designed load capacitance. In order to solve this problem, we can increase the input step voltage in nominal corner under the situation that the settling time is still met.

10, Comments and Conclusion

In this project, we have tried three structures and implemented a gain-boosted OTA which satisfies all the specs in 0.35 μm CMOS technology with 3 V supply for project conclusion. The power is only 4.95 mW in nominal corner by HSPICE simulation, with the core amplifier power 3.76 mW and bias power 1.18 mW respectively. The settling time is 38.65 ns and the dynamic range is 90.01 dB with an input equals to 1.7V. Although there is still room to reduce power, we try to over design a bit to sustain performance in other corners. The three methods to obtain an ultra low power OTA used in this project are: 1, use relatively large gm/ID; 2, enhance slew settling time; 3, optimize the common mode loop effect.

There are several issues which should be addressed in real design. The first thing is that the design should meet all the specs in all the fast/slow/nominal cases. In this project, we don't need to meet these specifications. The second thing is that the bandwidth of the common mode loop is larger than the differential signal path in this project to improve the settling time. In [2], it is said that the bandwidth of the common mode loop is about 30% of the differential bandwidth, so *A* should be 0.3. However, we think this is not a concrete rule that every design has to follow. By using our analysis and the PM equation, it is quite safe if *A* is chosen large because we have a relatively large C_L here. The parasitic capacitance is just in the range of hundreds of fF. So we don't have to worry much about that. In fact, we have designed several versions of circuit with different *A*:

Circuit parameter	*A*	Settling time (ns)	DR (dB)	Power (mW)
1	2.4	39.51	91.09	5.52
2	1.58	37.96	91.61	6.06
3	0.56	39.74	92.26	6.29

The third thing is that PSRR, CMRR are not calculated in this project. However, in real design these specifications are also very important. PMOS input pair helps to improve CMRR but in this design, due to speed and power efficiency considerations, we use NMOS input pair in our first stage. We also use high swing bias circuit in this amplifier design by using "Magic Battery". This would help improve PSRR. Again, since PSRR is not considered, we just design a resistive divider voltage reference for Vocdes. It is sensitive to VDD variation.

Another thing to note is that throughout the design, we have submitted lots of times because we initially found the results given by the server are sometimes different from ours. After many times of try, we find the reason is that we used HSPICE200609 on PC and the server is using HSPICE200102. When doing transient simulation, **HSPICE200102 in server gives more data points than HSPICE200609 and as a result the transient simulation results are different**.

11, References:

1, Jason S. and Anshi L., "A low power two-stage telescopic amplifer with 90 dB dynamic range and 200 ns settling time," UC Berkeley EE240 Project Report, 2004

2, Boris Murmann, EE214 Lecture Notes, Stanford University

3, Yun Chiu, Ken Wojciechowski, "A gain-boosted 90-dB dynamic range fast settling OTA with 7.8 mW power consumption," UC Berkeley EE240 Final Project Report, 2000

4, K. Bult and G. Geelen, "The CMOS gain-boosting technique," Analog Integrated Circuits and Signal Processing, vol. 1, no. 2, Oct. 1991, pp. 119-135.