UNIVERSITY OF CALIFORNIA
College of Engineering
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E. Alon **Homework #2** **EECS 240**
Due Tuesday, February 23, 2010

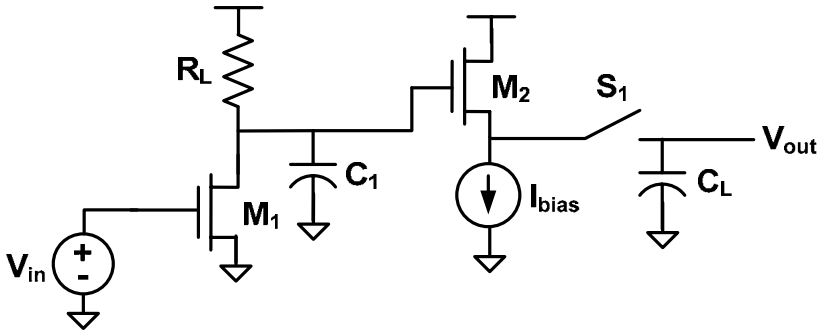
Use the EECS240 90nm CMOS process in all homeworks and projects unless noted otherwise. In this homework you may use just the typical (tt) device parameters.

1. Design a PMOS common-source stage driving a 2pF load with 1GHz unity-gain bandwidth. Choose a sufficiently long L to achieve an open-loop gain of at least 25 for output voltages between 0.35V and 1V and minimize the power dissipation of the circuit. Determine the device width and bias current, and verify the gain and bandwidth with SPICE. Also, plot the small-signal gain $a_{v0}=dV_o/dV_i$ as a function of the output DC level.

2. Integrate the input referred flicker noise of a 10/0.09 NMOS transistor in a common-source configuration from 1Hz to 2GHz. Specify the result in Volts rms. Use V*=200mV and your results from homework #1 to calculate g_m, C_{ox} = 17fF/μm^2, and the K_f parameters from the lecture notes. How does the result change if you reduce the lower limit of integration to 1 week^{-1}? Find the factor M by which W and I_D must be increased (keeping g_m/I_D constant) to accommodate the lower integration limit without an increase of the total noise.

3. Derive an expression for the input referred voltage noise of an NMOS common-source amplifier M1 with PMOS load M2. Assume M1 and M2 are both in saturation and that a capacitor C_L dominates the load at the output. Specify the result as the noise from M1 multiplied by a factor that is a function of the V* of the two transistors. What does this imply about the V* you should choose for M1 vs. M2? You can neglect flicker noise for this analysis.

4. In this problem we will be working with the circuit shown below. You can assume that the transistors are saturated and ignore flicker noise for this problem.



   a) Ignoring all capacitors and the switch (i.e., assuming the switch is always on), calculate the voltage noise density at the output (V_{out}) due to the current noise from M_1.

   b) Repeat part a), but now find the voltage noise density at the output due to the current noise from R_L and from M_2.

c) Using your results from parts a) and b), calculate the ratio of thermal noise contributed by M_2 relative to the thermal noise due to M_1. Based on this expression, comment on how the DC biasing of M_2 affects its contribution to the thermal noise at the output.

d) Now calculate the noise sampled on C_L when switch S1 is abruptly turned off after being on for a long period of time. You can assume that the current source is ideal (i.e., is noiseless) and that all capacitors except for C_L and C_1 are negligible.