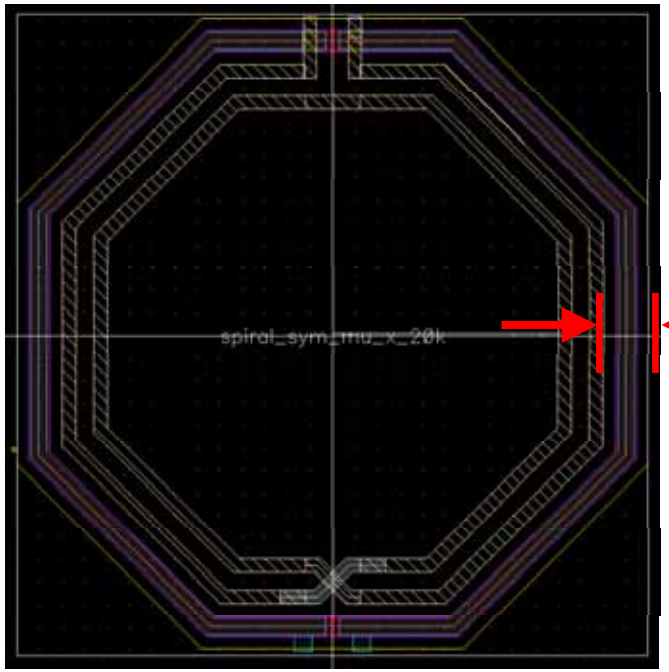
CR018 GPII Inductor Rule Violation SOTE



GRDIST=Distance between coil and INDDMY

•Customer may suffer the rule violation (UTM20K.E.3 & UTM40K.E.3) as using CR018 GPII Inductor PDK, due to TSMC had offered scalable guard-ring distance (10um~50um) for inductor of CR018 GPII. (T-018-LO-DR-001).

• Current rules definition:

UTM20K.E.3	Minimum extension of dummy"layer "INDDMY" region beyond one UTM region which used as one inductor device.	G	≧	50
UTM40K.E.3	Minimum extension of dummy"layer "INDDMY" region beyond one UTM region which used as one inductor device. Recommendations: 1. Keep this enclosure as small and as close to 50 um as possible. 2. Keep INDDMY regions for separate inductors located as uniformly as possible over the whole chip area.	G	≧	50

CR018 GPII IND Rule Violation SOTE

❑**Future Update Plan:**

- **TSMC will relax the rule and update DRM in 2010/Q2. “T-018-LO-DR-001”**
- **Please customer waive the rule violation caused by guard-ring distance as using CR018 GPII PDK, until DRM and new DRC deck update.**
- **The new rules update will be defined as following table: (It will be treated as recommendation rules).**

UTM20K.E.3U	Minimum extension of dummy"layer "INDDMY" region beyond one UTM region which used as one inductor device. Recommendations: Keep INDDMY regions for separate inductors located as uniformly as possible over the whole chip area.	G	≧	10
UTM40K.E.3U	Minimum extension of dummy"layer "INDDMY" region beyond one UTM region which used as one inductor device. Recommendations: Keep INDDMY regions for separate inductors located as uniformly as possible over the whole chip area.	G	≧	10

❑ **About the detail model offering scope, please refer to the most updated SPICE document “T-018-CM-SP-018”.**