UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

E. Alon **Homework #4/Mini Design Project** **EECS 240**
Due Thursday, Apr. 1, 2010

Use the EECS240 90nm CMOS process in all home works and projects unless noted otherwise. In this homework you may use just the typical (tt) device parameters.

1. **Capacitive Feedback Amplifier:** The bulk of this homework will deal with designing a nearly complete capacitive feedback amplifier. You can use ideal current and voltage sources and resistors to DC bias your amplifier, but you have to actually implement any current source loads in the signal path. As long as you meet the specifications, you are free to use any amplifier topology you'd like.

   Your goal in this design will be to minimize power dissipation while meeting the following required specifications:

   1. Target closed-loop gain: 2
   2. Settling time: 10ns
   3. Settling accuracy: <0.25%
   4. Integrated output noise from 1MHz to 100GHz: <300μV
   5. Output swing: +/-150mV.

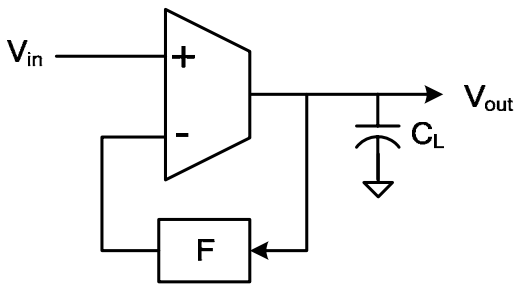
   Note that output swing is defined based on meeting the settling accuracy constraint. In other words, if you quote your output swing as +/-150mV, your output must settle to within +/-375μV.

   To verify the noise performance of your amplifier, you should use the .noise analysis in HSPICE. This analysis requires a .ac analysis to be performed first. As an example, to find the total noise at node vo (and also calculate it when referred to an input source vi), we could use the following statements:

   .ac dec 100 1x 100g
   .noise v(vo) vi dec 100 1x 100g

   In addition to a final spice deck and a clearly labeled schematic of your design, you should submit a description of the procedure you followed to design the circuit (including your intermediate calculations/results). In addition, you should submit print-outs and plots from the simulations you ran to verify the 5 design specifications.

2. **Settling Time:** In this problem we will be examining the settling behavior of the feedback OTA shown below. You can assume that the circuit that implements the feedback gain F has no loading on the OTA. Furthermore, you can assume that the OTA is implemented by a simple differential pair with a total bias current of I_{bias}, and that the transistors in this differential pair have a given V*.



a) Assuming purely linear settling, derive an expression for the settling time of this OTA as a function of the relative error ε, the load capacitance C_L, the feedback factor F, the bias of the input transistors V*, and the bias current I_{bias}.

b) Now re-derive an expression for the settling time including the fact that the OTA might slew. Your expression should be a function of the same parameters as in part a), along with the magnitude of the input step V_{i_step}.