EECS240 – Spring 2010

Lecture 21: Matching

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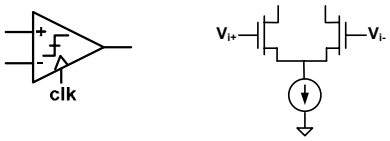
Offset



- To achieve zero offset, comparator devices must be perfectly matched to each other
- How well-matched can the devices be made?
  - Not arbitrary – direct function of design choices

Device Mismatch Categories

- Die-to-die
  - All devices on same chip (or wafer) have same characteristics
- Within die (long-range)
  - All devices within certain region have same characteristics
- Local (short-range)
  - Every device different, random
  - Usually most important source of mismatch

Sources of Local Variation

- Deterministic sources:
  - Local poly density
  - Sub-90nm: stress, litho interactions, …
- Random sources:
  - Dopant fluctuations
  - Line-edge roughness
  - Oxide traps
- Focus our modeling on random variations
  - Deterministic handled with good layout practices

References

- M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE JSSC,* vol. 24, pp. 1433 - 1439, Oct. 1989
  - Mismatch model
  - Statistical data for 2.5μm CMOS
- J. A. Croon, M. Rosmeulen, S. Decoutere, W. Sansen, and H. E. Maes, "An easy-to-use mismatch model for the MOS transistor," *IEEE JSSC*, vol. 37, pp. 1056 - 1064, Aug. 2002
  - 0.18μm CMOS data

Mismatch Statistics

- Total mismatch set by composite of many single, independent events
  - Correlation distance << device dimensions
  - E.g., number of dopant atoms implanted into the channel
- Individual effects are small: linear superposition holds
- → Mismatch is zero mean, Gaussian distribution

Parameter Mismatch Model

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2$$

$\sigma^2(\Delta P)$: variance of P
WL: active gate area
D_x: distance between device centers
A_P: measured area proportionality constant
S_P: measured distance proportionality constant,
: $\cong 0$ for "good" layout

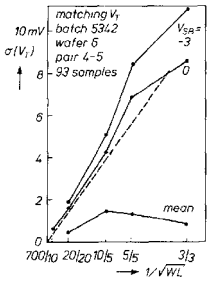
V_T Mismatch

- **Mismatch in V_T between two identical devices:**

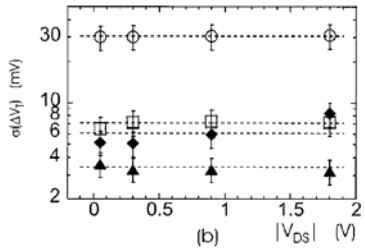
$$\sigma^2(\Delta V_T) = \frac{A_{V_T}^2}{WL} + S_{V_T}^2 D_x^2$$

2.5μm CMOS process:
$A_{V_T,NMOS} \cong 30$ mV μm
$A_{V_T,PMOS} \cong 35$ mV μm

- **Often largest source of offset**



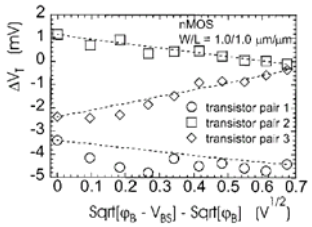
Drain Bias, V_{DS}



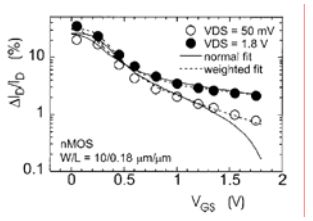
ΔV_T largely independent of V_{DS}

Back-Gate Bias, V_{SB}

- **Mismatch can depend on V_{SB}**
- **Why?**

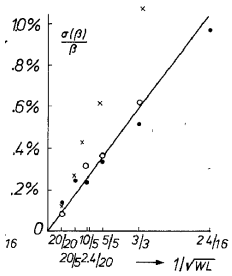


Current Matching, $\Delta I_D/I_D$



Strong bias dependence (we knew that already)

Current Factor



$$\beta = \mu C_{ox} \frac{W}{L}$$

Sources of β Mismatch

- **Mobility variations**
  - **E.g., due to dopant variations, random defects**
- **Oxide thickness variation**
  - **Usually very well-controlled**
- **Edge roughness**

Edge Model

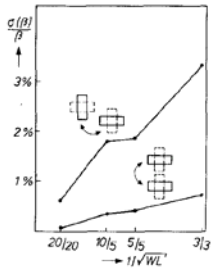
$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{\sigma^2(W)}{W^2} + \frac{\sigma^2(L)}{L^2} + \frac{\sigma^2(C_{ox})}{C_{ox}^2} + \frac{\sigma^2(\mu_n)}{\mu_n^2}$$

For: $\sigma^2(W) \propto 1/L$ and $\sigma^2(L) \propto 1/W$

Simplifies to:

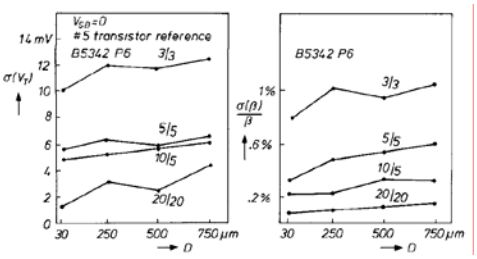
$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_L^2}{WL^2} + \frac{A_W^2}{W^2L} + \frac{A_{C_{ox}}^2}{WL} + \frac{A_\mu^2}{WL} + S_\beta^2 D^2$$

Orientation Effects



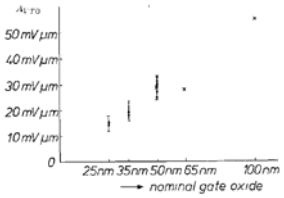
- **Si and transistors are not (perfectly) isotropic**
- **→ keep direction of current flow same!**

Distance Effect

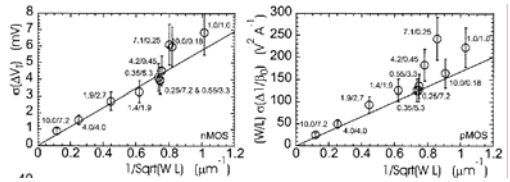


Process Dependence

- **A_{Vt} tends to scale with technology**
- **Proportional to t_{ox}**
- **Also depends on doping level**



0.18 µm CMOS



Current Matching

Voltage Matching

"Golden Rule" of Layout for Matching

- Everything you can think of might matter
  - Even whether or not there is metal above the devices
- How to avoid systematic errors?

Ref: A. Hastings, "The art of analog layout," Prentice Hall, 2001

Common Centroid Layout

- Cancels linear gradients
- Required for moderate matching

Simulating Mismatch

- Brute force: Monte Carlo
  - HSPICE "throws the dice"…

Simulating Mismatch