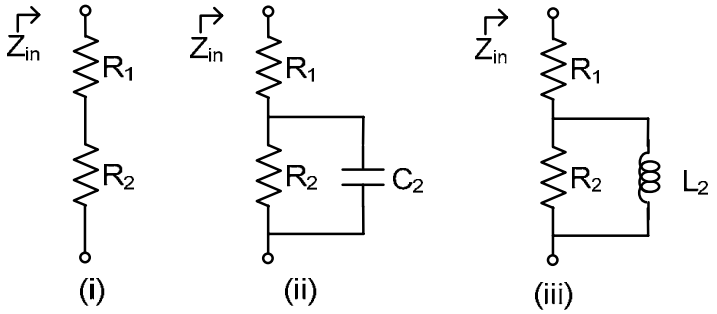
UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

E. Alon **Homework #3** **EECS 240**
Due Thursday, March 4, 2010

Use the EECS240 90nm CMOS process in all home works and projects unless noted otherwise. In this homework you may use just the typical (tt) device parameters.

1. **Pole-Zero Doublets:** In this problem we will be looking at the behavior of the circuits shown below in order to gain some intuition into the origin and response of pole-zero doublets.

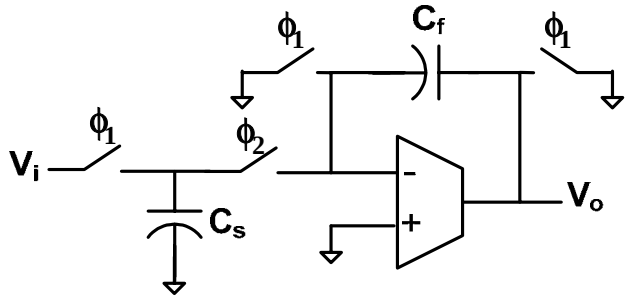


   a. Without doing any math, how will the magnitude of the impedance of circuits (ii) and (iii) compare with circuit (i)? In other words, will those circuits always have lower, higher, or the same impedance as circuit (i)?
   b. Derive the impedance $Z_{in}(s)$ of circuits (i), (ii), and (iii).
   c. Now derive and sketch the time-domain voltage response of circuits (i) and (ii) to a current step. Hint: immediately after the current step, what is the voltage across circuit (ii)? What is the final value of the voltage?
   d. For parts d. and e. of this problem, we will consider the following transfer function (with ω_{p1}, ω_{p2}, and ω_z all real and positive) :

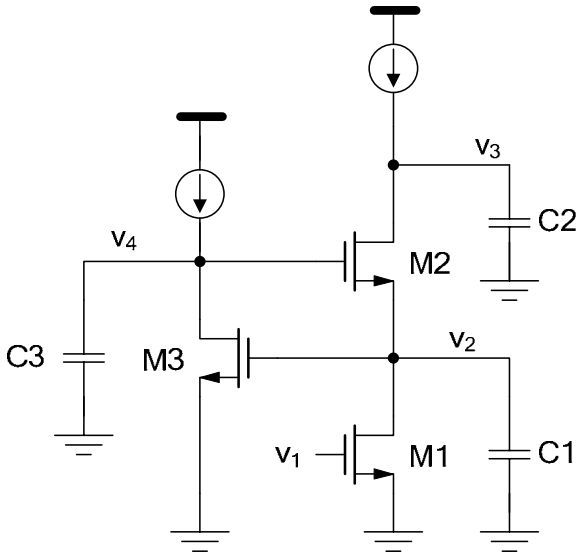
$$H(s)=\frac{(1+s/\omega_z)}{(1+s/\omega_{p1})(1+s/\omega_{p2})}$$

   Sketch $\|H(j\omega)\|$ as a function of ω for (1) $\omega_{p1} < \omega_z < \omega_{p2}$ and (2) $\omega_{p1} < \omega_{p2} < \omega_z$.
   e. Sketch the time domain step response of H(s) for cases (1) and (2). Will the step response ever overshoot its final value in these two cases? Hint: you may want to find an $H_1(s)$ and $H_2(s)$ such that $H(s) = c_1H_1(s) + c_2H_2(s)$. – i.e., you should use a partial fraction expansion.

2. **Switched-capacitor amplifier:** What is the total noise variance at the output of the switched capacitor amplifier shown below at the end of a complete cycle (i.e., during φ_2)? You can assume that the OTA is simply implemented by an NMOS common-source stage with a given g_m and infinite r_o.



3. **Gain Boosted Cascode:** This problem will focus on the gain-boosted cascode amplifier shown below. To simplify the analysis, you can ignore the r_o of the transistors and all of the capacitors except for those explicitly drawn in the diagram.



a. What is the frequency response $H(s) = v_3(s)/v_1(s)$ of this amplifier? Approximately what is the unity gain frequency of the amplifier?
b. Approximately what conditions are required to guarantee that the gain boosting feedback loop maintains at least 45º of phase margin? You should provide your answer in terms of g_{m1}, g_{m2}, g_{m3}, C1, C2, and C3.
c. Assuming this amplifier is used in unity gain feedback, what conditions are required to guarantee that the gain boosting feedback loop does not introduce any significant pole-zero doublets that might limit the settling response?
d. In order to meet the criteria from parts b) and c) and assuming that $C_1 = C_3 = 50\text{fF}$, $C_2 = 2\text{pF}$, $V^*_{M1} = 150\text{mV}$, and $V^*_{M2} = 100\text{mV}$, what are the minimum and maximum g_{m3}/g_{m1}?