C2 Interface

The Silicon Labs 2-Wire Interface (C2) is a two-wire serial communication protocol designed to enable in-system programming, debugging, and boundary-scan testing on low pin-count Silicon Labs devices. C2 communication involves an interface master (the programmer/debugger/tester), and an interface target (the device to be programmed/debugged/tested). The two wires used in C2 communication are C2 Data (C2D) and C2 Clock (C2CK).

C2 facilitates a pin-sharing scheme, where the C2 pins on the target device are available for user functions while C2 communication is idle. Each C2 frame is initiated with a START condition on the C2CK pin that signals the target device to configure its C2D pin for C2 communication. Each C2 frame is terminated with a STOP condition on the C2CK signal that allows the target device to restore its C2D pin to its user-defined state. The C2CK signal is shared with an active-low /RST signal on the target device. In this configuration the width of a low strobe is used to differentiate between a C2 communication strobe and a reset event.

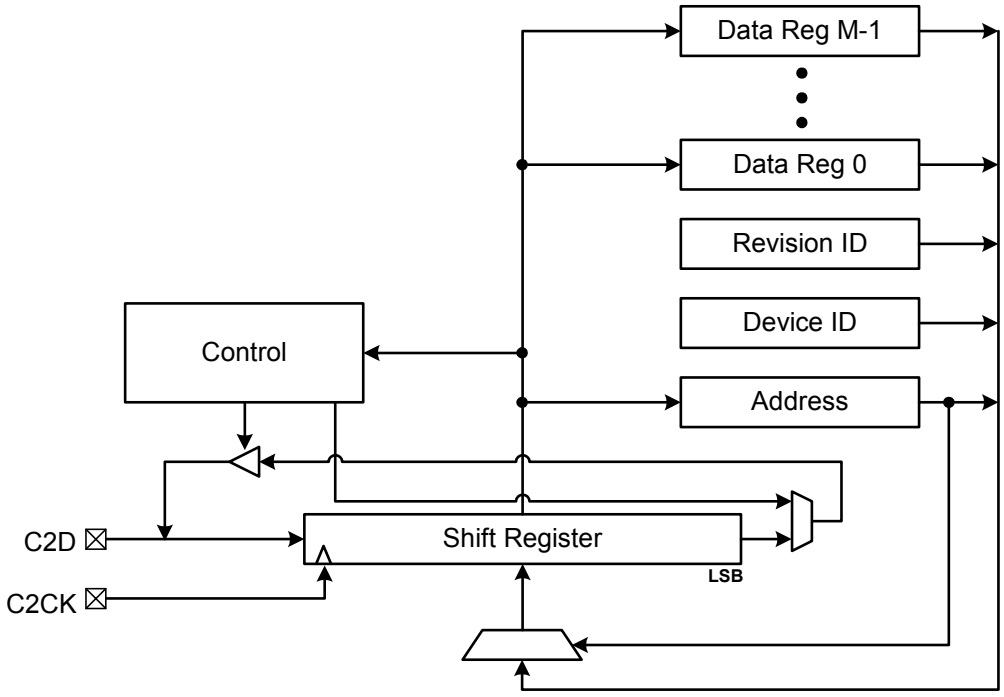


Figure 1. C2 Interface Block Diagram

C2 Interface

C2 Basics

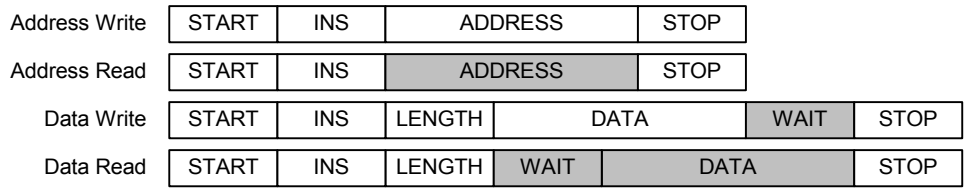
The C2 interface operates similar to JTAG, with the three JTAG data signals (TDI, TDO, TMS) mapped into one bi-directional C2 data signal (C2D). The signal direction of C2D is strictly specified by the instruction protocol such that contention between the target device and interface master is never allowed. All data is transmitted and received LSB first.

The C2 interface provides access to on-chip programming and debug hardware through a single Address register and a set of Data registers, as shown in Figure 1. The Address register defines which Data register will be accessed during Data register read/write instructions (analogous to the JTAG Instruction register). Data registers provide access to various device-specific functions (note: it is not required that all Data registers be both readable and writable). Read and write access to all registers is performed through a common shift register that serves as a serial-to-parallel-to-serial converter.

All C2 devices include an 8-bit Device ID register and an 8-bit Revision ID register. These registers are read-only. Following a device reset, the C2 Address register defaults to 0x00, selecting the 8-bit Device ID register. This allows a C2 master to perform a Device ID register read without knowing the length of the target device's Address register. The length of the target Address register can then be determined using the Device ID register content.

C2 Instruction Frames

A C2 master accesses the target C2 device via a set of four basic C2 frame formats: Address Write, Address Read, Data Write, and Data Read. These frames are summarized in Figure 2; detailed descriptions follow. All C2 bit fields are described in Table 2 on page 3.



Note: During shaded fields, the C2D signal is driven by the target device.

Figure 2. C2 Frame Summary

Note that the master initiates each frame with the START and INS (Instruction) fields. The content of the INS field defines the frame format. The four C2 instructions are listed in Table 1.

Table 1. C2 Instructions

Instruction	INS Code
Data Read	00b
Address Read	10b
Data Write	01b
Address Write	11b

Table 2. C2 Bit Field Descriptions

	Field	Description
Generated by Master Only	START	A START condition initiates a C2 frame. The master generates this condition by leaving its C2D driver disabled and generating an active-low strobe on C2CK. All C2 frames begin with the START field.
	INS	The INS field is a 2-bit code specifying the current C2 instruction. The four valid C2 instructions are shown in Table 1. All C2 frames include the INS field.
	STOP	A STOP condition ends a C2 frame. The master generates this condition by disabling its C2D driver and generating an active-low C2CK strobe. The slave returns C2D to its user-defined state on the rising edge of this C2CK strobe. All C2 frames are terminated with the STOP field.
	LENGTH	The LENGTH field is a 2-bit code indicating the number of bytes to be read or written during Data register accesses. The number of bytes to transfer is LENGTH + 1 (for example, LENGTH = 01b results in a 2-byte transfer).
Master or Slave	ADDRESS	The ADDRESS field is used to transfer data during Address register accesses. The length of this field must be the same length as the slave device's Address register. The Address register defaults to all zero's following any reset, selecting the Device ID register.
	DATA	The DATA field appears in Data register accesses; the length of this field is determined by the LENGTH field as described above.
Slave Only	WAIT	A WAIT field appears during Data Read and Data Write frames to allow the slave device to access slower registers or memories. This variable-length field consists of a series of zero or more '0's transmitted by the slave device, terminated by a single '1'.

Note: All fields are transmitted LSB first.

Address Write Frame

An Address Write frame loads the target Address register. The Address Write sequence is shown in Figure 3.

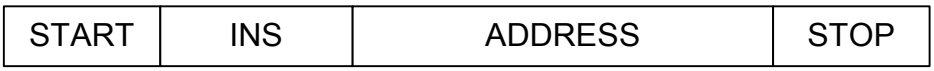


Figure 3. Address Write Sequence

The length of the ADDRESS field must always be the length of the slave device's Address register. Following a device reset, the target device's Address register defaults to all zeros, selecting the Device ID register. **Note: All fields are transmitted LSB first.**

Address Read Frame

An Address Read frame returns status information or Address register contents from the target device. This instruction is typically used to quickly access status information, though the function of the Address Read instruction is target device-specific. The Address Read sequence is shown in Figure 4.

Figure 4. Address Read Sequence

The length of the ADDRESS field must always be the length of the slave device's Address register. **Note: All fields are transmitted LSB first.**

Data Write Frame

A Data Write frame writes a specified value to the target Data register, as selected by the target Address register. The Data Write sequence is shown in Figure 5.

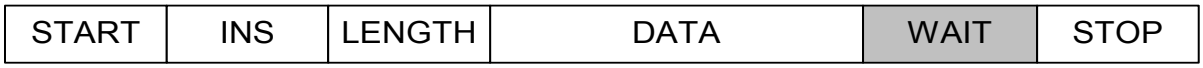


Figure 5. Data Write Sequence

LENGTH is a 2-bit field that specifies the length of the DATA field as follows:

DATA Length in bytes = (LENGTH + 1)

The DATA field length must be a multiple of 8 bits. For example, a LENGTH of 01b indicates a DATA length of 2 bytes. The length of the DATA field is not required to be the same length as the target Data register. For example, to write only the eight MSB's of a 10-bit register, LENGTH is set to 00b and DATA specifies only 8 bits of data to be written to the 8 MSB's of the target register. The remaining register bits are undefined. To write all 10 bits of data, LENGTH should be 01b; in this case (shown in Figure 6), the 10 MSB's of the 16-bit DATA field are written to the target register. **Note: All fields are transmitted LSB first.**

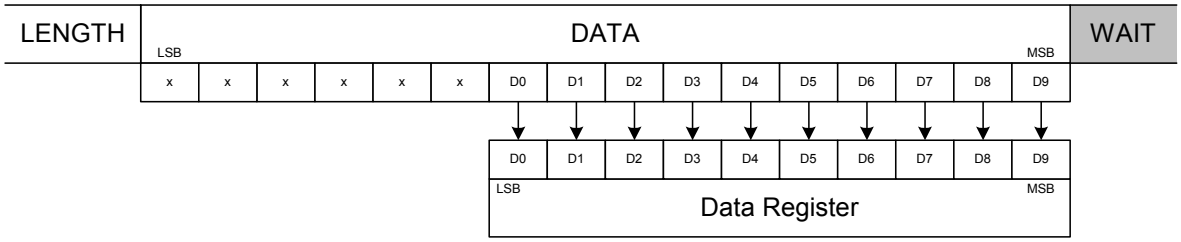


Figure 6. DATA Field for a 10-bit Data Register Write

The length of the WAIT field is controlled by the target device. During the WAIT field, the target device transmits '0's on the C2D pin until it has finished writing to the target Data register. To indicate the write complete status, the target device transmits a '1' to terminate the WAIT field.

Data Read Frame

A Data Read frame reads the contents of the target Data register, as selected by the target Address register. The Data Read sequence is shown in Figure 7.

Figure 7. Data Read Sequence

LENGTH is a 2-bit field that specifies the length of the DATA field as follows:

DATA Length in bytes = (LENGTH + 1)

The DATA field length must be a multiple of 8 bits. For example, a LENGTH of 01b indicates a DATA length of 2 bytes. As with the Data Write frame, the length of the DATA field is not required to match the length of the target Data register. In this case, the read data is right justified in the DATA field. For example, if LENGTH is 00b (1 byte) and the target register is 12-bits, the 8 LSBs of the target register are read into the DATA field. If LENGTH is 01b (2 bytes) and the target register is 12-bits, the 12-bit Data register makes up the 12 LSBs of the DATA field; the remaining 4 bits are undefined (shown in Figure 8). **Note: All fields are transmitted LSB first.**

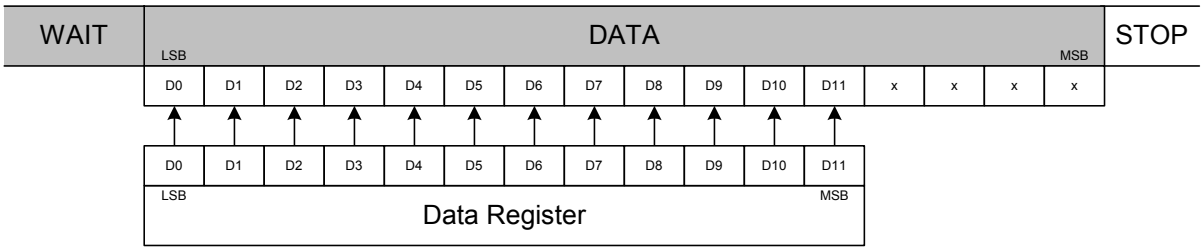


Figure 8. DATA Field for a 12-bit Data Register Read

The length of the WAIT field is controlled by the target device. During the WAIT field, the target device transmits ‘0’s on the C2D pin until it has finished reading the target Data register and is ready to shift out data. To indicate the ready status, the target device transmits a ‘1’ to terminate the WAIT field.

C2 Timing Specifications

The following sections illustrate the timing sequence for each of the four C2 frame formats and the device reset command. Table 3 on page 9 lists all C2 timing specifications.

The slave device samples input data and updates output data on rising edges of C2CK. In the following illustrations, shaded C2D bits indicate times when the master's C2D driver must be disabled.

Device Reset Timing

During C2 instructions, C2CK must not be held low longer than t_{CL}. This requirement allows the device to be reset by holding C2CK low for t_{RD}. The START field of the first C2 instruction must begin at least t_{SD} after C2CK returns high following a device reset. See Figure 9.

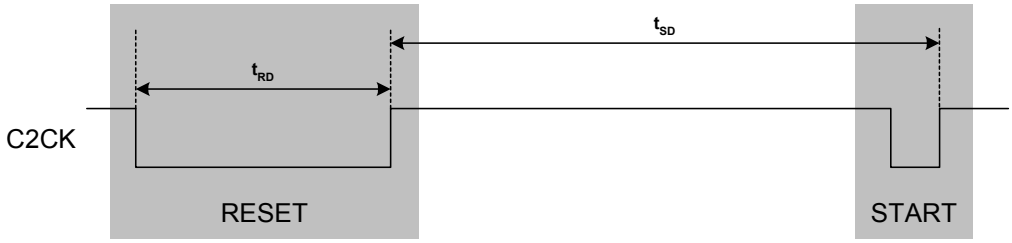


Figure 9. Device Reset Timing

Address Write Timing

Figure 10 shows the timing for an 8-bit Address Register Write frame. The frame begins with a START (rising edge on C2CK). Note that during a START condition, the master's C2D driver should be disabled. Following the START, the interface master must enable its C2D driver to transmit the INS and ADDRESS bits. Following the last ADDRESS bit, the master disables its C2D driver and strobes C2CK one last time for the STOP field; the slave device returns the C2D pin to its user-defined state following the last rising edge on C2CK.

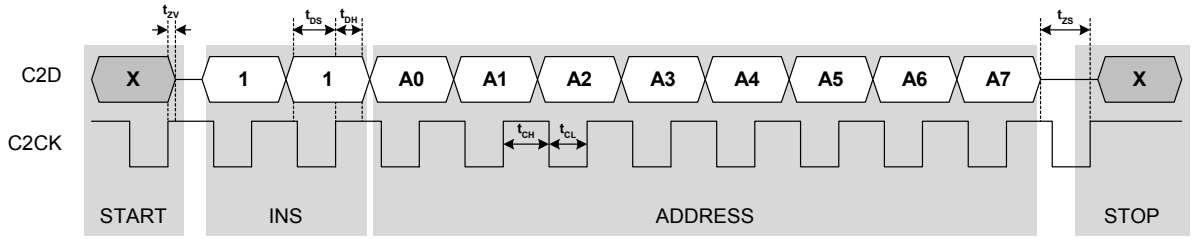


Figure 10. Address Write Timing

Address Read Timing

Figure 11 shows the timing for an 8-bit Address Register Read frame. The frame begins with a START followed by the 2-bit INS field. Following the INS bits, the interface master disables its C2D driver and strobes C2CK; the slave device outputs the LSB of its Address register on the rising edge of C2CK. Seven more C2CK strobes are required to complete the ADDRESS field. Following the last ADDRESS bit, the master strobes C2CK one last time for the STOP field; the slave device returns the C2D pin to its user-defined state following the last rising edge on C2CK.

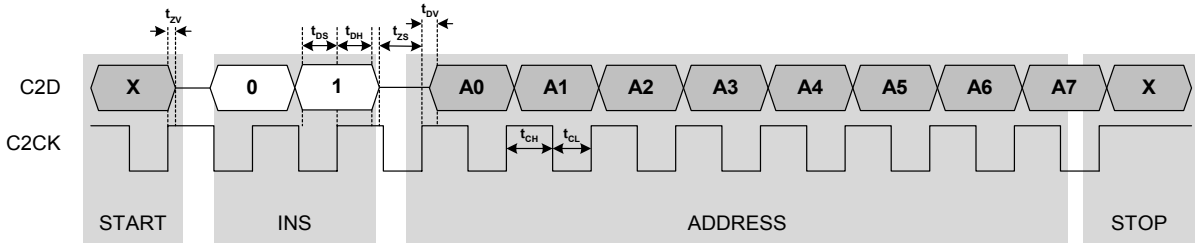


Figure 11. C2 Address Register Read Timing

Data Write Timing

Figure 12 shows the timing for a 1-byte Data Register Write frame. The frame begins with a START followed by the 2-bit INS and 2-bit LENGTH fields. In this example, the LENGTH field is 00b indicating a 1-byte transfer. The master transmits the 8-bits of data; following the last DATA bit, the master disables its C2D driver for the WAIT field. In this example the slave transmits only one '0' during the WAIT field. Following the WAIT field, the master strobes C2CK one last time for the STOP field; the slave device returns the C2D pin to its user-defined state following the last rising edge on C2CK.

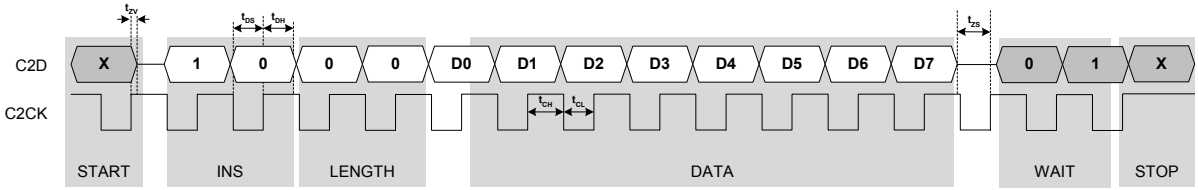


Figure 12. Data Write Timing

Data Read Timing

Figure 13 shows the timing for a 1-byte Data Register Read frame. The frame begins with a START followed by the 2-bit INS and 2-bit LENGTH fields. In this example, the LENGTH field is 00b indicating a 1-byte transfer. After the last bit of the LENGTH field is transmitted, the master disables its C2D driver for the WAIT field. In this example only one '0' is transmitted during the WAIT field. Following the WAIT field, the master strobes C2CK and the slave shifts out the DATA field. Following the last DATA bit, the master strobes C2CK one last time for the STOP field; the slave device returns the C2D pin to its user-defined state following the last rising edge on C2CK.

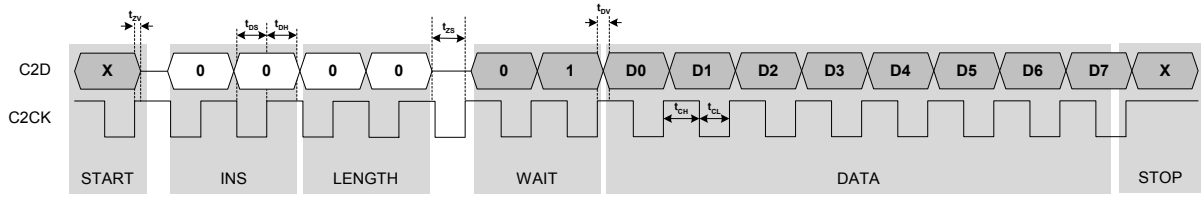


Figure 13. Data Read Timing

Table 3. C2 Timing Requirements

Parameter	Description	Min.	Max.
t_{RD}	C2CK low time for a device reset	20µs	-
t_{SD}	Start bit delay after a device reset	2µs	-
t_{CL}	C2CK low time for bit transfers	20ns	5000ns
t_{CH}	C2CK high time	20ns	-
t_{DS}	C2D setup	10ns	-
t_{DH}	C2D hold	10ns	-
t_{ZS}	C2D High-Z Setup	0ns	-
t_{DV}	C2D valid	-	20ns
t_{ZV}	C2D High-Z valid	-	20ns

C2 Interface

Contact Information

Silicon Laboratories Inc.

4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: productinfo@silabs.com
Internet: www.silabs.com