Documentation Registres MAX9271

mwrite (i2cport , addr , registre , valeurs);

```
mwrite (i2cport, 0x40, 0x02, 0x1C);
```

- PRNG=11 => Automatically detect the pixel clock range.
- SRNG=00=>Automatically detect the pixel clock range.

```
mwrite (i2cport, 0x40, 0x03, 0x00);
```

- AUTOFM=00=> Calibrate spread-modulation rate only once after locking.
- SDIV=00000=>Autocalibrate sawtooth divider.

```
mwrite (i2cport, 0x40, 0x04, 0x83);
```

- SEREN=1=>Disable serial link. Reverse control-channel communication remains unavailable for 350Fs after the serializer starts/stops the serial link.
- CLINKEN=0
- PRBSEN=0
- SLEEP=0
- INTTYPE=00
- REVCCEN=1=>Enable reverse control channel from deserializer (receiving)
- FWDCCEN=1=>Enable forward control channel to deserializer (sending)

```
mwrite (i2cport, 0x40, 0x05, 0x80);
```

- I2CMETHOD=1 =>Disable sending of I2C register address when converting UART to I2C (command-byte-only mode).
- ENJITFILT=0
- PRBSLEN=00
- ENWAKEN=0
- ENWAKEP=0

```
mwrite (i2cport, 0x40, 0x06, 0x50);
```

- CMLLVL=0101 =>250mV output level.
- PREEMP=0000=>Preemphasis off.

```
mwrite (i2cport, 0x40, 0x07, 0x06); // perd le lock, car Hamming code enable
```

- DBL=0
- DRS=0
- BWS=0
- ES=0
- HVEN=1=>HS/VS encoding enabled. Power-up default when LCCEN = low and MS/HVEN = high.

- EDC=10=>6-bit hamming code (single-bit error correct, double-bit error detect) and 16 word interleaving. Power-up default when LCCEN = low and RX/SDA/EDC = high.

```
sleep(0.020); // DS : tLock 2ms (link start time), serializer delay ~ 17ms
mwrite (i2cport, 0x48, 0x07, 0x0E); // retrouve le lock
sleep(0.020);
mwrite (i2cport, 0x40, 0x08, 0x00);
```

- INVVS =0=>No VS or DIN0 inversion.
- INVHS=0 =>No HS or DIN1 inversion.

```
mwrite (i2cport, 0x40, 0x09, 0x00);
```
- réservé

```
mwrite (i2cport, 0x40, 0x0A, 0x00);
```
- réservé

```
mwrite (i2cport, 0x40, 0x0B, 0x00);
```
- réservé

```
mwrite (i2cport, 0x40, 0x0C, 0x00);
```
- réservé

```
mwrite (i2cport, 0x40, 0x0D, 0x6E);
```
- I2CLOCACK=0=>Acknowledge not generated when forward channel is not available.
- I2CSLVSH=11=>1046ns/469ns I2C setup/hold time.
- I2CMSTBT=011=>105kbps (typ) I2C-to-I2C master bit-rate setting
- I2CSLVTO=10=>1024Fs (typ) I2C-to-I2C slave remote timeout

```
mwrite (i2cport, 0x40, 0x0E, 0x42);
```
- DIS_REV_P=0=>OUT+ reverse channel receiver enabled.
- DIS_REV_N=1=>OUT- reverse channel receiver disabled.
- GPIO5EN=0
- GPIO4EN=0
- GPIO3EN=0
- GPIO2EN=0
- GPIO1EN=1=>Enable GPIO1
- reserved

```
mwrite (i2cport, 0x40, 0x0F, 0xC2);
```
- reserved 00
- GPIO5OUT=0
- GPIO4OUT=0
- GPIO3OUT=0
- GPIO2OUT=0
- GPIO1OUT=1=>Set GPIO1 high.
- SETGPO=0

0x02	0x1F	SS = 000 no spread spectrum RESERVED = 1 PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial-data rate
0x03	0x00	AUTOFM = 00, calibrate spread-modulation rate only once after locking SDIV = 000000, autocalibrate sawtooth divider
0x04	0x87	SEREN = 1, serial link enabled CLINKEN = 0, configuration link disabled PRBSEN = 0, PRBS test disabled SLEEP = 0, sleep mode disabled (see the *Link Startup Procedure* section) INTTYPE = 01, local control channel uses UART REVCCEN = 1, reverse control channel active (receiving) FWDCCEN = 1, forward control channel active (sending)
0x05	0x00	I2CMETHOD = 0, I²C packets include register address ENJITFILT = 0, jitter filter disabled PRBSLEN = 00, continuous PRBS length RESERVED = 00 ENWAKEN = 0, OUT- wake-up receiver disabled ENWAKEP = 1, OUT+ wake-up receiver enabled
0x06	0x80, 0xA0	CMLLVL = 1000 or 1010, output level determined by the state of CONF1 and CONF0 at power-up PREEMP = 0000, preemphasis disabled
0x07	0xXX	DBL = 0 or 1, single-/double-input mode setting determined by the state of LCCEN and TX/SCL/DBL at startup DRS = 0, high data-rate mode BWS = 0 or 1, bit width setting determined by the state of LCCEN and GPIO1/BWS at startup ES = 0 or 1, edge-select input setting determined by the state of LCCEN and TX/SCL/ES at startup RESERVED = 0 HVEN = 0 or 1, HS/VS tracking encoding setting determined by the state of LCCEN and MS/HVEN at startup EDC = 00 or 10, error-detection/correction setting determined by the state of LCCEN and RX/SDA/EDC at startup
0x08	0x00	INVVS = 0, serializer does not invert VSYNC INVHS = 0, serializer does not invert HSYNC RESERVED = 000000

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x09	0x00	I2CSRCA = 0000000, I²C address translator source A is 0x00 RESERVED = 0
0x0A	0x00	I2CDSTA = 0000000, I²C address translator destination A is 0x00 RESERVED = 0
0x0B	0x00	I2CSRCB = 0000000, I²C address translator source B is 0x00 RESERVED = 0
0x0C	0x00	I2CDSTB = 0000000, I²C address translator destination B is 0x00 RESERVED = 0
0x0D	0xB6	I2CLOCACK = 1, acknowledge generated when forward channel is not available I2CSLVSH = 01, 469ns/234ns I²C setup/hold time I2CMSTBT = 101, 339kbps (typ) I²C-to-I²C master bit-rate setting I2CSLVTO = 10, 1024µs (typ) I²C-to-I²C slave remote timeout
0x0E	0x42	DIS_REV_P = 0, OUT+ reverse channel receiver enabled DIS_REV_N = 1, OUT- reverse channel receiver disabled GPIO5EN = 0, GPIO5 disabled GPIO4EN = 0, GPIO4 disabled GPIO3EN = 0, GPIO3 disabled GPIO2EN = 0, GPIO2 disabled GPIO1EN = 1, GPIO1 enabled RESERVED = 0
0x0F	0xFE	RESERVED = 11 GPIO5OUT = 1, GPIO5 set high GPIO4OUT = 1, GPIO4 set high GPIO3OUT = 1, GPIO3 set high GPIO2OUT = 1, GPIO2 set high GPIO1OUT = 1, GPIO1 set high SETGPO = 0, GPO set low