Analog Electronic Circuits(EC2.103): Course project

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***Abstract*—Quadrature down converters (QDCs) play a crucial role in modern wireless receivers, enabling interference mitigation and improving communication quality. This paper presents the design and implementation of a QDC prototype suitable for applications such as Bluetooth, Wi-Fi, and WLAN systems.**

Keywords—Quadrature oscillator, mixer, opamps, low pass filter (LPF)

I. Quadrature Down Converter

The QDC architecture consists of a quadrature oscillator, mixer stages, and low-pass filters to downconvert the input signal to an intermediate frequency (IF) while preserving the in-phase (I) and quadrature (Q) components. The quadrature oscillator generates two sinusoidal signals with a 90-degree phase difference, which are then mixed with the input signal to produce the I_{IF} and Q_{IF} signals. Low-pass filters are employed to extract the desired I_{FINAL} and Q_{FINAL} components.

Quadrature Oscillators are mainly used to decrease the frequency of the communication signal for superior signal quality at the receiver.

Another use of decreasing the frequency is in radio where the equipment that takes a radio frequency (RF) signal and converts it to a lower, intermediate frequency (IF) signal that is suitable for digital processing.

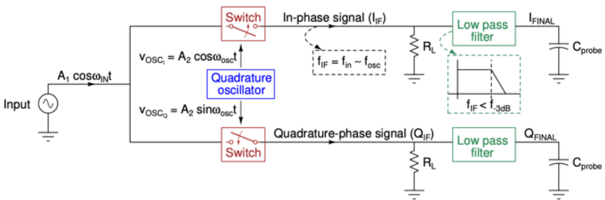

Fig 1: Quadrature Down Converter

II. Quadrature Oscillator

A. Introduction

The quadrature oscillator is one type of phase-shift oscillator, but the three RC sections are configured so that each section contributes 90° of phase shift. The outputs are labelled sine and cosine (quadrature) because there is a 90° phase shift between op amp outputs (see Figure 2).

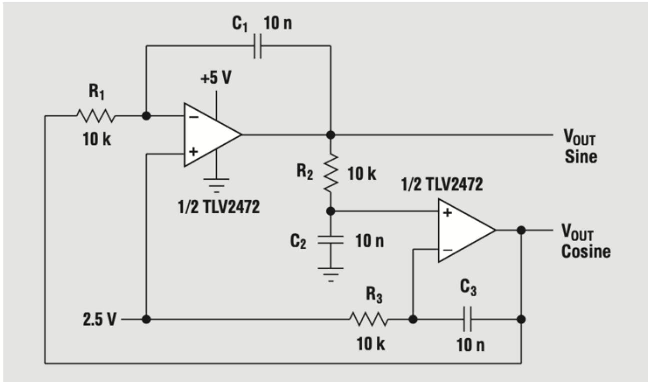

Fig 2 : Design of quadrature oscillator at 1.65KHz

B. Design of Quadrature oscillator

$$V_{OUT\ sine} = \frac{-V_{OUT\ cos}}{j\omega R_1 C_1} \quad (1)$$

$$V_{+2} = \frac{V_{OUT\ sine}}{1 + j\omega R_2 C_2} \quad (2)$$

$$V_{OUT\ cos} = V_{+2} \frac{1 + j\omega R_3 C_3}{j\omega R_3 C_3} \quad (3)$$

For stable oscillation, loop gain should be equal to 1. Eq. (1) ∗ Eq. (2) ∗ Eq. (3) = 1.

If $R_1C_1 = R_2C_2 = R_3C_3 = RC$, then

$$1 = \frac{1}{\omega^2 R^2 C^2} \quad (4)$$

$\omega = 1/RC$, $\omega = 1/2\pi f$. We want to generate oscillator for 100KHz, therefore $RC = 1.59 * 10^{-6}$. C = 10nf and R = 160Ω.

C. LTSpice Stimulation

Following figures display circuit and simulations, for simulation we have used R=125Ω and C=1.3nf

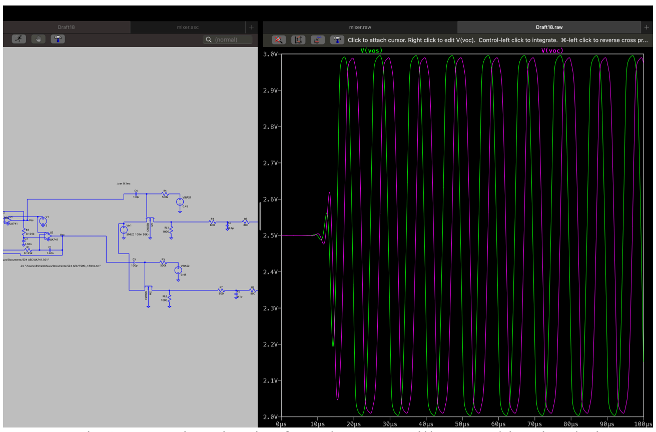

Fig 3 : LTSpice circuit of quadrature oscillator and its simulation

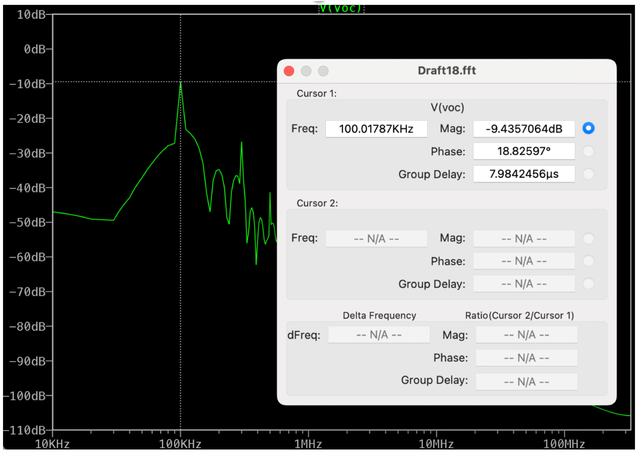

Fig 4 : FFT of output cos wave

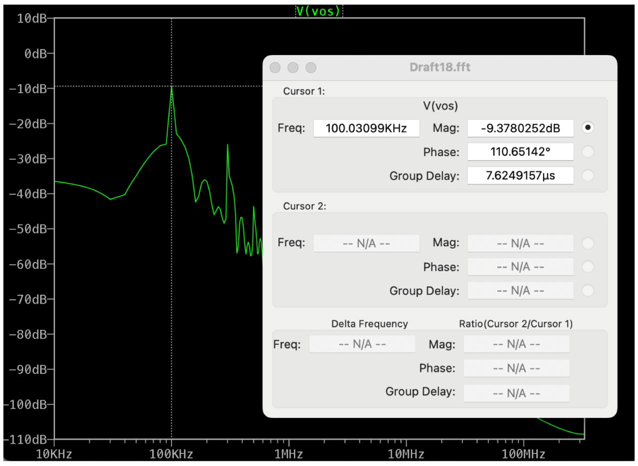

Fig 5 : FFT of output sine wave

Phase difference = 110 – 18 = 92degree.

D. Circuit Realization in Lab

For lab realization we used R=220Ω and C=1nf. V_{DD} = 7.7V and V_{SS} = 2.01V. Following figures display output of oscillator:

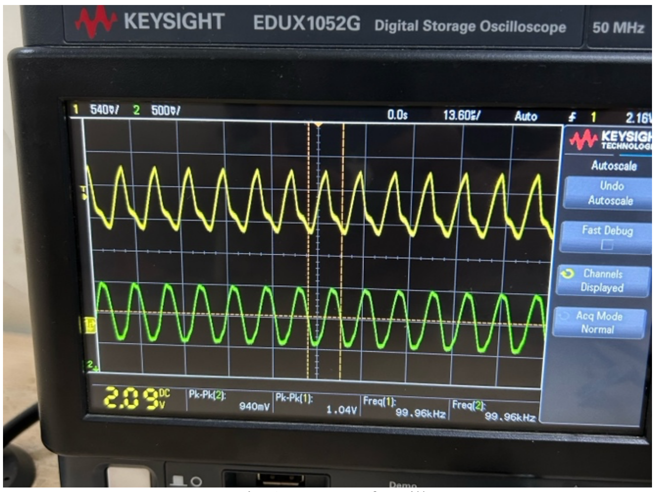

Fig 6 : Output of oscillator

III. Mixer

A. Introduction

Mixers are widely used to shift signals from one frequency range to another, for convenience in transmission or further signal processing.

B. Design of Mixer

We will be implementing mixer with switch mechanism with help of MOSFET. Current in drain terminal of NMOS is given as ($V_{DS} < V_{GS} – V_{TH}$: linear mode):

$$I_D = \frac{\mu_n C_{ox} W}{2L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \quad (5)$$

and when $V_{DS} << 2(V_{GS} - V_{TH})$ then current can be approximated as :

$$I_D = \frac{\mu_n C_{ox} W}{2L}[2(V_{GS} - V_{TH})V_{DS}] \quad (6)$$

And if $V_{TH} < V_{GS}$, then we will approximate $V_{GS} - V_{TH} = V_{GS}$. Hence $I_D = K(V_{GS}').(V_{DS})$. If we apply V_{OSC} at V_{GS} and V_{IN} at V_{DS} then,

$$V_{IN} * V_{OSC} = A_1 \sin \omega_{IN} t \, A_2 \sin \omega_{OSC} t \quad (7)$$

$$V_{IN} * V_{OSC} = \frac{A_1 A_2}{2}\left[\sin((\omega_{IN} - \omega_{OSC})t) \sin((\omega_{IN} + \omega_{OSC})t)\right]. \quad (8)$$

Also this mixing happens only when $V_{GS} > V_{TH}$. So we will turn MOSFET on and off repeatedly with V_{OSC}.

We will be using NMOS. V_{BIAS}(see Figure 7) will be equal to threshold voltage(V_{TH}) of NMOS which is 0.45V. We don't want any current in branch connecting gate to V_{BIAS} and hence we placed a high resistor R_{BIAS} (see Figure 7) of value 500KΩ.

To apply V_{OSC}(see Figure 7), which will turn on MOSFET for positive cycle and off for negative cycle, we want to connect it directly to gate with a capacitor, C_C(see Figure 7), between it and gate so voltage at gate is $V_{BIAS} + V_{OSC}$. Capacitor C_C along with R_{BIAS} is high pass filter. So we set C_C to 0.1uF, making high pass filter with -3dB frequency of 3Hz and consequently allowing every desired signal of 100KHz except DC signal. Load resistance R_L(see Figure 7) of 1KΩ was used as specified.

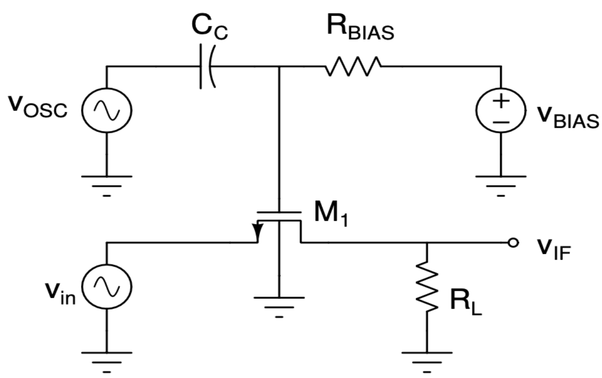

Fig 7 : Design of mixer(switch)

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C. *LTSpice Simulation*

For simulation purpose V_{OSC} is sine wave of 100mV_{PP} at 100KHz and V_{IN} is sine wave of 1V_{PP} at 101KHz.

Following figures demonstrate circuit and output of mixer simulation.

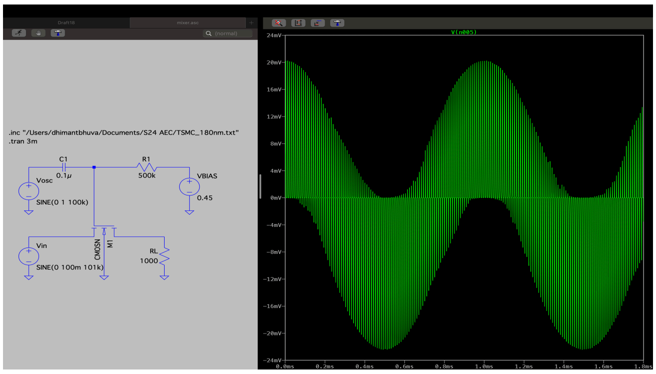

Fig 8 : LTSpice circuit of mixer(switch) and its simulation

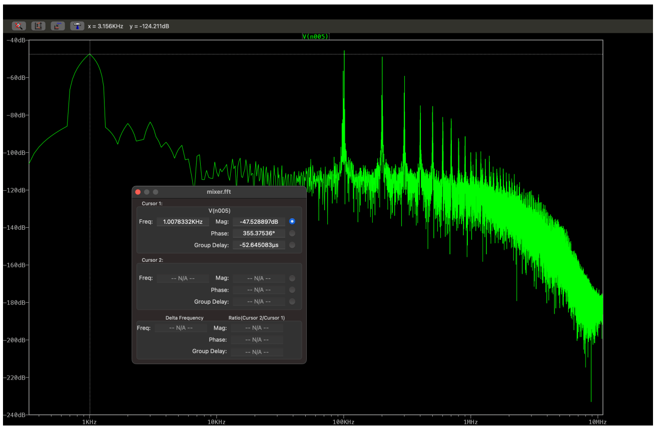

Fig 9 : LTSpice circuit of mixer(switch) fft with f_{IN}=99KHz

D. *Circuit Realization in Lab*

For lab realisation we are using IC CD4007 for MOSFET. NMOS in CD4007 has V_{TH}(threshold voltage) around 0.45V and hence V_{BIAS} of 0.45V was applied. As values used in simulation were not present in lab hence we used R_{BIAS} = 170KΩ and C_C = 0.1uF, which together act as high pass filter with -3dB frequency at 9.3Hz. Load resistance was provided as mentioned value of 1KΩ.

V_{OSC} was 1V_{PP} sine wave at 100KHz frequency whereas V_{IN} was sine wave of 100mV_{PP} with input frequency of 101KHz. Following figures display output of switch(mixer) :

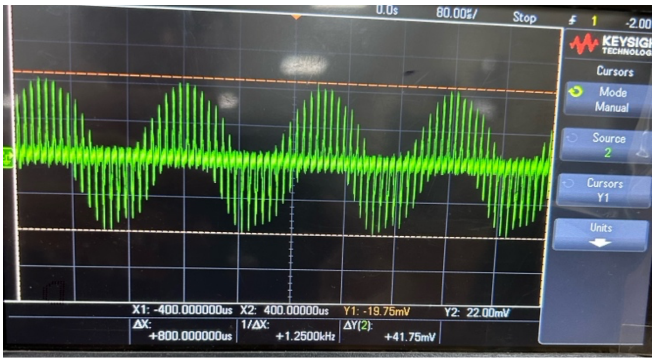

Fig 10 : Output of mixer

IV. Low Pass Filter(LPF)

A. *Introduction*

A low-pass filter (LPF) is a circuit that only passes signals below its cutoff frequency while attenuating all signals above it.

Output from mixer would contain two frequencies: $|f_{IN} - f_{OSC}|$ and $f_{IN} + f_{OSC}$, while former one is our only interest of frequency. To get the lower frequency we apply LPF at end of mixer and get the desired signal with frequency $|f_{IN} - f_{OSC}|$.

B. *Design of LPF*

A passive LPF, using a resistor and a capacitor, with -3dB cut-off frequency of 2KHz is used.

Following figure represents the circuit for a simple RC-LPF.

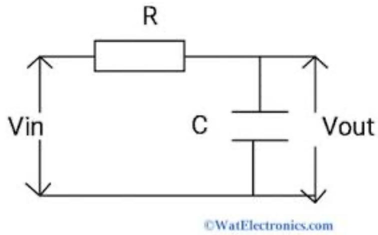

Fig 11 : circuit diagram of RC LPF

$$V_{OUT} = V_{IN}(1/1 + SRC) \tag{9}$$

Cut-off frequency, f_C or -3dB frequency, is defined when $V_{OUT} = V_{IN}/\sqrt{2}$.

So,

$$f_c = \frac{1}{2\pi RC} \tag{10}$$

For -3db frequency of 2KHz we selected R=8000Ω and C=10nF.

C. *LTSpice Simultion*

Following figures show circuit and simulation of LPF.

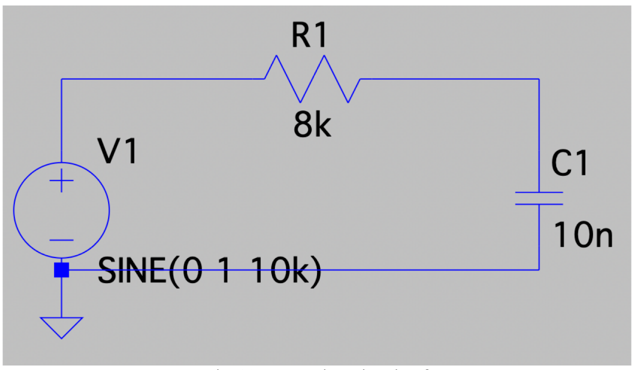

Fig 12 : LTSpice circuit of LPF

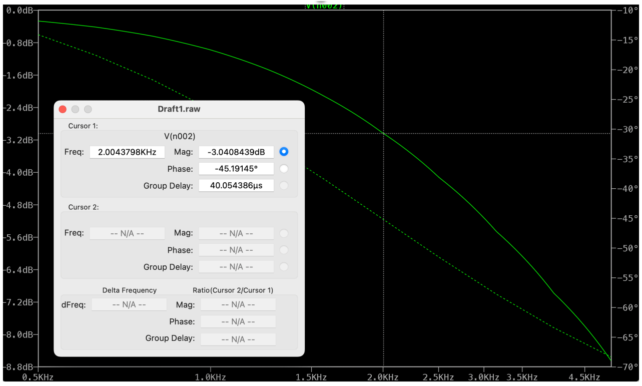

Fig 13 : -3dB representation at 2KHz

D. Circuit Realization in Lab

We implemented LPF with 3KHz as cut-off frequency to get less attenuation around 1KHz and less noise. So new value of R = 530Ω and C = 0.1µf.

Following figures demonstrate LPF:

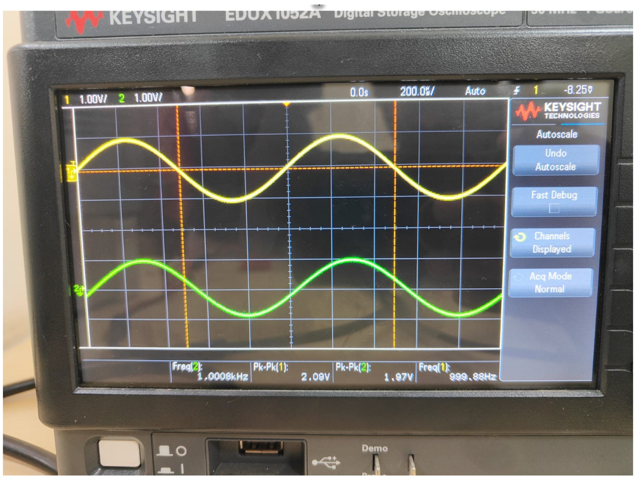

Fig 14 : LPF output vs input at 2KHz

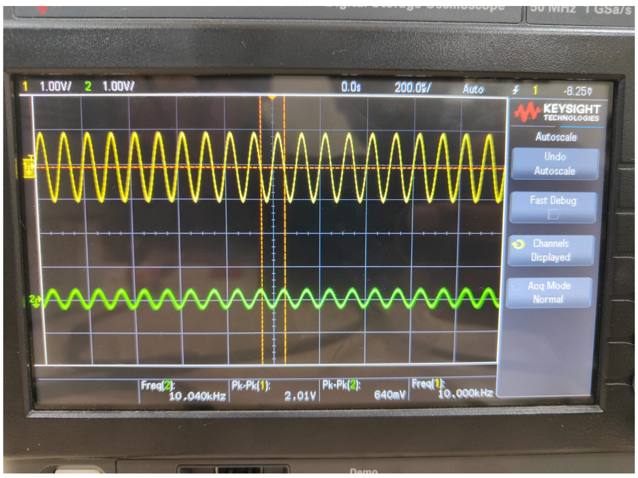

Fig 15 : LPF output vs input at 10KHz

V. COMPLETE CIRCUIT

The complete circuit prototype consists of combining all the above three components into a single circuit. so, Firstly the oscillator generates and feeds two waves,sine($V_{out\text{-}sine}$) and cosine($V_{out\text{-}cosine}$), into the mixer which multiplies it by the signal wave of chosen frequency(f_{IN}) and then the multiplied frequency signals, I_{IF} and Q_{IF}, is passed down to the low pass filter which filters out the wave component with the addition of the two frequencies(f_{IN}+f_{OSC}) to give I_{FINAL} and Q_{FINAL}($|f_{IN}$ - $f_{OSC}|$)

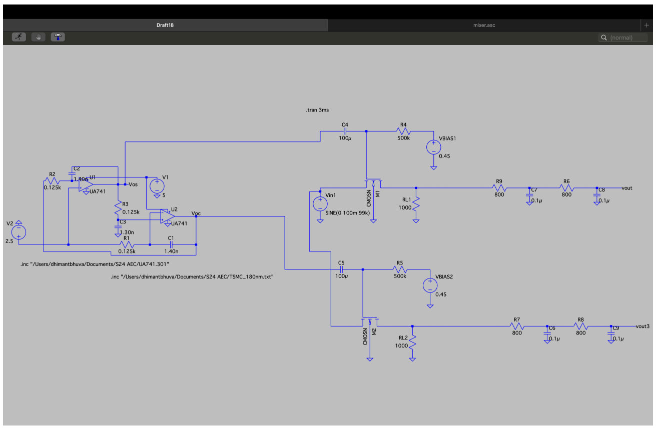

Fig 16 : Complete circuit in LTSpice

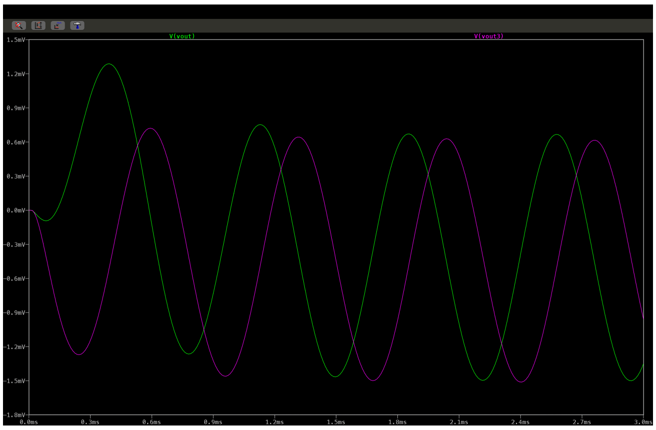

Fig 17 : Complete circuit's simulation

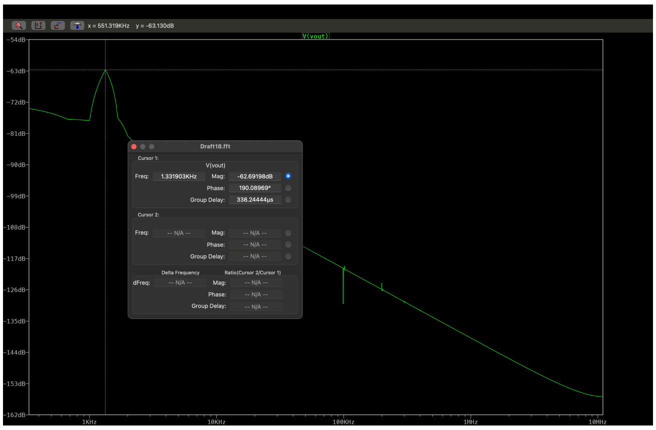

Fig 18 : I_{FINAL} FFT

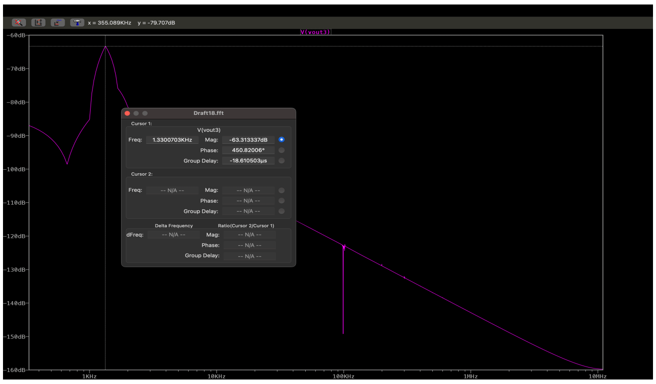

Fig 19 : Q_{FINAL} FFT

VI. Results

Results are obtained at f_{IN} = 99KHz.

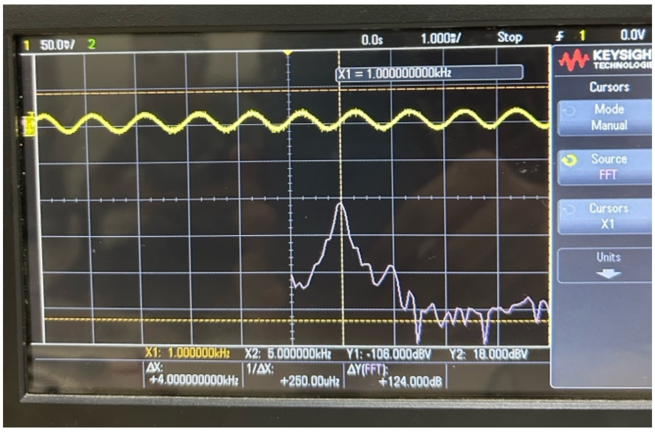

Fig20: final output I_{FINAL}

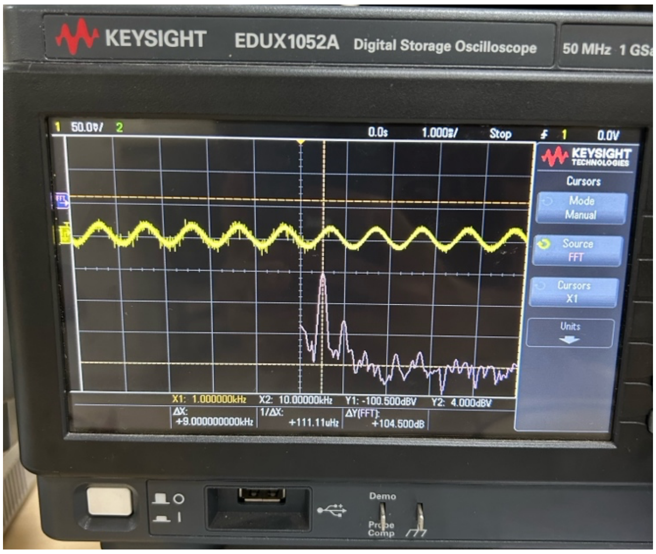

Fig21: final output Q_{FINAL}

Parameters	Simulated	Observed
Oscillator Frequency	100KHz	99.96KHz
Oscillator amplitude (I-phase)	$1V_{PP}$	$1.04V_{PP}$
Oscillator amplitude (I-phase)	$1V_{PP}$	940mV
Input frequency	99KHz	99KHz
V_{BIAS}	0.45V	0.45V
C_C	0.1µF	0.1µF
Supply	5V	7.7V

Table 1:Compairing simulations and lab realisation

Contribution

Dhimant Bhuva:

- Mixer design
- Report, Mid-eval and final-eval presentation
- Lab realization of Mixer(switch)

Jal Parikh

- Quadrature Oscillator
- Low Pass Filter design
- Lab realization of Quadrature and LPF

References

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