XR808 Datasheet

Single-Chip Wi-Fi MCU for Internet-of-Things Applications

Revision 0.1

Jul. 20, 2019

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Revision History

Version	Data	Summary of Changes
0.1	2019-7-20	Initial Version

Table 1- 1 Revision History

Contents

Tables

Figures

1 Overview

1.1 General Description

XR808 is a highly integrated low-power Wi-Fi Microcontroller System-on-Chip (SoC) solution designed for Internet of Things (IoT), Machine-to-Machine (M2M), Smart Home, Cloud Connectivity and Smart Energy applications.

The XR808 application subsystem is powered by an ARM Cortex-M4F CPU that operates up to 160MHz. It supports an integrated 256KB SRAM and 160KB ROM, a QSPI interface to SIP up to 16MB Flash. Integrated I-cache enables Execute In Place (XIP) from flash. It also includes many peripherals, including UART, TWI, SPI, PWM, and GPADC.

The Wi-Fi subsystem contains the 802.11b/g/n baseband, MAC and radio with integrated PA, LNA, Switch and harmonic filter, which is design to meet both the low power, high integration and high performance network application. a novel digital RF transmitter is design using XRADIOTECH's MPD™ technology to deliver higher output power and maintain higher efficiency, and also to keep the chip not sensitive to antenna mismatch but always have good EVM at different VSWR.

The SoC is optimized for low-power operation by using several low-power state and fast wake-up times from hardware to software. Multiple power domains and clocks can be shut down individually. The application subsystem and Wi-Fi subsystem can be put into low-power states independently, supporting a variety of application use cases. Also an optional external DC-DC regulator can provide from 1.5V to 2.5V for whole VDD_ANA power domain with on chip DC-DC control signal, without sacrifice standby power consumption even using high quiescent current DC-DC.

The SoC is designed for networked low-power embedded applications. It has an integrated network processor with a large set of TCP/IP with IPv4/IPv6 based services. These services can be accessed via a serial UART/SPI link connected to an external host CPU.

1.2 Features

- **General System Features**

Table 1- 1 XR808 Features

Chip List	Description	XR808ST	XR808CT
Package	Trays and tape-in-reel	4x4mm^2	4x4mm^2
		QFN32	QFN32
Supply voltage	Power supply from system	1.62~5.5V	
PMU	LDO for external device (EXT LDO)	Yes	
External Clock	Reference High frequency clock	24/26/40MHz	
MCU Core	Core Type	Cortex-M4F	
	Core clock maximum frequency	160MHz	160MHz
Memory	Internal ROM	160KB	
	Internal RAM	256KB	256KB

	Internal Flash		/	/
	External Flash with XIP		128Mb	
Backup register	Backup register for power save		16B	
Secure boot			Yes	
Crypto Engine	AES/DES/3DES/SHA/MD5/CRC		Yes	
TRNG	Provide random number seed		Yes	
Watchdog reset protection	Protect specified peripherals been reset by watchdog reset		Yes	
BOR	BOR Detection		Yes	
Wi-Fi	802.11 b/g/n		Yes	
Peripheral	GPIO	General Purpose	20	13
	UART		3	2
	SPI	Master and slave	1	/
	TWI	Max.400Kbps	2	/
	GPADC	VBAT	1	1
		Normal	5	/
	DMA	8Channel	1	1
	RTC	-	1	1
	Timer	Watchdog	1	1
		Normal	2	2
		Wakeup	1	1
	PWM	Output	8	8
		Input capture	8	8
	32K	Internal RCOSC	1	1
		External XTAL	1	/
	WAKEUP IO	From RTC wakeup	5	5

- **Wi-Fi Subsystem**

- IEEE 802.11b/g/n, 1x1 SISO 2.4GHz
- Integrated MAC, BB, RF and Embedded TCP/IP Stack
- Integrated T/R switch, harmonic filter, PA and LNA
- Antenna diversity
- Station, AP Modes
- Smart-Config Technology for Autonomous and Fast Wi-Fi Connections
- Security support for WEP, WPA/WPA2 personal, WPS2.0
- Industry-Standard BSD Socket Application Programming Interfaces (APIs)

- **Power Management**

- Integrate highly flexibility power management unit by several LDOs and external DC-DC controller
- Wide range power supply: 1.62-5.5V

- **Miscellaneous**

- Integrates 1Kbit eFuse to store device specific information and RF calibration data

1.3 Application

- Smart Audio
- Smart Video
- Security Systems
- Smart Energy
- Internet Gateway
- Smart Home
- Access Control
- Cloud Connectivity
- Industrial Control
- IP Network Sensor Nodes

1.4 Block Diagram

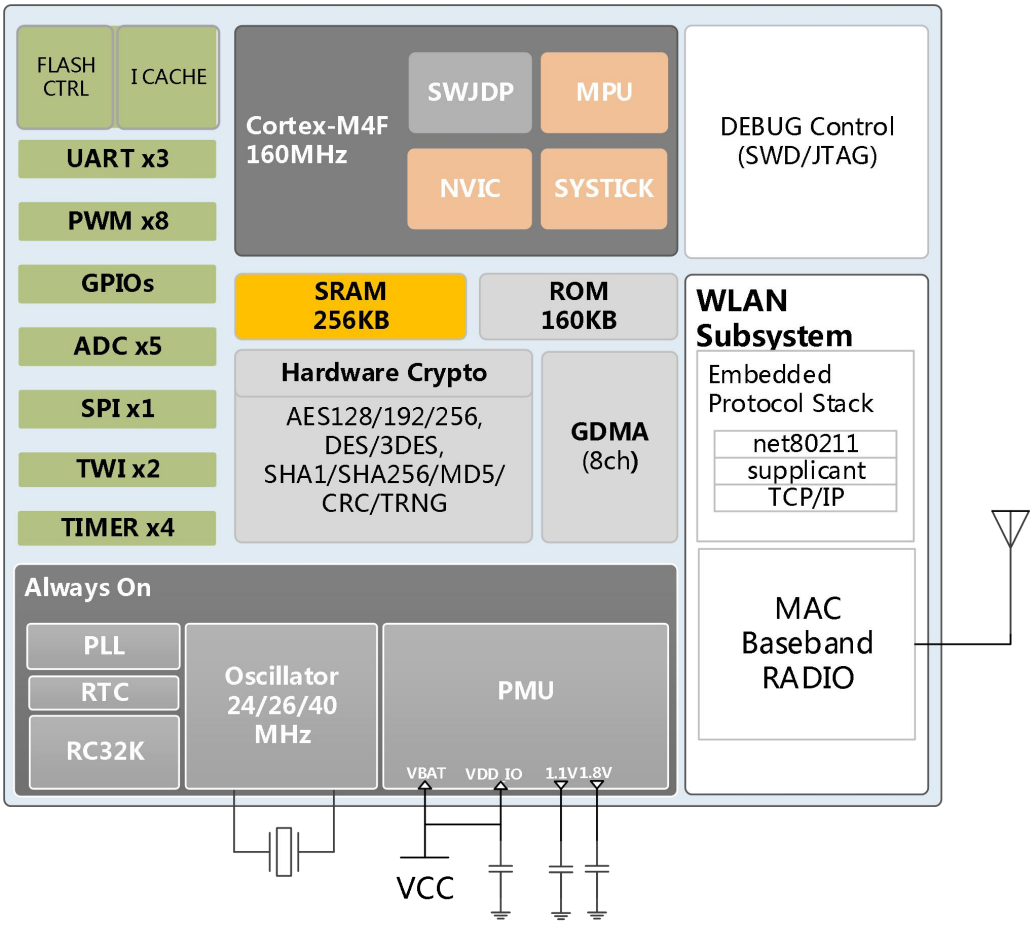


Figure 1- 1 XR808 Functional Block Diagram

2 Function Description

2.1 System Overview

2.1.1 Power Management

A single 1.62~5.5V power supply is required for the XR808. It could be from an AC-DC converter, USB to supply to 5V or a DC-DC converter to convert higher voltage supply to 3.3V or even lower. It could be from a battery directly too, no matter it is lithium, single 3V button or 2 serial NI-MH battery.

The Power Management Unit (PMU) contains a DC-DC control interface, several Low Drop-out Regulators (LDOs), and a reference band-gap circuit. The circuits are optimized for low quiescent current, low drop-out voltage, load regulation, high ripple rejection, and low output noise. The PMU integrates several LDOs for different circuits: TOP LDO, RTC LDO, SoC LDO, EXT LDO, as shown in Figure 2-1. They have different operating conditions and features:

- **TOP LDO** provide programmable voltage from 1.4V to 3.6V with maximum 350mA load current, for Analog and PSRAM, also SoC LDO input. Normally, make sure VBAT voltage is higher than this programmable output voltage setting.
- **RTC LDO** is the main supply only for RTC domain to optimize power consumption at HIBERNATION state.
- **SoC LDO** is the main supply for whole chip digital circuit with programmable voltage from 0.6V to 1.35V to let DVFS operate effectively.
- **EXT LDO** is main power supply for external device in application, and also can be provide to VDDIO, GPADC and CODEC. It has maximum 200mA load current. The output voltage is limited to 3.3/3.1V (by register configure setting), when VBAT is lower than the value, it will automatically switch to bypass mode to let output voltage follow VBAT.

When using external DC-DC to further reduce power, the connection can be set as figure 2-1. PA23 GPIO pin is specified for external DC-DC pup, the detail software setting and flow is integrated in to our SDK. When external DC-DC is used, the output voltage on VDD18 should be at least 0.1V step higher than TOP LDO setting voltage to have DC-DC be operating normally.

There are four power domains in the system: RTC domain, OA domain, Digital Core domain and Wi-Fi domain. They mainly used for different scenario to maintain ultra-low power application. We define XR808 into **ACTIVE, STANDBY, HIBERNATION** and **SHUTDOWN** power management states, is shown in table 2-1.

Table 2- 1 Power Management States

POWER MODE	CM4F	Wi-Fi	EXT LDO	RTC LDO	TOP LDO	SoC LDO	DCXO /DPLL	Description
ACTIVE	ACTIVE	ACTIVE	ON	ON	ON	ON	ON	All CPU active
	ACTIVE	OFF	ON	ON	ON	ON	ON/OFF	APP CPU active
STANDBY	SLEEP	ACTIVE	ON	ON	ON	ON	ON	APP CPU goes to sleep, Wi-Fi DTIMx state

	SLEEP	SLEEP	ON	ON	LP	LP	OFF	
	SLEEP	OFF	ON	ON	LP	LP	OFF	APP CPU goes to sleep, Wi-Fi power off
HIBERNATE	OFF	OFF	ON/OFF	ON	OFF/LP	OFF	OFF	Only RTC on, waiting for timer or wakeup IO to interrupt
SHUTDOWN	OFF	OFF	OFF	OFF	OFF	OFF	OFF	CHIP_PWD pin keep low level

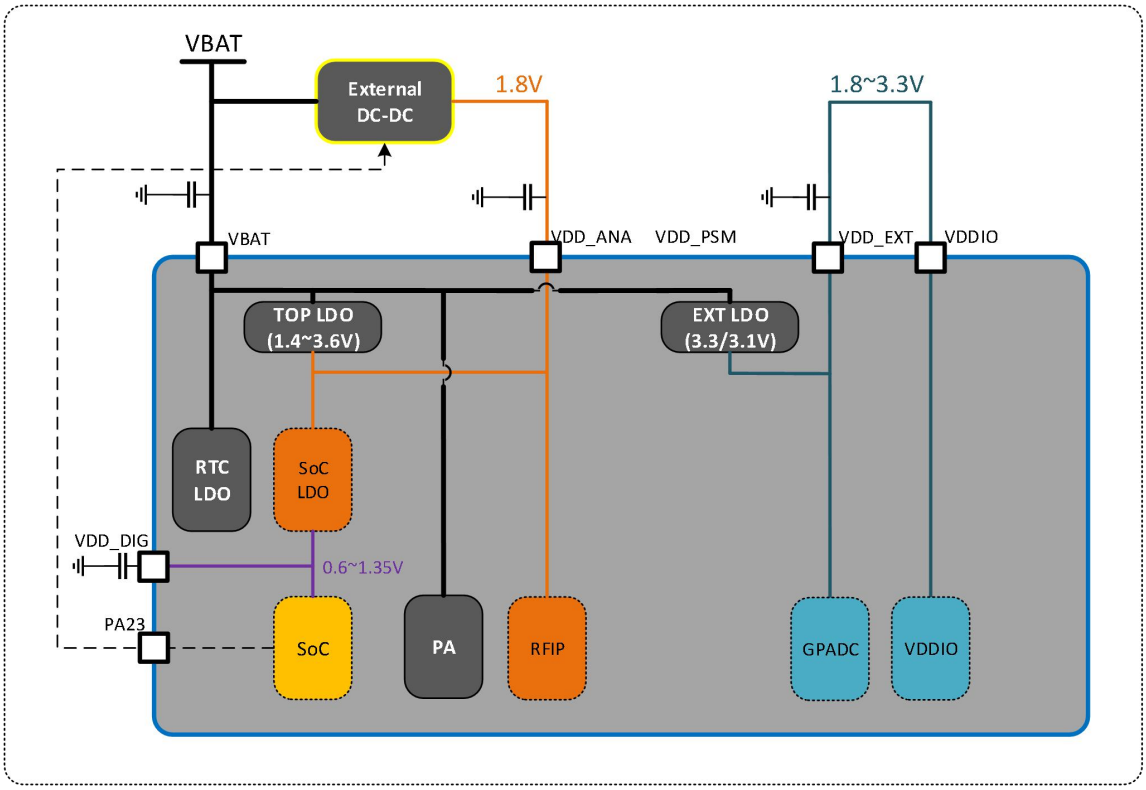


Figure 2- 1 Power Architecture

2.1.2 Clock

The clock management system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based up a module's individual requirements. The system depends on, and generates two different clocks: a high frequency clock *HFCLK* and a low frequency clock *LFCLK.*

The system supports two LFCLK clock sources, the 32.768 KHz crystal oscillator and the 32.768 KHz RC oscillator. The 32.768 KHz crystal oscillator requires an external AT-cut quartz crystal to be connected to the LXTAL1 and LXTAL2 pins. The LFCLK clock and all of the available LFCLK sources are switched off by default when the system is powered up. The LFCLK clock can be started by selecting the preferred clock source in PRCM register. It is used for each subsystem to achieve lower current consumption for different running mode. In addition, the LFCLK is also used in RTC circuit to achieve accuracy timing.

There is only one clock source for HFCLK, the 24MHz, 26Mhz, 40MHz crystal oscillator. The HFCLK is enabled automatically when the system is powered up and can be switched off when all subsystems won't use it anymore

in some low power modes.

The HFCLK is used to generate the clock source for Digital PLL, which is used to generate the clock sources for Cortex-M4F core, Wi-Fi and peripherals. There is also an Audio PLL used to generate the clock source for Audio Subsystem.

The following figure shows the clock control block diagram.

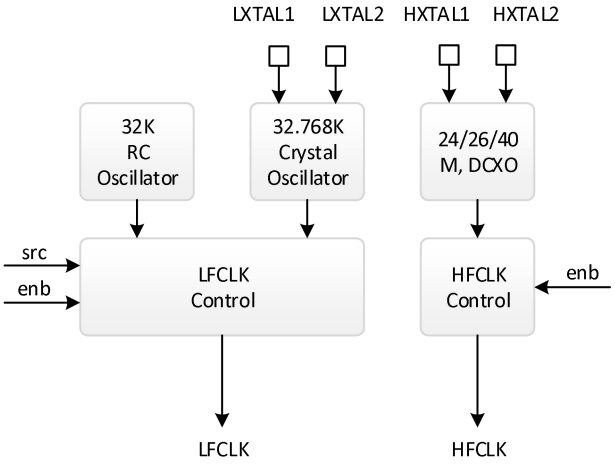


Figure 2- 2 Clock Control

2.1.3 Power State and Power Sequence

2.1.3.1Power-on Sequences

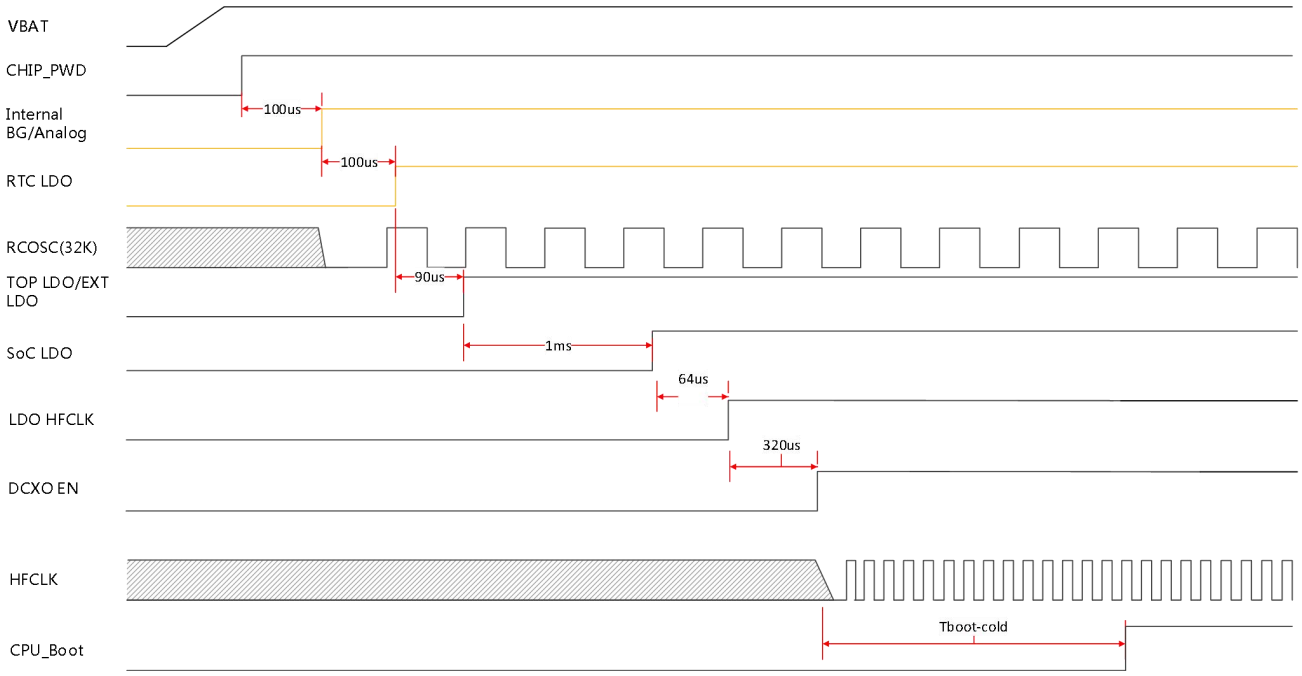
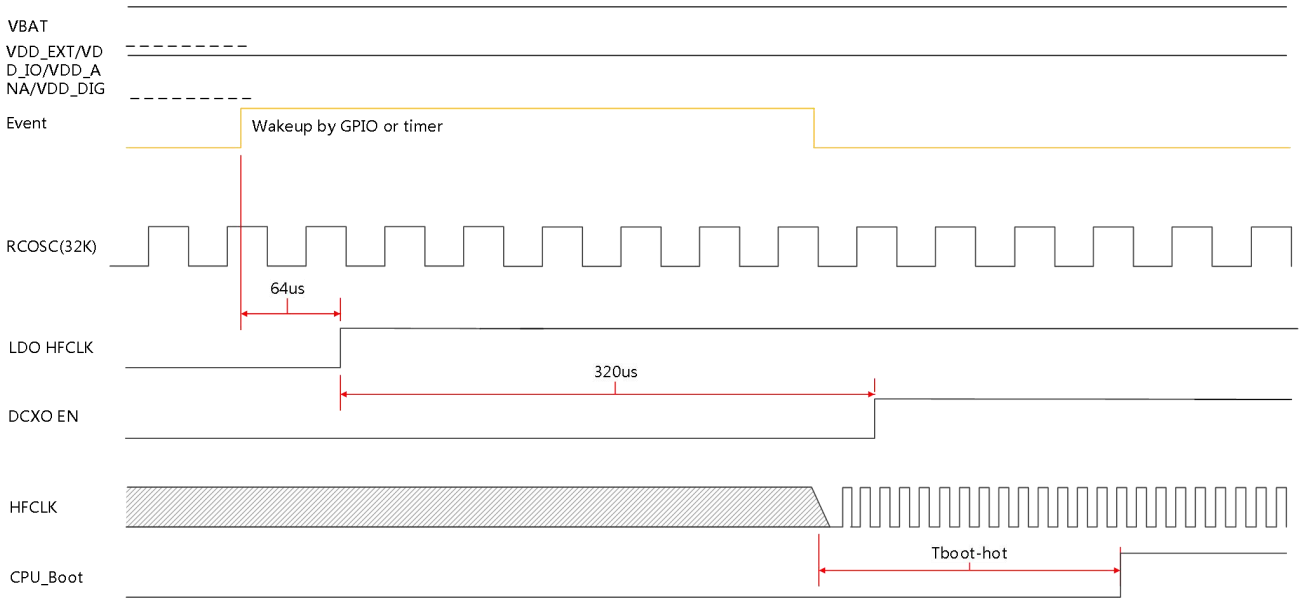
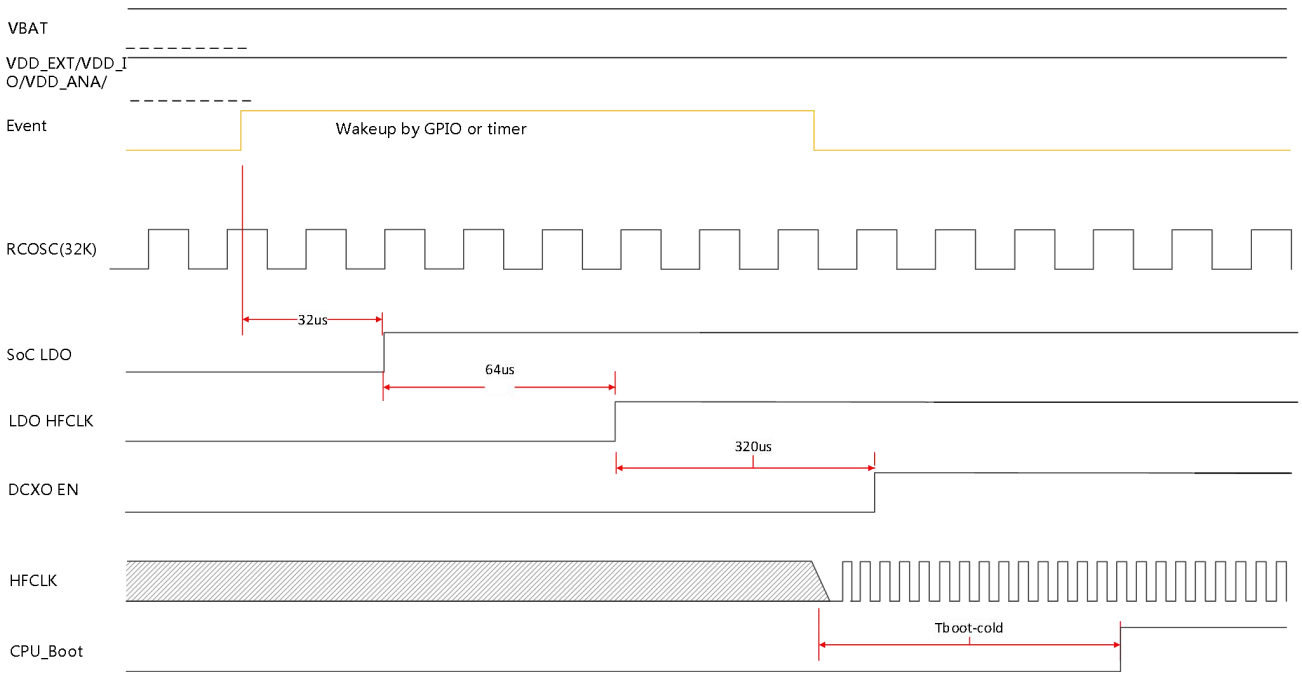


Figure 2- 3 Power-on Sequence

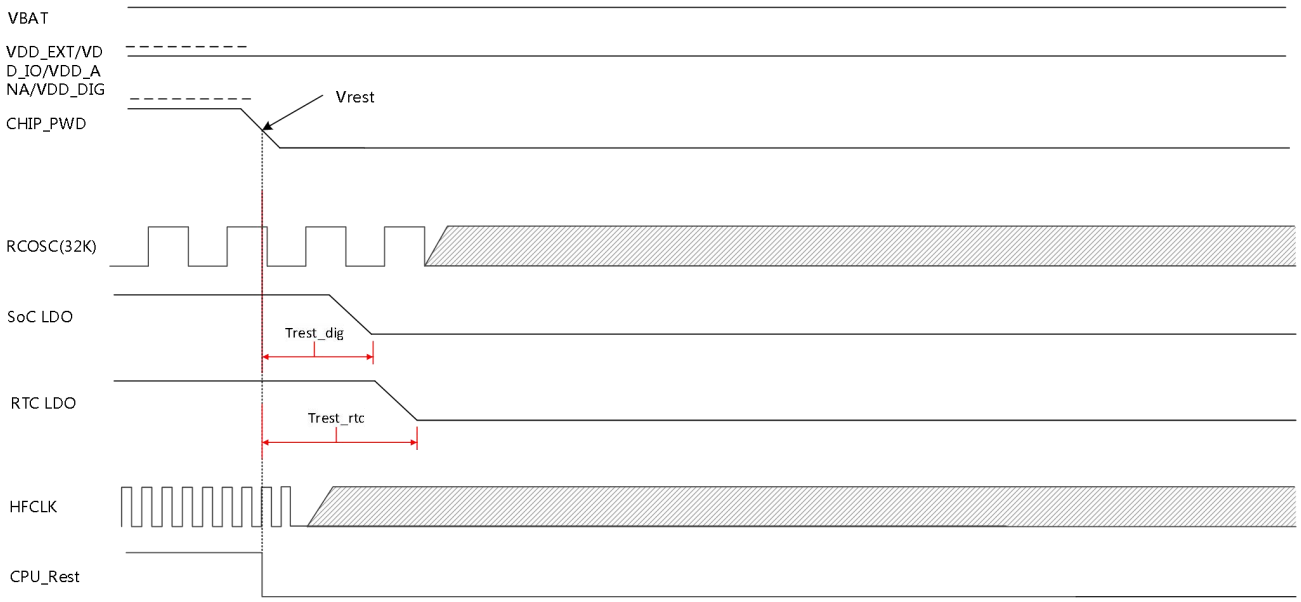
2.1.3.2Wakeup from Standby



2.1.3.3 Wakeup from Hibernation



2.1.3.4 Shutdown Sequence



2.1.4 Memory Mapping

TBD

Figure 2- 4 Memory Mapping

Table 2- 2 SRAM Memory Mapping

RAM Region	SIZE	AR400A Address
BROM	32KB	0x00000000 – 0x00007FFF
ROM	128KB	0x00008000 – 0x00027FFF
SRAMA0	256KB	0x00200000 – 0x0023FFFF
FLASH ROM	16MB	0x00400000 – 0x013FFFFF

2.1.5 CPU

XR808 features an ARM Cortex-M4F processor, which is the most energy efficient ARM processor available. It supports the clock rates from 32KHz up to 160MHz. The processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption.

The ARM Cortex-M4 core has low-latency interrupt processing with the following features:

- Thump-2 instruction set for optimal performance and code size
- Handler and thread modes
- Memory Protection Unit (MPU) for memory protection features
- Floating Point Unit (FPU) to support DSP related function
- Nested Vectored Interrupt Controller (NVIC) to achieve low latency interrupt processing
- Three Advanced High-Performance bus AHB-Lite interfaces: ICode, DCode and system bus
- Bit-band support for memory and select peripheral that include atomic bit-band write and read operations
- Wake-up Interrupt Controller (WIC) providing ultra-low power sleep mode support

2.1.6 DMA

There are 8 AHB DMA channels for this DMA controller. Only one channel can be active and the sequence is according to the priority level.

The DMA controller can support 8-bit/16-bit/32-bit data width. The data width of Source and Destination can be different, but the address should be aligned. Although the increase mode of NDMA should be address aligned, but its byte counter should not be multiple. The DMA Source Address, Destination Address, Byte Counter Registers can be modified even if the DMA is started.

2.1.7 Crypto Engine

The Crypto Engine (CE) is one encrypt/decrypt algorithms accelerator. It is suitable for a variety of applications.

Features:

- Supports AES, DES, 3DES, SHA-1, MD5, CRC32/16, SHA256, TRNG
- Supports ECB, CBC, CTR modes for AES/DES/3DES
- Supports 128-bits, 192-bits and 256-bit key size for AES
- Supports 160-bits hardware PRNG with 192-bits seed

The TRNG generates random numbers from the 8 free-run ring oscillators (RCO). IRQ will be issued once the random data is successfully generated.

2.1.8 Timer

Timer 0 and 1 can take their inputs from internal RC oscillator, external 32768Hz crystal or OSC. They provide the operating system's scheduler interrupt. It is designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 24-bit programmable overflow counter and work in auto-reload mode or no-reload mode.

The watch-dog is used to resume the controller operation when it had been disturbed by malfunctions such as noise and system errors. It features a down counter that allows a watchdog period of up to 16 seconds. It can generate a general reset or an interrupt request.

2.1.9 RTC

The real time clock (RTC) is for calendar usage. It is built around a 30-bit counter and used to count elapsed time in YY-MM-DD and HH-MM-SS. The unit can be operated by the backup battery while the system power is off. It has a built-in leap year generator.

The alarm generates an alarm signal at a specified time in the power-off mode or normal operation mode. In normal operation mode, both the alarm interrupt and the power management wakeup are activated. In power-off mode, the power management wakeup signal is activated. In this section, there are two kinds of alarm. Alarm 0 is a general alarm; its counter is based on second. Alarm 1 is a weekly alarm; its counter is based on the real time.

2.2 Peripherals

2.2.1 GPIO

The XR808 GPIO unit provides as many as 31 GPIO (General Purpose IO) pins. All ports are brought out of the device using alternate function multiplexing. The GPIO function can be multiplexed on a multi-function I/O pin by

selecting the GPIO alternate function in the GPIO Controller registers.

There are two types of GPIO designs in XR808: GPIO and AGPIO. Each GPIO can be configured with the following options:

- Input / Output / Floating(Hi-Z) mode
- Input mode: Pull-up or Pull-down
- Output mode: Active driving
- Pull-up/down control: the pull-up and pull-down resistance is 90KΩ with ±30% variation over PVT condition
- External Interrupt IO with 5 trigger modes: high-level, low-level, rising edge, falling edge, double edge
- 5 WAKEUP IOs can be set to wake system by external interrupt at HIBERNATION mode (RTC on only)
- All IOs can be set to wake system by external interrupt at STANDBY mode (RTC and OA domain on)

The digital IO AGPIO function is equivalent to GPIO as shown above. A dedicated internal control signal is used to select between the digital and analog functions. These IOs are multiplexed with 8 channels ADC (1 is internal connected to measure VBAT voltage).

GPIO PA23 has a special function which is used to enter test mode when it is high on first power-up. So we need to keep it without pull high (floating or tie low) to have whole chip power up correctly.

Table 2- 3 XR808ST GPIO Multiplexing

GPIO	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
PA00			TWI1_SCL		EINTA0
PA01			TWI1_SDA		EINTA1
PA10	ADC_CH0	PWM2/ECT2			EINTA10
PA11	ADC_CH1	PWM3/ECT3			EINTA11
PA12	ADC_CH2	PWM4/ECT4			EINTA12
PA13	ADC_CH3	PWM5/ECT5		UART1_TX	EINTA13
PA14	ADC_CH4	PWM6/ECT6		UART1_RX	EINTA14
PA19/WUPIO5	UART2_RTS	TWI0_SCL	PWM0/ECT0	SPI1_MOSI	EINTA19
PA20/WUPIO6	UART2_CTS	TWI0_SDA	PWM1/ECT1	SPI1_MISO	EINTA20
PA21/WUPIO7	UART2_RX		PWM2/ECT2	SPI1_CLK	EINTA21
PA22/WUPIO8	UART2_TX		PWM3/ECT3	SPI1_CS0	EINTA22
PA23/WUPIO9/TEST	EXT_DCDC_PUP				EINTA23
PB00	UART0_TX	JTAG_TMS	PWM4/ECT4	SWD_TMS	EINTB0
PB01	UART0_RX	JTAG_TCK	PWM5/ECT5	SWD_TCK	EINTB1
PB02	SWD_TMS	JTAG_TD0	PWM6/ECT6		EINTB2
PB03	SWD_TCK	JTAG_TDI	PWM7/ECT7		EINTB3
PB04			UART1_TX	FLASH_MOSI/IO0	EINTB4
PB05			UART1_RX	FLASH_MISO/IO1	EINTB5

PB06			UART1_CTS	FLASH_CS	EINTB6
PB07			UART1_RTS	FLASH_CLK	EINTB7

Table 2- 4 XR808CT GPIO Multiplexing

GPIO	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
PA19/WUPIO5	UART2_RTS		PWM0/ECT0		EINTA19
PA20/WUPIO6	UART2_CTS		PWM1/ECT1		EINTA20
PA21/WUPIO7	UART2_RX		PWM2/ECT2		EINTA21
PA22/WUPIO8	UART2_TX		PWM3/ECT3		EINTA22
PA23/WUPIO9/TEST	EXT_DCDC_PUP				EINTA23
PB00	UART0_TX	JTAG_TMS	PWM4/ECT4	SWD_TMS	EINTB0
PB01	UART0_RX	JTAG_TCK	PWM5/ECT5	SWD_TCK	EINTB1
PB02	SWD_TMS	JTAG_TD0	PWM6/ECT6		EINTB2
PB03	SWD_TCK	JTAG_TDI	PWM7/ECT7		EINTB3
PB04				FLASH_MOSI/IO0	EINTB4
PB05				FLASH_MISO/IO1	EINTB5
PB06				FLASH_CS	EINTB6
PB07				FLASH_CLK	EINTB7

2.2.2 UART

The XR808 provides 3 UART controllers: one is used for debug and two with auto-flow control are used for communication with external devices. The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

Features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- Support DMA controller interface
- Support Software/ Hardware Flow Control
- Support IrDA 1.0 SIR
- Support RS-485 mode
- Support configurable baud rate from 9600, 19200, 38400, 115200 and 921600 etc.
- Support baud rate detection

2.2.3 SPI

The XR808 features two SPI controllers. Each controller can be configured to a SPI master or a SPI slave. They are used as an extension interface to control the peripheral devices. They support two options of clock polarity (CPOL) and two options of initial clock phase (CPHA).

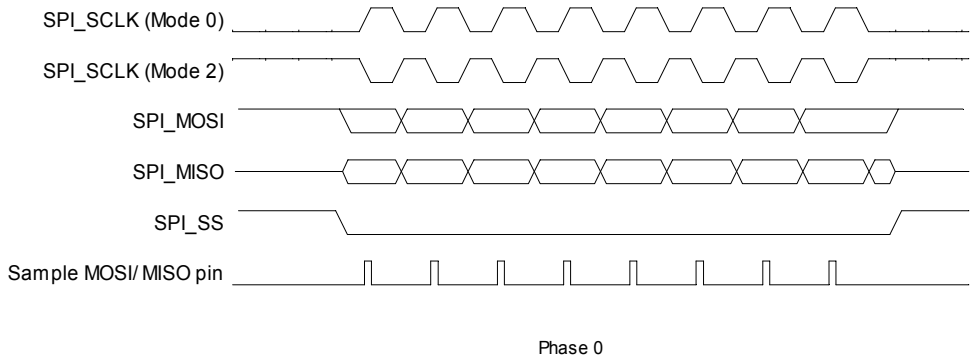


Figure 2- 5 SPI Phase 0 Transfer Format

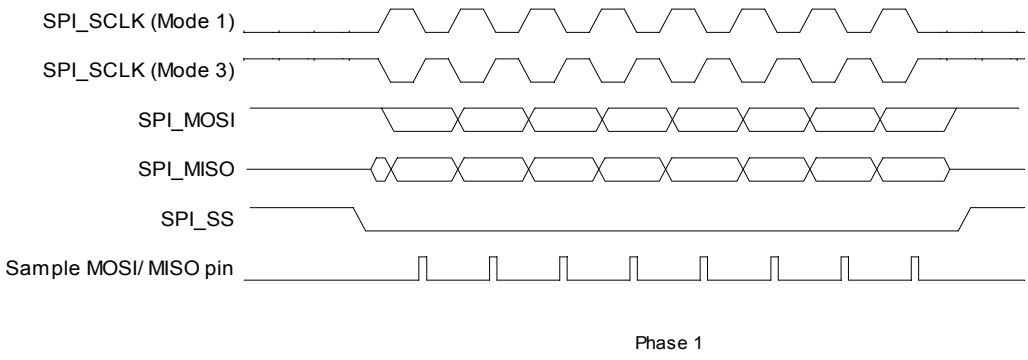


Figure 2- 6 SPI Phase 1 Transfer Format

2.2.4 TWI

The XR808 features two TWI serial interfaces. They can be configured as master and salve mode. Each TWI controller supports three IO mapping. The TWI controllers can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400K bps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

Features:

- Compatible with IIC protocol and SCCB protocol
- Software-programmable for Slave or Master
- Supports Repeated START signal

- Multi-master systems supported
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speeds up to 400Kbits/s (‘fast mode’)
- Allows operation from a wide range of input clock frequencies

2.2.5 PWM

XR808 features 8 PWMs to generate pulse sequences with programmable frequency a duration for LCD, vibrators and other devices. The PWM controller provides 8 PWM channels, which are divided into four pairs of PWM pair, each is composed of three parts: a clock controller, two timer modules, a programmable dead-zone generator. The PWM channel logic can be configured as input capture function. The capturer detects the rising edge and the falling edge of the signal and calculates the high-level and the low-level duration with a 16-bit counter.

Features:

- 8 PWM channels, divided into 4 PWM pairs
- Supports pulse, period and complementary pair outputs
- Support input capture
- Programmable dead-zone generator
- Configurable output frequency, 0%-100% duty adjustable

2.2.6 GPADC

XR808 features one GPADC function. The ADC function contains a 6-channel analog switch, a single end input asynchronous 12-bit SAR (Successive Approximation Register) ADC. The channels 0 to 4 are used to detect the voltage of the external input and the channel 8 is dedicated to detect the voltage of the VBAT.

Features:

- 12-bit Resolution and 10-bit effective SAR type A/D converter
- 6-channel multiplexer, 5 normal channel and 1 VBAT voltage detection channel
- 64 FIFO depth of data register
- DMA support
- Power supply 1.62~3.6V，internal Capless LDO provide 1.4V/2.5V/0.4*VDD-EXT to Vref

- Maximum Sampling frequency: 1 MHz
- Support self-calibration
- Support data compare and interrupt
- Support four operation mode: Single conversion mode, Single-cycle conversion mode, Continuous conversion mode, Outbreak conversion mode

2.3 Wi-Fi Subsystem

2.3.1 Wi-Fi MAC

Supports MAC enhancements including:

- 802.11d - Regulatory domain operation
- 802.11e - QoS including WMM
- 802.11h - Transmit power control dynamic and frequency selection
- 802.11i - Security including WPA2 compliance
- 802.11r - Roaming

2.3.2 Wi-Fi Baseband

Features:

- Compatible with IEEE 802.11 b/g/n standard
- 802.11n MCS0-7 with data rate up to 72.2Mbps (BPSK, r=1/2 through 64QAM, r=5/6)
- 6M~54M data rate for 802.11g
- DSSS, CCK modulation with long and short preamble
- Short Guard Interval
- Long Guard Interval
- RX antenna Diversity

2.3.3 Wi-Fi Radio

Features:

- Integrated 2.4GHz PA, LNA, and T/R switch
- Internal impedance matching network and harmonic filter allow chip to connect to antenna directly

- High Power Amplifier with 1.8~5.5V full range directly support XRADIOTECH's MPD™ technology ensure linearity tracking automatically to always keep EVM and mask within specifications
- Special Architecture and Device design to keep the reliability of PA up to 5.5V high voltage and also deliver high output power (>25dBm)

3 Electrical Characteristics

3.1 Absolute Maximum Rating

Table 3- 1 Absolute Maximum Rating

Symbol	Parameter	Maximum rating	Unit
I/O	In/Out current for input and output	-35 to 35	mA
VBAT	1.62-5.5V Power supply	-0.3 to 6	V
CHIP_PWD	RESET pin for chip	-0.3 to 6	V
VDD_ANA	Power supply	-0.3 to 3	V
VDD_DIG	Power supply	-0.3 to 1.5	V
VDD_EXT	Power supply	-0.3 to 4	V
VDD_IO	Power supply	-0.3 to 4	V
T_{opr}	Operating Temperature	-40 to 105	°C
$T_{junction}$	Junction Temperature	-40 to 125	°C
T_{stg}	Storage Temperature	-55 to 125	°C
VESD	HBM	±2000	V
VESD	CDM	±500	V

3.2 Recommended Operating Conditions

Table 3- 2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{opr}	Ambient Operating Temperature	-40	-	105	°C
VBAT	Power supply of chip input	1.62	1.8/3.6/5	5.5	V
CHIP_PWD	RESET	1.62	-	5.5	V
VDD_ANA	Power supply of analog/RF input	1.4	1.8	2.5	V
VDD_DIG	Power supply of digital input	0.6	1.1	1.35	V
VDD_EXT	Power supply of external device output	1.62	3.3	3.5	V
VDD_IO	Power supply of GPIO input	1.62	1.8/3.3	3.6	V

3.3 Digital IO Characteristics

Table 3- 3 DC Characteristics of VDD_IO=3.3V

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input Low Voltage	VDD_IO=3.3V	-0.3	1.32	V
V_{IH}	Input High Voltage	VDD_IO=3.3V	2.06	3.6	V
V_{OL}	Output Low Voltage	|IOL| = 7.5~50 mA	-0.3	0.4	V
V_{OH}	Output High Voltage	|IOH| = 7.5~50 mA	2.9	3.6	V

R_{PU}	Input Pull-up Resistance	PU=high, PD=low	35	95	KΩ
R_{PD}	Input Pull-down Resistance	PU=high, PD=low	35	95	KΩ

Table 3- 4 DC Characteristics of VDD_IO=1.8V

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input Low Voltage	VDD_IO=1.8V	-0.3	0.6	V
V_{IH}	Input High Voltage	VDD_IO=1.8V	1.18	1.98	V
V_{OL}	Output Low Voltage	|IOL| = 2.25~15 mA	-0.3	0.4	V
V_{OH}	Output High Voltage	|IOH| = 2.25~15 mA	1.44	2.0	V
R_{PU}	Input Pull-up Resistance	PU=high, PD=low	63	190	KΩ
R_{PD}	Input Pull-down Resistance	PU=high, PD=low	63	190	KΩ

3.4 Bootstrap Modes and Pins

Table 3- 5 Bootstrap pins

Symbol	Bootstrap Function Name	Value	Description
PA23	Test Mode	0	Normal operation mode
		1	Enter into test/debug mode when releasing CHIP_PWD
PB02, PB03	Boot Mode	00	when releasing CHIP_PWD will cause the system going to firmware update mode.
		01	Internal normal boot
		10	
		11	

3.5 High Frequency Reference Clock

XR808 must use high frequency reference clock, it can use an external high frequency crystal and a built-in oscillator.

Table 3- 6 External High Frequency Crystal Characteristics Requirements

Parameter	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		-	24,26,40	-	MHz
ESR		-	-	60	Ohm
C_{in_xtal}(1)	Single-ended	0	-	25.4	pF
C_{shunt}(1)		-	2	-	pf

Load Capacitance(1)		-	0	27	pF
Crystal Frequency Accuracy at Nominal Temp.	25 °C	-10	-	+10	ppm
Crystal Drift Due to Temperature	-20 to +85 °C	-10	-	+10	ppm
Crystal Pull Ability		10	-	150	ppm/pF

(1) The load capacitance value (C_{load}) and shunt capacitance depends on XTAL model, XTAL1 and XTAL2 pin have inside capacitance (C_{in_xtal}), so external added load capacitance value(PCB Welding Capacitance) C_{load_ext}= C_{load} * 2 - C_{in_xtal} l - C_{pcb}-C_{shunt}*2, C_{pcb} is PCB parasitic capacitance(Single ended) . C_{in_xtal} has tuning range about 25.4pF, which is controlled by software, for details please go to software user manual.

3.6 Low Frequency Reference Clock

XR808 use low frequency reference clock, it can either use an external low frequency crystal and a built-in oscillator, or internal RCOSC. The external crystal and a built-in oscillator is used during power save modes.

External Low Reference Clock Source

Table 3-7 External Low Frequency Crystal Characteristics Requirements

Parameter	Conditions	Min.	Typ.	Max.	Unit
Nominal Frequency		-	32.768	-	KHz
Load Capacitance(1)		-	12.5	-	pF
C_{shunt}(1)		-	2	-	pf

(1) The load capacitance value (Cload) and shunt capacitance depends on LXTAL model, external added load capacitance value(PCB Welding Capacitance) C_{load_ext} = C_{load} * 2 - C_{pcb} - C_{shunt} * 2, C_{pcb} is PCB parasitic capacitance(Single ended) .

Internal RCOSC Reference Clock Source

XR808 have an integrated RC oscillator low frequency reference clock source inside. RCOSC takes effect when there is no external crystal.

3.7 Wi-Fi 2.4G RF Receiver Specifications

Table 3- 8 RF Receiver Specifications

Condition: VBAT=3.6V, VDD_ANA=1.8V, XTAL=40MHz, Temperature=25°C

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412		2484	MHz
RX Sensitivity (802.11b)	1Mbps DSSS		TBD		dBm

	2Mbps DSSS		TBD		dBm
	5.5Mbps CCK		TBD		dBm
	11Mbps CCK		TBD		dBm
RX Sensitivity (802.11g)	6Mbps OFDM		TBD		dBm
	9Mbps OFDM		TBD		dBm
	12Mbps OFDM		TBD		dBm
	18Mbps OFDM		TBD		dBm
	24Mbps OFDM		TBD		dBm
	36Mbps OFDM		TBD		dBm
	48Mbps OFDM		TBD		dBm
	54Mbps OFDM		TBD		dBm
RX Sensitivity (802.11n, 20MHz)	MCS 0		TBD		dBm
	MCS 1		TBD		dBm
	MCS 2		TBD		dBm
	MCS 3		TBD		dBm
	MCS 4		TBD		dBm
	MCS 5		TBD		dBm
	MCS 6		TBD		dBm
	MCS 7		TBD		dBm
Maximum Receive Level	6 Mbps OFDM		TBD		dBm
	54 Mbps OFDM		TBD		dBm
	MCS0		TBD		dBm
	MCS7		TBD		dBm
Receive Adjacent Channel Rejection	1 Mbps CCK		TBD		dBc
	11 Mbps CCK		TBD		dBc
	BPSK rate 1/2, 6 Mbps OFDM		TBD		dBc
	64QAM rate 3/4, 54 Mbps OFDM		TBD		dBc
	HT20, MCS 0, BPSK rate 1/2		TBD		dBc
	HT20, MCS 7, 64QAM rate 5/6		TBD		dBc

3.8 Wi-Fi 2.4G RF Transmitter Specifications

Table 3- 9 RF Transmitter Specifications 1

Condition1: VBAT=3.6V, VDD_ANA=1.8V, XTAL=40MHz, Temperature=25°C

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412		2484	MHz
TX Power[1]	1Mbps DSSS mask compliant		TBD		dBm
	11Mbps CCK mask compliant		TBD		dBm
	6Mbps OFDM mask compliant		TBD		dBm
	54Mbps OFDM EVM compliant		TBD		dBm

	HT20, MCS 0 mask compliant		TBD		dBm
	HT20, MCS 7 EVM compliant		TBD		dBm
EVM	1Mbps DSSS 16dBm		TBD		dB
	11Mbps CCK 16dBm		TBD		dB
	6Mbps OFDM 15dBm		TBD		dB
	54Mbps OFDM EVM 15dBm		TBD		dB
	HT20, MCS 0 mask 15dBm		TBD		dB
	HT20, MCS 7 EVM 14dBm		TBD		dB
Carrier Suppression				-30	dBc
Accuracy of Power Control	Closed-loop control across all temperature ranges and channels	-1.5		1.5	dB
Harmonic Output Power	2nd Harmonic			-40	dBm/MHz
	3rd Harmonic			-45	dBm/MHz

1. Refer to IEEE 802.11 specification for Tx spectrum limits:

- 802.11b mask (18.4.7.3)

- 802.11g mask (19.5.4)

- 802.11g EVM (17.3.9.6.3)

- 802.11n HT20 mask (20.3.21.1)

- 802.11n HT20 EVM (20.3.21.7.3)

2. Use N9020A, Channel Estimation: Seq

Table 3- 10 RF Transmitter Specifications 2

Condition2: VBAT=5.0V, VDD_ANA=1.8V, XTAL=40MHz, Temperature=25°C

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412		2484	MHz
TX Power[1]	1Mbps DSSS mask compliant		TBD		dBm
	11Mbps CCK mask compliant		TBD		dBm
	6Mbps OFDM mask compliant		TBD		dBm
	54Mbps OFDM EVM compliant		TBD		dBm
	HT20, MCS 0 mask compliant		TBD		dBm
	HT20, MCS 7 EVM compliant		TBD		dBm
EVM	1Mbps DSSS 16dBm		TBD		dBm
	11Mbps CCK 16dBm		TBD		dBm
	6Mbps OFDM 15dBm		TBD		dBm
	54Mbps OFDM EVM 15dBm		TBD		dBm
	HT20, MCS 0 mask 15dBm		TBD		dBm
	HT20, MCS 7 EVM 14dBm		TBD		dBm
Carrier Suppression				-30	dBc

Accuracy of Power Control	Closed-loop control across all temperature ranges and channels	-1.5		1.5	dB
Harmonic Output Power	2nd Harmonic			-40	dBm/MHz
	3rd Harmonic			-45	dBm/MHz

Table 3- 11 RF Transmitter Specifications 3

Condition3: VBAT=1.8V, VDD_ANA=1.5V, XTAL=40MHz, Temperature=25°C

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412		2484	MHz
TX Power[1]	1Mbps DSSS mask compliant		TBD		dBm
	11Mbps CCK mask compliant		TBD		dBm
	6Mbps OFDM mask compliant		TBD		dBm
	54Mbps OFDM EVM compliant		TBD		dBm
	HT20, MCS 0 mask compliant		TBD		dBm
	HT20, MCS 7 EVM compliant		TBD		dBm
EVM	1Mbps DSSS 16dBm		TBD		dBm
	11Mbps CCK 16dBm		TBD		dBm
	6Mbps OFDM 15dBm		TBD		dBm
	54Mbps OFDM EVM 15dBm		TBD		dBm
	HT20, MCS 0 mask 15dBm		TBD		dBm
	HT20, MCS 7 EVM 14dBm		TBD		dBm
Carrier Suppression				-30	dBc
Accuracy of Power Control	Closed-loop control across all temperature ranges and channels	-1.5		1.5	dB
Harmonic Output Power	2nd Harmonic			-40	dBm/MHz
	3rd Harmonic			-45	dBm/MHz

3.9 Power Consumptions

Table 3- 12 Power Consumption 1

Temp=25°C, VBAT=3.6V, VDD_ANA=1.8V, external DC-DC 90% efficiency, MCU 160MHz

Power Mode	MCU State	Wi-Fi State	TX/RX	Test Condition		Current Consumption			Unit
						Min.	Typ.	Max.	
ACTIVE	ACTIVE	Active	TX[1]	1M DSSS	19dBm		TBD		mA
				11M CCK	19dBm		TBD		mA
				6M OFDM	15dBm		TBD		mA
				54M OFDM	15dBm		TBD		mA

				HT20, MCS0	15dBm		TBD		mA
				HT20, MCS7	14dBm		TBD		mA
			RX	1M DSSS	-		TBD		mA
				11M CCK	-		TBD		mA
				54M OFDM	-		TBD		mA
				HT20, MCS0	-		TBD		mA
				HT20, MCS7	-		TBD		mA
STANDBY	SLEEP	Active	TX[1]	1M DSSS, null frame	19dBm		TBD		mA
			RX	RX listen	-		TBD		mA
				1M DSSS	-		TBD		mA
		PS Mode[2]	RX	DTIM1	-		TBD		uA
				DTIM3	-		TBD		uA
				DTIM8	-		TBD		uA
				DTIM10	-		TBD		uA
		OFF	-	-	-		TBD		uA
HIBERNATION[3]	OFF	OFF	-	-	-		TBD		uA
SHUTDOWN[4]	OFF	OFF	-	-	-		TBD		uA

1. Data is captured at TX continues mode on the duration of transmitting;

2. Use XR808 by external 32K XTAL, Beacon length 1ms;

3. RTC and wake up timer on only;

4. CHIP_PWD keeps at low level;

Table 3- 13 Power Consumption 2

Temp=25°C, VBAT=3.6V, VDD_ANA=1.8V, Internal TOP LDO supply, MCU 160MHz

Power Mode	MCU State	Wi-Fi State	TX/RX	Test Condition		Current Consumption			Unit
						Min.	Typ.	Max.	
ACTIVE	ACTIVE	Active	TX[1]	1M DSSS	19dBm		TBD		mA
				11M CCK	19dBm		TBD		mA
				6M OFDM	15dBm		TBD		mA
				54M OFDM	15dBm		TBD		mA
				HT20, MCS0	15dBm		TBD		mA
				HT20, MCS7	14dBm		TBD		mA
			RX	1M DSSS	-		TBD		mA
				11M CCK	-		TBD		mA
				54M OFDM	-		TBD		mA
				HT20, MCS0	-		TBD		mA

				HT20, MCS7	-		TBD		mA
STANDBY	SLEEP	Active	TX[1]	1M DSSS, null frame	19dBm		TBD		mA
			RX	RX listen	-		TBD		mA
				1M DSSS	-		TBD		mA
		PS Mode[2]	RX	DTIM1	-		TBD		uA
				DTIM3	-		TBD		uA
				DTIM8	-		TBD		uA
				DTIM10	-		TBD		uA
		OFF	-	-	-		TBD		uA
HIBERNATION[3]	OFF	OFF	-	-	-		TBD		uA
SHUTDOWN[4]	OFF	OFF	-	-	-		TBD		uA

1. Data is captured at TX continues mode on the duration of transmitting;

2. Use XR808 by RCOSC, Beacon length 1ms；

3. RTC and wake up timer on only;

4. CHIP_PWD keeps at low level;

4 Package Specifications

4.1 Pin Layout

XR808 uses 4mm x 4mm QFN.

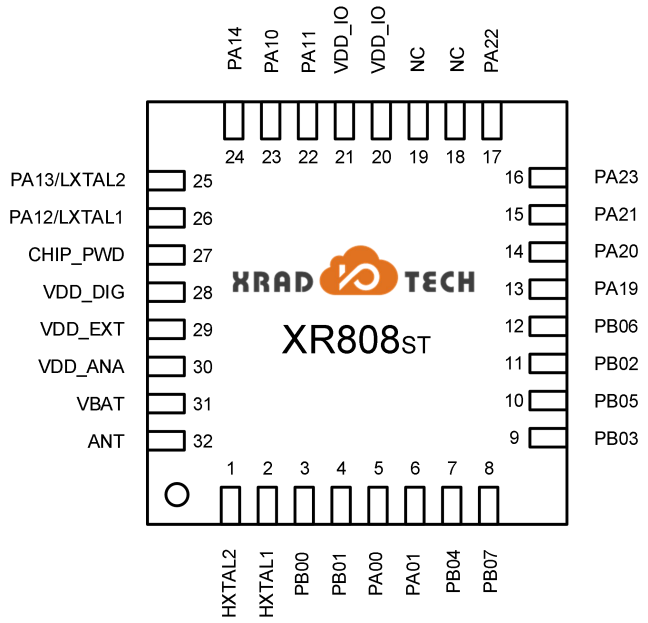


Figure 4- 1 XR808ST Pin Layout

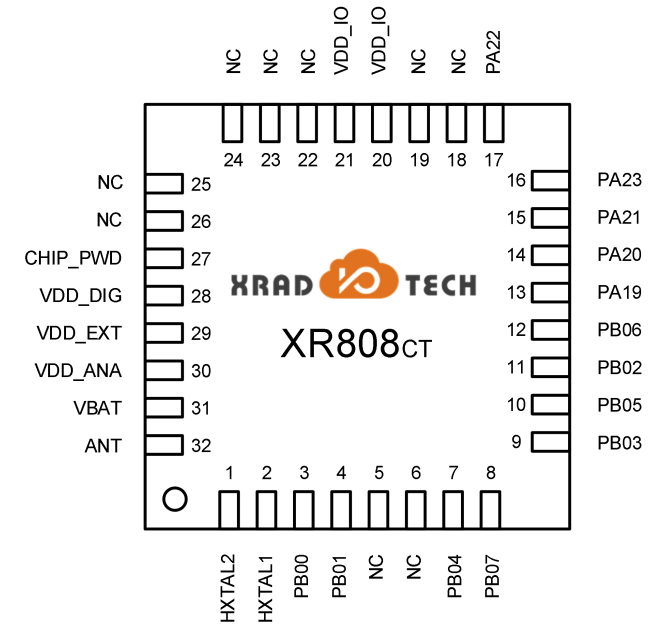


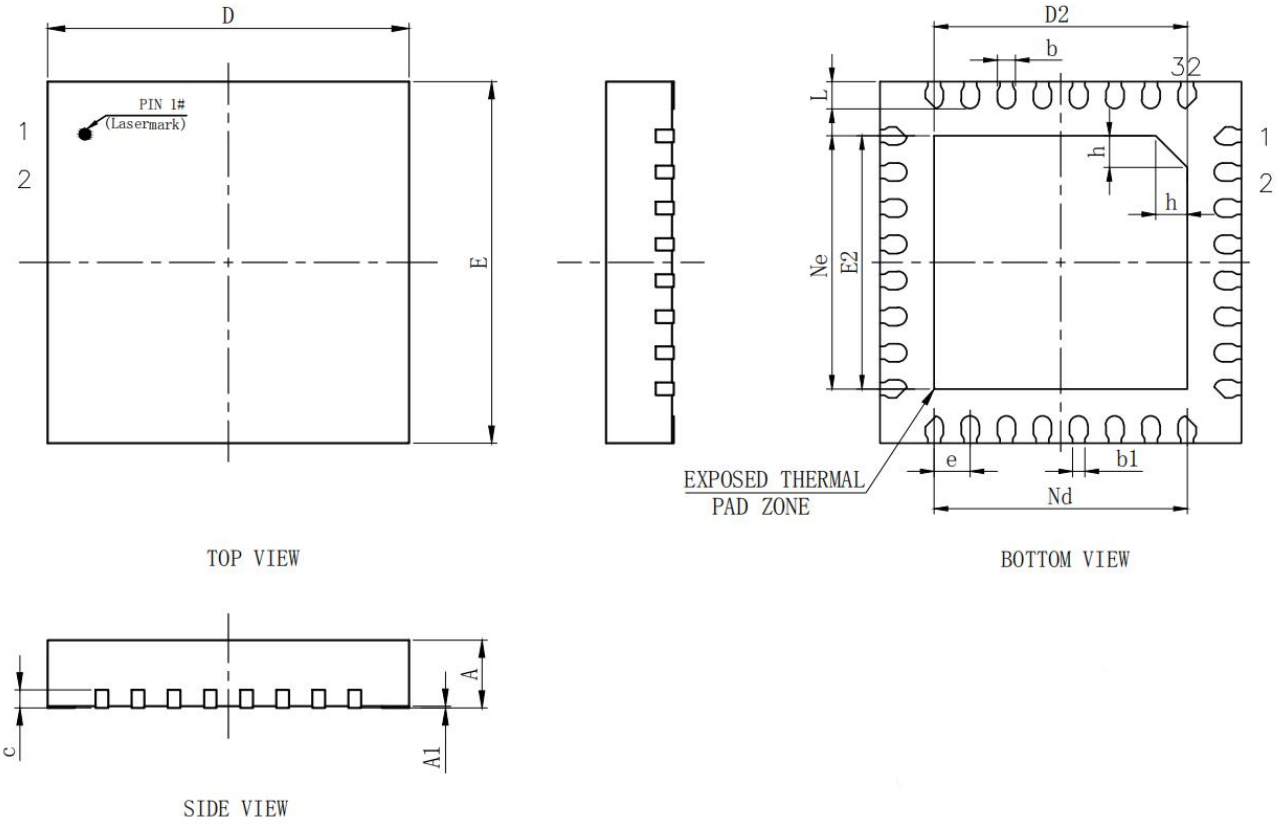
Figure 4- 2 XR808CT Pin Layout

4.2 Pin Descriptions

Table 4- 1 Pin Description

Pin Name	I/O	XR808ST	XR808CT	Pin Description
Power, Reset and Clocks				
HXTAL1	Analog	2	2	40MHz crystal
HXTAL2	Analog	1	1	40MHz crystal
LXTAL1	Analog	26	/	32.768KHz crystal
LXTAL2	Analog	25	/	32.768KHz crystal
CHIP_PWD	Input	27	27	Chip Power Down/System Reset
VDD_ANA	Power	30	30	Analog power supply
VDD_DIG	Power	28	28	1.1V digital power supply
VBAT	Power	31	31	1.62-5.5V power supply
VDD_EXT	Power	29	29	external device power supply
VDD_IO	Power	21, 20	21, 20	GPIO power supply
Programmable I/O				
PA00	In/Out	5	/	Programmable input/output
PA01	In/Out	6	/	Programmable input/output
PA10	In/Out	23	/	Programmable input/output, gpadc in
PA11	In/Out	22	/	Programmable input/output, gpadc in
PA12	In/Out	26	/	Programmable input/output, gpadc in
PA13	In/Out	25	/	Programmable input/output, gpadc in
PA14	In/Out	24	/	Programmable input/output, gpadc in
PA19	In/Out	13	13	Programmable input/output, wakeup io
PA20	In/Out	14	14	Programmable input/output, wakeup io
PA21	In/Out	15	15	Programmable input/output, wakeup io
PA22	In/Out	17	17	Programmable input/output, wakeup io
PA23	In/Out	16	16	Programmable input/output, test strap pin/wakeup io
PB00	In/Out	3	3	Programmable input/output
PB01	In/Out	4	4	Programmable input/output
PB02	In/Out	11	11	Programmable input/output
PB03	In/Out	9	9	Programmable input/output
PB04	In/Out	7	7	Programmable input/output
PB05	In/Out	10	10	Programmable input/output
PB06	In/Out	12	12	Programmable input/output
PB07	In/Out	8	8	Programmable input/output
Wi-Fi Radio Interface				
ANT	Analog	32	32	RF Antenna

4.3 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
	0. 80	0.85	0. 90
	0. 85	0.90	0. 95
A1	0	0.02	0. 05
b	0. 15	0.20	0. 25
b1	0. 14REF		
c	0. 18	0.20	0. 25
D	3. 90	4. 00	4. 10
D2	2. 70	2. 80	2. 90
e	0. 40BSC		
Ne	2. 80BSC		
Nd	2. 80BSC		
E	3. 90	4. 00	4. 10
E2	2. 70	2. 80	2. 90
L	0. 25	0.30	0. 35
h	0. 30	0. 35	0. 40
L/F载体尺寸	122X122		

Figure 4- 3 QFN32 Package Outline Drawing

4.4 Package Thermal Characteristics

Table 4- 2 QFN32 Package Thermal Characteristics

Symbol	Parameter	Conditions	Typ.	Unit
Θ_{JA}	Junction-to-Ambient	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	TBD	°C /W
Θ_{JB}	Junction-to-Board	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	TBD	°C /W
Θ_{JC}	Junction-to-Case	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	TBD	°C /W

5 Carrier Information

TBD

6 Reflow Profile

7 Application Circuit

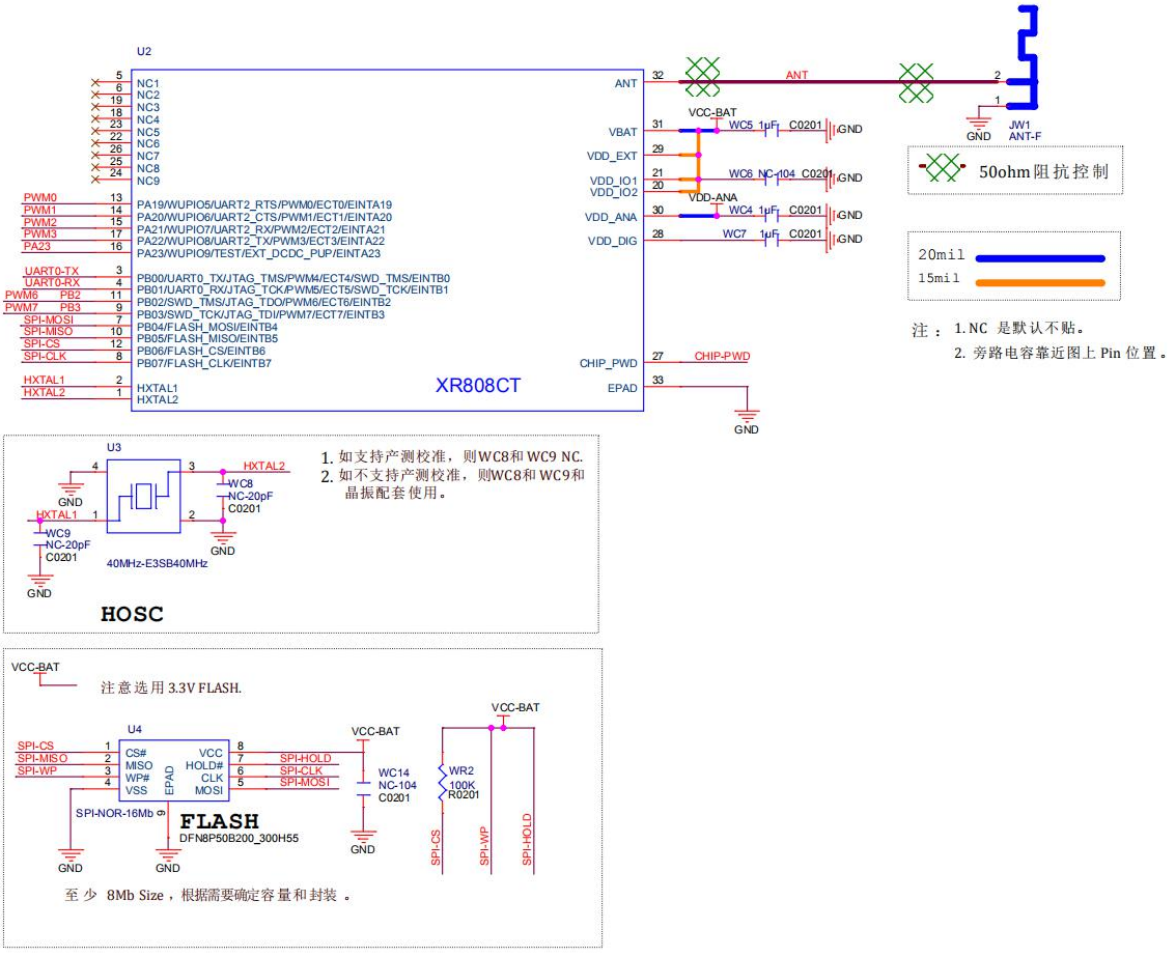


Figure 6- 1 Reference Design of XR808CT

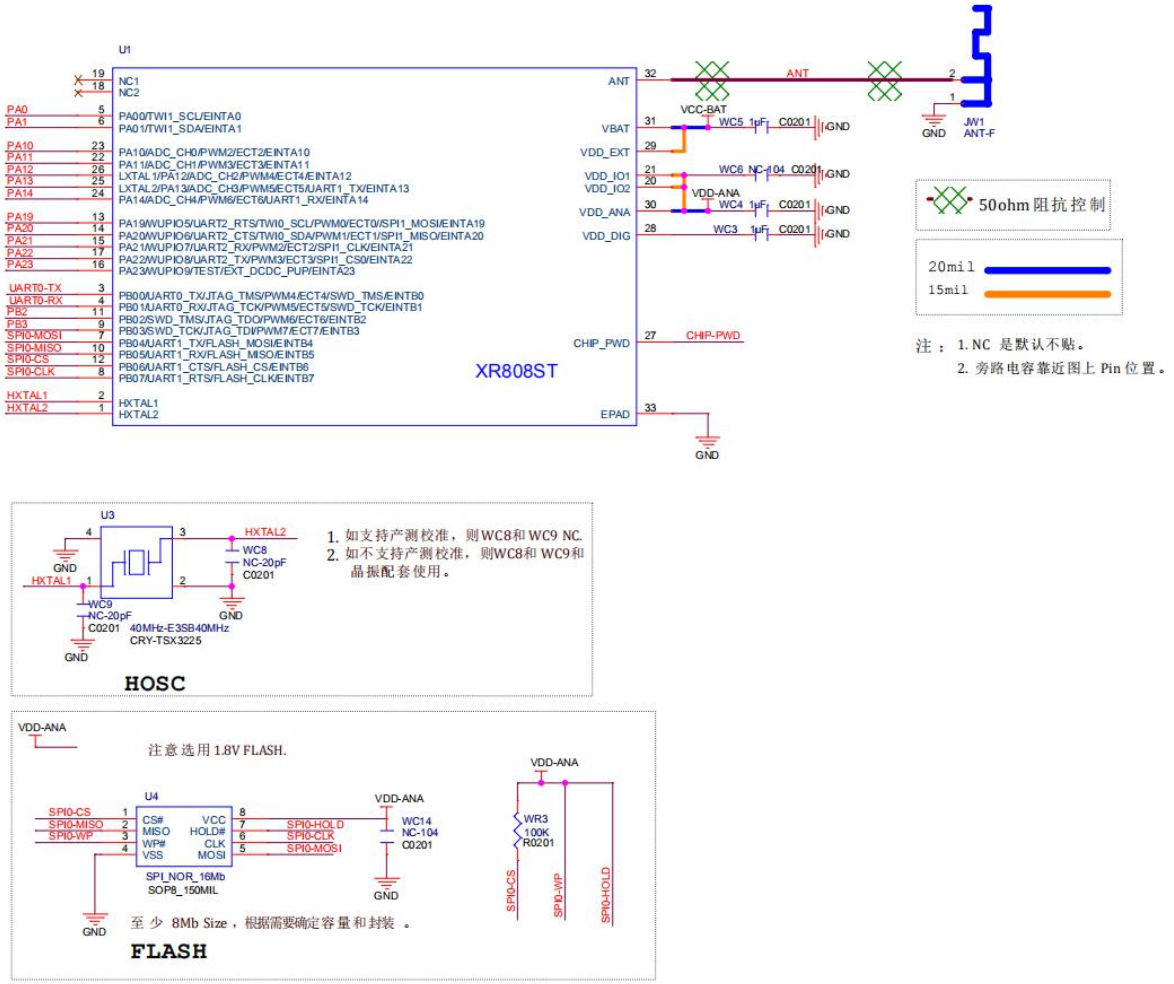


Figure 6- 2 Reference Design of XR808ST

