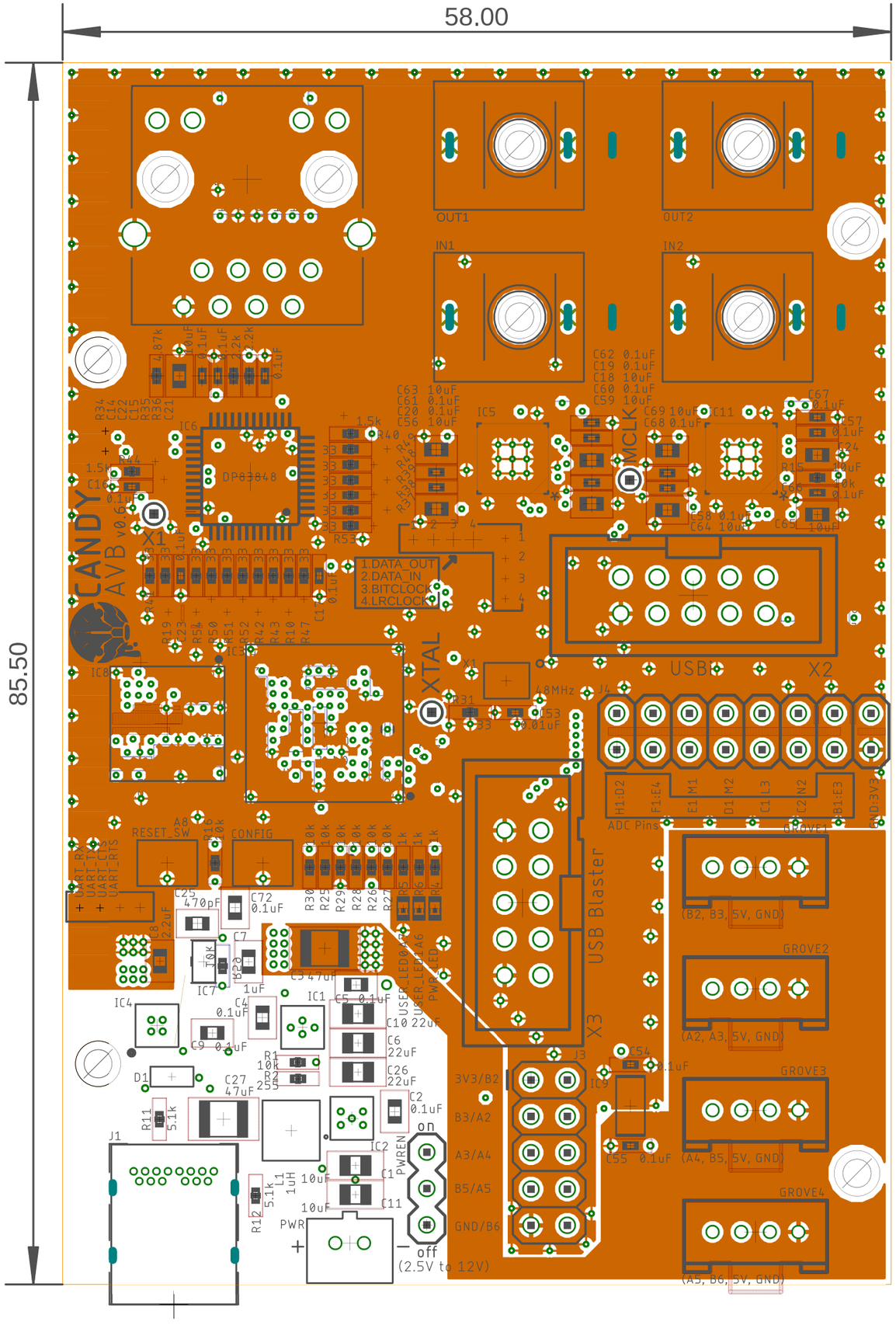

v0.1: First Release.

v0.2: Fix ADC1 pins connection.
Fix the C37 and C41 silk position.

v0.3: Fix C3 GND Pin connection.
Add Test Pad CP2102N UART line.
Add Test Pad DP83848 Ethernet line.

v0.4: Connect L11 to RX_CLK.
Change M12 from RX_CLK to RX_DV.
Refactoring some FPGA pins connection.
Rotate the X1 connector 180 degrees.

v0.5: Change C26 from 47uF to 22uF x3.
Change C1 from 47uF to 10uF x2.
Change L1 package size.
Create GND plane on top layer.

v0.6: Add the power swith MIC2005A
for the ADAU1761.