Projekt „Niskolatencyjny, synchroniczny i skalowalny system SDR” (NESTER)

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**Raport z pracy o dzieło z prawami autorskimi pt.:  
„Opracowanie  schematów i PCB modułu EEM z układem FPGA”  
zrealizowanej w okresie od 13.01.2020 r. do 26.02.2020 r.  
Pracę wykonał Piotr Zdunek**

Celem pracy było opracowanie schematów i PCB modułu EEM z układem FPGA  
Realizacja pracy obejmowała:

* Analizę wymagań
* Analiza opóźnienia systemu ADC-FPGA-DAC
* Dobór komponentów
* Realizację schematów

Wynikiem pracy jest:

* Zbiór wymagań pozwalających na realizację systemu

<https://github.com/sinara-hw/Fast_Servo/wiki/Requirements>

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| --- |
| System requirements:   * FastServo shall resemble the Stabilizer architecture and mechanical design * FastServo shall support PoE, Ethernet, USB interfaces (the same as Stabilizer) * FastServo shall support Trenz FPGA modules - e.g. TE0710-02-35-2CF or TE0712-02-100-2C * FastServo shall support 2x fast ADC channels * FastServo shall support 2x fast DAC channels * FastServo shall support 1 or 2 EEM connectors routed to the FPGA (to be discussed)   DAC subsystem requirements:   * DAC channel shall have latency + BW suitable for 3MHz closed-loop applications (including latency of loop filter on FPGA) * DAC channel shall have fixed +-1V input/output range * DAC channel bandwidth shall be 100 MHz or 125MHz 16bit   ADC channel requirements   * ADC channel AFE shall be based on [FmcAdc100M14 design](https://ohwr.org/project/fmc-adc-100m14b4cha/wikis/home) * ADC channel shall use LTC2195 as an ADC * ADC channel bandwidth shall be 100 or 125MHz 16bit |

* Analiza opóźnienia toru danych ADC-FPGA-DAC (prace jeszcze trwają)

<https://docs.google.com/document/d/1A6bej79ME2-iZyJ6t_FZ-XkVyk64ExRZh2uJX7Lg3b4/edit?usp=sharing>

* Dobór komponentów
  + ADC – LTC2195 – porównanie różnych układów <https://docs.google.com/spreadsheets/d/1j0nTGpnnnBx4UXwtZlGYXvdnvVj7PuF5h2WQjEc7hA4/edit?usp=sharing>

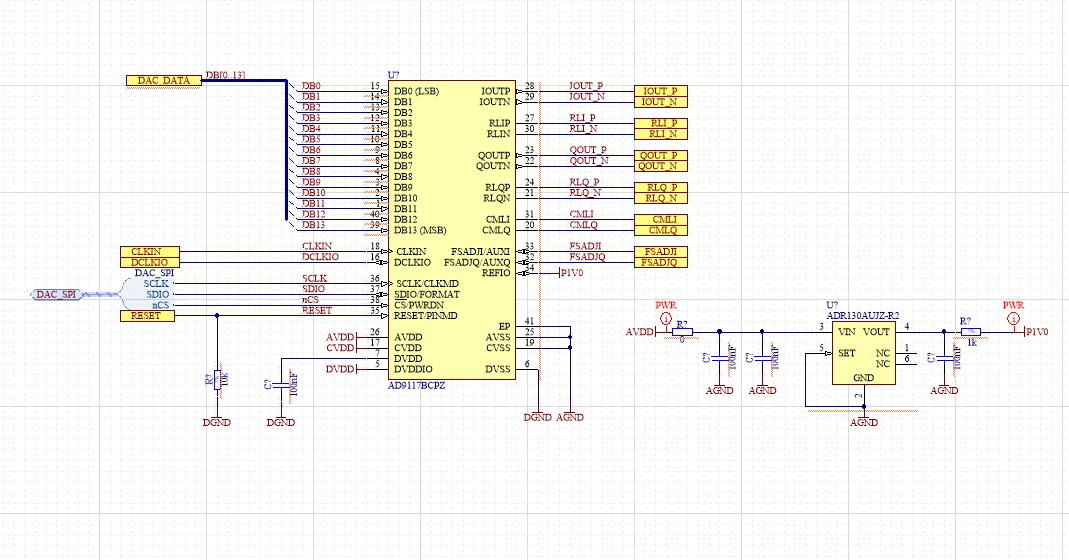
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| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| MFN Part number | No. CH | Sample rate [GSPS] | Bits | INL | DNL | Latency | Price [USD] | Project used |
| DAC3xJ82 | 2 | 1.6/2.5 | 16 | 6 | 4 |  | 100 |  |
| DAC5682Z | 2 | 1 | 16 | 4 | 2 |  | 54 |  |
| LTC2000 | 1 | 2.5 | 16 | 1 | 0,5 | 11 cycles (DAC clk - up to 2500 MHz), for 500 MHz, latency = 11\*2 = 22 ns | 127 | Shuttler |
| ~~AD9125~~ | ~~2~~ | ~~1~~ | ~~16~~ | ~~3,7~~ | ~~2,1~~ | ~~64 cycles (1 x interpolation fdac up to 1 GHz) + FIFO delay, depending on the mode(8 reg deep), for 500 MHz fdac, latency = 64\*2 + 8\*2 = 144 ns~~ | ~~50~~ |  |
| MAX5898 | 2 | 0,5 | 16 | 3 | 1 | 2.9 ns (tpd) + 1.4 ns (td) + 22 cycles (500 MHz) = 2.9 + 1.4 + 44 = 48.3 ns (for 1 x interpolation) | 27 |  |
| AD9783 | 2 | 0,5 | 16 | 4 | 2 | 7 cycles (7 ns \* 2ns = 14 ns) + SET/HLD setup (to be analysed) approx. 2.4 ns = 16.4 ns | 43 | NIST servo |
| AD9747 | 2 | 0.25 | 16 | 4 | 2 | 7 cycles (250 MHz DAC CLK), latency = 7\*4 = 28 ns |  |  |
| MAX5875/ | 2 | 0.2 | 16 | 3 | 2 | 1.1 ns + 9 cycles \*5 ns = 46.1 ns |  |  |
| MAX5878 | 2 | 0.25 | 16 | 3 | 2 | 9 cycles (500 MHz clk) latency = 9\*2 = 18 ns |  |  |
| AD9788 | 2 | 0.8 | 16 | 3.7 | 2.1 | 40 cycles (800 MHz clk) latency = 40\*1.25 ns = 50 ns |  |  |
| AD9117 | 2 | 0.125 | 14 | 1.2 (precalibration), 0.6 (postcalibration) | 1.4 (precalibration), 0.6 (postcalibration) | 4 cycles for 1 channel, 3.5 cycles for second channel (input latched on falling edge), data clock = 125 MHz, latency = 4\*8ns = 32 ns | 15 |  |

* + DAC – AD9117 – porównanie różnych układów

<https://docs.google.com/spreadsheets/d/1_hZ97hf2xaO5iiprr2quBoDU6UxvHmOqcvnQKTeb41w/edit?usp=sharing>

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| MFN Part number | Channels | Sample rate [MSPS] | Bits | INL | DNL | Latency | SFDR dBc (fin=10MHz) | Price [USD] | Project used |
| AD9461 | 1 | 130 | 16 | 5 | 0,6 |  | 90 | 107 |  |
| LTC2107 | 1 | 210 | 16 | 1,6 | 0,4 |  | 103 (for fin=5 MHz) | 140 | CCD GK camera |
| LTC2195 | 2 | 125 | 16 | 2 | 0,5 | 1.1ns+2\*tser + 4ns + 7\*4 ns pipeline delay = 34 ns | 90 | 160 | NIST servo |
| ADS42LB69 | 2 | 250 | 16 | 3 | 0,6 |  | Not sure. | 240 |  |
| ADS5483 | 1 | 135 | 16 | 3 | 0,5 |  | 98 | 135 |  |
| LTC2209 | 1 | 160 | 16 | 5,5 | 1 |  | 100 | 116 |  |

* + FPGA – moduł TE07020
* schemat elektryczny urządzenia zawierający dobrane komponenty (prace jeszcze trwają). Załączam dwa zrzuty schematów z projektu.
  + Układ DAC



* Moduł FPGA

