High Frequency Ceramic Solutions

Sub-GHz Impedance Matched Balun + LPF integrated Passive Component for Texas Instruments' CC1310 Chipset

P/N: 0850BM14E0016

Detail Specification: 9/16/2016

Do you need a small 900MHz antenna? Go to: www.johansontechnology.com/antennas

General Specifications

Part Number	0850BM14E0016	
Frequency (MHz)	770 ~ 860	860 ~ 928
Unbalanced Impedance (Ω)	50	
Balanced Impedance (Ω)	Impedance matched to Texas Instruments' CC1310 chipset	
Insertion Loss (dB)	1.3 typ (1.6 max.)	1.8 typ (2.2 max.)
Return Loss (dB)	9.5 min.	9.5 min.
Phase Difference (deg)	180±17	180±15
Amplitude Difference (dB)	3.5 max.	2.0 max.
Attenuation (dB)	15 min.@ 1720~1736 MHz 15 min.@ 1736~1856MHz 30 min.@ 2310~2580 MHz 30 min.@ 2580~2784 MHz 33 min.@ 3080~3440MHz 35 min.@ 3440~3712 MHz	
Power Capacity	2W max. CW	

Texas Instruments - Approved!

Quantity/Reel	4,000 pcs
Operating Temperature	-40°C to +85°C
Storage Temperature Range	-40°C to +85°C
Storage Period	18 months max
Recommended Storage Conditions for unused T&R product	+5 ~ +35 °C, Humidity 45~75%RH, 18 mos. max

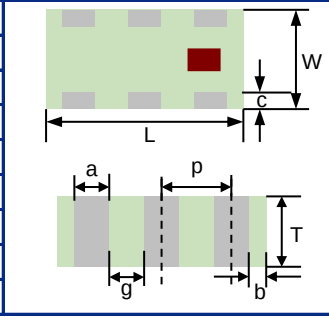
For more TI matched balun-filters, go to: www.johansontechnology.com/ti

Part Number Explanation

P/N Suffix	**Packing Style**	Bulk	Suffix = S	eg. 0850BM14E0016S
		T & R	Suffix = E	eg. 0850BM14E0016T
		100% Tin	Suffix = None	eg. 0850BM14E0016(T or S)

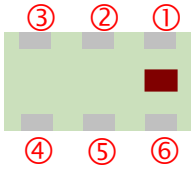
Mechanical Dimensions

	In	mm
L	0.063 ± 0.004	1.60 ± 0.10
W	0.031 ± 0.004	0.80 ± 0.10
T	0.024 ± 0.004	0.60 ± 0.10
a	0.008 ± 0.004	0.20 ± 0.10
b	0.008 +.004/-.008	0.20 +0.1/-0.2
c	0.006 ± 0.004	0.15 ± 0.10
g	0.012 ± 0.004	0.30 ± 0.10
p	0.020 ± 0.002	0.50 ± 0.05



Terminal Configuration

No.	Function	No.	Function
1	Unbalanced Port	4	Balanced Port RF_P
2	RX/TX		
3	Balanced Port RF_N	5	GND
		6	GND



Would you like us to review your layout for free? Need an antenna recommendation for your application?
Contact us at:
www.johansontechnology.com/ask-a-question

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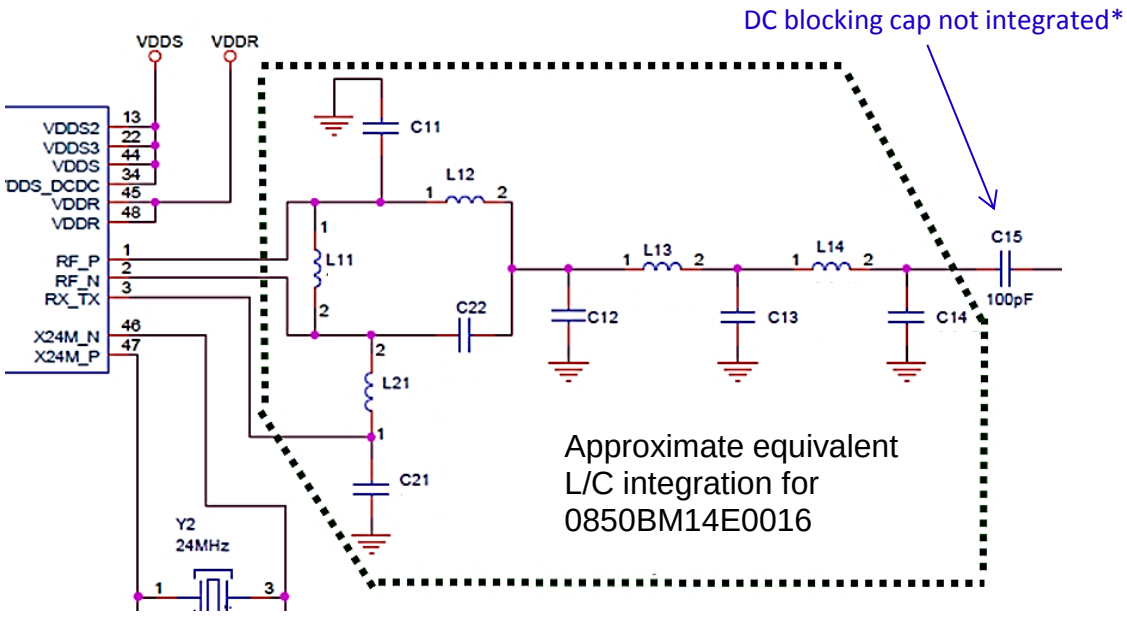
Equivalent L/C Circuit Integrated into IPC



*Even though Pins 3, 4, and 1 are internally *DC blocked* from GND, Pins 3/4 are *DC coupled* to Pin 1 (there's a DC path between them). We recommend the designer place a DC blocking cap (68-100pF) in series after Pin 1 (between IPC and antenna).

Would you like the reference design, schematic, and gerber files? Need us us to review your layout for free or an antenna recommendation for your application? Contact us at:

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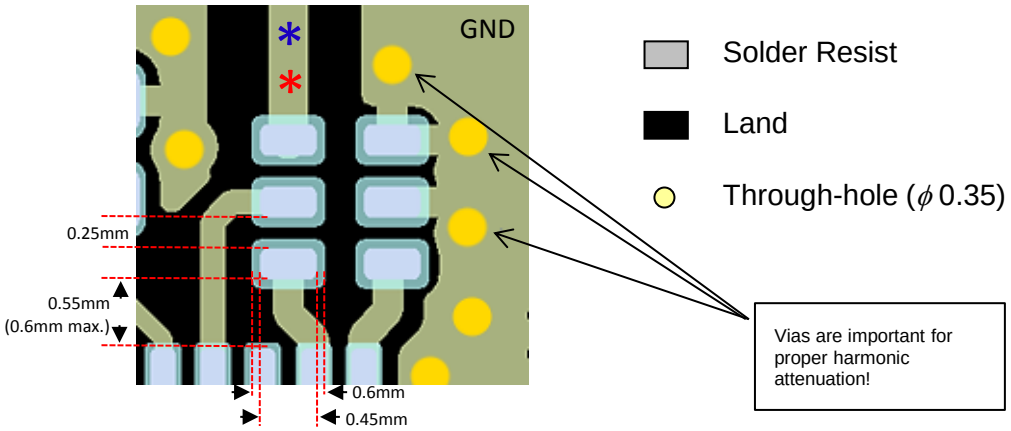
Pad-Soldermask Guidelines

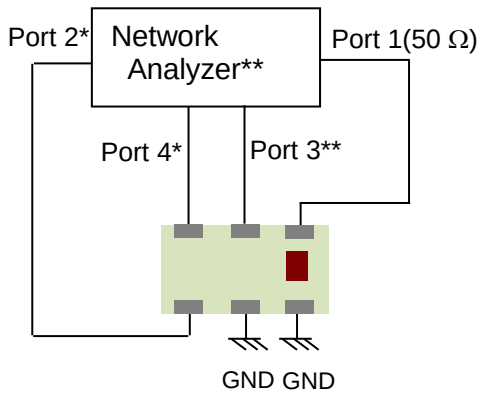
Request reference design, schematic, and gerber files at: www.johansontechnology.com/ask-a-question



* Even though Pins 3, 4, and 1 are DC blocked from GND, Pins 3/4 are DC coupled to Pin 1 (there's a DC path between them). We recommend the designer place a DC blocking cap (68-100pF) in series after Pin 1 (between IPC and antenna) per page 2 of the datasheet.

* Line width should be designed to match 50ohm characteristic impedance, depending on PCB material and thickness. Grounded CPWG is recommended.

Measurement Diagram



Port 1:Unbalanced Port
Ports 2 and 4: Balanced Port
*Ports 2 and 4 Terminate impedance
=Conjugate match to TI CC13XX chipset
Port 3: RX_TX Port
**Port 3 Terminate impedance
=The load Impedance looking into RX_TX pin of TI CC13XX chipset
$IL=S_{DS}21$
$RL=S_{SS}11$
Amp_balance = dB(S(2,1)/S(4,1))
Phase_balance = Phase(S(2,1)/S(4,1))

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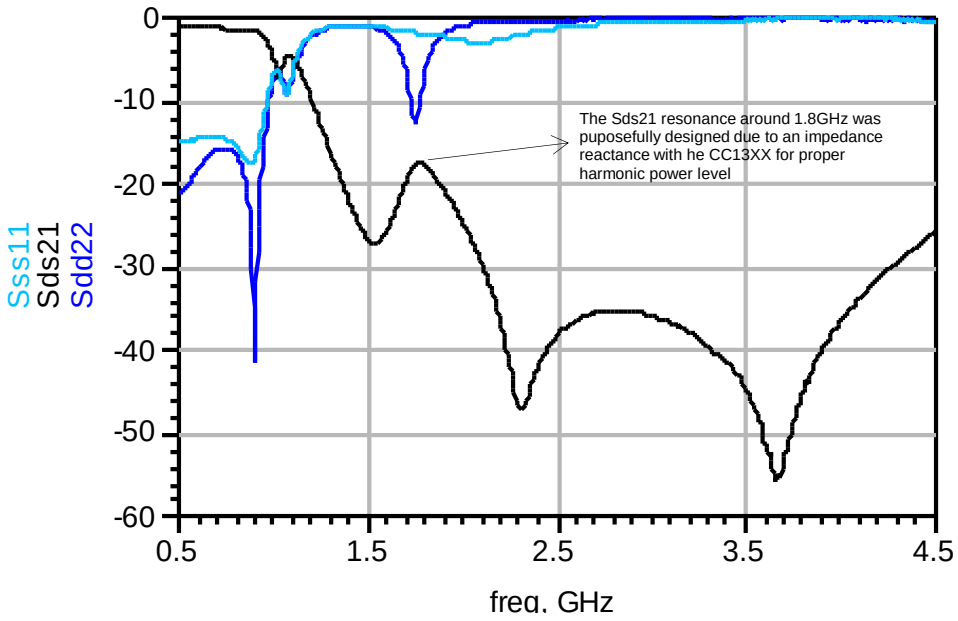
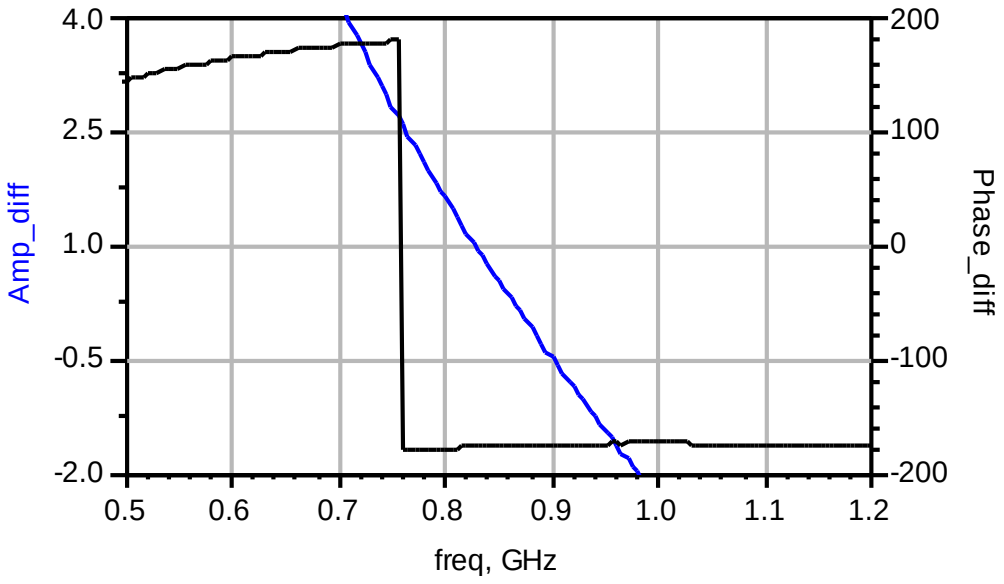
Typical Electrical Characteristics (T=25°C)





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Application Notes, Layout Files, and more
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