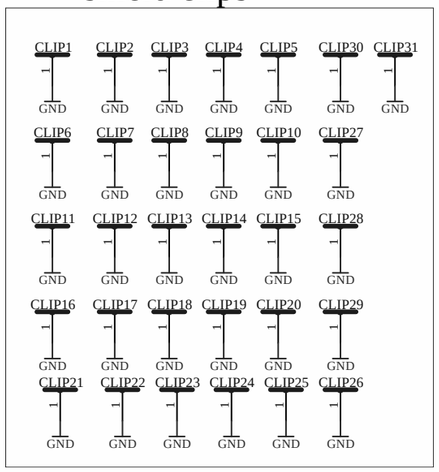
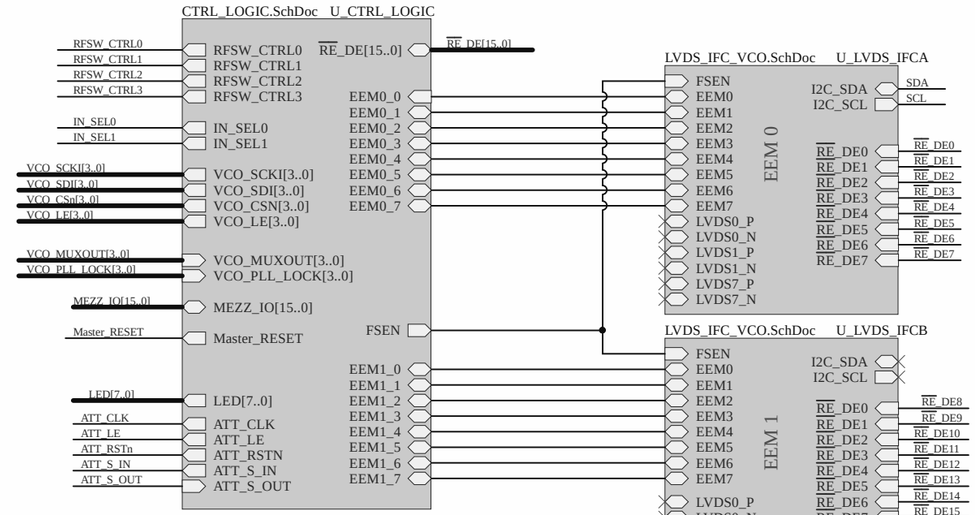
shield clips

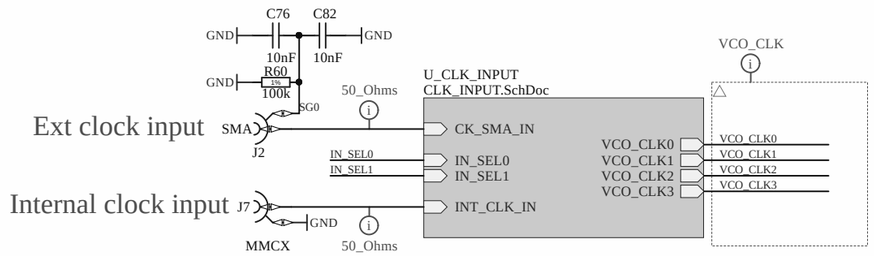


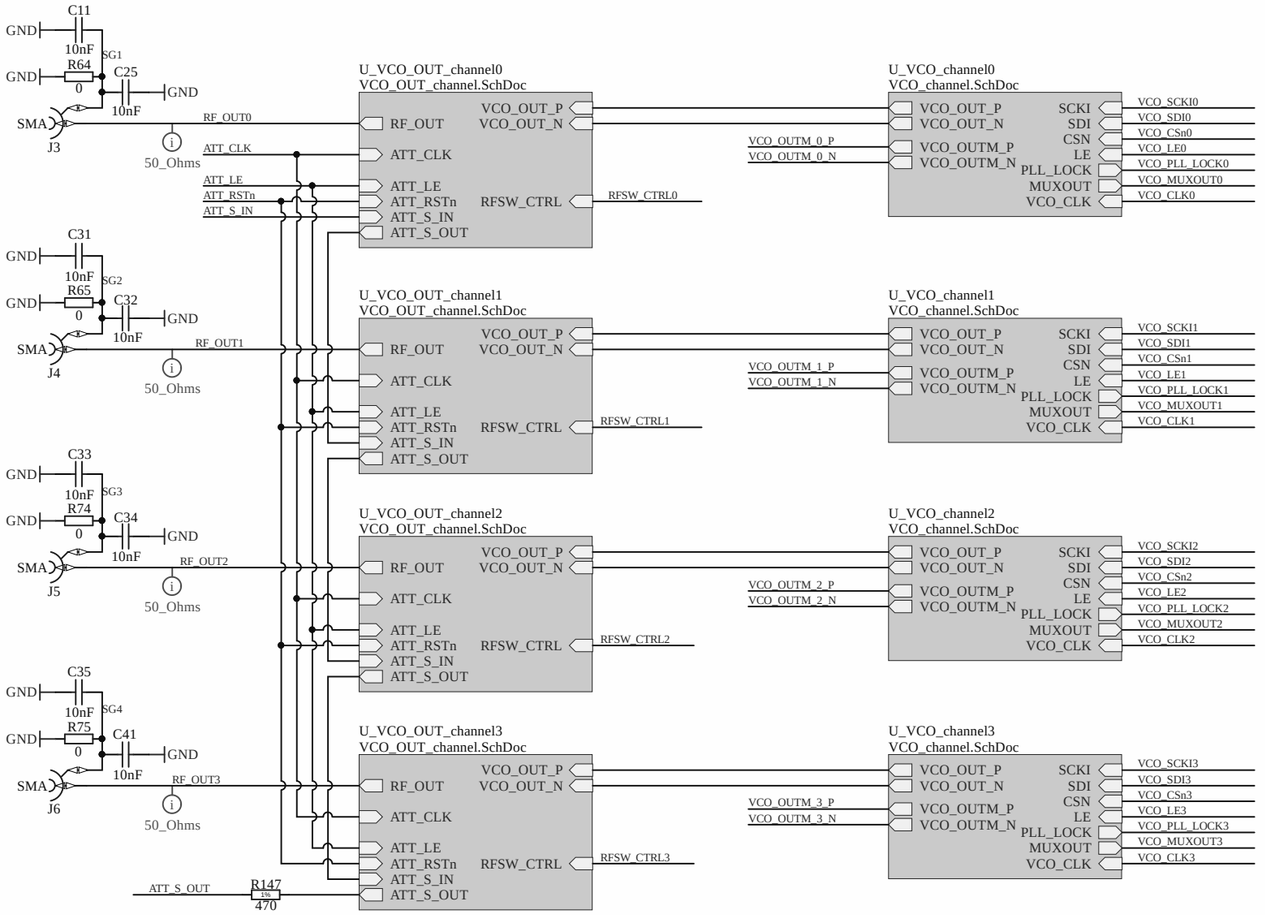
Output SMAs

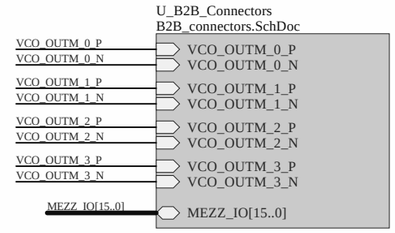
SMA Insulating washers

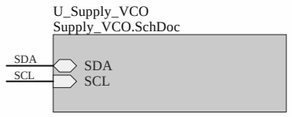
WASHER1 D11.1xd6.6	WASHER2 D11.1xd6.6
WASHER3 D11.1xd6.6	WASHER4 D11.1xd6.6
WASHER5 D11.1xd6.6	WASHER6 D11.1xd6.6
WASHER7 D11.1xd6.6	WASHER8 D11.1xd6.6
WASHER9 D11.1xd6.6	WASHER10 D11.1xd6.6

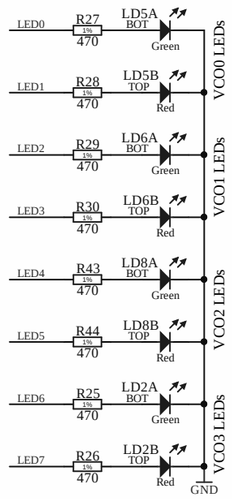












FTG1 FTG2 FTG3 FTG4

Project/Equipment	ARTIQ/SINARA		
Document	*3U VCO/PLL (MIRNY) v1.0* *Top entity*	Designer K.B.	
		Drawn by K.B.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	2018-10-15
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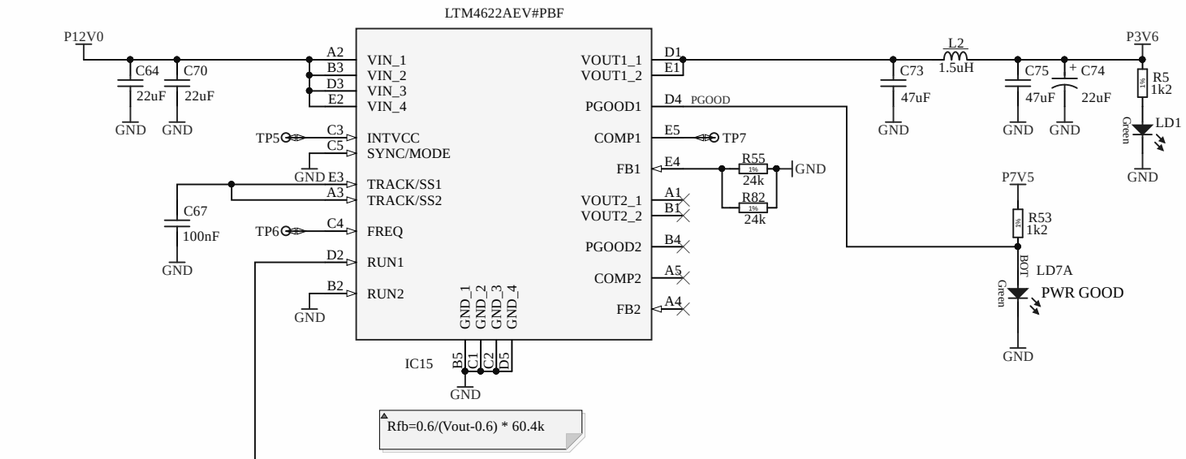
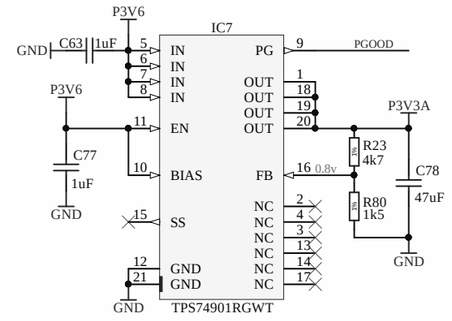
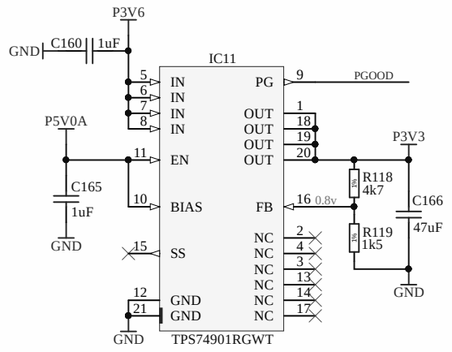




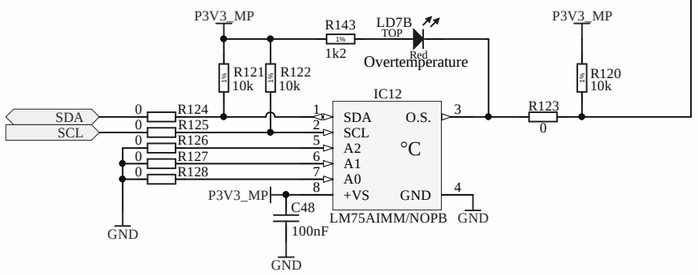


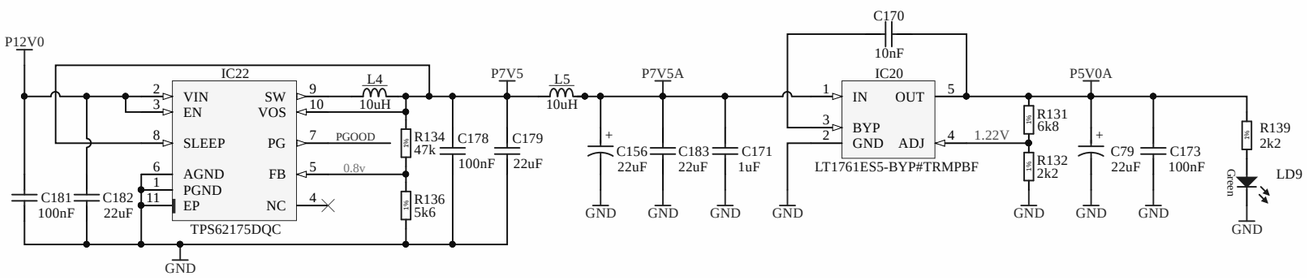
Power budget (max ratings):

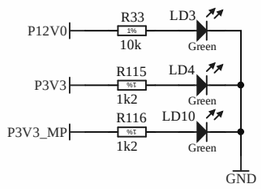
P3V3:	
LVDS interface 4x	660
LVDS load 4x24mA	96
CPLD	100
ADF4351	4*(27+36+80+26)=676
SY89855UMG	4*(85)=340
TCXO	6
TOTAL P3V3	1878
TOTAL POWER	6.1974 W
P5V0	
HMC542BLP4E	4*2.9=11.6
HMC349LP4C	4*3.5=14
TOTAL 5V0	25.6
TOTAL POWER	0,125 W
DC/DC converter losses	
TPS62175 eff .95	0,05*(0,026)*7,5=0.01 W
LTM:3.6V eff .9	0.1*1,878*3,6=0,676 W
LDO losses	
3.6V->3.3V	0.564 W
7.5V->5V	0,064 W
Total power from 12V	7.64 W
Total current from 12V	0.6367 A

ADR: 1001 000

Thermal shutdown.







P3V3 TP12
P3V3A TP13
P3V3_MP TP14
P3V6 TP15
P5V0A TP16
P12V0 TP18

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Power supply DC/DC & LDOs

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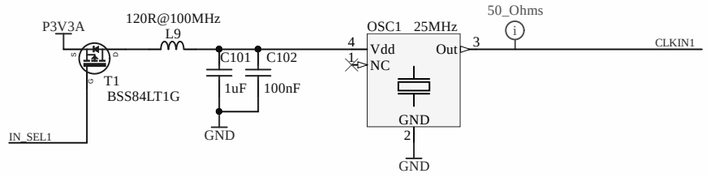
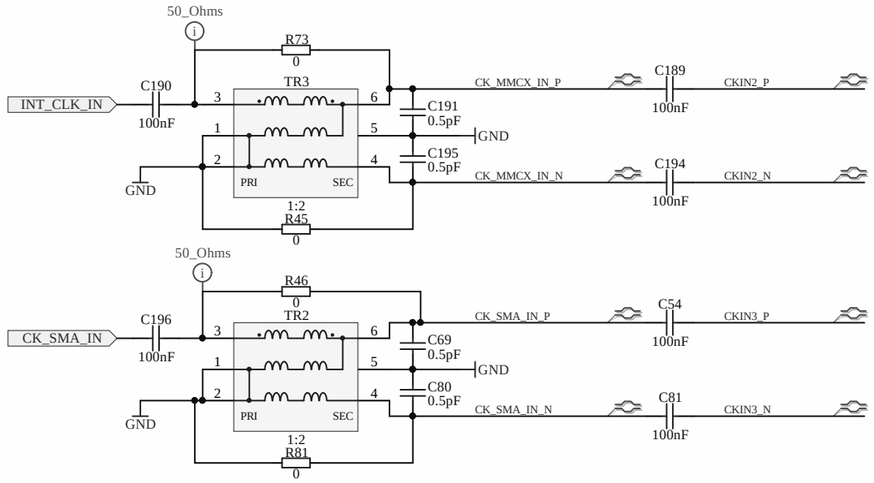
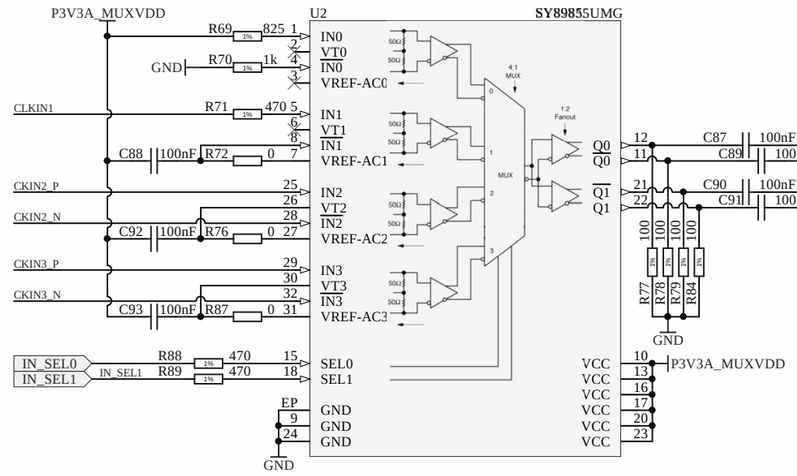


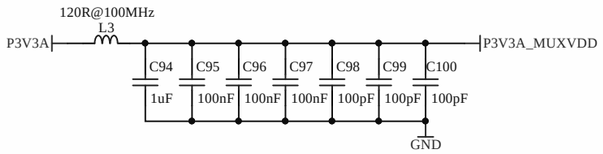


AC-Coupled Input Termination, Such as LVDS and LEVPECL



TRUTH TABLE

SEL1	SEL0		
0	0	IN0 Input Selected	-
0	1	IN1 Input Selected	XO
1	0	IN2 Input Selected	MMCX
1	1	IN3 Input Selected	SMA



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Clock distribution and generation

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$RF_{OUT} = [INT + (FRAC/MOD)] \times (f_{PFD}/RF\ Divider)$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
FRAC is the numerator of the fractional division (0 to MOD − 1).
MOD is the preset fractional modulus (2 to 4095).
RF Divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))]$$

where:
REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit (0 or 1).
R is the RF reference division factor (1 to 1023).
T is the reference divide-by-2 bit (0 or 1).

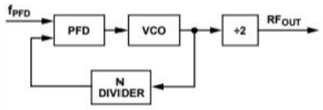
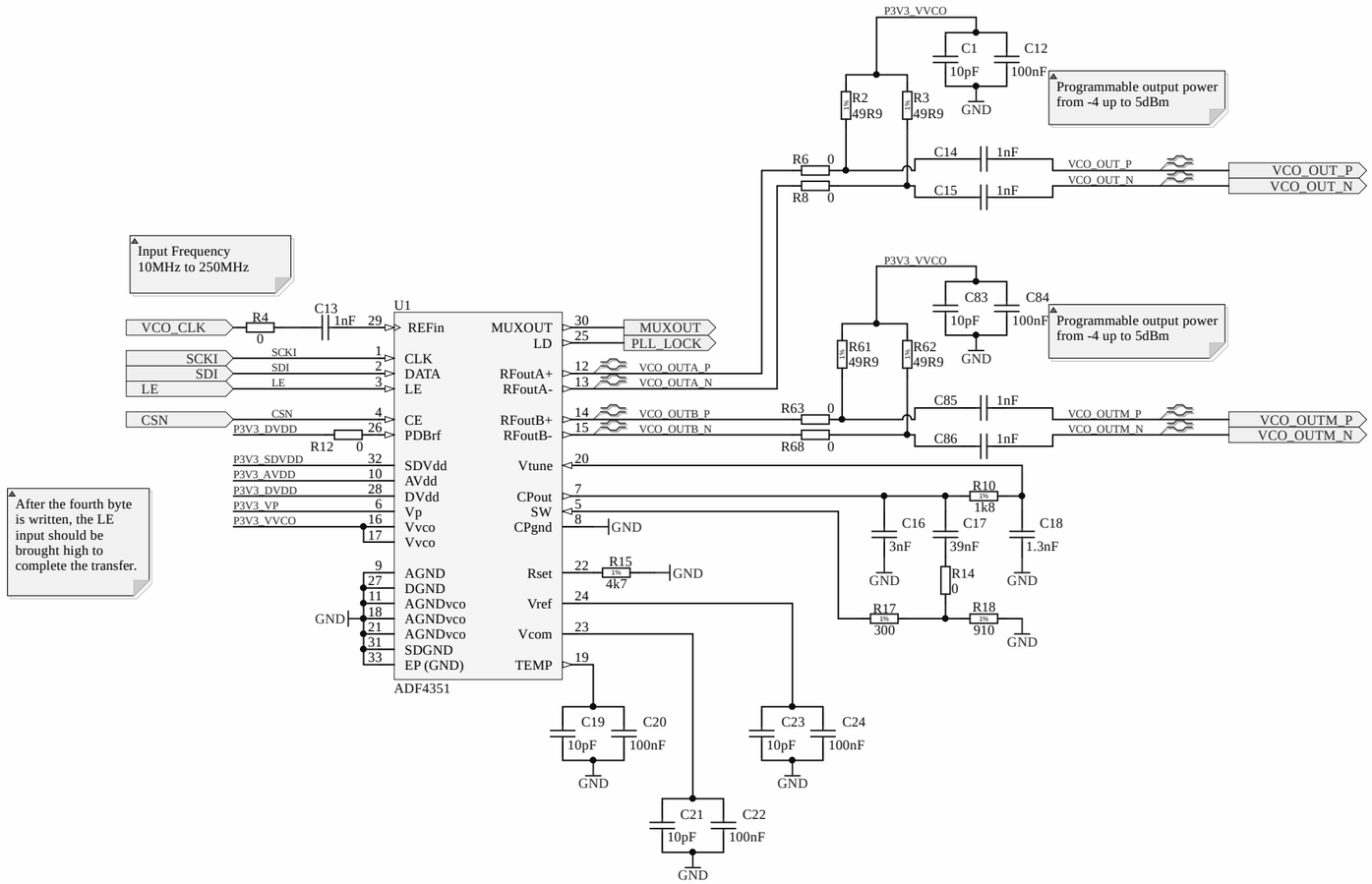
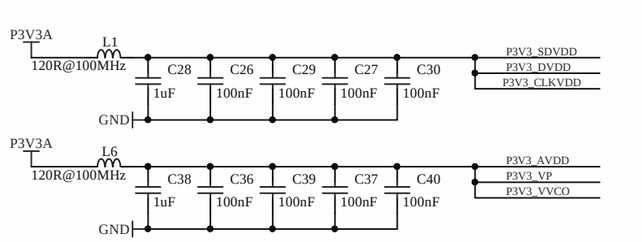


Figure 30. Loop Closed Before Output Divider

D = 0
T = 0
R = 1
MOD = 4000

Start Freq	Stop Freq	VCO Divider	Channel Spacing
40.0MHz	68.75MHz	64	97.656 Hz
68.75MHz	137.5MHz	32	195.31 Hz
137.5MHz	275MHz	16	390.63 Hz
275MHz	550MHz	8	781.25 Hz
550MHz	1.10GHz	4	1.5625kHz
1.10GHz	2.20GHz	2	3.125kHz
2.20GHz	4.00GHz	1	6.25kHz





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ADF4351 VCO

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One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

Discrete-elemet filter with R57/59 & R58/C28

3x Mini-Circuits FV1206 filters

Jumper

Jumper

Amplifier
+13dB @ 2GHz typ.

IC2
ERA-4XSM+

TR1
1:2

Digital Attenuator

IC3
HMC542BLP4E

F clk max = 30MHz

SPDT switch

IC4
HMC349ALP4CE

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Output stage : Attenuator, amplifier and filter

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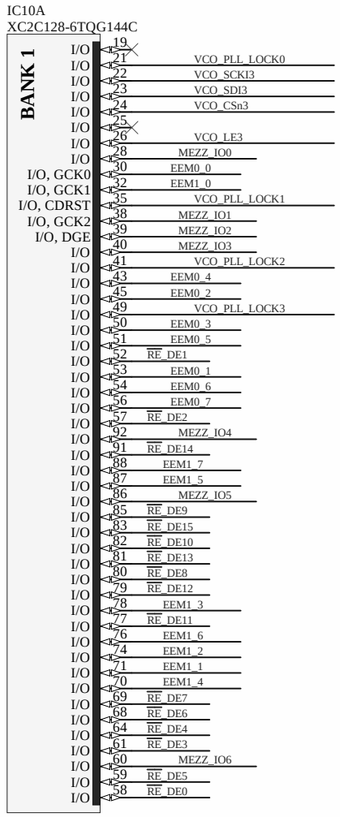

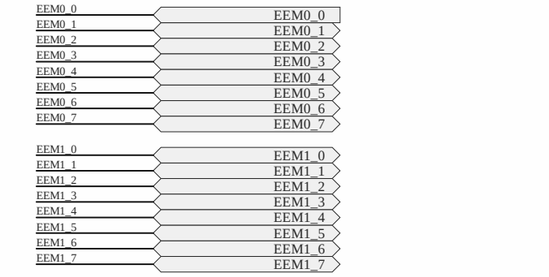

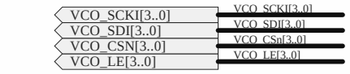

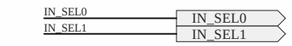

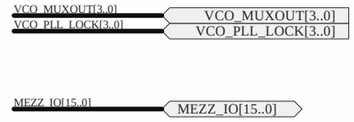

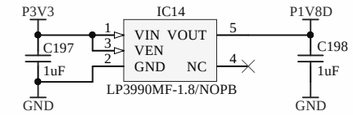

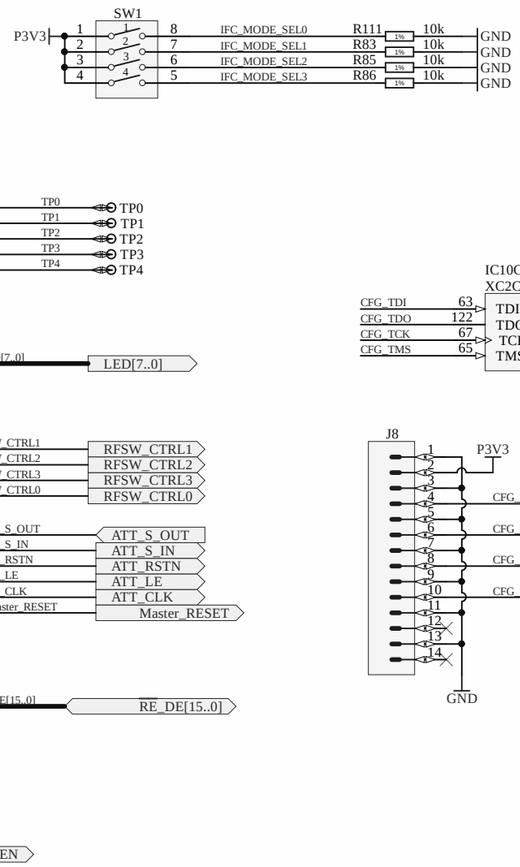

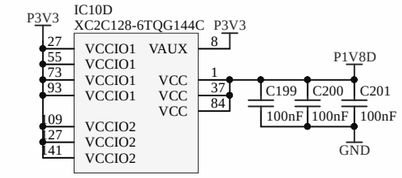

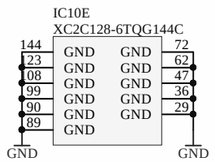

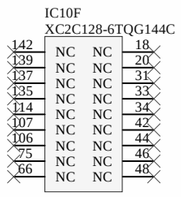

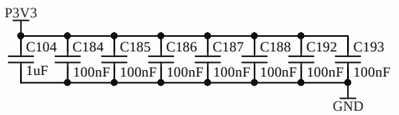

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CPLD logic & option switches

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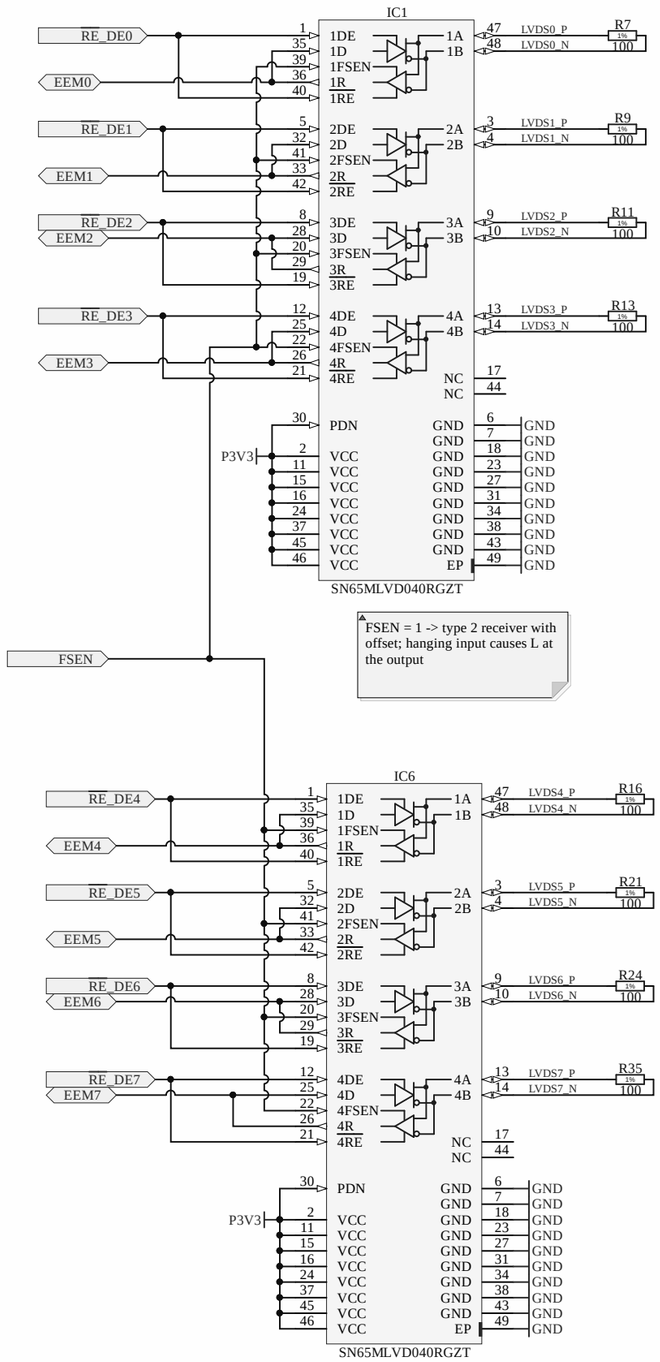
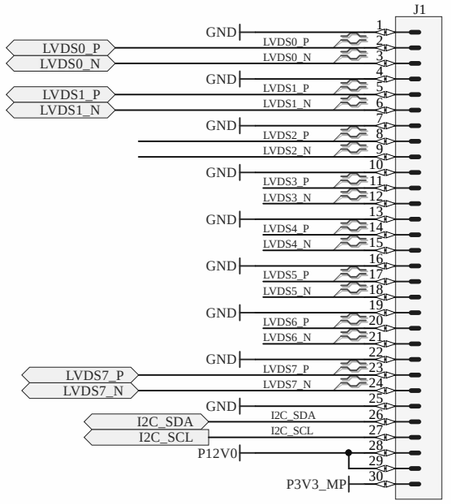
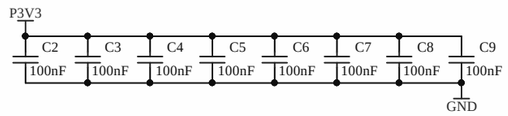
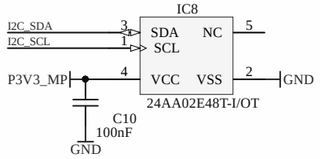


EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A







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LVDS to LVTTL interface & EEM connector

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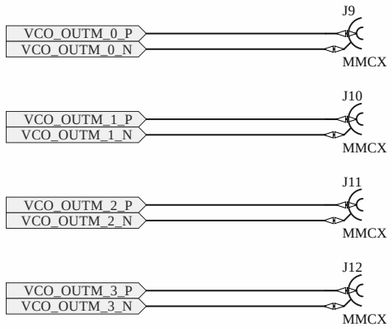
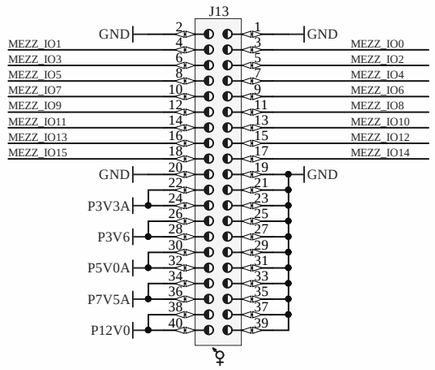
Board-2-Board Analog Connectors



Board-2-Board Digital Connector



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AFE Mezzanine Connectors

Designer	K.B.	
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