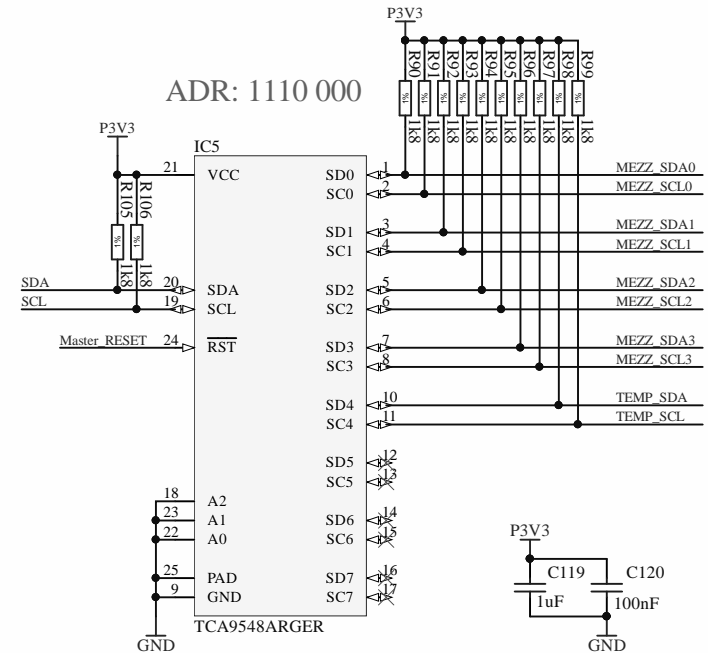
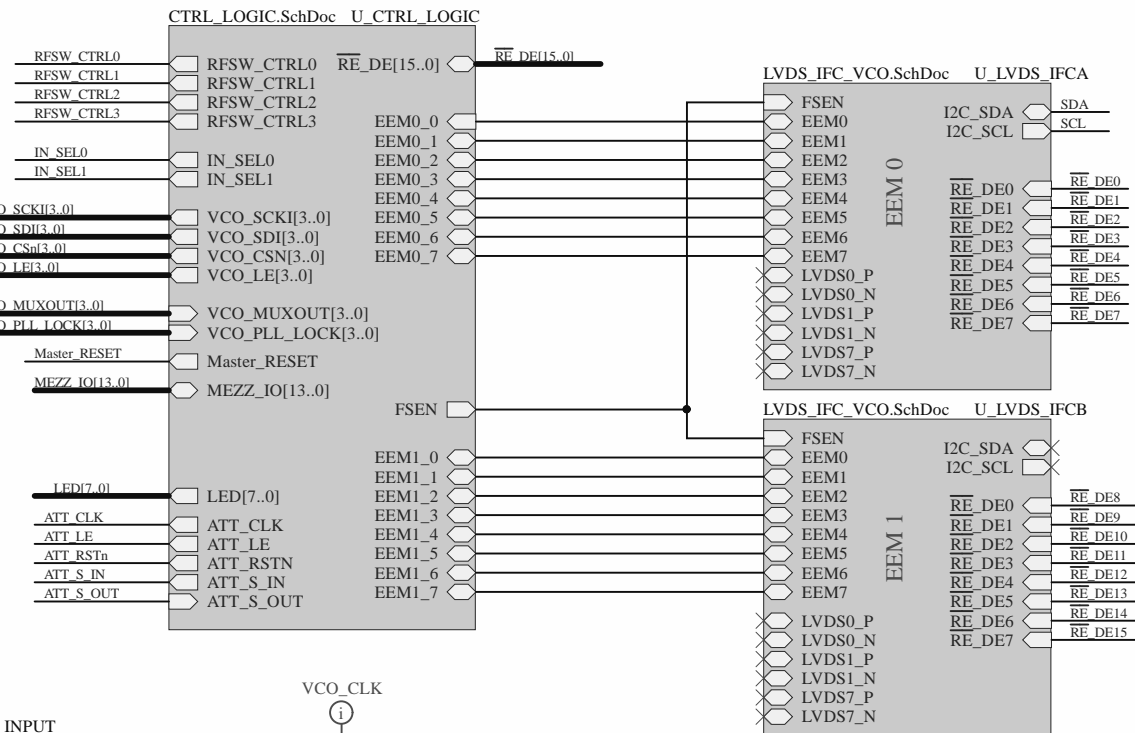
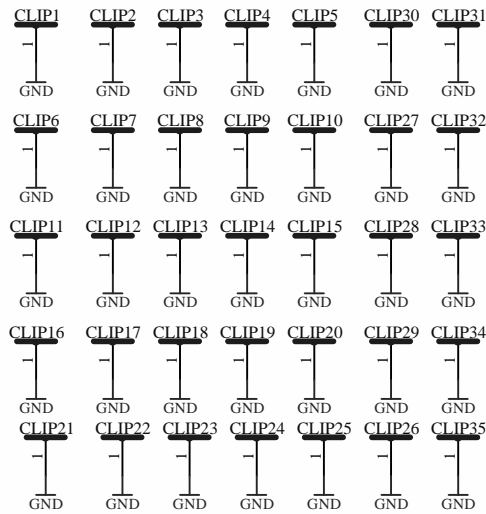


shield clips



I2C tree:

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}
```

Ext clock input

Internal clock input

Output SMAs

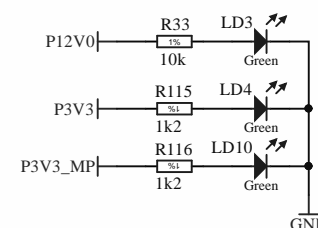
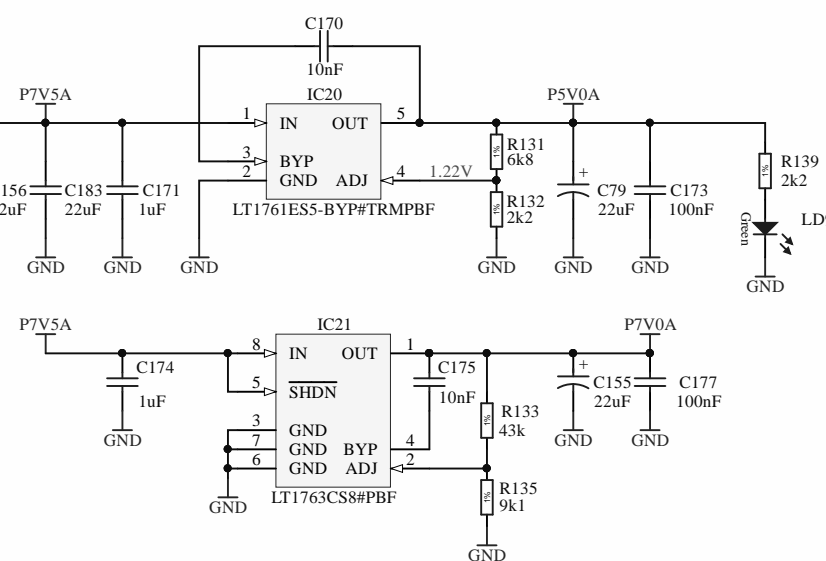
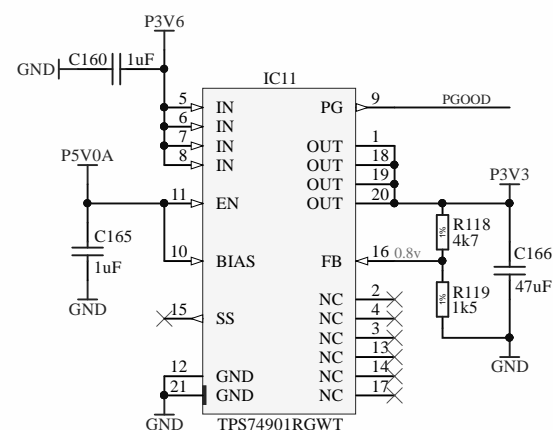
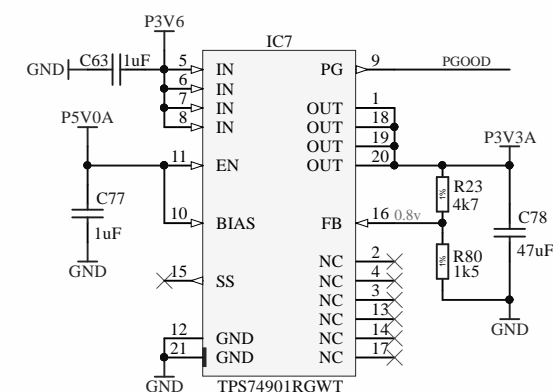
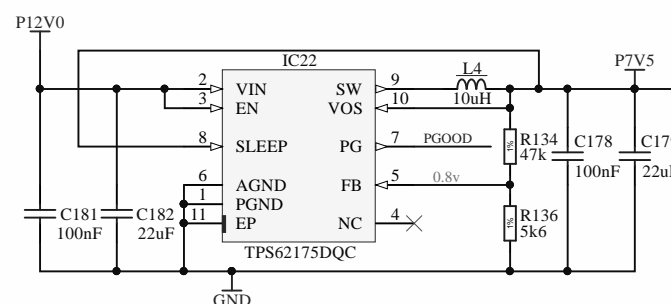
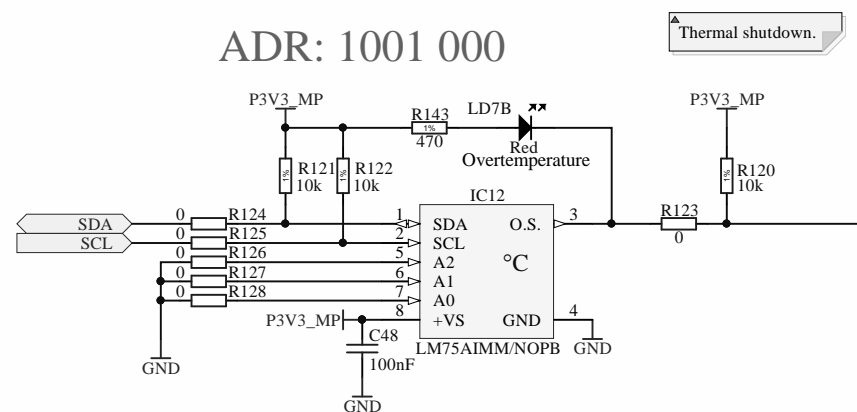
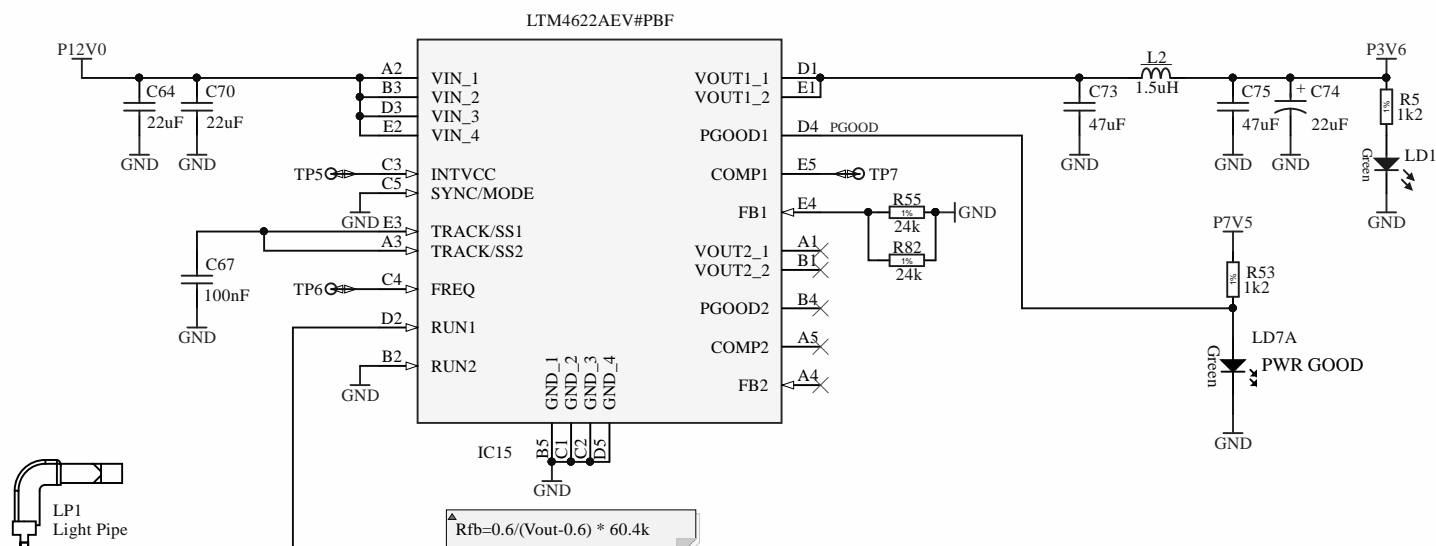
SMA Insulating washers

WASHER1 D11.1xd6.6	WASHER2 D11.1xd6.6
WASHER3 D11.1xd6.6	WASHER4 D11.1xd6.6
WASHER5 D11.1xd6.6	WASHER6 D11.1xd6.6
WASHER7 D11.1xd6.6	WASHER8 D11.1xd6.6
WASHER9 D11.1xd6.6	WASHER10 D11.1xd6.6

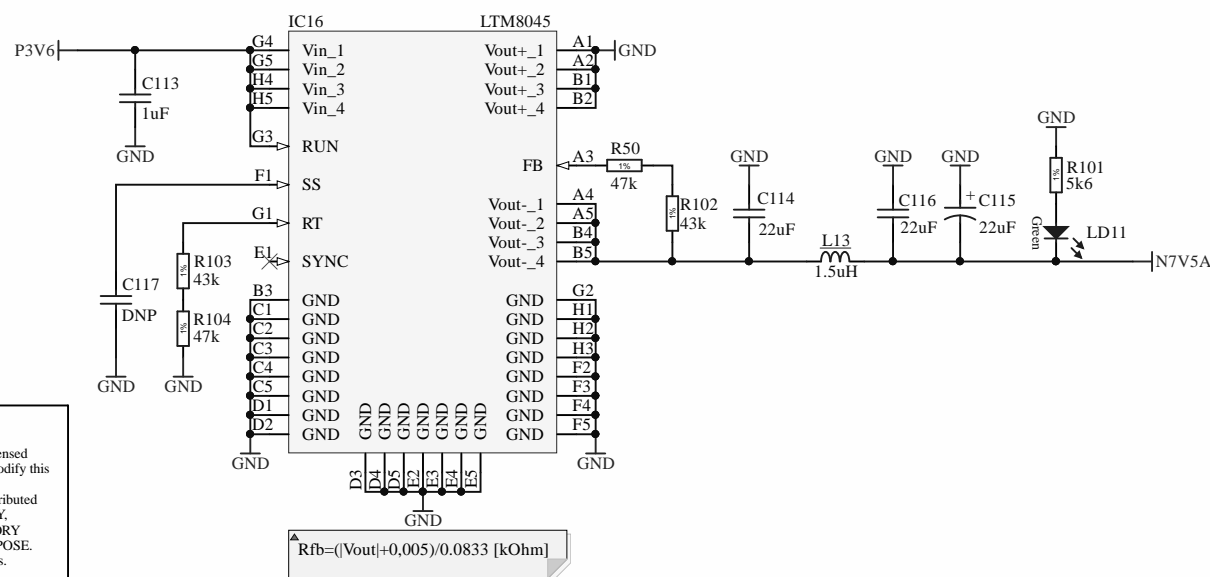
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File		Mirny.schdoc	-
Print Date		2018-12-03 17:52:58	Sheet 1 of 8
Warsaw University of Technology		ISE	ARTIQ
Nowowiejska 15/19			A3



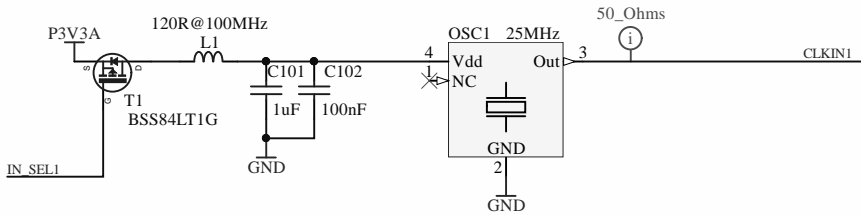
▲ Power budget (max ratings):	
P3V3:	
LVDS interface 4x	660
LVDS load 4x24mA	96
CPLD	100
ADF4351	$4 \times (27 + 36 + 80 + 26) = 676$
SY89855UMG	$4 \times (85) = 340$
TCXO	6
TOTAL P3V3	1878
TOTAL POWER	6,1974 W
P5V0:	
HMC542BLP4E	$4 \times 2,9 = 11,6$
HMC349LP4C	$4 \times 3,5 = 14$
TOTAL 5V0	25,6
TOTAL POWER	0,125 W
P7V0:	
ERA-4XSM+	$4 \times 85 = 340$
TOTAL 7V0	340
TOTAL POWER	2,38
DC/DC converter losses	
TPS62175 eff. 95	$0,05 \times (0,366) \times 7,5 = 0,137 \text{ W}$
LTM4622: 3.6V eff. 9	$0,1 \times 1,878 \times 3,6 = 0,676 \text{ W}$
LTM8045 eff. 8	$0,2 \times (4 \times 25) \times 3,6 = 0,72 \text{ W}$
LDO losses	
3.6V->3.3V	0,564 W
7.5V->5V	0,064 W
Total power from 12V	
Total power from 12V	10,5 W
Total current from 12V	0,875 A



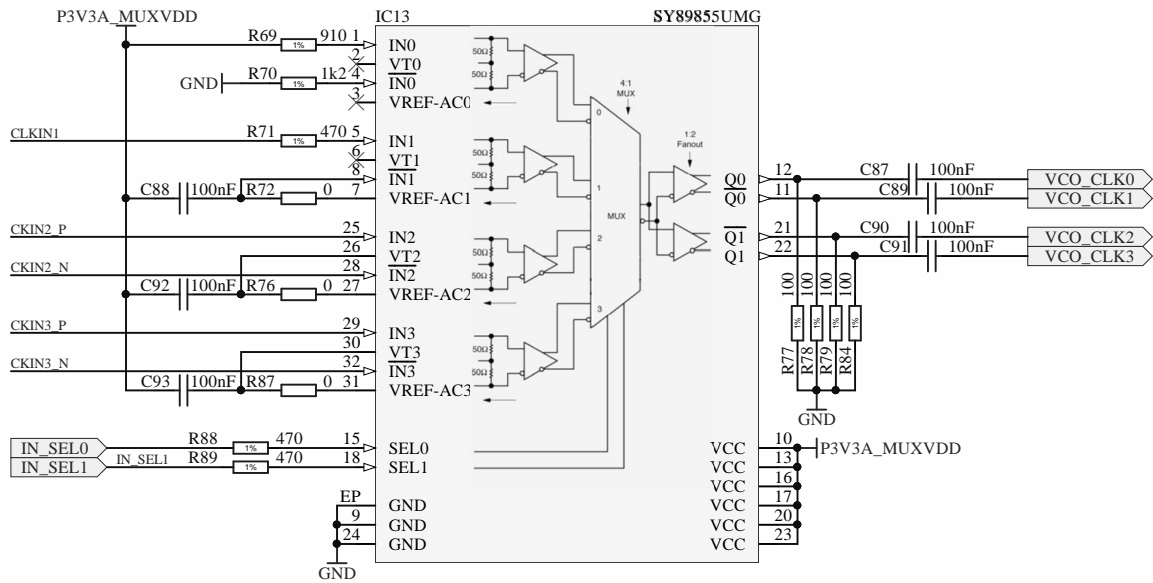
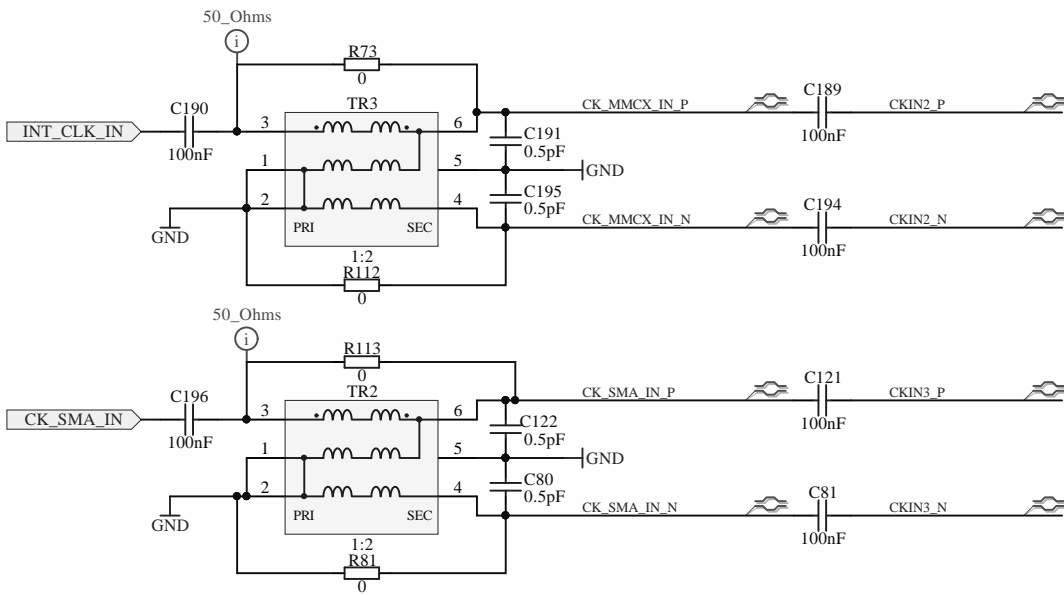
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Project/Equipment		ARTIQ/SINARA				
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			Drawn by	K.B.	XX/XX/XXXX	
			Check.by	-	-	
			Last Mod.	-	2018-12-03	
			File	Supply_VCO.SchDoc		
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Warsaw University of Technology Nowowiejska 15/19		ISE	ARTIQ		Sin A3	Re



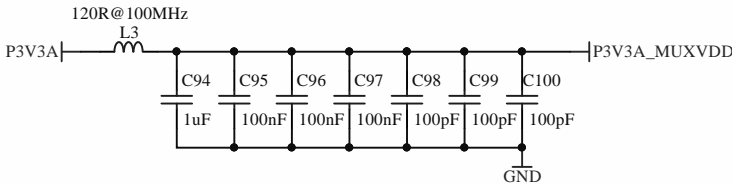
AC-Coupled Input Termination, Such as LVDS and LEVPECL



TRUTH TABLE

SEL1	SEL0	
0	0	IN0 Input Selected
0	1	IN1 Input Selected
1	0	IN2 Input Selected
1	1	IN3 Input Selected

-
XO
MMCX
SMA



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Print Date		2018-12-03 17:52:58	Sheet 3 of 8
Warsaw Univeristy of Technology Nowowiejska 15/19		ISE	ARTIQ
		Size	A3
		Rev	-

$RF_{OUT} = [INT + (FRAC/MOD)] \times (f_{PPD}/RF\ Divider)$
where:
 RF_{OUT} is the RF frequency output.
 INT is the integer division factor.
 $FRAC$ is the numerator of the fractional division (0 to MOD - 1).
 MOD is the preset fractional modulus (2 to 4095).
 $RF\ Divider$ is the output divider that divides down the VCO frequency.

$f_{PPD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))]$
where:
 REF_{IN} is the reference frequency input.
 D is the RF REF_{IN} doubler bit (0 or 1).
 R is the RF reference division factor (1 to 1023).
 T is the reference divide-by-2 bit (0 or 1).

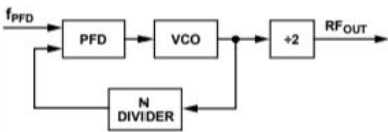
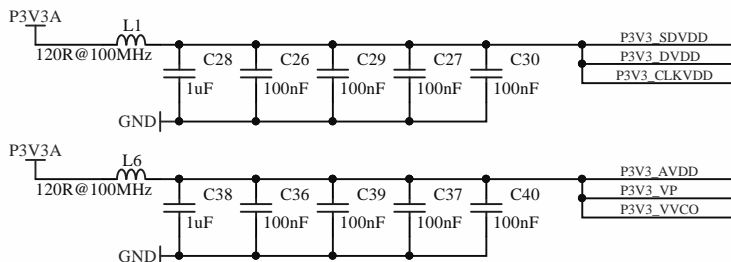
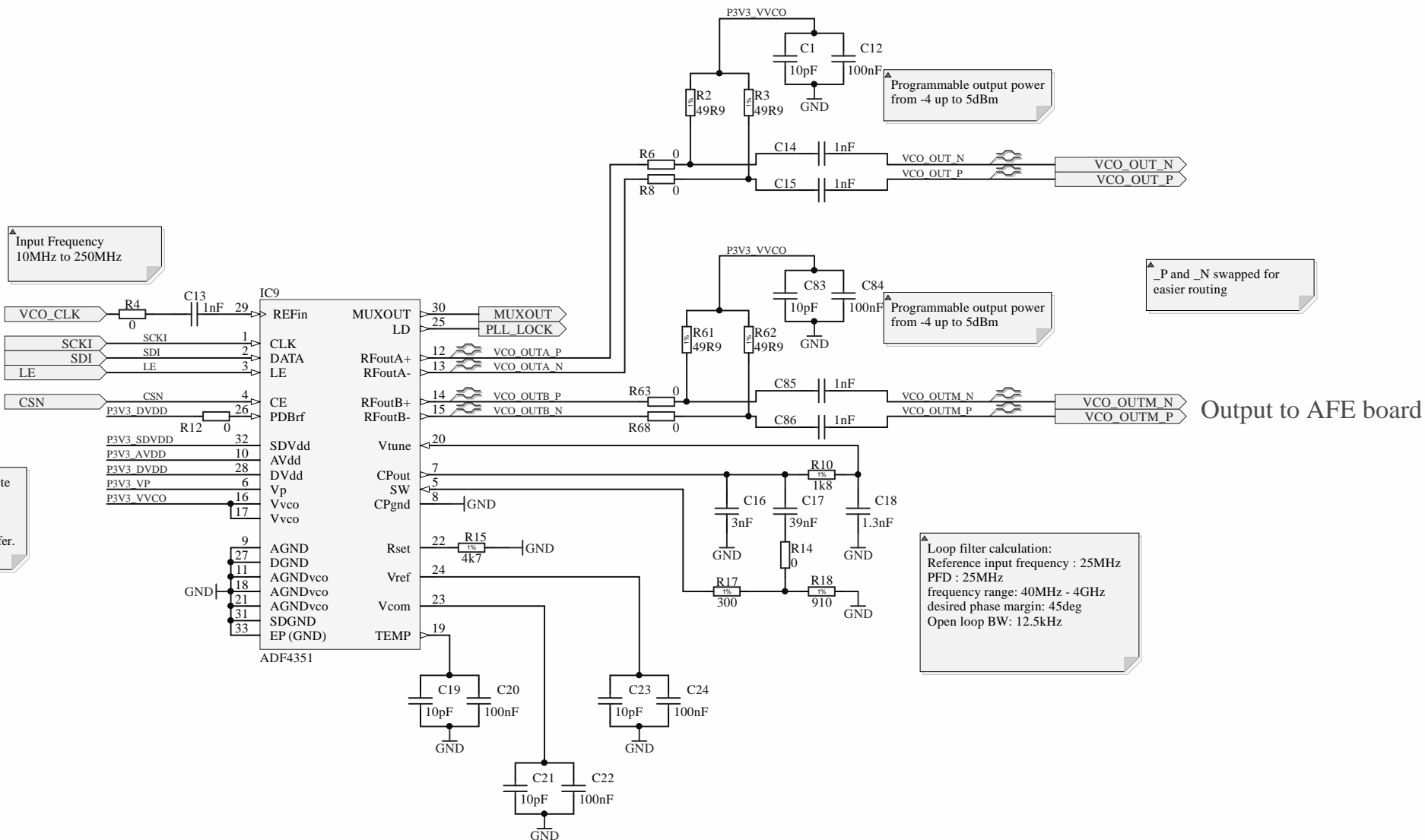


Figure 30. Loop Closed Before Output Divider

D = 0
T = 0
R = 1
MOD = 4000

Start Freq	Stop Freq	VCO Divider	Channel Spacing
40.0MHz	68.75MHz	64	97.656 Hz
68.75MHz	137.5MHz	32	195.31 Hz
137.5MHz	275MHz	16	390.63 Hz
275MHz	550MHz	8	781.25 Hz
550MHz	1.10GHz	4	1.5625kHz
1.10GHz	2.20GHz	2	3.125kHz
2.20GHz	4.00GHz	1	6.25kHz

After the fourth byte is written, the LE input should be brought high to complete the transfer.



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Warsaw University of Technology ISE		Print Date	2018-12-03 17:52:58
Nowowiejska 15/19		Sheet	4 of 8
		Size	A3
		Rev	-

ARTIQ

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom Filter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

Discrete-elemet filter with R57/59 & R58/C28

Mini-Circuits FV1206 filter

Jumper

Jumper

Digital Attenuator

F clk max = 30MHz

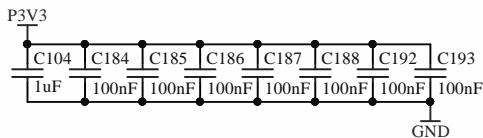
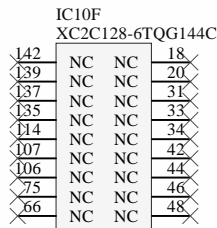
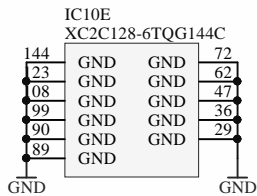
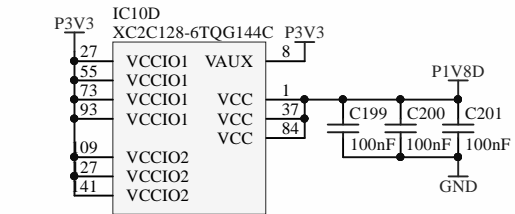
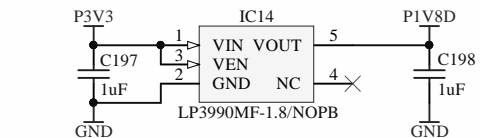
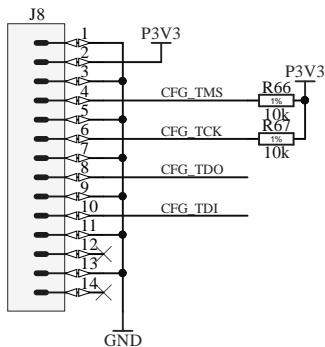
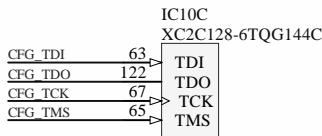
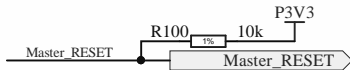
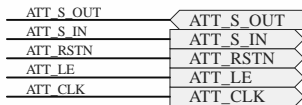
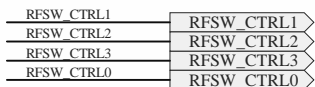
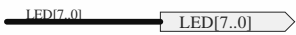
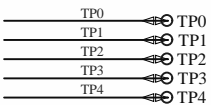
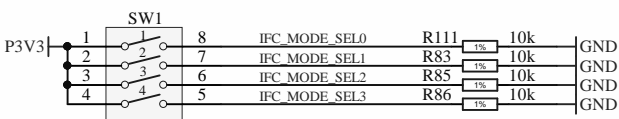
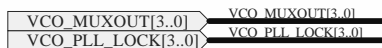
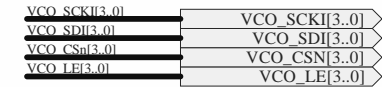
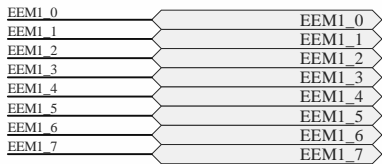
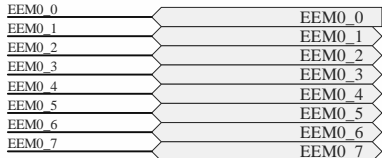
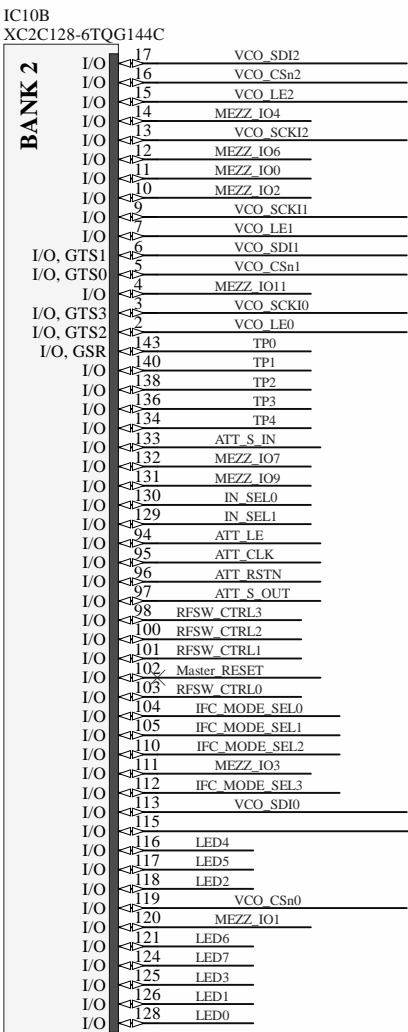
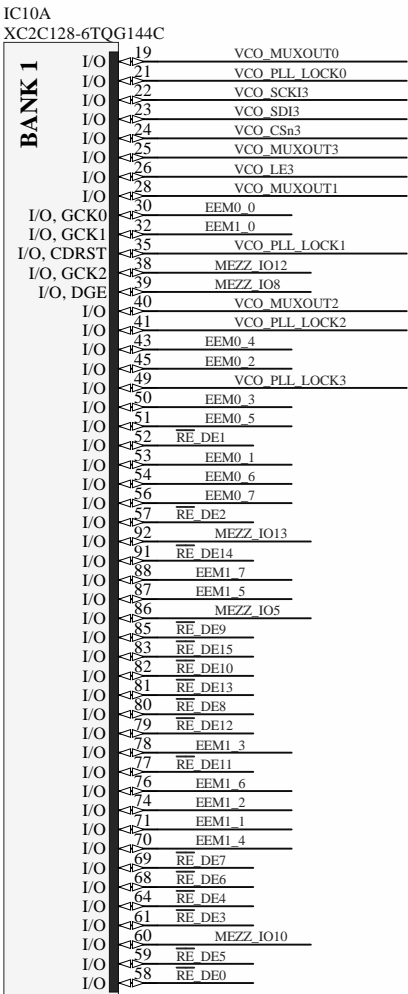
Amplifier
+13dB @ 2GHz typ.

SPDT switch

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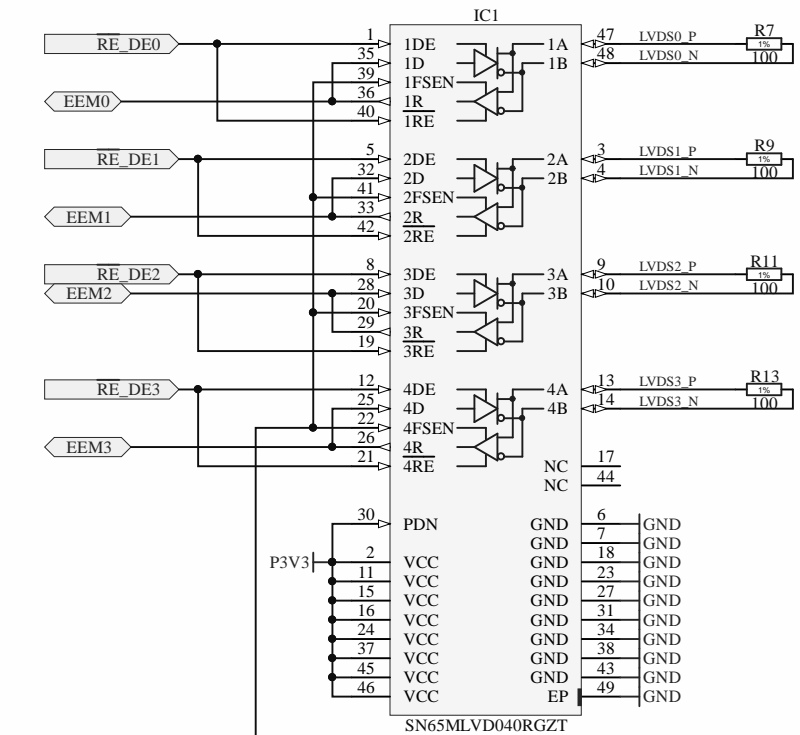
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Document		Designer K.B.	
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		Last Mod. - 2018-11-30	
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ARTIQ			
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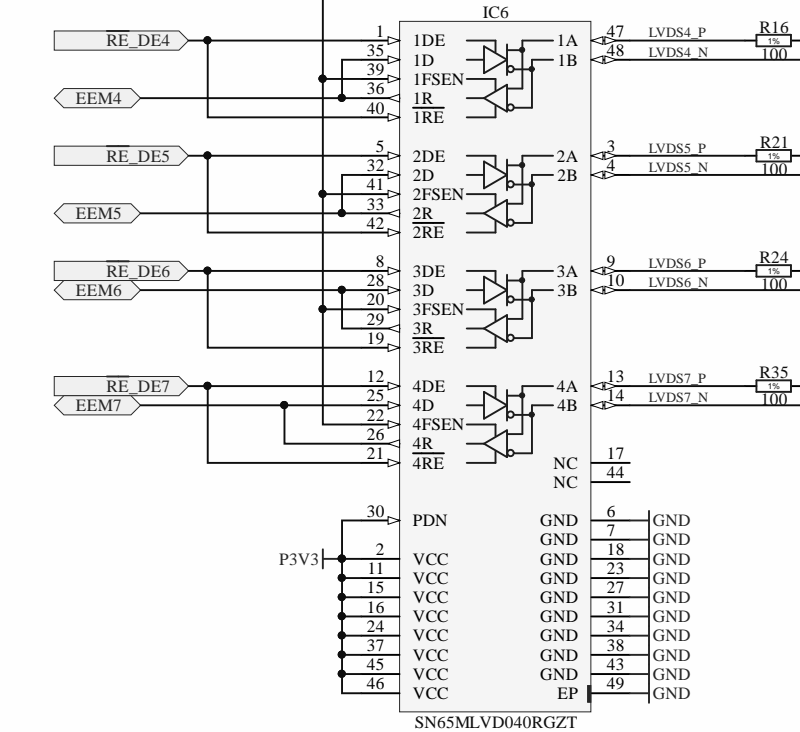
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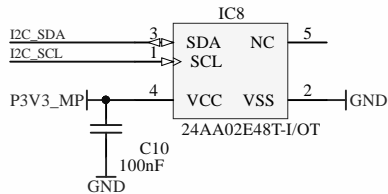
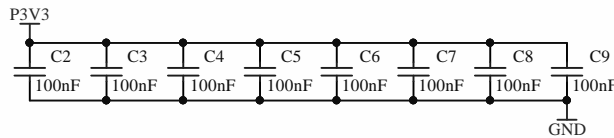
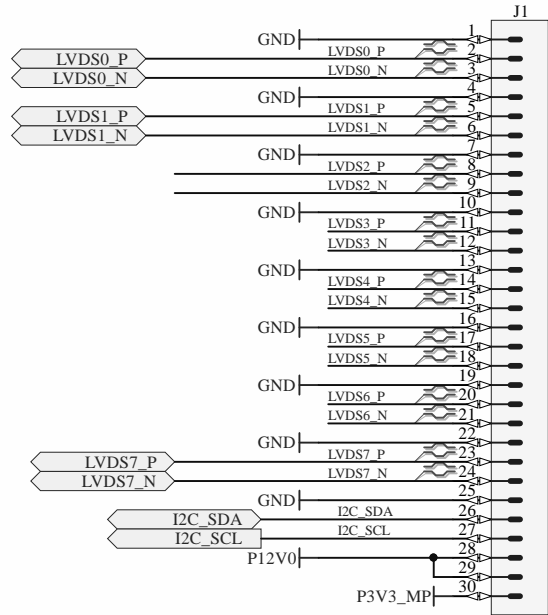
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		Sheet	6 of 8
		Size	A3
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FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output



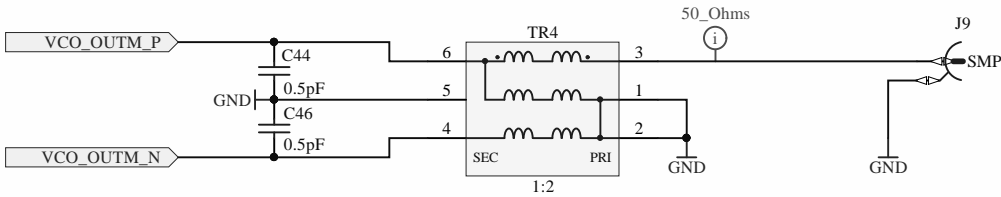
EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A



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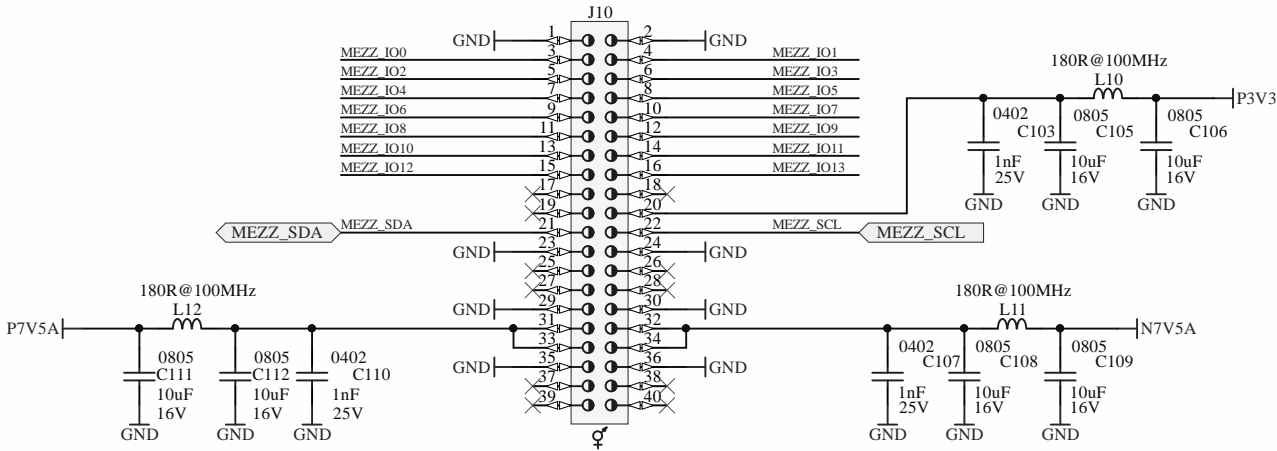
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Print Date		2018-12-03 17:52:59	Sheet 7 of 8
Warsaw Univeristy of Technology Nowowiejska 15/19		ISE	ARTIQ
		Size	A3
		Rev	-

Board-2-Board Analog Connectors



MEZZ_IO[13..0]

Board-2-Board Digital Connectors



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Warsaw Univeristy of Technology Nowowiejska 15/19		ISE	
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