This document describes Zynq Video Board Rev.1.2 connectors' pinouts.

General purpose buttons and LEDs

There are several buttons and LEDs which usage can be configured by the user. The table below shows their Mars ZX2 module and Zynq chip pin and ball assignment.

LED pin assignment

PCB desi gnator	ZX2 module pin (SO- DIMM)	ZX2 module signal name	Zynq-702 0 ball	FPGA pin name
LED1	44	IO_B34_L8_W14_P	W14	IO_L8P_34
LED2	46	IO_B34_L8_Y14_N	Y14	IO_L8N_34
LED3	48	IO_B34_L6_P14_P	P14	IO_L6P_34
LED4	50	IO_B34_L6_VREF_R14_N	R14	IO_L6N_VREF_34
LED5	54	IO_B34_L5_T14_P	T14	IO_L5P_34
LED6	56	IO_B34_L5_T15_N	T15	IO_L5N_34
LED7	69	IO_B34_L22_W18_P	W18	IO_L22P_34
LED8	71	IO_B34_L22_W19_N	W19	IO_L22N_34

General purpose buttons pin assignment

PCB desi gnator	ZX2 module pin (SO- DIMM)	ZX2 module signal name	Zynq-702 0 ball	FPGA pin name
SW1.U7	148	IO_MIO48_B13_L11_SRCC_U7	B12	PS_MIO48
SW2.U10	152	IO_MIO50_B13_L12_MRCC_T9	B13	PS_MIO50
SW3.V7	154	IO_MIO51_B13_L12_U10	B9	PS_MIO51
SW4.T9	150	IO_MIO49_B13_L11_V7	C12	PS_MIO49

Note: PCB button designators do not match Mars ZX2 signal names (see table).

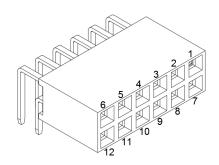
JTAG connector pinout



JTAG pin description

Signal name	Pin	Pin	Signal name
GND	1	2	+3V3
GND	3	4	JTAG_TMS
GND	5	6	JTAG_TCK
GND	7	8	JTAG_TDO
GND	9	10	JTAG_TDI
GND	11	12	NC
GND	13	14	SRST_RDYN

Digilent Pmod connectors



Digilent Pmod J6 connector pinout

Pin number	ZX2 module pin (SO- DIMM)	ZX2 module signal name	Zynq-70 20 ball	FPGA pin name
1	64	IO_B34_L24_P15_P	P15	IO_L24P_34
2	66	IO_B34_L24_P16_N	P16	IO_L24N_34
3	74	IO_B34_L16_V20_P	V20	IO_L16P_34
4	76	IO_B34_L16_W20_N	W20	IO_L16N_34
5	GND			
6	+3V3			
7	68	IO_B34_L23_N17_P	N17	IO_L23P_34
8	70	IO_B34_L23_P18_N	P18	IO_L23N_34
9	78	IO_B34_L15_T20_P	T20	IO_L15P_34
10	80	IO_B34_L15_U20_N	U20	IO_L15N_34
11	GND			
12	+3V3			

Digilent Pmod J7 connector pinout

Pin number	ZX2 module pin (SO- DIMM)	ZX2 module signal name	Zynq-70 20 ball	FPGA pin name
1	43	IO_B34_L13_MRCC_N18_P	N18	IO_L13P_MRCC_34
2	45	IO_B34_L13_MRCC_P19_N	P19	IO_L13N_MRCC_34
3	55	IO_B34_L10_V15_P	V15	IO_L10P_34
4	57	IO_B34_L10_W15_N	W15	IO_L10N_34
5	GND			
6	+3V3			
7	49	IO_B34_L14_SRCC_N20_P	N20	IO_L14P_SRCC_34
8	51	IO_B34_L14_SRCC_P20_N	P20	IO_L14N_SRCC_34
9	59	IO_B34_L7_Y16_P	Y16	IO_L7P_34
10	61	IO_B34_L7_Y17_N	Y17	IO_L7N_34
11	GND			
12	+3V3			

MIPI-CSI connector pinout

The Zynq Video Board supports two 2-lane CSI-MIPI interfaces broken-out on FPC connector.

MIPI CSI connector pinout

Pin nu mber	ZVB signal name	ZX2 m odule pin (S O-DIM M)	ZX2 module signal name	Zynq-7 020 ball	FPGA pin name
1	+5V0				
2	+5V0				
3	+3V3				
4	+3V3				
5	NC				
6	NC				
7	NC				
8	NC				
9	I2C_1_SCL_2V8	84	IO_B35_L23_M14_P	M14	IO_L23P_35
10	I2C_1_SDA_2V8	86	IO_B35_L23_M15_N	M15	IO_L23N_35
11	I2C_0_SCL_2V8	97	IO_B35_L10_AD11_K19_P	K19	IO_L10P_AD11P_35
12	I2C_0_SDA_2V8	99	IO_B35_L10_AD11_J19_N	J19	IO_L10N_AD11N_35
13	NC				

14	NC				
15	NC				
16	NC				
17	NC				
18	GPIO	134	IO_B35_L6_VREF_F17_N	F17	IO_L6N_VREF_35
19	NC				
20	NC				
21	GND				
22	CSI1_CLK_P				
23	CSI1_CLK_N				
24	GND				
25	CSI1_D0_P				
26	CSI1_D0_N				
27	CSI1_D1_P				
28	CSI1_D1_N				
29	NC				
30	NC				
31	NC				
32	NC				
33	GND				
34	NC				
35	NC				
36	GND				
37	NC				
38	NC				
39	GND				
40	CSI2_CLK_P				
41	CSI2_CLK_N				
42	GND				
43	CSI2_D0_P				
44	CSI2_D0_N				
45	CSI2_D1_P				
46	CSI2_D1_N				
47	NC				
48	NC				
49	NC				
50	NC				

Testpad list

Testpad list

Designator	Side	Description
GND	top	GND
TP1	top	CAM1_PWDN signal
TP4	top	CAM2_PWDN signal
TP5	bottom	VOUT_1V8 signal
TP6	bottom	Mars ZX2 SO-DIMM pin 123
TP7	bottom	Mars ZX2 SO-DIMM pin 65
TP11	bottom	GND