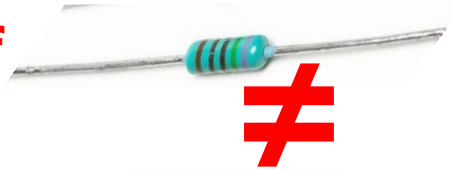
# IC Fab. Tech. OUTLINE

- Thin Film Formation
- Photolithography and Ecthing
- Doping
- IC Resistor
- Sheet Resistance
- Diode
- **nMOSFET: Process Flow**
- **nMOSFET: Fab. and Layout**
- **nMOSFET: Layout Rules**

# The Design of a Resistor

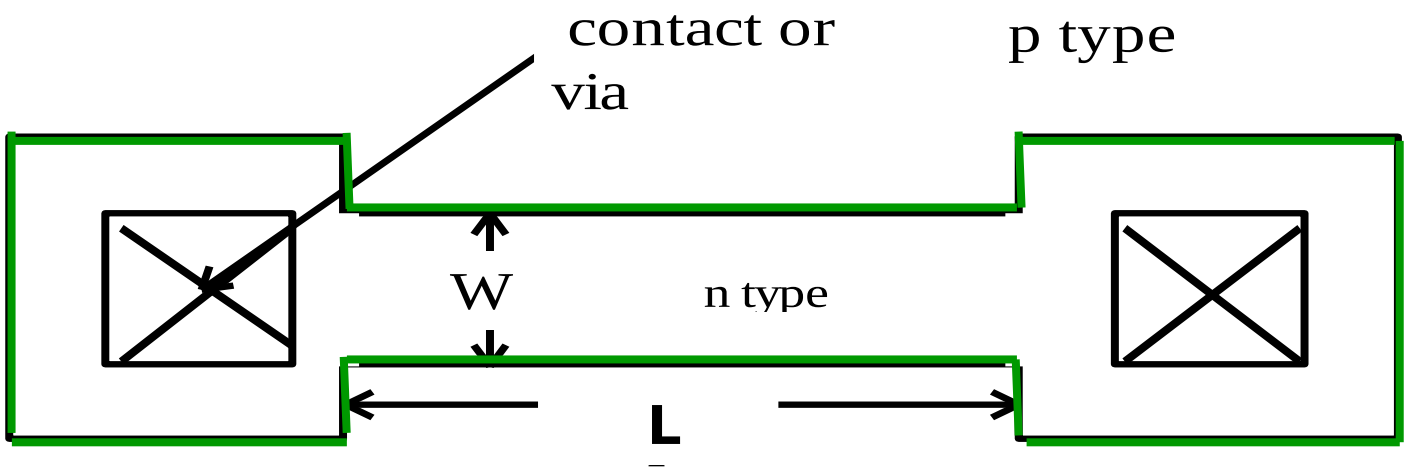
**$R_s = \rho / t$ is called the sheet resistance.**

**Example: if we need a resistance of 1K and the sheet resistance is $R_s = 200\Omega/\square$, design its layout.**



$\neq$

$R = R_s(L/W)$



# The Design of a Resistor

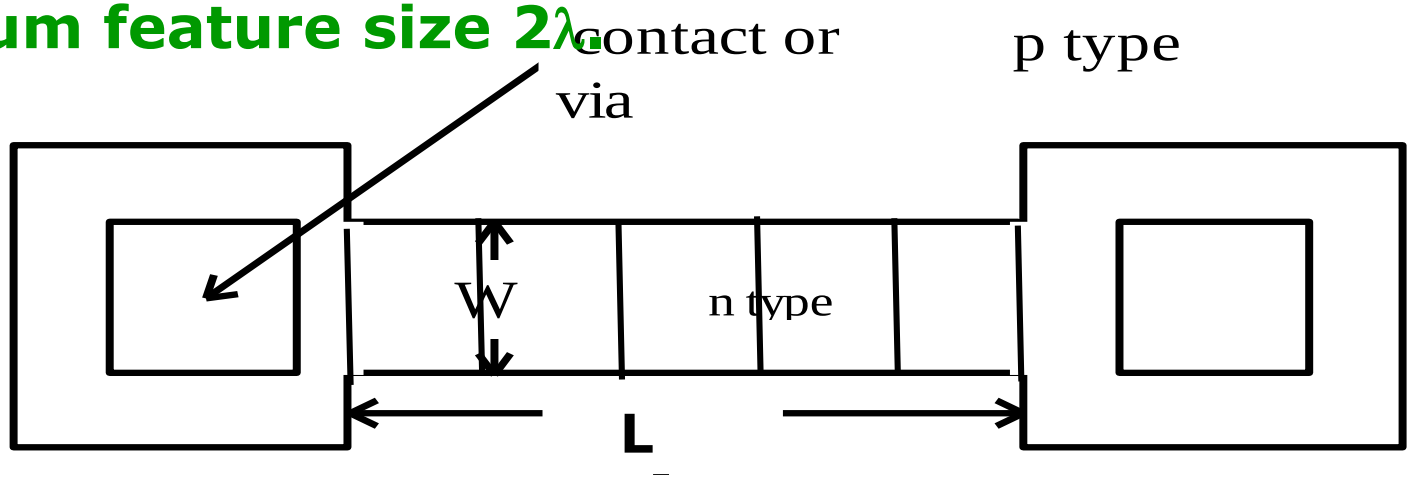
**Rs=ρ/t is called the sheet resistance.**

**Example: if we need a resistance of 1K and the sheet resistance is Rs=200Ω/□, we need 5 squares (L/W=5).**

**≠**

**R=Rs(L/W)**

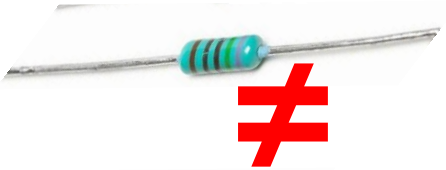
**Normally each square will be the minimum feature size 2λ.**



# The Design of a Resistor

**Rs=ρ/t is called the sheet resistance.**

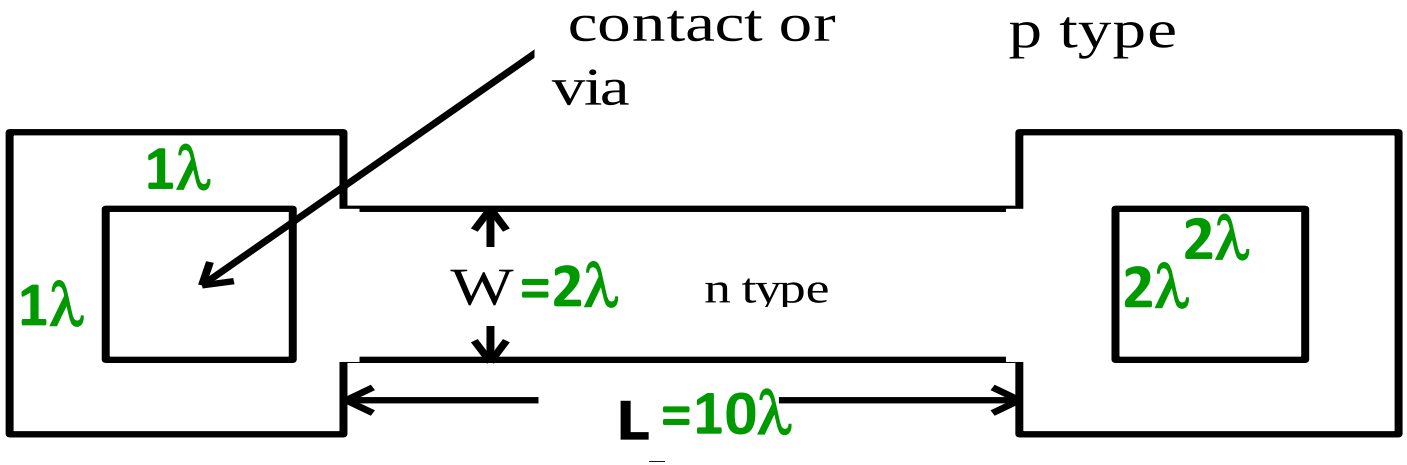
**Example: if we need a resistance of 1K and the sheet resistance is Rs=200Ω/□, we need 5 squares.**



**≠**

**R=Rs(L/W)**

**Normally each square will be the minimum feature size 2λ.**



# IC Fabrication Techniques

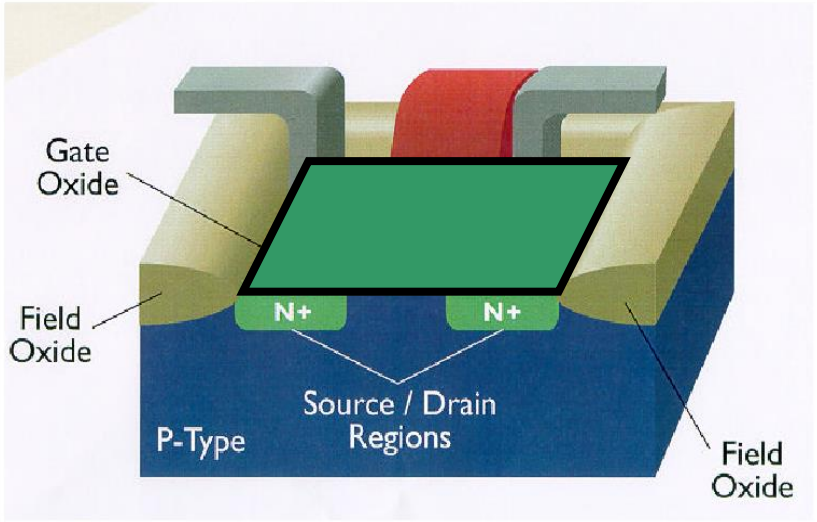
## nMOSFET Fab.: OUTLINE

- **nMOSFET: Process Flow**
- **nMOSFET: Layout Rules**

Lecture 10: Reference Reading

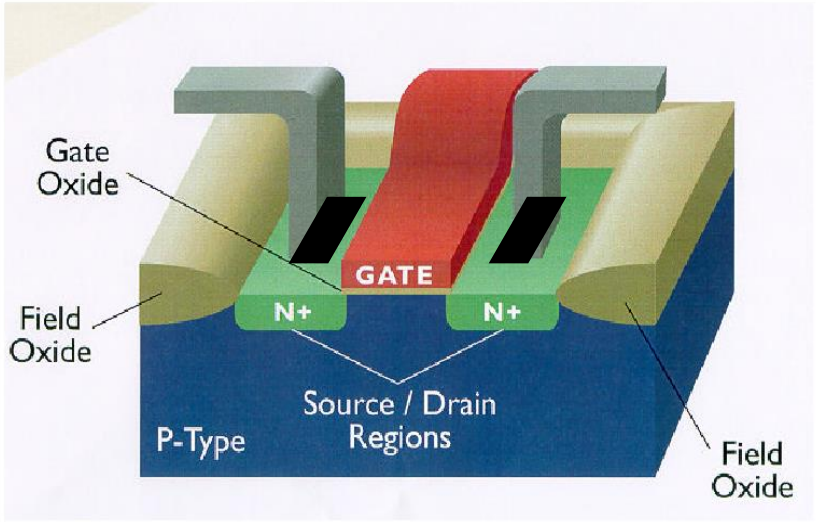
Chapter 4.3.1

# Process Flow: nMOSFET

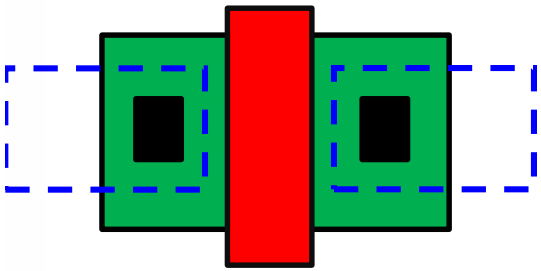



**Mask 1: Active region**

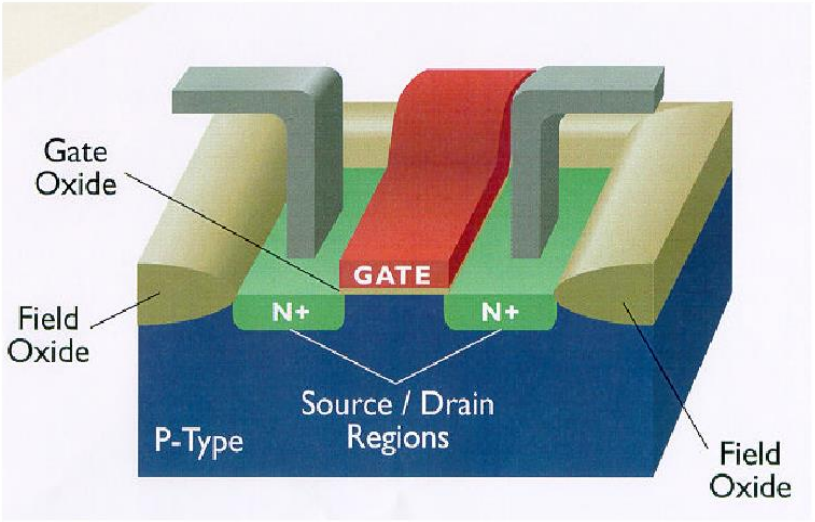
# Process Flow: nMOSFET



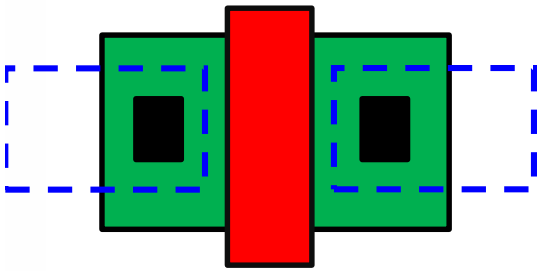

**Active region**



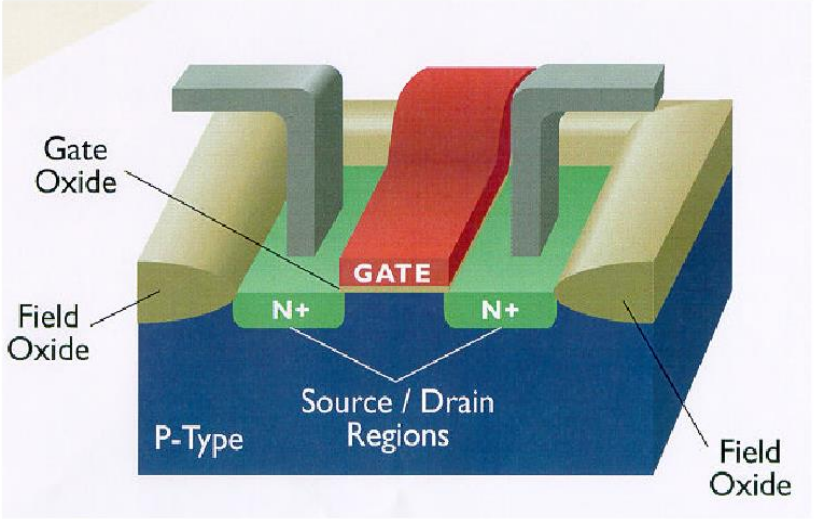
# Process Flow: nMOSFET



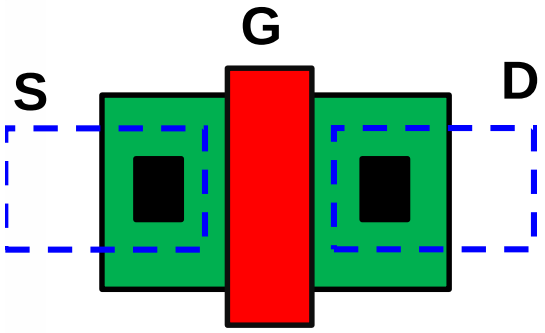

**Active region**



# Process Flow: nMOSFET



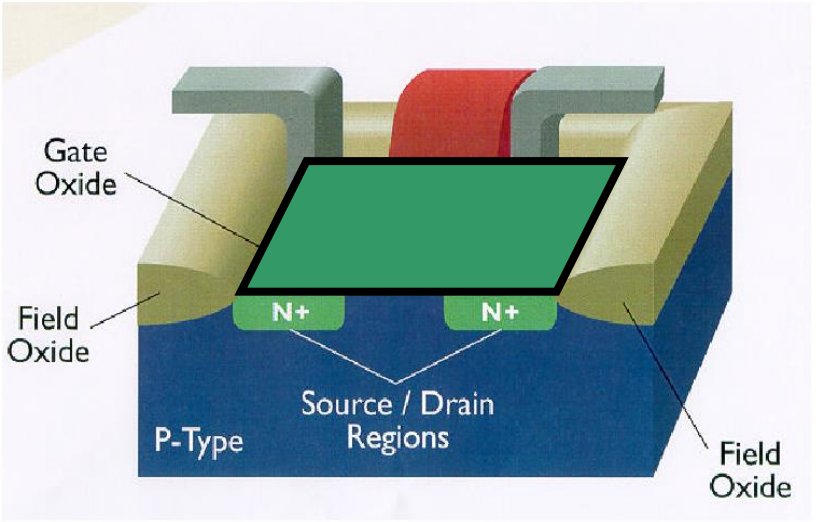

**Active region**



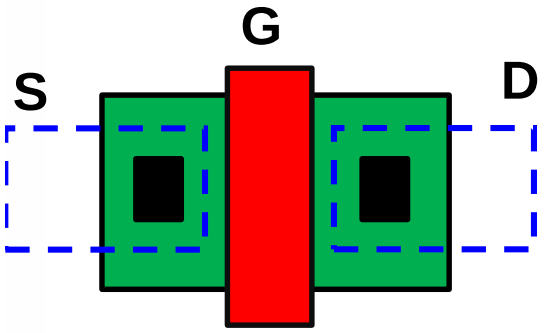

**Layout(版图)**

# Process Flow: nMOSFET

Si Substrate (p)




**Active region**




**Layout(版图)**

# Process Flow: nMOSFET

Si Substrate (p)

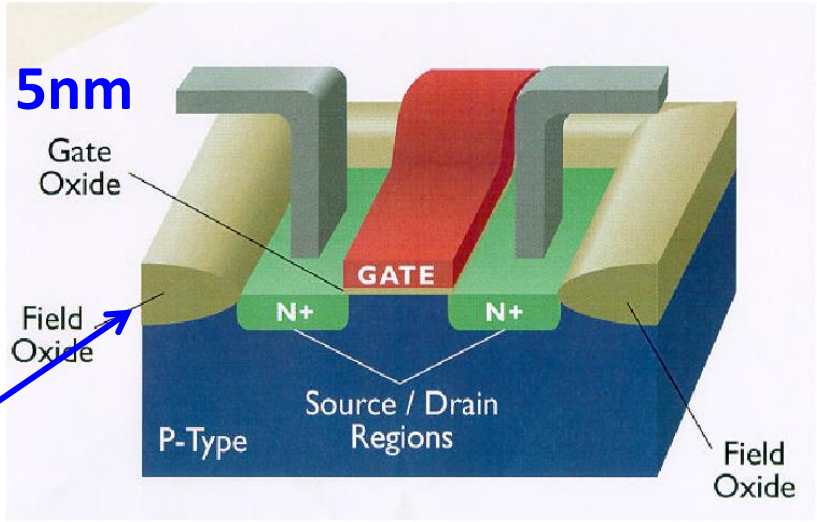
Oxidation (Layer

**Oxide 1**

$SiO_2$ Field Oxide (Thick Oxide)

**~ 500nm**

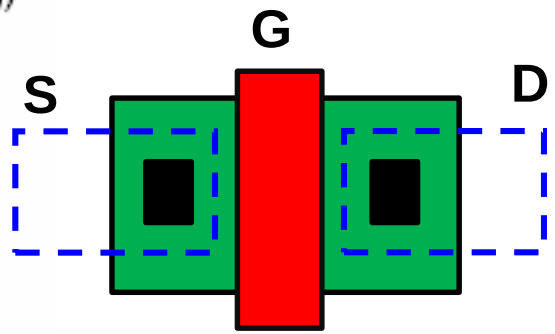
**~ 5nm**




**Mask 1: Active region**

**Mask 1**

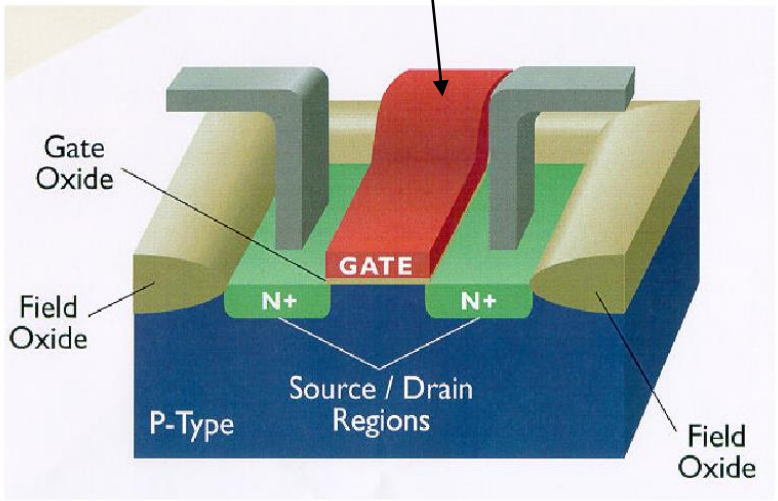
Oxide etching (Patterning)

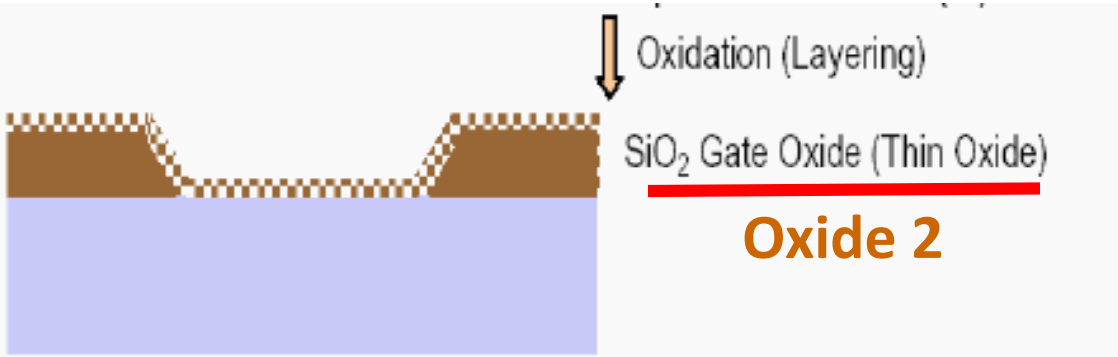



**Layout(版图)**

# Process Flow: nMOSFET

**Mask 2: Gate**

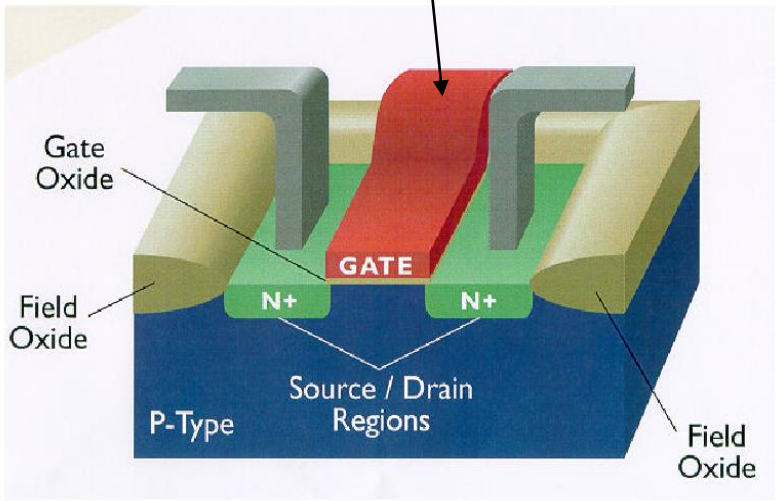


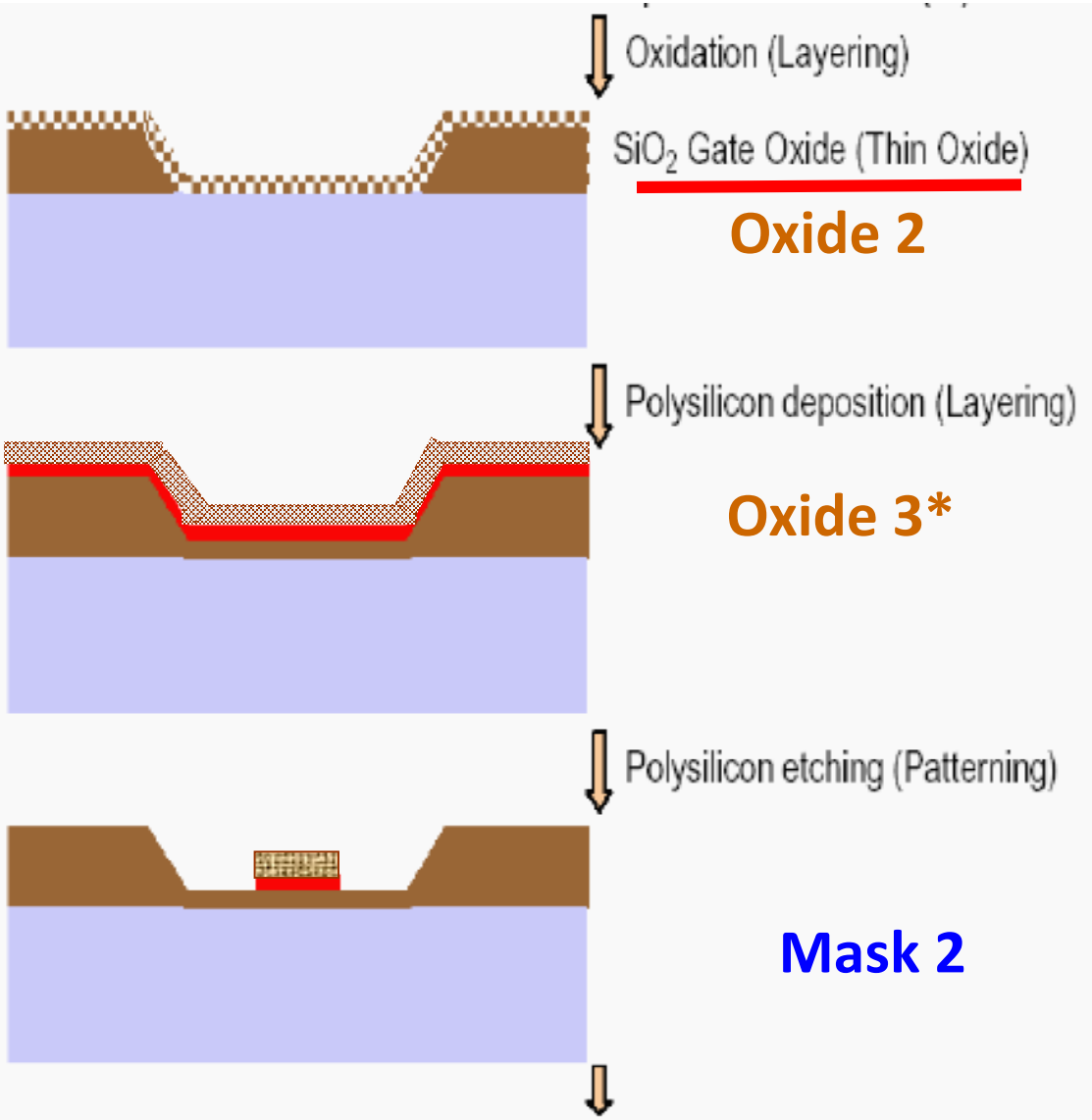




*** normally, photoresist only**

# Process Flow: nMOSFET

**Mask 2: Gate**

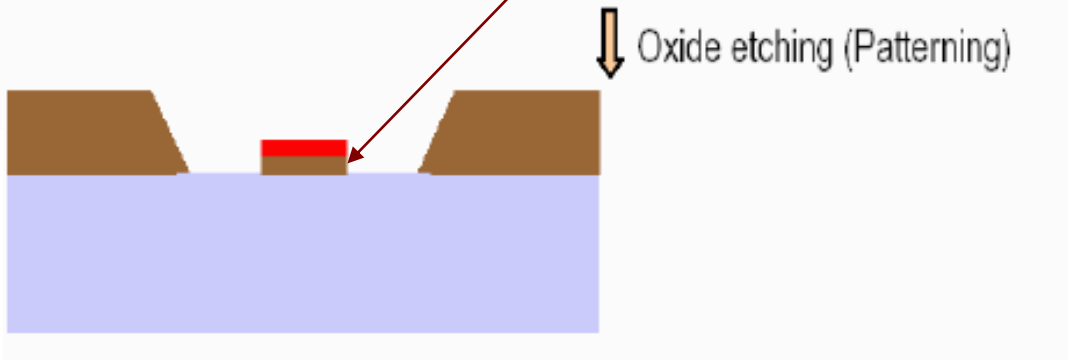


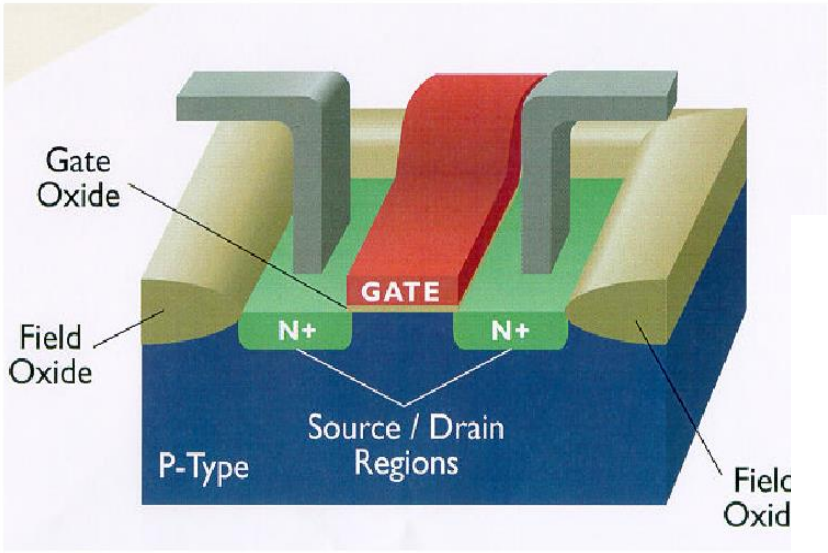




*** normally, photoresist only**

# Process Flow: nMOSFET

**Keep gate oxide**



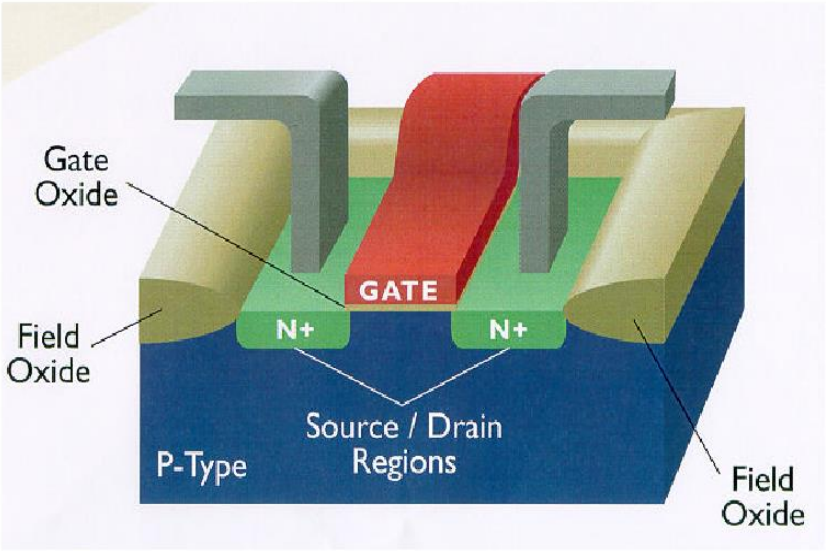




**Gate becomes n+ type.**

*Normally need new mask for n+.

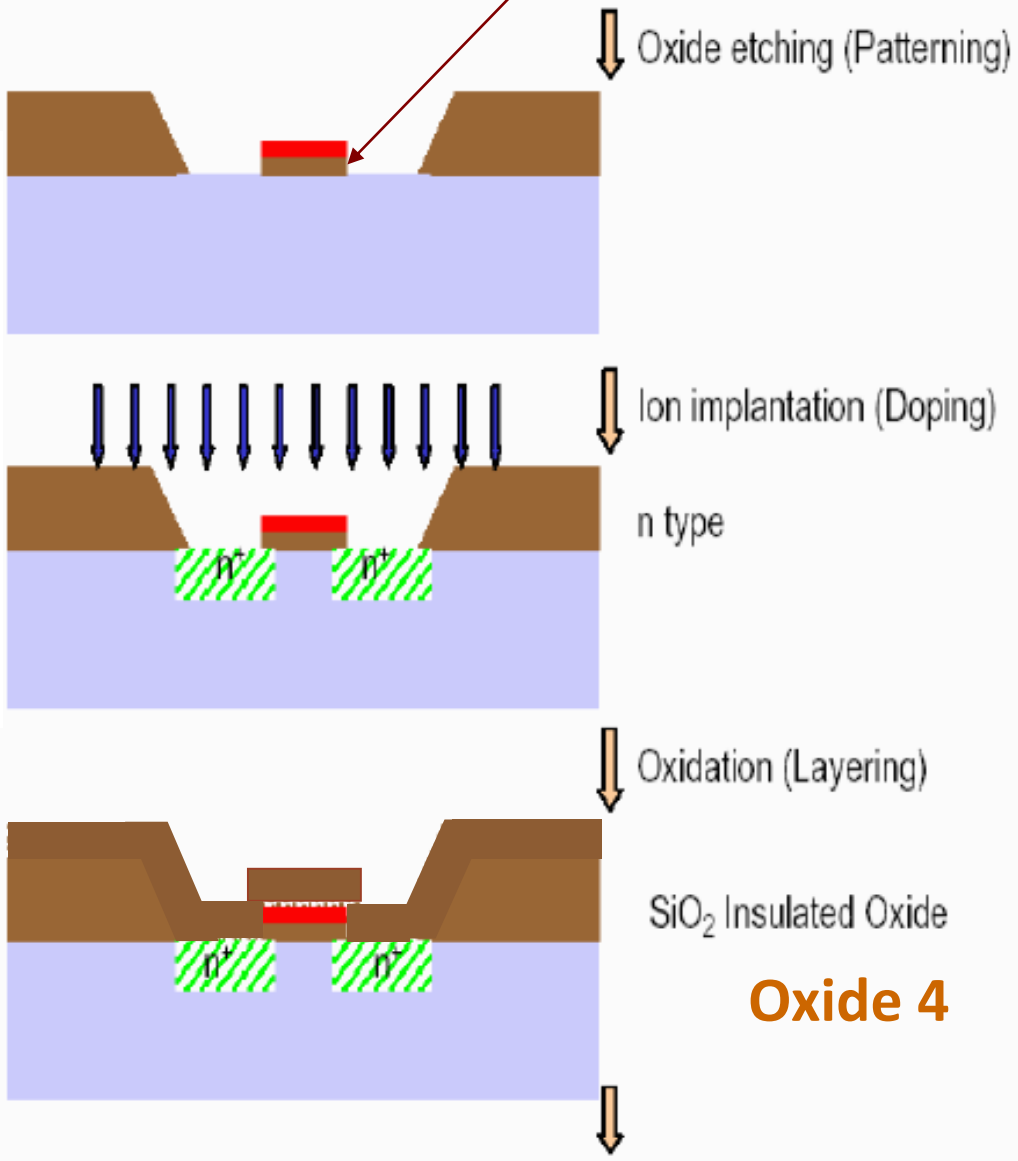
# Process Flow: nMOSFET

**Keep gate oxide**




**Gate becomes n+ type.**

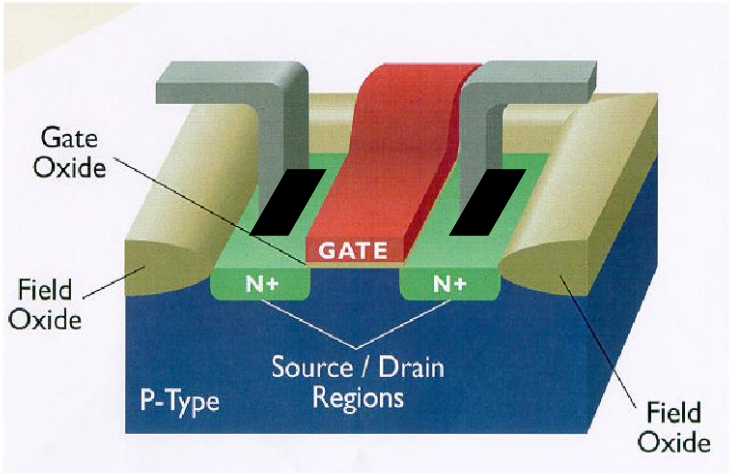
*Normally need new mask for n+.




**Oxide 4**

# Process Flow: nMOSFET

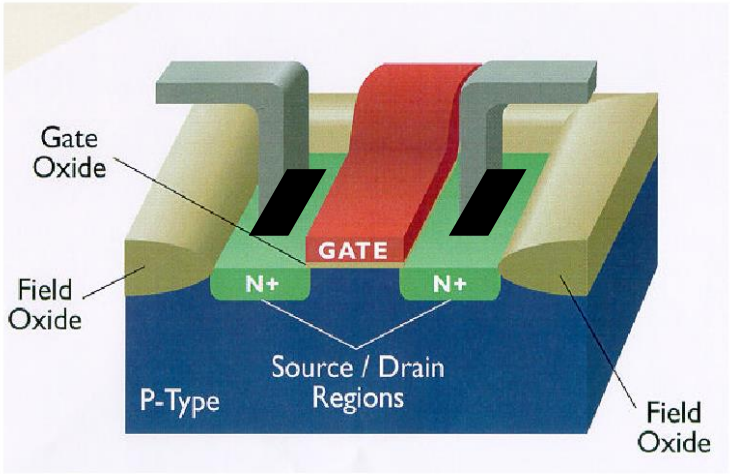
**Mask 3: contacts**

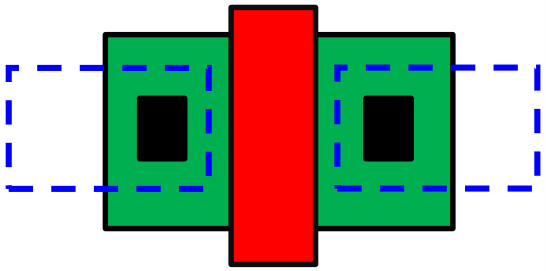


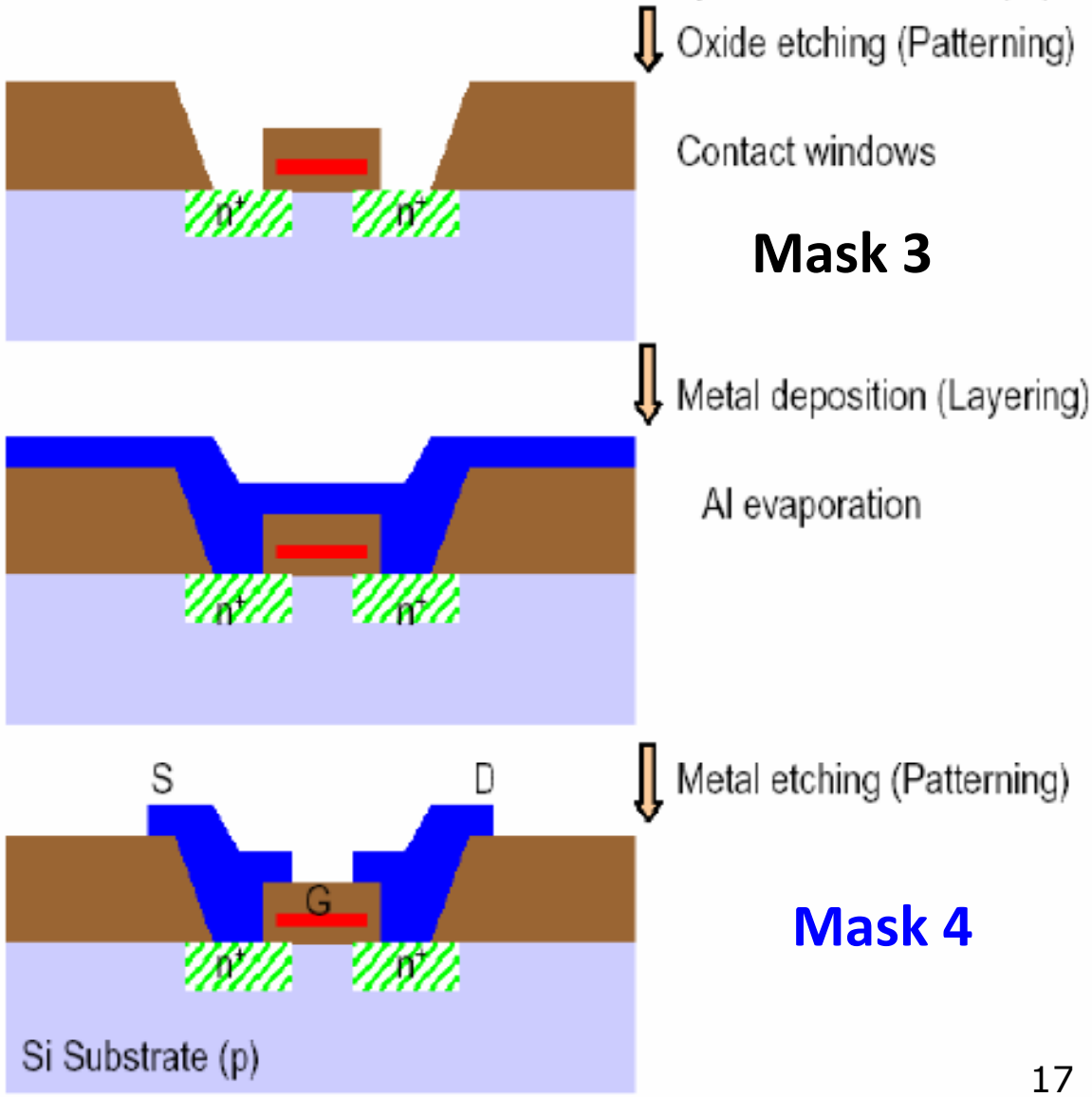

**Mask 4: metal lines**

# Process Flow: nMOSFET

**Mask 3: contacts**





# IC Fabrication Techniques

## nMOSFET Fab.: OUTLINE

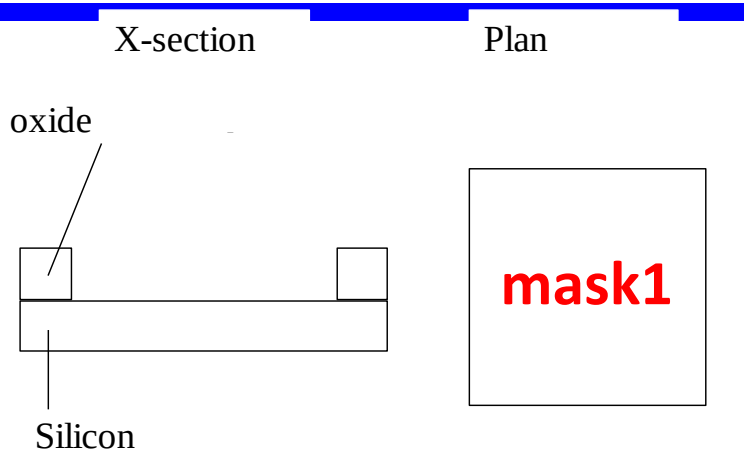
- nMOSFET: Process Flow
- **nMOSFET: Fab. and Layout**
- nMOSFET: Layout Rules

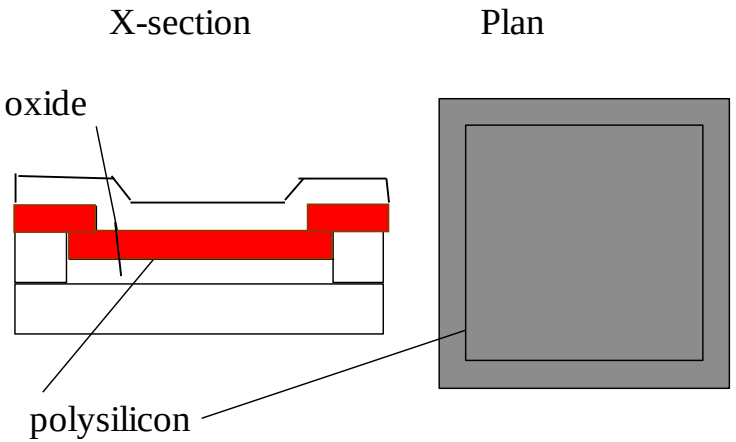
Lecture 10: Reference Reading

Chapter 4.3.1

# Fabrication of an MOS transistor-1

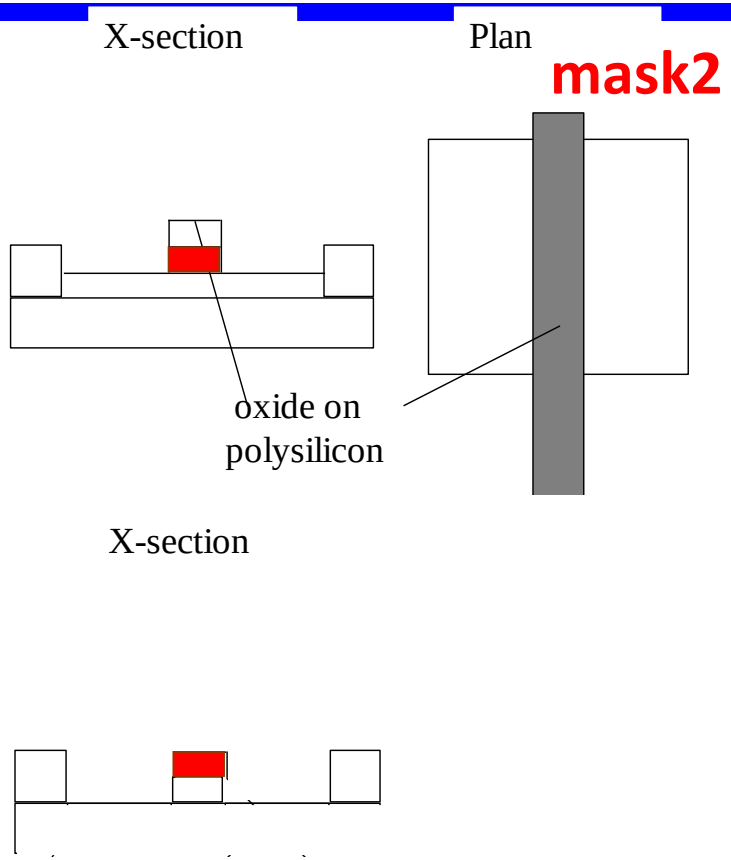
- The cleaned Si slice is oxidised (**oxide1**) and a window is opened in the oxide (**mask1**). The sides of the mask 1 must be equal in size to a multiple of the minimum feature size.
- The slice of silicon is re-oxidised (**oxide2**), which fills the window with new thinner oxide and then polycrystalline silicon covers the entire surface.
- The following is: an oxide (**oxide3***) is grown on the polysilicon.



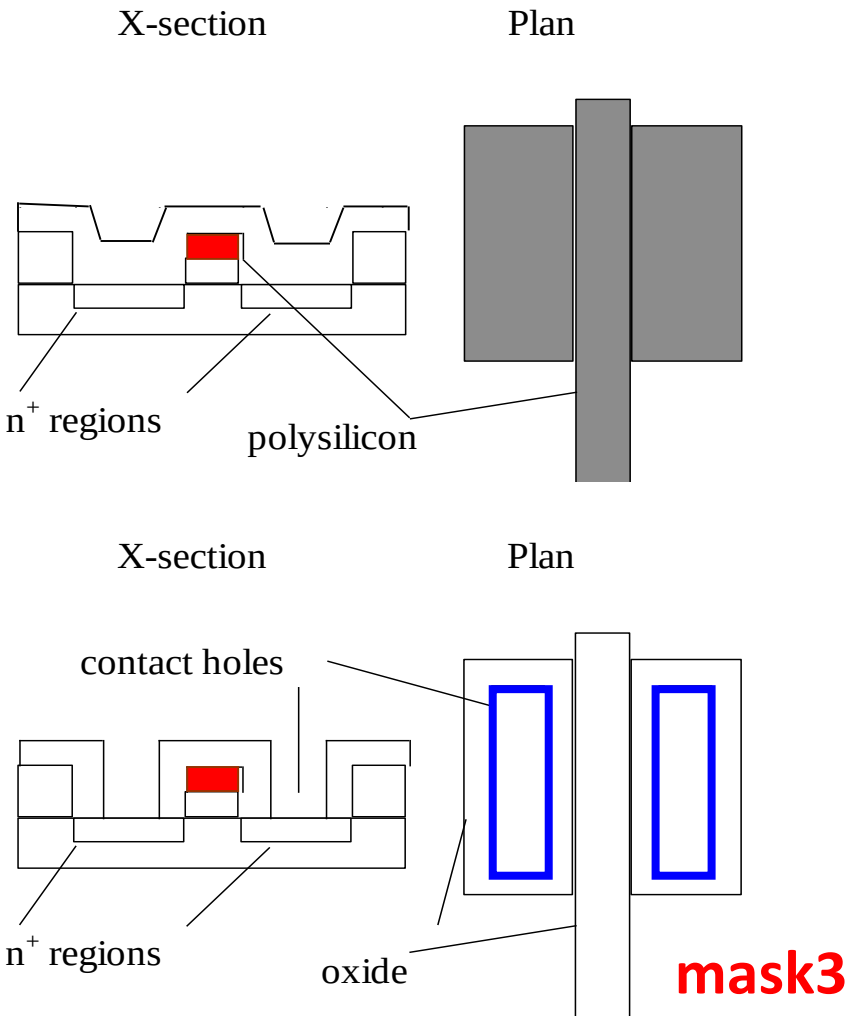
# Fabrication of an MOS transistor-2

- The oxide and polysilicon are photoengraved in the shape of the gate stripe after which it acts as a mask (**mask2)** for the etching of the polysilicon gate electrode. Note that resist cannot be used for this as it is unable to sustain the chemical attack of the poly etchants.
- For the smallest device the stripe will have a width equal to the minimum feature size. The stripe will have to overlap the ends of the rectangle.
- The oxide is etched from the source and drain regions and it is also removed from the surface of the poly. The implant creates the source and drain regions and dopes the polysilicon to make it very conducting.



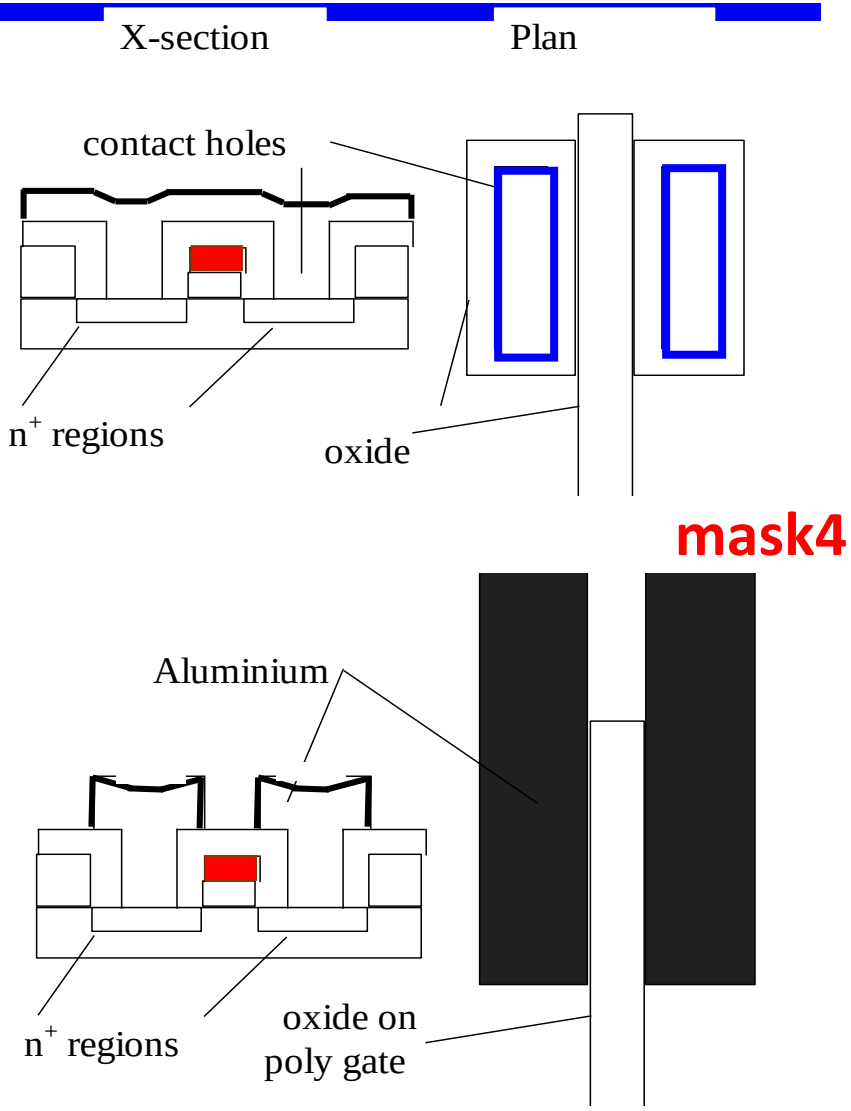
# Fabrication of an MOS transistor-3

- Oxide is deposited on the surface (**oxide4**) and the contact or via holes are opened (**mask3)**. Each of these holes must have dimensions that are equal to the minimum feature size (or a multiple of it).
- They must be at least a minimum alignment error from the gate or the edge of the implant.
- A contact to the gate must be made away from the device and that must be made on a widened part of the stripe so that this contact hole is a square with sides equal to a minimum feature size and a distance equal to the maximum alignment error from the edge of the poly.



# Fabrication of an MOS transistor-4

- Aluminium is evaporated to cover the whole slice and is then covered with photoresist.
- Al is patterned into the shape of the conductor patterns across the chip (**mask4)**. It makes contact to the source and drain down the contact holes.
- The width of the aluminium stripes must cover the contact holes with an allowance on either side of an amount equal to the minimum alignment accuracy.
- As shown in the adjacent diagram the source and drain aluminium appears to be touching the gate poly. This is not so because the oxide on the poly gives insulation.



# IC Fabrication Techniques

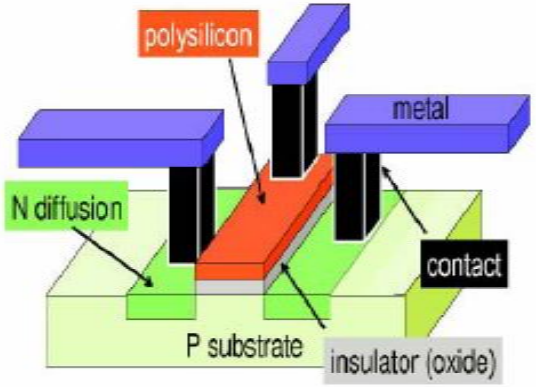
## nMOSFET Fab.: OUTLINE

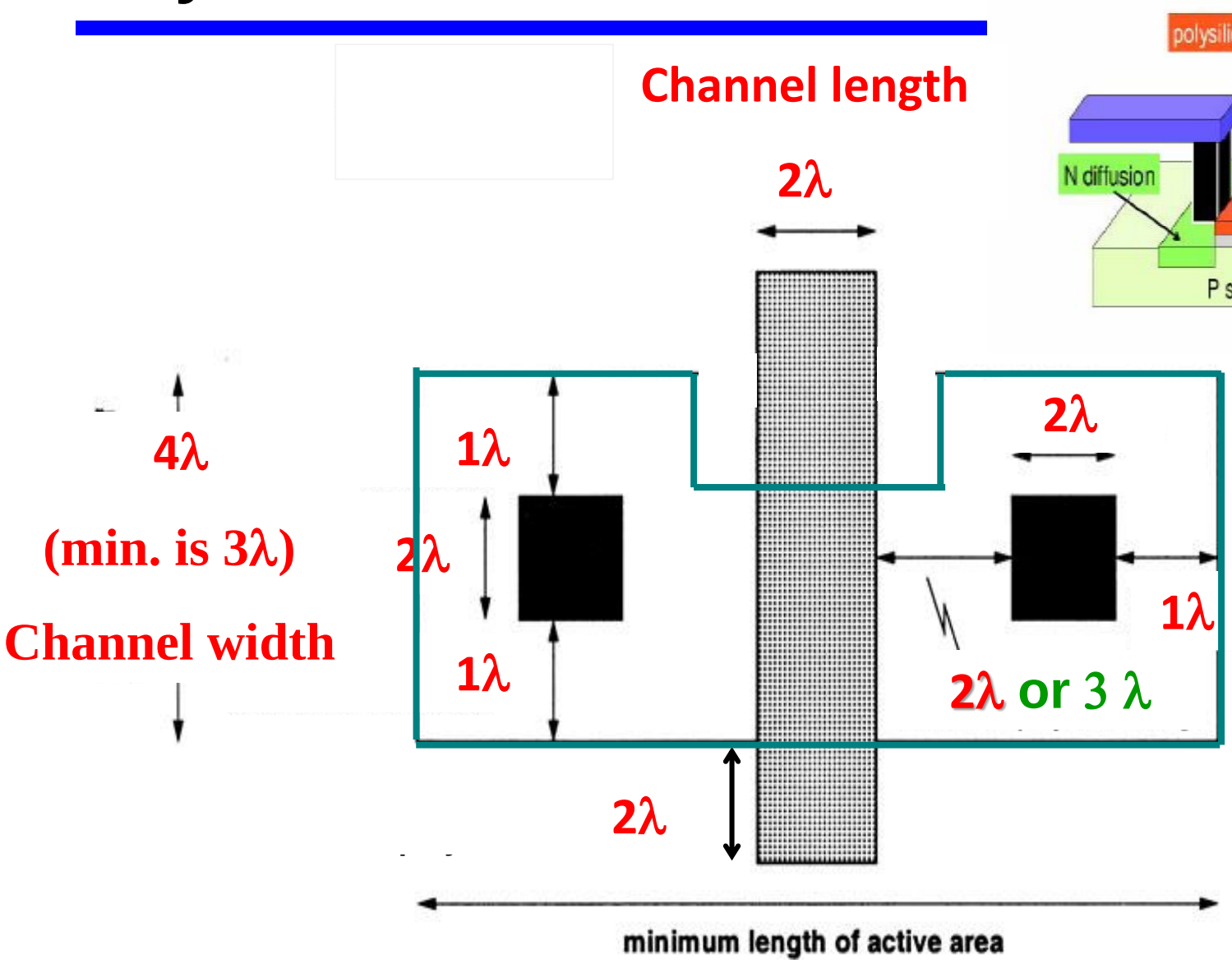
- nMOSFET: Process Flow
- nMOSFET: Fab. and Layout
- **nMOSFET: Layout Rules**

Lecture 10: Reference Reading

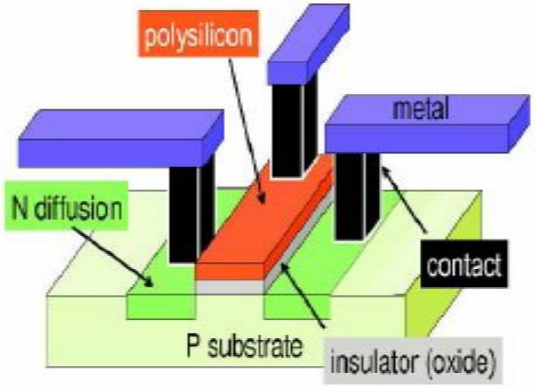
Chapter 6 + Handout + www

# Layout rules to minimise MOST size



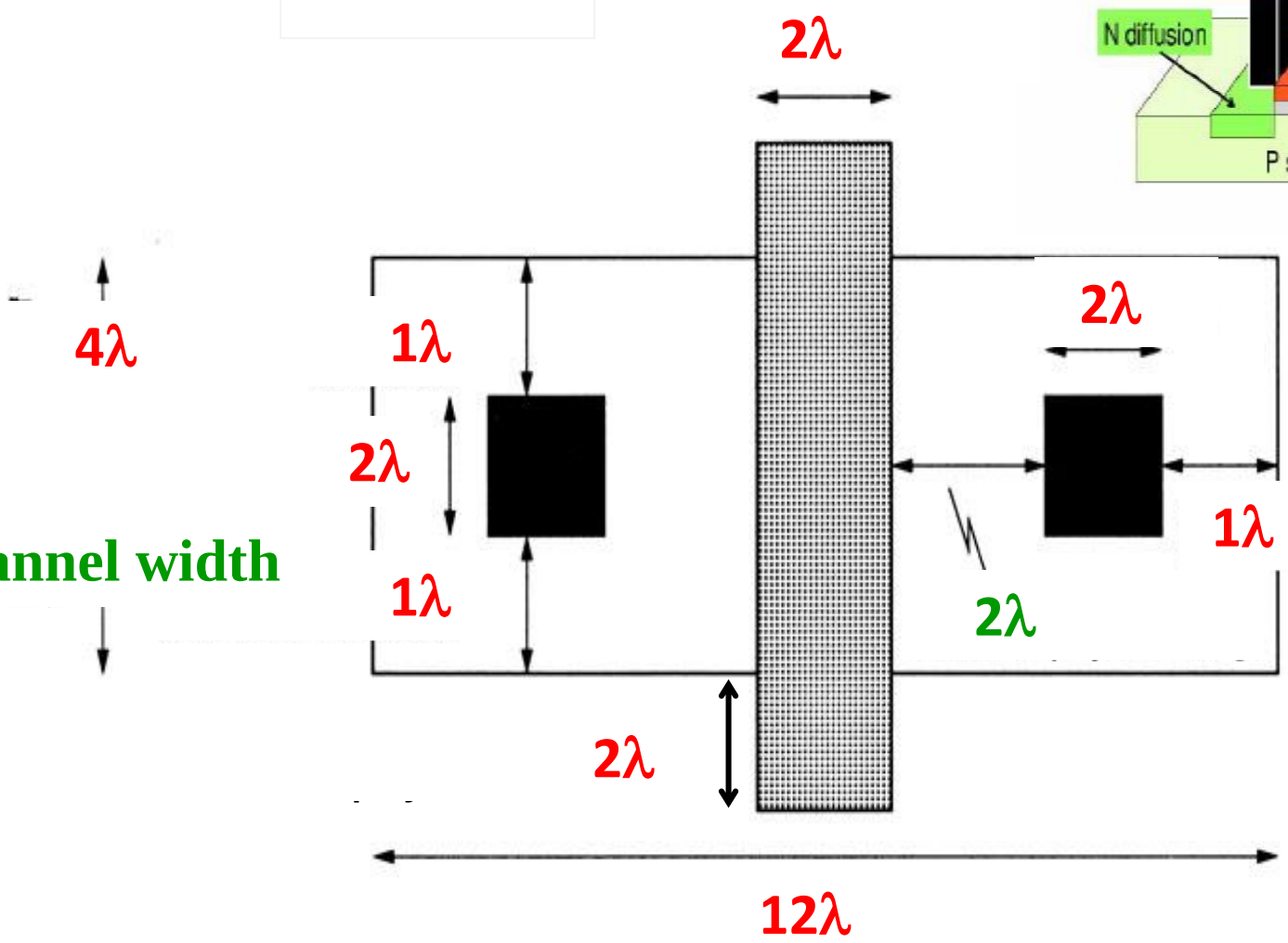



# Layout rules to minimise MOST size

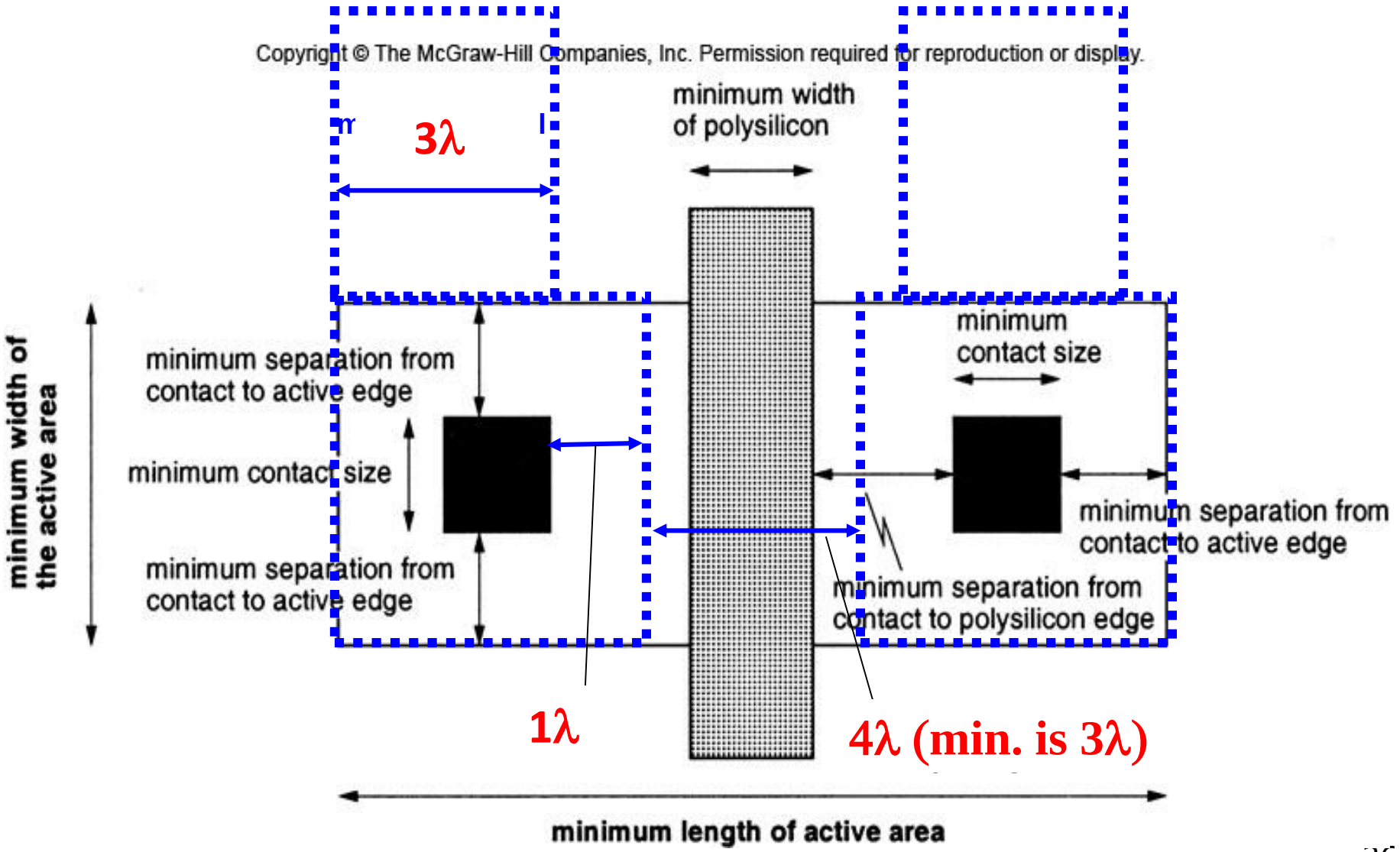



Channel length

Channel width

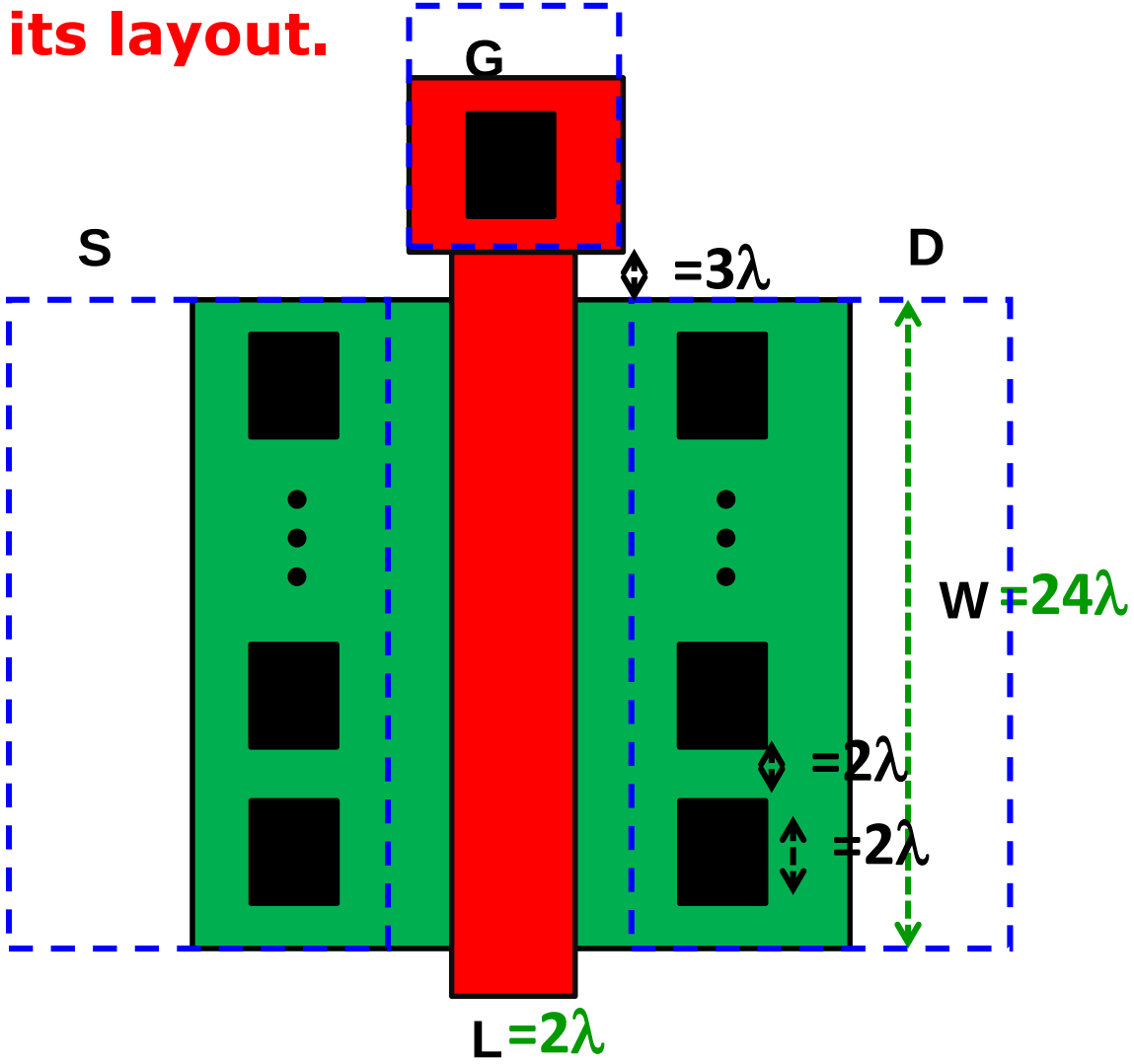


# Layout rules to minimise MOST size



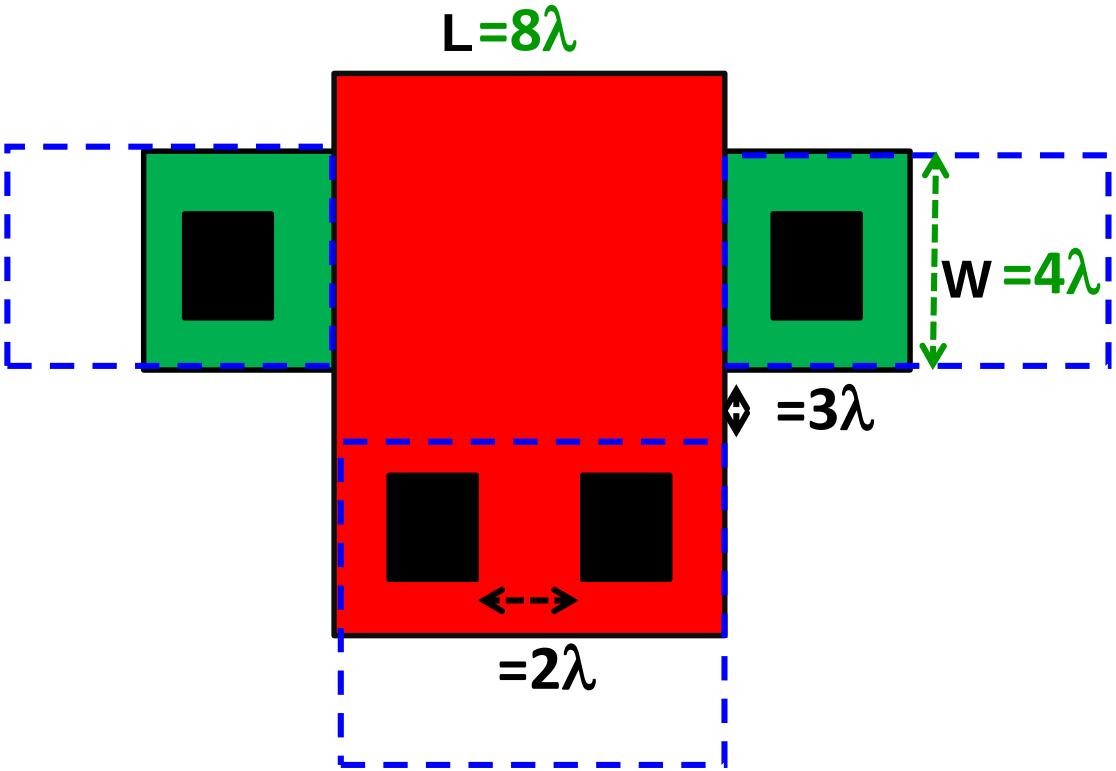
# The Design of a MOSFET

**Example: if we need a MOSFET with W/L = 12, design its layout.**

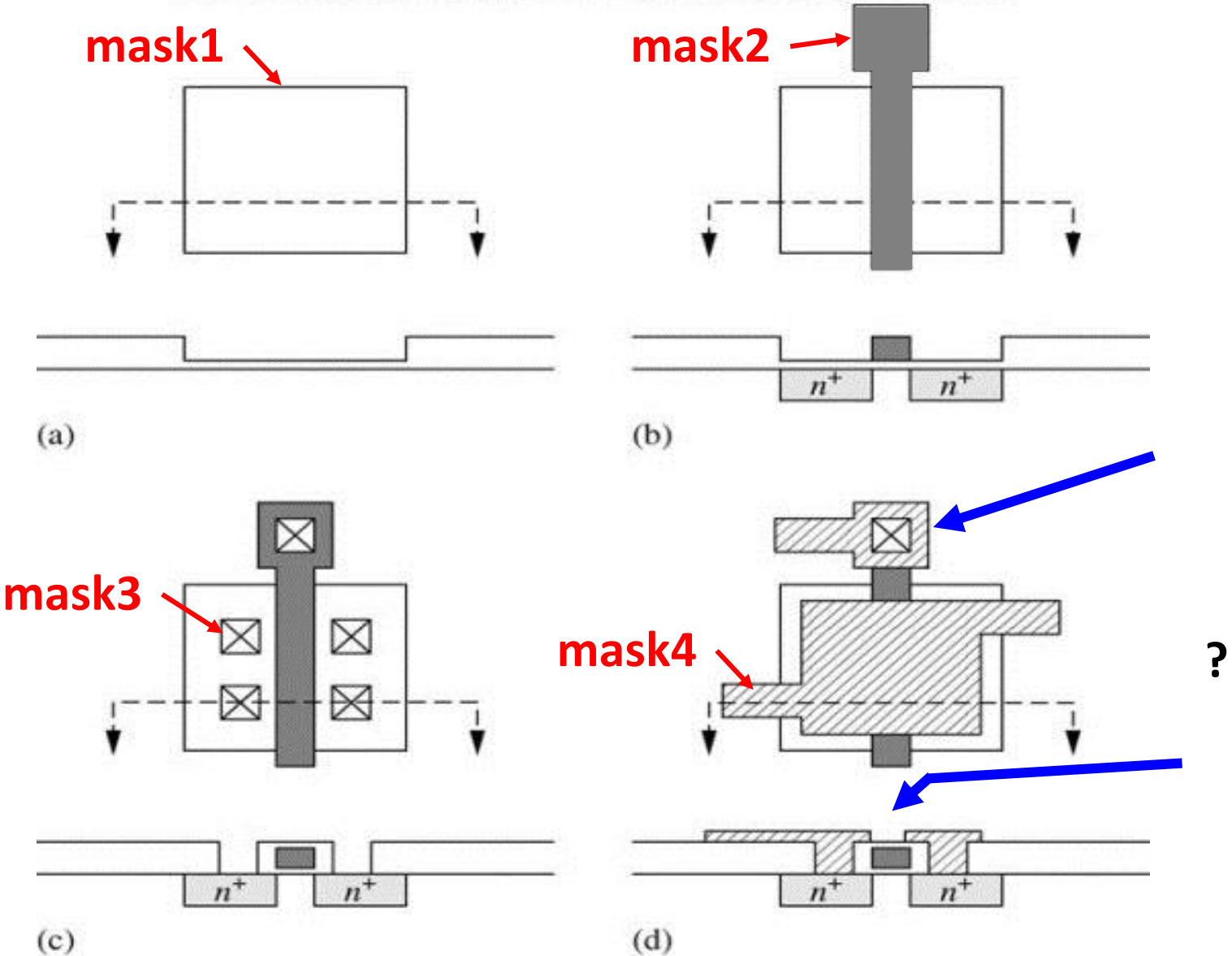


# The Design of a MOSFET

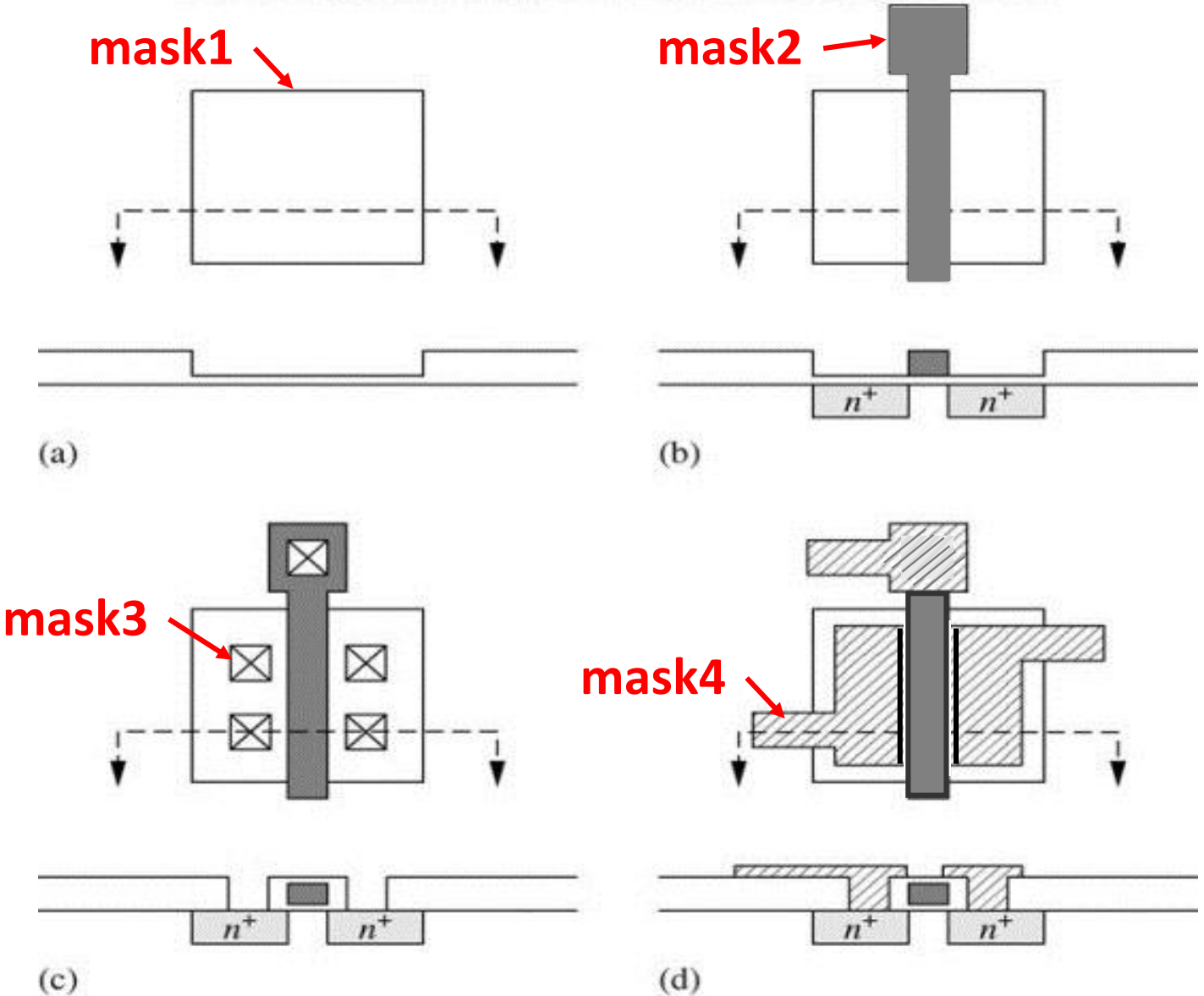
**Example: if we need a MOSFET with W/L = 0.5, design its layout.**



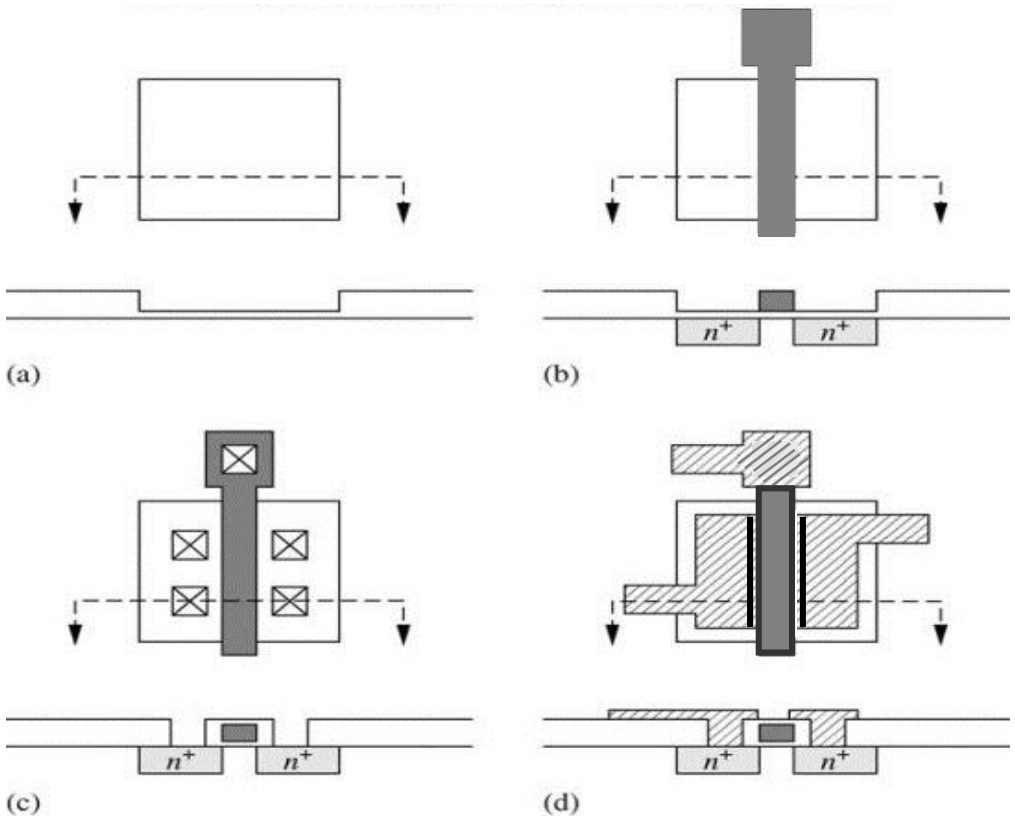
# Mask Sequence for a Polysilicon-Gate Transistor



# Mask Sequence for a Polysilicon-Gate Transistor



# Mask Sequence for a Polysilicon-Gate Transistor

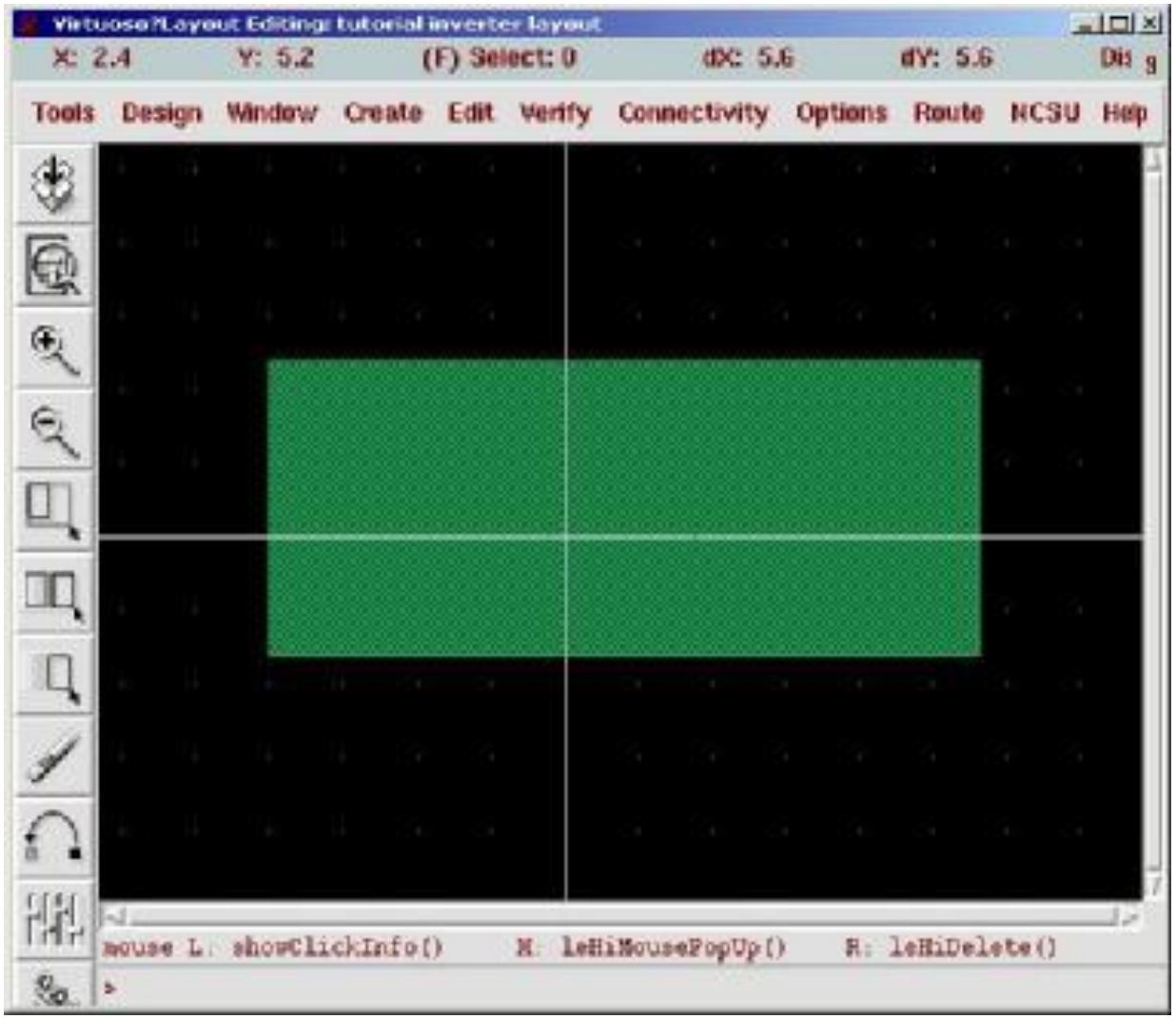



- **Mask 1**: Defines active area or thin oxide region of transistor
- **Mask 2**: Defines polysilicon gate of transistor, **aligns to mask 1**
- **Mask 3**: Delineates the contact window, **aligns to mask 2 & 1.**
- **Mask 4**: Delineates the metal pattern, **aligns to mask 3.**

Channel region of transistor formed by intersection of first two mask layers. Source and Drain regions formed wherever mask 1 is not covered by mask 2

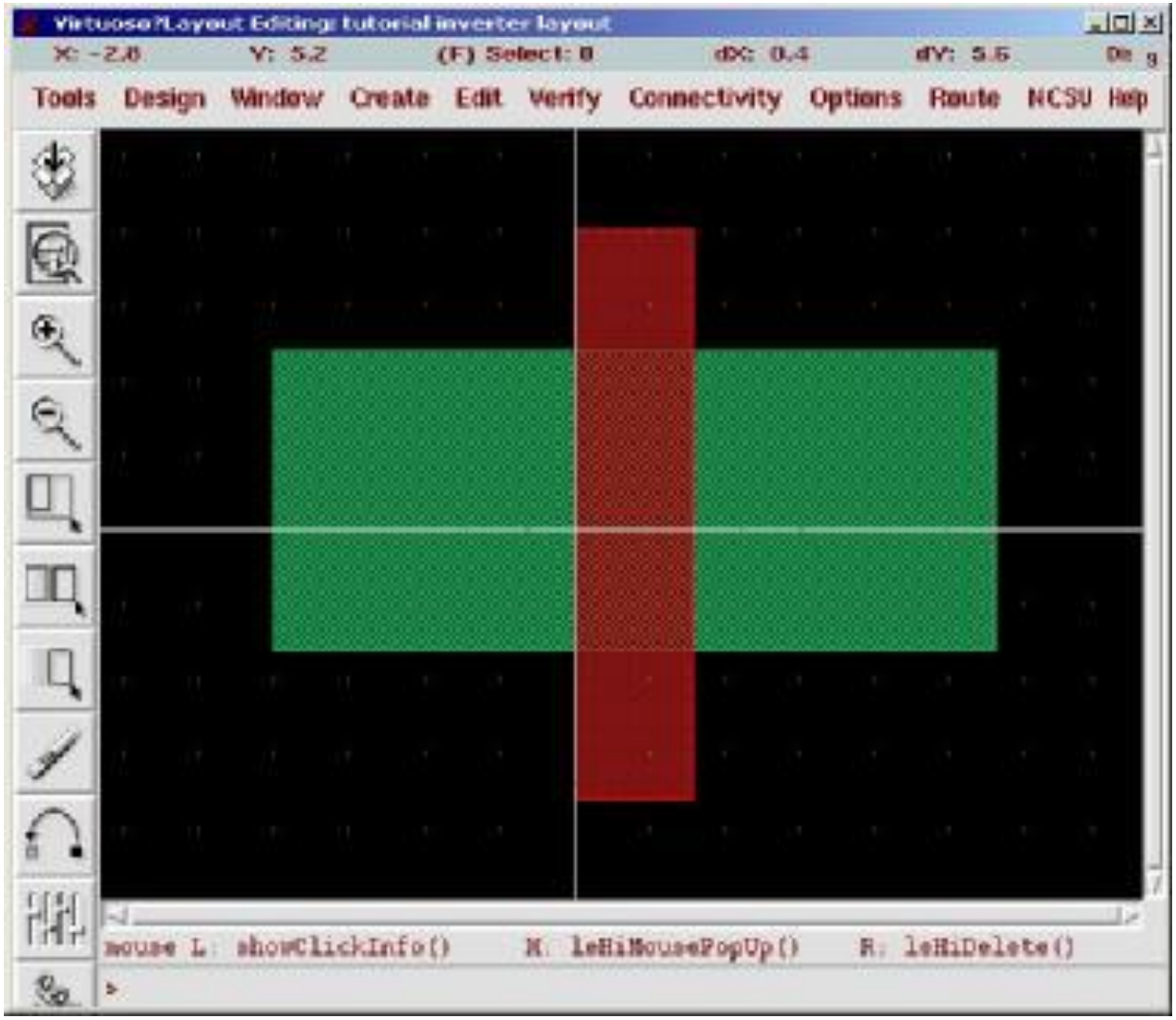
# How to draw layouts: **after calculation**

1. Drawing the N-Diffusion (***n active***)



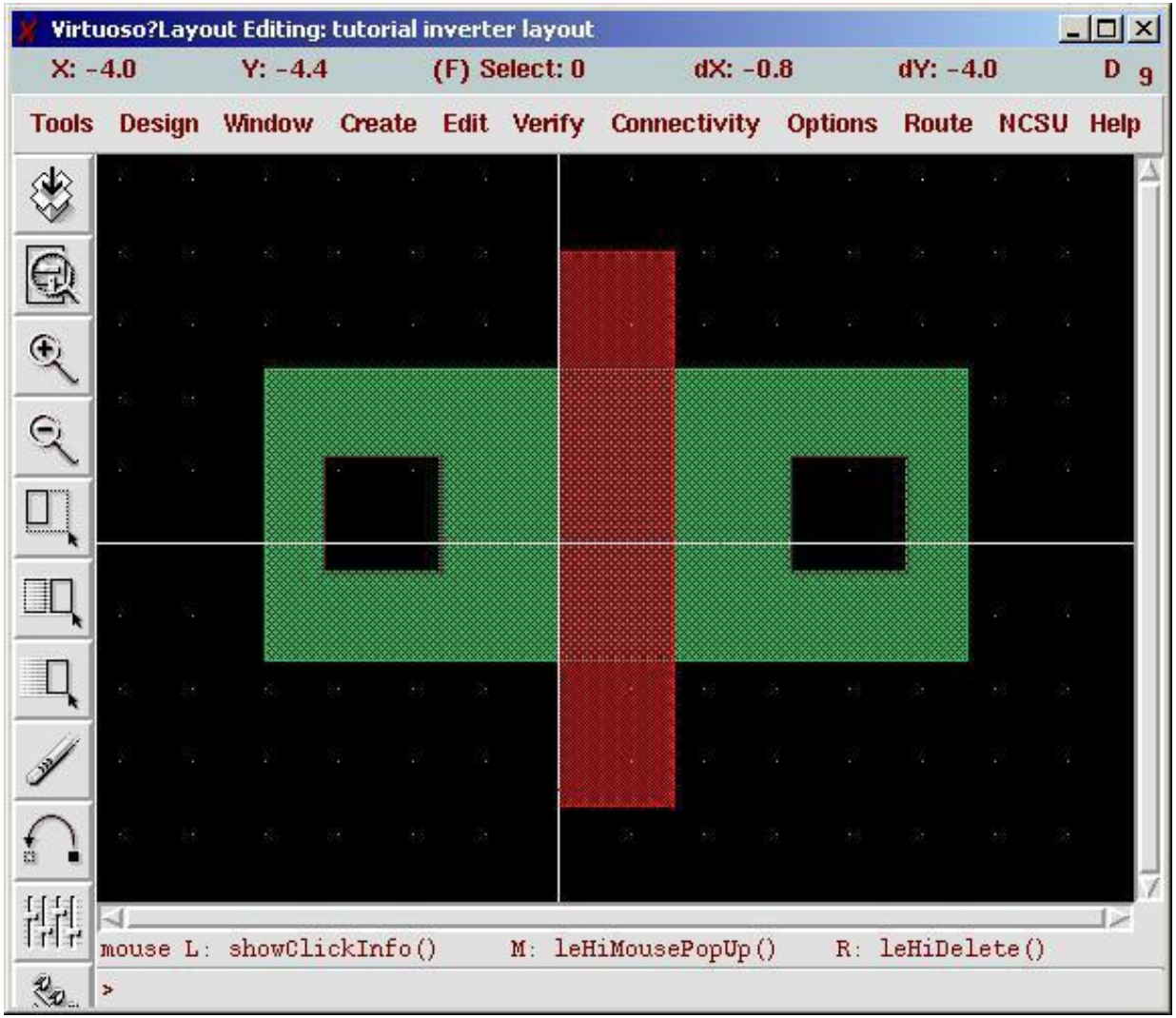
# How to draw layouts:

## 2. Drawing poly-Si Gate (***poly***)



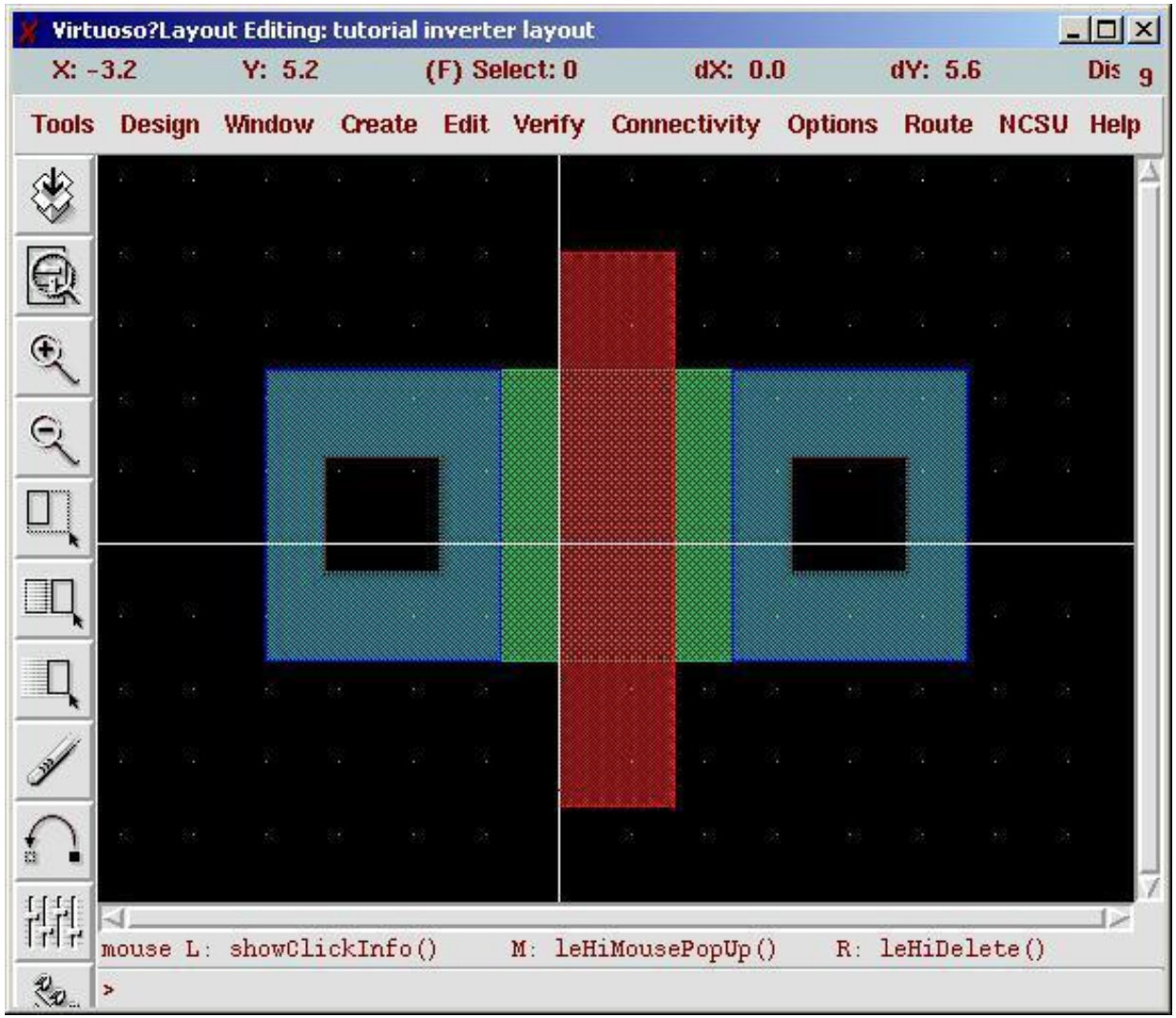
# How to draw layouts:

## 3. Making active contact



# How to draw layouts:

## 4. Covering the contacts with Metal



# Paper design: graph paper with a stipulated scale

## 标准坐标纸, 型号： 50cm*75cm


- Collect the graph paper at Room EE215 from Miss Kong