

Lecture 1
of
EEE201

CMOS Digital Integrated Circuits

**Department of Electrical & Electronic Engineering
Xi'an Jiaotong-Liverpool University (XJTLU)**

Thursday, 13th September 2018

□ Introduction

- about the module leader
- about the module
 - textbook, assessment

□ Silicon CMOS Integrated Circuits

- quick overview



About the Module Leader

(Sang Lam)

- ❑ E-mail address:
s.lam@xjtlu.edu.cn
- ❑ Office: EE220, EE Building
- ❑ Technical background:
Electronic Engineering and Physics
- ❑ Research interests:
semiconductor electronics and photonics (spanning from 30 MHz to 300 THz in the EM spectrum)
- ❑ Others (e.g. H&S, Student-Staff Liaison)

XJTLU FIND A PROGRAMME STUDY WITH US DEPARTMENTS RESEARCH LIFE AT XJTLU ABOUT ALUMNI NEWS EVENTS

SANG LAM PH.D.

Associate Professor

PROFILE

Sang Lam studied electronic engineering at the [Hong Kong University of Science and Technology \(HKUST\)](#) where he graduated with a Bachelor of Engineering degree. In his final year project, he worked on a gigahertz low-noise amplifier and downconversion mixer realised using a 0.5-micron CMOS process. Then he carried out research in silicon CMOS devices for radio-frequency (RF) integrated circuits (ICs) and received his Master of Philosophy degree in [Electrical and Electronic Engineering](#). He also earned a Master of Science degree in [Physics](#) from [HKUST](#). After working for a few years in Hong Kong, he went to the UK to pursue doctoral research on semiconductor photonics at the nanometre scale. Participating a multi-university and interdisciplinary project funded by EPSRC of the UK, he worked on photonic crystal cavities with embedded quantum dots (QDs) at the [University of Sheffield](#). On completion of his PhD research, Dr. Lam returned to Hong Kong to co-found a start-up company. After building the foundation of the start-up, he worked as an R&D engineer for [Hong Kong Applied Science and Technology Research Institute Company Limited \(ASTRI\)](#), an R&D organization established by the Hong Kong Government. Prior to joining [Xi'an Jiaotong-Liverpool University \(XJTLU\)](#) as an academic staff member of the [Department of Electrical and Electronic Engineering \(EEE\)](#), he worked on a PEM fuel cell project at ASTRI. Besides, he also assisted in R&D projects on

(URL: <http://www.xjtlu.edu.cn/en/departments/academic-departments/electrical-and-electronic-engineering/staff/sang-lam>)



Xi'an Jiaotong-Liverpool University

西交利物浦大學

About the Module EEE201

(teaching delivery)

- ❑ Level 2; 2.5 credits
- ❑ 26 hours of **lectures**
 - 2 hours/week (for 13 weeks)
- ❑ 8 hours of **practical** sessions
 - IC layout design
 - weeks 10 and 11
- ❑ no official **problem classes**
 - informal ones by teaching assistants
- ❑ 41 hours of private study
 - about 3 to 4 hours/week
 - i.e. about 0.5 hour/day (assuming no work on weekends)

Module Title	CMOS Integrated Circuits
Module Code	EEE201
Originating Department	Electrical and Electronic Engineering
Module Level ¹	2 (FHEQ level 5)
Module Credits (normally 5)	2.5
Pre-requisites (including Year 1)	EEE203 MTH013 MTH008 MTH007 MTH101 MTH102 MTH201
Shared Programme(s) (please name all)	BEng Electrical Engineering BEng Electronic Science and Technology BEng Telecommunications Engineering

Mode of Delivery and Hours

	Lectures	Seminars	Tutorials	Lab / Practicals	Fieldwork / Placement	Other (Private study)	Total
Hours / Semester	26			8		41	75
Delivery Pattern	2 HR/WEEK			4 HR/WEEK			

Description

Aims and Fit of Module (i.e. relationship to programme) To combine CMOS integrated circuit design exercises with very relevant industrial concepts and a deeper understanding of MOSFET device physics principles and electromagnetism. To provide the background for later modules, relevant final year projects, but particularly for employment in those industries that are firmly based in microelectronics technology. To further develop the concept of design as being more than simple problem solving, but something demanding high levels of innovation based on sound physics principles.
Learning Outcomes (for accreditation and other reasons, sub-headings could be added to this section) Students completing the module successfully should be able to: A. Demonstrate knowledge and understanding of CMOS-based integrated circuit design with considerations of power, speed, yield, packing density and design trade-offs associated with material, device and circuit limitations. B. Demonstrate knowledge of historical and future development of silicon-based integrated circuit

(<http://ebridge.xjtlu.edu.cn/>)



About the Module EEE201

(topics)

- ❑ **Silicon CMOS Digital Integrated Circuits**
 - mainstream semiconductor for integrated circuits
- ❑ **Two-terminal Devices: *p-n junction*; MOS capacitor**
- ❑ **MOSFET as Switch**
 - CMOS inverter; voltage transfer characteristics
- ❑ **CMOS combinational logic circuits**
 - NAND and NOR gates; complex logic circuits
- ❑ **CMOS Physical Layout Design**
 - interconnect consideration
- ❑ **Advanced CMOS Digital Circuits**
- ❑ **Memory Structures**



Xi'an Jiaotong-Liverpool University

西交利物浦大學

About the Module EEE201

(“prerequisite” modules)

□ EEE112 Integrated Electronics and Design

- semiconductors, energy bands
- diodes, *p-n* junction fabrication, depletion region, forward and reverse bias conduction; MOSFET

□ EEE109 Electronic Circuits

- semiconductor materials & properties
- diodes & transistors (MOSFETs)
- DC circuit analysis

□ Knowledge from these modules would be very helpful.

About the Module EEE201

(textbook)

❑ CMOS Digital Integrated Circuits Analysis & Design

- by Sung-Mo Kang *et al.*
- 4th edition, 2015
- published by McGraw Hill Education

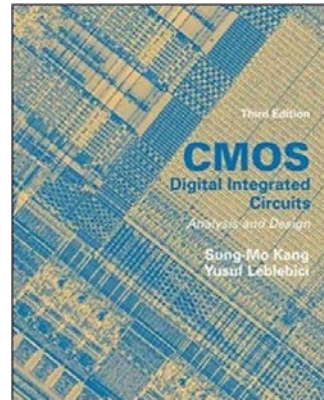
❑ Good textbook on the subject

- adopted by other top universities

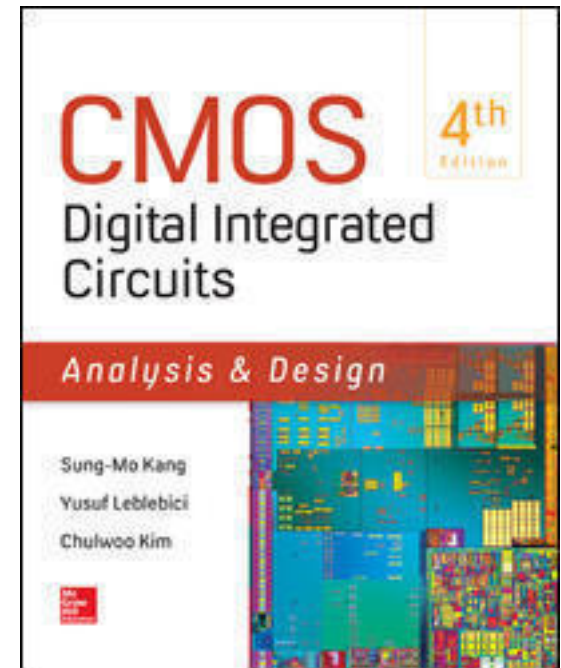
❑ previous editions

- 3rd edition, 2002
- same basic topics
- more copies at University's Library

(Image taken from Amazon.com; available at <https://www.amazon.com/Digital-Integrated-Circuits-Analysis-Design/dp/0072460539>)



(Image taken from the website of *McGraw-Hill Education*; available at <https://www.mheducation.com/highered/product/cmos-digital-integrated-circuits-analysis-design-kang-leblebici/M0073380628.html>)



Xi'an Jiaotong-Liverpool University
西交利物浦大學

Other Useful Books

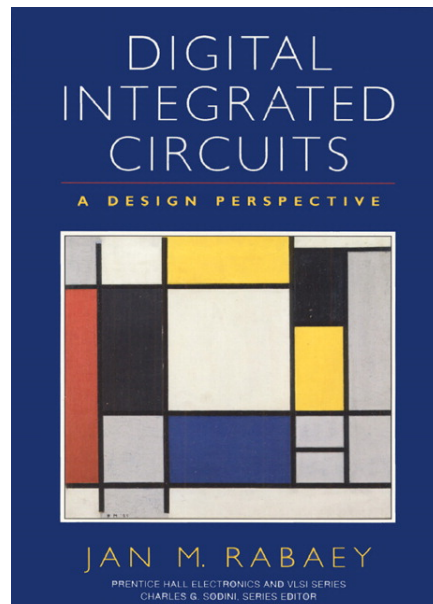
(recommended but optional)

(Image taken from Pearson; available at
<https://www.pearson.com/us/higher-education/program/Rabaey-Digital-Integrated-Circuits-2nd-Edition/PGM263532.html>)

❑ Digital Integrated Circuits: A Design Perspective, 2nd edition

- by Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic
- 2003; published by Pearson

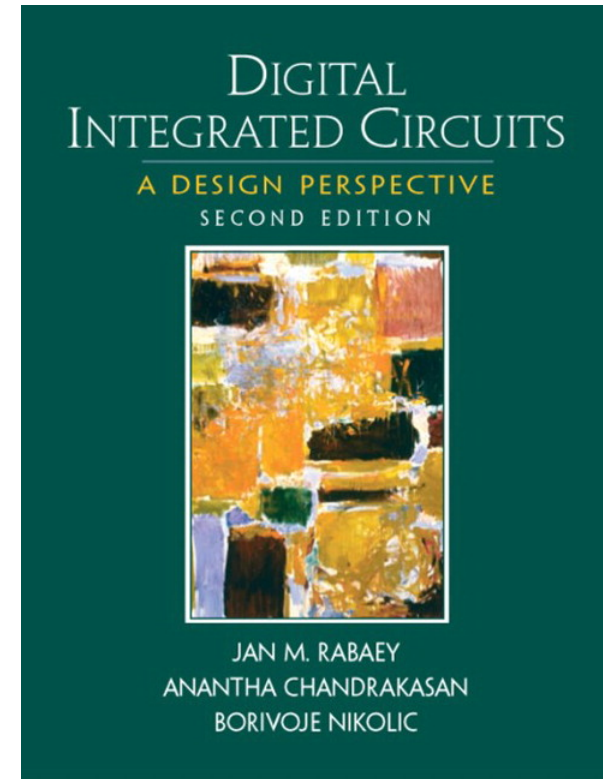
❑ previous edition, (1996)



- by Jan M. Rabaey only
- published by Prentice Hall
- more advanced textbook

(Images taken from Pearson; available at:
<https://www.pearson.com/us/higher-education/product/Rabaey-Digital-Integrated-Circuits-A-Design-Perspective/9780131786097.html?tab=contents>)

EEE201 CMOS Digital Integrated Circuits
Semester 1, 2018/2019 by S.Lam@XJTLU



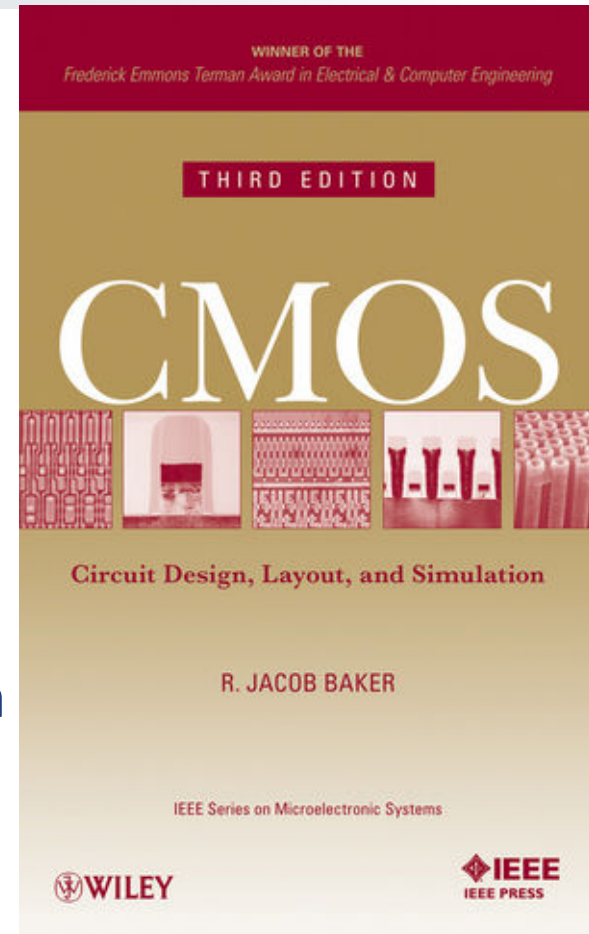
Xi'an Jiaotong-Liverpool University
西交利物浦大學

Other Useful Books

(optional)

- ❑ **CMOS: Circuit Design, Layout, and Simulation, 3rd edition (2010)**
 - by R. Jacob Baker
 - published by Wiley-IEEE Press
 - a good reference book on CMOS IC design (> 1100 pages!)
 - more suitable for advanced undergraduates or graduate students
 - useful even when working as IC design engineers
 - with helpful illustration to design at the device & structure levels

(Image taken from Wiley-IEEE Press; available at:
<https://www.wiley.com/WileyCDA/WileyTitle/productCd-0470881321,miniSiteCd-IEEE2.html>)

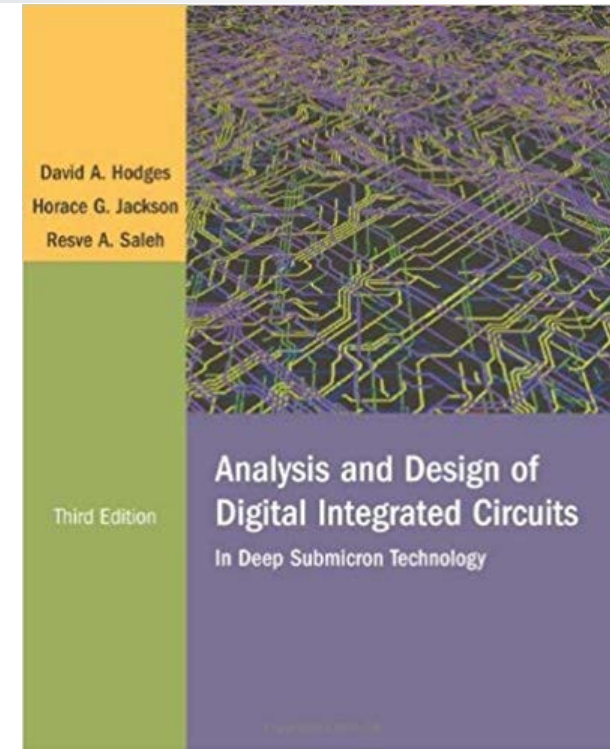


Xi'an Jiaotong-Liverpool University
西交利物浦大學

Other Useful Books

(optional)

- ❑ **Analysis and Design of Digital Integrated Circuits, 3rd edition (2003)**
 - by David A. Hodges, Horace G. Jackson, and Resve Saleh
 - published by McGraw-Hill Science/Engineering/Math
 - suitable for advanced undergraduates or graduate students
 - good chapters on semiconductor memories & interconnect design
 - with the deep submicron CMOS technology perspective



(Image taken from Amazon.com; available at <https://www.amazon.com/Analysis-Design-Digital-Integrated-Circuits/dp/0072283653>)



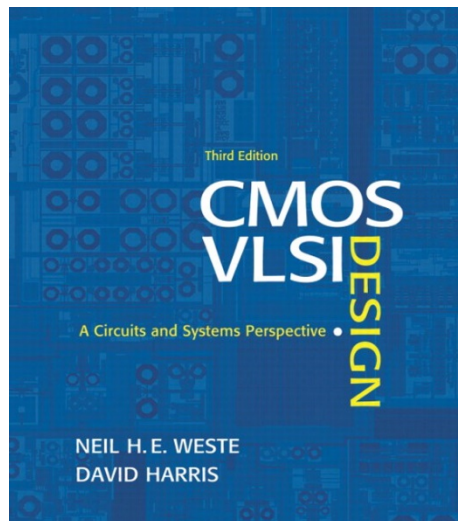
Xi'an Jiaotong-Liverpool University
西交利物浦大學

Other Useful Books

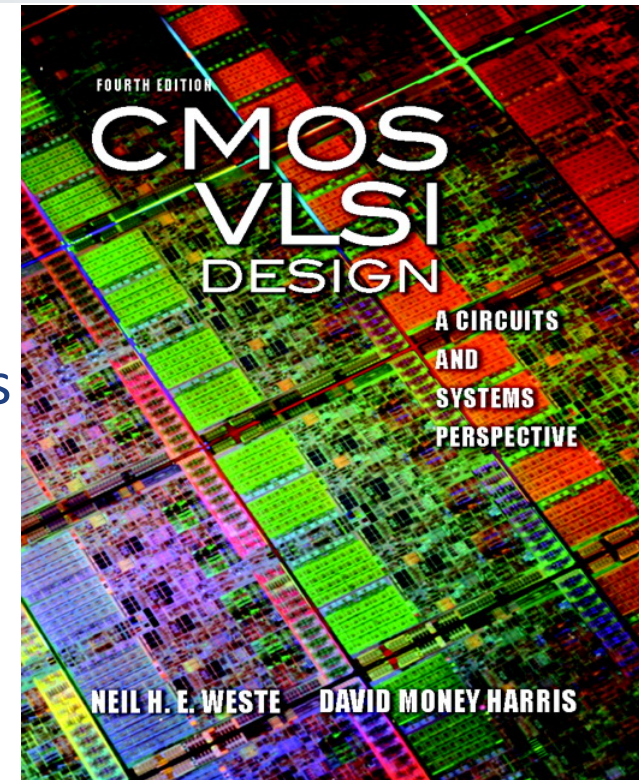
(optional)

- ❑ **CMOS VLSI Design: A Circuits and Systems Perspective**, 4th edition (2011)
 - by Neil Weste and David Harris
 - published by Pearson
 - suitable for advanced undergraduates or graduate students

- ❑ **previous edition**, 3rd edition (2005)



- more advanced textbook for VLSI design
- thorough chapters on delay & power dissipation



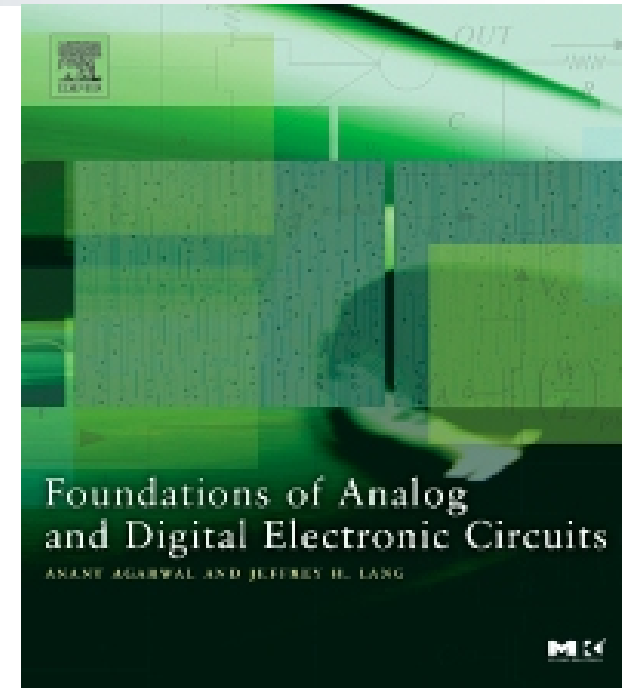
(Image taken from Pearson; available at:
<https://www.pearson.com/us/higher-education/product/Rabaey-Digital-Integrated-Circuits-A-Design-Perspective/9780131786097.html?tab=contents>)



Other Useful Books

(optional)

- ❑ **Foundations of Analog and Digital Electronic Circuits, 1st edition (2005)**
 - by Anant Agarwal & Jeffrey Lang
 - published by Elsevier
 - a good textbook to learn the basic concepts of digital circuits (as well as analogue circuits in an integrated approach)
 - good for people to learn about digital circuits but not familiar with semiconductor electronics

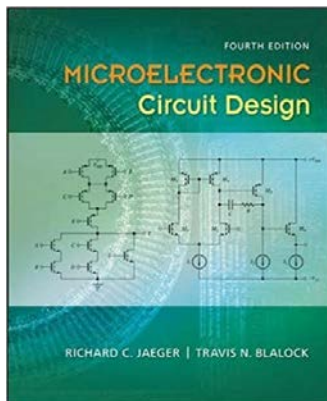


(Image taken from Elsevier; available at:
<https://www.elsevier.com/books/foundations-of-analog-and-digital-electronic-circuits/agarwal/978-0-08-050681-4>)

Other Useful Books

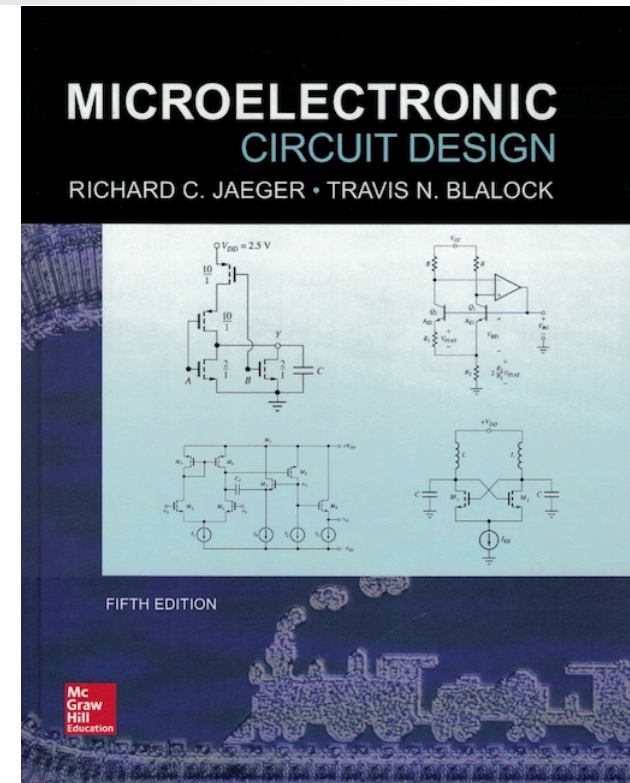
(optional)

- ❑ **Microelectronic Circuit Design, 5th edition (2016)**
 - by Richard Jaeger and Travis Blalock
 - published by McGraw-Hill Education
 - a comprehensive textbook to learn the basic concepts of digital circuits (as well as analogue circuits)
 - with some good illustration of semiconductor electronics



- ❑ **previous edition, 4th (2010)**

(Image taken from Amazon.cn; available at <https://www.amazon.com/Microelectronic-Circuit-Design-Richard-Jaeger/dp/0073380458/>)



(Image taken from the book authors' website; available at: <http://www.jaegerblalock.com/>)



Xi'an Jiaotong-Liverpool University
西交利物浦大學

About the Module EEE201

(assessment)

- ❑ No mid-term exam (0%); class participation (0%)
- ❑ Final Exam (70%)
 - Questions will test more on understanding rather than memorisation of knowledge.
- ❑ In-class **Quizzes** (10%) - continuous assessment
 - tentatively at least 10 in-class quizzes (\approx 5-10 min)
 - Each quiz consists of only quick questions, expecting only short answers to be submitted through ICE \Rightarrow bring your mobile devices so that you can access ICE
- ❑ IC Design Project (15%)
 - draw the physical layout of basic digital circuits on graph paper
 - write a report on the IC design, including the calculations
 - *practical sessions* in weeks 10-11
- ❑ Assignments (5%)

Related News

(plagiarism)

□ glossary

➤ plagiarism

an act of plagiarizing something;
something that has been
plagiarized

plagiarize: to copy another
person's ideas, words or work and
pretend that they are your own

➤ strip of

➤ verdict

➤ deception; deceive

(Source: *Oxford Advanced Learner's Dictionary*; available online
at: <http://oald8.oxfordlearnersdictionaries.com/dictionary/plagiarisms>)

German minister Annette Schavan stripped of doctorate



The education minister, on a five-day visit to South Africa, is to appeal against the decision

A German university has voted to strip Education Minister Annette Schavan of her doctorate after an investigation into plagiarism allegations.

The University of Duesseldorf's philosophy faculty decided on Tuesday that she had carried out "a deliberate deception through plagiarism".

The minister has denied the claims and said she will appeal.

An earlier plagiarism row brought an end to the political career of Germany's defence minister in 2011.

Large parts of Karl-Theodor zu Guttenberg's 2006 legal dissertations were found by Bayreuth University to have been copied and he stood down before it issued its damning verdict in May 2011.

Using the same words as Duesseldorf's Heinrich Heine University, it concluded that he had "deliberately deceived".

When Ms Schavan became the second minister in Chancellor Angela Merkel's government to be accused of copying her doctorate, in this case by an anonymous blogger, she insisted she had never "knowingly falsely cited any sources" and promised to respond to the accusations.

(Taken from BBC News; available at
<http://www.bbc.co.uk/news/world-europe-21347510>)

Related Stories

German minister denies plagiarism

Europe's 'plague of plagiarism'

Ex-German minister 'plagiarised'



Xi'an Jiaotong-Liverpool University

西交利物浦大學

Related News

(data fabrication)

□ glossary

(Source: *Oxford Advanced Learner's Dictionary*, available online at: <http://www.oxfordlearnersdictionaries.com/definition/english/fabricate>)

➤ fabrication

false information that is invented in order to trick people; the act of inventing such information

fabricate: *make up*; to invent false information in order to trick people



Stem cells: Scientist asks for research to be withdrawn

By James Gallagher
Health and science reporter, BBC News

🕒 10 March 2014 | Health

🔗 Share



A Japanese scientist behind a seemingly groundbreaking stem cell study says the findings should be withdrawn amid doubts over its quality.

It was reported in January that dipping cells in acid could cheaply and quickly convert them into stem cells.

But questions were raised about the images used in the scientific report and other research groups have failed to reproduce the results.

Author Prof Teruhiko Wakayama said: "It is no longer clear what is right."

The future of regenerative medicine is pinned on stem cells, which can transform into any other type of tissue. They are being investigated for restoring sight to the blind and repairing the damage caused by a heart attack.

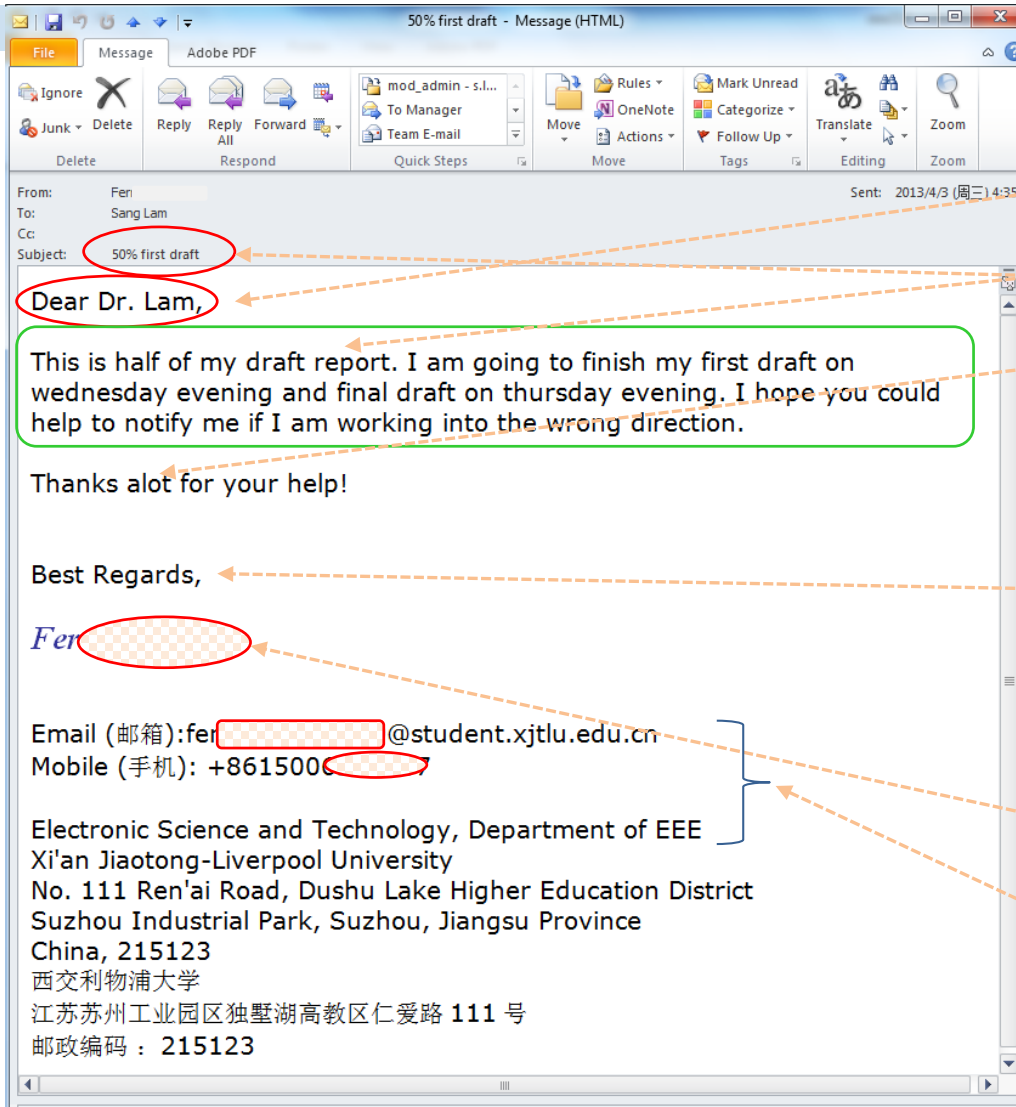
(Taken from BBC News; available at <http://www.bbc.com/news/health-26516458>)



Xi'an Jiaotong-Liverpool University
西交利物浦大學

E-mail Communication

(an example e-mail)



- ❑ Include a courteous greeting
- ❑ Get to the subject
- ❑ Use proper English and check your spelling
- ❑ Close with "Regards, Sincerely, etc."
- ❑ Identify yourself
- ❑ Extra information

Lecture 1
of
EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering
Xi'an Jiaotong-Liverpool University (XJTLU)

Thursday, 13th September 2018

□ Introduction

- about the module leader
- about the module
 - textbook, assessment

□ Silicon CMOS Integrated Circuits

- quick overview



Digital Integrated Circuits

(advantages)

□ Why digital?

- Nowadays, **information** is so commonly *represented*, *processed*, *stored* and *transmitted* in the *digital* format.
- Information in the digital format, known as digital data, can be in the form of text, voice/audio, images and videos.

□ Why digital circuits?

- **Digital data** is most conveniently *processed* and *transmitted* in the *electronic form*.
- As a result, electronic circuits for processing and transmitting digital data are needed. These circuits are called digital circuits.

Digital Integrated Circuits

(efficient & more immune to noise)

□ Why digital circuits?

- Can you give any common examples of processing and transmitting digital data in the *electronic form*?
- How about examples of storing digital data in the *electronic form*?
- In the digital format, data can be processed, stored and transmitted in more efficient ways and less vulnerable to errors (because of noise or interference).
- What are the examples of transmitting digital data in more efficient ways?

□ Why integrated circuits?

- portability, power dissipation \Rightarrow **cost**
- more functionality from integration



Xi'an Jiaotong-Liverpool University
西交利物浦大學

CMOS Digital Integrated Circuits

(why silicon CMOS)

□ Why CMOS digital integrated circuits?

- CMOS is short for complementary metal oxide semiconductor. It is the semiconductor technology with complementary transistors (the n-type MOSFET and p-type MOSFET) on the same chip.
- The CMOS technology uses silicon as the semiconductor material.
- Silicon semiconductor technology has been predominantly used for the realisation of digital integrated circuits.
- It is simply more efficient, including the power consumption and circuit density
- \Rightarrow lower **cost**

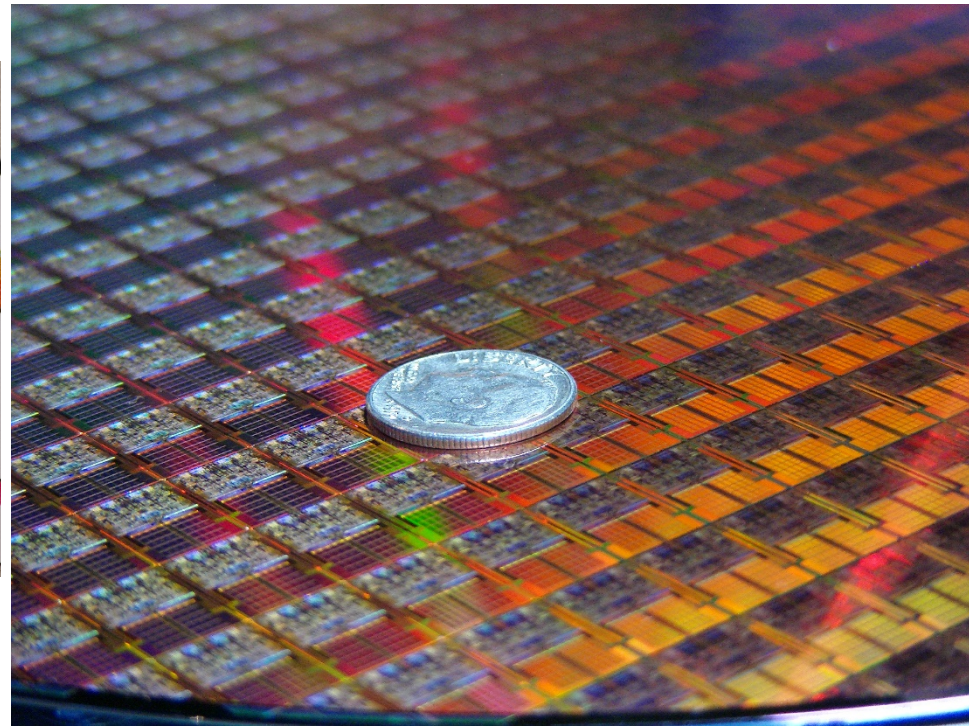
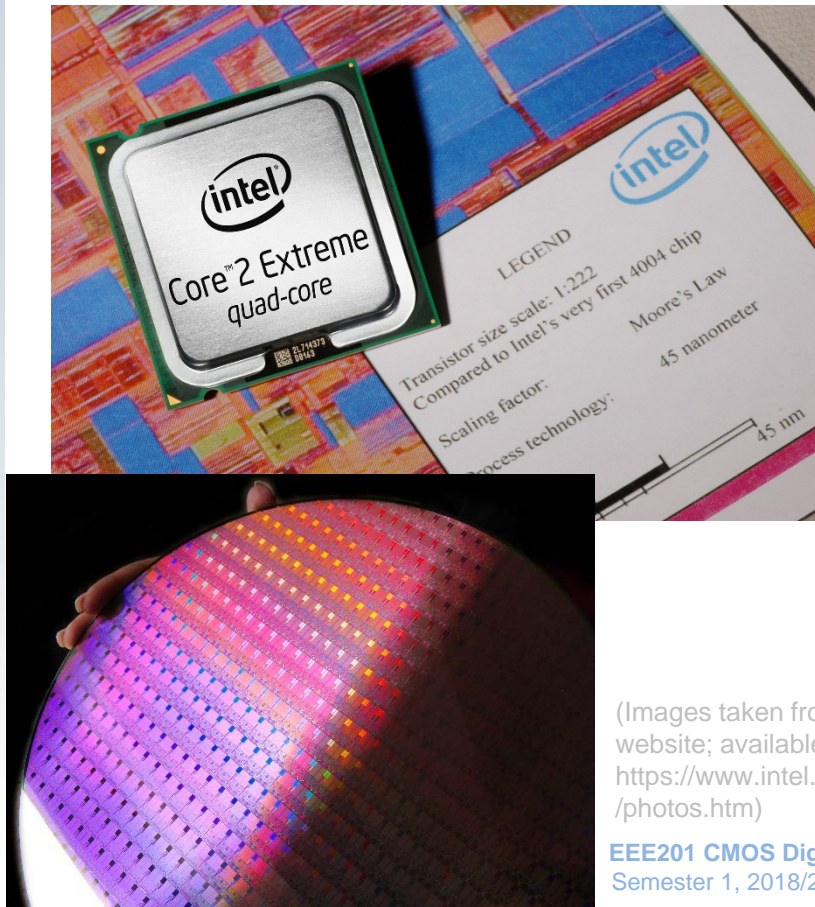


Xi'an Jiaotong-Liverpool University
西交利物浦大學

Examples of CMOS Digital ICs

(microprocessors)

- ❑ In 2007, Intel manufactured microprocessors in the 45nm technology with hafnium-based high-k metal-gate transistors.



(Images taken from Intel's corporate website; available at <https://www.intel.com/pressroom/kits/45nm/photos.htm>)



CMOS Digital ICs

(crystalline silicon)

- ❑ Digital ICs are predominantly fabricated on **silicon** wafers.

	IIIA	IVA	VA	VIA
	5 10.811 B Boron	6 12.01115 C Carbon	7 14.0067 N Nitrogen	8 15.9994 O Oxygen
	13 26.9815 Al Aluminum	14 28.086 Si Silicon	15 30.9738 P Phosphorus	16 32.064 S Sulfur
IIB	30 65.37 Zn Zinc	31 69.72 Ga Gallium	32 72.59 Ge Germanium	34 78.96 Se Selenium
	48 112.40 Cd Cadmium	49 114.82 In Indium	50 118.69 Sn Tin	52 127.60 Te Tellurium
	80 200.59 Hg Mercury	81 204.37 Tl Thallium	82 207.19 Pb Lead	83 208.980 Bi Bismuth
				84 (210) Po Polonium

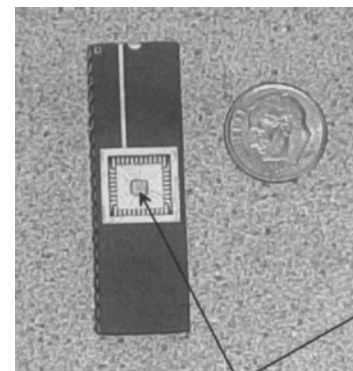
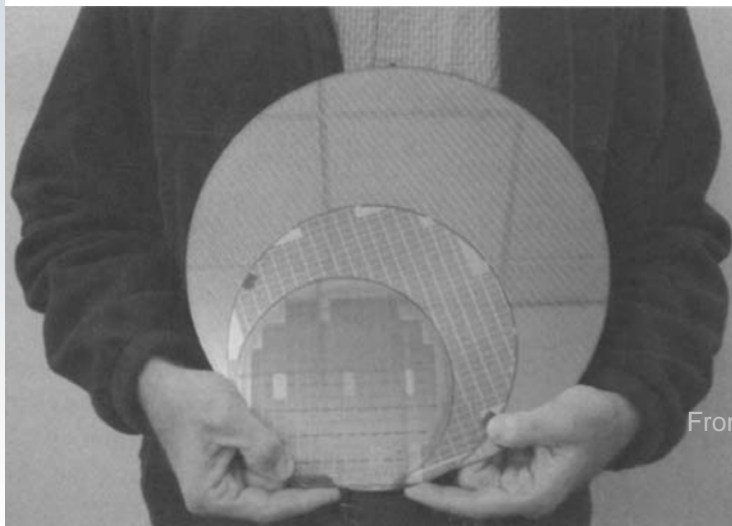
- Silicon is a group IV element. Silicon of very high purity with the perfect crystalline structure is needed for making digital ICs like microprocessors.
- It has a band-gap energy of 1.1 eV at room temperature.

From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.

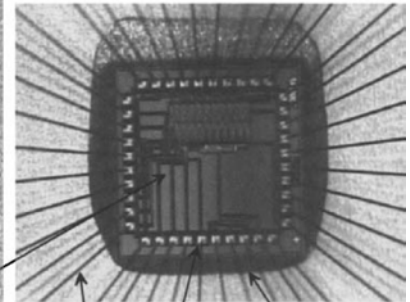
CMOS Digital ICs

(fabricated on silicon wafers)

- ❑ The diameter of silicon wafers for fabrication of digital ICs is typically from 100 mm (4 inch) to 300 mm (12 inch).
- ❑ After some on-wafer testing, the ICs on the wafers are diced into chips and then packaged.



(a)



(b)

Bond wire
Bonding pad
Epoxy to hold chip in place

From: R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, 3e, © 2010 Wiley-IEEE Press, USA.



Xi'an Jiaotong-Liverpool University
西交利物浦大學

Evolution of Electronic Devices

(from vacuum tubes to ICs)

Vacuum Tubes



Discrete Transistors

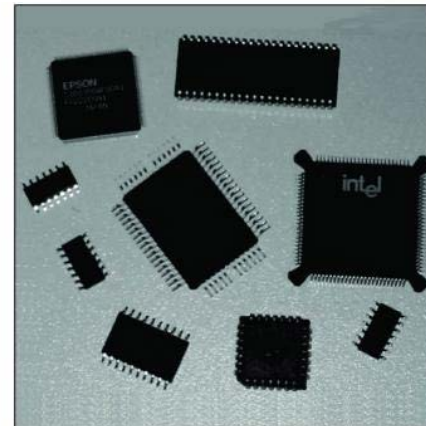


SSI & MSI
Integrated
Circuits
(ICs)



Note: SSI: small-scale integration
MSI: medium-scale integration
VLSI: very large-scale integration

VLSI
Surface-
Mount
Circuits



Xi'an Jiaotong-Liverpool University

西交利物浦大學

From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*,
4e, © 2010 McGraw-Hill, USA.

EEE201 CMOS Digital Integrated Circuits
Semester 1, 2018/2019 by S.Lam@XJTLU

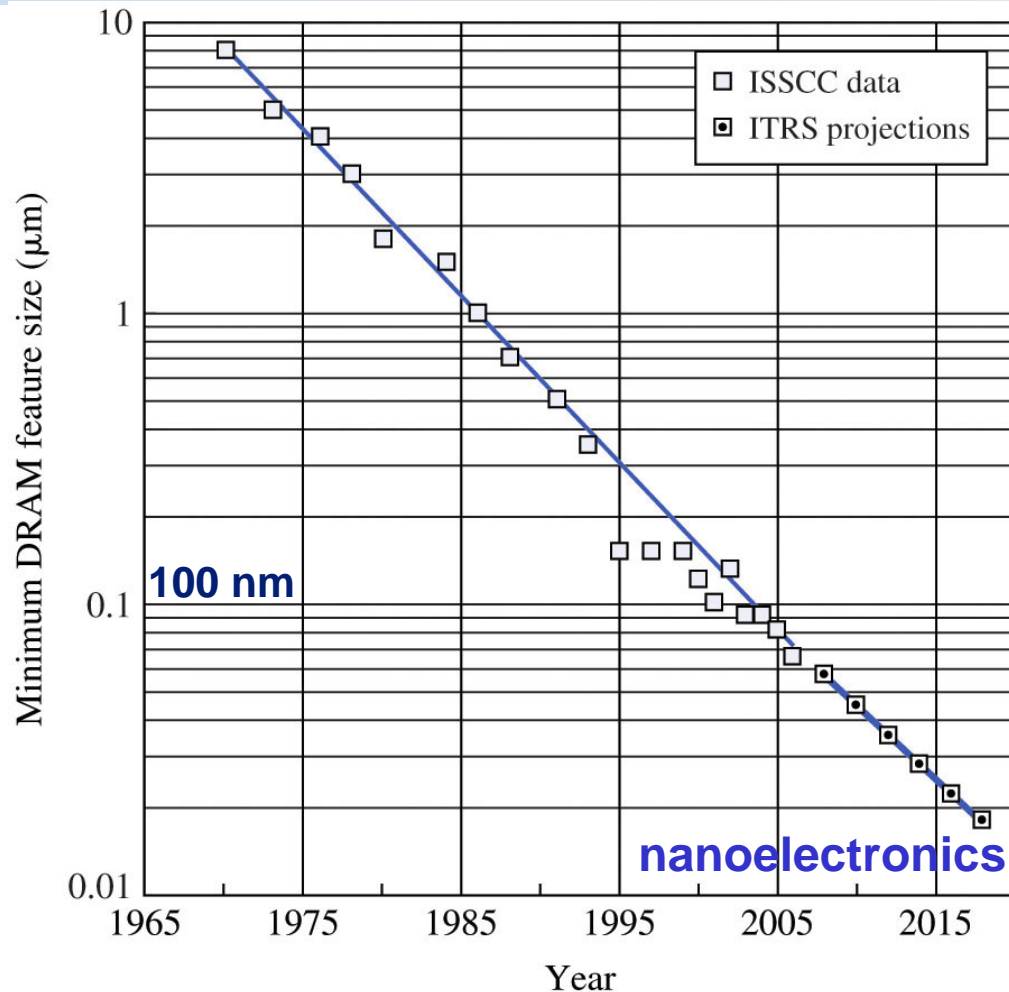
Microelectronic Proliferation

(number of transistors)

- ❑ The **integrated circuit (IC)** was invented in 1958.
- ❑ World transistor production has more than doubled every year for the past twenty years.
- ❑ Every year, more transistors are produced than in all previous years combined.
- ❑ By 2010, an Intel® Core™ processor with a 32nm processing die and second-generation high-k metal gate silicon technology held 560 million (5.6×10^8) transistors.
- ❑ Moore's Law & nanoelectronics

Device Feature Size

(down scaling)

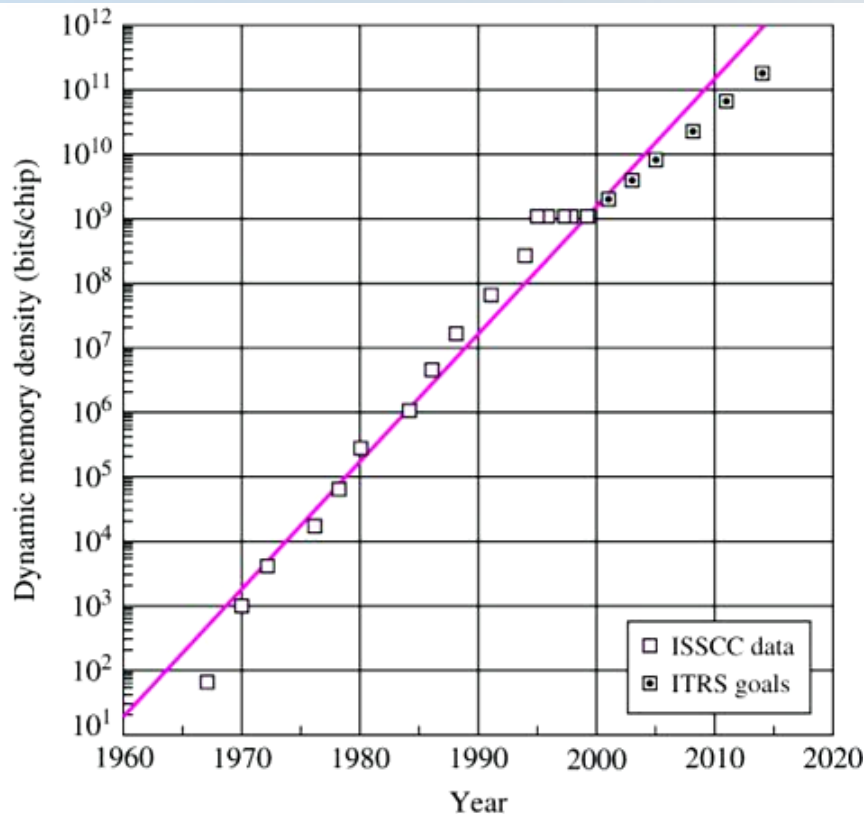


From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4th edition,
© 2010 McGraw-Hill, USA.

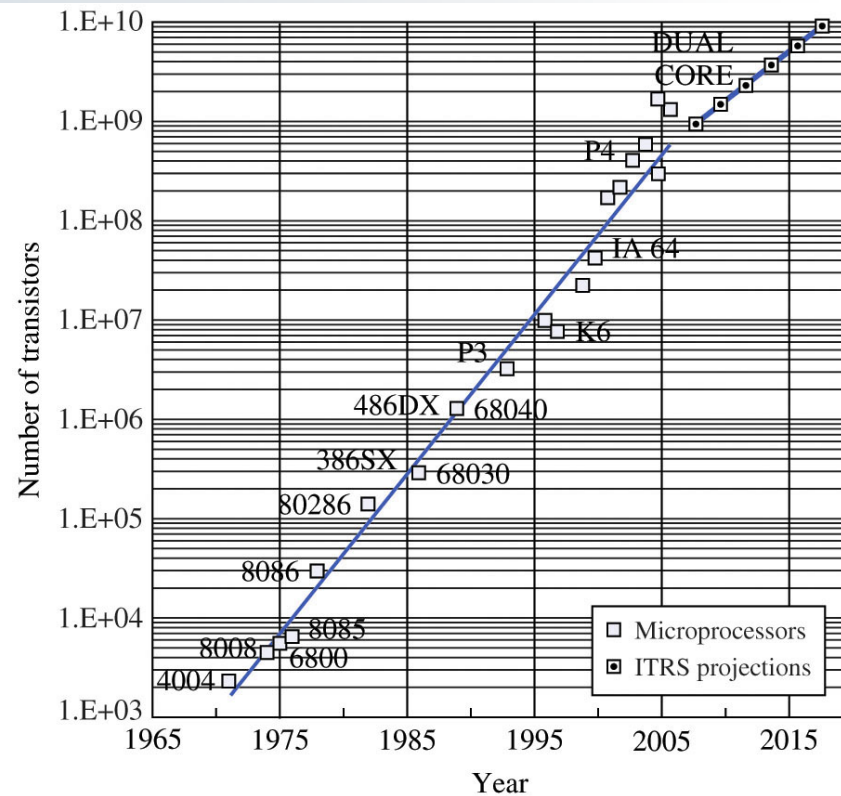
- Feature size reductions enabled by process innovations.
- Smaller features lead to more transistors per unit area and therefore higher density.

Microelectronics Complexity

(rapid increase)



Memory chip density
versus time.



Microprocessor complexity
versus time.



From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4th edition,
© 2010 McGraw-Hill, USA.

Silicon CMOS Digital ICs

(mainstream IC technology)

□ Why CMOS digital integrated circuits?

- CMOS is short for complementary metal oxide semiconductor. It is the semiconductor technology with complementary transistors (the n-type MOSFET and p-type MOSFET) on the same chip.
- The CMOS technology uses silicon as the semiconductor material.
- Silicon semiconductor technology has been predominantly used for the realisation of digital integrated circuits.
- It is simply more efficient, including the power consumption and circuit density
- \Rightarrow lower **cost**

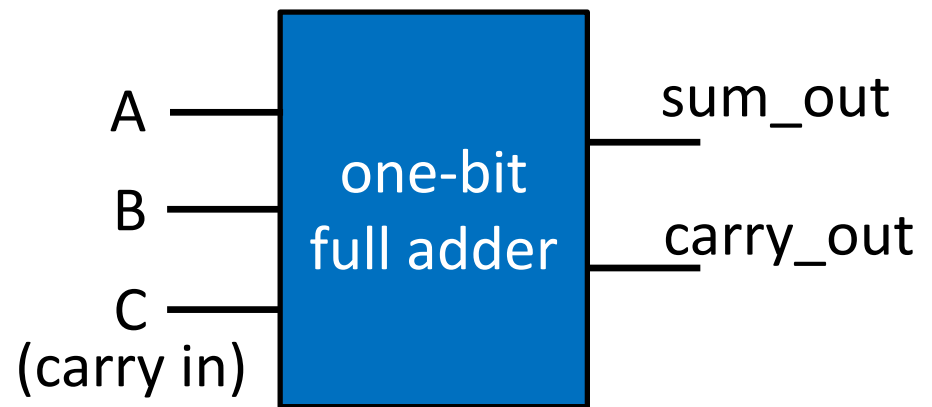
Silicon CMOS Digital ICs

(introductory level in EEE201)

- ❑ To design digital integrated circuits for fabrication in silicon CMOS technology, there are various levels: system, logic gate, **transistor schematic** and **physical layout**.

➤ taking a one-bit full adder as an example

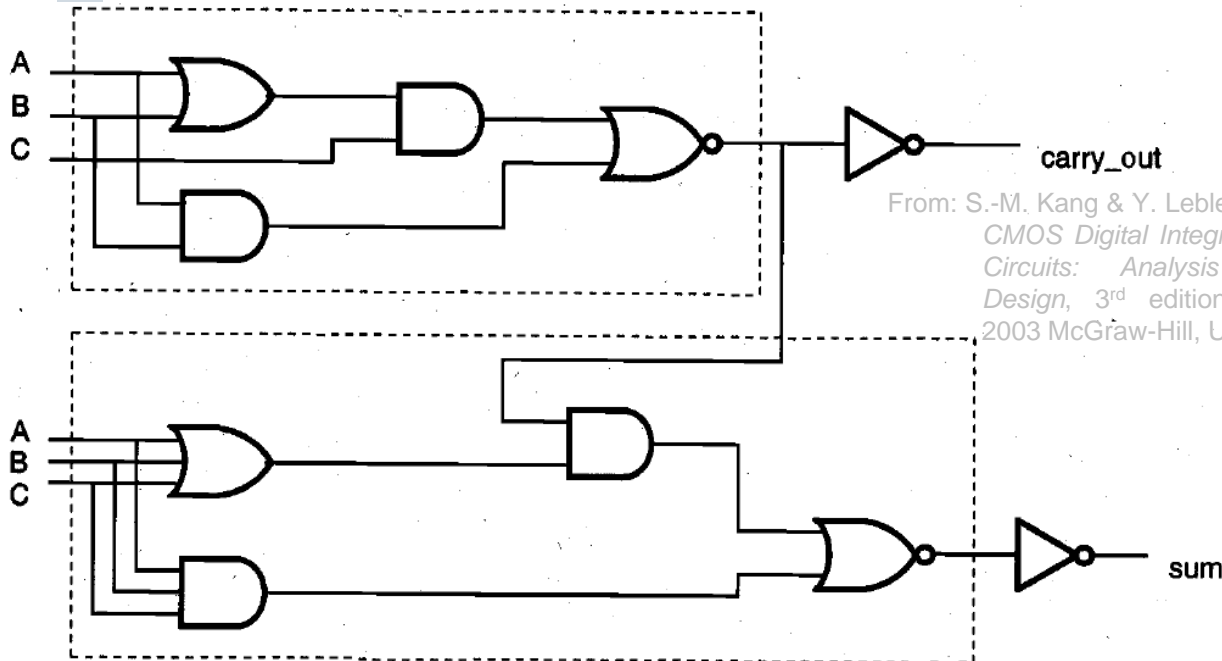
A	B	C	sum_out	carry_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Silicon CMOS Digital ICs

(logic gate level)

- ❑ A one-bit full adder can be implemented using basic logic gates (e.g. AND, OR, NOR and inverter).
- To build more complicated digital circuits, the basic approach is to combine various building-block circuits.



From: S.-M. Kang & Y. Leblebici,
*CMOS Digital Integrated
Circuits: Analysis &
Design*, 3rd edition, ©
2003 McGraw-Hill, USA.

- It is like playing with the LEGO toys though there is design and optimisation methodology.

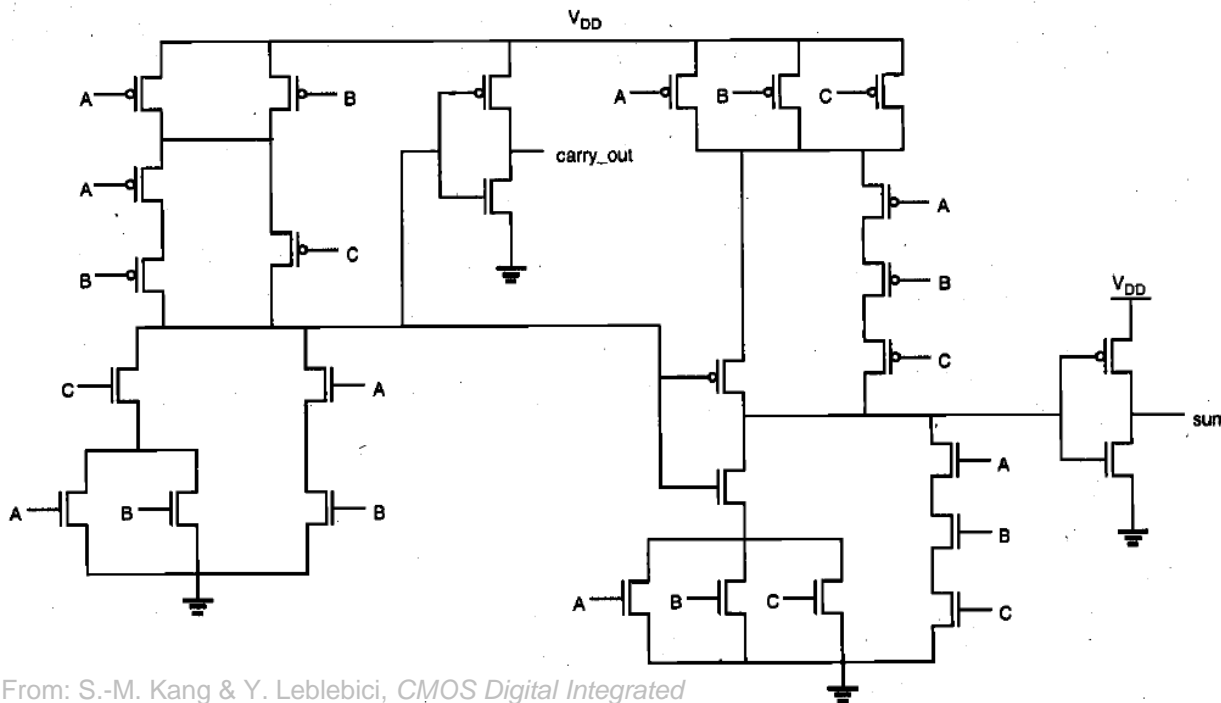


Xi'an Jiaotong-Liverpool University
西交利物浦大學

Silicon CMOS Digital ICs

(transistor schematic design)

- ❑ After the logic-gate level design, the digital circuits can be implemented with transistors (MOSFETs in particular). The following is a transistor schematic.



- the transistors' sizes need to be designed for meeting some current flow requirements, hence the speed etc.



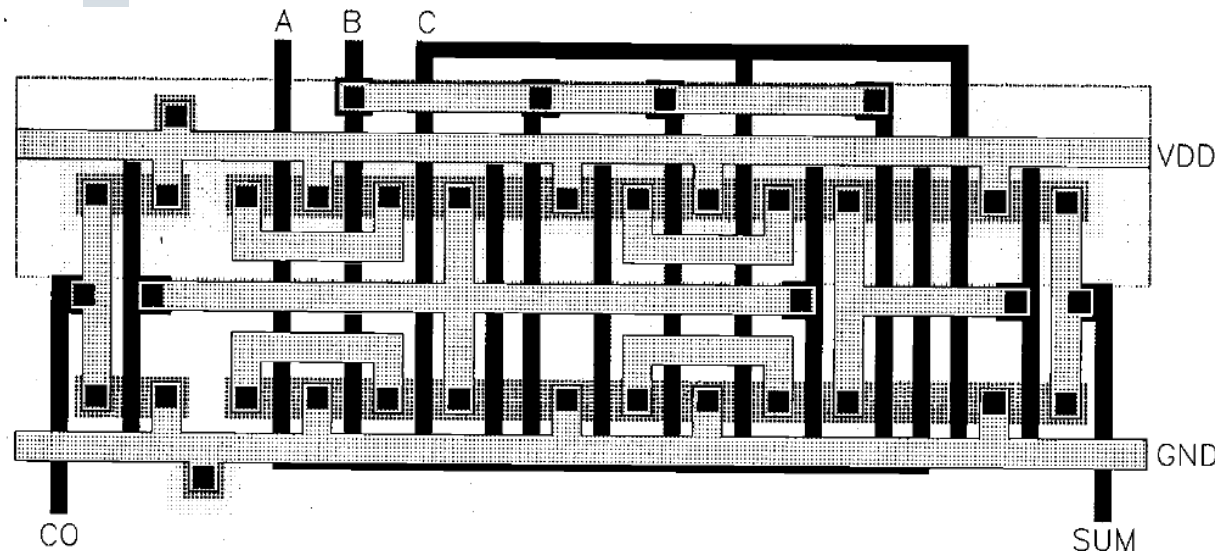
Xi'an Jiaotong-Liverpool University
西交利物浦大學

Silicon CMOS Digital ICs

(physical layout)

- ❑ After determining the transistors' sizes, the physical layout (i.e. the planar geometry of specific layer materials) of each transistor together with the wiring is to be drawn.

From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.



- Other steps like design verification, post-layout simulations are needed in modern computer-aided design of VLSI circuits.



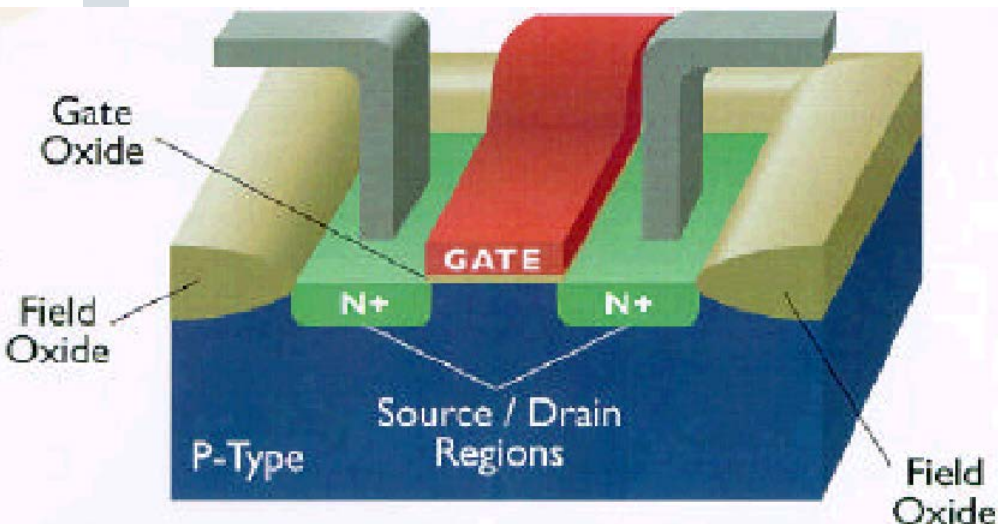
Xi'an Jiaotong-Liverpool University
西交利物浦大學

Silicon CMOS Digital ICs

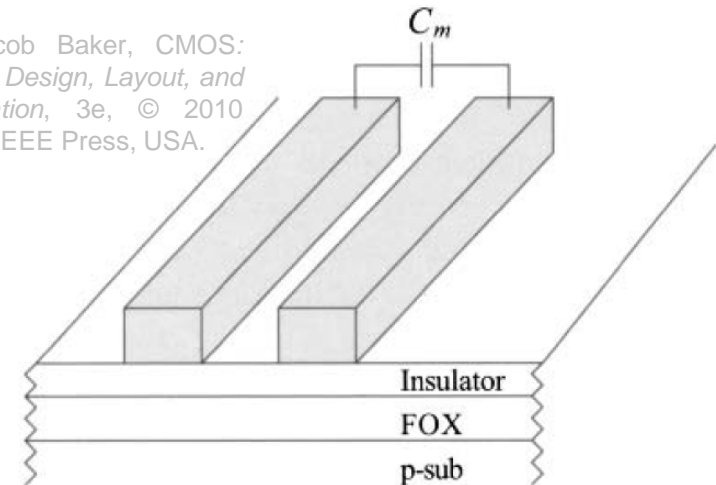
(device-level optimisation)

- ❑ To design CMOS ICs with optimised performance, especially for those critical parts, it needs good understanding of semiconductor electronics, the structure and operation principles of devices.

From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.



From: R. Jacob Baker, *CMOS: Circuit Design, Layout, and Simulation*, 3e, © 2010 Wiley-IEEE Press, USA.



Xi'an Jiaotong-Liverpool University
西交利物浦大學

Silicon CMOS Digital ICs

(mainstream IC technology)

- ❑ Silicon CMOS technology is likely to remain as the dominant technology for the realisation of particular digital ICs or called chips.
 - It is the most **mature** and well-developed semiconductor fabrication technology.
 - It is **reliable** and the designed ICs can be manufactured easily ⇒ **fabless** IC design companies.
 - Silicon CMOS technology is scalable i.e. the transistors can be scaled down in a fairly straight-forward way to increase the speed. It is not possible with the silicon BJT technology. ⇒ **Moore's law** for CMOS technology
 - To sum up, it is competitive in **cost**.



Xi'an Jiaotong-Liverpool University
西交利物浦大學