Lecture 5

of

EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Thursday, 18th October 2018

- **MOS Transistor**
  - structure from MOS capacitor
  - operation modes & I-V characteristics
  - physical understanding (slides 25-36)
  - **physical layout** & capacitance

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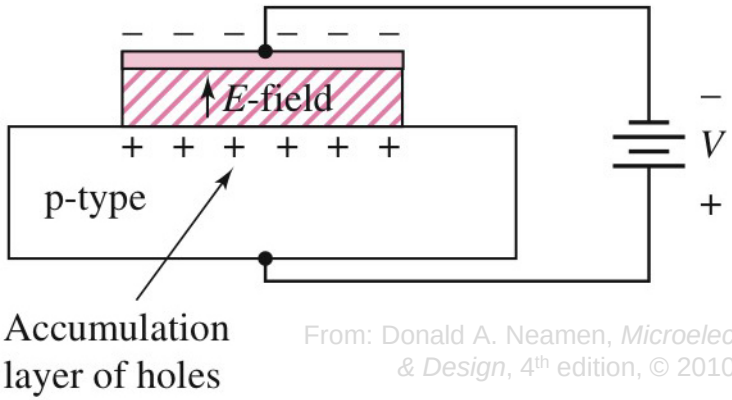
MOS Capacitor

(accumulation of majority carriers)

- We learn about the **MOS capacitor** with three **operation regions**, depending on the voltage applied to the gate (with the substrate grounded): **accumulation**, **depletion**, and **inversion** (**weak & strong inversion**).
  - **accumulation**: **majority carriers** of the substrate ***accumulate*** near the surface (oxide-semiconductor interface), with the carrier concentration even higher than the equilibrium concentration.



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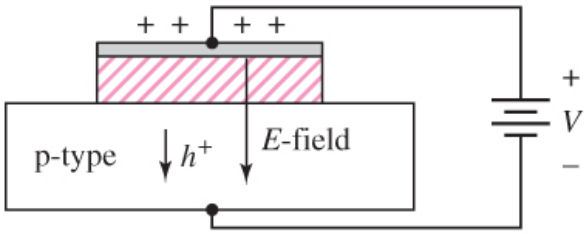
MOS Capacitor

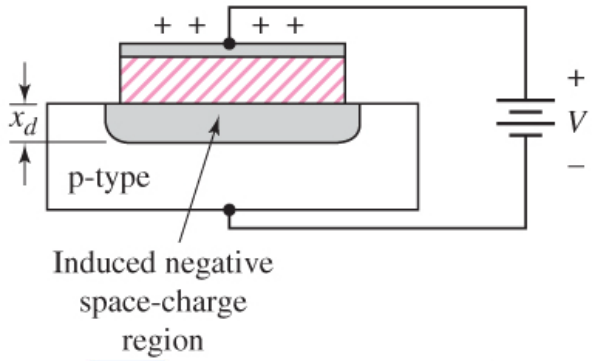
(depletion region & width)

- **depletion**: **majority carriers** of the substrate are ***depleted*** beneath the surface, resulting in a region without any mobile carriers but fixed dopant ions in space; it's called a **depletion region** or **space-charge** region.
- This is similar to the reverse-biased ***p-n*** junction.

$$x_d = \sqrt{\frac{2\varepsilon_{Si}\left|\phi_s - \phi_F\right|}{qN_a}}$$

x_d : depletion layer thickness





p-n junction:

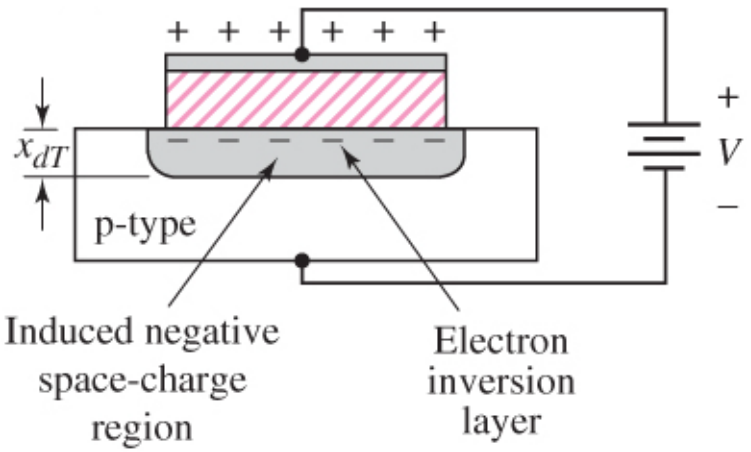
$$W_0 = \sqrt{\frac{2\varepsilon_{Si}\left(N_a + N_d\right)\left|V_{bias} - V_{bi}\right|}{eN_aN_d}}$$

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

MOS Capacitor

(strong inversion)

- **inversion**: a very thin charge layer of **minority carriers** is formed right beneath the surface of the semiconductor when an appropriate gate voltage is applied.



From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

- When the **minority carrier concentration** of the **inversion layer** is the same as the majority carrier concentration in the substrate, it is called **strong inversion**.

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MOS Capacitor

(inversion & threshold voltage)

- At ***strong* inversion**, the corresponding gate voltage is called the **threshold voltage V_T**:

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_a\varepsilon_{Si}(2\phi_F)}}{C_{ox}}$$

- When the minority carrier concentration in the inversion layer is smaller than the majority carrier concentration, it is called ***weak* inversion**.
- In ***weak* inversion**, the gate voltage is slightly below the **threshold voltage V_T**.
- This accounts for the **sub-threshold characteristics** of the MOS transistor.

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MOS Capacitor

(2-terminal device)

- If the substrate is not connected to ground but with a biased voltage V_B, V_T needs to be modified as follows:

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\phi_F - V_B)}}{C_{ox}}$$

- The MOS capacitor is a two-terminal device and it is not very useful by itself in digital ICs.
  - two electrodes: **gate** (denoted by G) & **substrate** (or called **bulk**/**body**) (denoted by B)
  - The MOS capacitor is however useful in analogue ICs in some circuits as well as CCD image sensors.
  - The ***p*-*n*** junction is also a 2-terminal device.

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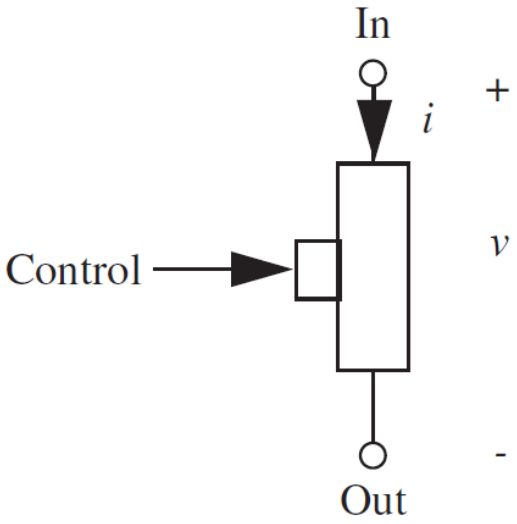
MOS Capacitor

(for constructing 3-terminal device)

- The **MOS capacitor** structure can be used for constructing a three-terminal device.
- In a 3-terminal device, the current flowing through the other two terminals can be ***controlled*** by the third terminal.



- Such a 3-terminal device is commonly used as a **switch**, especially in digital circuits.

From: Anant Agarwal & Jeffrey Lang, Foundations of Analog and Digital Electronic Circuits, © 2005 Elsevier, UK.

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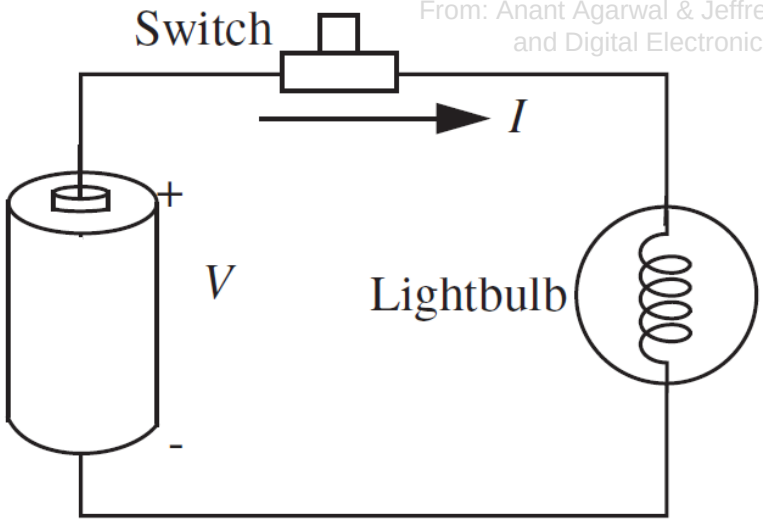
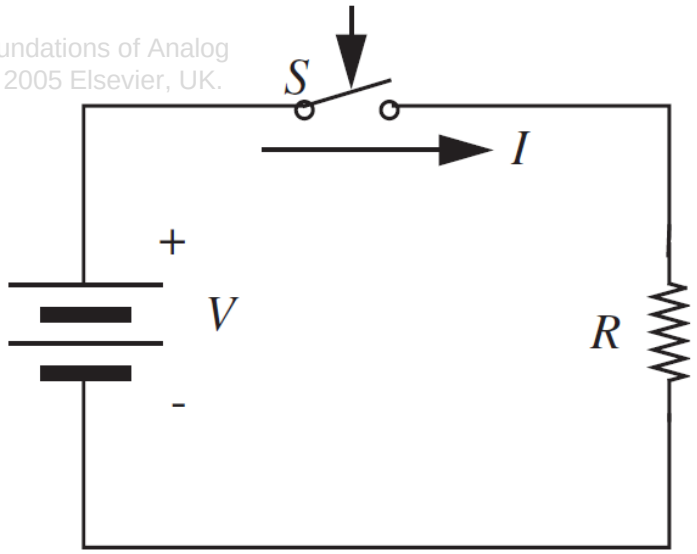
Switch & Digital States

(binary states)

- When the **switch** is turned on, it can be used to represent a digital state “1”; “0” when off.





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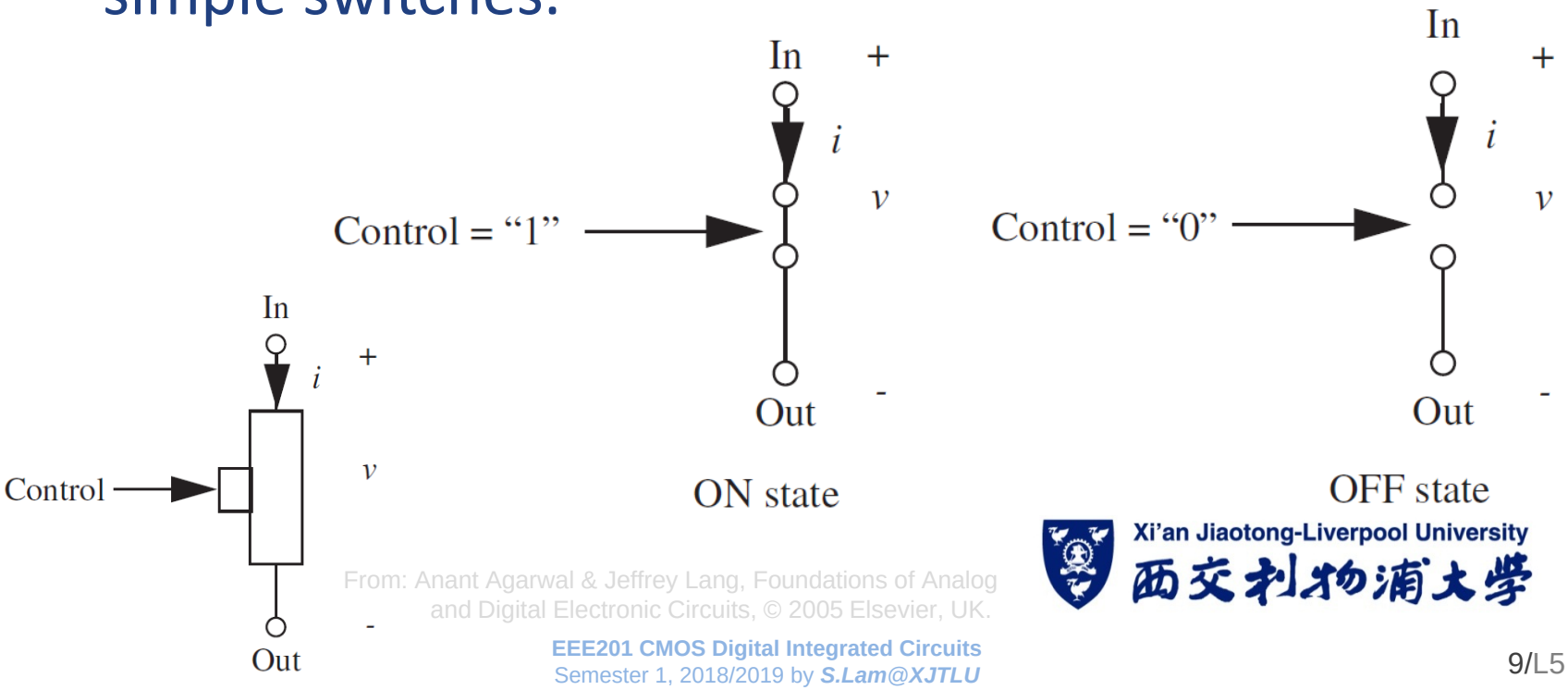
3-Terminal Device

(simple switches for building logic circuits)

- More importantly, the **switch** itself can be controlled by digital states “1” or “0”.
- Complex **logic circuits** can then be built from such simple switches.



From: Anant Agarwal & Jeffrey Lang, Foundations of Analog and Digital Electronic Circuits, © 2005 Elsevier, UK.

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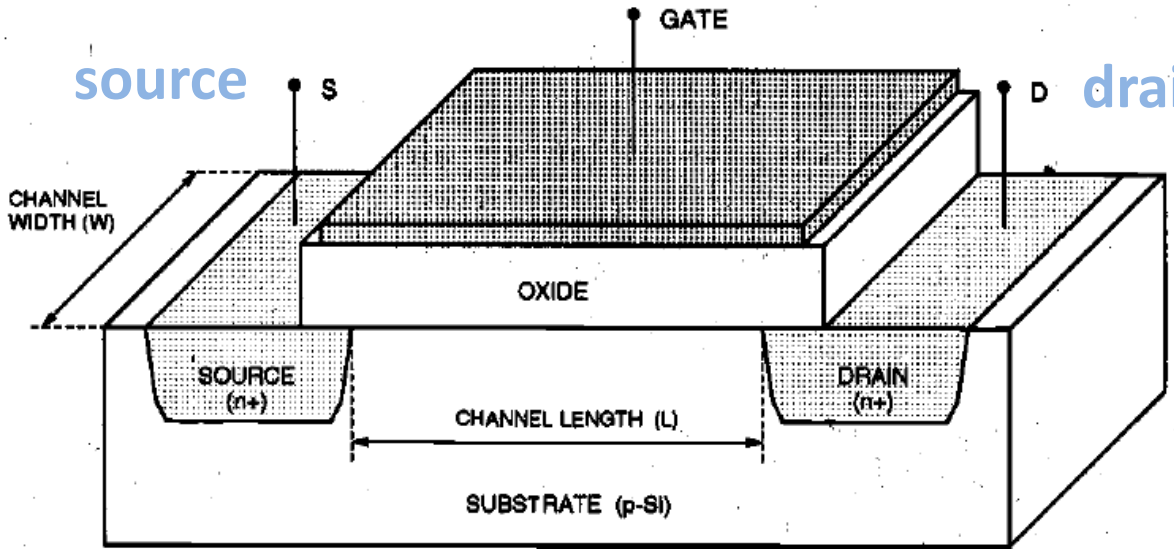
MOSFET from MOS Capacitor

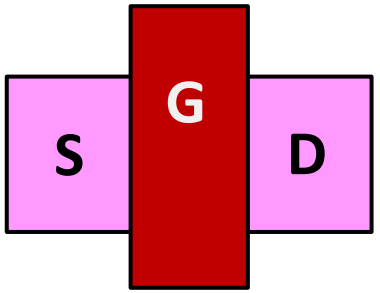
(physical structure)

- A highly useful 3-terminal device can be constructed from the **MOS capacitor** with the basic structure shown here:

From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.



layout:
(top view)



- It is called the **MOS field-effect transistor** (**MOSFET**) or simply **MOS transistor**.

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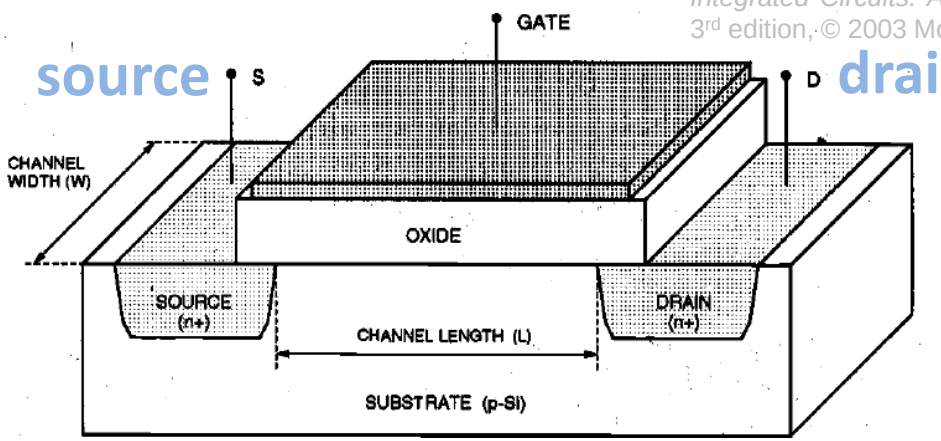
MOSFET from MOS Capacitor

(diffusion regions)

- In addition to the **gate electrode** and **substrate** (***p***-type in this case) of the **MOS capacitor**, there are two highly doped regions (called diffusion regions) on two sides of the gate.
  - The two diffusion regions are called the **source** and the **drain** which are the *conducting* terminals of the **MOS transistor**.



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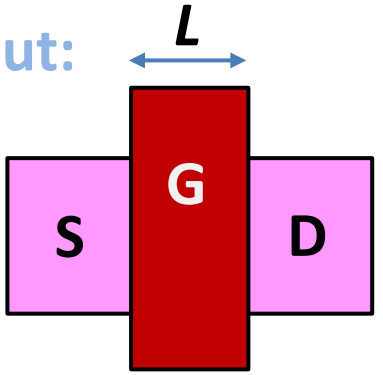

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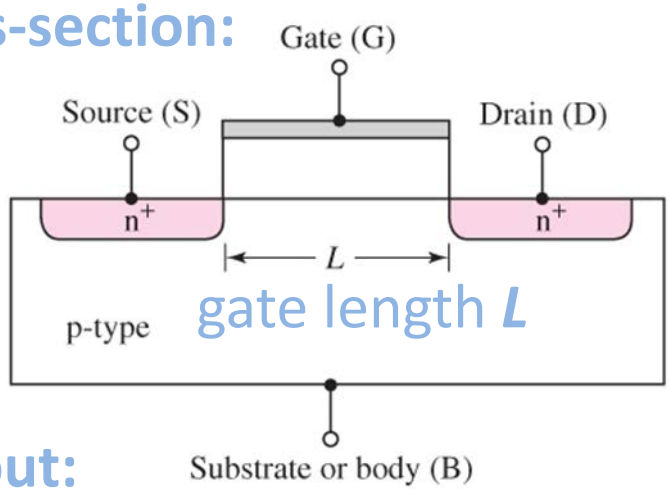
MOSFET from MOS Capacitor

(source & drain terminals)

- The basic structure of the **MOS transistor** is completely *symmetrical* with respect to the **source** and **drain** regions.

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

cross-section:



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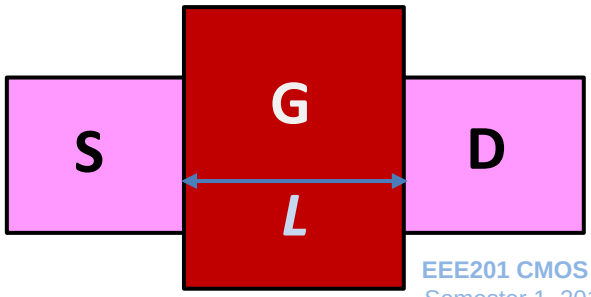

- The different roles of the **source** and **drain** terminals are defined by the applied terminal voltages and the current flow, especially in digital integrated circuits.
- **source** & **drain** for the carriers

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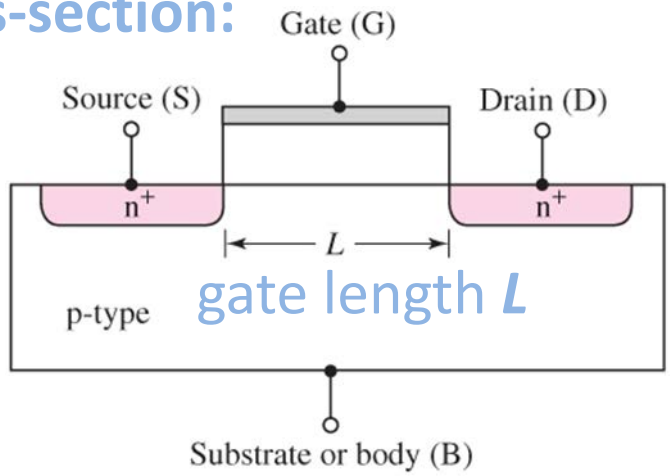
MOSFET from MOS Capacitor

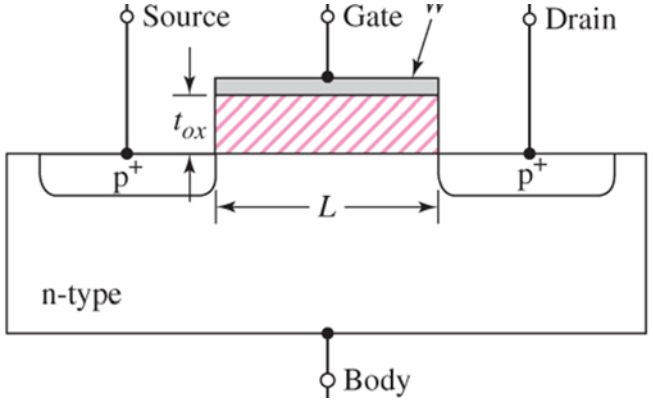
(nMOS & pMOS transistors)

- The structure of the nMOS and pMOS transistors are very similar. The differences are in the diffusion regions and the substrate.

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

cross-section:





nMOS: **n-type source** & **drain diffusion regions**; **electrons** as carriers in the **channel**

pMOS: **p-type diffusion regions**; **holes** as carriers in the **channel**

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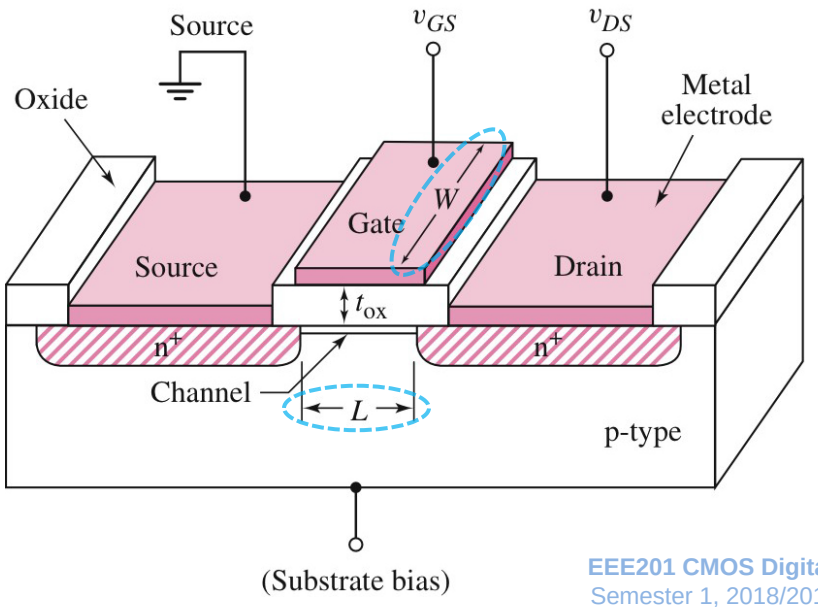
MOSFET from MOS Capacitor

(conduction between source & drain)

- When an appropriate voltage is applied to the gate, a ***conducting* channel** is formed between the **source** and **drain**.

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

  - The ***conducting* channel** is simply the **inversion layer** in the MOS capacitor.



  - The distance between the **source** and **drain** regions is called the **channel length** which is essentially the same as the **gate length** (defined by geometry).

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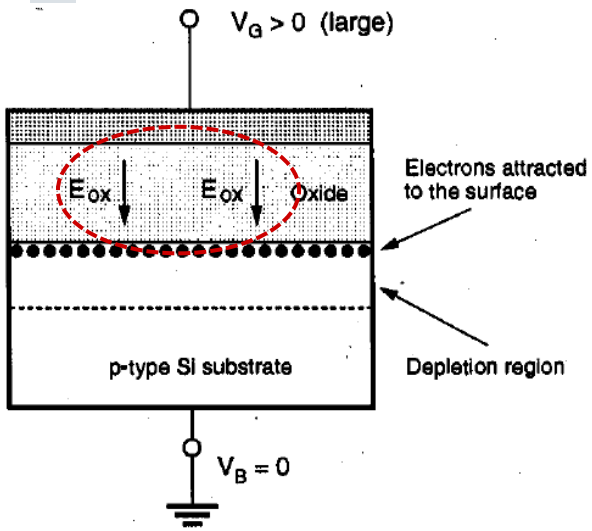
MOSFET from MOS Capacitor

(conduction controlled by electric field)

- Depending on the applied gate voltage (as in the case of the **MOS capacitor**), the conduction between the source and drain regions can be controlled from strong to weak and even to cut-off.

From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.



- As the conduction is *controlled* by the **electric field** because of the voltage applied to the gate, which is insulated from the channel, it is named ***field-effect*** **transistor**.
- Note that there is no electric current flowing through the gate, in contrast to the bipolar junction transistor (BJT) case.

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MOSFETs

(3-terminal device)

- There are several variants of the MOSFET such as the **enhancement-mode** MOSFET which can be regarded as the normally-off transistor.
  - Compared with the enhancement-mode MOSFET, the **depletion-mode** MOSFET can be regarded as the normally-on transistor.
- Looking at the basic structure of the MOSFET, it is a in fact a 4-terminal device. When used in CMOS circuits, two terminals (namely, the **source** and **body**) are typically connected together.
  - 3-terminal device

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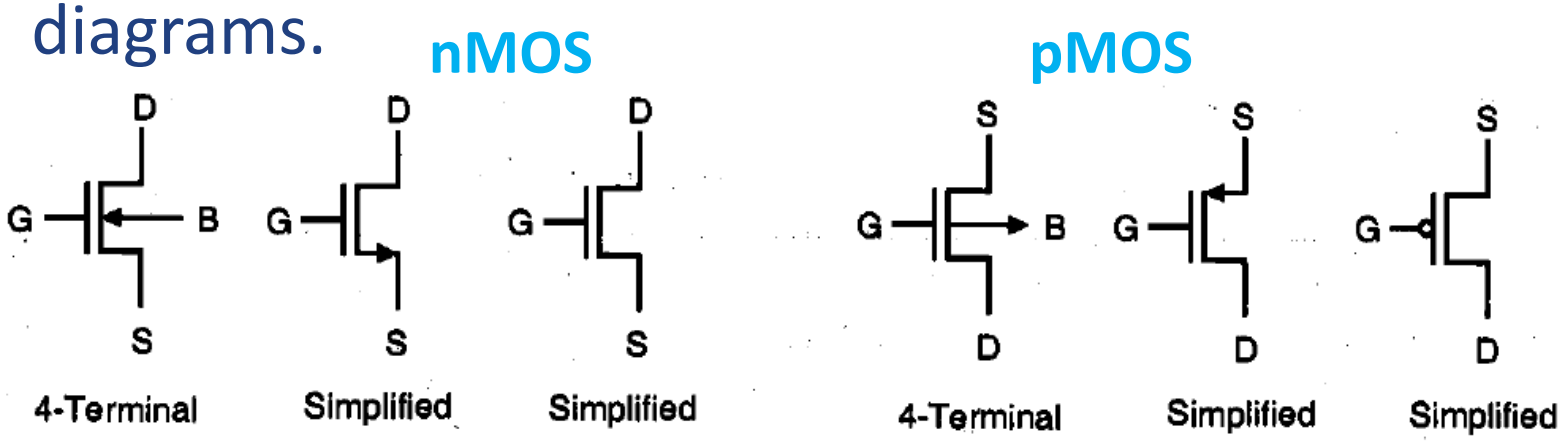
MOSFETs
(circuit symbols)

- The **MOS field-effect transistors** (**MOSFET**s) are represented using circuit symbols in circuit diagrams.



  - Note that the arrows in the MOSFETs' circuit symbols represent the current flow direction, as a sign of the ***p*-*n*** junction.
  - Simplified symbols are used usually in digital circuits.

From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.

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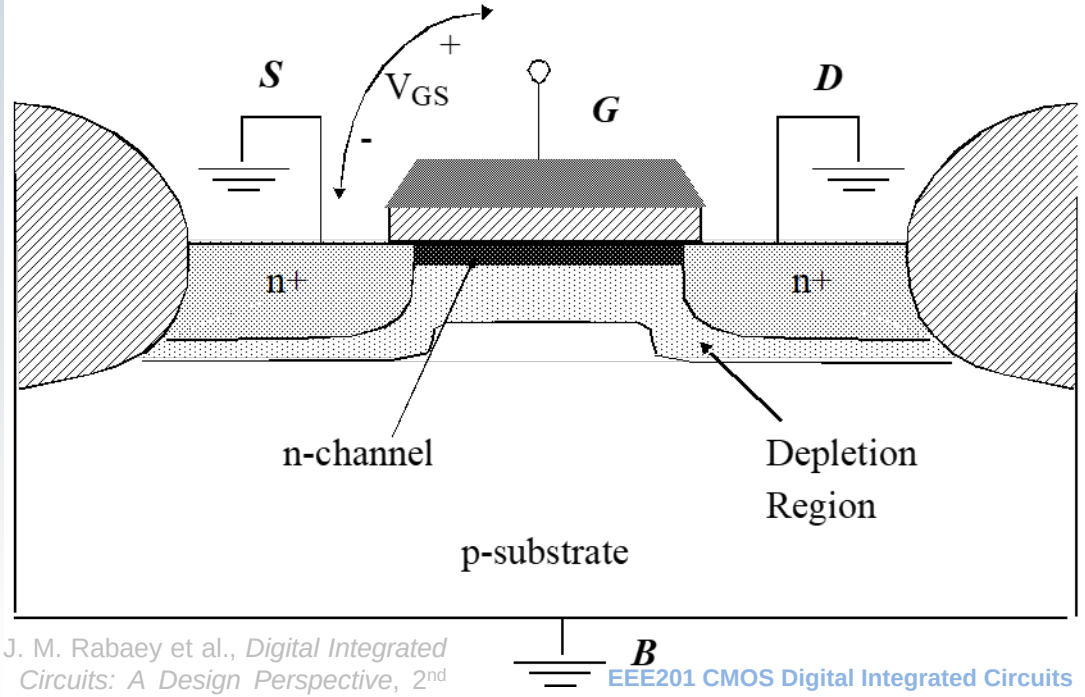
MOSFET - as MOS Capacitor

(source/drain tied together)

- Regardless of the apparent complexity of the MOSFETs of various types or as a 4-terminal device, the **transistor operation** can be understood from the basic principles of the **MOS capacitor**.



- When the **source**, **drain** and **body** are connected together, the 4-terminal **MOSFET** becomes the 2-terminal **MOS capacitor**.

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From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

MOSFET's Operation Regions

(I_{DS} dependent on V_{GS} & V_{DS})

- With the formation of the ***conducting*** **channel** controlled by the applied **gate voltage V_{GS}**, the current flow I_{DS} between the **source** and **drain** depends on the voltage V_{DS} applied across the two regions.

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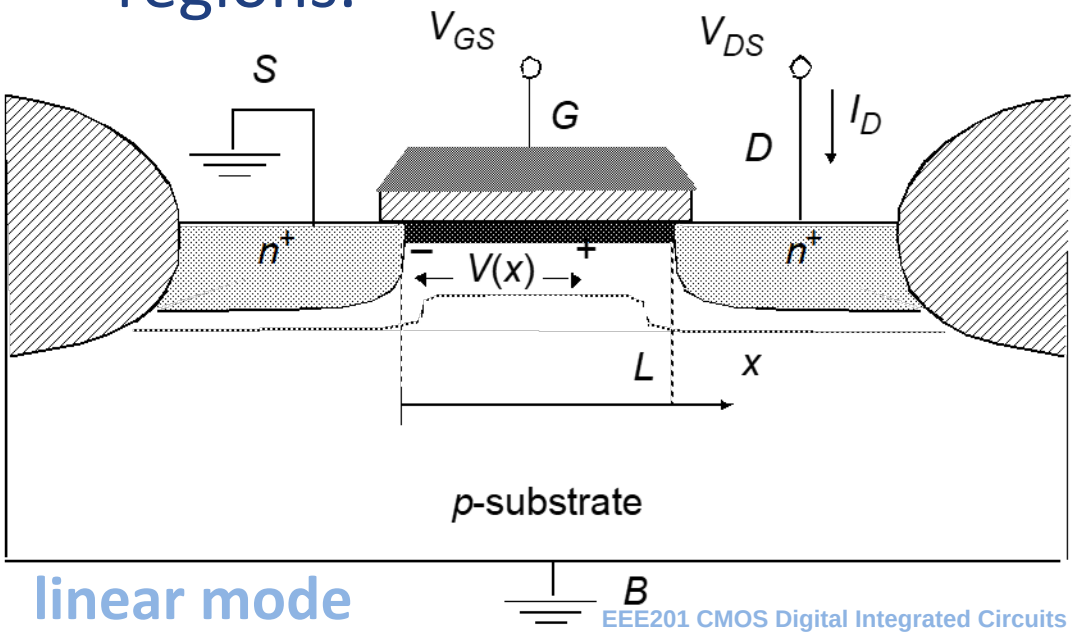

- The current I_{DS} of the **MOSFET** in general is a function of V_{GS} and V_{DS}.

linear mode

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MOSFET's Operation Regions

(channel pinch-off & saturation region)

- With the ***conducting* channel** formed between the **source** and **drain**, there are two major operation regions of the MOSFET: the **saturation region** and the **triode region** (which is also called the **linear region**).

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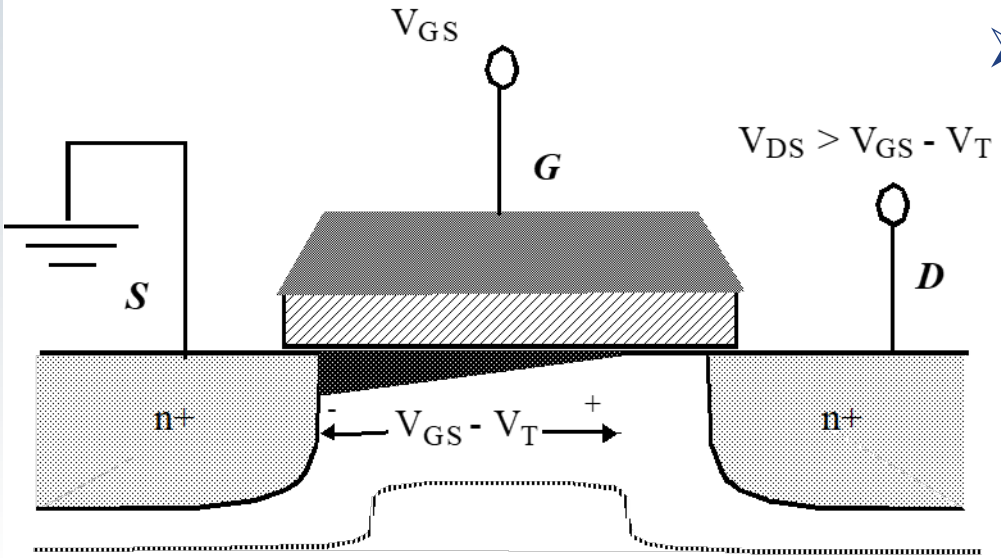

saturation mode

- Note the different situations of the ***conducting* channel** in the **saturation region** and the **triode region**.

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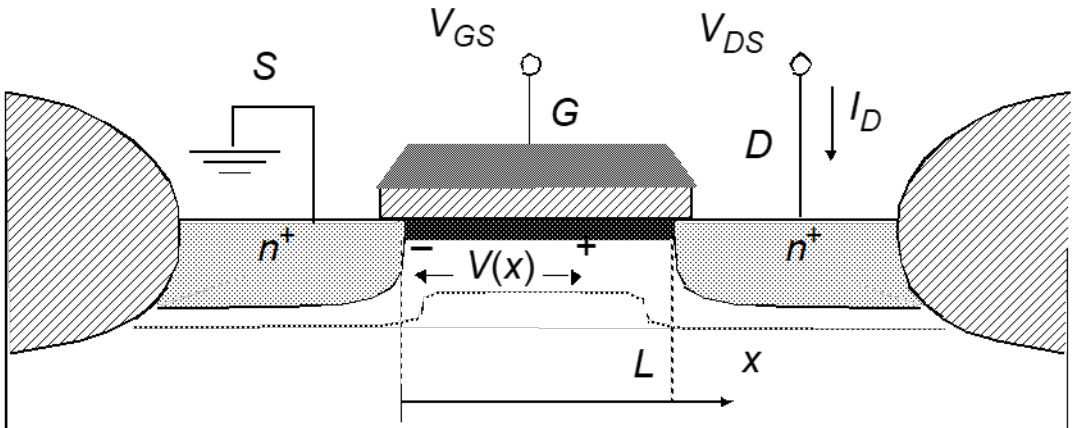
MOSFET's I-V Characteristics

(linear region)

- When $V_{GS} > V_T$ but with small V_{DS}, the current flow I_{DS} between the **source** and **drain** is roughly linearly dependent on the voltage V_{GS} & increases with V_{DS}.

$$I_{D,lin} = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \text{ when } V_T \le V_{GS} \,\&\, V_{DS} \le V_{GS} - V_T$$



From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

- In the linear region, the **channel** is almost uniform from the source to drain.

linear mode

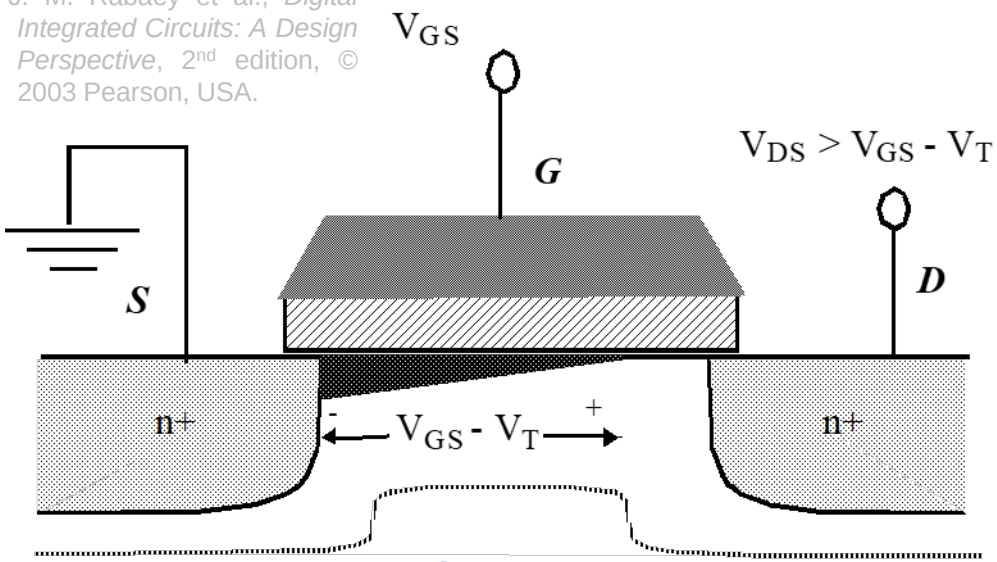
MOSFET's I-V Characteristics

(saturation region)

- In the **saturation region**, **pinch-off** of the channel occurs at the drain end and the current no longer increases with the V_{DS} in general.

$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \text{ when } V_T \le V_{GS} \le V_{DS} + V_T$$

From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.



saturation mode

- The channel pinch-off occurs because of the reversed-biased ***p-n*** junction at the drain, depleting carriers as V_{DS} keeps increasing.

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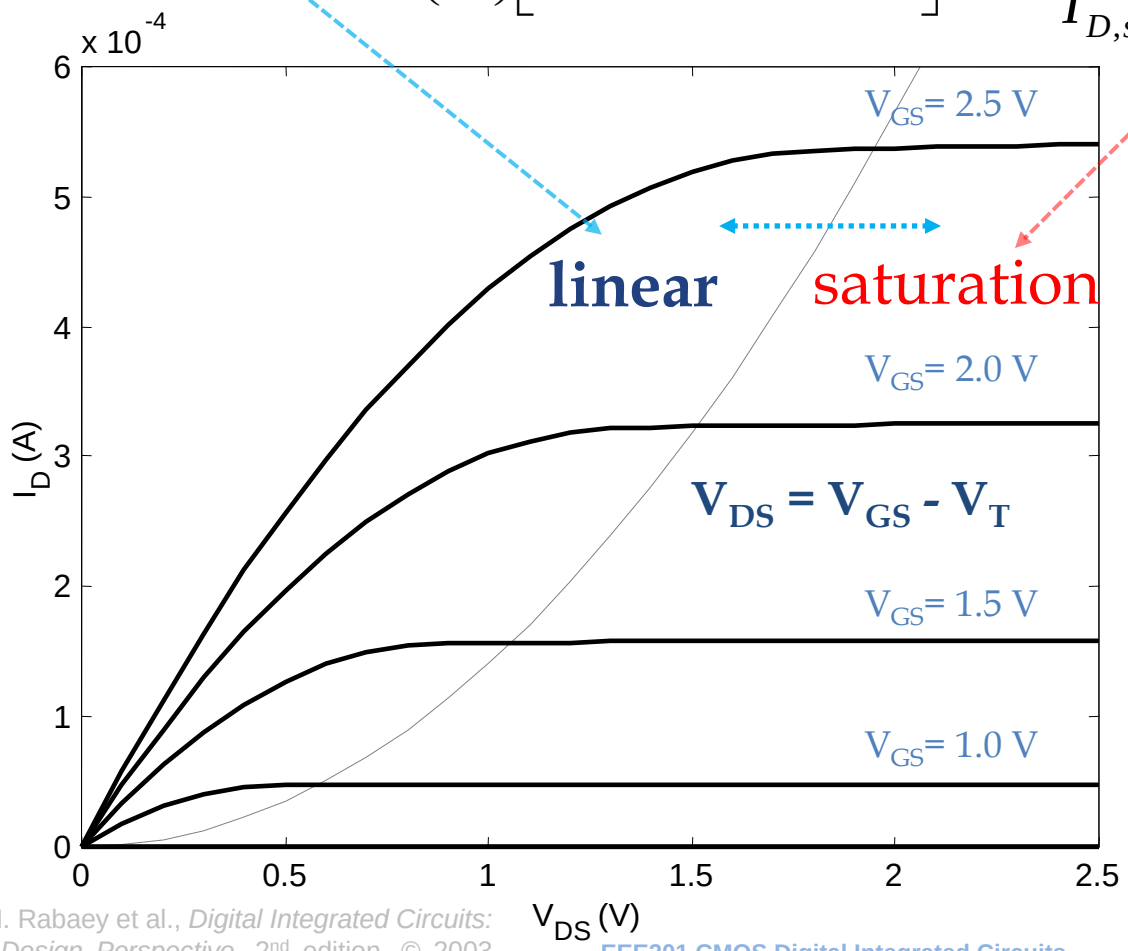
MOSFET's I-V Characteristics

(output characteristics – I_{DS} vs. V_{GS})

$$I_{D,lin} = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$



- This model for the drain current is not accurate, especially in CMOS technology with a short channel.

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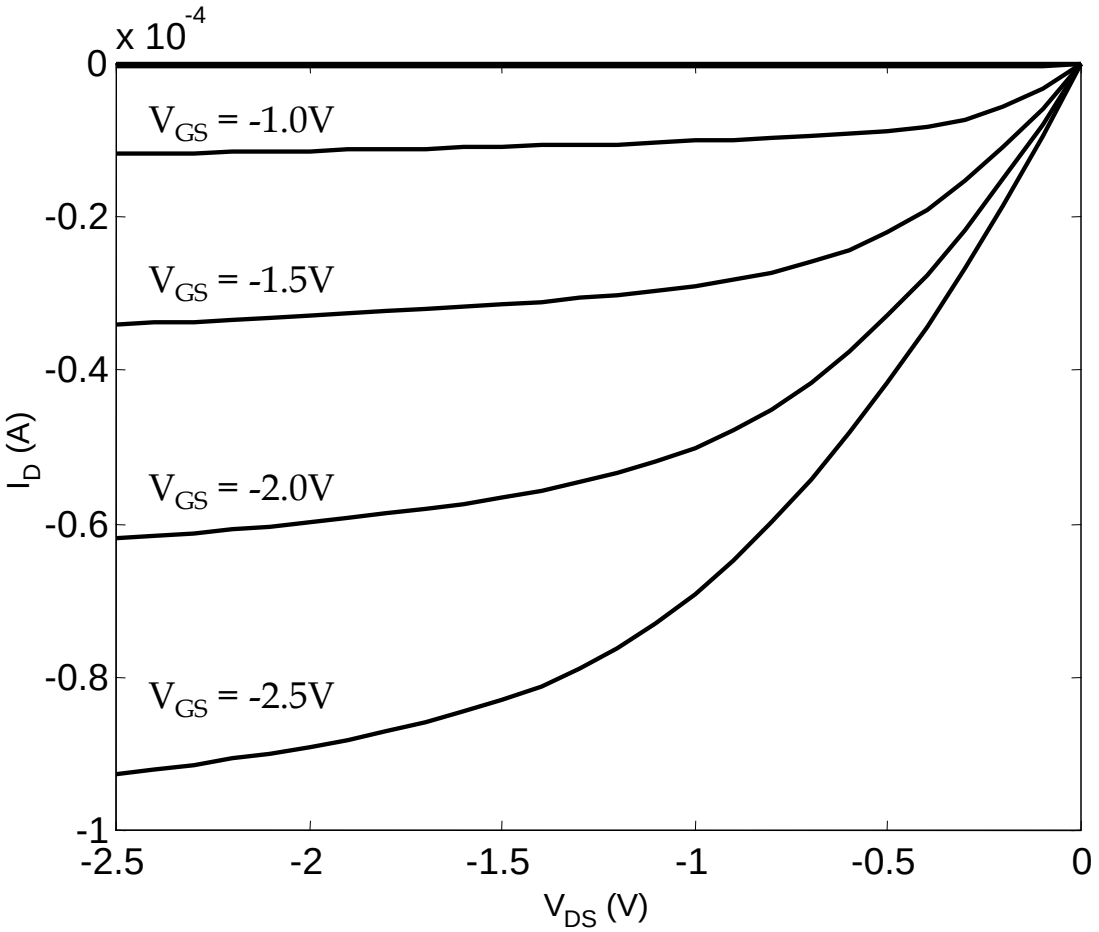
MOSFET's I-V Characteristics

(p-type MOSFET)



From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

- The derived equations for the nMOS transistor are applicable to the pMOS transistors but with the **polarities** of all **voltages** and **currents** reversed.

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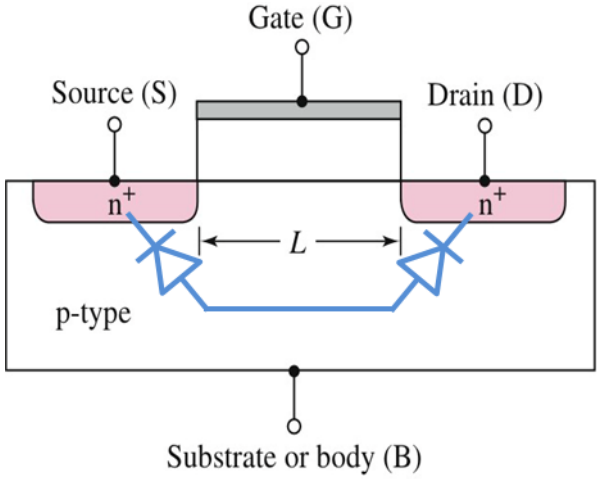
MOS Field-Effect Transistor

(basic transistor operation)



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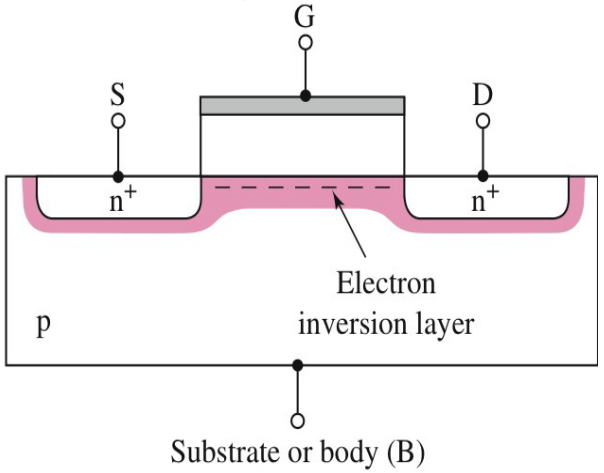

- With zero bias applied to the gate, there is no electrical conduction between the source and drain terminals.
  - This is equivalent to two diodes connected in series but of opposite direction to each other.
- When a large enough voltage is applied to the gate, an **inversion layer** is created and ***channels*** the source & drain terminals.

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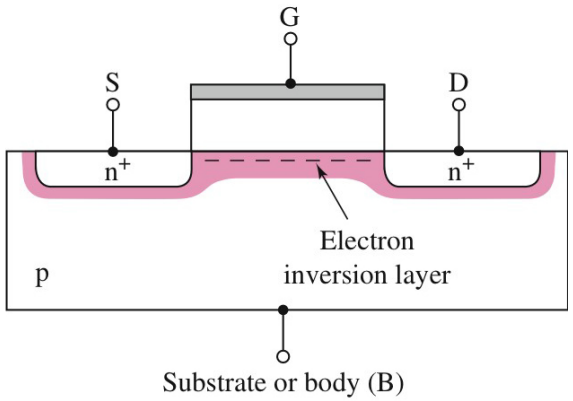
MOS Field-Effect Transistor

(basic transistor operation)

- With the **inversion layer** as a ***channel***, electric current can be generated between the **source** and **drain** terminals if a voltage is applied to the two terminals.



- Since a voltage must be applied to the gate to create the **inversion layer**, this type of transistors is called **enhancement-mode MOSFETs**.
- It is called an ***n*-channel** MOSFET (or **nMOSFET**) if the carriers of the **inversion layer** are **electrons**; (**pMOSFET** for holes.)

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MOS Field-Effect Transistor

(channel & current)

- In an **n**MOSFET, electrons flow from the **source** to the **drain** if a drain-to-source voltage is applied to the two terminals.
  - This means that the conventional current enters the drain and leaves the source in an **n**MOSFET.
- The magnitude of the current depends on the amount of charge in the **inversion layer**.

$$\boldsymbol{J}_{drift} = \sigma \boldsymbol{E} = (e\boldsymbol{n}\mu_n + e\boldsymbol{p}\mu_p)\boldsymbol{E}$$

- Since the gate terminal is electrically separated from the **channel** by a thin oxide or insulator layer, there is no gate current in MOSFETs.
  - The **channel** is also separated from the substrate by the depletion region $\Rightarrow$ no current through the substrate *essentially*.

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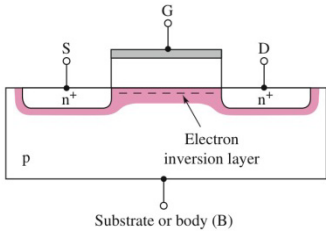
Threshold Voltage of MOSFETs

("turn-on" voltage)

- Since current conduction between the source and drain depends on the channel formation, the **threshold voltage**, denoted by V_{TN} for **n**MOSFETs (V_{TP} for pMOSFETs), is defined:



  - the applied **gate voltage** needed to create the inversion layer in which the carrier density is equal to the concentration of the majority carrier in the semiconductor substrate.
  - In simple terms, it is the **gate voltage** required to "**turn on**" the MOSFETs.
  - For enhancement-mode **n**MOSFETs, V_{TN} is a positive gate voltage;
  - V_{TP} is a negative gate voltage for **p**MOSFETs.

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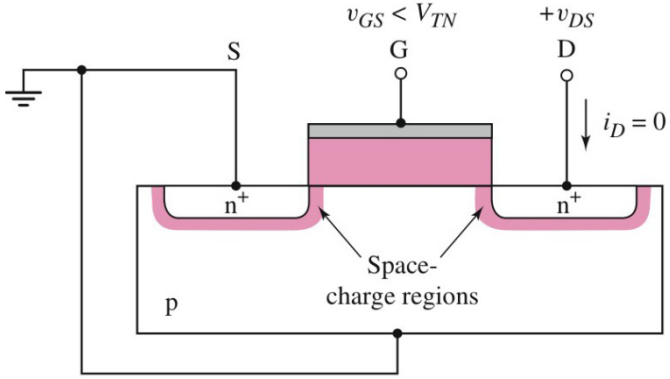
Threshold Voltage of MOSFETs

(drain current)

- In **n**MOSFETs, the **source** and the substrate are usually connected to the ground (i.e. 0 V).



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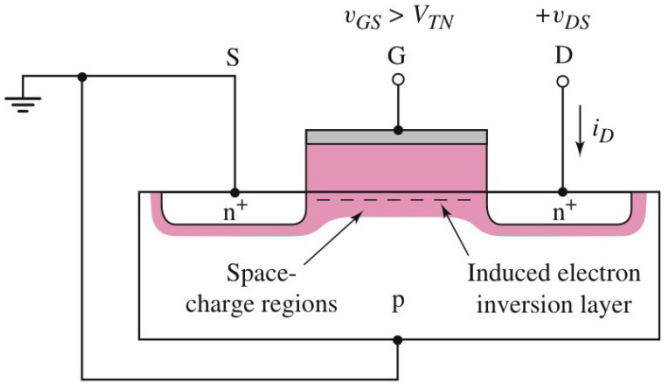

- When the gate-to-source voltage $\boldsymbol{v_{GS}}$ is smaller than $\boldsymbol{V_{TN}}$, there is no inversion layer.

  $\Rightarrow$ no drain current *essentially* even with a drain-to-source voltage $\boldsymbol{v_{DS}}$.

- When $\boldsymbol{v_{GS} > V_{TN}}$, an inversion layer is created and there is a drain current $\boldsymbol{i_D}$ with an applied *small* $\boldsymbol{v_{DS}}$.

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I-V Characteristics of MOSFETs

(drain current for small enough v_{DS})

- When $v_{GS} < V_{TN}$, the drain current i_D is *essentially* 0.
- When $v_{GS} > V_{TN}$, i_D increases with the applied v_{DS} up to a certain point.

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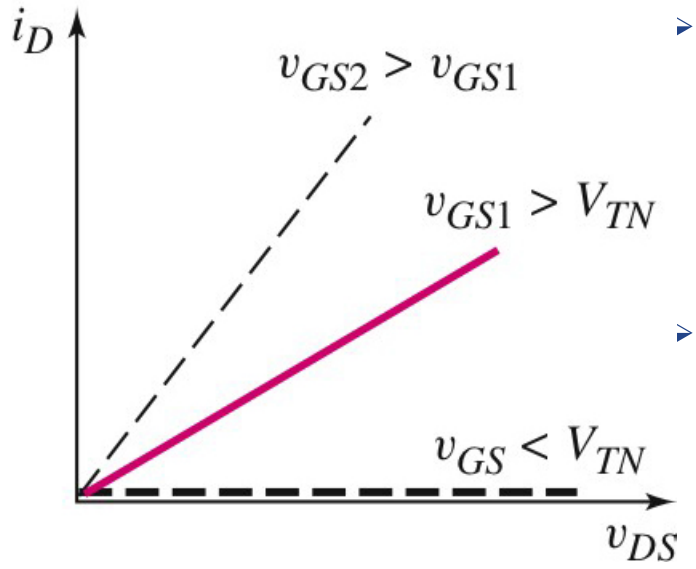

- For a larger $v_{GS2} > V_{TN}$, the inversion layer has a larger charge carrier density. Hence, i_D is larger for a given value of v_{DS}.
- The increase in i_D *almost linearly* with v_{DS} is only valid for small v_{DS}. This region of MOSFET operation is called the **triode region**.

Note the **voltage notation** of e.g. v_{DS} with the dual subscript, which denotes the voltage between the drain (D) and source (S), with the 1st subscript (D) being the positive voltage and the 2nd subscript (S) being the negative voltage (i.e. $v_D - v_S$).

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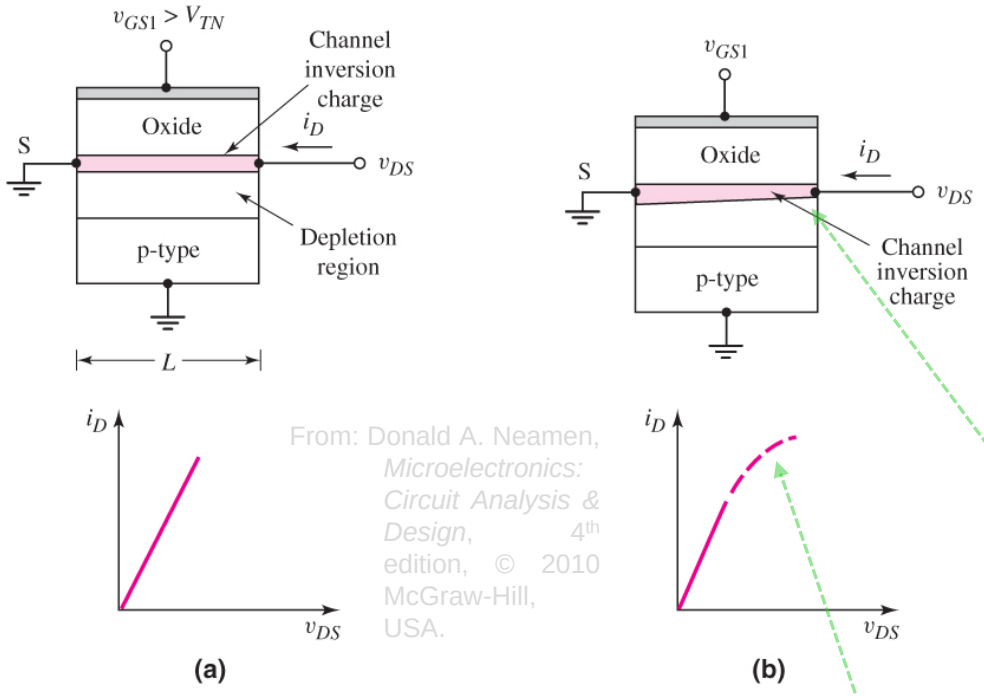
I-V Characteristics of MOSFETs

(triode region)



- When $v_{GS} > V_{TN}$ and *small enough* v_{DS}, i_D increases with the applied v_{DS}. (Fig. (a))
- As v_{DS} increases further, the voltage drop across the oxide (i.e. v_{GD}) near the drain decreases.
- As a result, the induced **inversion layer** near the drain has a lower charge carrier density (Fig. (b)).
  - The incremental conductance of the channel near the drain then decreases (i.e. $\Delta i_D / \Delta v_{DS}$ decreases).

$$J_{ndrift} = \sigma_n E = (en\mu_n)E$$

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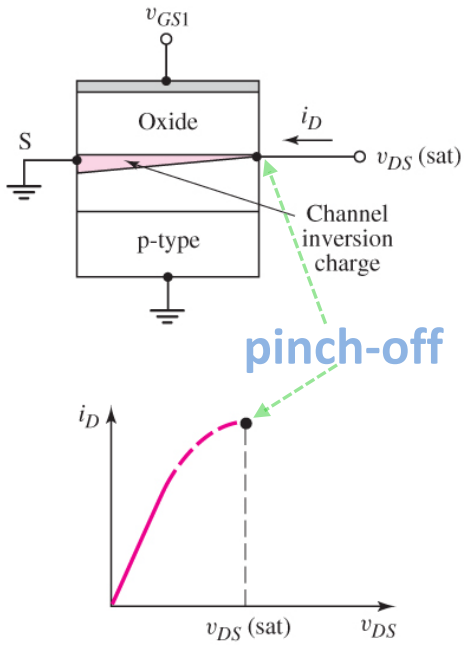
I-V Characteristics of MOSFETs

(pinch-off region)



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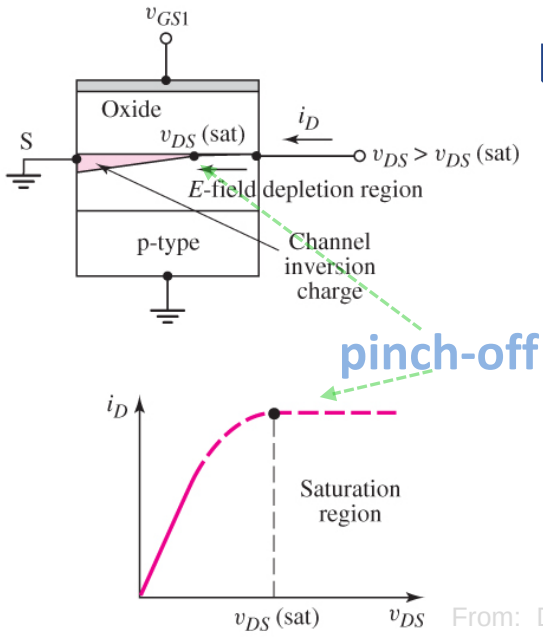
- As v_{DS} increases to the point that the voltage drop across the oxide at the drain (i.e. $v_{GD} = v_{GS} - v_{DS}$) is equal to V_{TN}, the induced **inversion** carrier density is zero at the drain.
  - The MOSFET is said to be at the **pinch-off** condition when $v_{GS} - v_{DS} = V_{TN}$.
  - The incremental conductance of the channel at the drain becomes zero (i.e. $\Delta i_D / \Delta v_{DS} = 0$ *ideally*).
- A voltage $v_{DS(sat)}$ is defined when the **inversion layer** starts to be ***pinch off*** at the drain:

$$v_{DS(sat)} = v_{GS} - V_{TN}$$

I-V Characteristics of MOSFETs

(saturation region)



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- When v_{DS} increases beyond $v_{DS(sat)}$, the **pinch-off** point (at which the inversion charge is just zero) moves toward the source terminal.
  - This is called the **saturation region** of the MOSFET when $v_{DS} > v_{DS(sat)}$.
- In the **saturation region** of an nMOSFET, electrons enter the channel at the **source** and travel through the **channel** toward the **drain**, and then at the point where the inversion carrier density goes to zero, are injected into the ***E*-field depletion region** and are *swept* to the **drain**.

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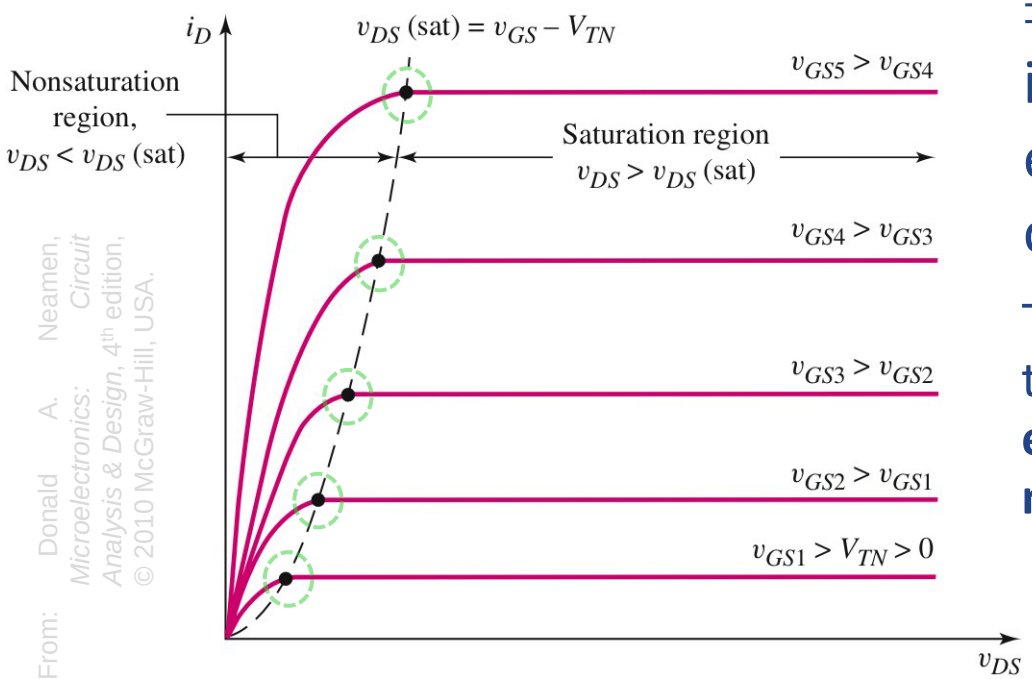
I-V Characteristics of MOSFETs

(***I-V*** curves)

- The dependence of the **drain current i_D** on the applied **gate-to-source voltage v_{GS}** and the **drain-to-source voltage v_{DS}** can be reflected in a family of i_D - v_{DS} curves.
  - Note that $v_{DS(sat)}$ is a function of the applied v_{GS}.



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$\Rightarrow$ the voltage $v_{DS(sat)}$ is a single point on each of the i_D - v_{DS} curve.

The *I-V* curves shown on the left is of an **enhancement-mode nMOSFET** (based on V_{TN}).

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I-V Characteristics of MOSFETs

(mathematical relationship)

- The i_D - v_{DS} characteristics of the MOSFET can be derived from fundamental principles but the derivation is not required in this class. The mathematical relationships are simply given here.
  - In the **triode region** (also called non-saturation region) where $v_{DS} < v_{DS(sat)}$, $i_D = K_n\left[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2\right]$
  - In the **saturation region** where $v_{DS} > v_{DS(sat)}$,

$$i_{Dsat} = K_n\left[(v_{GS} - V_{TN})^2\right]$$

i_{Dsat} can be obtained by setting $v_{DS} = (v_{GS} - v_{TN})$ in the 1st eqn.

  - where K_n is referred as the conduction parameter for simplicity:

$$K_n = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right) = k_n'\frac{W}{L}$$

$C_{ox} = \varepsilon_{ox} / t_{ox}$ being the MOS **capacitance per unit area** and $\varepsilon_{ox} = (3.9)(8.85\times10^{-12})$ F/m for SiO_2

  - Note that K_n is a function of both electrical & geometrical parameters.

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p-type MOSFET
(***p***-channel)

- The complementary transistor of the ***n***-channel MOSFET is a ***p***-channel MOSFET.
  - The transistor structure and operation are similar.

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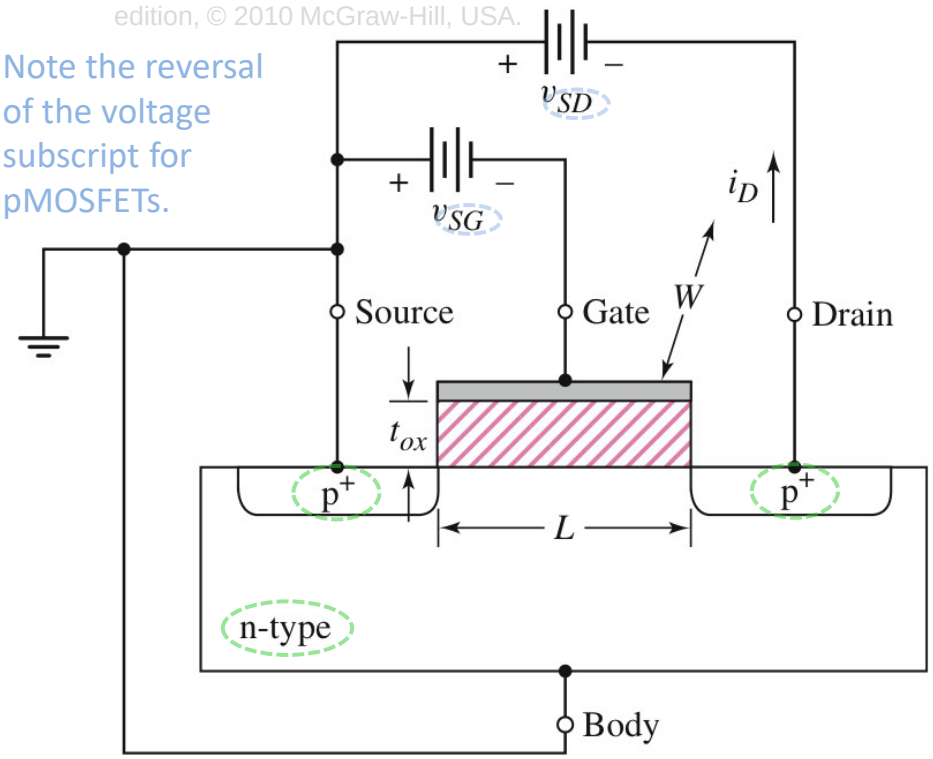
Note the reversal of the voltage subscript for pMOSFETs.



  - The differences are:

    the substrate is ***n***-type and the S/D regions are ***p***-type for pMOSFET;

    holes are the charge carrier in the **channel**;

    the threshold voltage is negative (i.e. $V_{TP} < 0$).

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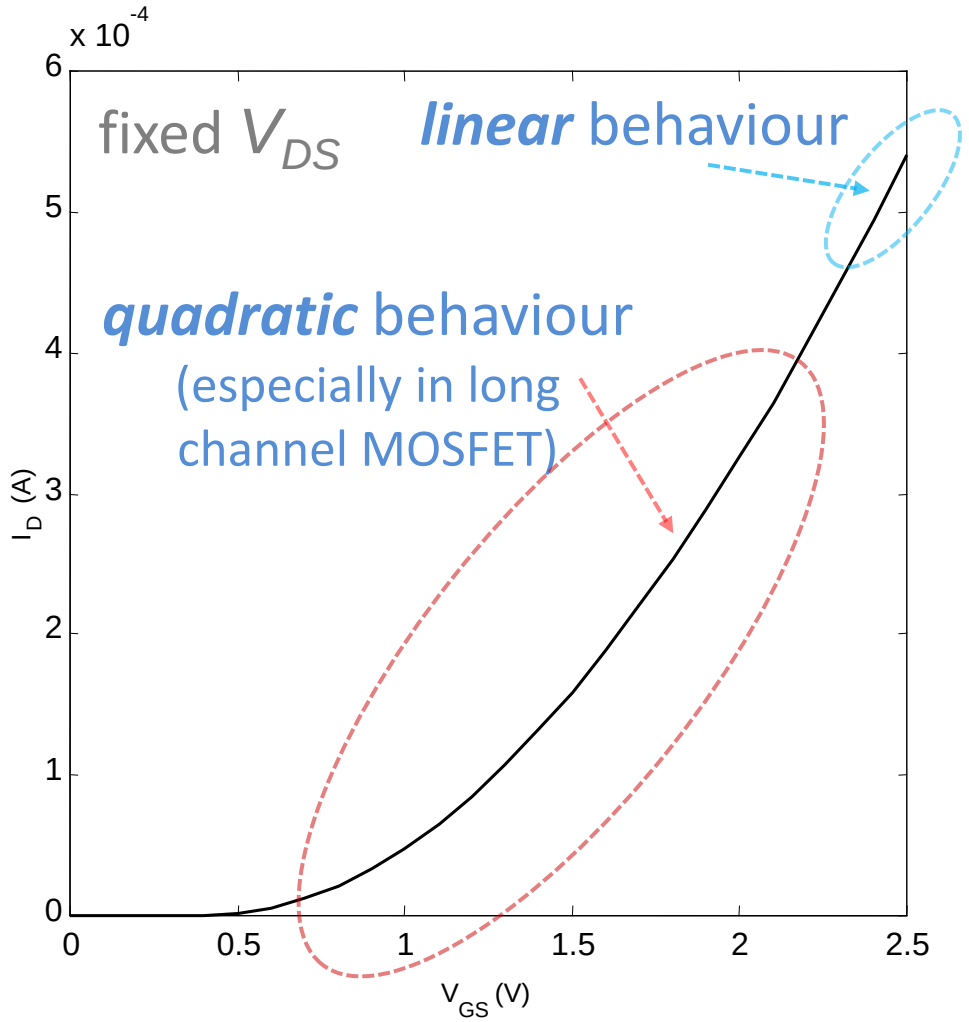
I-V Characteristics of MOSFETs

(transfer characteristics – I_{DS} vs. V_{GS})



- The device behaviour of the MOSFET (e.g. short-channel transistors) can be revealed more by the **transfer characteristics**.
  - quadratic or linear dependence of I_{DS} on V_{GS}

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From: J. M. Rabaey *et al.*, *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

I-V Characteristics of MOSFETs

(sub-threshold conduction)

- It can be more obvious in the semi-logarithmic scale.

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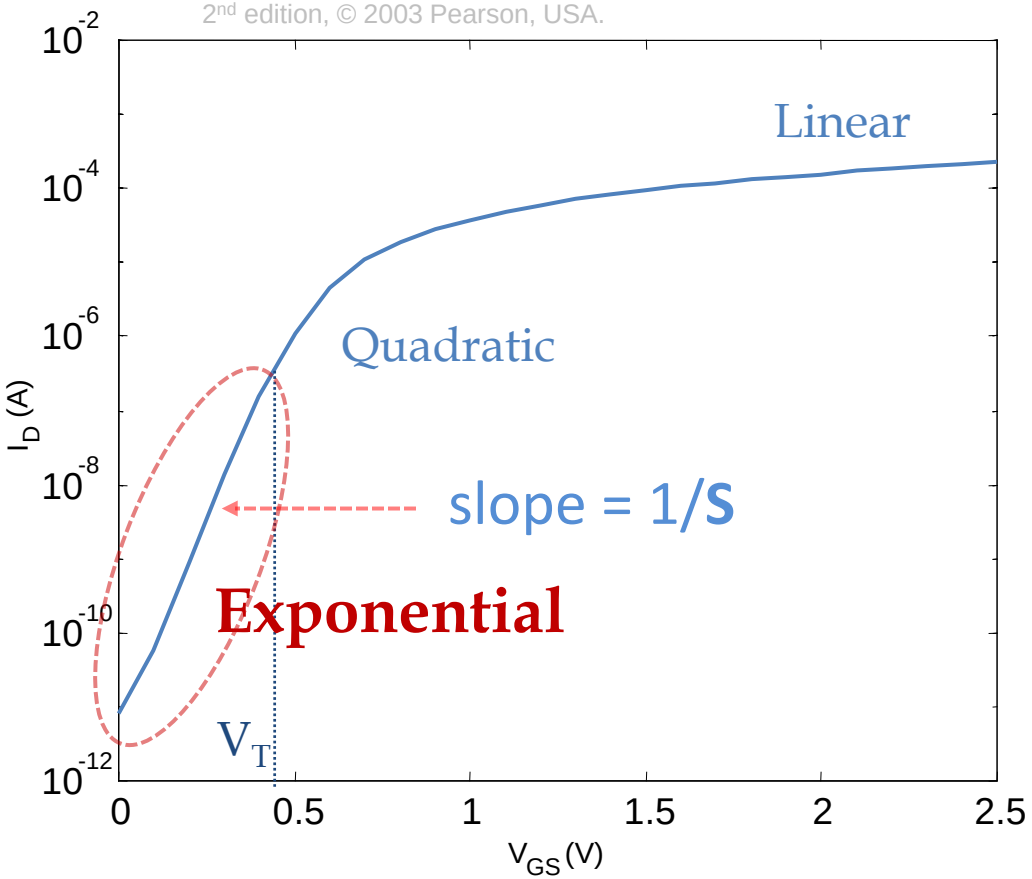

- Note the ***exponential*** dependence of I_{DS} on V_{GS} below the threshold voltage V_T.
- It is **sub-threshold conduction** of the MOSFET.

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Sub-threshold Conduction

(60 mV per decade)

- The inverse of the slope in the **exponential** dependent part of the curve in semi-log scale is called the **sub-threshold swing *S***.
  - *S* is ΔV_{GS} for I_{DS2}/I_{DS1} =10.
  - Typical values for *S* are from 60 to 100 **mV/decade**.
  - It tells how well the MOSFET can be turned off (i.e. with almost no current I_{DS} in the off state).

$$I_D \approx I_0 e^{\frac{qV_{GS}}{nkT}} \text{ when } V_{GS} < V_T, \quad n = 1 + \frac{C_D}{C_{ox}}$$

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

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MOSFET: weak & strong inversion

(leakage current implication)

- **Strong Inversion** $V_{GS} > V_T$:
  - linear region (resistive) $V_{DS} < V_{DSAT}$
  - saturated (constant current) $V_{DS} \geq V_{DSAT}$
- **Weak Inversion** (**sub-threshold**) $V_{GS} \leq V_T$
  - Exponential in V_{GS} with linear V_{DS} dependence
- The **weak inversion** has the implication of the off-state leakage current of the MOSFETs.
  - 0.1 nA for each transistor $\Rightarrow$ 1 A for a chip of 10 billion transistors! $\Rightarrow$ high power dissipation even when the circuits are supposed to be turned off.

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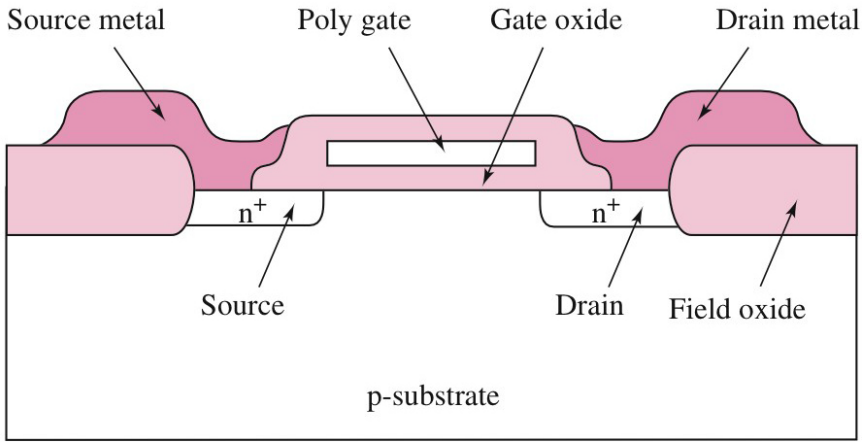
MOS Field-Effect Transistor

(actual structure)

- In integrated circuits (ICs), the actual MOSFET structure is somewhat more complex.
  - The gate material is heavily-doped polysilicon of high conductivity comparable to that of metal.
  - A thick oxide, called the **field oxide**, is deposited outside the device area to isolate from neighbouring MOSFETs.



From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

- In commercial IC fabrication, the gate length L is typically smaller than 1 μm (10^{-6} m). The gate oxide thickness is t_{ox} < 10 nm.
- See MOSIS (www.mosis.com)

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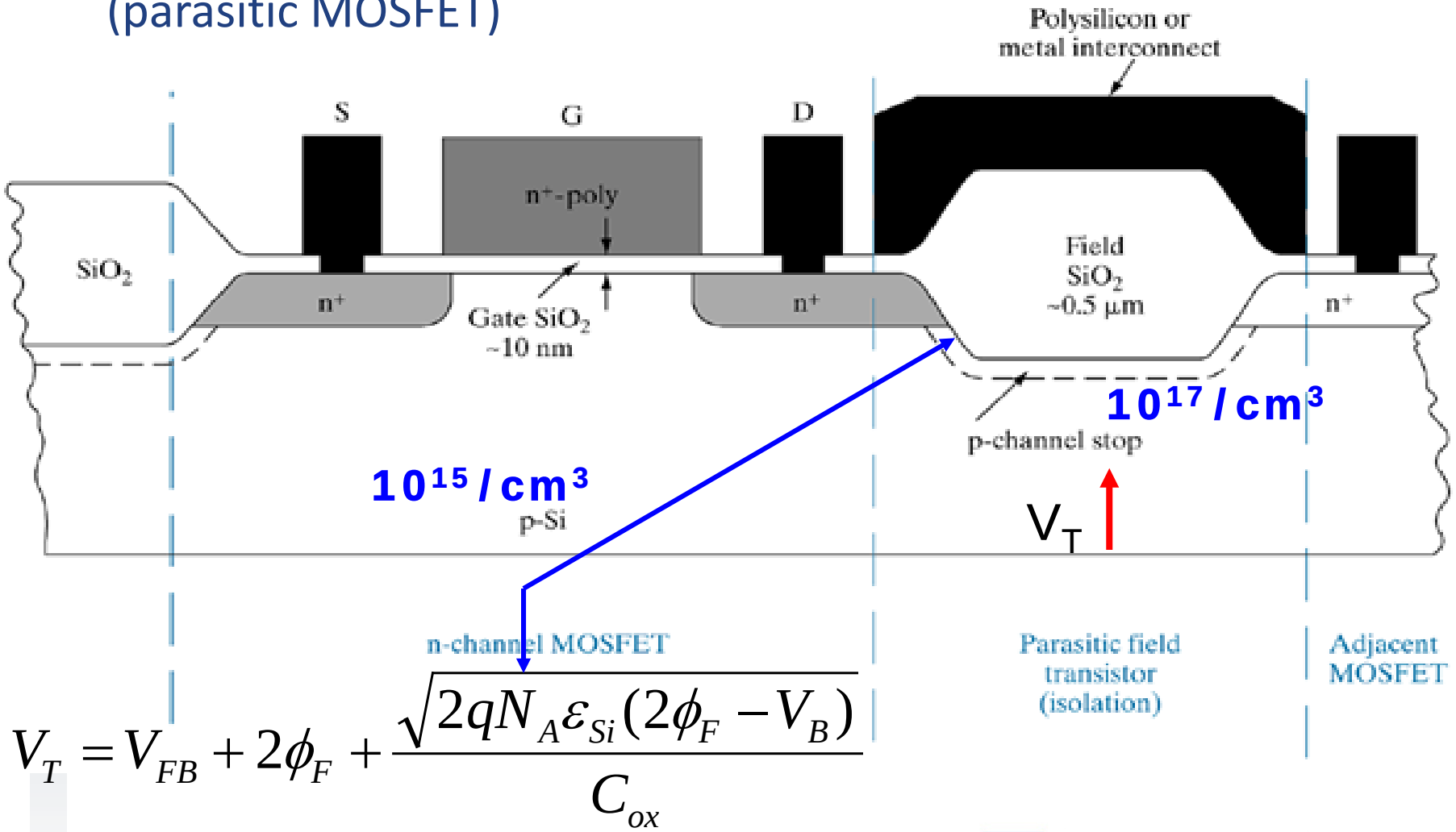
MOS Field-Effect Transistor

(parasitic MOSFET)



$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\phi_F - V_B)}}{C_{ox}}$$

p-channel stop implantation for V_T control (not to scale).

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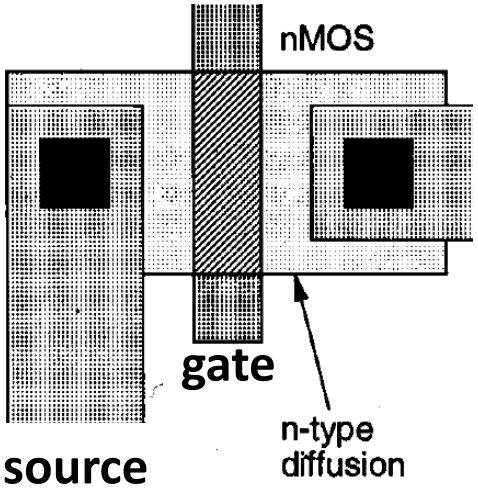
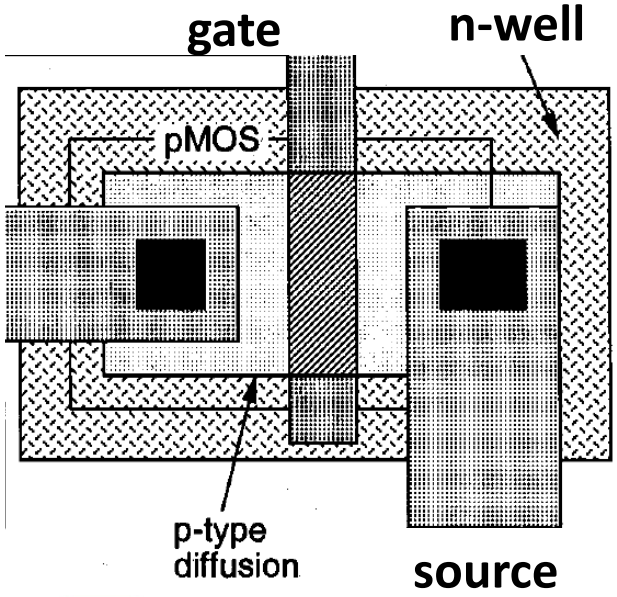
Layout of MOSFET
(nMOS & pMOS)

- Although the actual structure of the MOSFET varies for different fabrication processes, the physical layout of the nMOS and pMOS transistors remain almost the same.



From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.

Note the difference in the layout area of the nMOS & pMOS transistors



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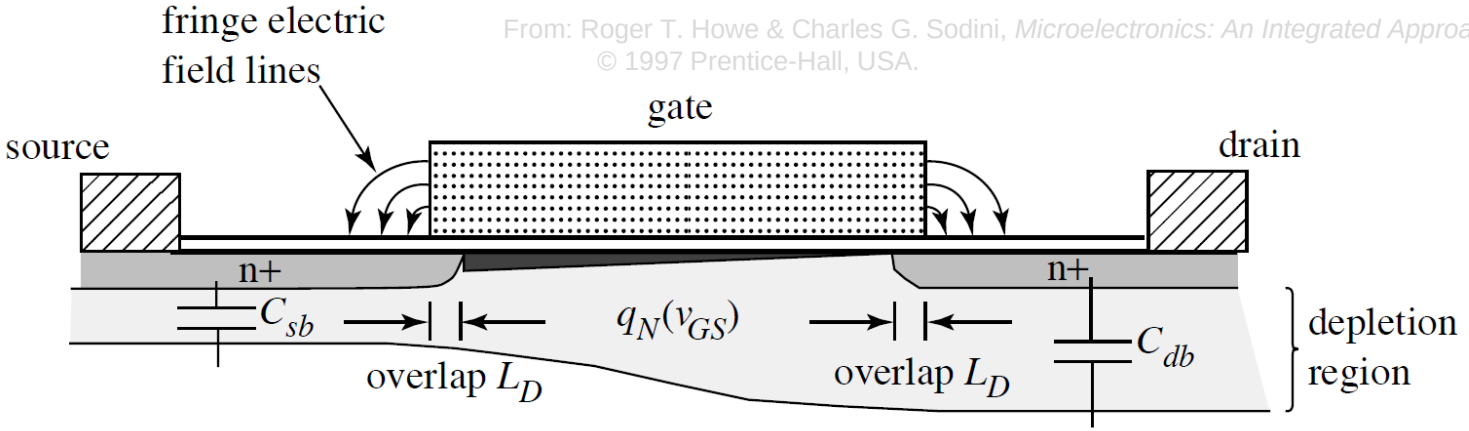
Capacitances of MOSFET

(speed of digital circuits)

- In using the MOSFETs as switches to build logic circuits, we want high switching speed for faster logic circuits.
- The speed of CMOS digital circuits is limited also by the **capacitances** associated with the MOSFET.



- associated with the gate & junctions

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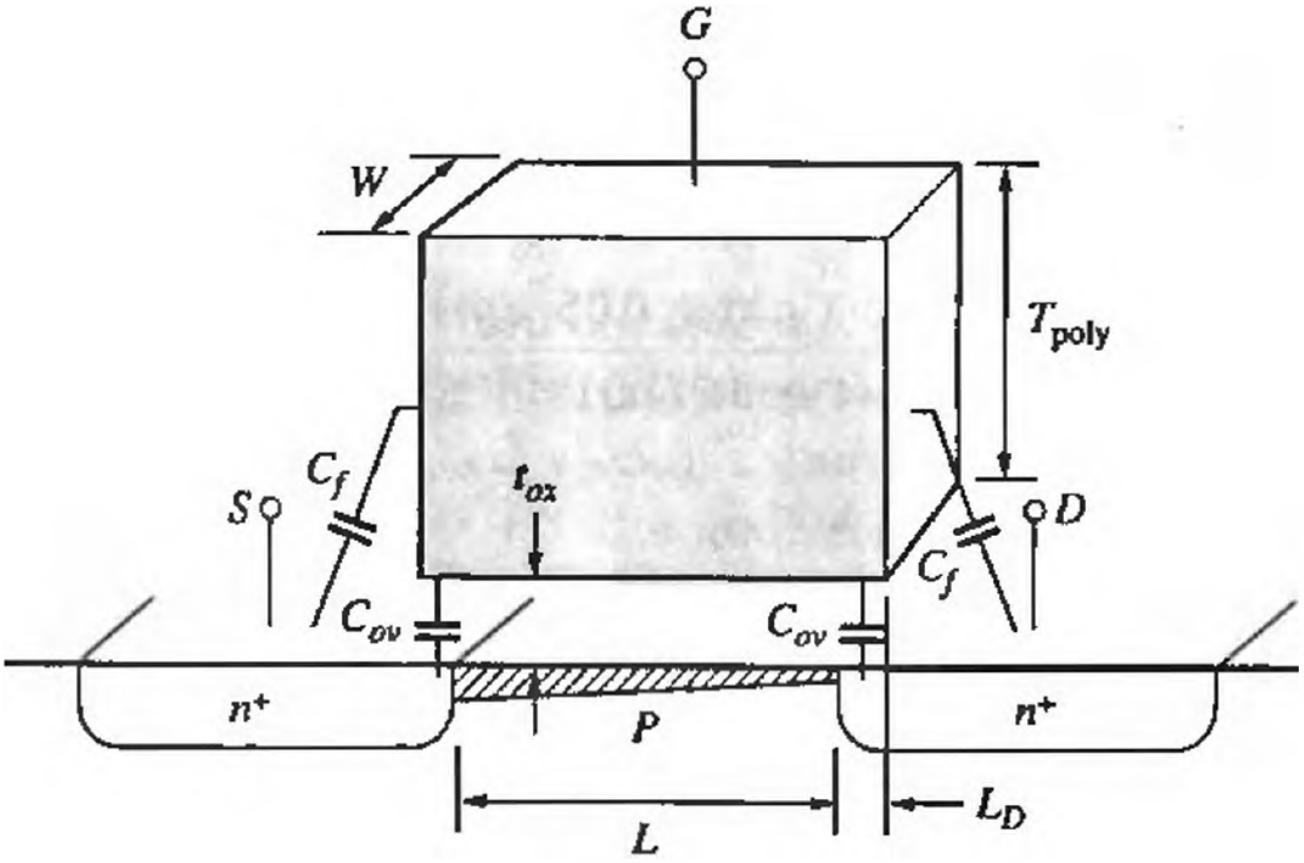
Capacitances of MOSFET

(associated with the gate)



From: D.A. Hodges *et al.*, *Analysis and Design of Digital Integrated Circuits: In Deep Submicron Technology*, 3rd edition, © 2003 McGraw Hill, USA.

- **Capacitances** associated with the gate electrode consist of the **fringing capacitance** C_f and the **overlapping capacitance** C_{ov} besides the dominant gate oxide capacitance $C_{ox} = \varepsilon_{ox}/t_{ox}$.

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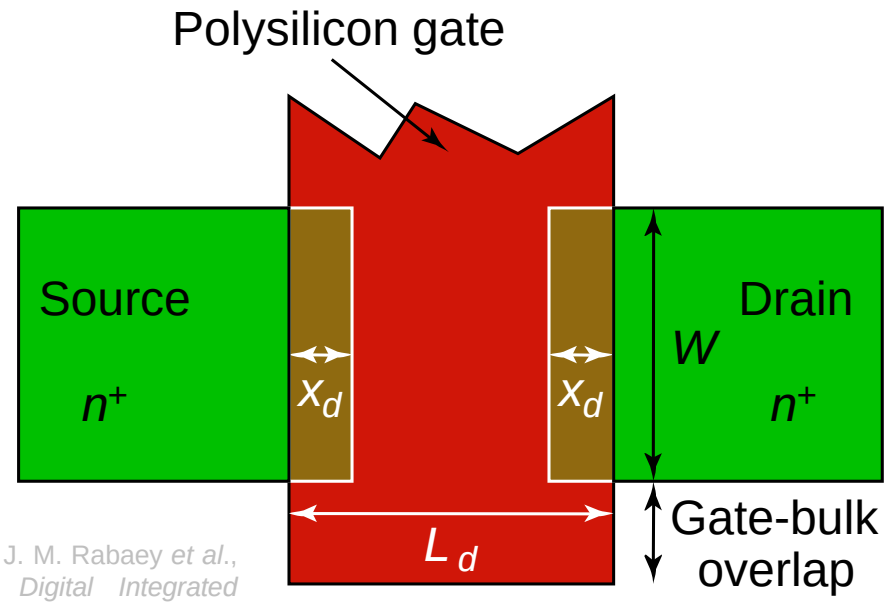
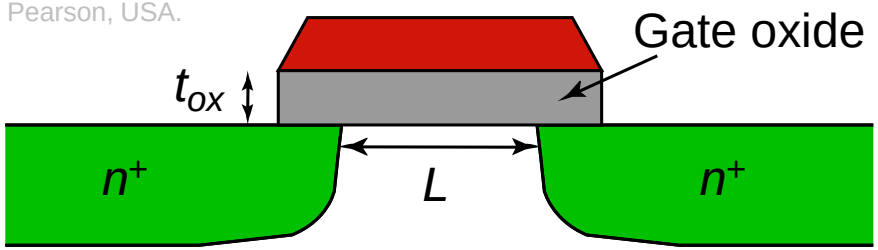
Gate Capacitance of MOSFET

(estimation using the layout)



top view



cross section

From: J. M. Rabaey *et al.*, *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

- The capacitance associated with the gate oxide can be estimated with the physical layout of the MOSFET, with the transistor sizes (***W*** & ***L***) fixed:

$$C_{gate} = \left(\frac{\varepsilon_{ox}}{t_{ox}} \right) WL$$

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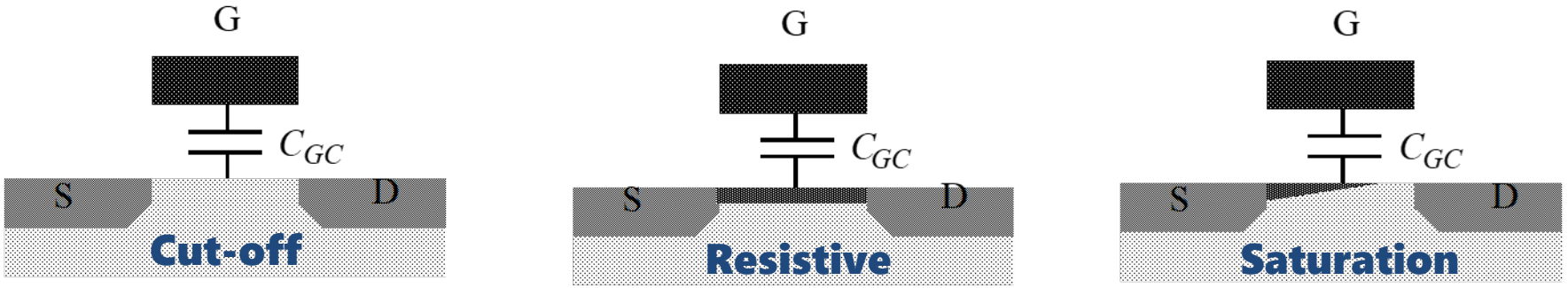
Gate Capacitances of MOSFET

(dependent on operation regions)

- The actual **gate capacitances** of the MOSFET depends on the transistor operation regions.



From: J. M. Rabaey *et al.*, *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

- C_{GC}: gate-to-channel capacitance

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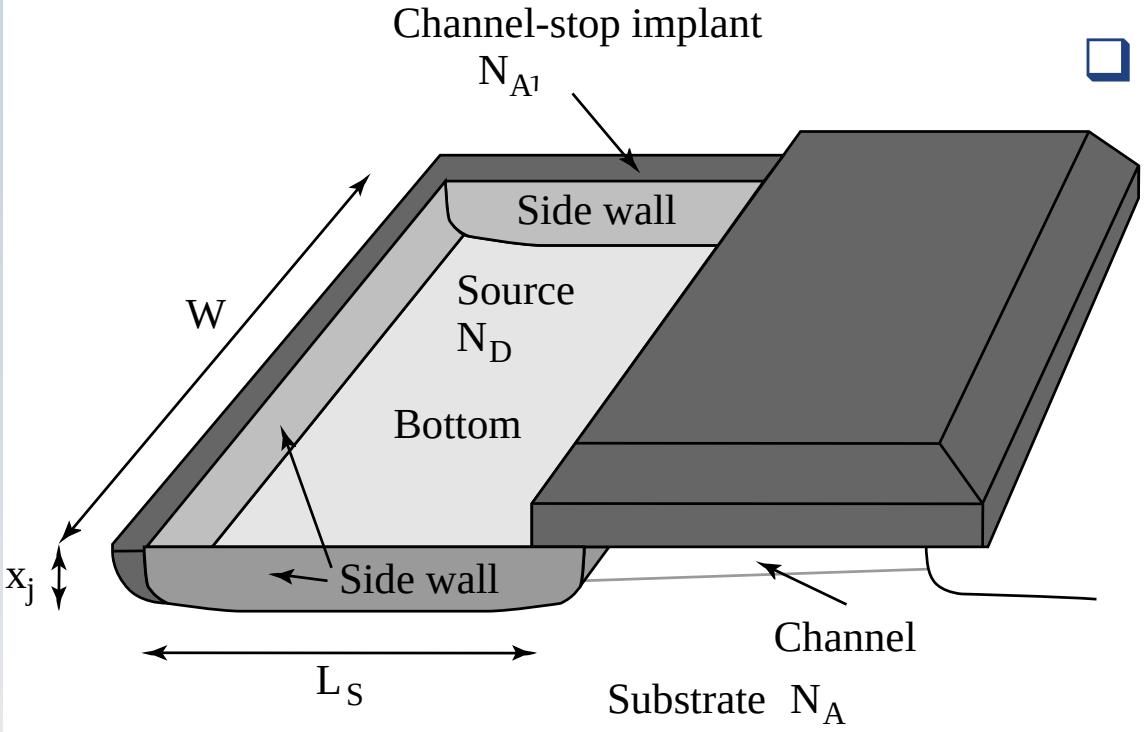
Capacitances of MOSFET

(associated with diffusion regions)



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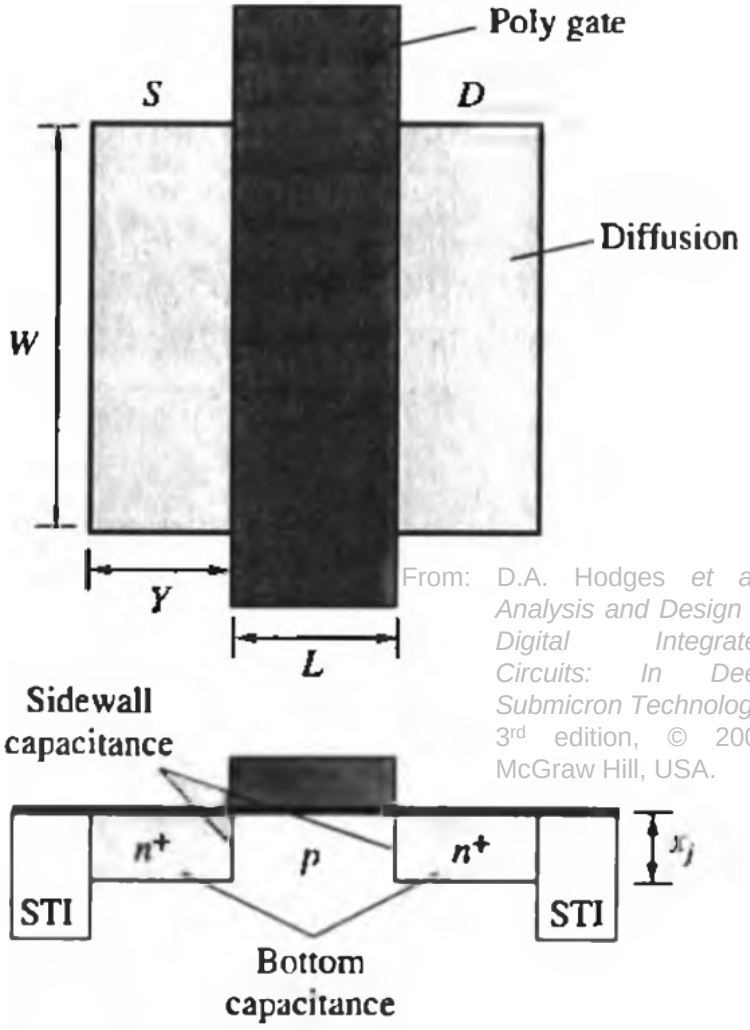
- The **source** and **drain diffusion regions** inherently contain *parasitic* ***p-n*** junctions which give rise to junction capacitances with one component dependent on area & other perimeter.

$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

Diffusion Region Capacitances

(***p-n*** junction capacitance)



From: D.A. Hodges *et al.*, *Analysis and Design of Digital Integrated Circuits: In Deep Submicron Technology*, 3rd edition, © 2003 McGraw Hill, USA.

- In the *parasitic* ***p-n*** junctions of the **source** and **drain diffusion regions**, the junction boundary is a curved surface.
- To estimate the diffusion region capacitance from the physical layout, the ***sidewall*** part is estimated by the perimeter.

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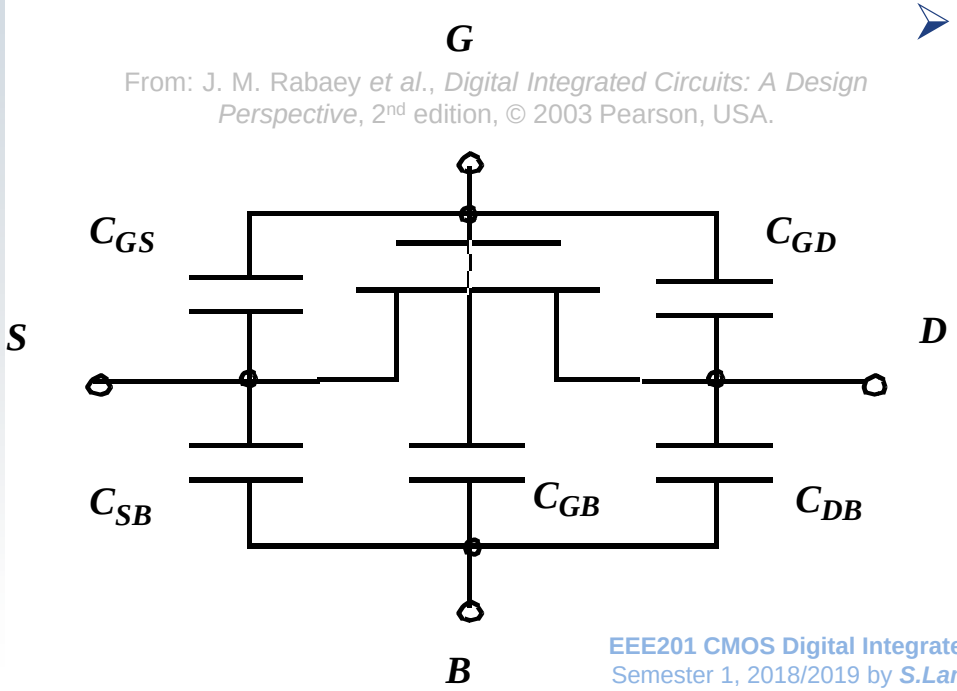
Capacitances of MOSFET

(model for better speed estimation)

- In CMOS digital ICs, it is desirable to keep the capacitances minimum in the IC layout design.
- Even when the capacitances may not be minimised, they need to be modelled properly.



From: J. M. Rabaey *et al.*, *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

- With the capacitances included properly in the MOSFET model, the **circuit speed** of the digital ICs can be more accurately estimated even before chips are made.

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