EEE201

Xi'an Jiaotong-Liverpool University

西交利物浦大學

nMOS & CMOS Logic Families

(materials developed by Prof. C. Z. Zhao)

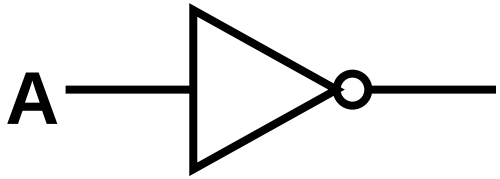
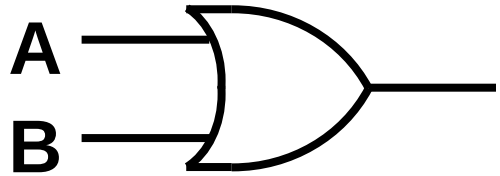
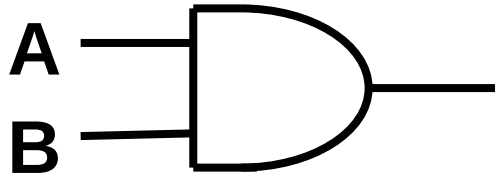
Special Thanks To:

Prof. V. D. Agrawal & Prof. J. J. Danaher, Auburn University
Prof. Mary Jane Irwin, Pennsylvania State University
Prof. Steve Hall, UoL

outline

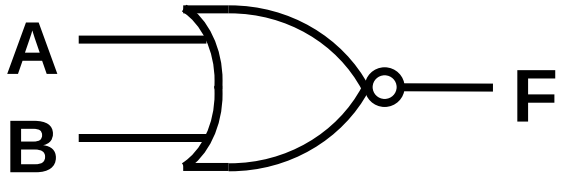
- Devices and Gates and Logic Symbols
  - Logic symbols and functions
  - MOSFETs in series/parallel connection
- CMOS Logic Family
- nMOS Logic Family
- Circuit Extraction from Layouts

Logic Functions, Symbols, & Notation

NAME	SYMBOL	NOTATION	TRUTH TABLE
"NOT"		$F = \overline{A}$	A F 0 1 1 0
"OR"		F = A+B	A B F 0 0 0 0 1 1 1 0 1 1 1 1
"AND"		F = A•B	A B F 0 0 0 0 1 0 1 0 0 1 1 1

Logic Functions, Symbols, & Notation

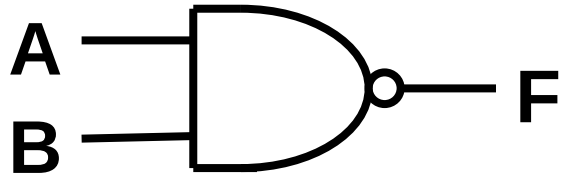
“NOR”



$F = \overline{A+B}$

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

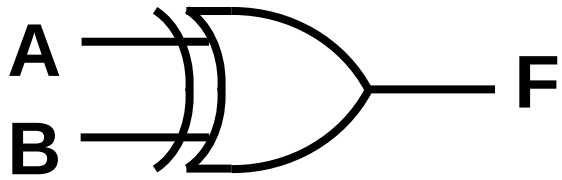
“NAND”



$F = \overline{A \cdot B}$

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

“XOR”
(exclusive OR)

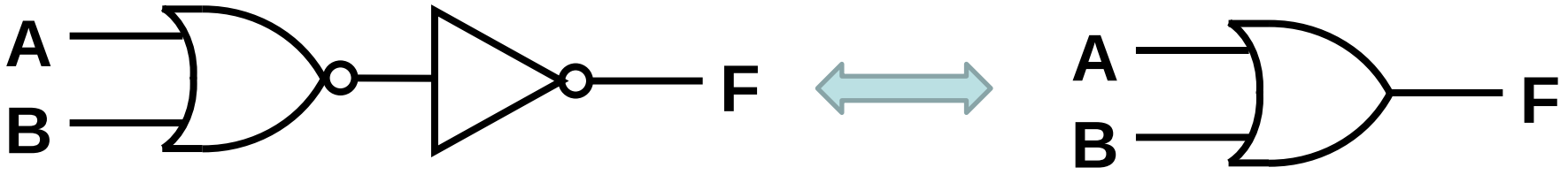


$F = A \oplus B$

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Logic Functions, Symbols, & Notation

“NOR” + Inverter = “OR”



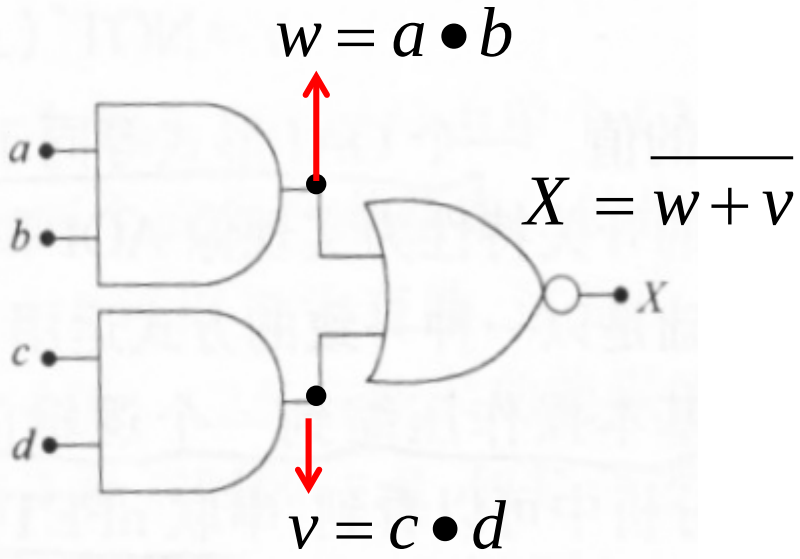
“AND” + Inverter = “NAND”

Logic Functions, Symbols, & Notation

AOI

AND-OR-inverter such as

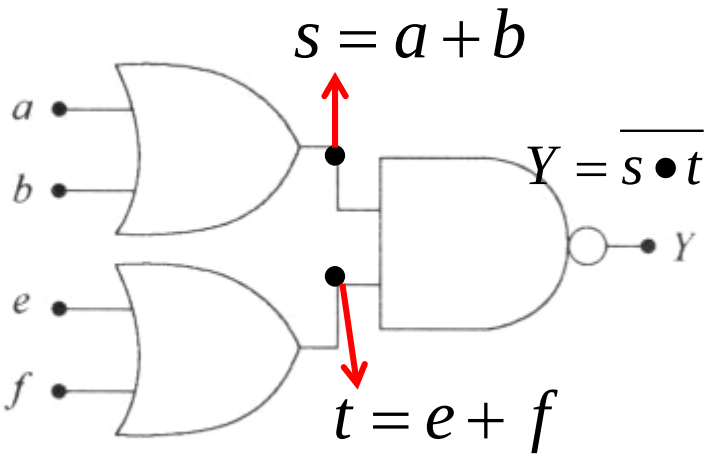
$$X = \overline{(a \bullet b) + (c \bullet d)}$$



OAI

OR-AND-inverter such as

$$Y = \overline{(a + b) \bullet (e + f)}$$

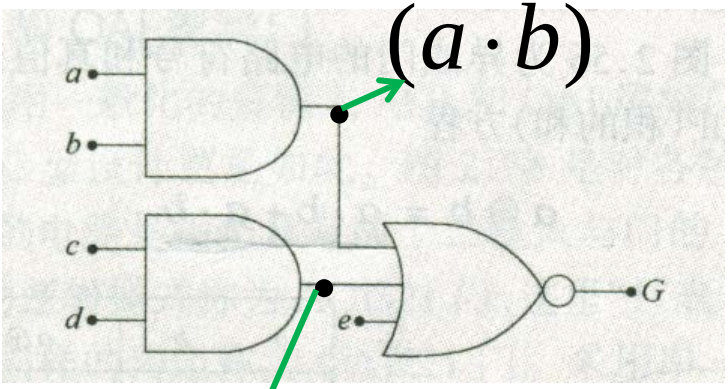


Logic Functions, Symbols, & Notation

AOI

AND-OR-inverter, such as

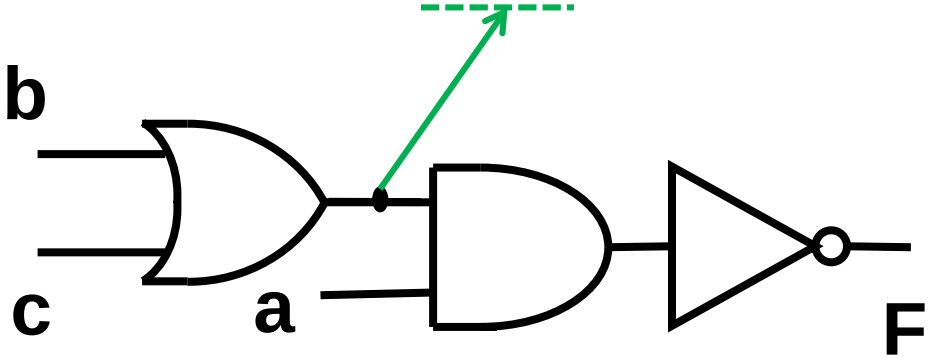
$$G = \overline{(a \cdot b) + (c \cdot d) + e}$$

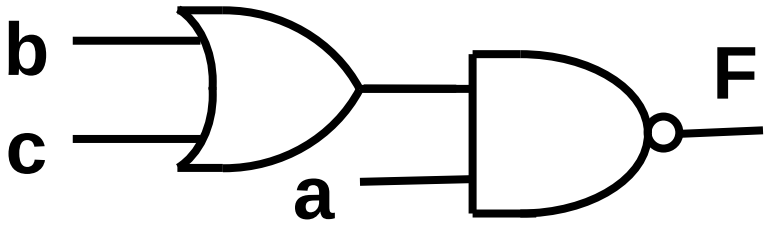


OAI

OR-AND-inverter, such as

$$F = \overline{a \cdot (b + c)}$$

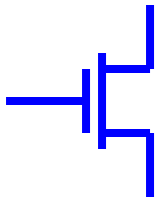




A MOSFET layout & symbols

$(W/L)_p$

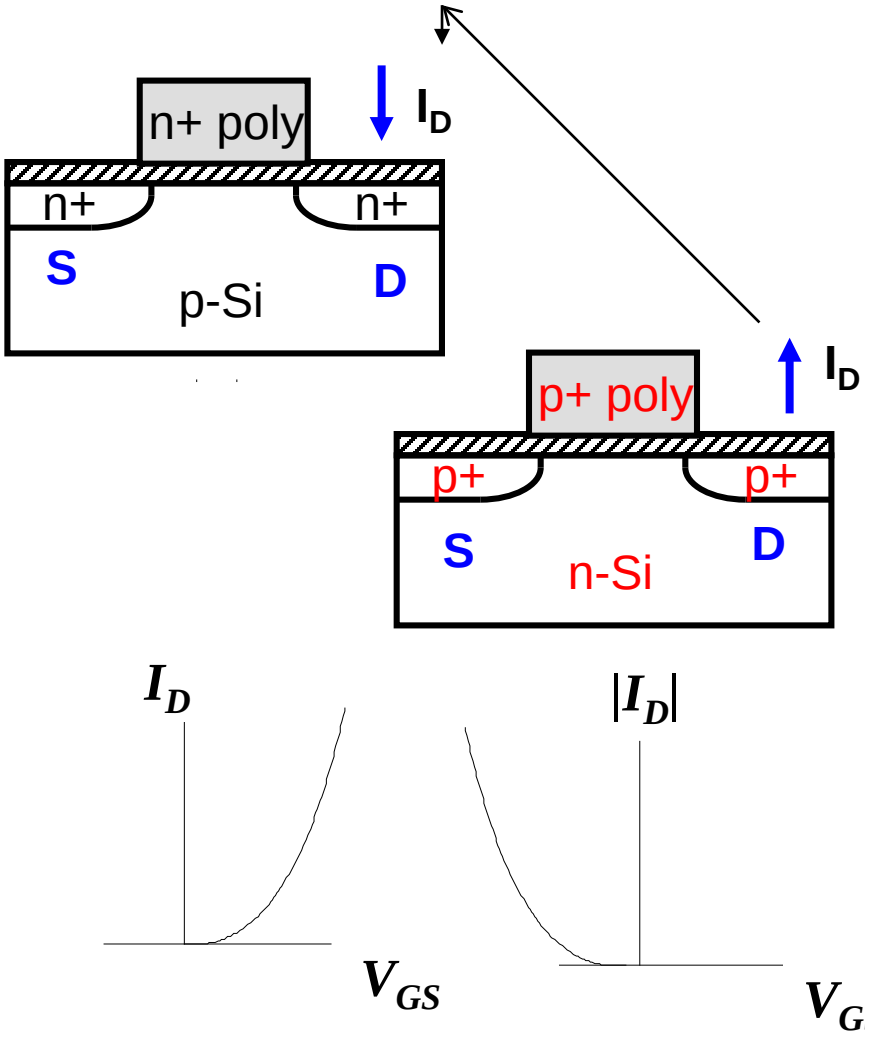
1.96/0.18



$(W/L)_n$

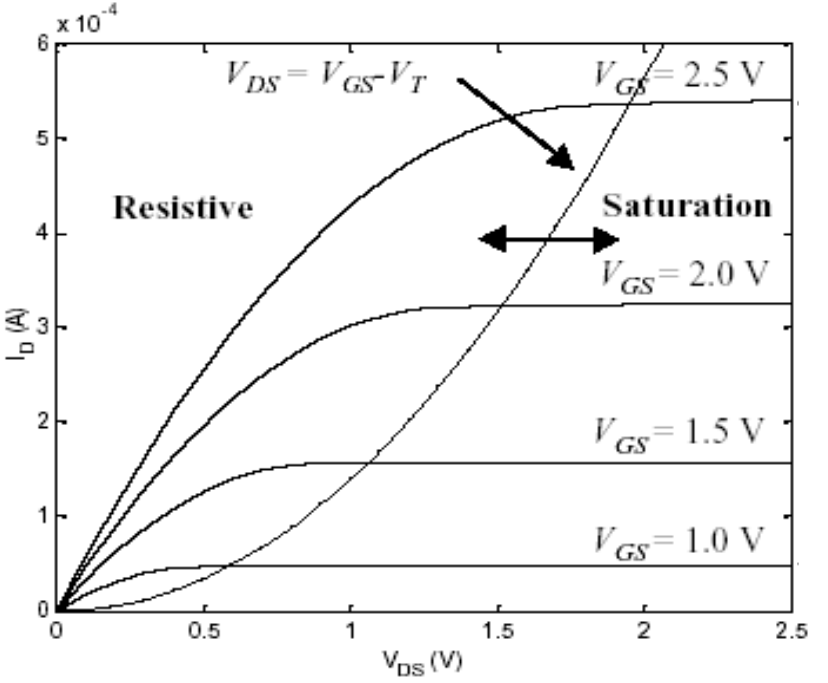
0.48/0.18

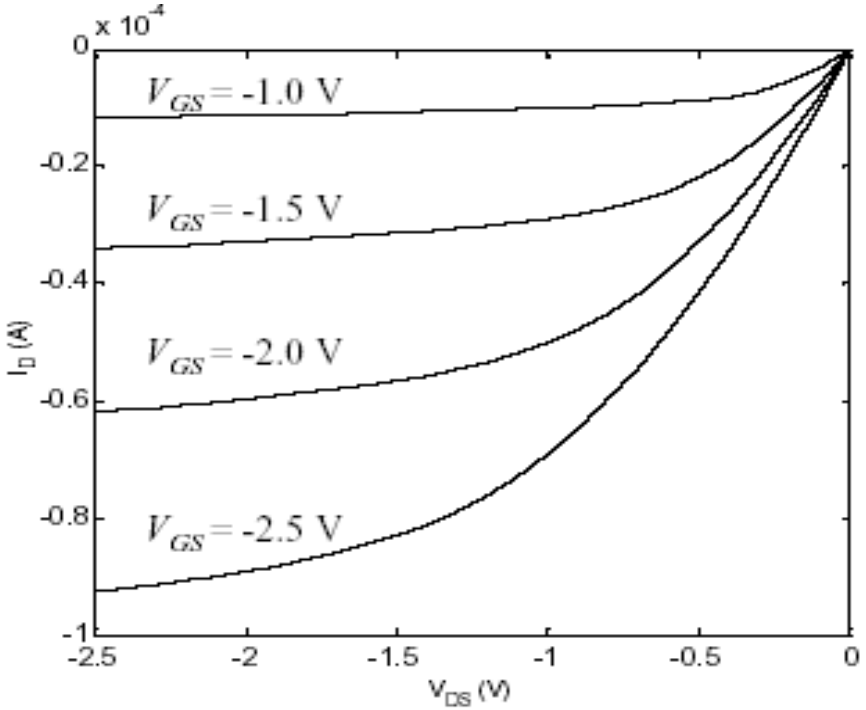
MOSFETs



n channel enhancement

p channel enhancement

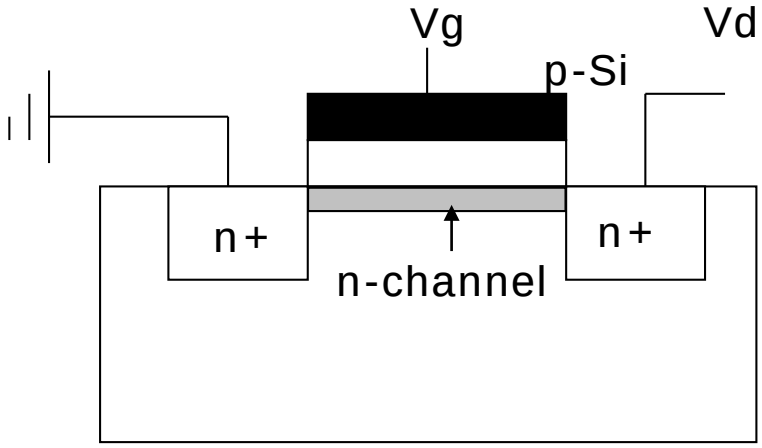


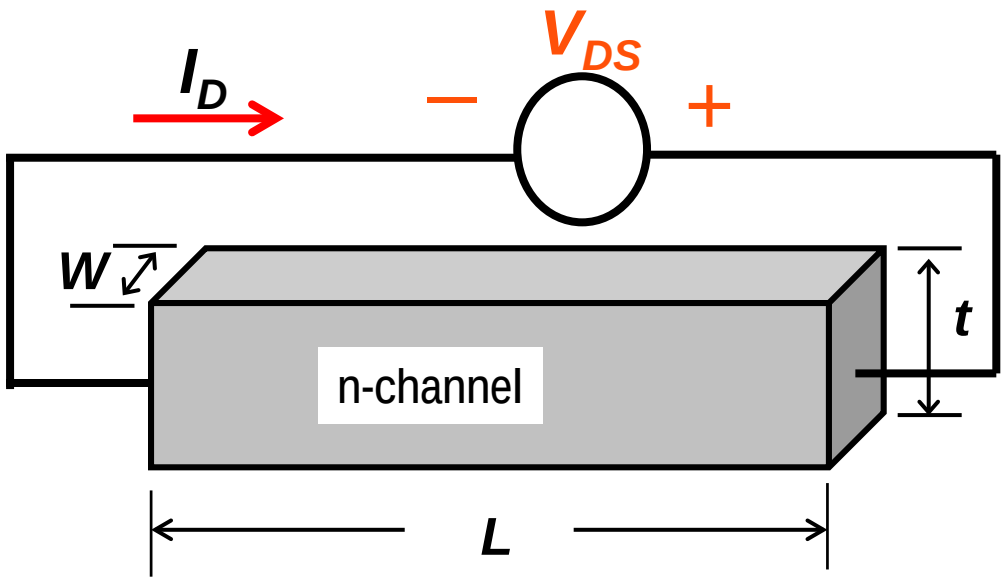


Recall

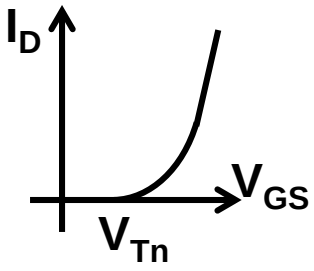
An n-channel as a resistor

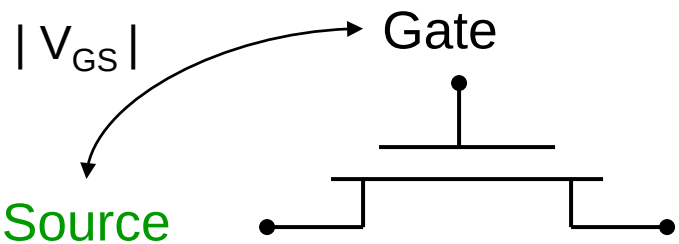
- Without gate bias, MOSFET is off because two diodes are "back-to-back". One of them will be reversely biased. To switch on, the interfacial region is inverted by applying a gate bias.
- Above a certain gate-to-source voltage (***threshold voltage V_T***), a conducting layer of mobile electrons is formed at the Si surface beneath the oxide. These electrons can carry current between the source and drain.





Switch Model of NMOS Transistor

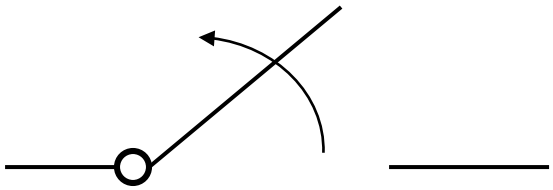




Source
(of carriers)

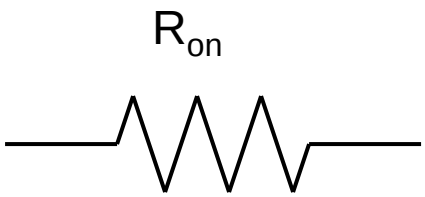
Drain
(of carriers)

Open (off) (Gate = ‘0’)



$V_{GS} < V_{Tn}$

Closed (on) (Gate = ‘1’)



$V_{GS} > V_{Tn}$

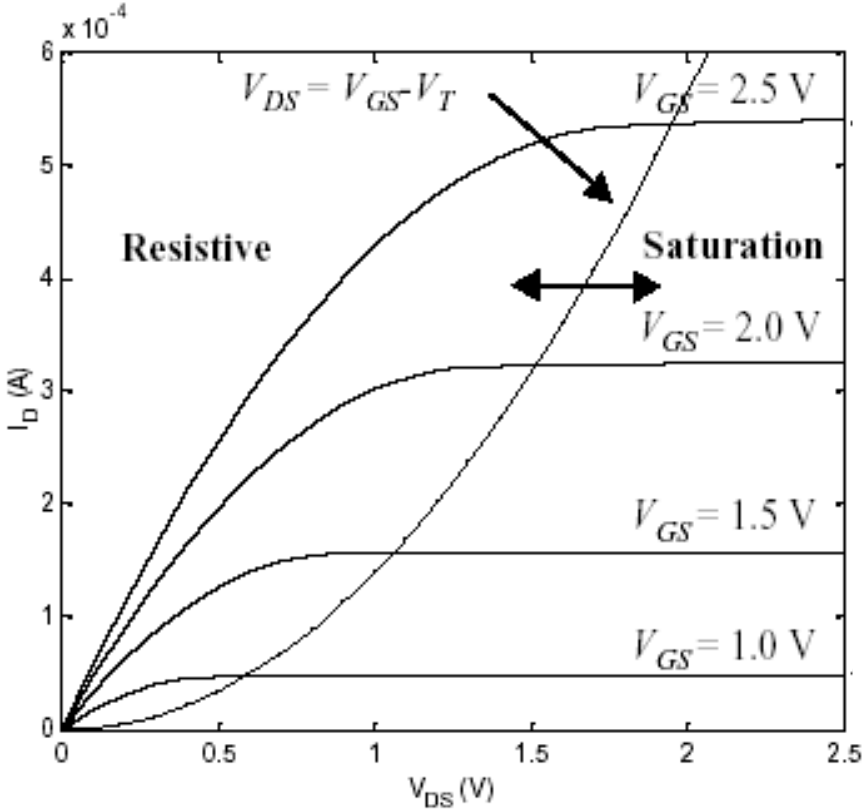
nMOS Transistor Equations

$$I_{D,lin} = \frac{\mu_n C_{Ox}}{2}\frac{W}{L}\left(2\left(V_{GS} - V_{Tn}\right)V_{DS} - V_{DS}^2\right) \qquad (1)$$

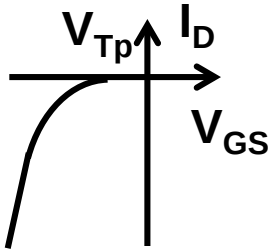
$$\text{for } V_{GS} \geq V_{Tn} \text{ and } V_{DS} < V_{DS,sat} (= V_{GS} - V_{Tn})$$

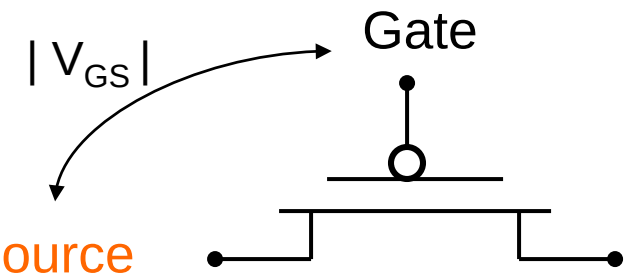
$$I_{D,sat} = \frac{\mu_n C_{Ox}}{2}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)^2 \qquad (2)$$

$$\text{for } V_{GS} \geq V_{Tn} \text{ and } V_{DS} \geq V_{DS,sat}$$



Switch Model of PMOS Transistor

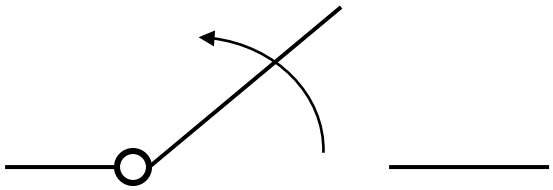




Source (of carriers)

Drain (of carriers)

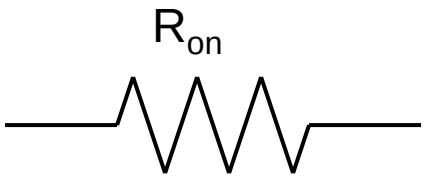
Open (off) (Gate = ‘1’)



$V_{GS} > V_{Tp}$

$|V_{GS}| < |V_{Tp}|$

Closed (on) (Gate = ‘0’)



$V_{GS} < V_{Tp}$

$|V_{GS}| > |V_{Tp}|$

pMOS Transistor Equations

$$I_{D,lin} = \frac{\mu_p C_{Ox}}{2}\frac{W}{L}\left(2\left(V_{GS} - V_{Tp}\right)V_{DS} - V_{DS}^2\right) \qquad (1)$$

for $V_{GS} \le V_{Tp}$ and $V_{DS} > V_{DS,sat} (= V_{GS} - V_{Tp})$

or for $|V_{GS}| \ge |V_{Tp}|$ and $|V_{DS}| < |V_{DS,sat}| (= |V_{GS} - V_{Tp}|)$

$$I_{D,sat} = \frac{\mu_p C_{Ox}}{2}\frac{W}{L}\left(V_{GS} - V_{Tp}\right)^2 \qquad (2)$$

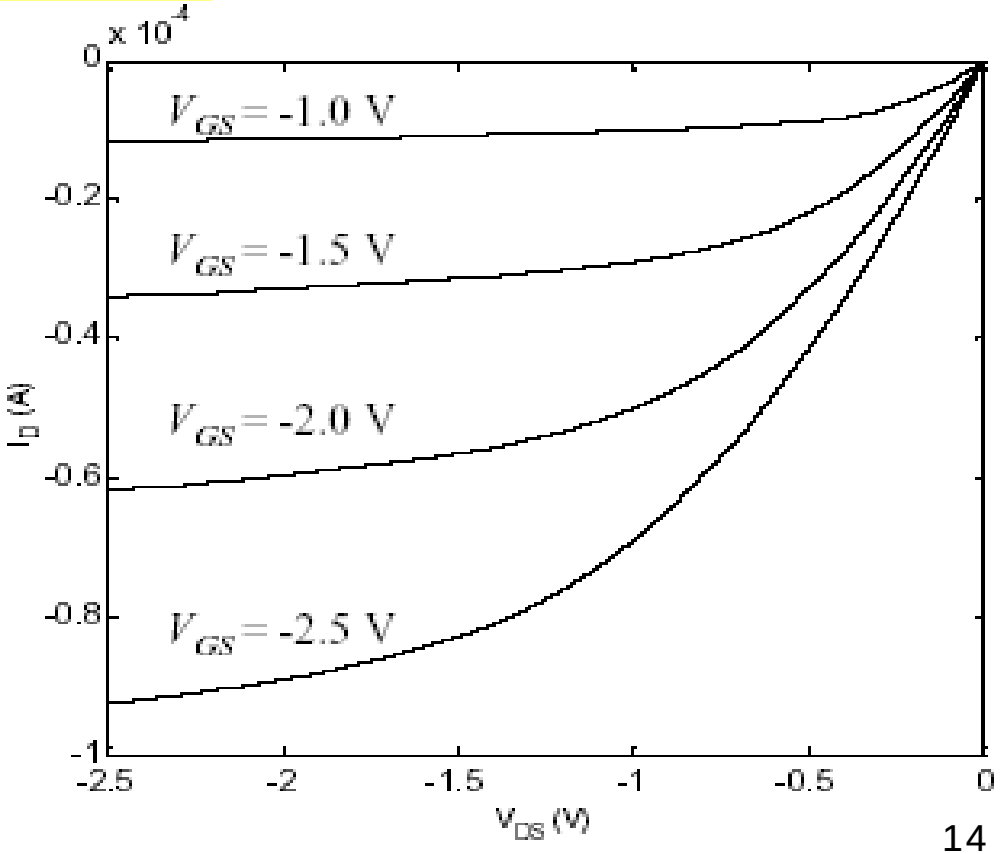
for $V_{GS} \le V_{Tp}$ and $V_{DS} \le V_{DS,sat}$

or for $|V_{GS}| \ge |V_{Tp}|$ and $|V_{DS}| \ge |V_{DS,sat}|$

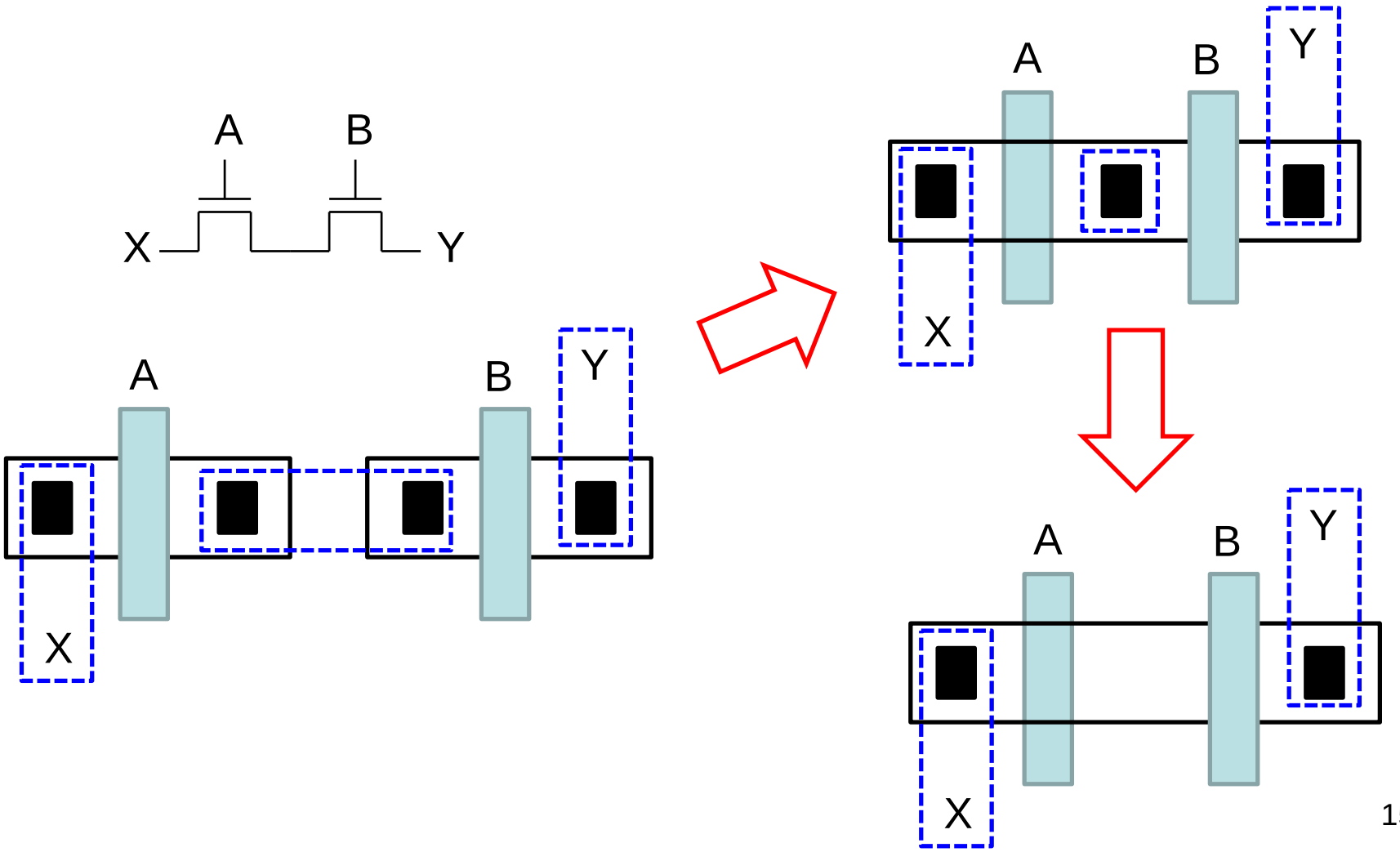
n ⟶ p

< ⟶ >

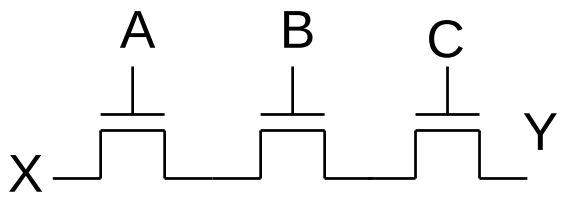
> ⟶ <

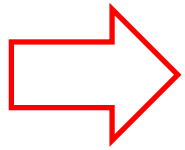


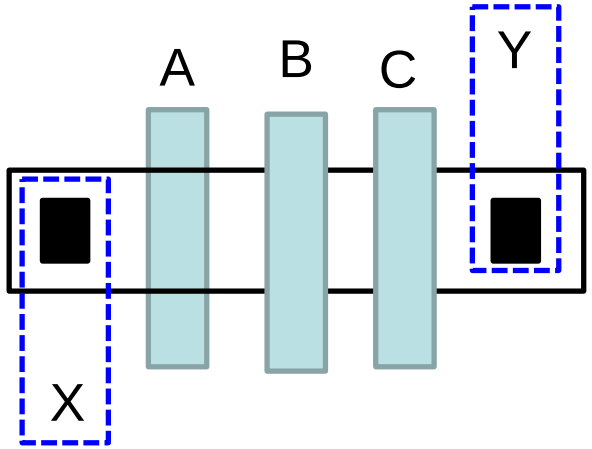
NMOS Transistors in Series/Parallel Connection

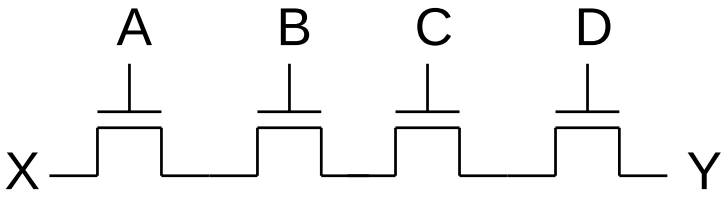


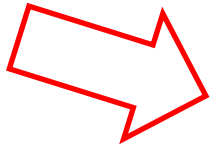
NMOS Transistors in Series/Parallel Connection

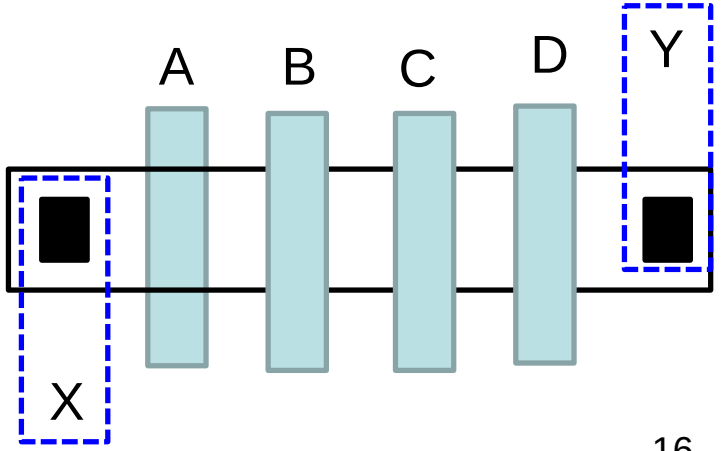




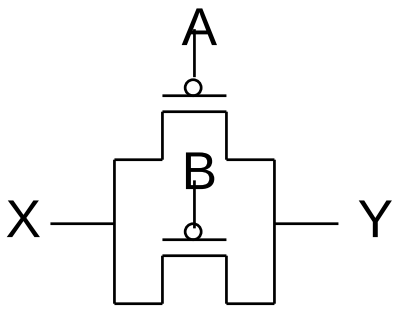


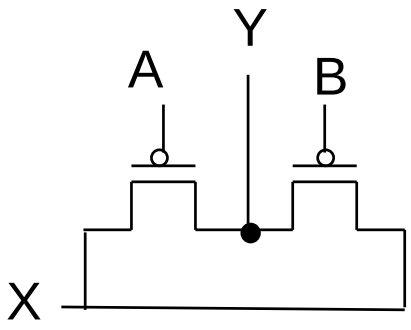


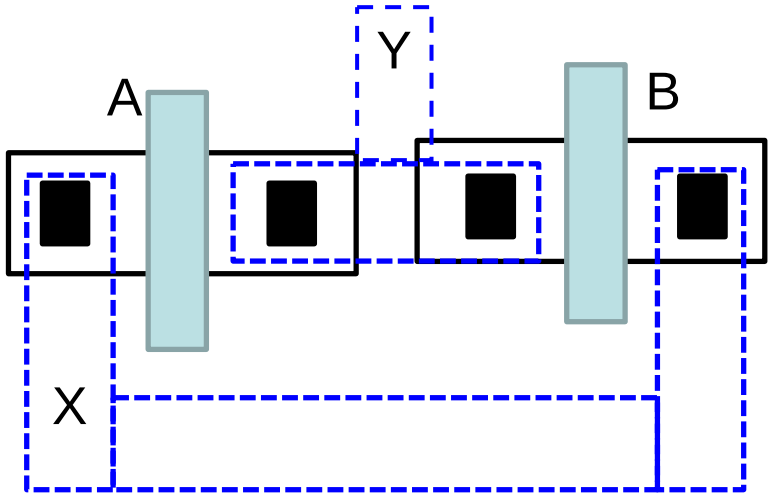


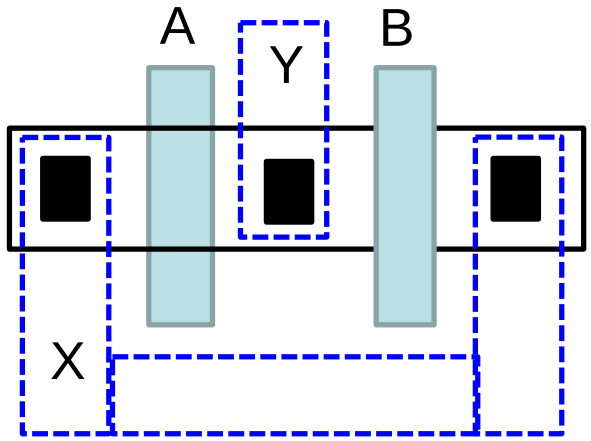


PMOS Transistors in Series/Parallel Connection

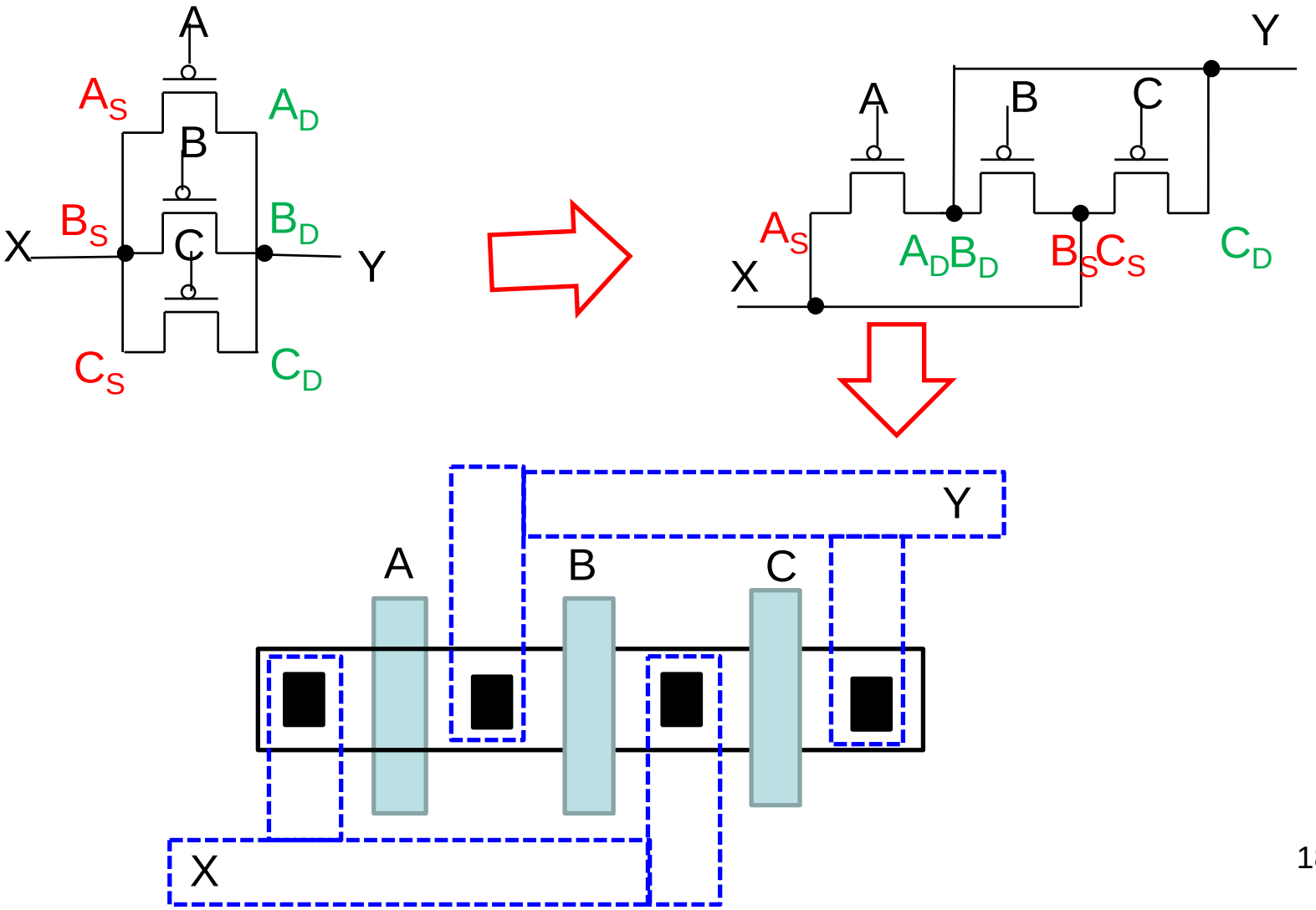




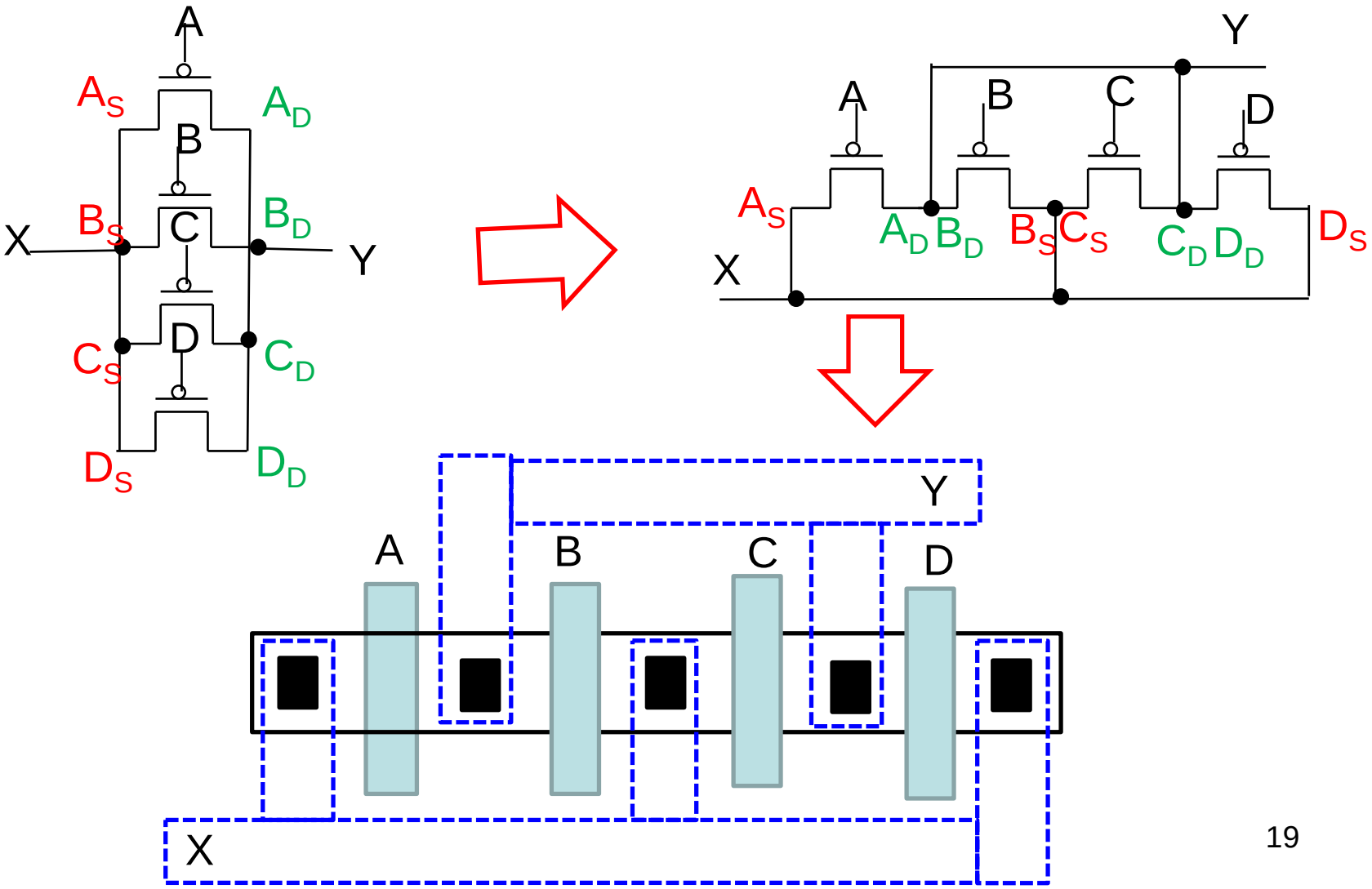




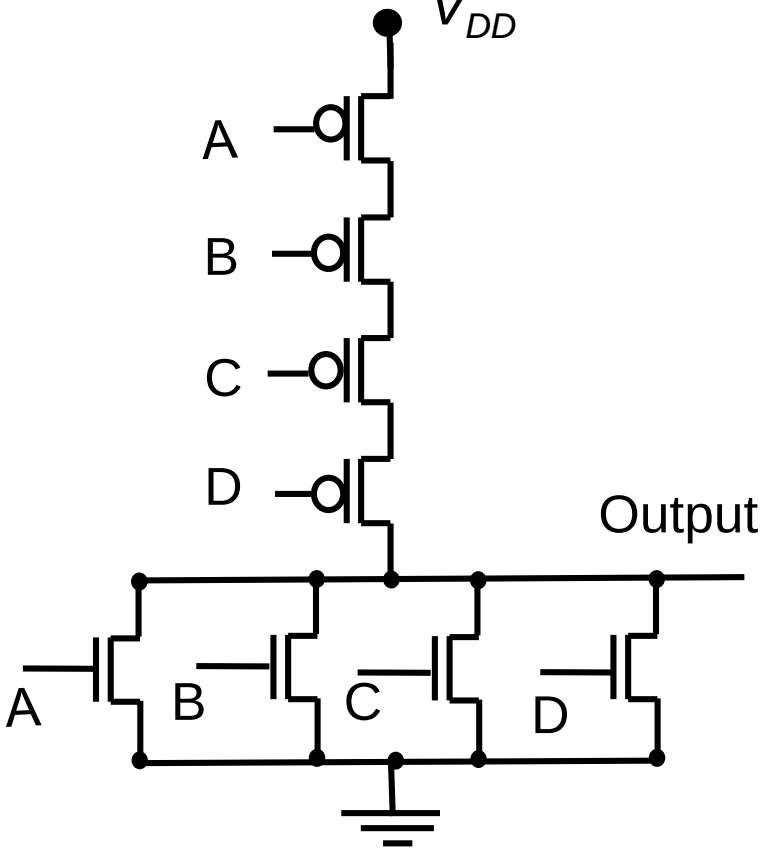
PMOS Transistors in Series/Parallel Connection

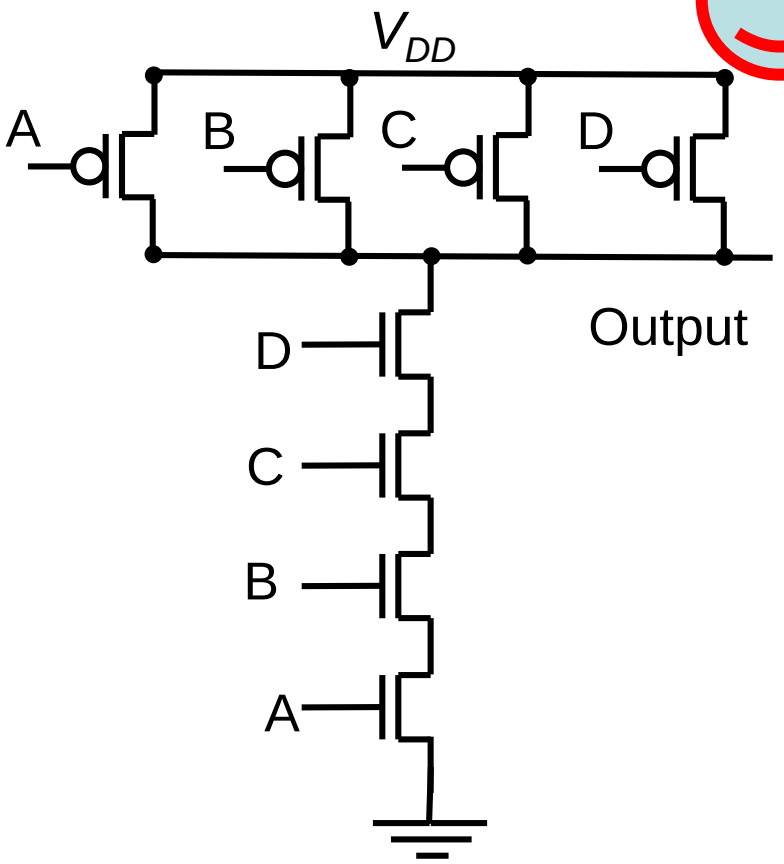


PMOS Transistors in Series/Parallel Connection

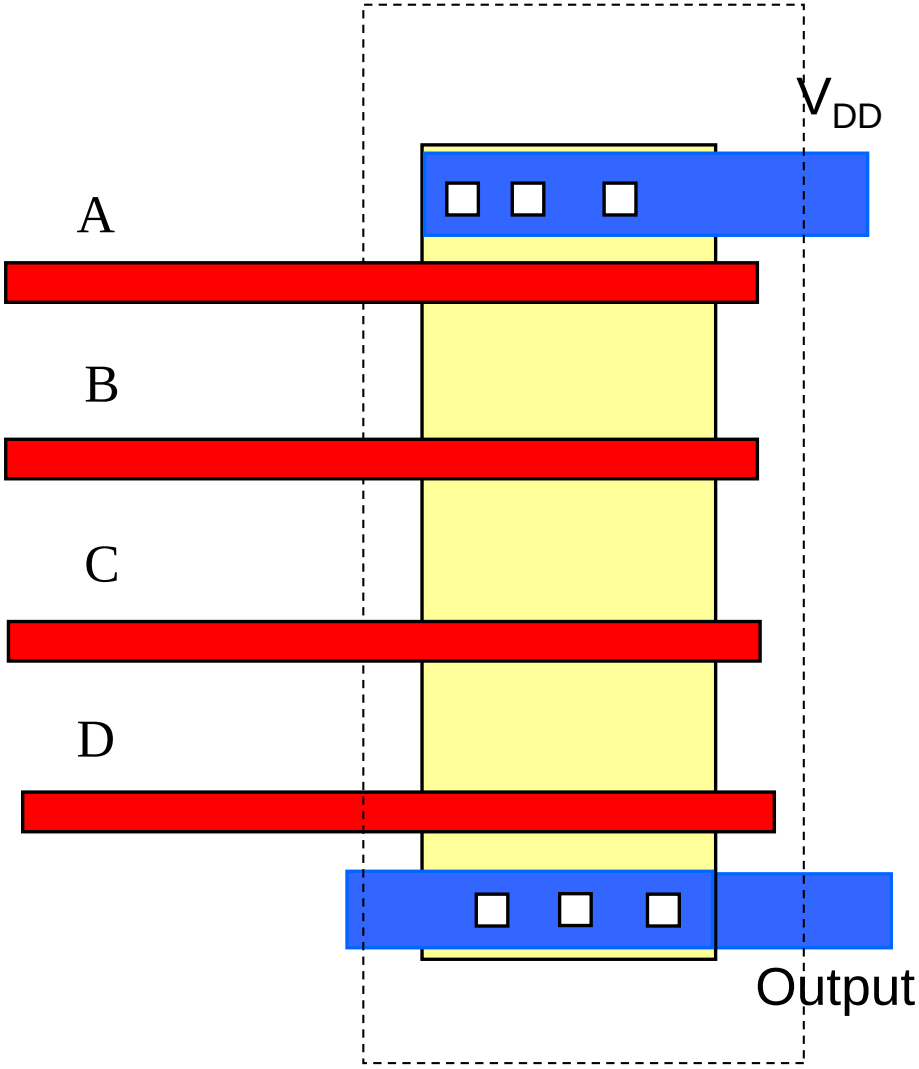


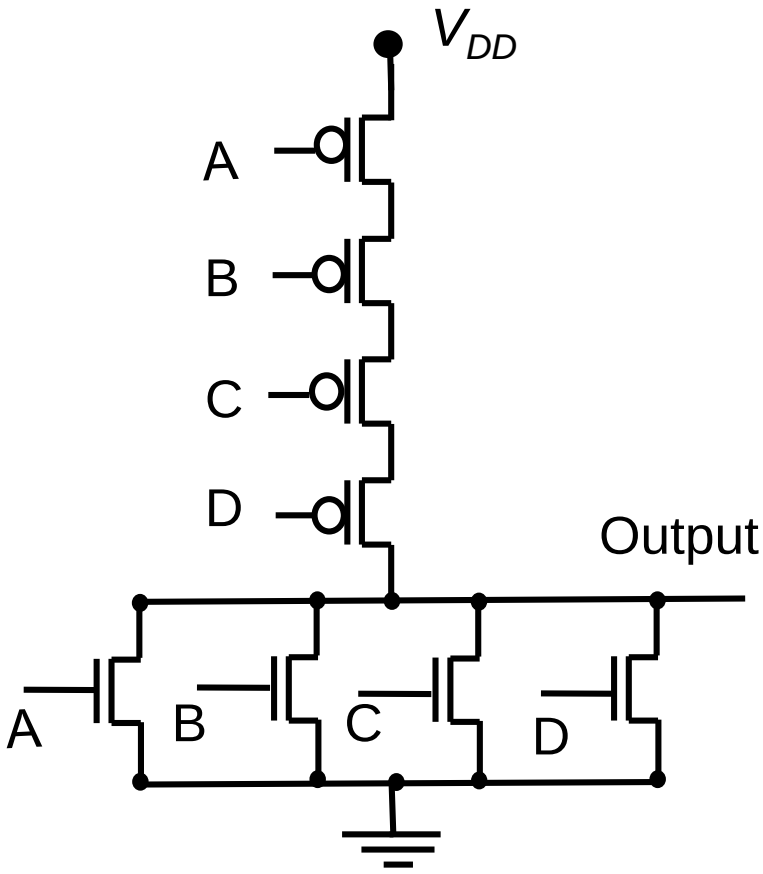
Complex connection



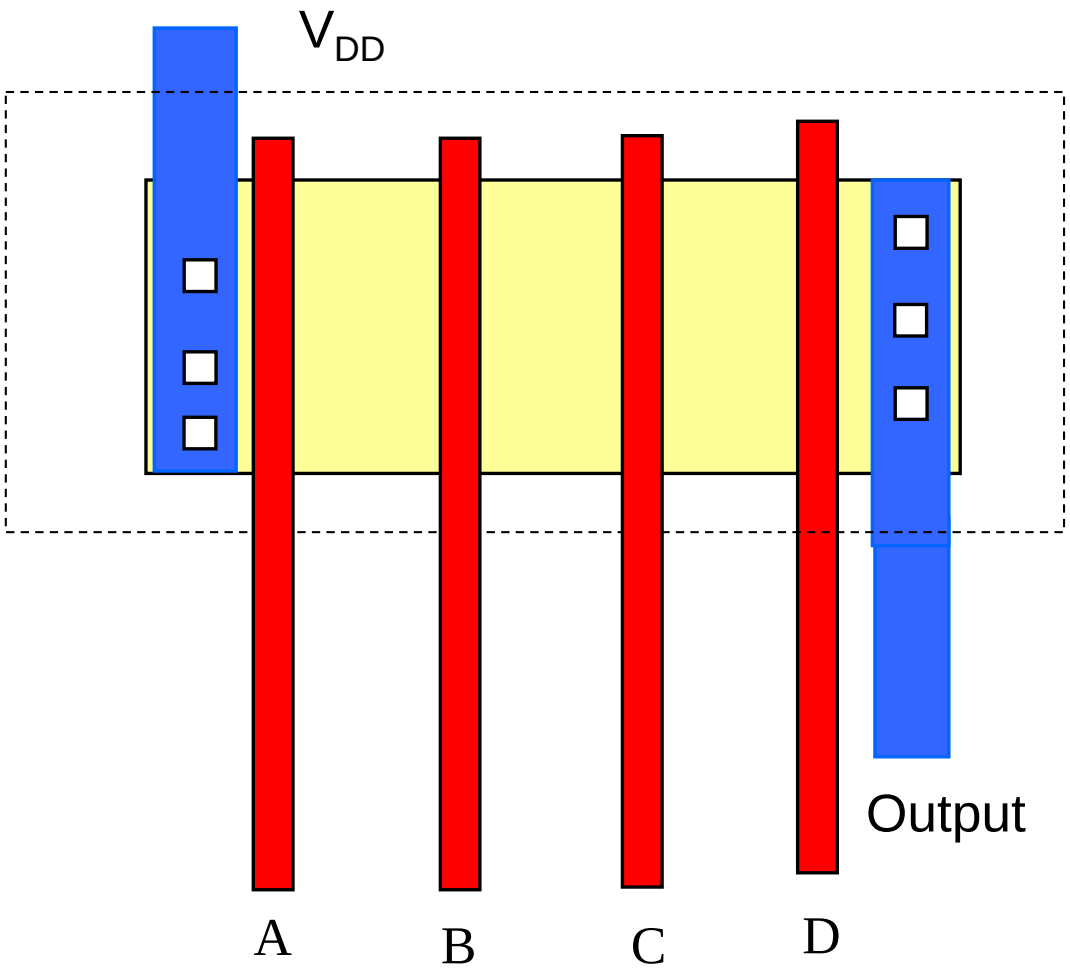


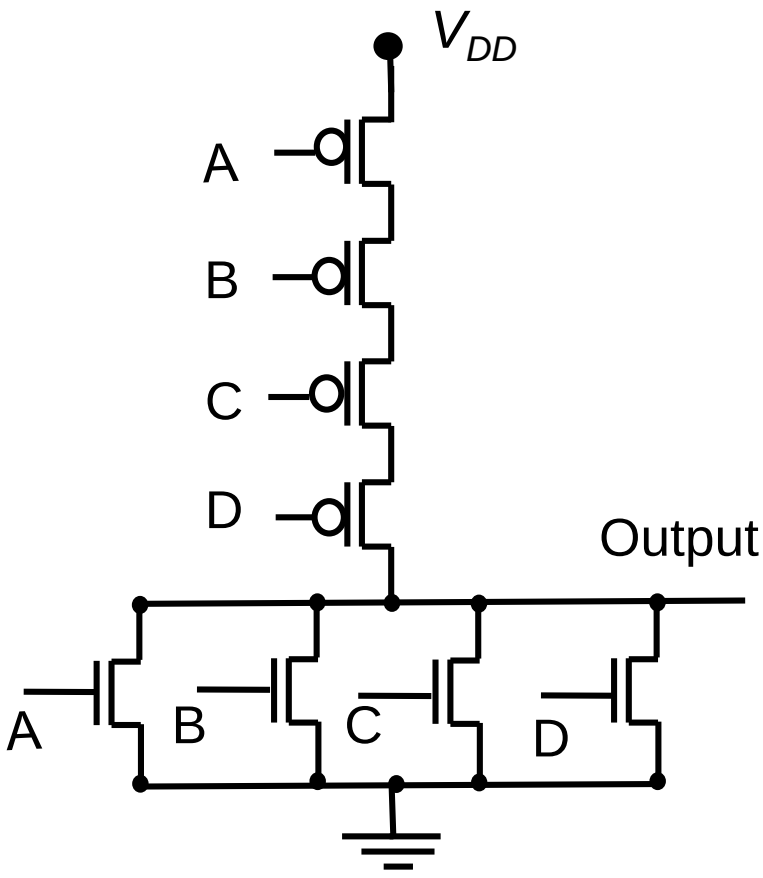
Complex connection



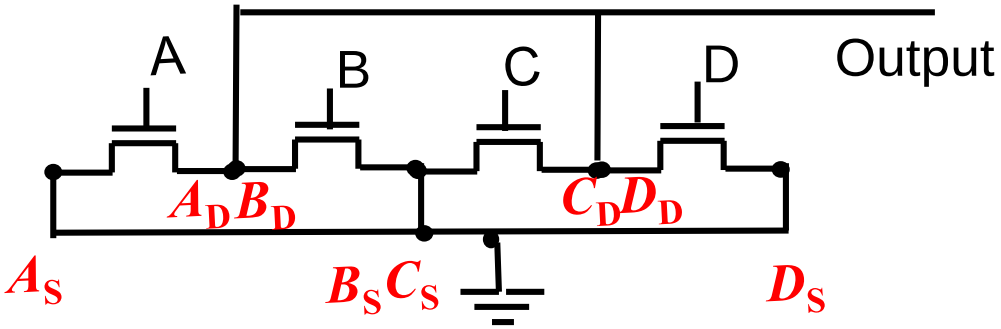


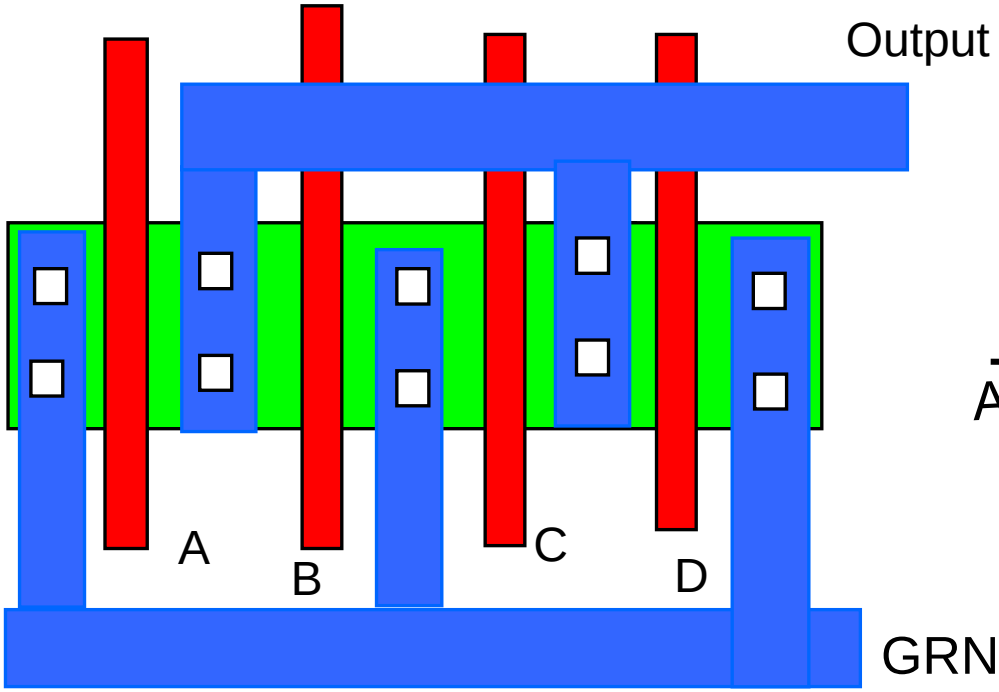
Complex connection

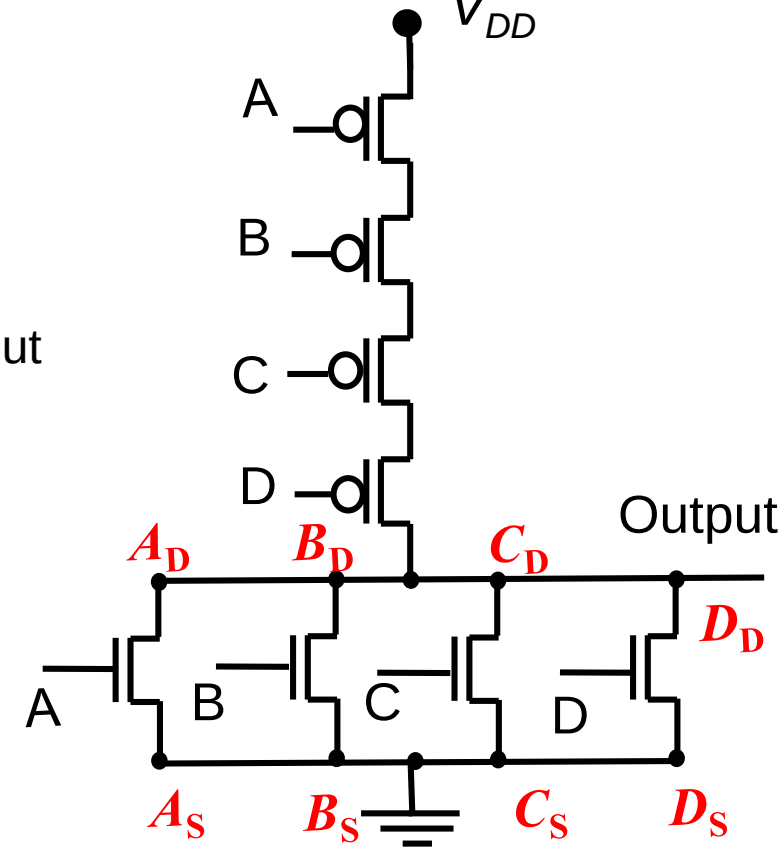




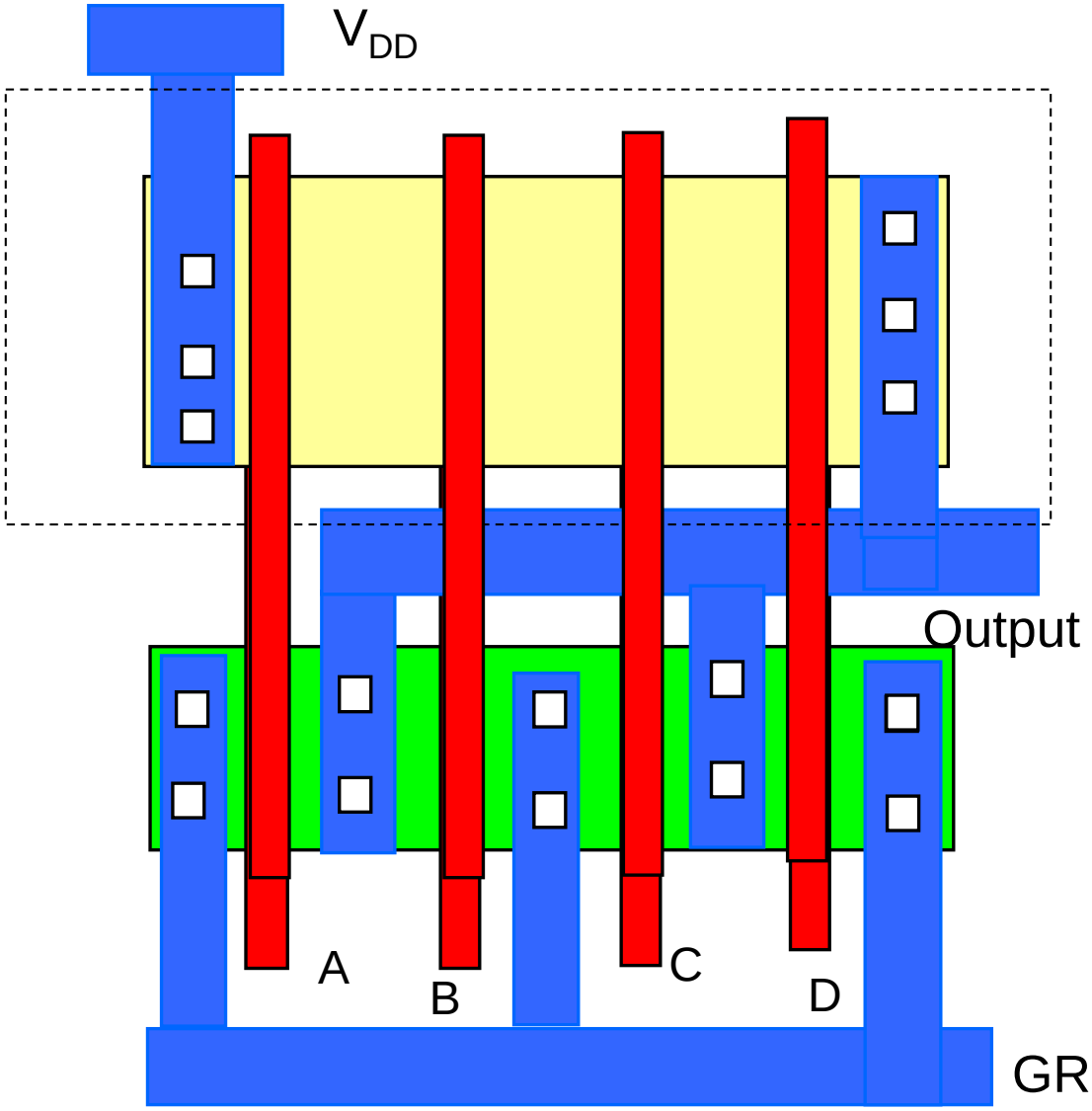
Complex connection

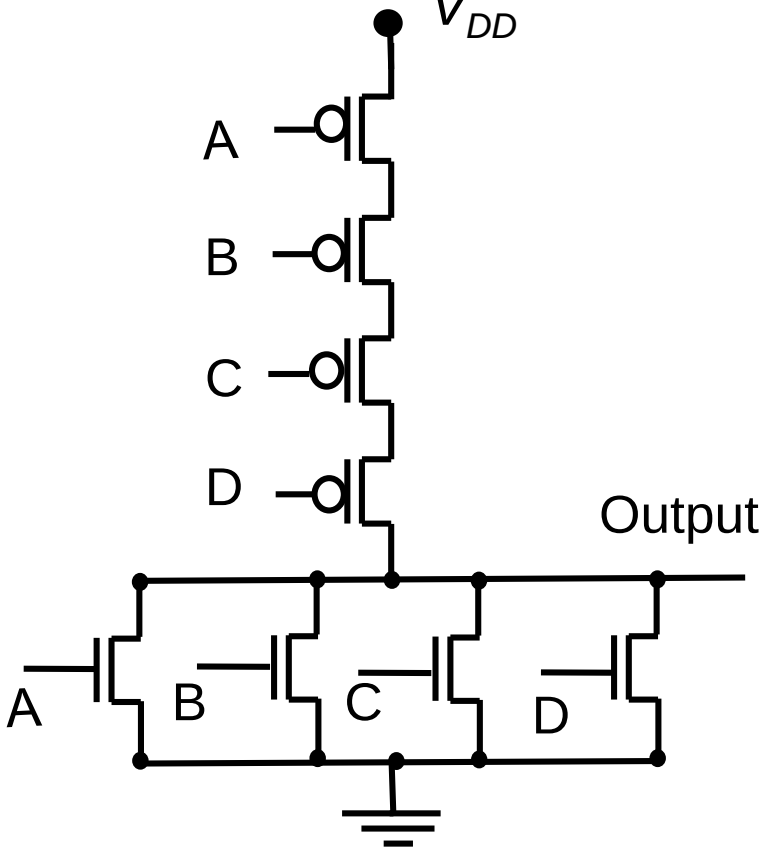




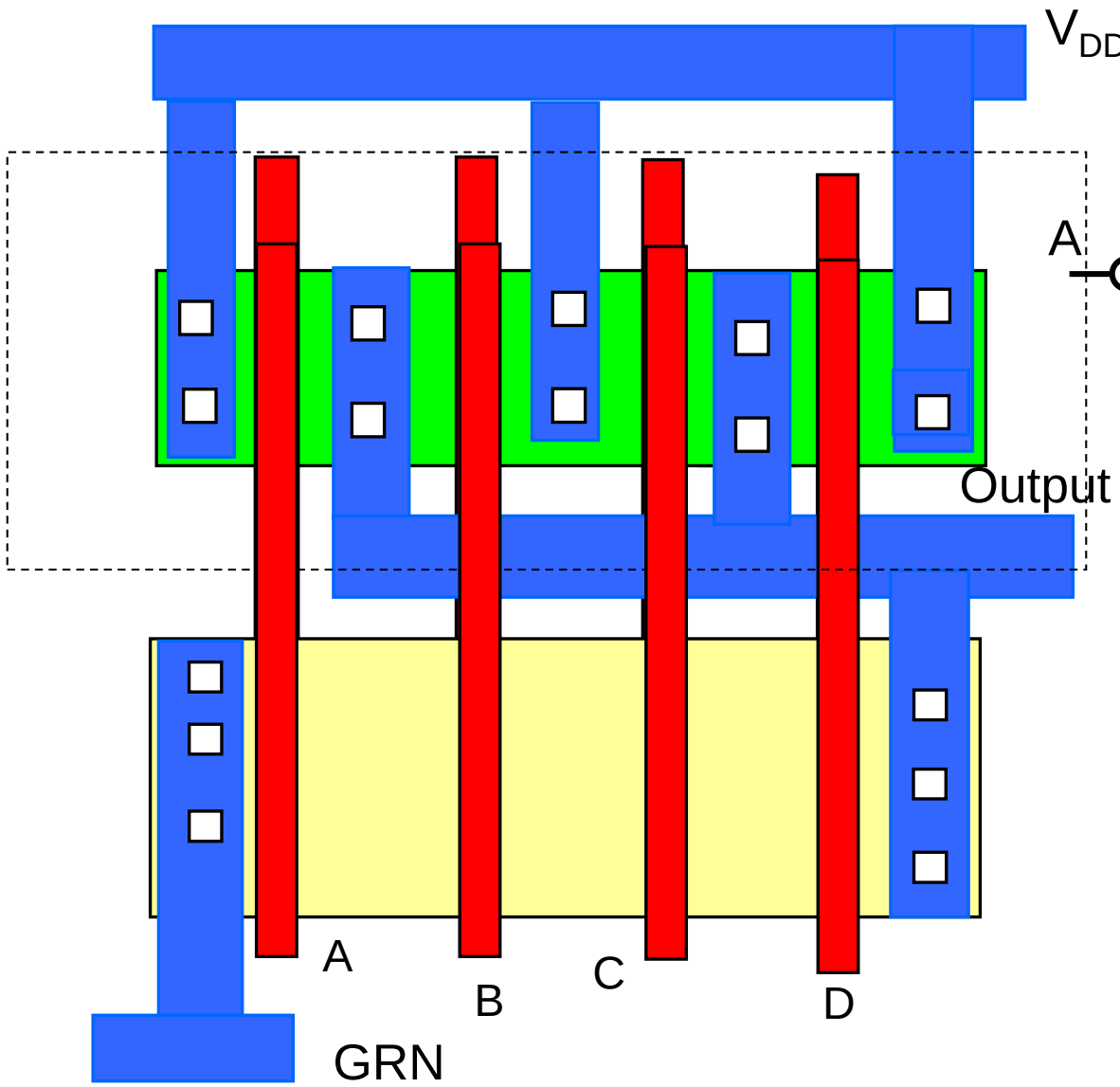


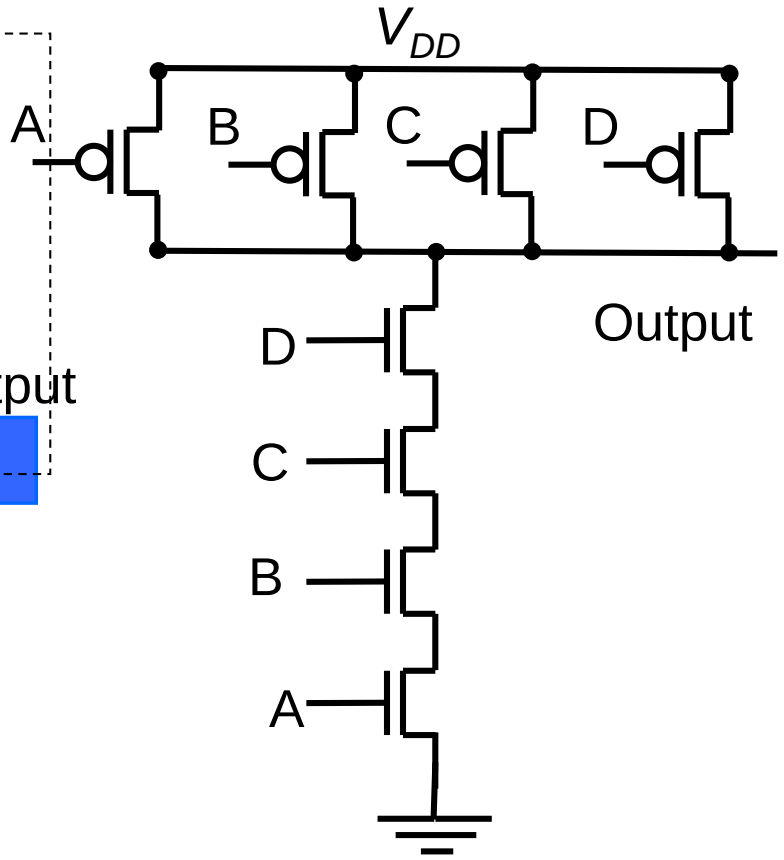
Complex connection





Complex connection

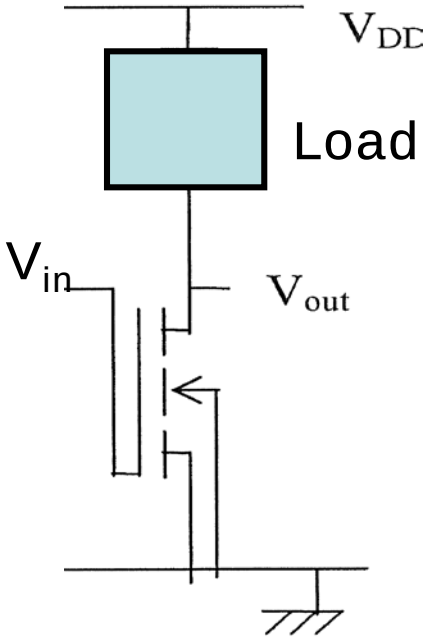




nMOS logic family

- Inverter
- NAND gate
- NOR gate
- General gate
  - Complicated gate

NMOS Logic Inverter

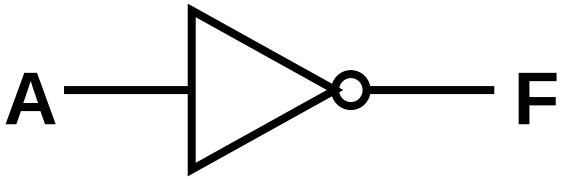


V_{in} = V_{DD} causes NMOS transistor to be on (in triode). Low effective resistance of transistor causes voltage divider with V_{out} **near** 0V.

V_{in} = 0V causes NMOS transistor to be off (cutoff). High effective resistance of transistor causes voltage divider with V_{out} near V_{DD}.

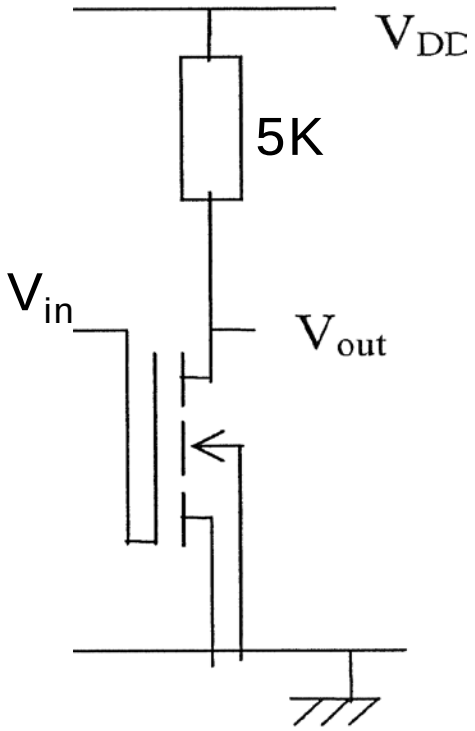
Vin	***Vout***
0 (0V)	1 (V_{DD})
1 (V_{DD})	0 (0V)

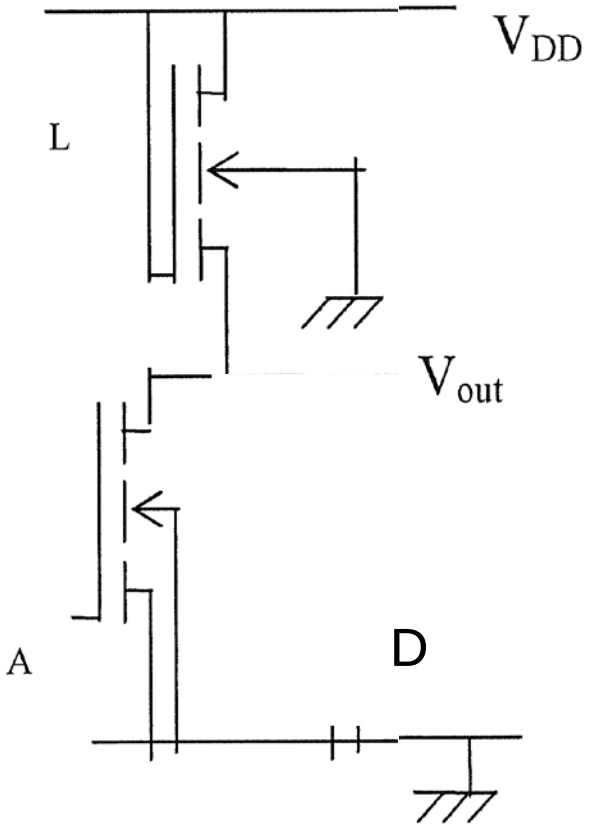
$F = \overline{A}$

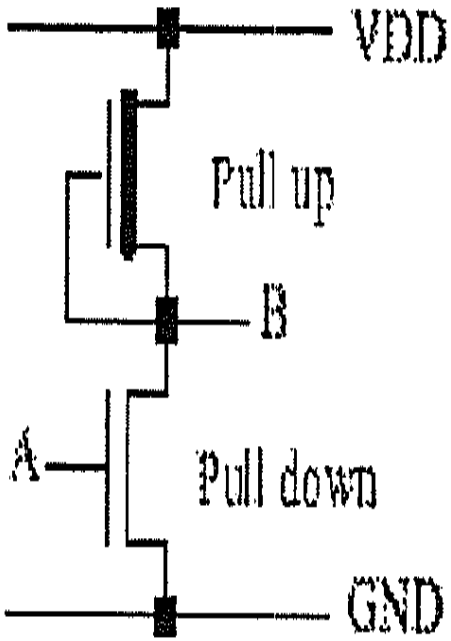


DC power consumption is high !

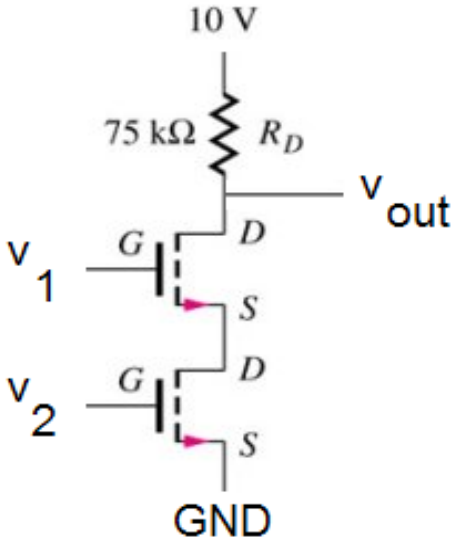
NMOS Logic Inverters







NMOS Logic NAND Gate

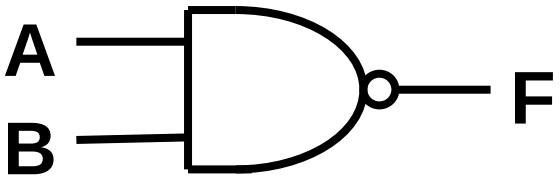


V_1 = V_2 = 10V causes both NMOS transistors to be on (in triode). Low effective resistance of transistors causes voltage divider with V_{out} **near** 0V.

V_1 = 0V or V_2 = 0V (or both) cause one or both NMOS transistors to be off (cutoff). High effective resistance of series transistors cause voltage divider with V_{out} near 10V.

V_1	V_2	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

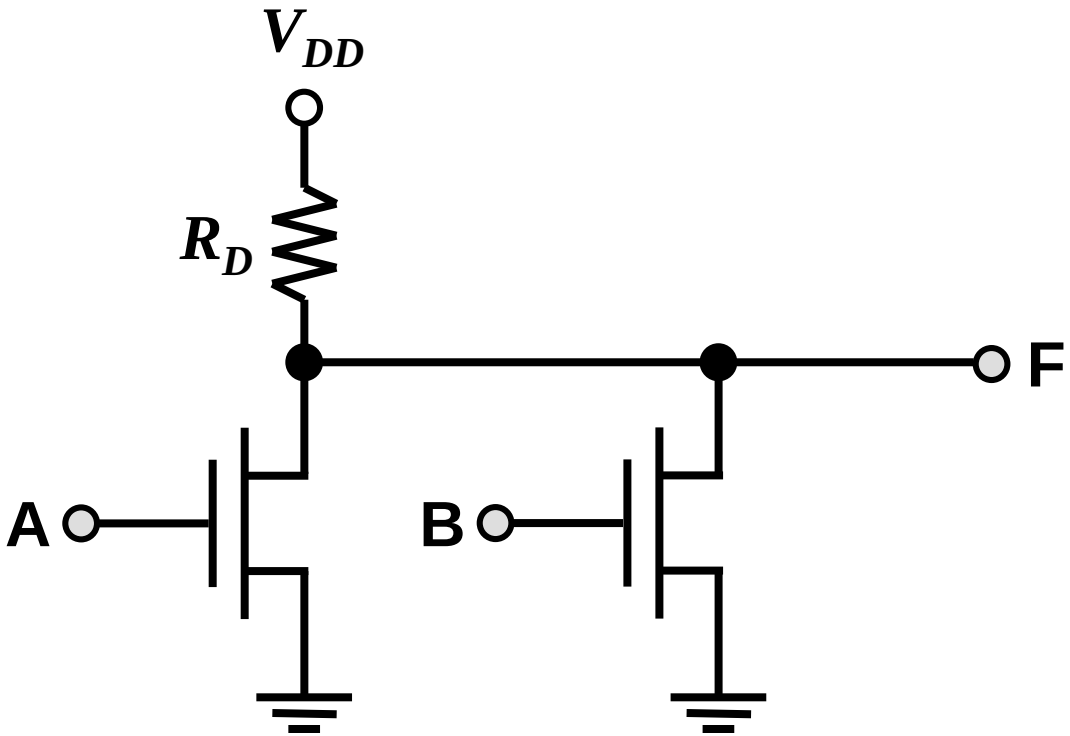
- Output is low only if both inputs are high

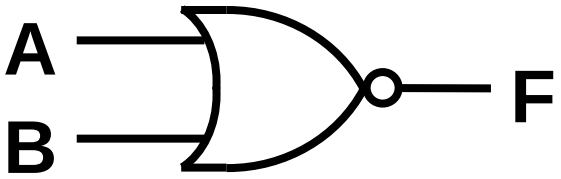


$F = \overline{A \cdot B}$

NMOS Logic NOR Gate

- Output is low if either input is high





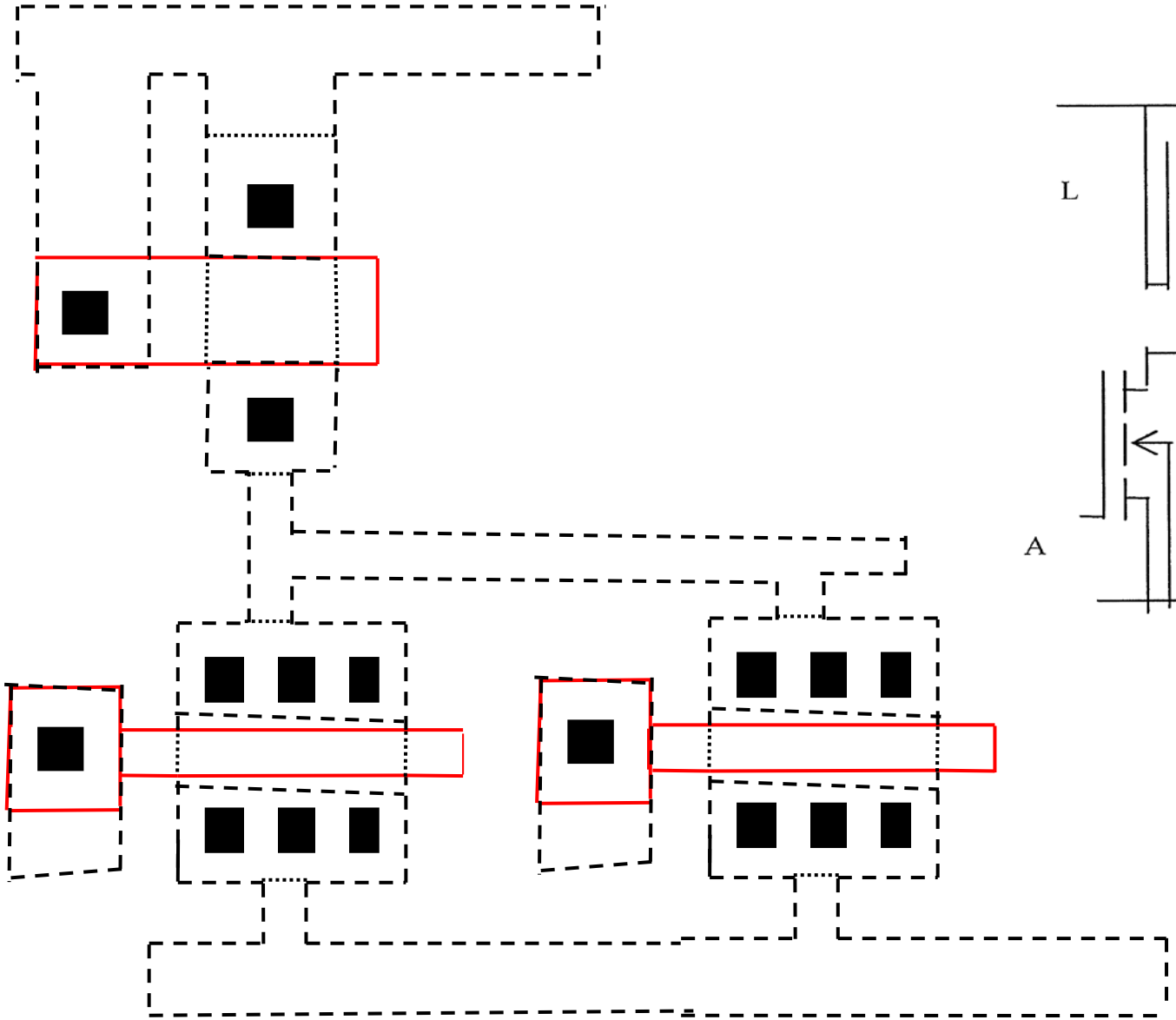
$F = \overline{A+B}$

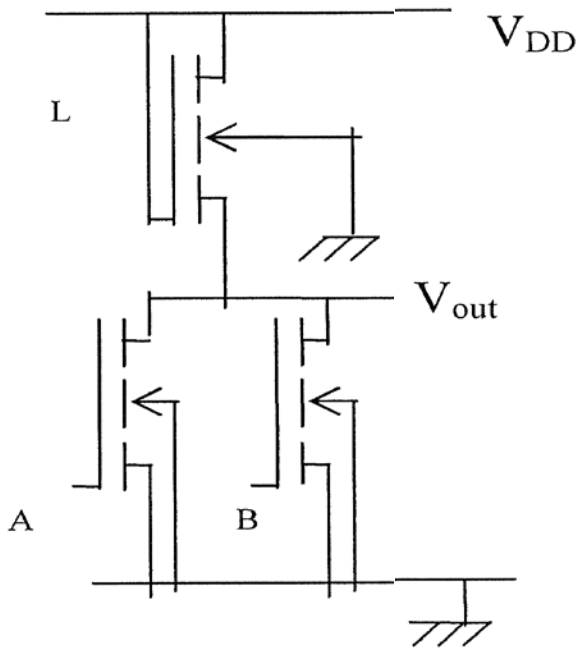
Truth Table

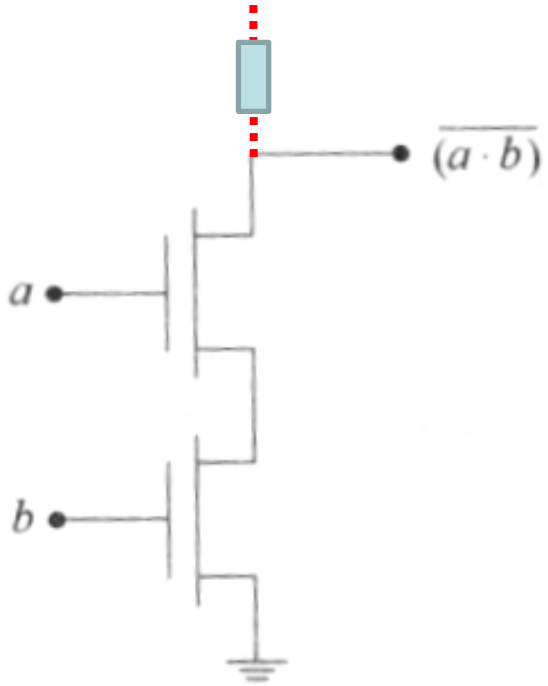
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

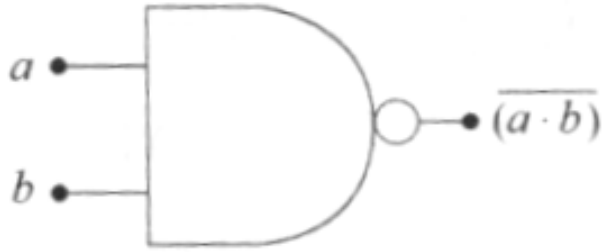
Recall

NMOS NOR gate: example

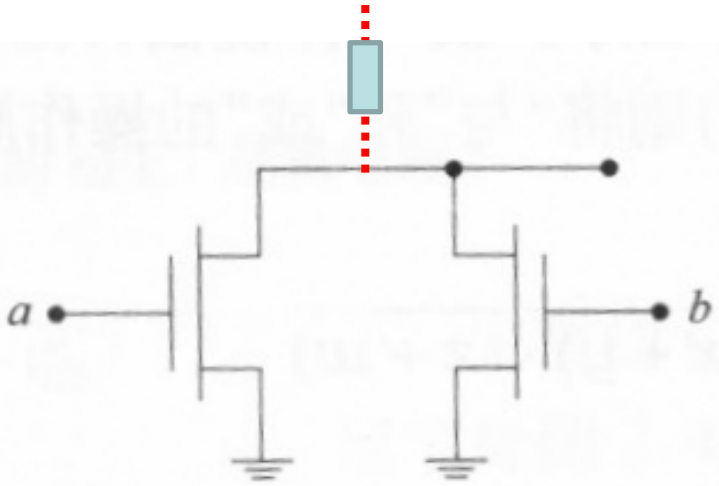


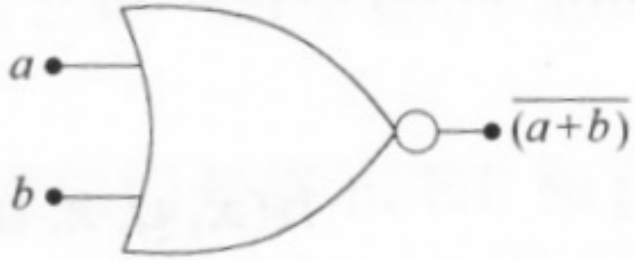






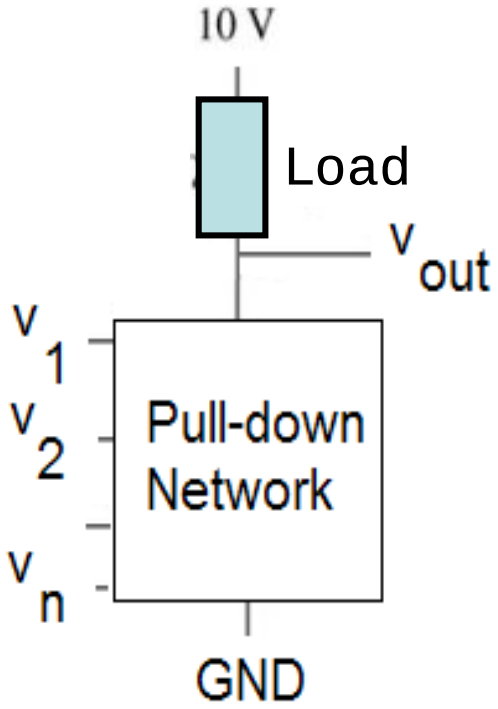
nMOS Transistors in Series Connection





nMOS Transistors in Parallel Connection

NMOS Logic (General)



Any combination of inputs V_1 V_2 … V_n that should result in an output of 0 should produce a low-resistance path from V_{out} to ground in the pull-down network.

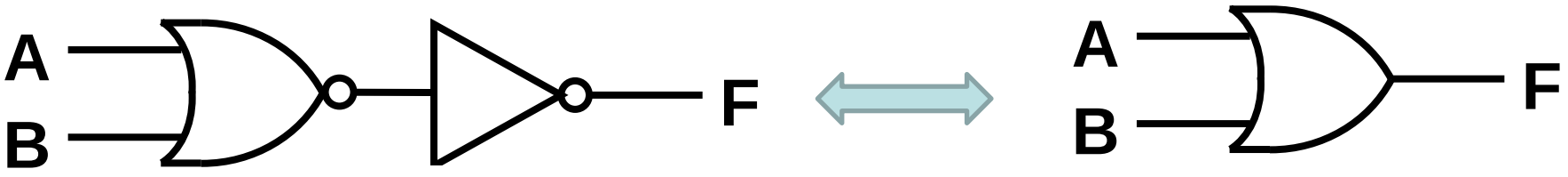
Any combination of inputs that does not pull the output V_{out} to ground through the network will result in the output pulled high through the pull-up resistor R_D.

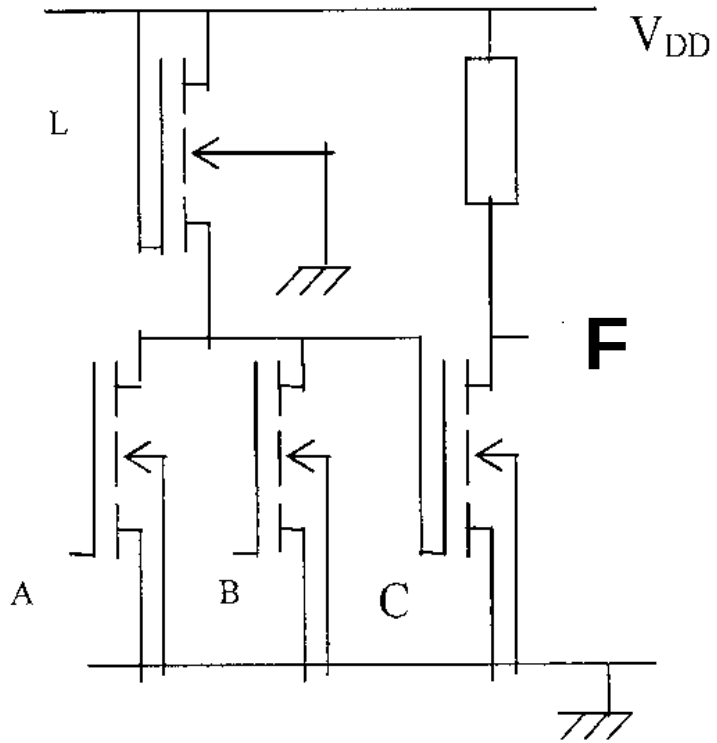
NMOS logic draws current continuously when V_{out} is low.

DC power consumption is high !

Recall

NMOS Logic (General)



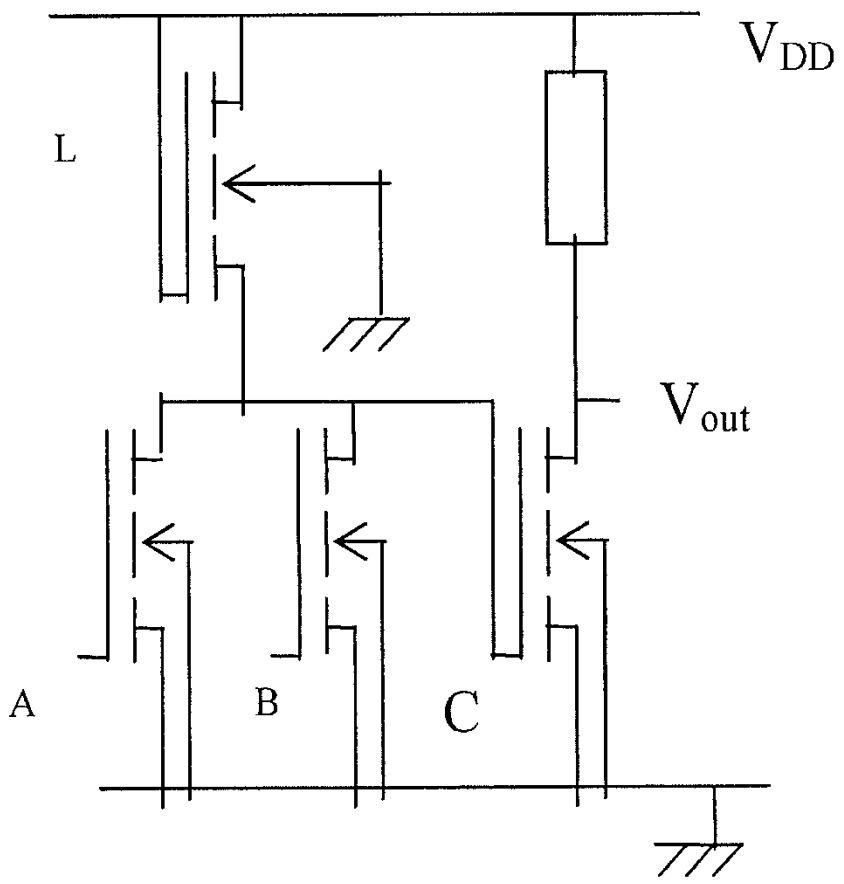


Revision of answers to nMOS IC design (Integrated Electronics & Design)

Recall

Revision of answers to IC design

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.



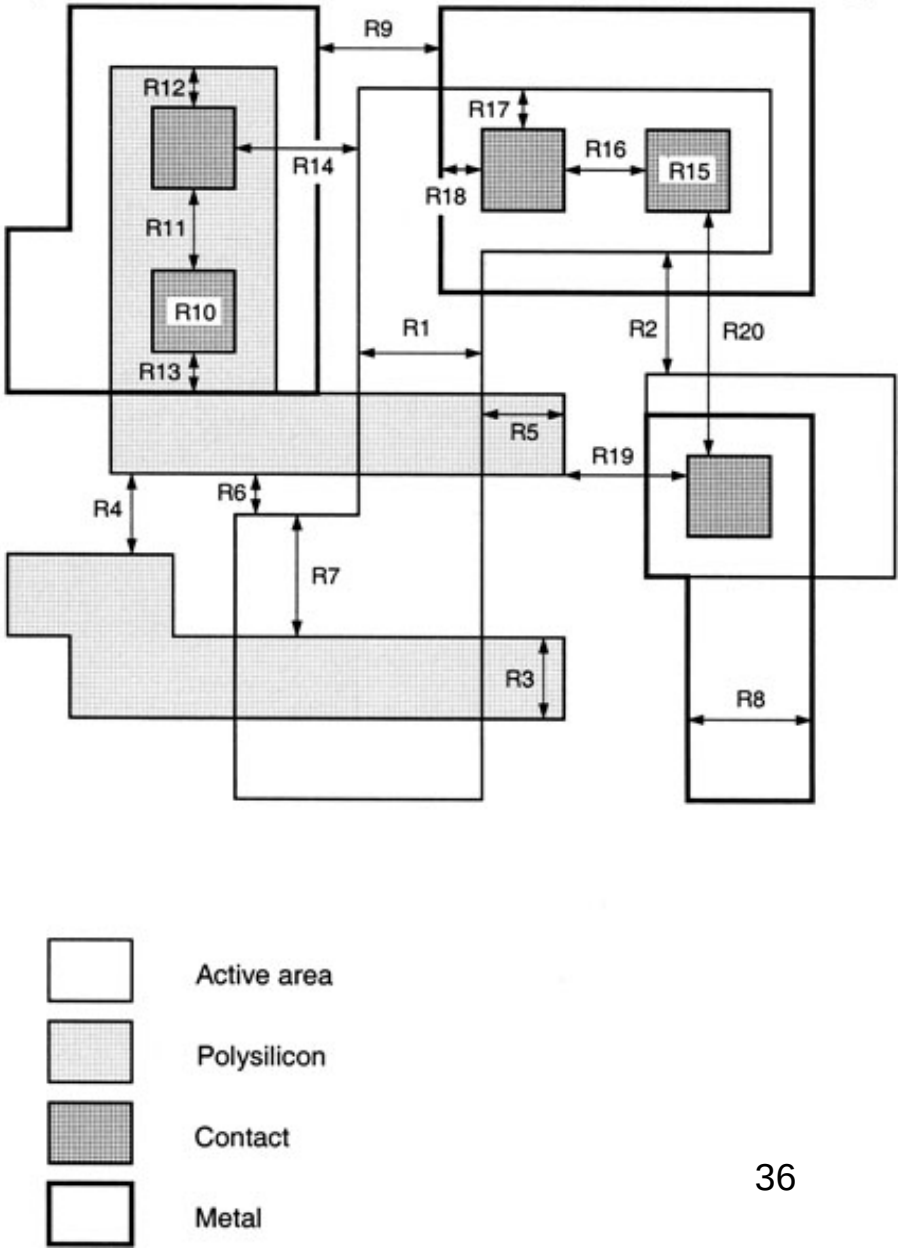
Truth Table

A	B	Vout
0	0	0
0	1	1
1	0	1
1	1	1

MOSIS Rules

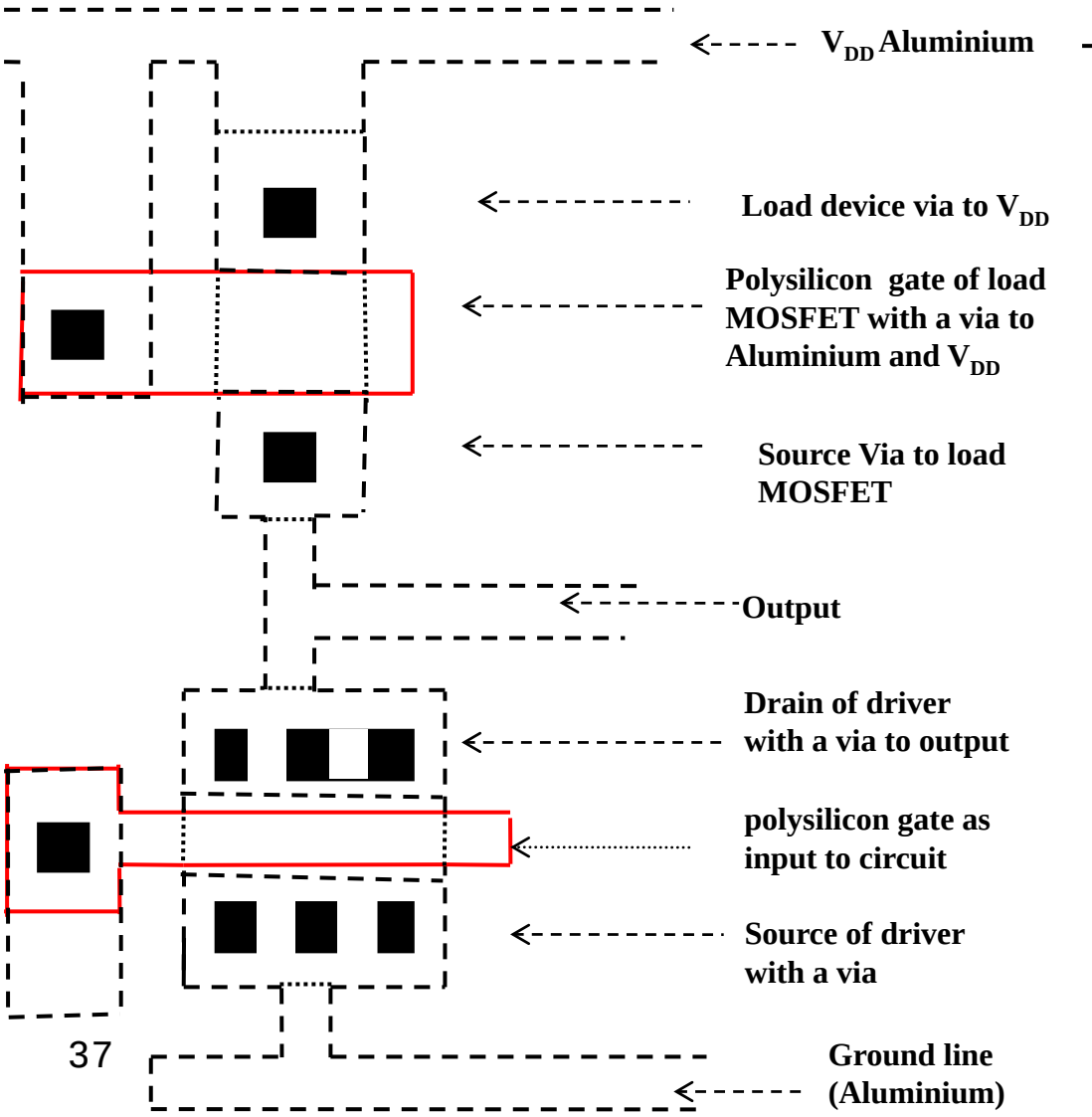
Recall

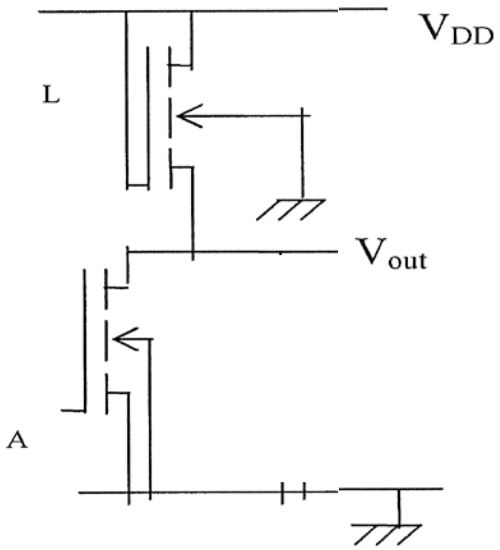
Rule number	*Description*	*λ-Rule*
	Active area rules	
R1	Minimum active area width	3λ
R2	Minimum active area spacing	3λ
	Polysilicon rules	
R3	Minimum poly width	2λ
R4	Minimum poly spacing	2λ
R5	Minimum gate extension of poly over active	2λ
R6	Minimum poly-active edge spacing (poly outside active area)	1λ
R7	Minimum poly-active edge spacing (poly inside active area)	3λ
	Metal rules	
R8	Minimum metal width	3λ
R9	Minimum metal spacing	3λ
	Contact rules	
R10	Poly contact size	2λ
R11	Minimum poly contact spacing	2λ
R12	Minimum poly contact to poly edge spacing	1λ
R13	Minimum poly contact to metal edge spacing	1λ
R14	Minimum poly contact to active edge spacing	3λ
R15	Active contact size	2λ
R16	Minimum active contact spacing (on the same active region)	2λ
R17	Minimum active contact to active edge spacing	1λ
R18	Minimum active contact to metal edge spacing	1λ
R19	Minimum active contact to poly edge spacing	3λ
R20	Minimum active contact spacing (on different active regions)	6λ



Recall

NMOS Inverter: example





Truth Table

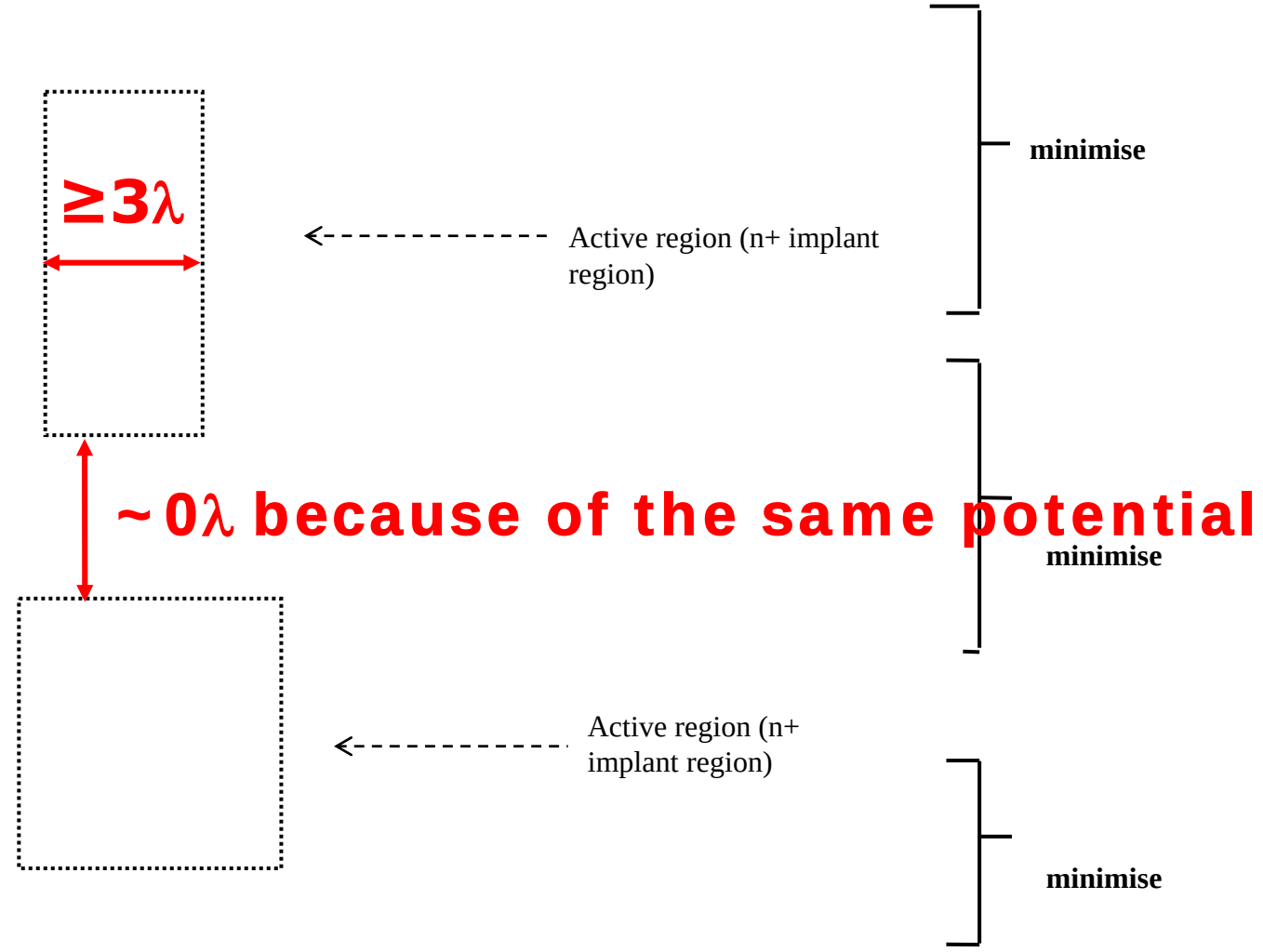
A	Vout
0	1
1	0

37

Recall

NMOS Inverter: example

Mask1

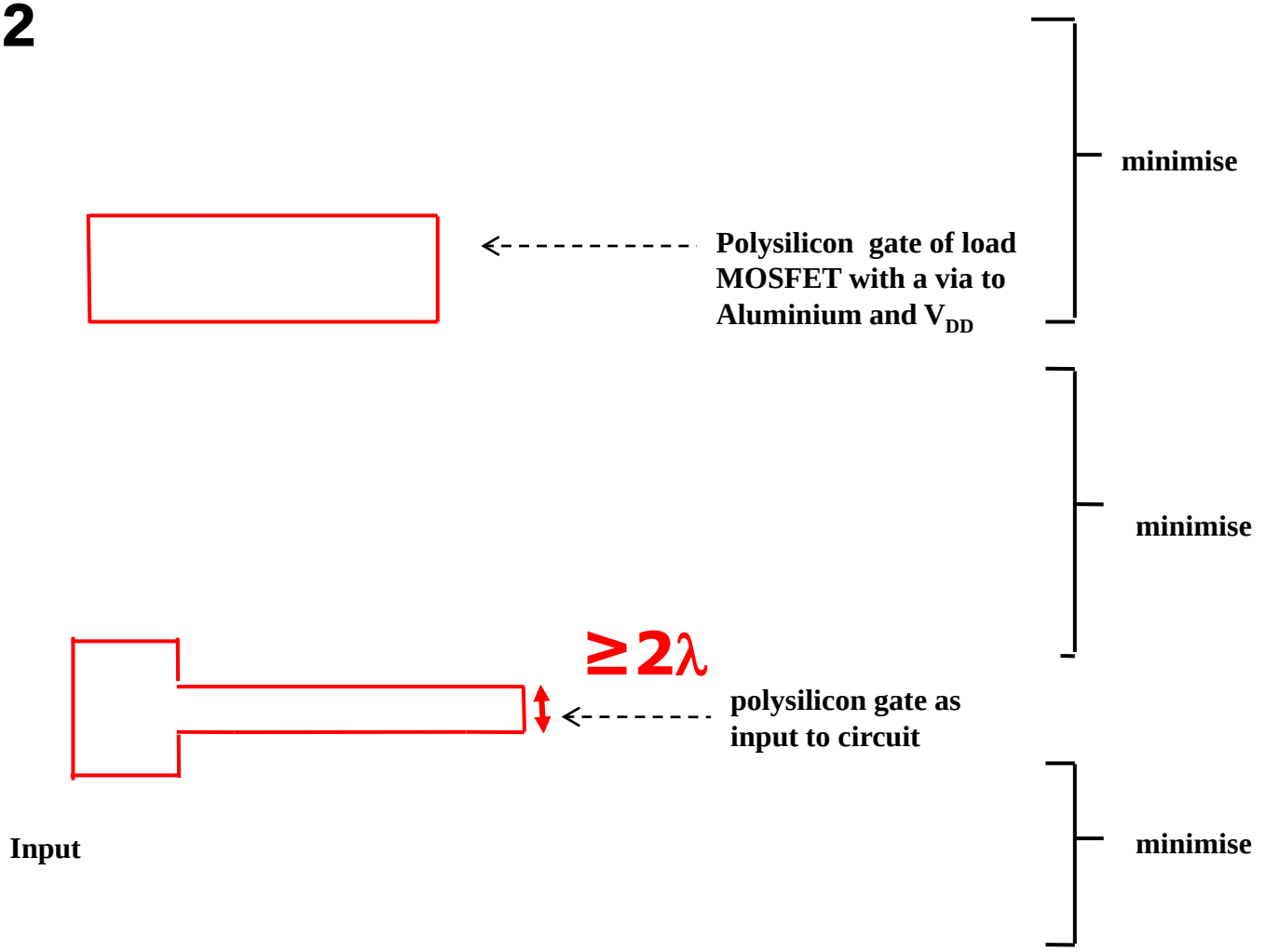


38

Recall

NMOS Inverter: example

Mask2

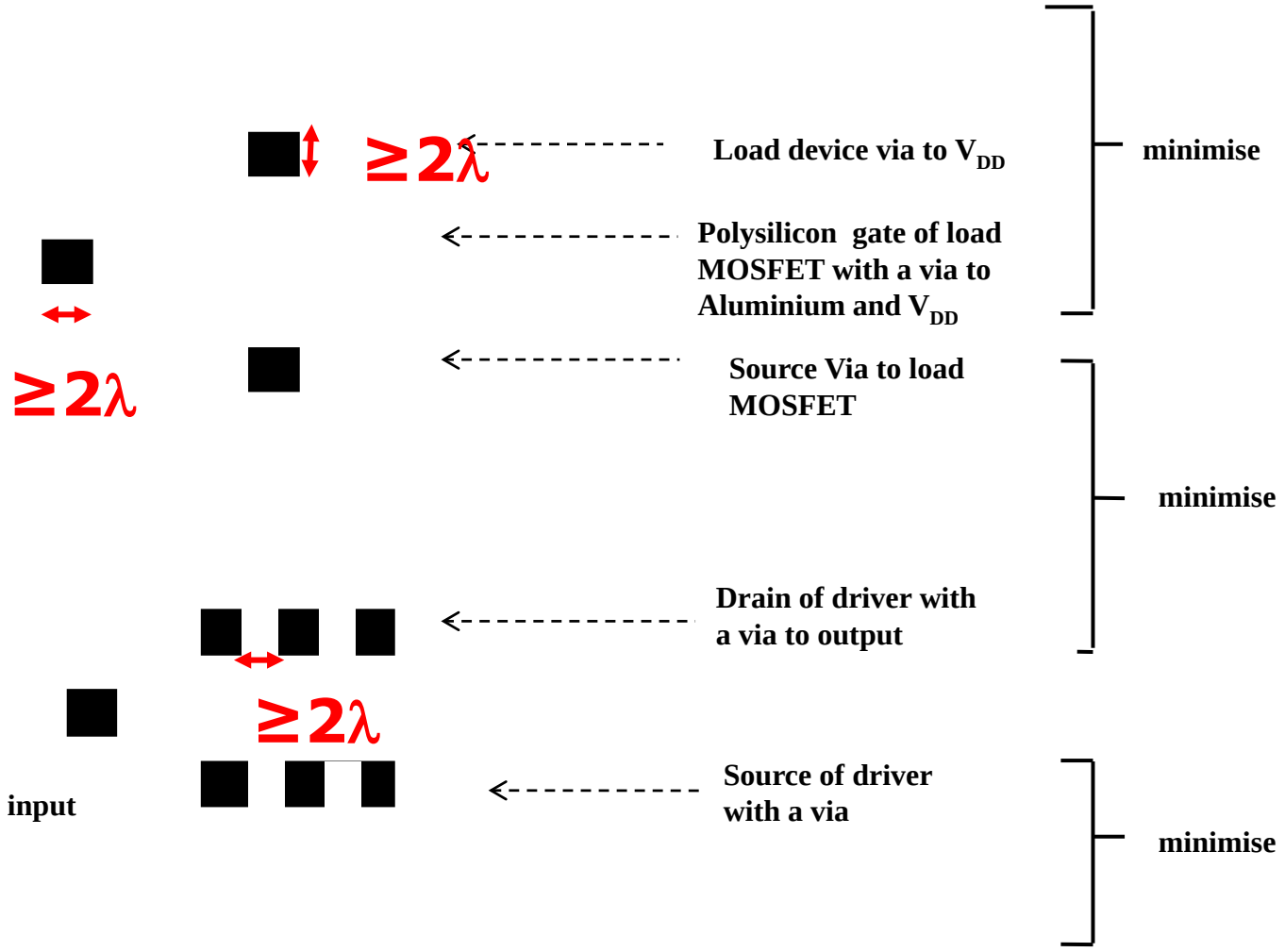


39

Recall

NMOS Inverter: example

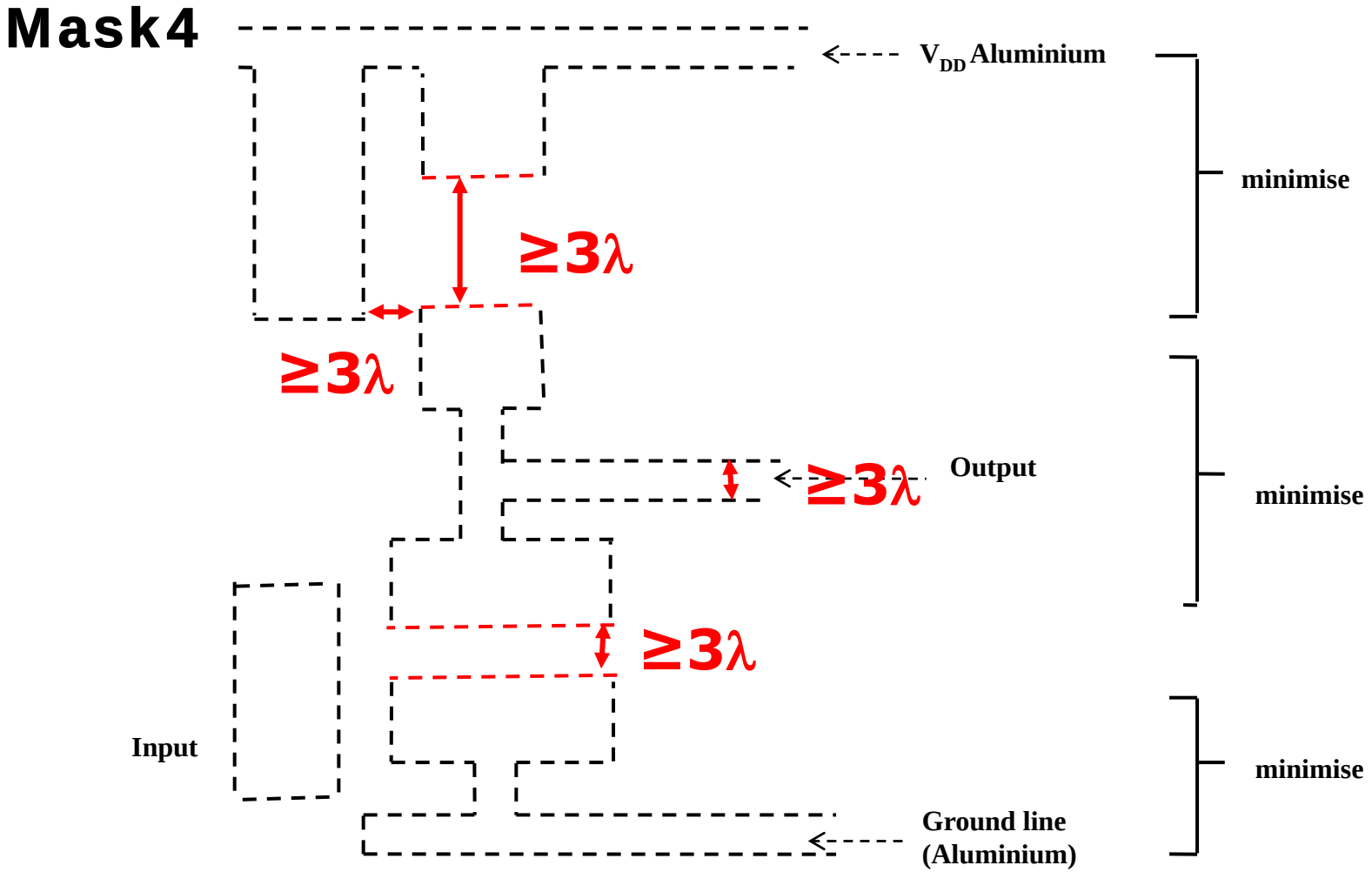
Mask3



40

Recall

NMOS Inverter: example

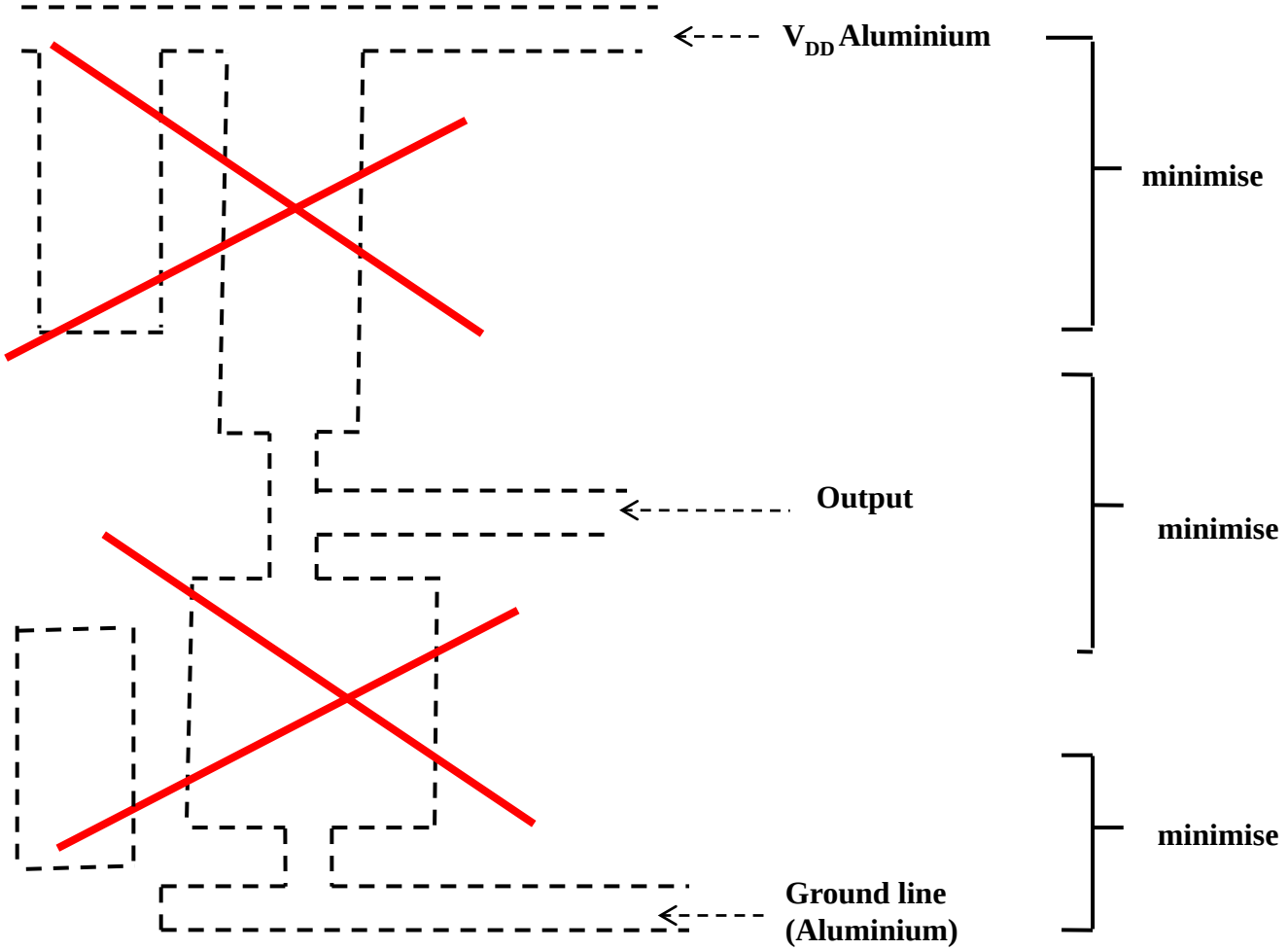


41

Recall

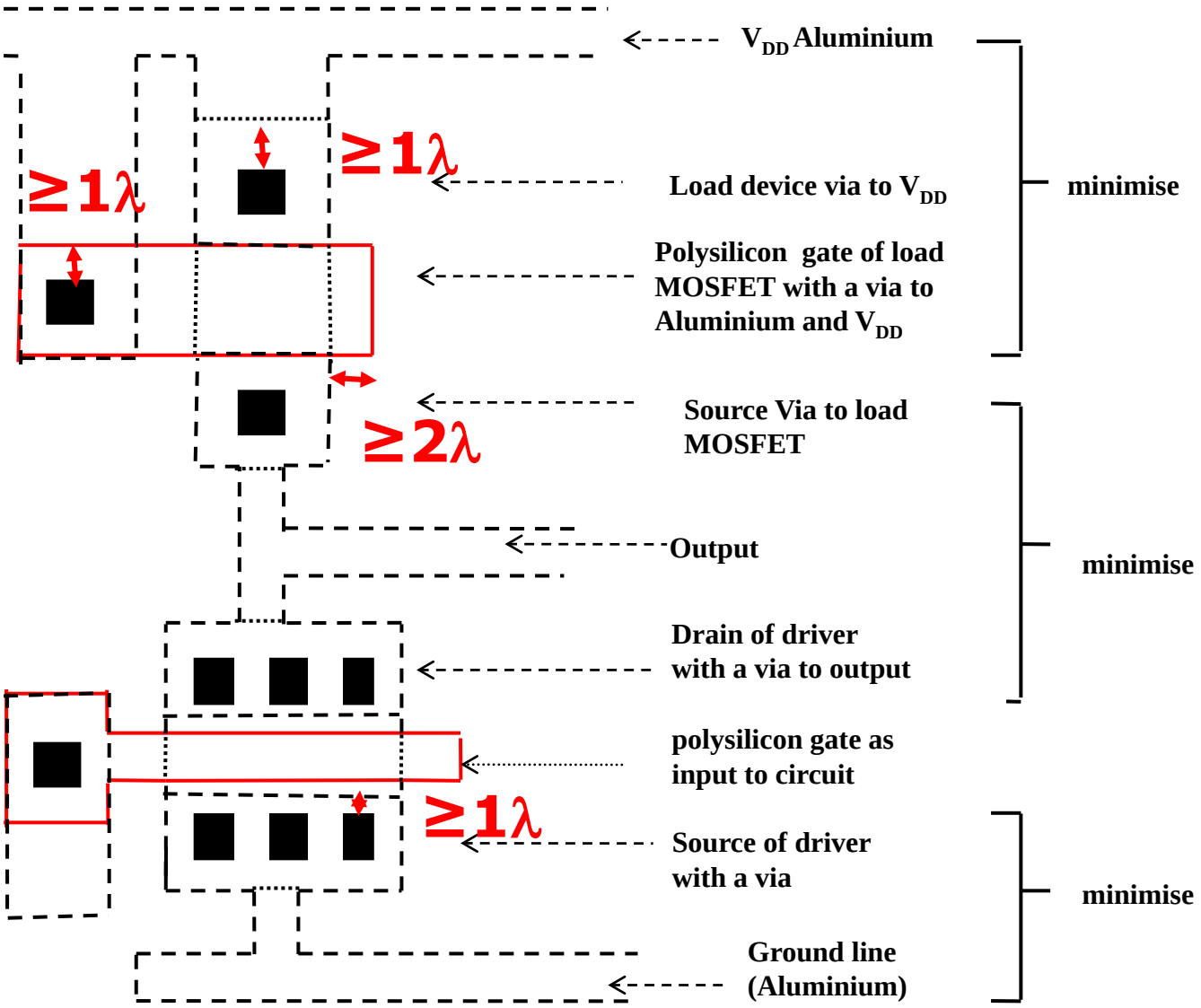
NMOS Inverter: example

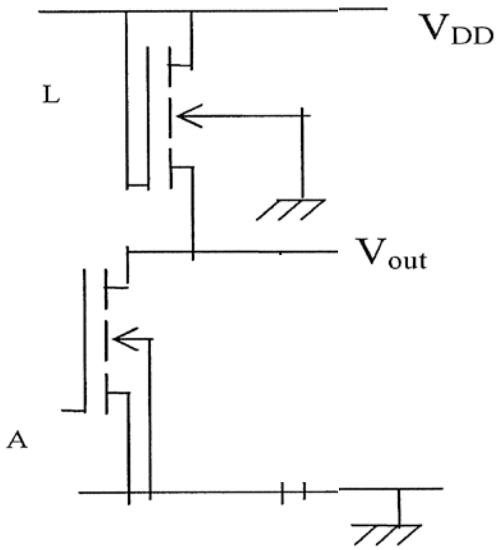
Mask4



Recall

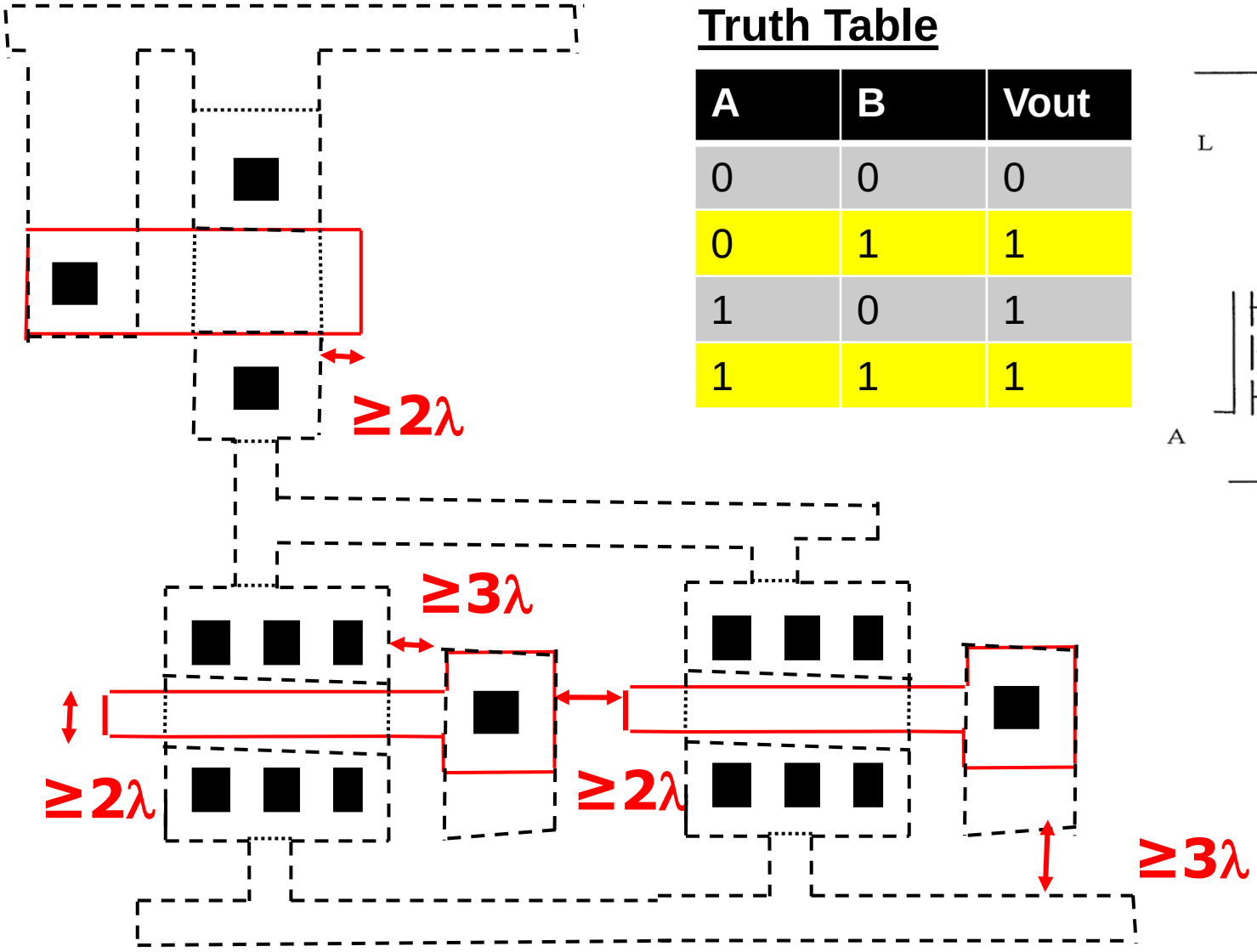
NMOS Inverter: example





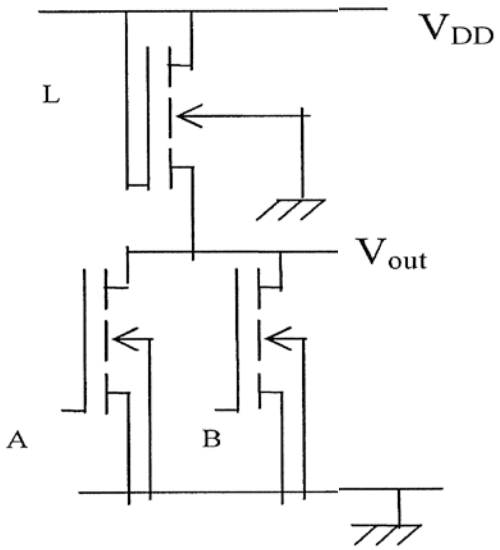
Recall

NMOS NOR gate: example



Truth Table

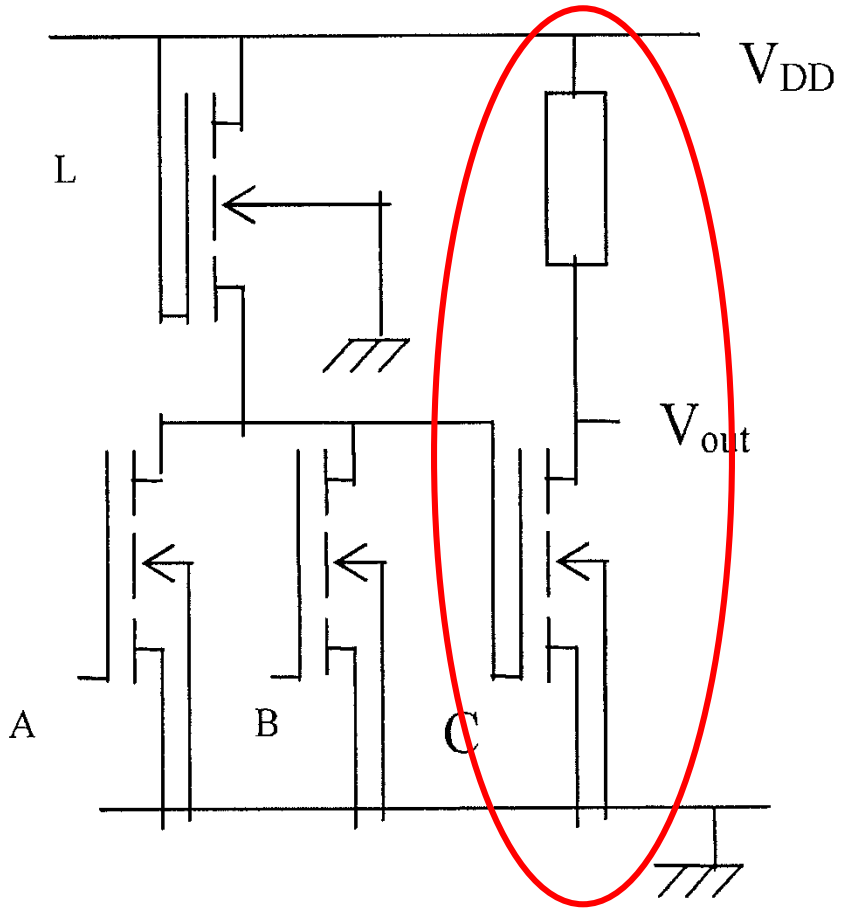
A	B	Vout
0	0	0
0	1	1
1	0	1
1	1	1



Recall

Complicated gate: example

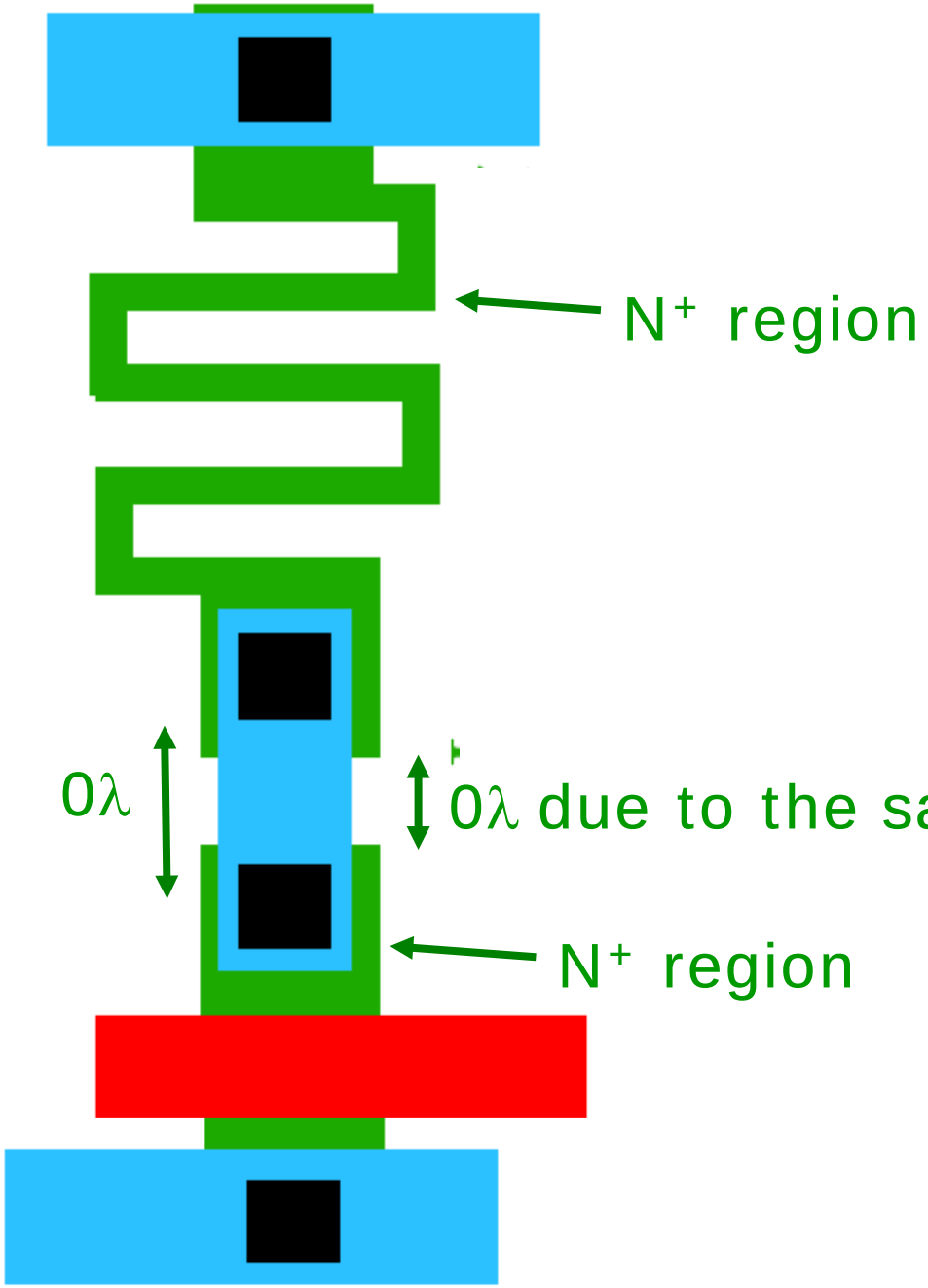
- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.

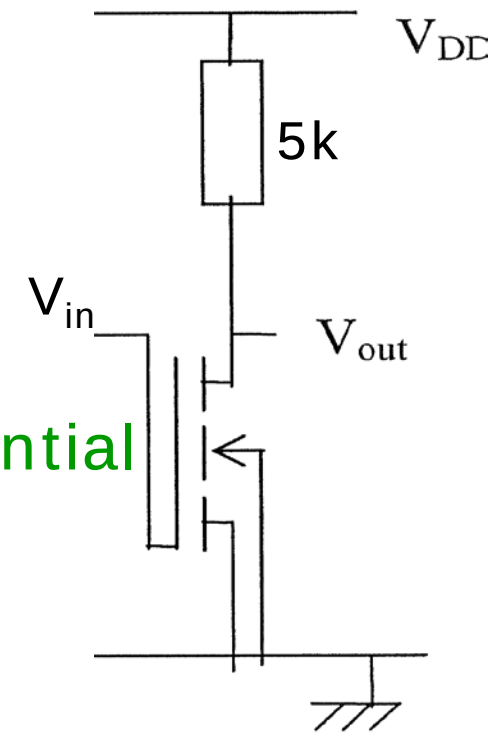


Truth Table

A	Vout
0	1
1	0

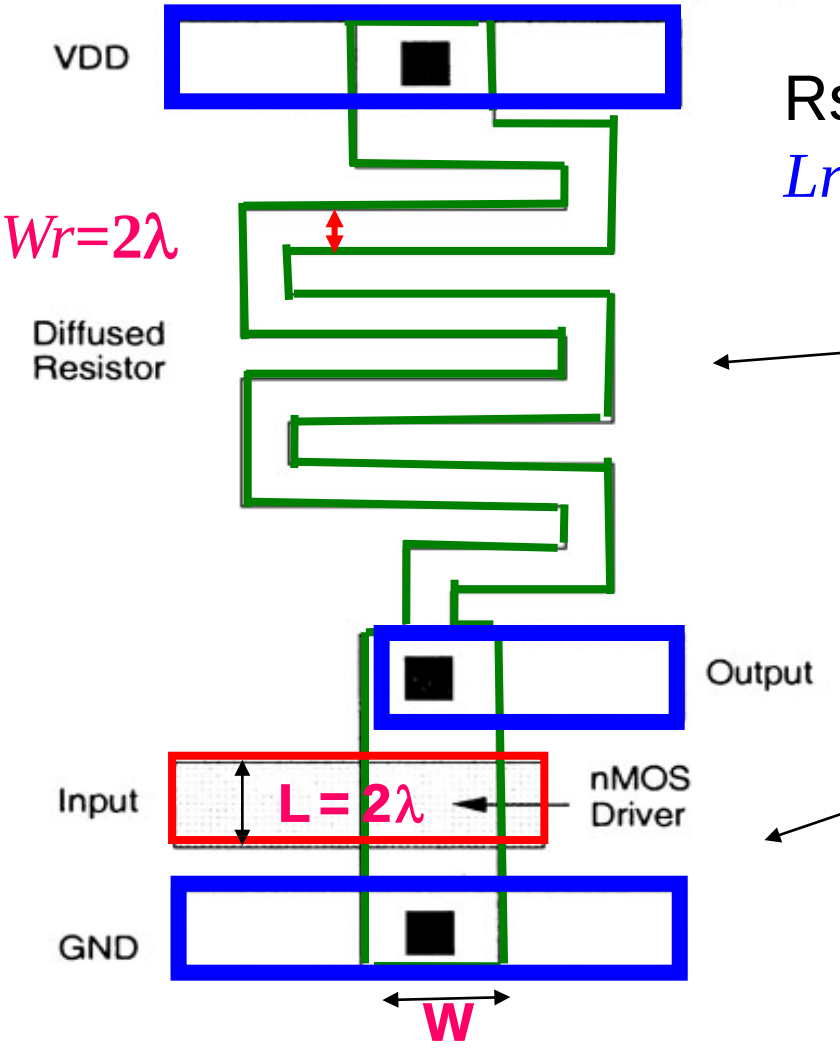
Recall


N+ region
0λ
0λ due to the same potential
N+ region


VDD
5k
Vin
Vout

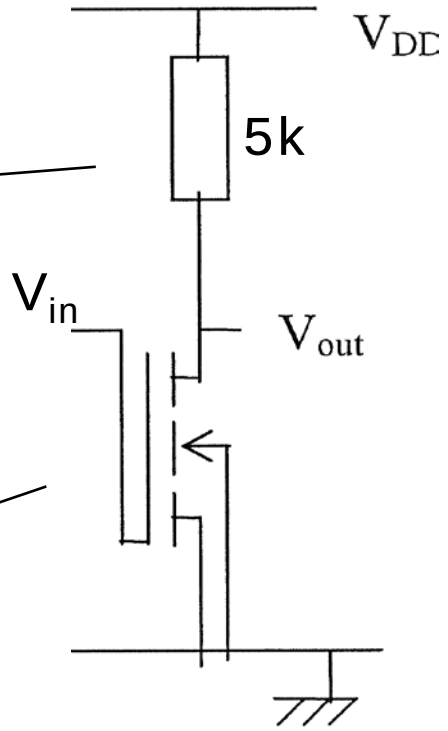
Recall

NMOS Logic (Inverter): example1



Rs = 100Ω/sq →

Lr/Wr = **50**, *Wr* ≥ **2λ**



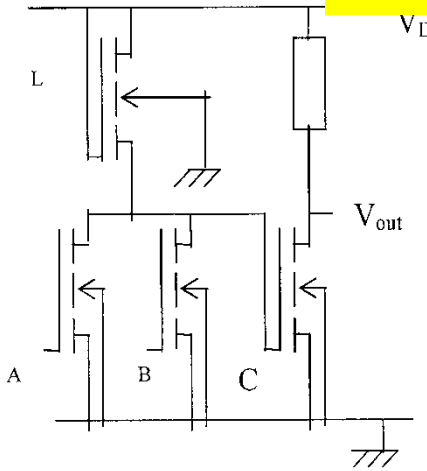
MOSFET

→ W/L=**12**,

L=2λ

Recall

NMOS IC: example



$>3\lambda$

V_{DD}

$\geq 2\lambda$

V_{out}

$\geq 3\lambda$

$\geq 2\lambda$

$\geq 2\lambda$

$\geq 3\lambda$

A

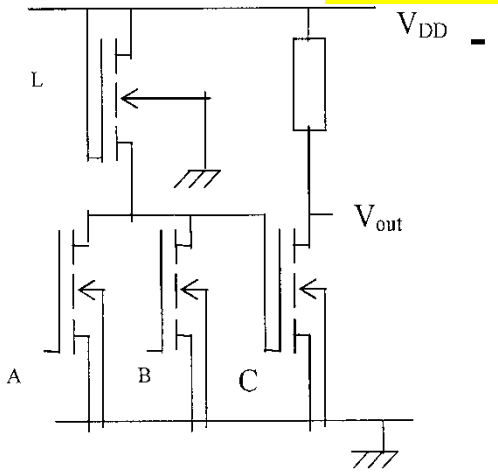
B

GRN

$>3\lambda$

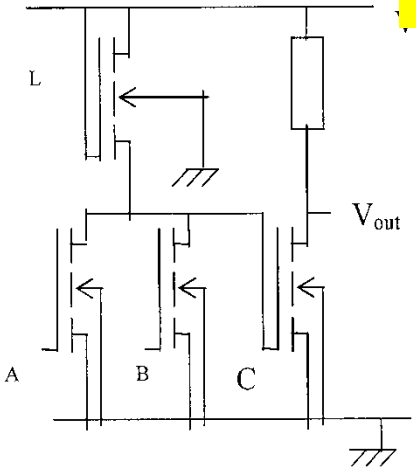
Recall

NMOS IC: example



Recall

NMOS IC: example



Recall

NMOS IC: example