Lecture 10

of

EEE307

Electronics for Communications

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Friday, 22nd November 2019

- Phase Locked Loop
  - phase detector & type I PLLs
  - loop dynamics (phase domain)
  - PFD & type II PLLs
  - charge pump PLLs
- Frequency Synthesizers

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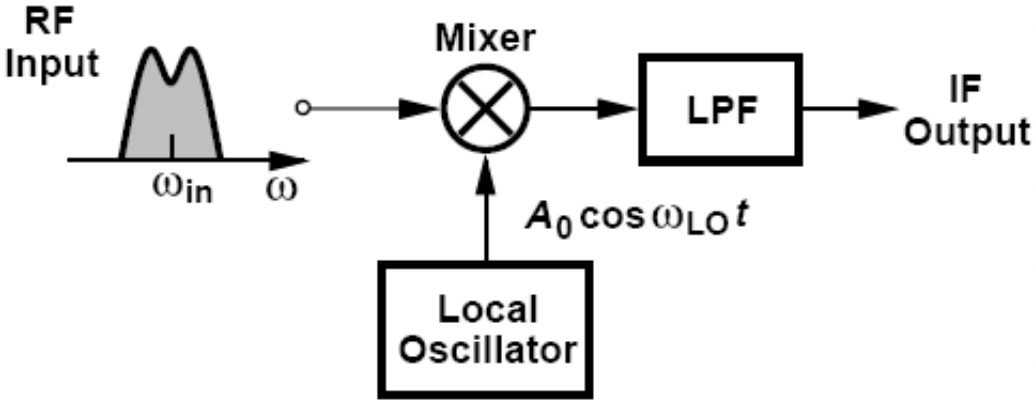
Radio Transmitters & Receivers

(local oscillator signal required)

- In radio transmitters and receivers, a **local oscillator** (LO) signal is required as a mixer input for the upconversion and downconversion to and from the carrier frequencies of the radio waves.



From: Behzad Razavi, *RF Microelectronics*,

- While a **voltage-controlled oscillator** (VCO) can generate such a required signal, it is not used alone to feed the LO port of the mixers.

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Signal-Generation with VCO

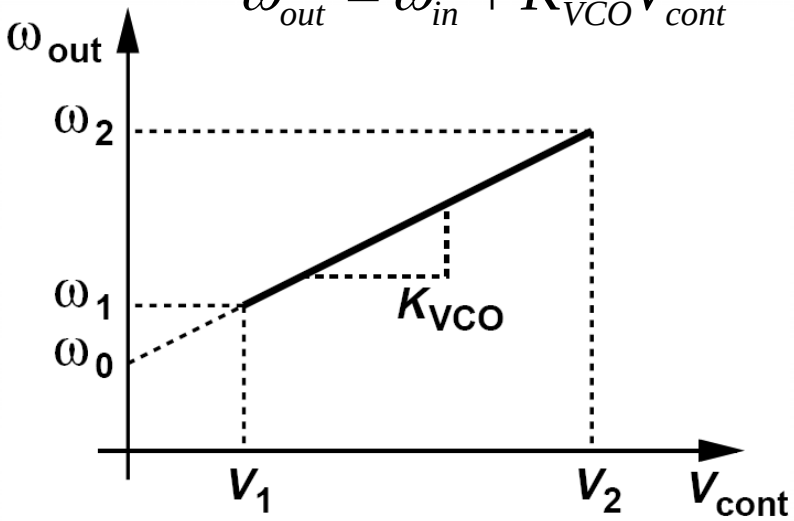
(open-loop problems)

- A VCO is seldom used in the open-loop condition for signal generation in wireless transmitters and receivers:

  - open-loop: fix the input voltage V_{cont} and get a sinusoidal signal of the desired frequency

$$\omega_{out} = \omega_{in} + K_{VCO} V_{cont}$$

open-loop VCO



  - It is like the uncommon open-loop use of operational amplifiers. (What would be the problems?)

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Frequency Synthesizer as LO

(VCO in phase locked loop)

- A VCO is usually used in the so-called **phase-locked loop** (**PLL**) for generating LO signals in a transceiver.

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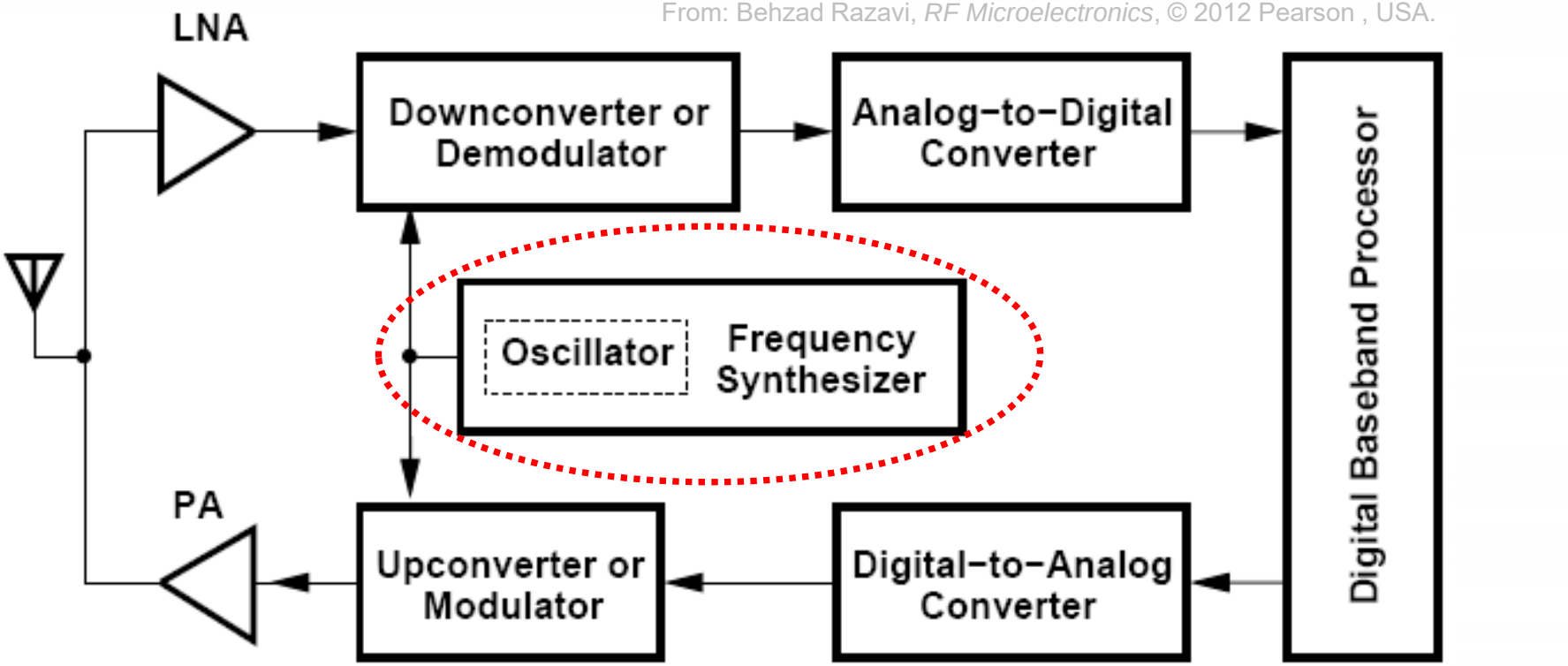

- It is called a **frequency synthesizer**.

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VCO in Phase Locked Loop

(stable synthesized frequencies)

- By using a VCO in a **PLL** for **frequency synthesis** (i.e. generating sinusoidal electrical signals of desirable frequencies), a highly stable yet tunable LO signal can be created for radio transceivers.
  - The VCO is treated as a linear time-invariant system and configured in a feedback system to form the PLL.
  - The ***synthesized*** **frequencies** of the **PLL** output are a multiple of a reference frequency (e.g. by a crystal oscillator), with the same **frequency stability** and precision as that of the reference input.
  - Do you remember **crystal oscillators**? Signal generation with stable ω_{osc}.

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Usefulness of Phase Locked Loops

(in FM communication & digital systems)

- Apart from **frequency synthesis** or **multiplication** from highly stable low-frequency signals, **PLLs** can also be used for **frequency modulation** (FM) and frequency demodulation which are important in FM communication.
- **PLLs** are also used in digital systems, especially in data communications, for signal **synchronisation**.
  - in microprocessors for **skew reduction** or **compensation** to overcome the delay between the buffered clock signal and the data stream; a delay locked loop is an alternative
  - also in harddisk drive electronics in reading and transferring data

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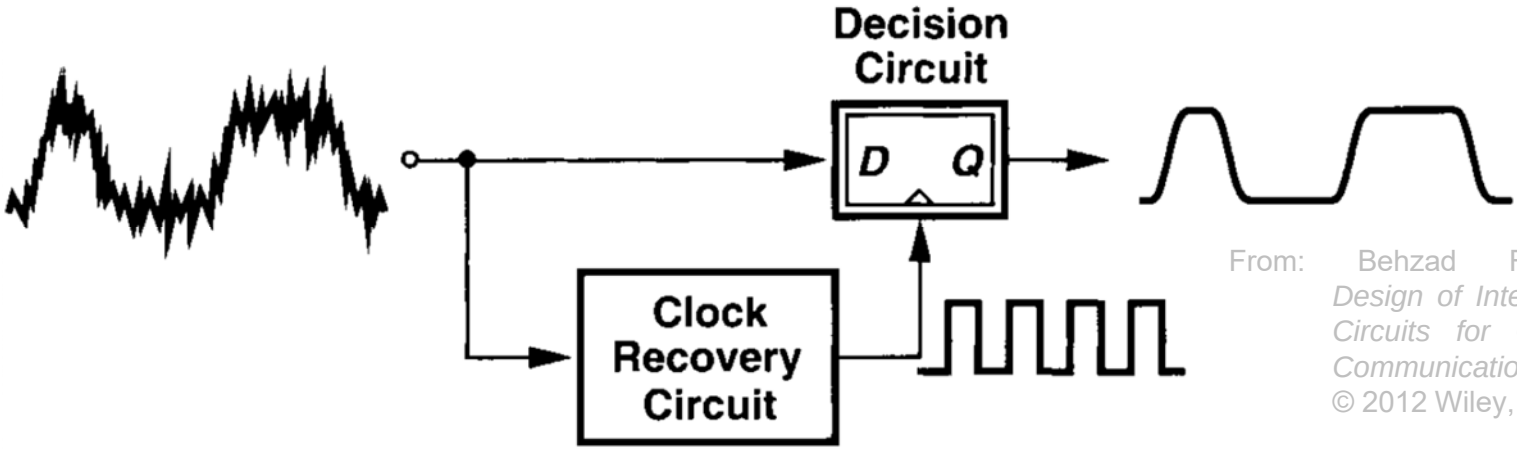
PLLs in Clock & Data Recovery

(digital data streams)

- An important application of PLLs is **clock recovery**, namely, ***recovering* clock timing** information from an ***incoming* data stream** corrupted by noise.
  - The incoming data is sometimes also cleaned up and the whole process is known as **clock** and **data recovery** (CDR).



From: Behzad Razavi, *Design of Integrated Circuits for Optical Communications*, 2e

  - CDR is necessary in high-speed asynchronous serial data links.

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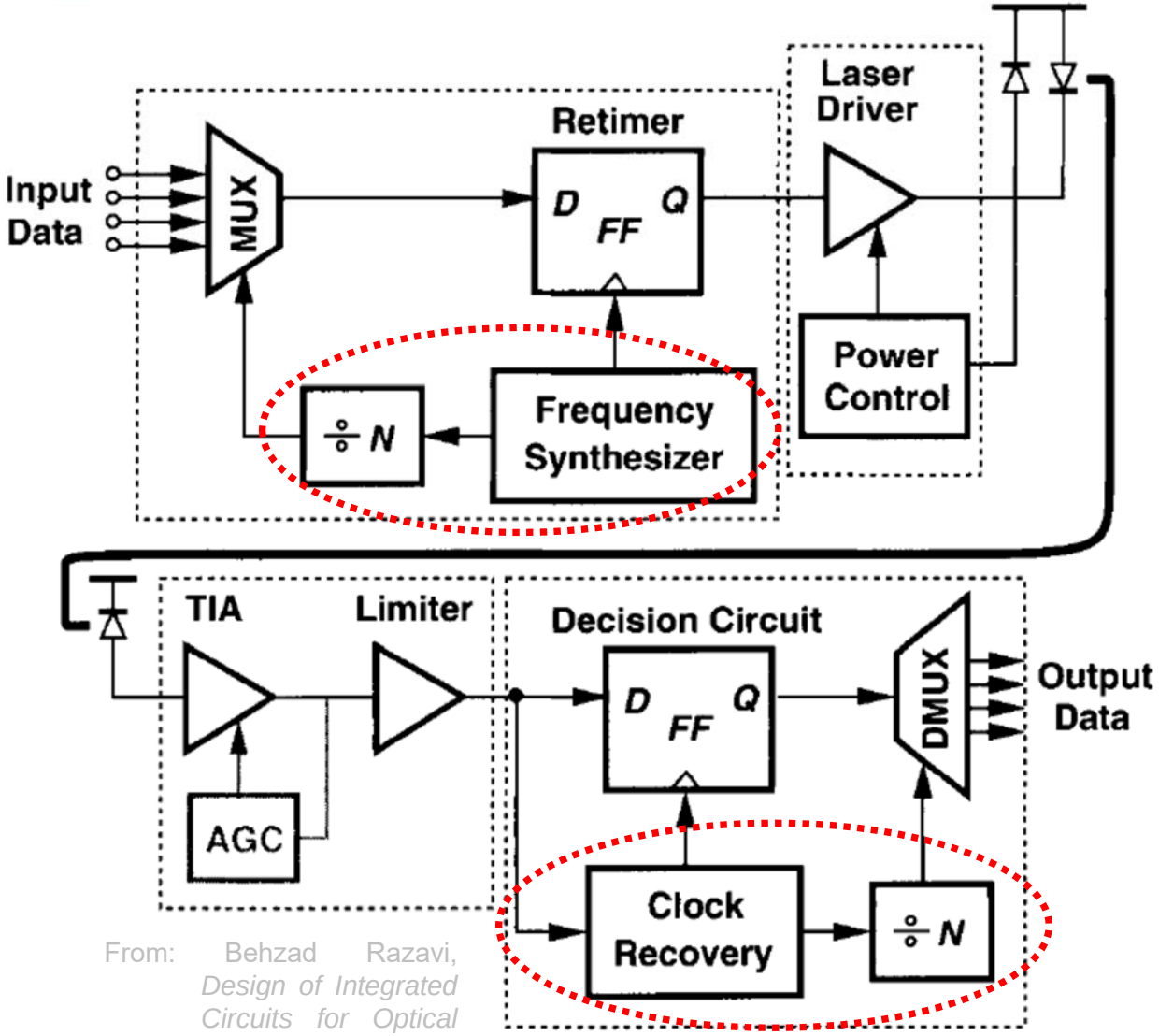
Optical Communication Systems

(frequency synthesis & clock recovery)



From: Behzad Razavi, *Design of Integrated Circuits for Optical Communications*, 2e © 2012 Wiley, USA.

- **Frequency synthesis** and **clock recovery** are essential in fibre-optic communication systems.
  ⇒ importance of **PLLs** in modern communication systems.

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Phase Locked Loop

(three basic constituents)

- A **phase-locked loop** (**PLL**) is a negative ***feedback*** system with the output signal tracking the input signal by comparing the phase (and frequency) of the output with that of the input.
- A PLL consists of three basic parts cascaded together and forming a closed loop:
  - a **phase detector** (a phase/frequency detector in better designs of PLLs)
  - a low-pass loop filter
  - a **voltage-controlled oscillator** (VCO)
  - a feedback divider in some cases

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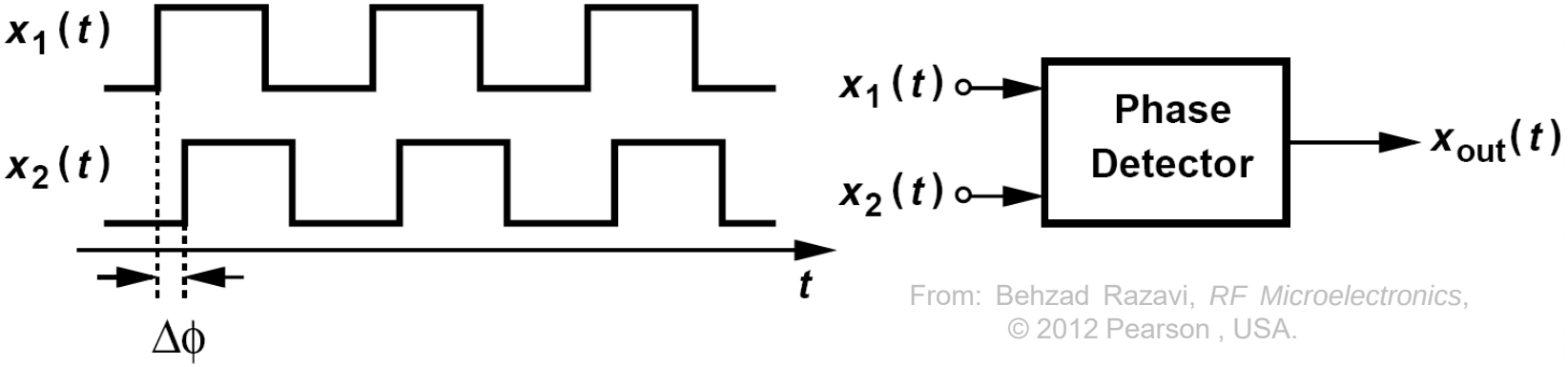
Phase Detector

(detecting phase difference)

- A **phase detector** is a circuit that senses two periodic inputs and produces an output which has an average value proportional to the difference between the **phases** of the inputs.



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  - The input/output characteristic of the PD is ideally a straight line, with its slope called the "gain" and denoted by K_{PD}.

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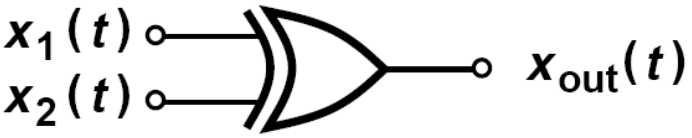
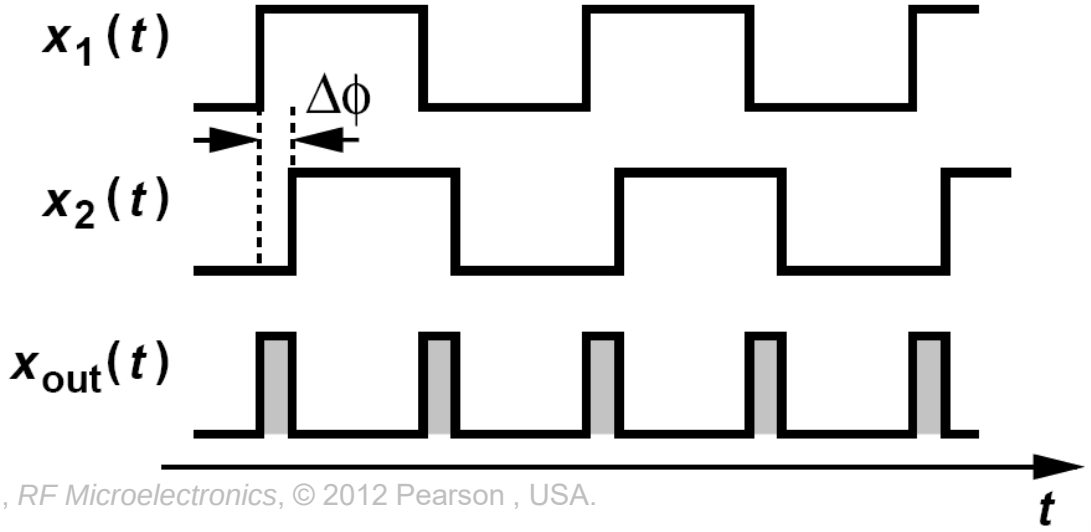
Phase Detector

(implementation using XOR gate)

- An **exclusive-OR** (**XOR**) gate can serve this purpose of phase difference detection. It generates pulses which have the pulse width equal to $\Delta\phi$.





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$$F = A \oplus B$$

A	B	F
0	0	0
0	**1**	**1**
1	**0**	**1**
1	1	0

- An **XOR gate** outputs a logic "1" only when the two inputs are *different*.

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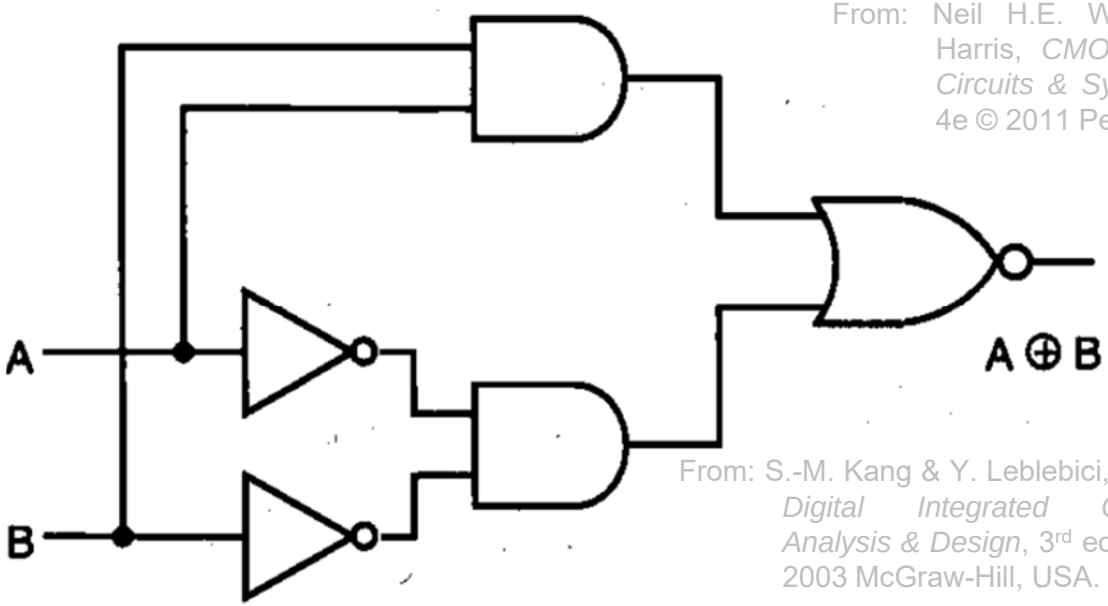
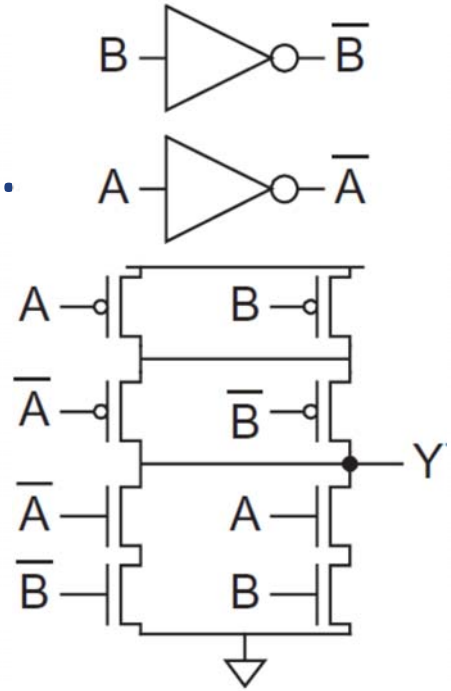
Implementation of XOR Gate

(5 logic gates & 12 MOSFETs)

- Based on the truth table and Boolean algebra, the **XOR** gate can be implemented using the fundamental logic gates: $F = A \oplus B = A'B + AB'$
- The XOR gate can be implemented by 12 CMOS transistors (4 for two inverters).



From: Neil H.E. Weste & David M. Harris, *CMOS VLSI Design: A Circuits & Systems Perspective*, 4e © 2011 Pearson , USA.



From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.

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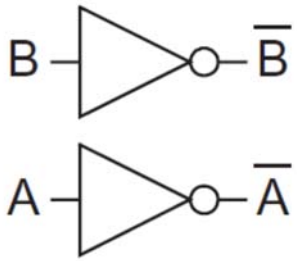
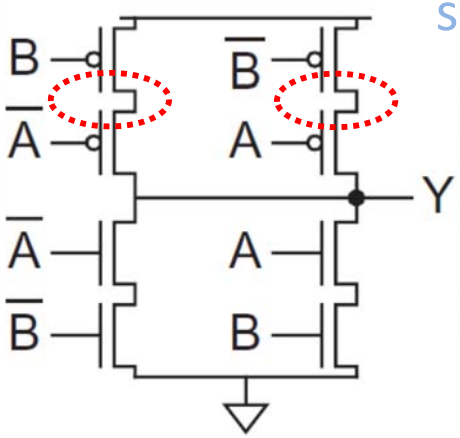
Implementation of XOR Gate

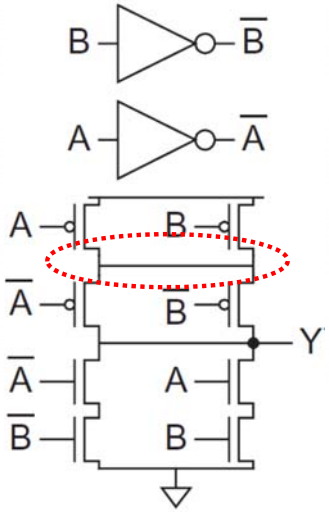
(transmission gate approach using 10 MOSFETs)

- There can be improvement in the CMOS implementation of the **XOR** gate to make it more ***compact*** (i.e. smaller size):
  - modified interconnections of MOSFETs for slightly more area-efficient physical layout.
  - design with two transmission gates





save contacts at two S/D regions



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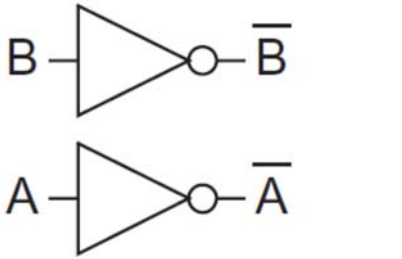

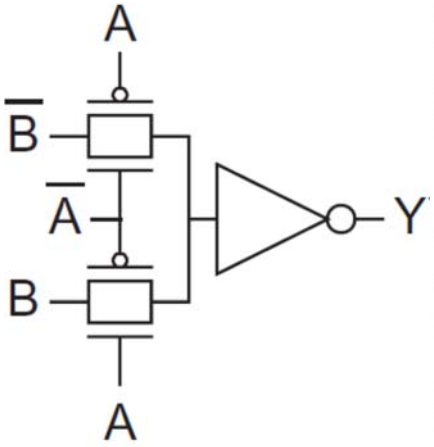

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Simple Phase Locked Loop

(dynamic negative feedback control)

- As the output of the **phase detector** (PD) is proportional to the the **phase difference** $\Delta\phi$, it is fed to the input of the VCO to vary the frequency so that the VCO output will have zero $\Delta\phi$ through dynamic **feedback control**.

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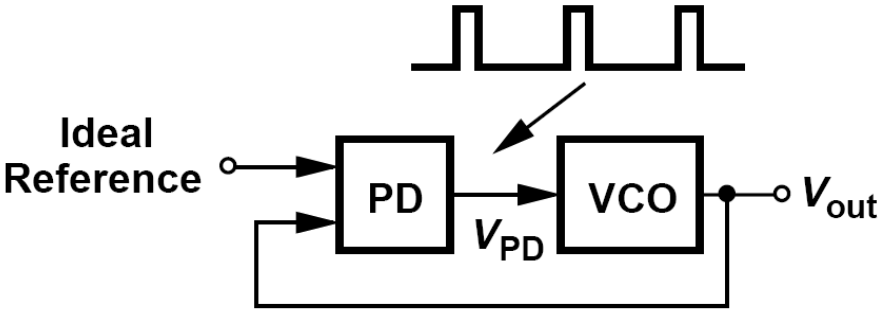

  - When $\Delta\phi$ is large, the VCO will be driven accordingly to vary the frequency in such a way to minimise $\Delta\phi$.
  - When $\Delta\phi \approx 0$, the input voltage of the VCO is fixed and the frequency of the VCO output remains constant.
  - It is a **negative feedback system**.

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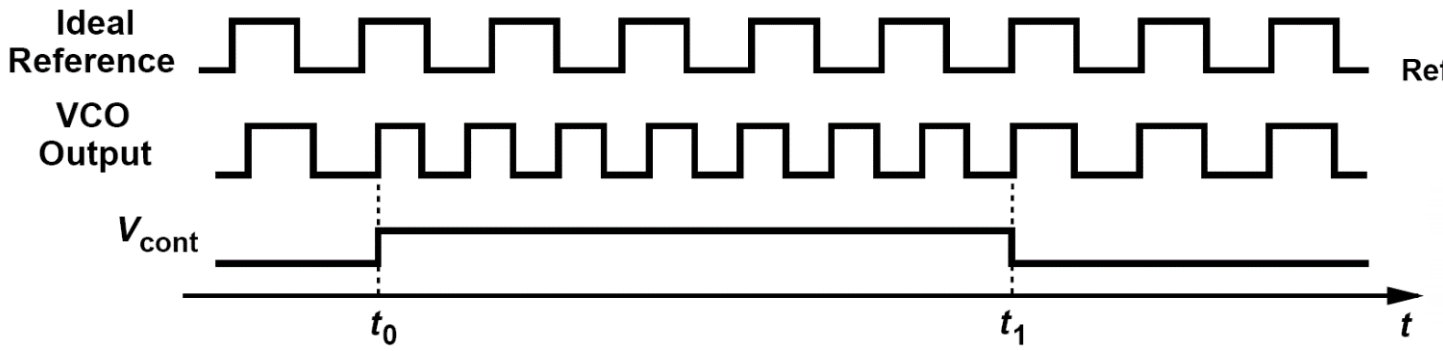
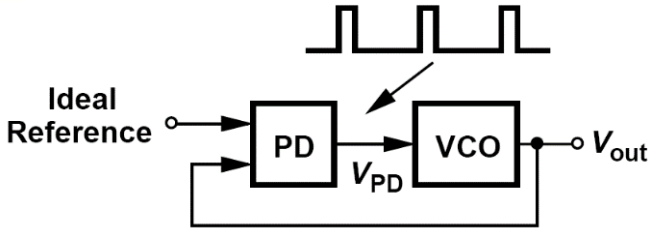
Simple Phase Locked Loop

(phase locking)





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- The **phase locking** in the simple PLL through ***dynamic* negative feedback control** can be illustrated by trying to align the output phase of the VCO output with that of a reference clock.
  - At t_0, the VCO output frequency increases with a larger V_{cont} and gradually decreases the phase error.
  - At t_1, the phase alignment is achieved and the VCO frequency stops increasing with V_{cont} returned to its original value.

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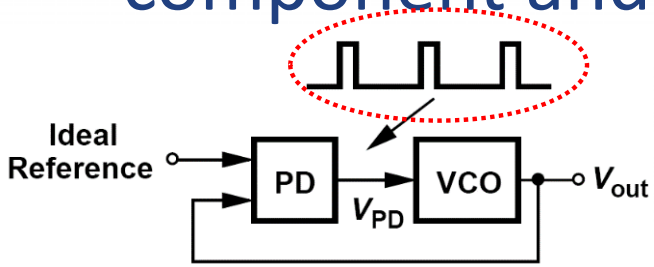
Problem of Simple PLL

(sidebands at the output)

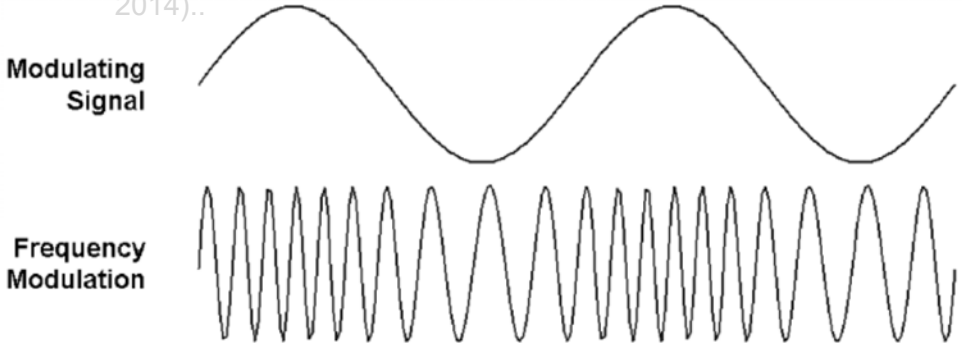
- In the simple PLL, the PD produces ***repetitive*** **pulses** at its output. Such a signal consists of a DC component and a high frequency component.

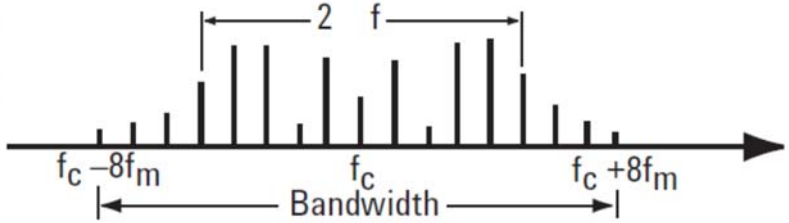


From: Behzad Razavi, *RF Microelectronics*, © 2012 Pearson , USA.

- The latter is undesirable because it ***modulates*** the VCO frequency and hence generate large **sidebands**.
- This is a situation of **frequency modulation** (FM).

From: "*Spectrum Analysis Amplitude and Frequency Modulation*," Keysight Technologies Application Note (July 31, 2014)..





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Basic PLL Topology

(with low-pass filter)

- To resolve the problem of the **sidebands** at the VCO output, the high frequency component of the PD output can be *filtered*.
- A **low-pass filter** is placed between the PD and the VCO to suppress the ***repetitive* pulses**.

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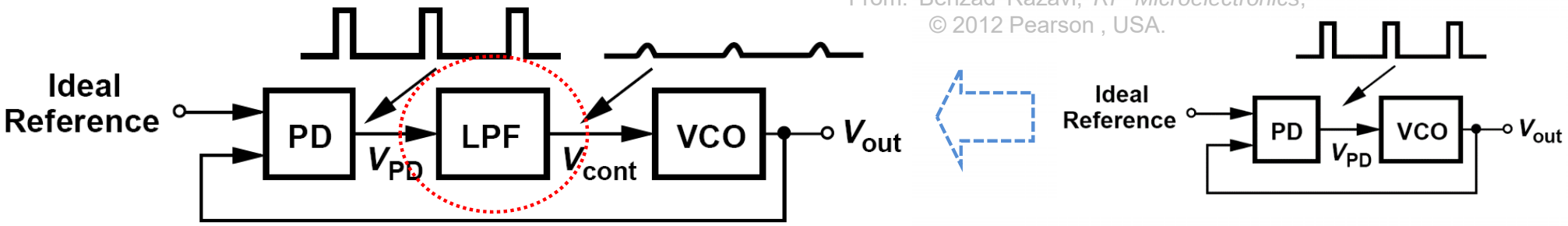

- This forms the basic PLL topology (called type I PLL).
  - 3 essential constituent blocks:
    PD, LPF and VCO in a feedback loop.

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Phase Locked Loop

(simple implementation)

- A simple PLL can be implemented with an XOR gate, a *first-order* RC low-pass filter and a **cross-coupled LC oscillator**.

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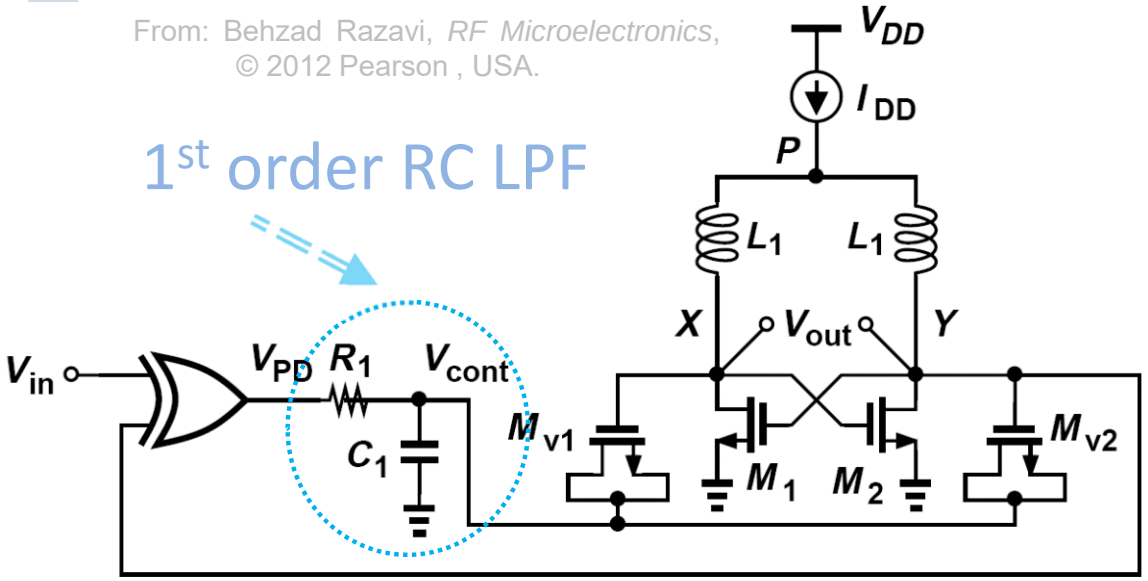

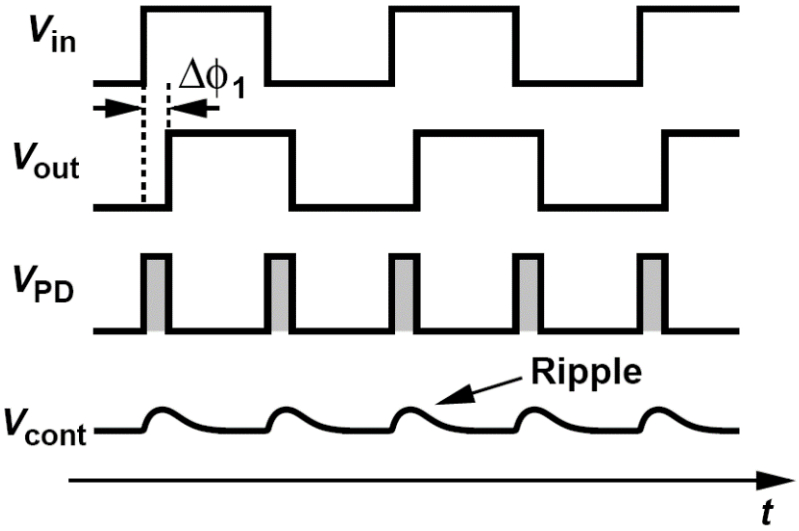

- Note the differential output (at nodes *X* and *Y*) with the cross-coupled LC oscillator.

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Phase Locking in PLL

(voltage follower analogy)

- We say a **PLL** is an electronic circuit that ***locks*** the **phase** of the output to that of the input.
  - To illustrate the **phase locking** concept, the voltage follower analogy can be used.
  - In the voltage follower configuration, if the op amp has a large enough voltage gain, the output voltage "***tracks***" the input voltage closely.

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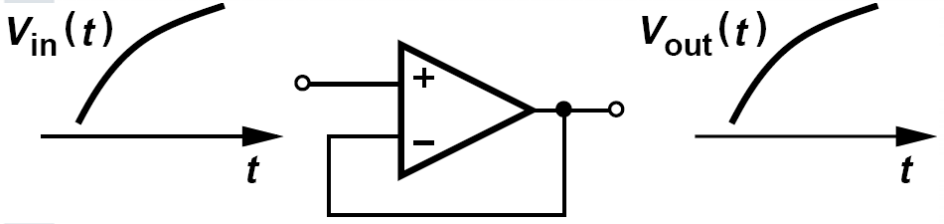

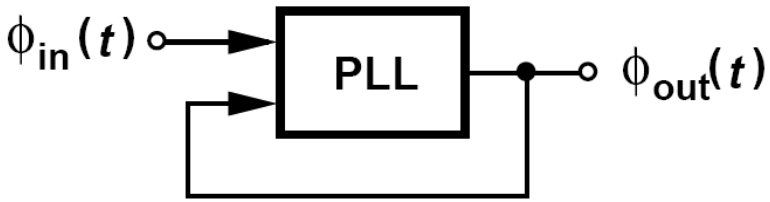

- Similarly, a PLL ensures that $\phi_{out}(t)$ tracks $\phi_{in}(t)$, in other words, the output ***locked*** to the input in the **phase** domain.

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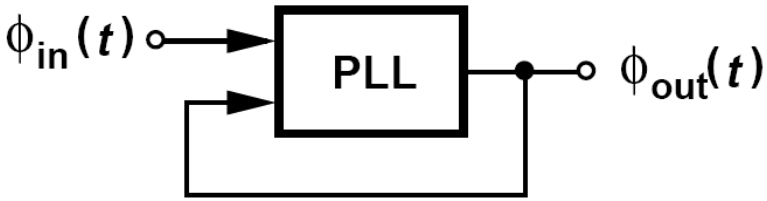
Phase Locking in PLL

(exactly equal frequencies)

- We say the loop is "locked" if $\phi_{out}(t)$ - $\phi_{in}(t)$ is constant with time $\Rightarrow$ the output is ***synchronised*** with the input.



- When **phase locking** is achieved, there is an important and unique consequence - the input and output frequencies of the PLL are *precisely* equal.

$$\phi_{out}(t) - \phi_{in}(t) = \text{constant}$$

$$\frac{d\phi_{out}}{dt} - \frac{d\phi_{in}}{dt} = 0 \Rightarrow \frac{d\phi_{out}}{dt} = \frac{d\phi_{in}}{dt} \Rightarrow \omega_{out} = \omega_{in}$$

  - This attribute is critical in using PLLs for frequency synthesis.

  - In a stand-alone VCO, $\omega_{out} = \omega_{in} + K_{VCO}V_{cont}$

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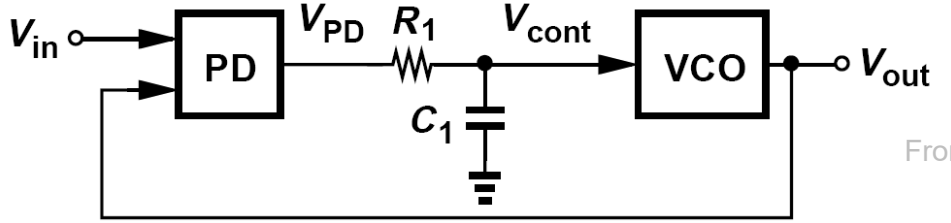
Phase Locked Loop

(transient response in V_{cont})



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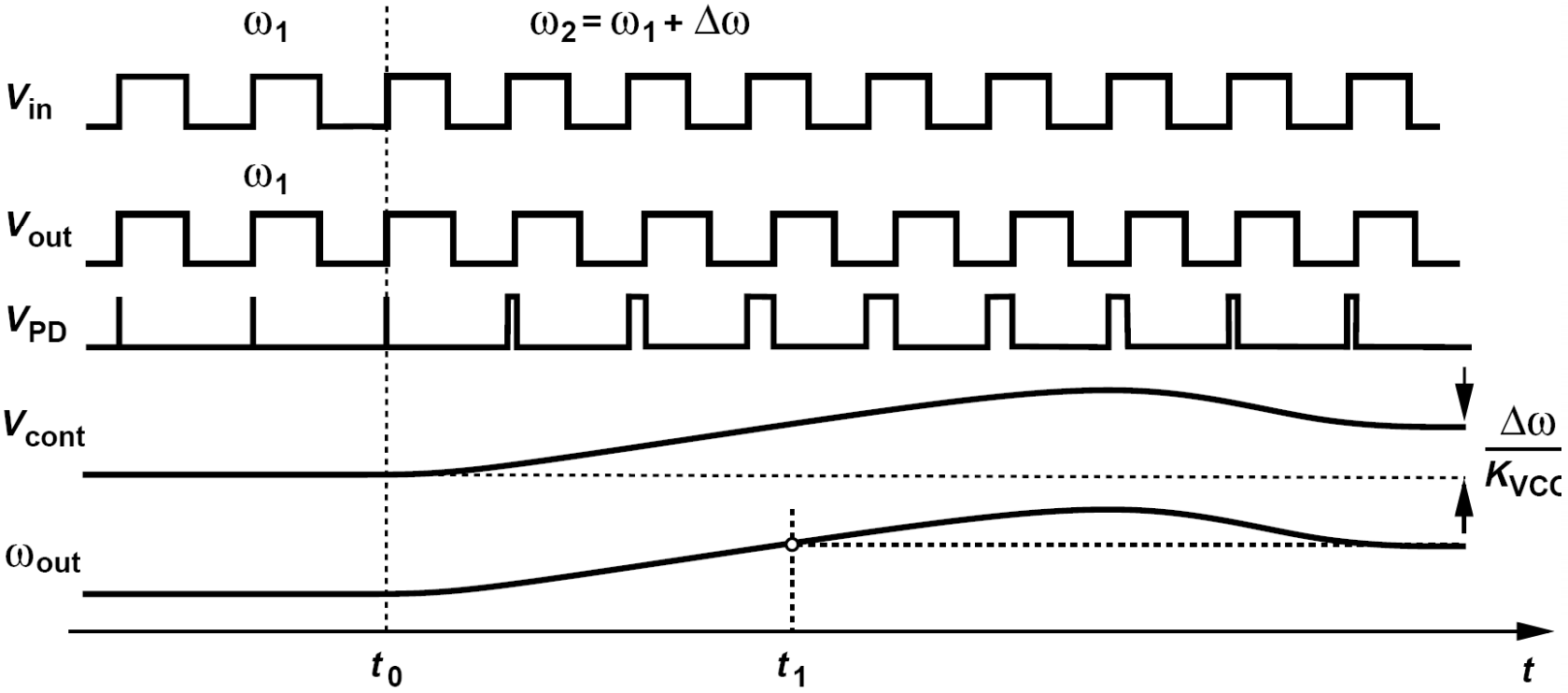

- V_{cont} reveals more the transient behaviour of the PLL.

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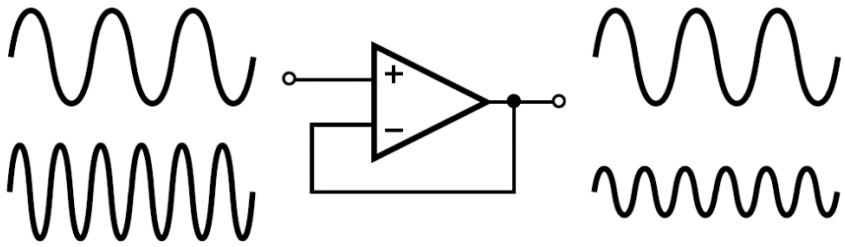
Phase Locked Loop

(transient response)

- The ***transient* response** of PLLs is generally a nonlinear phenomenon. (Do you know why?)
- It can be viewed with the voltage follower analogy.

slow input sinusoid

fast input sinusoid



little attenuation

much attenuated sinusoidal output

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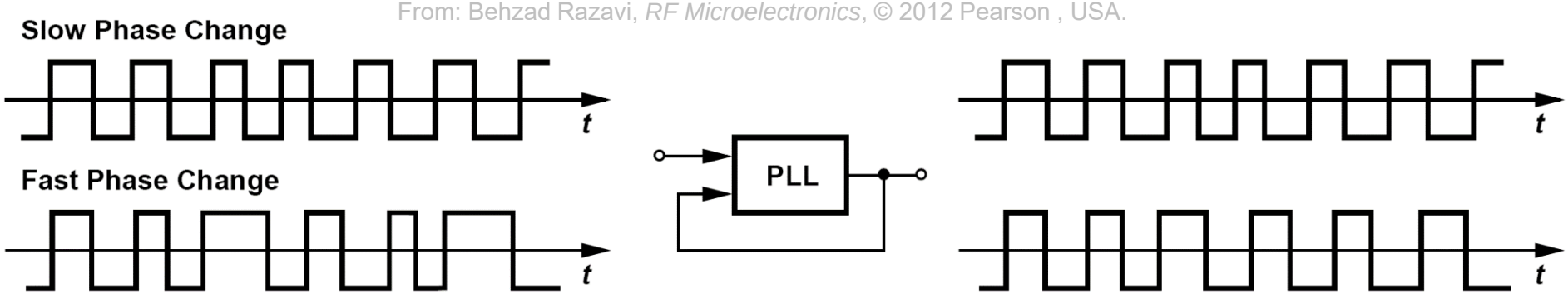

- How about a PLL's response to varying phase change?

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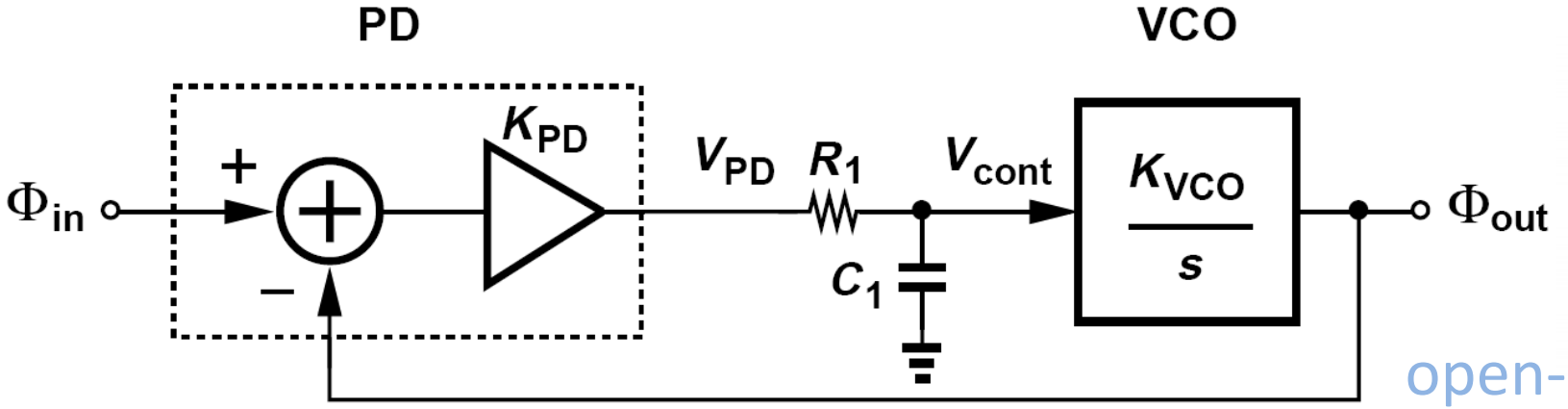
Loop Dynamics

(phase domain)

- A "**phase**-domain model" can be constructed for studying PLLs' transient response using a linear approximation.



From: Behzad Razavi, *RF Microelectronics*, © 2012 Pearson , USA.

open-loop transfer function

$$\frac{K_{PD}}{(R_1C_1s+1)}\left(\frac{K_{VCO}}{s}\right)$$

- The *closed-loop* **transfer function**:

$$H(s)=\frac{\Phi_{out}(s)}{\Phi_{in}(s)}=\frac{K_{PD}K_{VCO}}{R_1C_1s^2+s+K_{PD}K_{VCO}}$$

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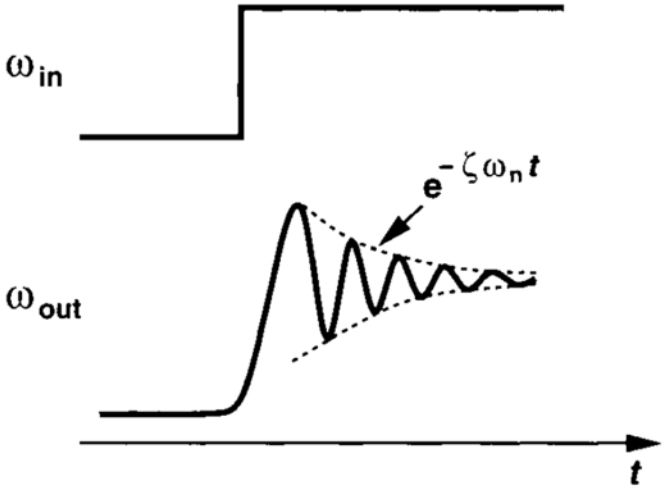
Loop Dynamics

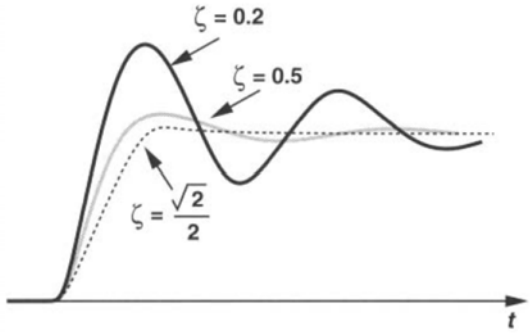
(transient responses in time domain)

- Based on the ***closed-loop*** **transfer function**, it can be seen that the PLL is a second-order feedback system.

$$H(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

- A system with a second-order transfer function can have the following transient responses:





- overdamped
- critically damped
- under-damped

depending on the damping factor

$$\omega_n = \sqrt{K_{PD}K_{VCO}\omega_{LPF}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$$

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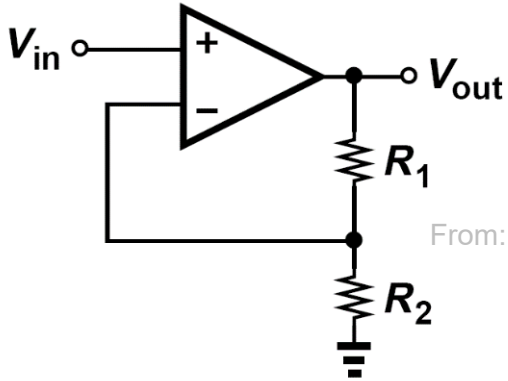
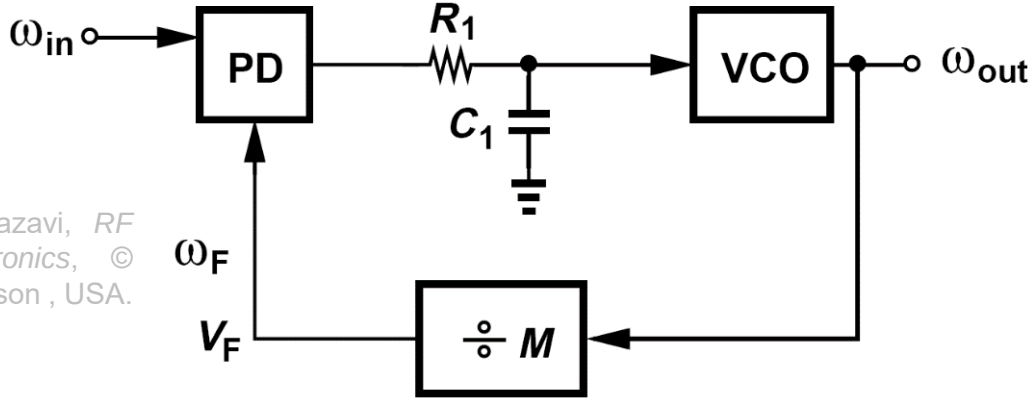
PLL for Frequency Multiplication

(divided output fed back to input)

- A PLL can be configured to generate an output frequency which is a **multiple** of the input frequency.
  - This is done by ***dividing*** the output frequency of the PLL and then feeding back to the input.
  - The analogy is the non-inverting amplifier.





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- The $\div M$ circuit is a **counter** that generates one output pulse for every M input pulses.
  - The divide ratio, M, is called the "modulus".

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Limitations of Type I PLL

(unequal input frequencies)

- The type I PLL is rarely used for making modern frequency synthesizers for modern communication systems.
  - It suffers from a limited "**acquisition range**". If the VCO frequency and the input frequency are very different at the startup, the type I PLLs may never achieve "**phase locking**"
  - The limitation is because **phase detectors** produce little information if sensing inputs of *unequal* frequencies.
- A **frequency detection** function needs to be added to the phase detector in the PLL.

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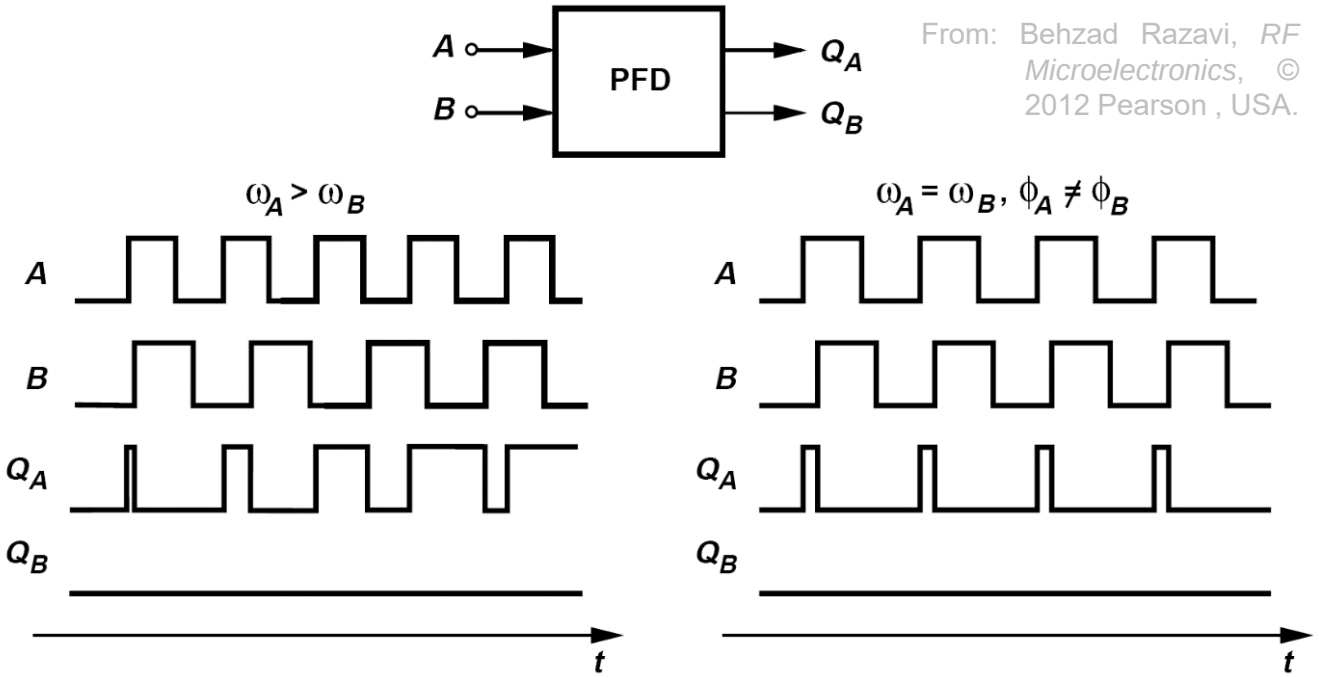
Phase/Frequency Detection

(sensing both phase & frequency difference)

- A phase/frequency detector has two outputs Q_A and Q_B, sensing both the phase and frequency of the two inputs ***A*** and ***B***.
  - Sequential logic (vs. XOR as combinational logic) is used.



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- Q_A outputs pulses whose width is proportional $\phi_A - \phi_B$ while $Q_B = 0$.
- If ***A*** has a lower frequency than ***B***, Q_B outputs pulses.

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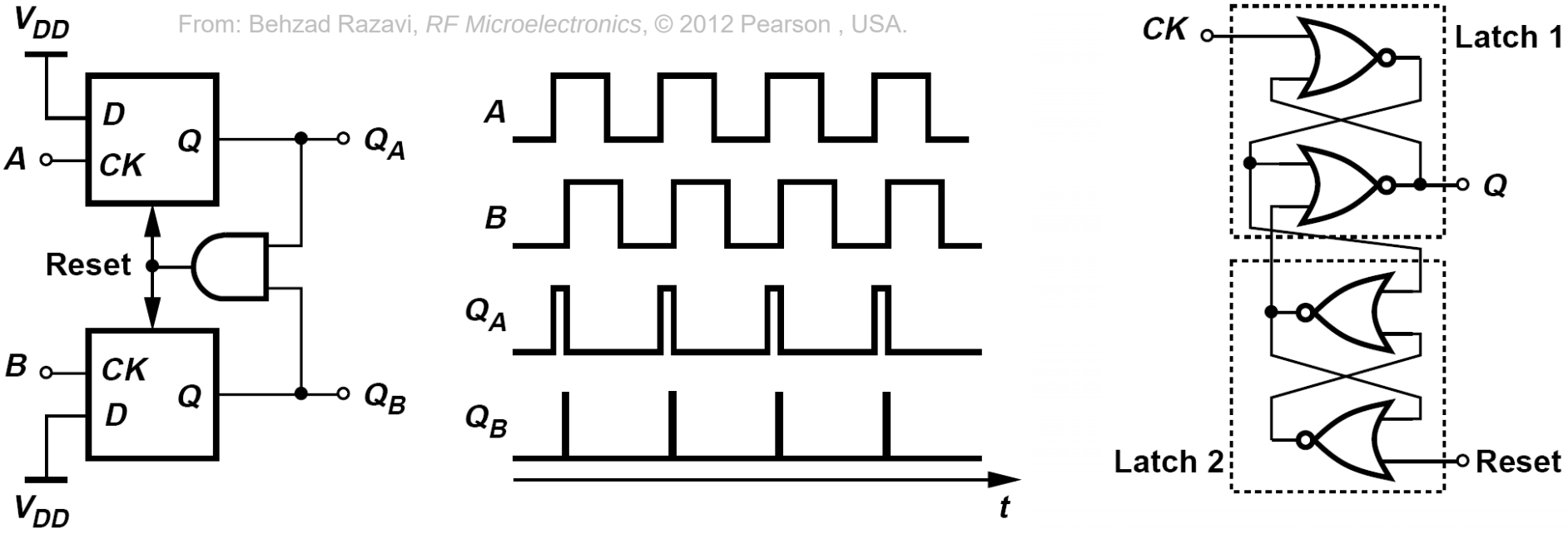
Phase/Frequency Detector

(D-flipflop implementation)

- The **phase/frequency detector** (PFD) can be realised using two **D-flipflops** and one AND logic gate.
  - Signals ***A*** & ***B*** are inputted as the clocks of the D-flipflops.



- The D-flipflop can be implemented using four cross-coupled NOR gates.

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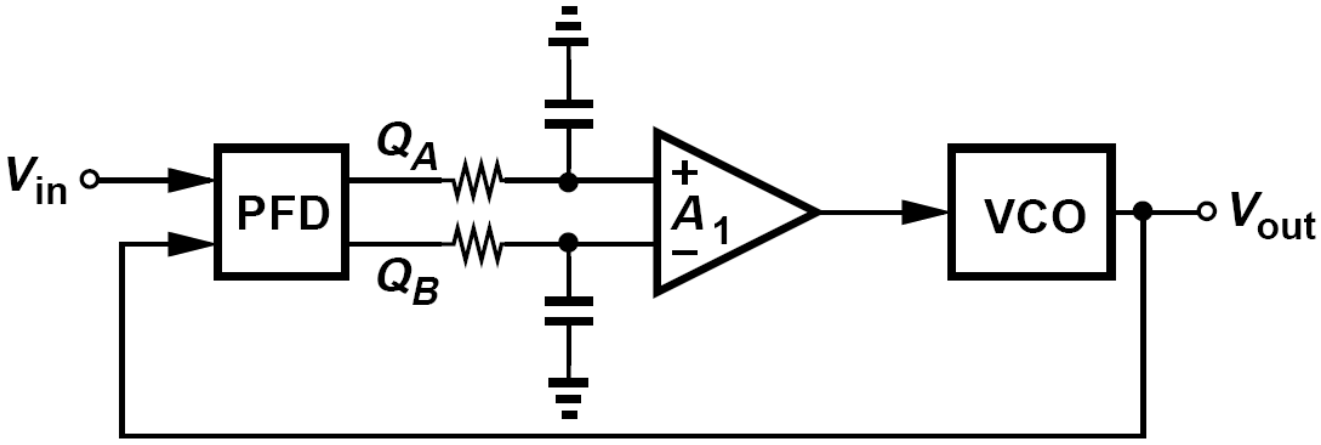
Improved Type I PLL

(with phase/frequency detector)

- Using a phase/frequency detector (PFD), the design of the type I PLL can be improved to resolve issue of the limited **acquisition range**.
  - The PFD has two outputs, Q_A and Q_B. A differential amplifier can be used to extract the DC component of (Q_A - Q_B) with two low-pass filters.



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  - Note the polarity of Q_A and Q_B fed to the differential inputs of the amplifier.

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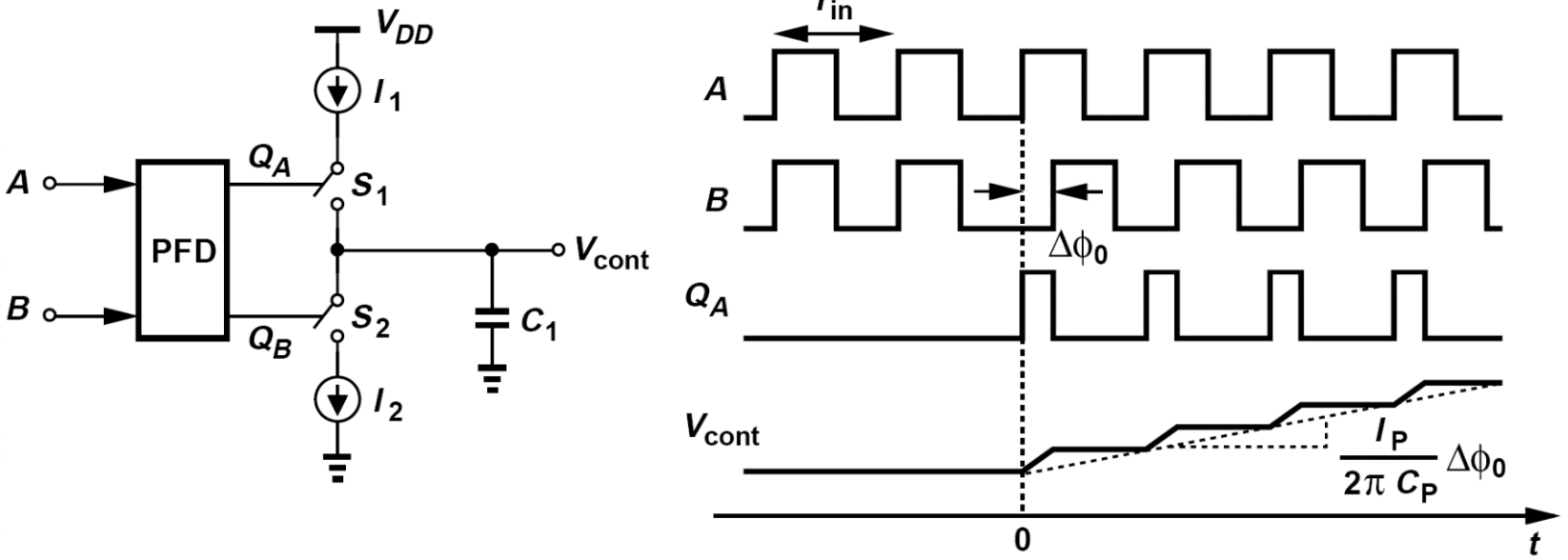
Charge Pump

(switched current sources)

- The more common approach to process the two outputs Q_A and Q_B using a **charge pump** interposed between the PFD and VCO in the PLL.



  - A charge pump consists of two ***switched*** **current sources** that ***pump*** **charge** into or out of the loop filter according to the inputs.

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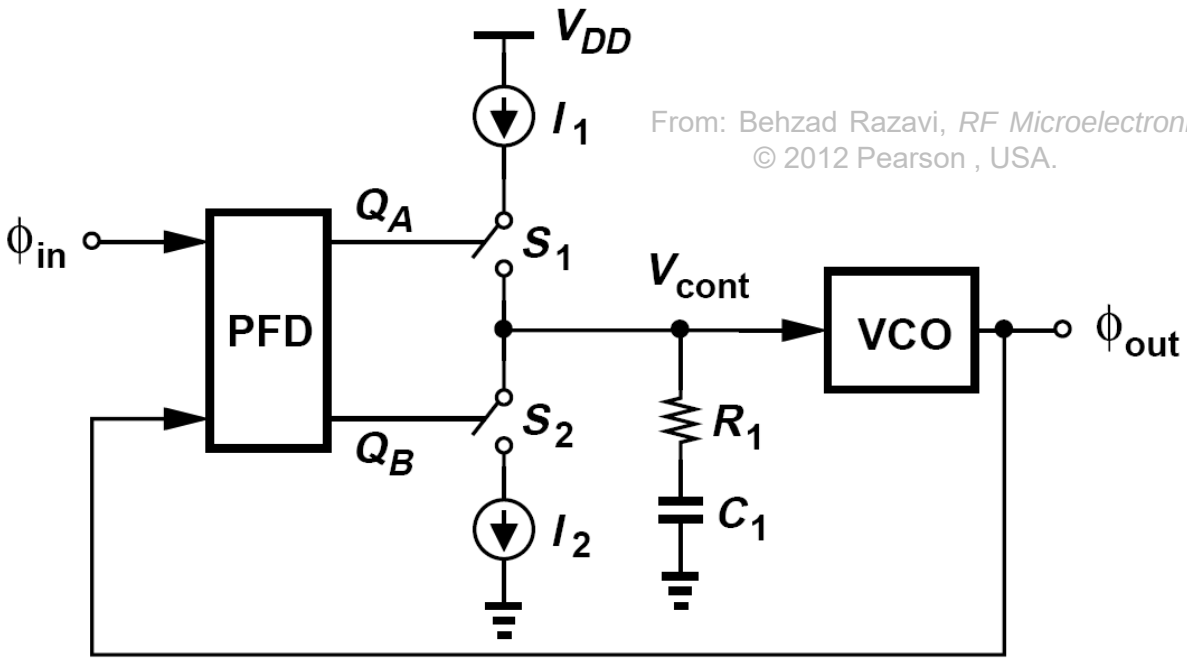
Charge-Pump PLL

(added resistor for better stability)

- Skipping analysis of the loop dynamics, a better design of PLLs using a **charge pump** is obtained with an added resistor R_1 in series with the capacitor C_1. This is called the **charge-pump PLL**.



- This is a type II PLL used to build frequency synthesizers.

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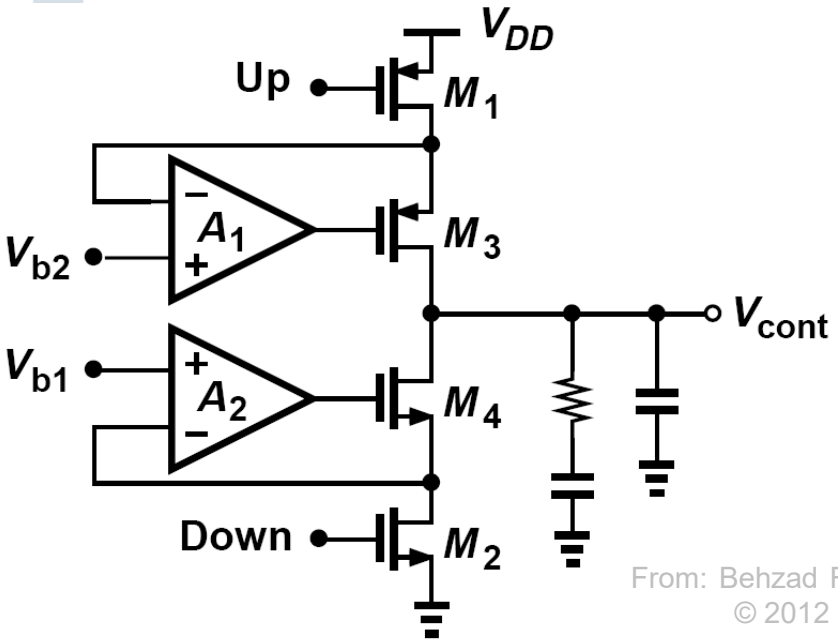
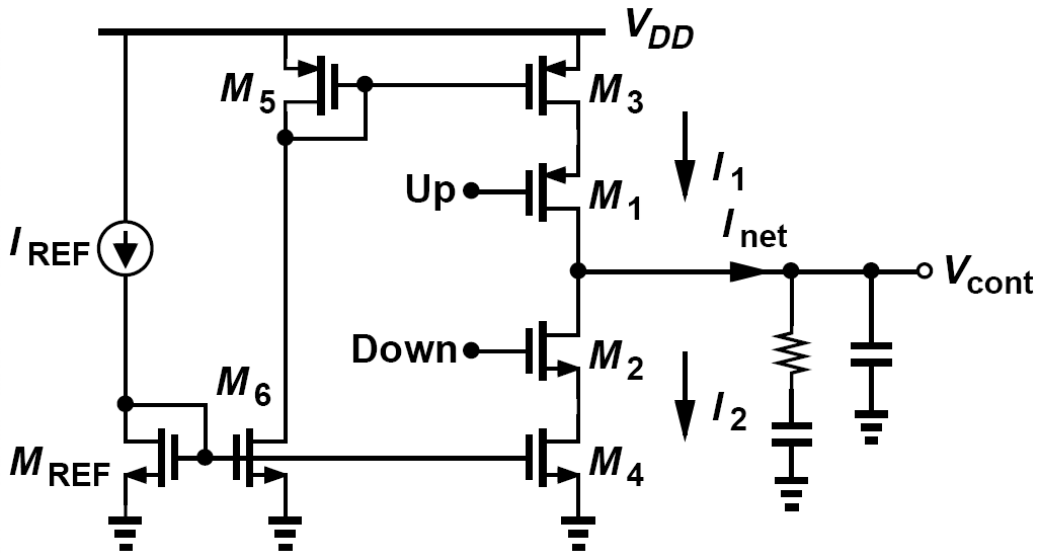
Charge Pump CMOS Circuit

(implementation of switched current sources)

- The **charge pump** can be realised using MOS transistors as switches and to configure current mirrors.





- The design can be improved by suppressing the channel-length modulation.

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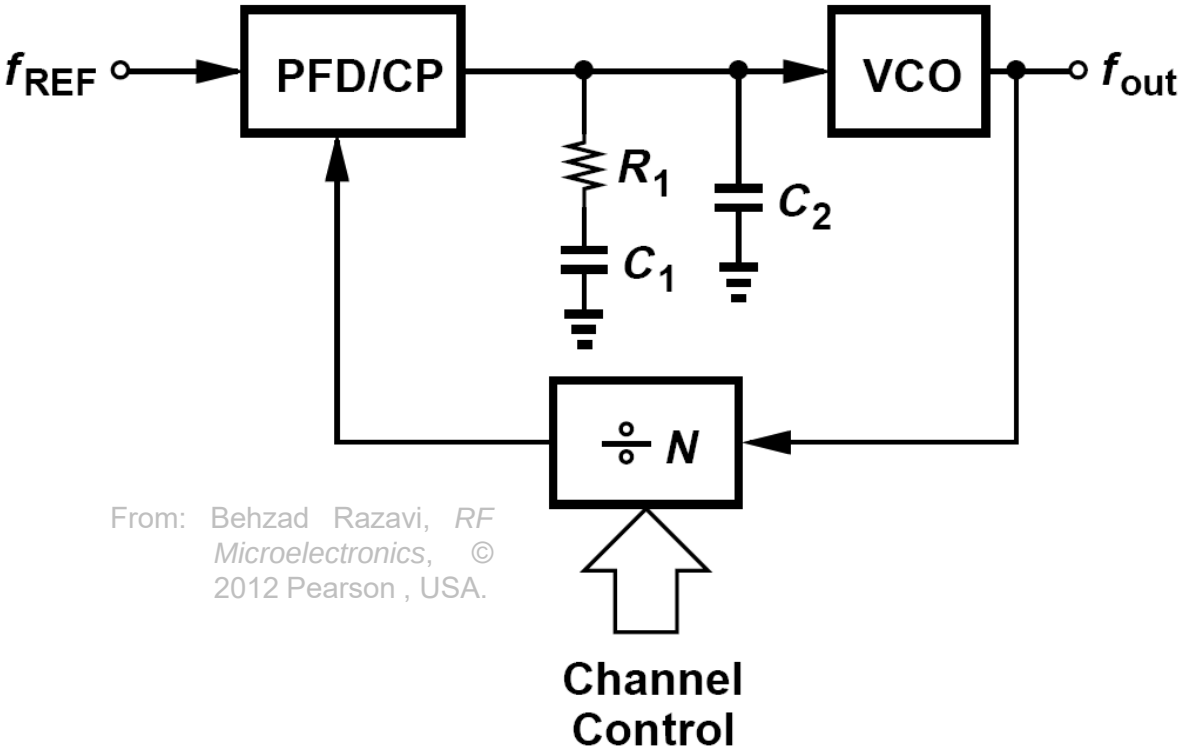
Frequency Synthesizer

(integer-*N*)

- With the phase/frequency detector and the **charge pump** designs, a **PLL** can be configured to become a frequency synthesizer.



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- An integer-*N* **frequency synthesizer** produces an output frequency that is an **integer multiple** of the reference frequency.
- This is frequency multiplication.

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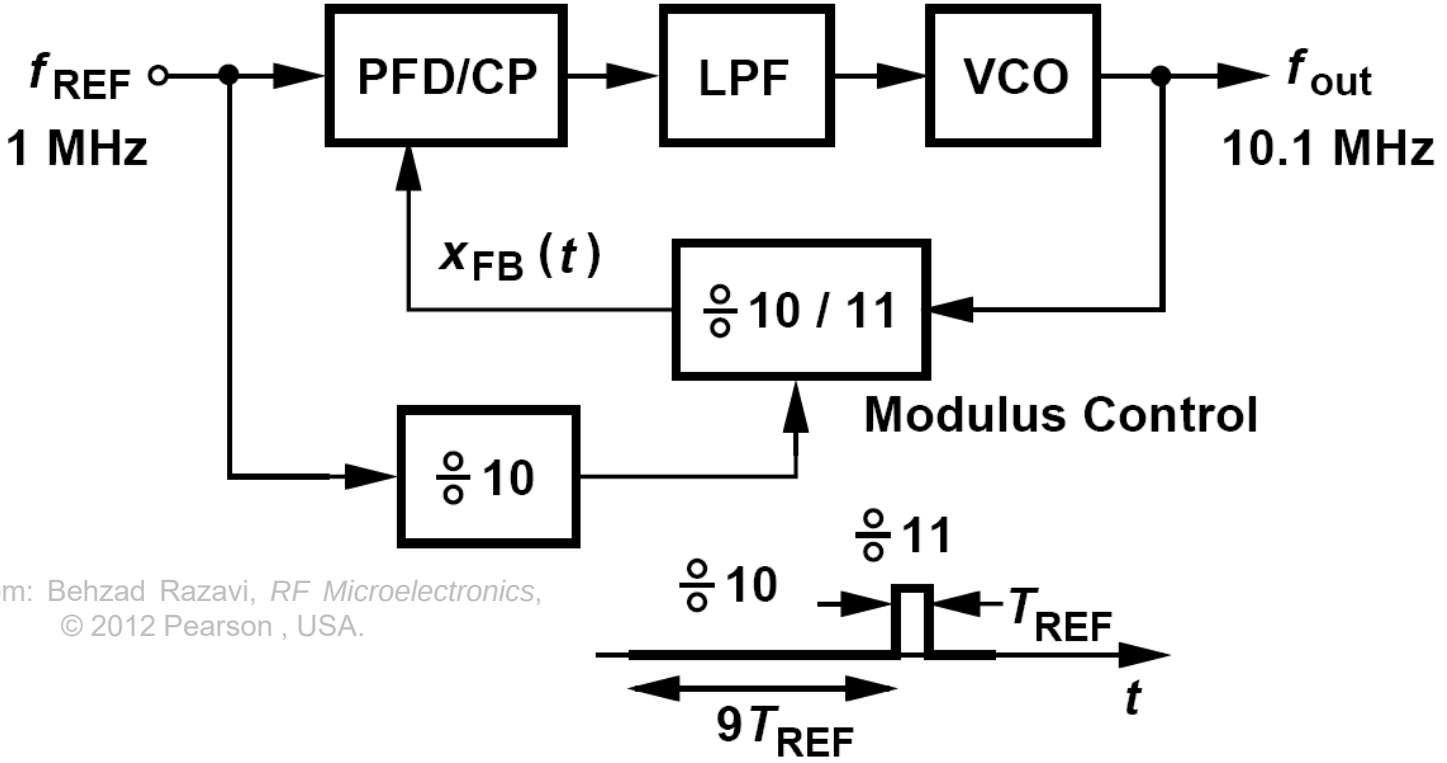
Frequency Synthesizer

(fractional-*N*)

- The integer-*N* **frequency synthesizer** can be revamped to a fractional-*N* **frequency synthesizer**.



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