Lecture 3

of

EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Thursday, 27th September 2018

- **Silicon p-n junction**
  - physical structure
  - electrostatics
  - I-V characteristics & capacitance
  - **physical layout**

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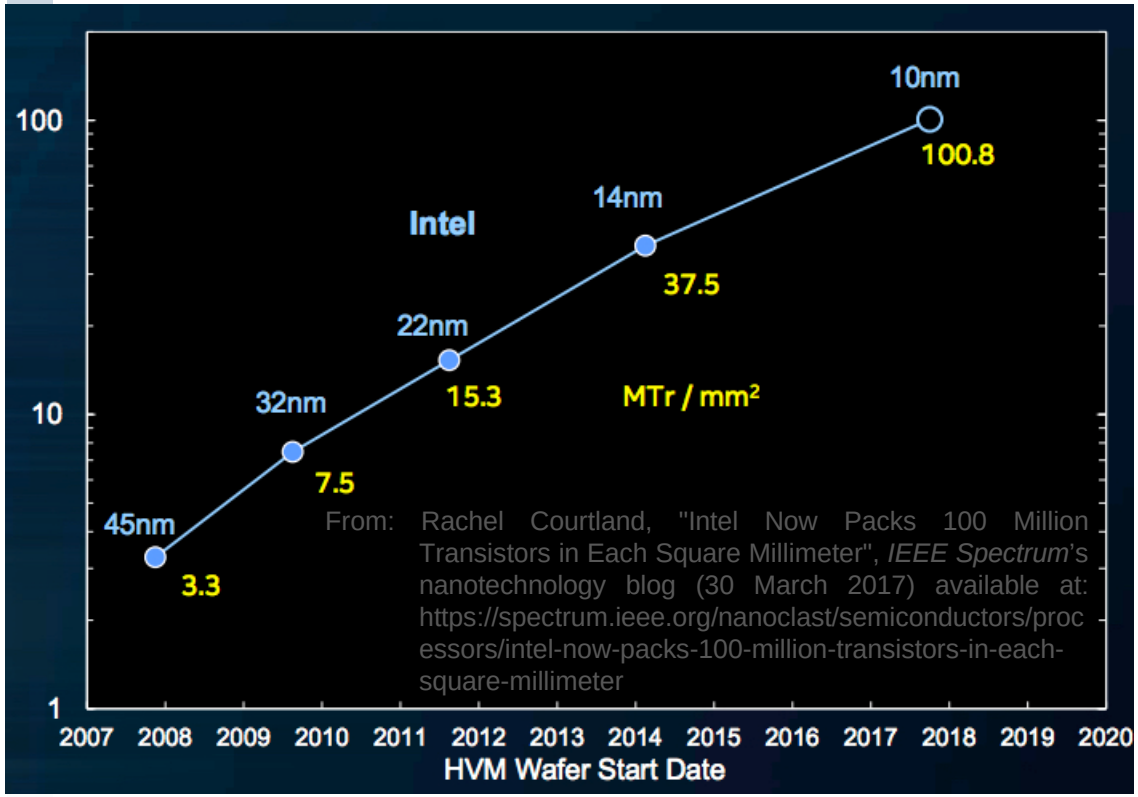
Silicon CMOS Digital ICs

(billions of transistors)

- In modern digital ICs, a massive number of transistors are packed in a small chip area.



- In 2018, an Intel microprocessor (e.g. Core i7) contains multi-billion transistors.
- 101 million transistors per mm^2 in the 10-nm technology node.

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Silicon CMOS Digital ICs

(building blocks for complex construction)

- One can imagine the huge complexity of digital ICs constructed with billions of transistors.
- No matter how complex the digital IC are, they are still constructed using the fundamental building blocks, namely silicon semiconductor devices.
  - At the physical layout design level, the major building block is the MOS transistor, with interconnect wires also being essential in connecting different MOS transistors to form complex circuits.
  - A basic understanding of the underlying building blocks is needed before complex construction.
  - Start from basics in engineering.

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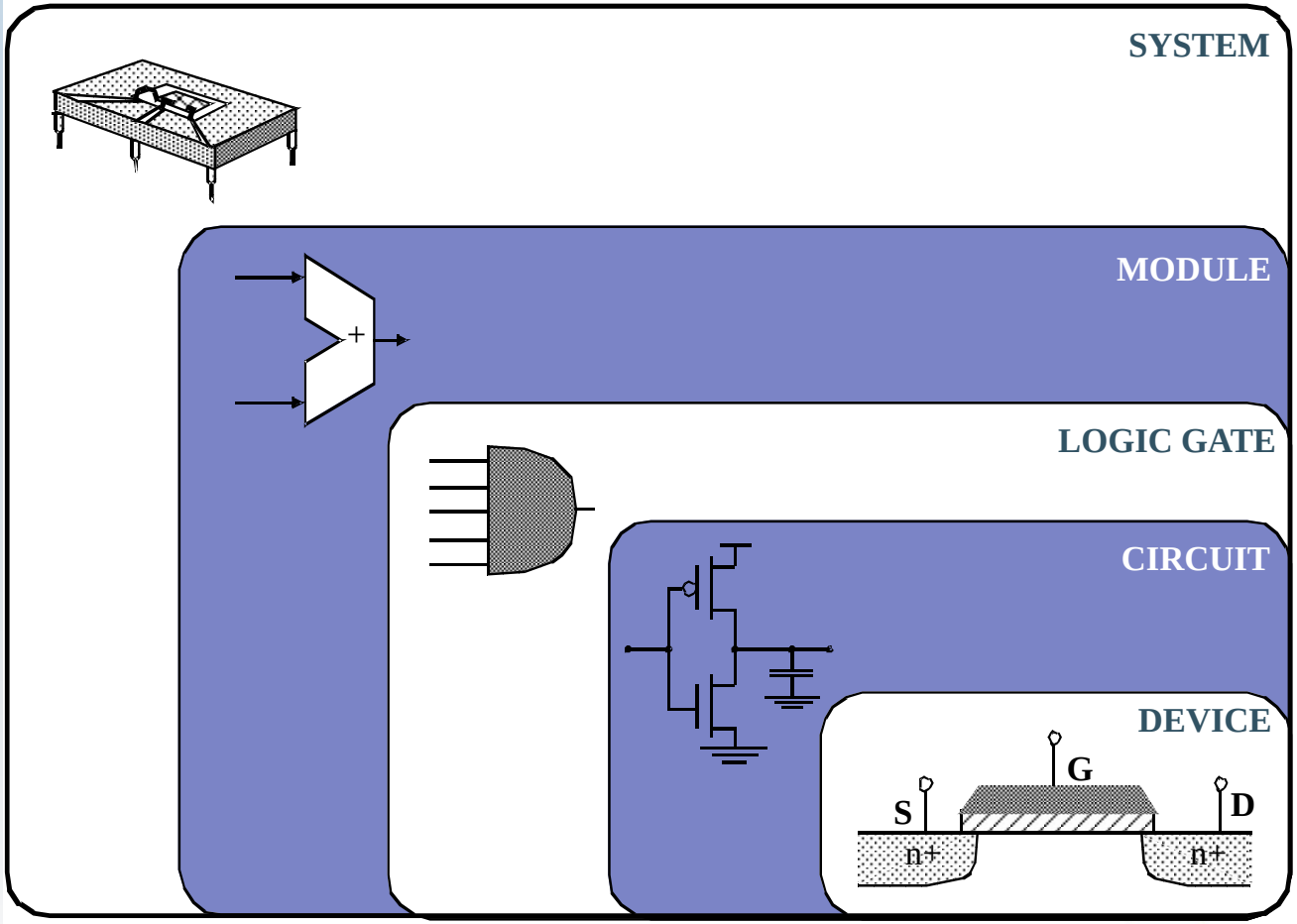
Silicon CMOS Digital ICs

(from MOS transistor to complex construction)



- Silicon CMOS digital ICs of whatever complexity start from the **MOS transistor** for their construct-ion.

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Silicon *p-n* Junction

(*p-n* junction & MOS transistor)

- The MOS transistor itself is composed of two fundamental structures in semiconductor electronics, namely the ***p-n* junction** and the **MOS capacitor**.
- The ***p-n* junction** is essentially a diode from the circuit point of view.
  - A diode allows current to flow in only one direction.
- The ***p-n* junction** as a diode is not explicitly used in the silicon CMOS digital ICs (except in the I/O ports' electrostatic discharge protection).
  - It is everywhere in a silicon CMOS IC.

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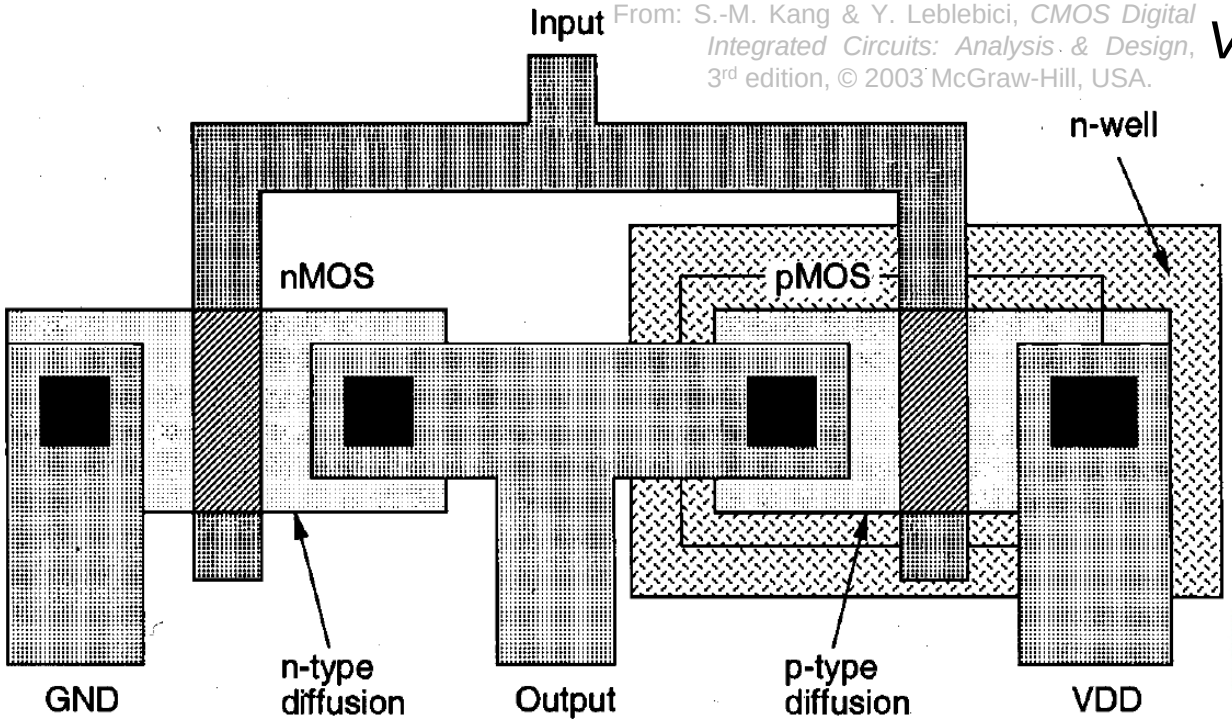
Silicon *p-n* Junction

(existence in digital IC)

- Two MOS transistors (nMOS and pMOS) are used to construct the fundamental logic gate, inverter.
  - Do you see where the ***p-n* junctions** are in the circuit?



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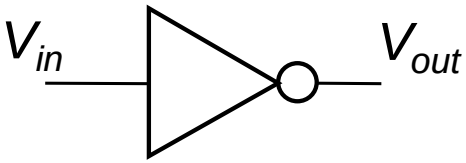

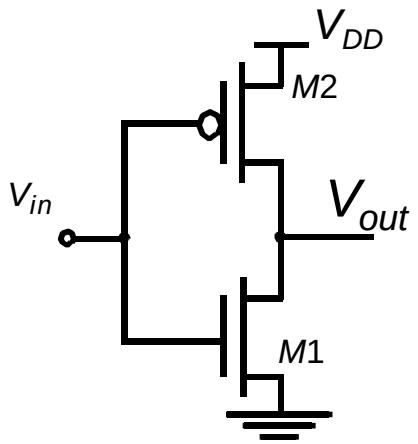

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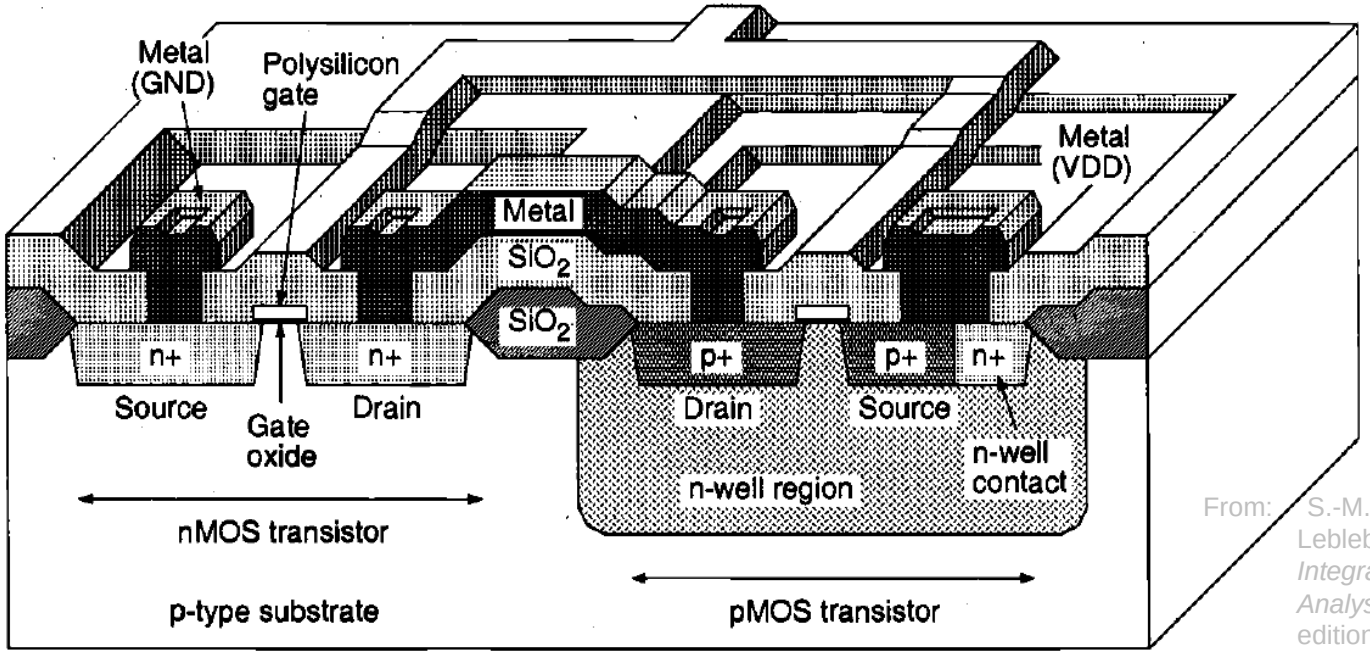
Silicon *p-n* Junction

(existence parasitic diode)

- The existence of the ***p-n* junction** is more obvious when looking at the 3D cross-sectional structure.



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- It exists as parasitic diodes but usually reverse-biased.

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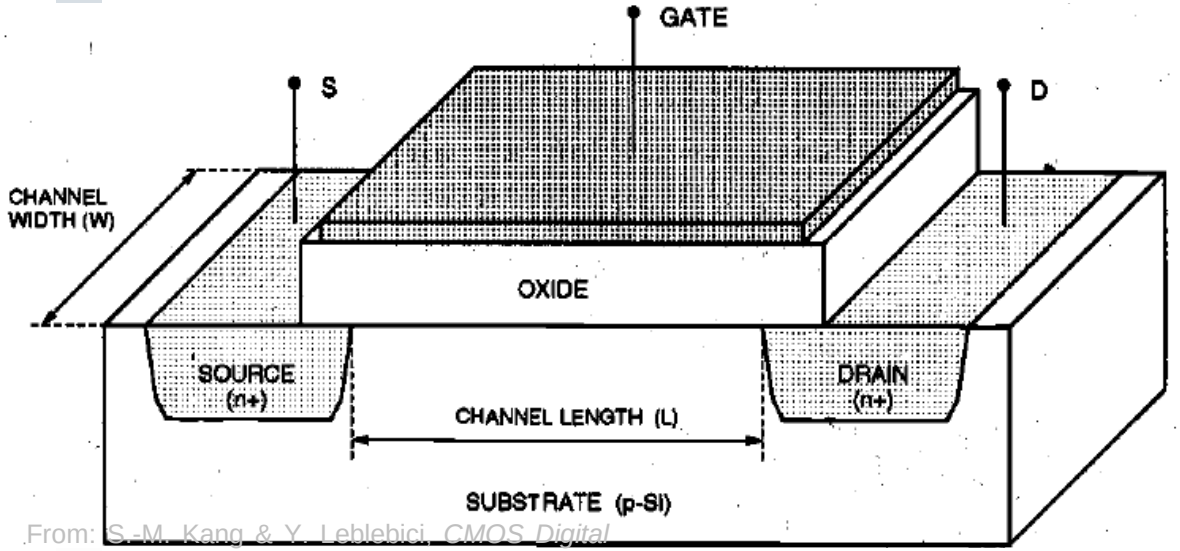
Silicon *p-n* Junction

(normally reverse-biased)

- The nMOS transistor (shown here) contains two ***p-n* junctions** which do not conduct current in the normal situation as they are reverse-biased.
- The ***p-n* junction** however can directly influence the behaviour of the device, not in the static case.



From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.

- The parasitic capacitance of the ***p-n* junction** affects the **switching speed** of the MOS circuits.

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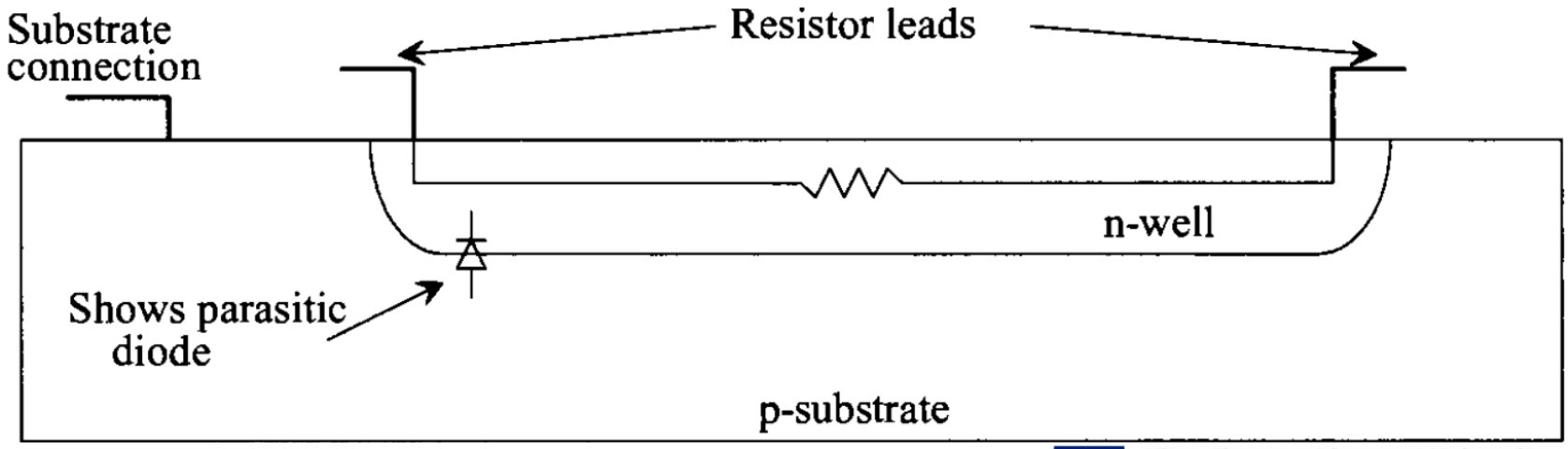
Silicon *p-n* Junction

(parasitic diode)

- In some mixed-signal ICs, integrated resistors may be used in the circuit design.
  - The implementation of an integrated resistor using an ***n***-well on a ***p***-substrate contains the ***p-n* junction** as a distributed parasitic diode.



From: R. Jacob Baker, CMOS: *Circuit Design, Layout, and Simulation*, 3e, © 2010 Wiley-IEEE Press, USA.

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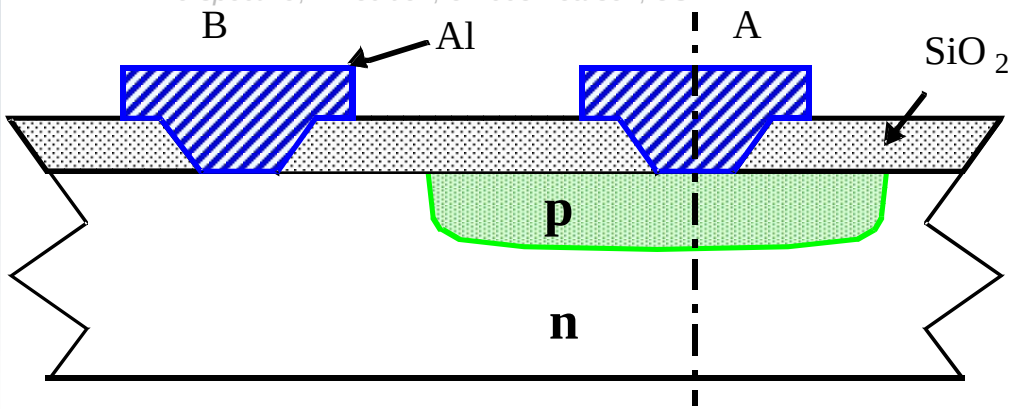
p-n Junction – CMOS implementation

(simplest semiconductor device)

- To help the physical layout design of CMOS digital ICs, it is good to know the basic properties and device equations of the ***p-n* junction** as a diode.
- As the simplest semiconductor device, the ***p-n* junction** diode is typically implemented as shown in the cross-sectional diagram here.

From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.



- The structure consists of a *p*-type region on an ***n***-type substrate or vice versa.

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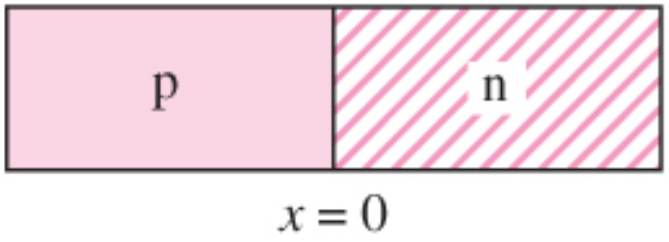
Silicon *p-n* Junction

(physical structure)

- For simplicity of explanations, the ***p-n* junction** diode is usually represented by a structure with a ***p***-type block next to an ***n***-type.



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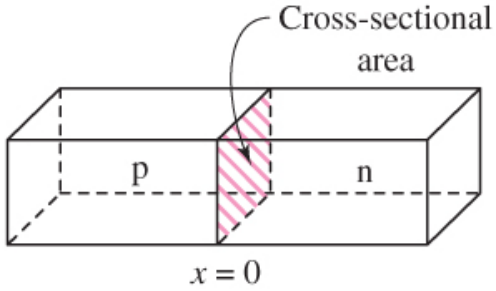

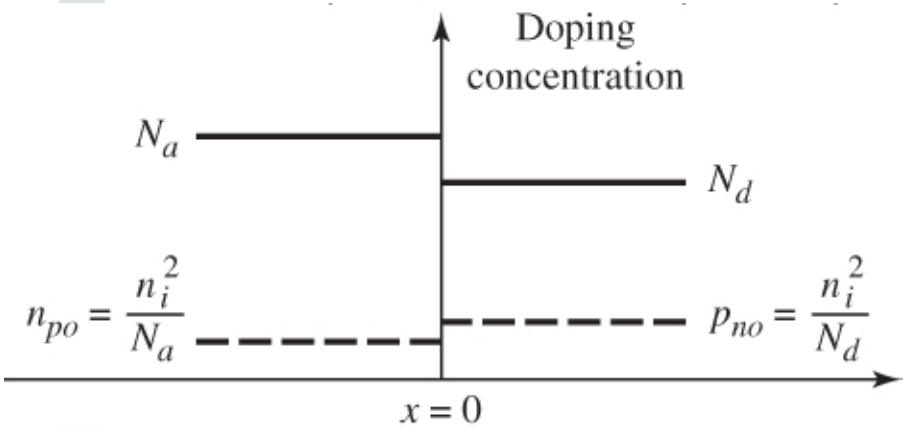

- The ***p***-region is doped with **acceptor impurities** (e.g. boron) of concentration N_a while the ***n***-region **donor impurities** (e.g. phosphorous or arsenic) of N_d.

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Silicon *p*-*n* Junction

(majority & minority carriers)

- In the ***p*-region**, there are plenty of **holes** as the **majority carriers**, with the hole concentration $p_p \approx N_a$ at room temperature.
  - The subscript ***p*** in p_p means that it is in the ***p*-region**.
- In the ***n*-region**, there are plenty of **electrons** as the **majority carriers**, with the electron concentration $n_n \approx N_d$ at room temperature.
  - The subscript ***n*** in n_n means that it is in the ***n*-region**.
- The **minority carrier** concentrations are respectively n_p (electron concentration) in the ***p*-region** and p_n (hole concentration) in the ***n*-region**.
  - mass action law

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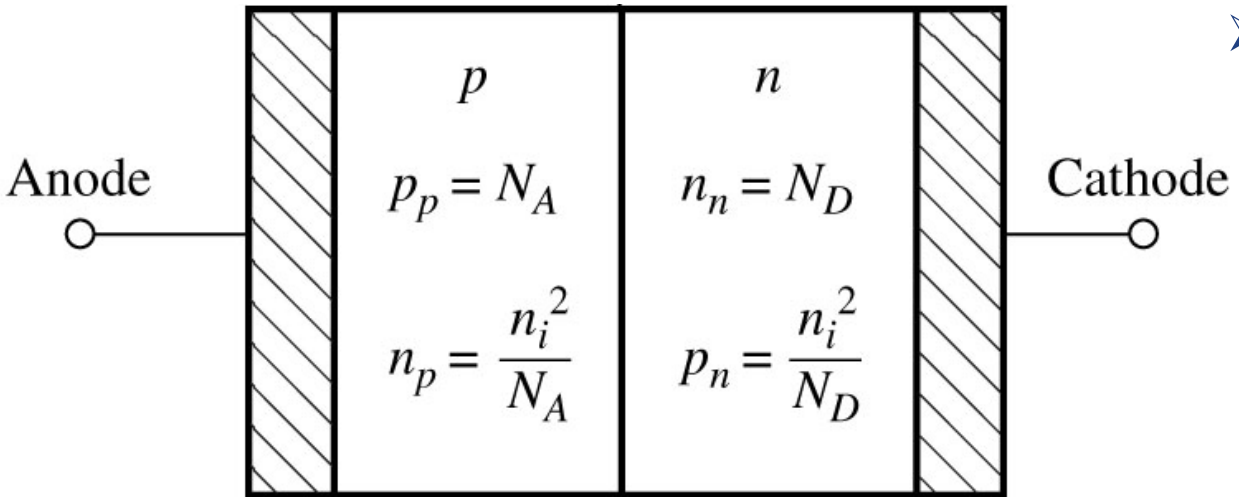
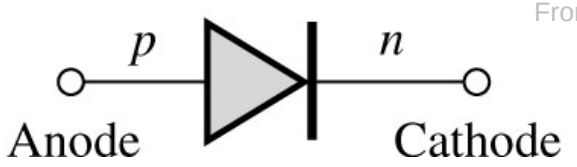
Carrier Concentrations

(mass action law)

- In thermal equilibrium, the mass action law applies in the ***p***-region as well as in the ***n***-region.
  - The minority carrier concentrations can be determined accordingly.



- Can you distinguish the different carrier concentrations p_p, p_n, n_p, and n_n?



From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.

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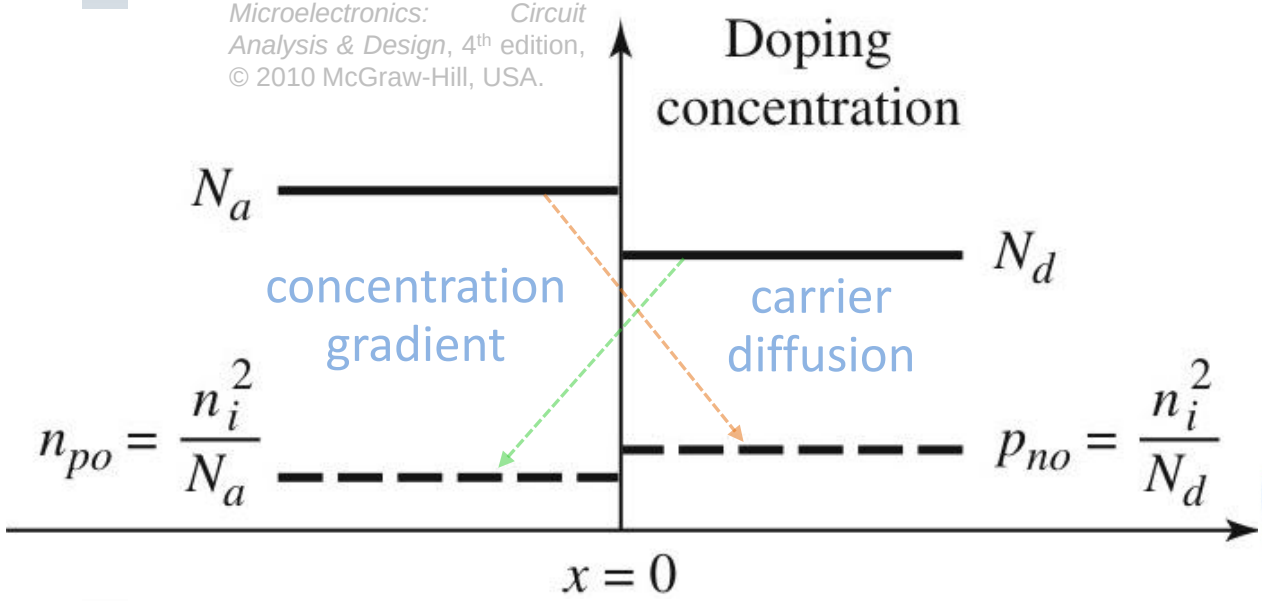
Concentration Gradient

(carrier diffusion across junction)

- Due to the large **concentration gradient** in both electrons and holes between the ***p***-region and the ***n***-region, carrier **diffusion** occurs across the junction and an equilibrium state is reached.



- **Holes** diffuse from the ***p***-region to the ***n***-region.
- **Electrons** diffuse from the ***n***-region to the ***p***-region

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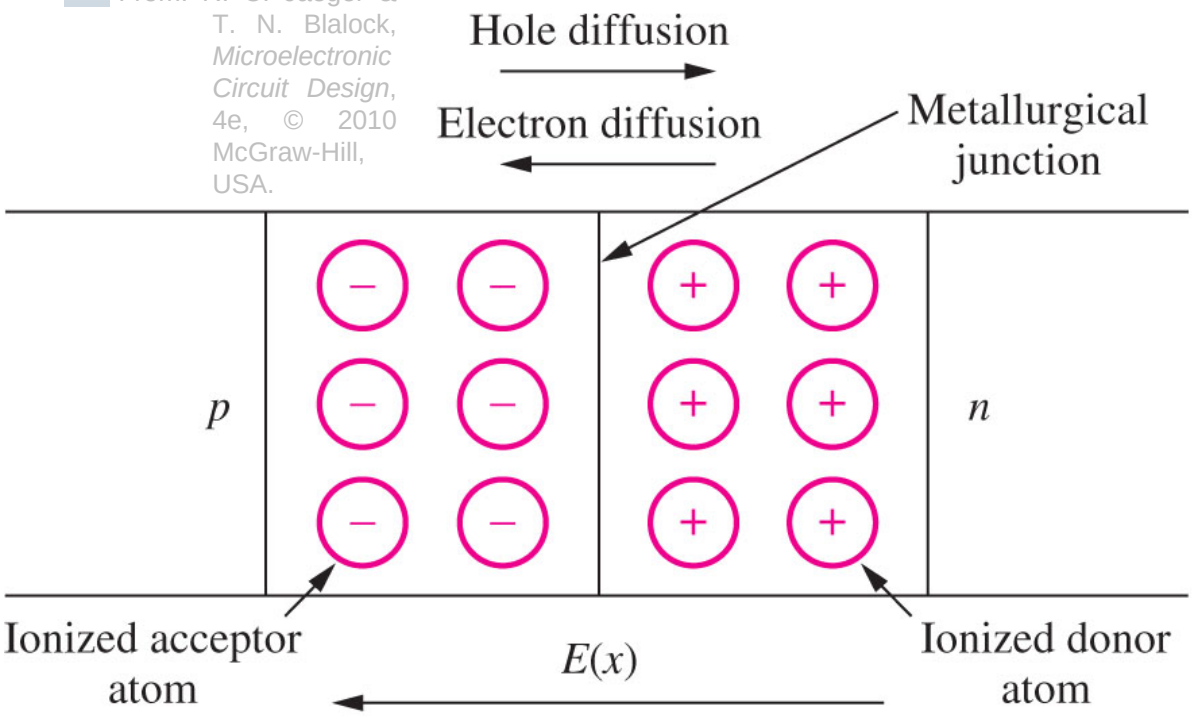
Carrier Diffusion

(immobile dopant ions)

- When the holes leave the p-type region, they leave behind immobile acceptor dopant ions, which are negatively charged.



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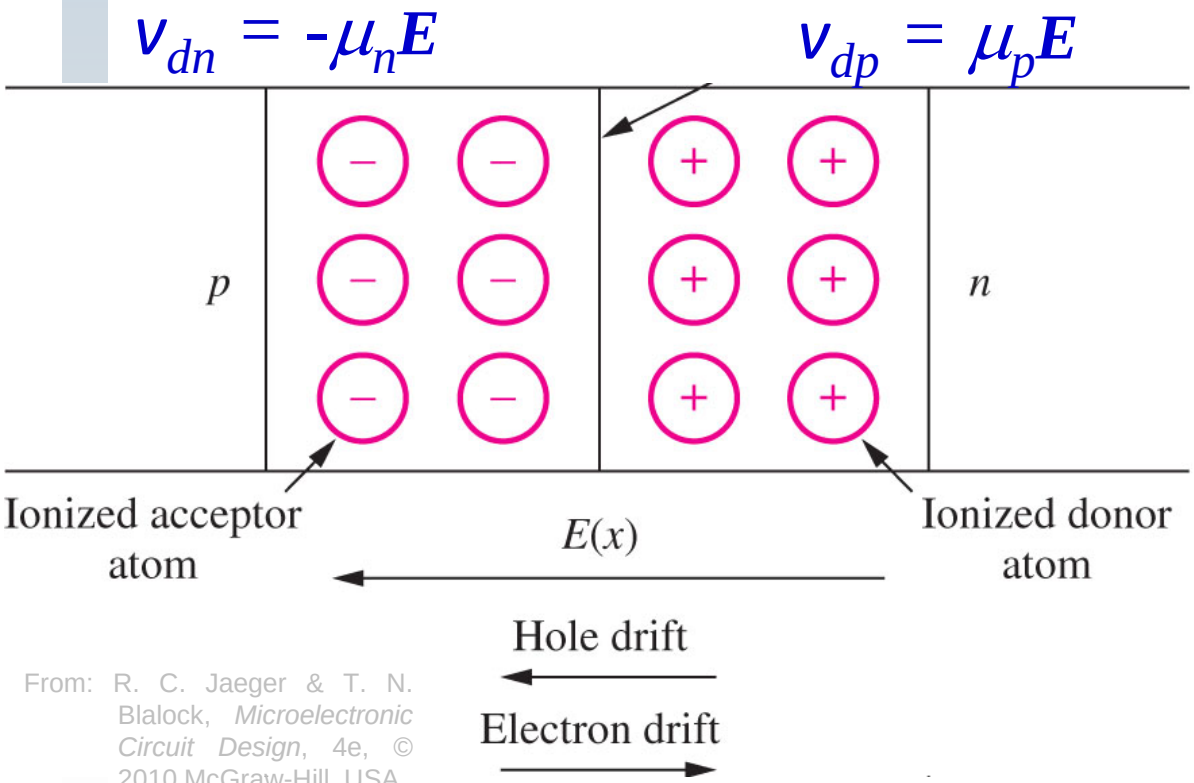
- Similarly, when the electrons leave the n-type region, immobile donor dopant ions are left behind and they are positively charged.

Carrier Drift

(electric field from immobile charges)

- With the opposite charges on the two sides near the boundary of the p-type and n-type regions, an electric field is created.



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- It points from the n-type region to the p-type region.
- It causes **drift** action of the charge carriers, opposite to the diffusion direction.

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Depletion Region

(equilibrium of drift & diffusion)

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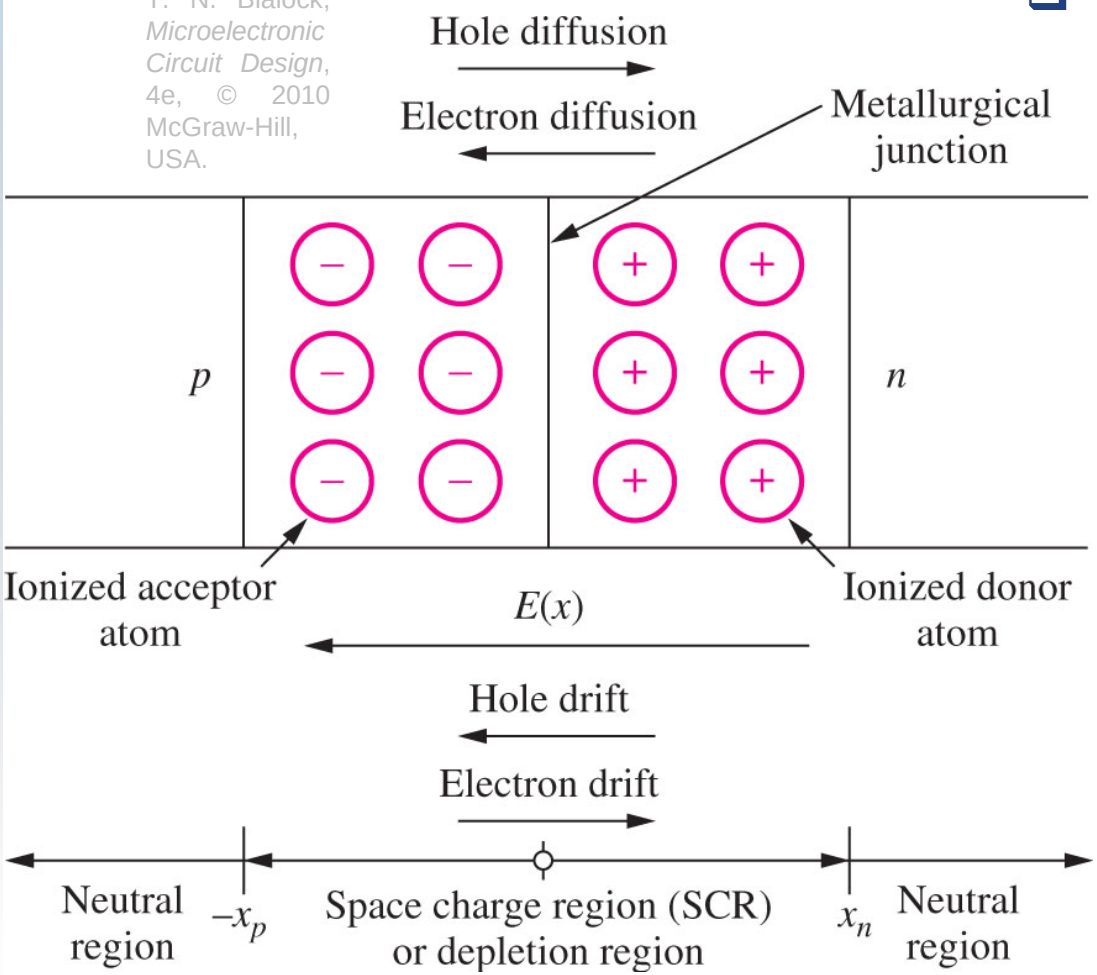

- With the drift action counteracting with the carrier diffusion, an equilibrium is attained
  - A **space-charge region** or called **depletion region** is formed at the metallurgical junction.

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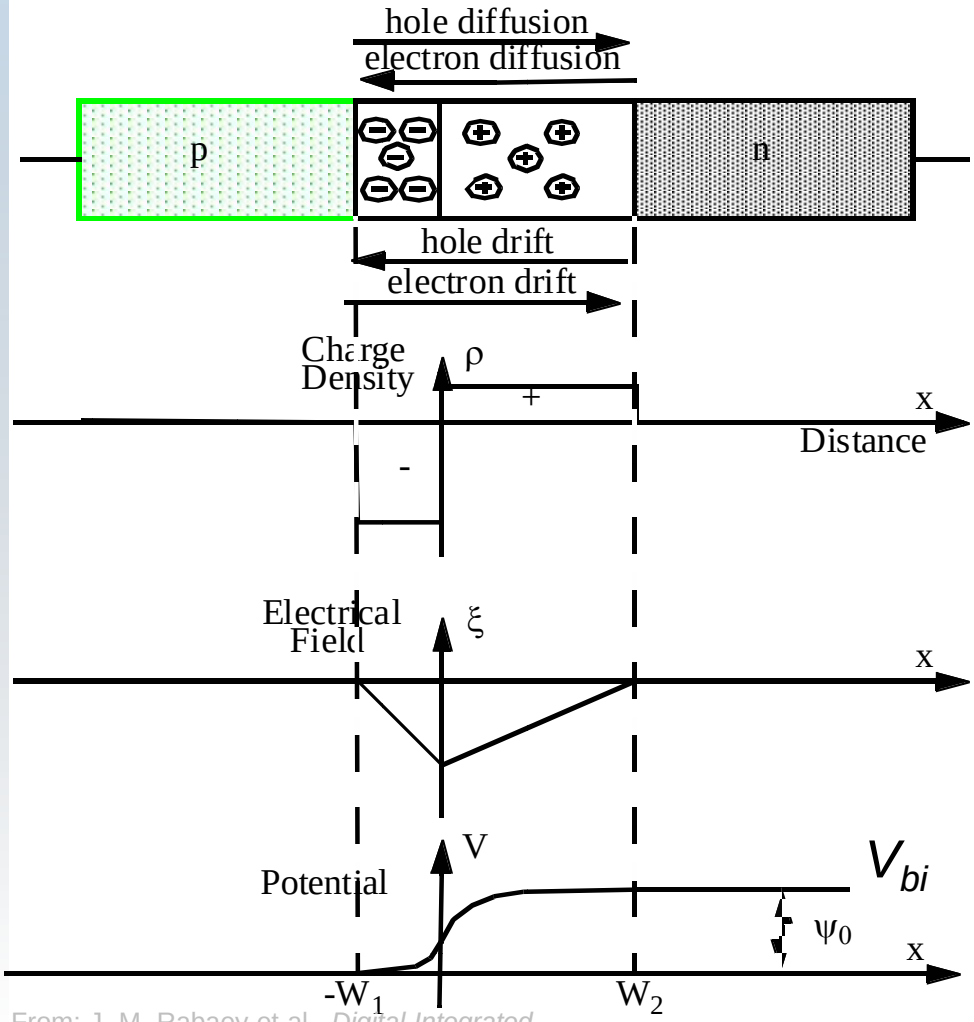
p-n Junction: Electrostatics

(charge density to electric potential)



- Using electrostatic analysis, the **electric field** can be determined from the **charge density** and the **electric potential** from the **electric field**.
- There is a **potential** difference (V_{bi}) between the p-type and n-type regions.

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From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

p-n Junction: band diagram

(E_f aligned with each other)

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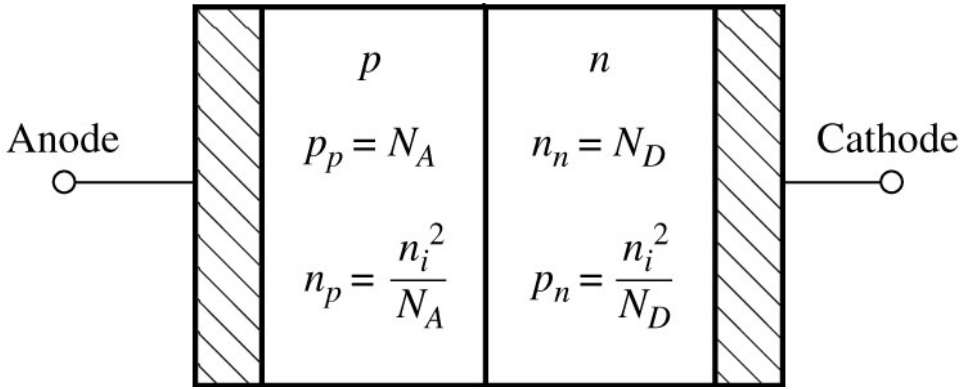

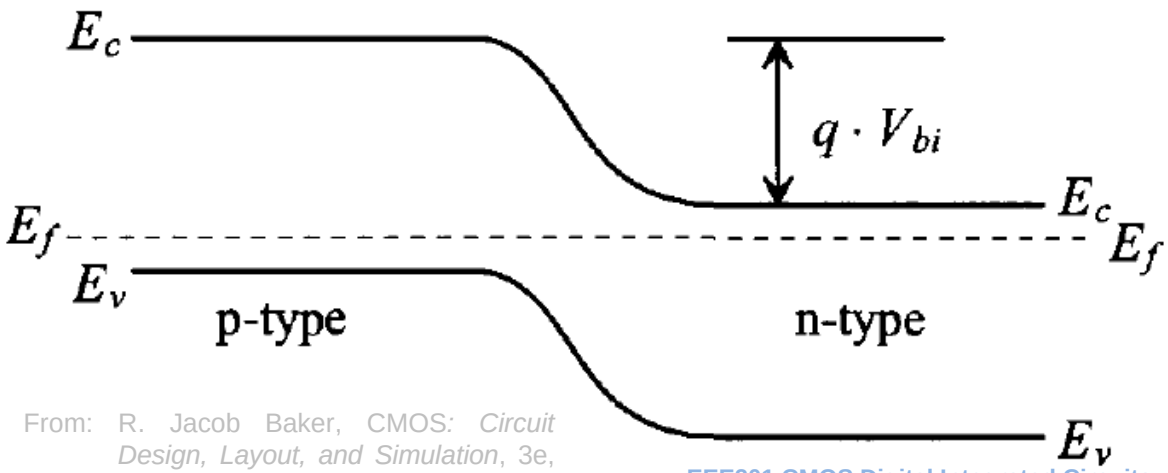

From: R. Jacob Baker, CMOS: *Circuit Design, Layout, and Simulation*, 3e, © 2010 Wiley-IEEE Press, USA.

- Using the energy band diagram, the **Fermi energy E_f** level on the side of the p-type region aligns with that on the side of the n-type region, when an **equilibrium** is reached.

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Silicon *p-n* Junction

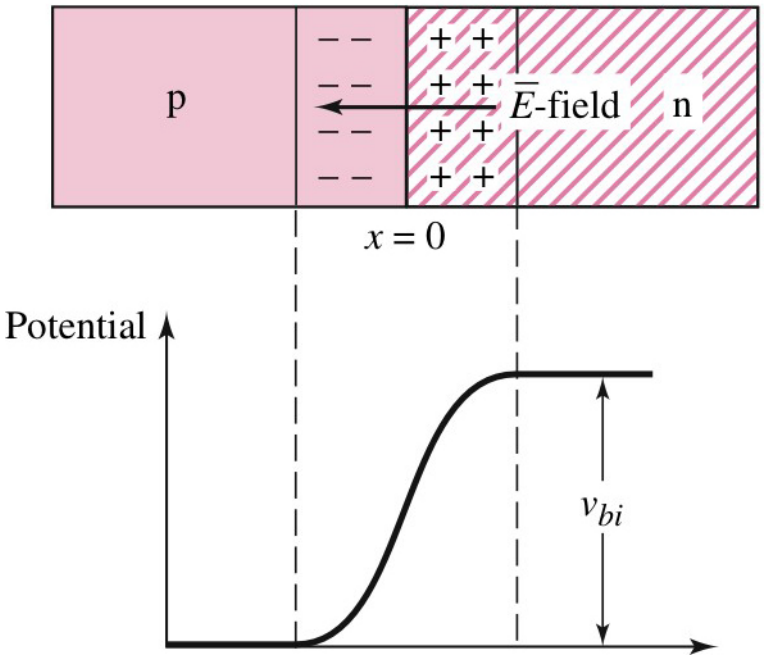
(built-in potential/voltage)

- The built-in potential or **built-in voltage V_{bi}** is given by:

$$V_{bi} = \frac{k_B T}{e} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$$= V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

  - $V_T = k_B T/e$ is called the thermal voltage and $V_T \approx 26$ mV at T = 300 K.
  - e is the electronic charge (1.60×10^{-19} C)



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Silicon *p-n* Junction

(depletion width)

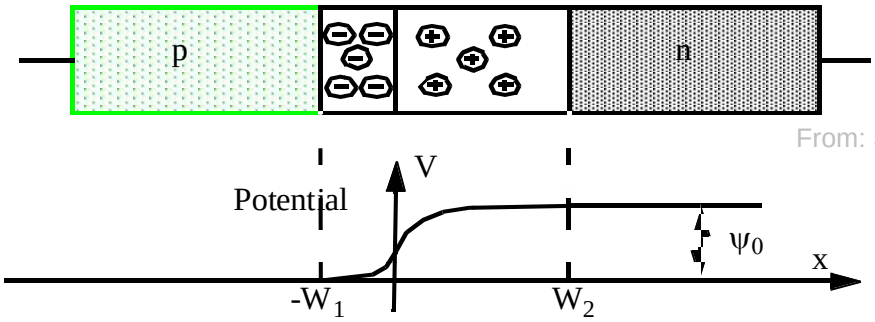
- With typical doping concentrations N_D and $N_A \approx 10^{16}$ cm^{-3}, V_{bi} is about 0.7 V for the silicon ***p-n*** junction at room temperature.
- As for the width of the **depletion region**, it is given by

$$W_0 = W_p + W_n = \sqrt{\frac{2\varepsilon_{Si}(N_a + N_d)V_{bi}}{eN_aN_d}}$$

  - Note $\varepsilon_{Si} = 11.9\varepsilon_0 = 11.9 \times (8.85\times10^{-12}$ F/m)

$$W_p = \frac{N_d}{N_a + N_d} W_0$$

$$W_n = \frac{N_a}{N_a + N_d} W_0$$



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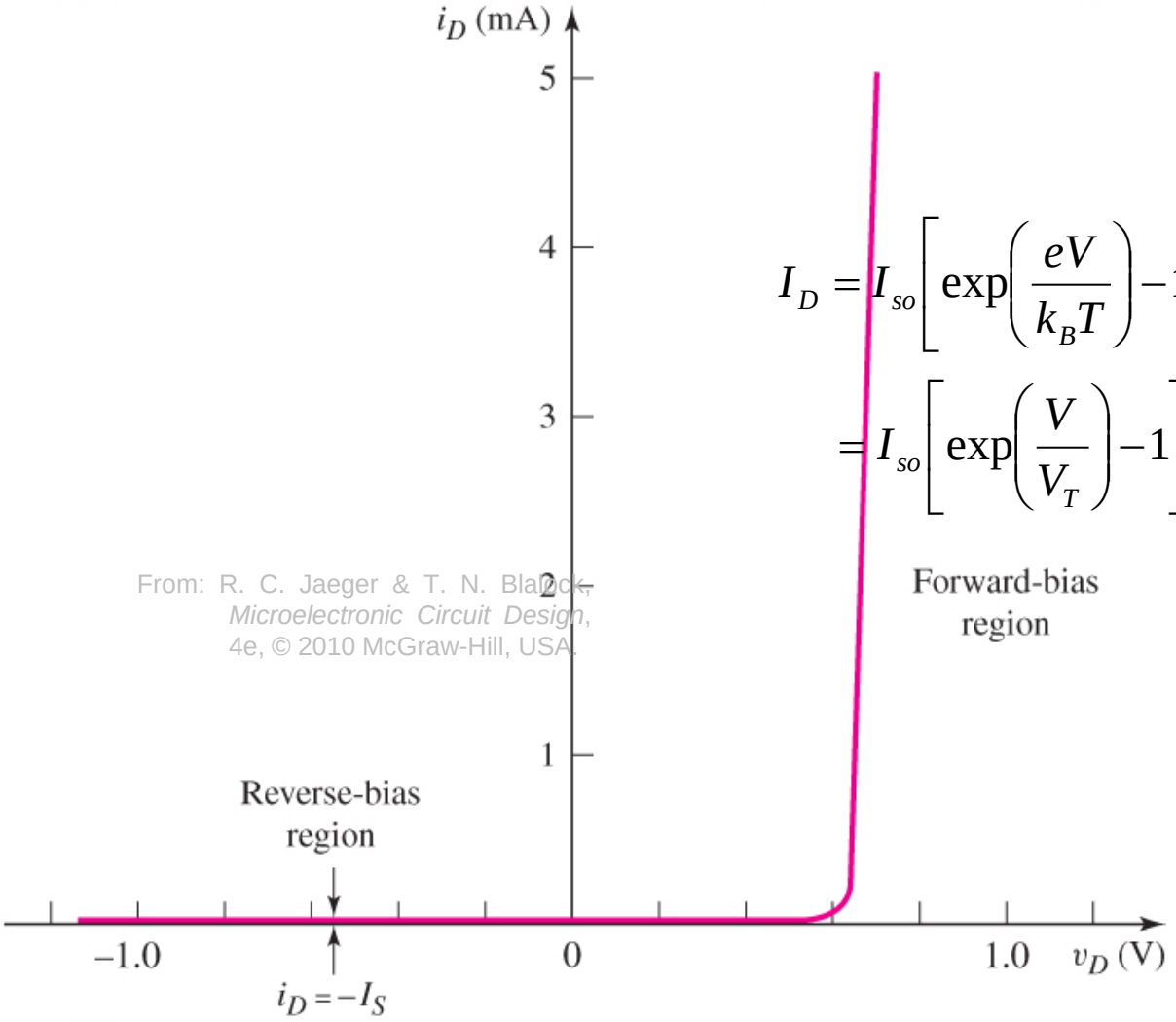
Silicon *p-n* Junction current

(exponential behaviour)



- When forward biased, the current flowing through the silicon ***p***-n junction diode increases ***exponentially***.
- When reverse biased, there is only a negligible current.

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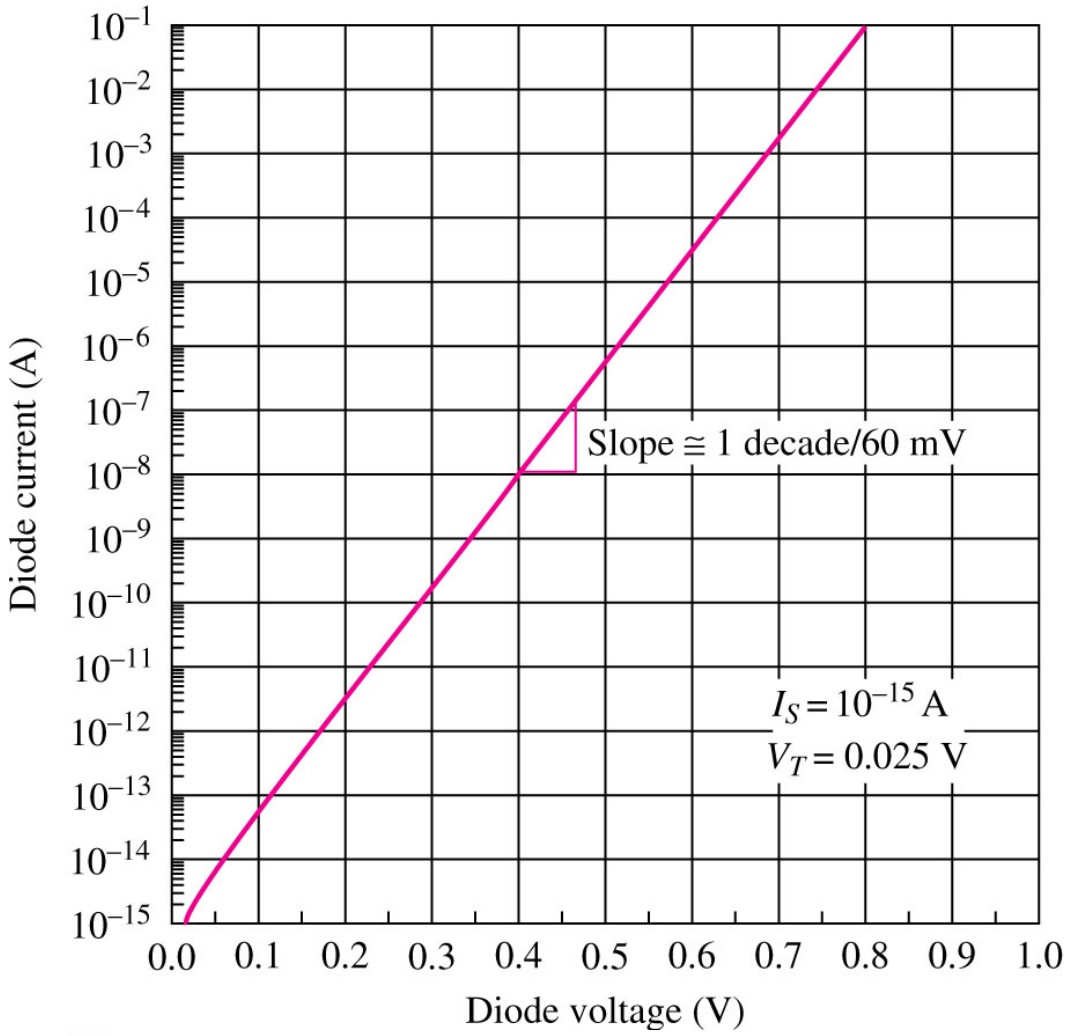
Silicon *p-n* Junction current

(60 mV per decade)



- With the exponential behaviour, the forward-biased current of the p-n junction is a straight line in a semi-logarithmic plot.
- The inverse of the slope is 60 mV per decade, which is a useful number later for looking at the MOS transistor.

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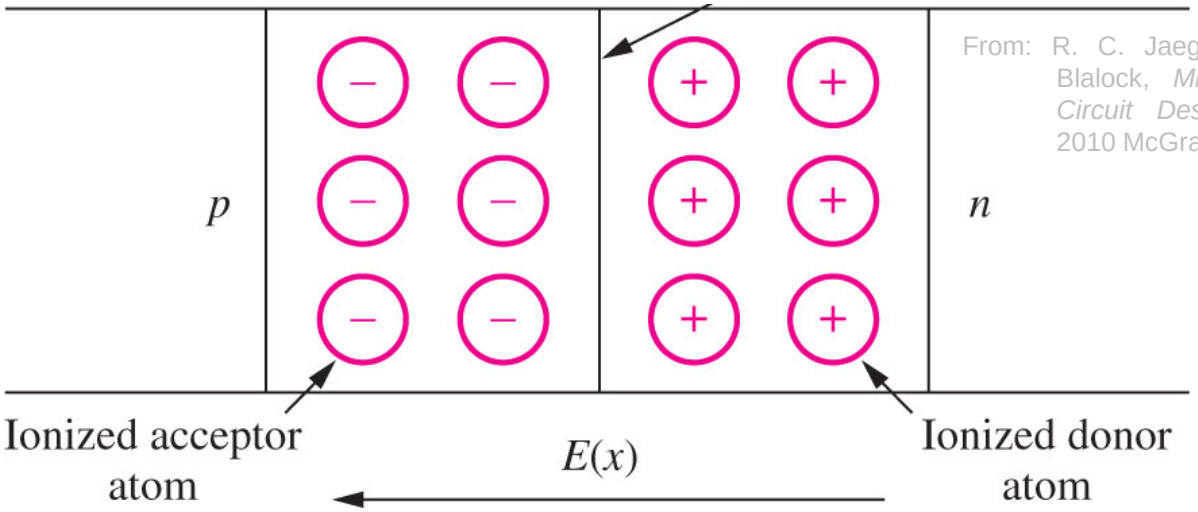
From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.

Capacitance of *p-n* Junction

(parallel plate capacitance)

- With immobile dopant ions of opposite charge on both sides of the metallurgical junction, the ***p-n* junction** is almost like a parallel-plate capacitor.



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Note that the **depletion width** W_0 is a voltage-dependent variable.

- In a parallel-plate capacitor, the capacitance is:

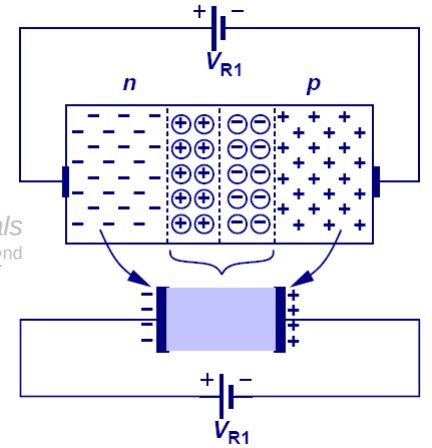
$$C = \frac{\varepsilon A}{d} \Rightarrow C_j = \frac{\varepsilon_{Si} A_j}{W_0}$$

Capacitance of *p*-*n* Junction

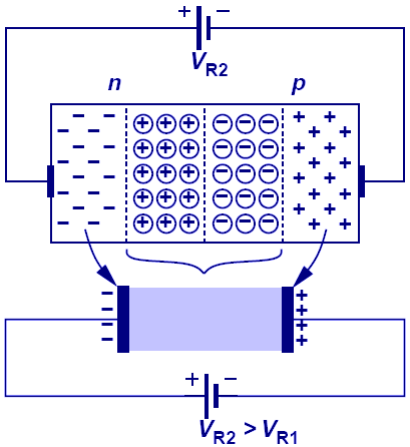
(junction capacitance)

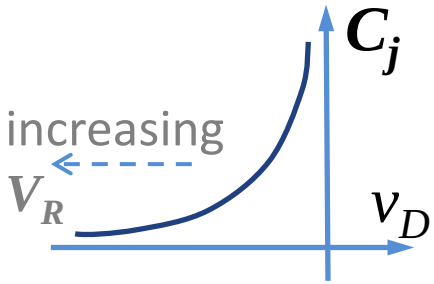
- Under **reverse bias**, the ***p*-*n*** junction can be viewed as a voltage-dependent capacitor.
- By varying the reverse bias voltage V_R, the depletion width changes, therefore changing the capacitance.
- This **junction capacitance**, or called depletion capacitance, can be expressed as

$$C_j = \frac{C_{j0}}{\sqrt{1+\frac{V_R}{V_{bi}}}}$$



From: Behzad Razavi, *Fundamentals of Microelectronics*, 2nd edition, © 2013 Wiley, USA.





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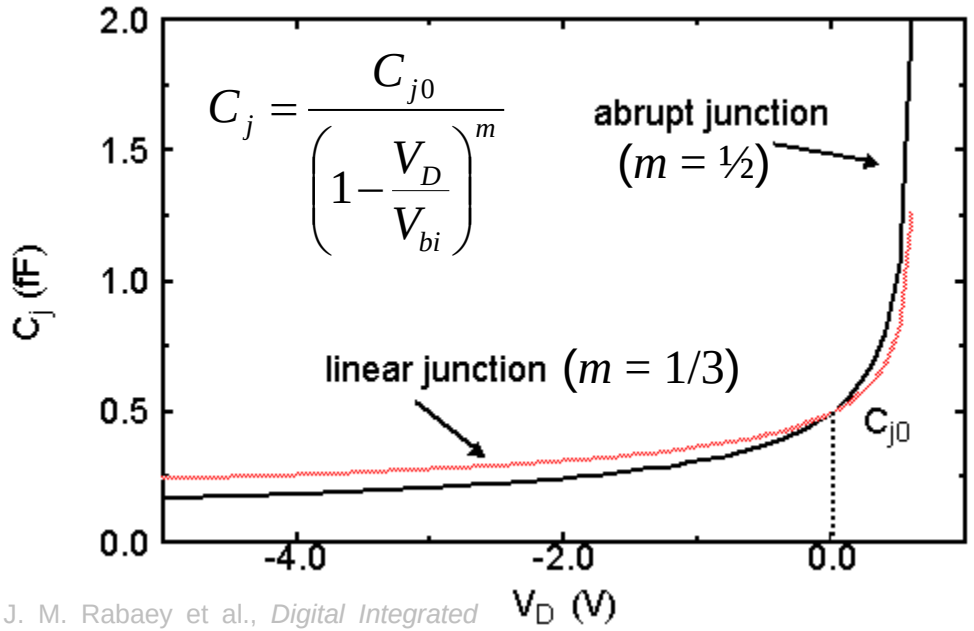
Junction Capacitance

(forward-biased)

- When forward-biased, the **depletion width** becomes smaller. As a result, the **junction capacitance** increases with the forward-bias voltage before reaching the built-in voltage.



- The voltage dependence of the junction capacitance has a slight difference between an abrupt junction and a linear unction.

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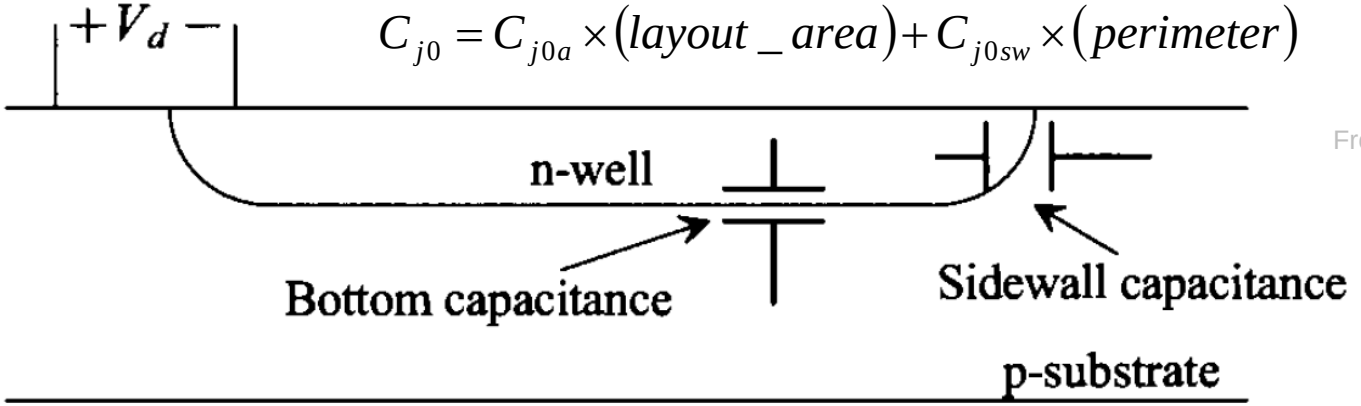
From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

Junction Capacitance

(sidewall capacitance)

- In estimating the junction capacitance in CMOS IC design, the zero-bias junction capacitance C_{j0} needs to be determined first.
- C_{j0} consists of two parts given in the parameter data of a CMOS IC process: one proportional to the area while the other (called **sidewall capacitance**) to the perimeter.



From: R. Jacob Baker, CMOS: *Circuit Design, Layout, and Simulation*, 3e, © 2010 Wiley-IEEE Press, USA.

Note: C_{j0a} & C_{j0sw} are normalised capacitances with data provided by the CMOS process.

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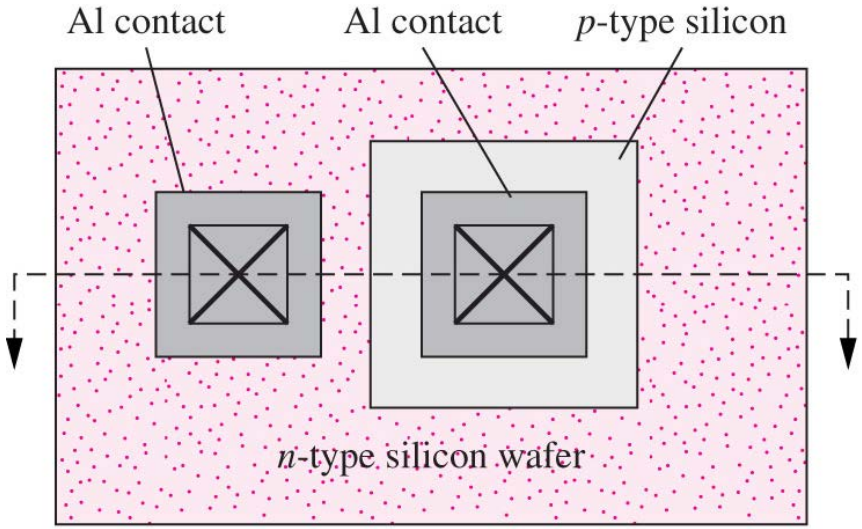
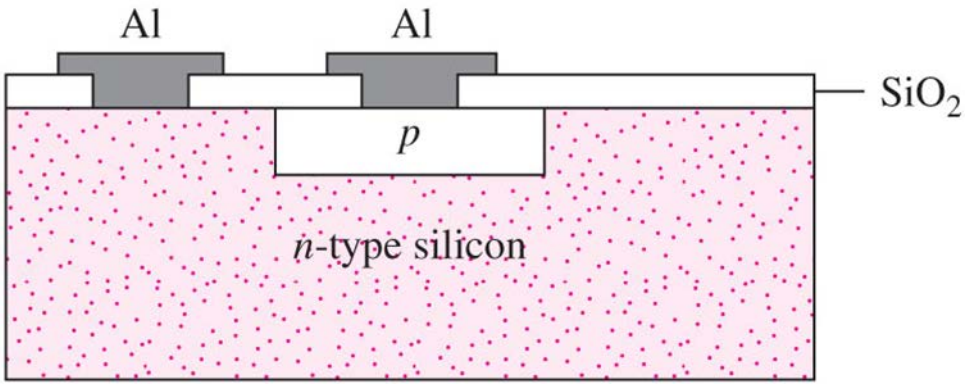
Silicon *p-n* Junction

(simple implementation)



From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.



- If a ***p-n* junction** diode is to be designed in a CMOS IC, the **physical layout** is of simple one (for small-current loading) is shown here together with the corresponding cross-sectional structure.

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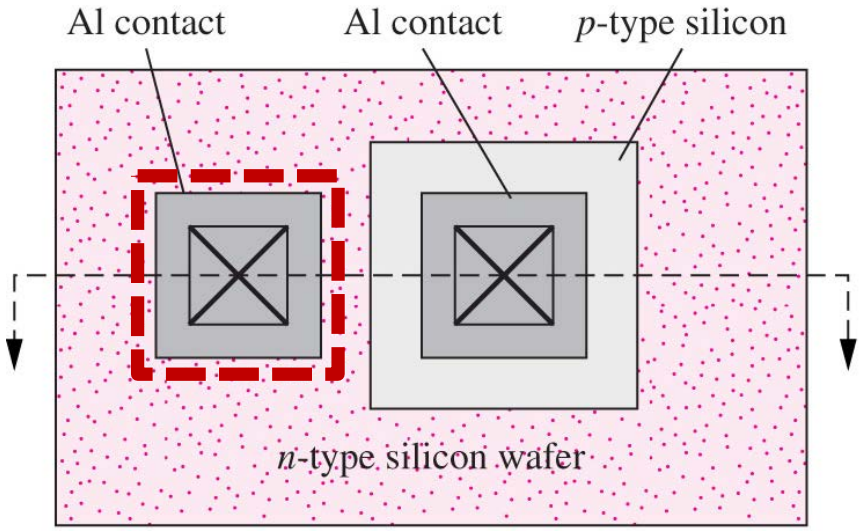
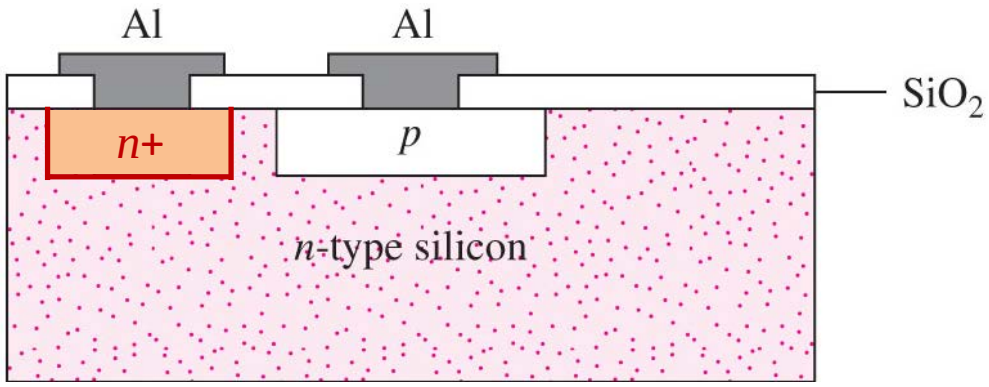
Silicon *p-n* Junction

(improved implementation)



From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.



- An improvement can be made in the contact of the n-type substrate by using a heavily doped ***n+*** region.
- The electrical connection is better in this case because of the so-called **ohmic contact**.

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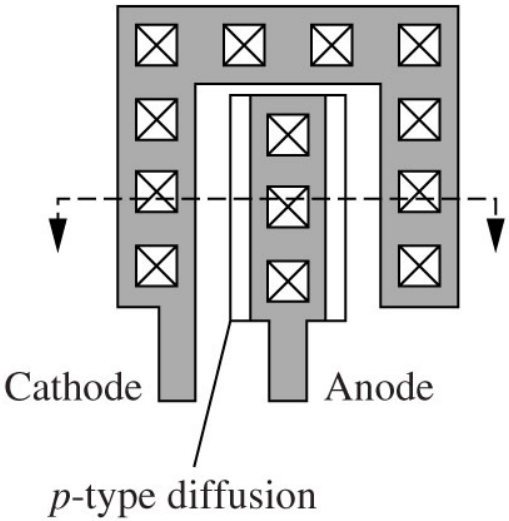
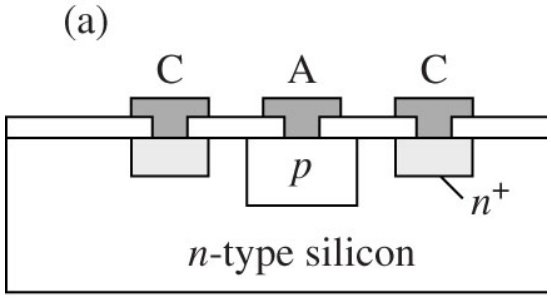
Silicon *p-n* Junction

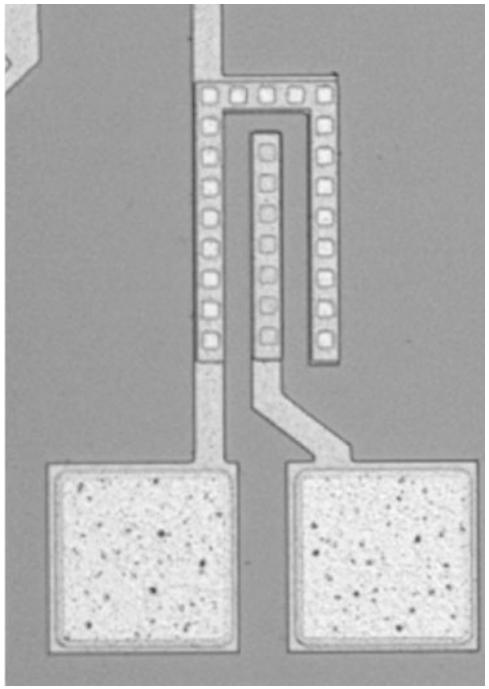
(further improved implementation)

- To reduce the series resistance of the ***p-n* junction** diode, an annular layout can be used.





From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.



- The current can flow in more paths from the anode to the cathode. Such a design can also accommodate a larger diode current. However, the junction capacitance will increase unavoidably.

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