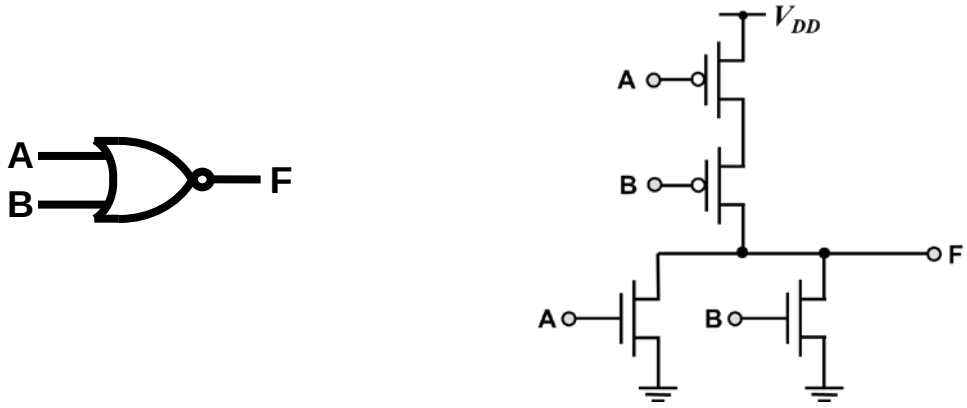
EEE201 CMOS Digital Integrated Circuits
CMOS IC Layout Design Project

Assessment Weighting
This assessment counts **15%** of the module marks.

Aims
This project aims to provide students with an experience of designing a simple silicon **CMOS** integrated circuit (IC) at the layout level, as well as offering an insight into the CMOS manufacturing process flow.

Learning Outcomes
On completion of this project you should be able to:
1. Understand the manufacturing processes involved in fabricating silicon-based devices, in particular CMOS ICs.
2. Understand the design process and constraints involved in developing CMOS ICs.
3. Design mask layout of a CMOS logic circuit.
4. Produce an engineering style report.

Design Task
The objective of this assignment is to design and minimise the layout area and the number of masks required to manufacture the simple logic circuit shown in Figure 1(a), formed at the device level as shown in Figure 1(b).



(a) (b)

Fig. 1 NOR2 gate: (a) logic symbol and (b) circuit schematic of a CMOS 2-input NOR gate

The process parameters for the design are listed in Table 1. You should use these data to calculate the aspect ratio (or equivalently width/length) of each component and then determine a suitable layout to interconnect the components, while minimising the IC area.

Table 1: CMOS process parameters

Oxide areal capacitance	$3x10^{-4}$ F/m^2
Threshold Voltage V_T	0.3 V
Supply Voltage V_{DD}	3 V
Electron mobility	0.1 $m^2V^{-1}s^{-1}$
Hole mobility	0.05 $m^2V^{-1}s^{-1}$
Minimum feature size	0.3 μm
Maximum alignment error	0.15 μm