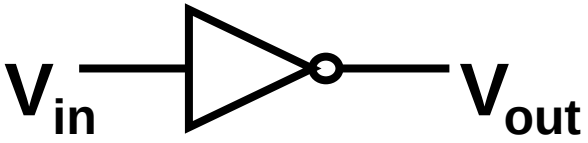
MOS Inverter Static Characteristics

(material developed by Prof. Cezhou Zhao
with slides from other sources,
thanks to Kenneth R. Laker, University of Pennsylvania)

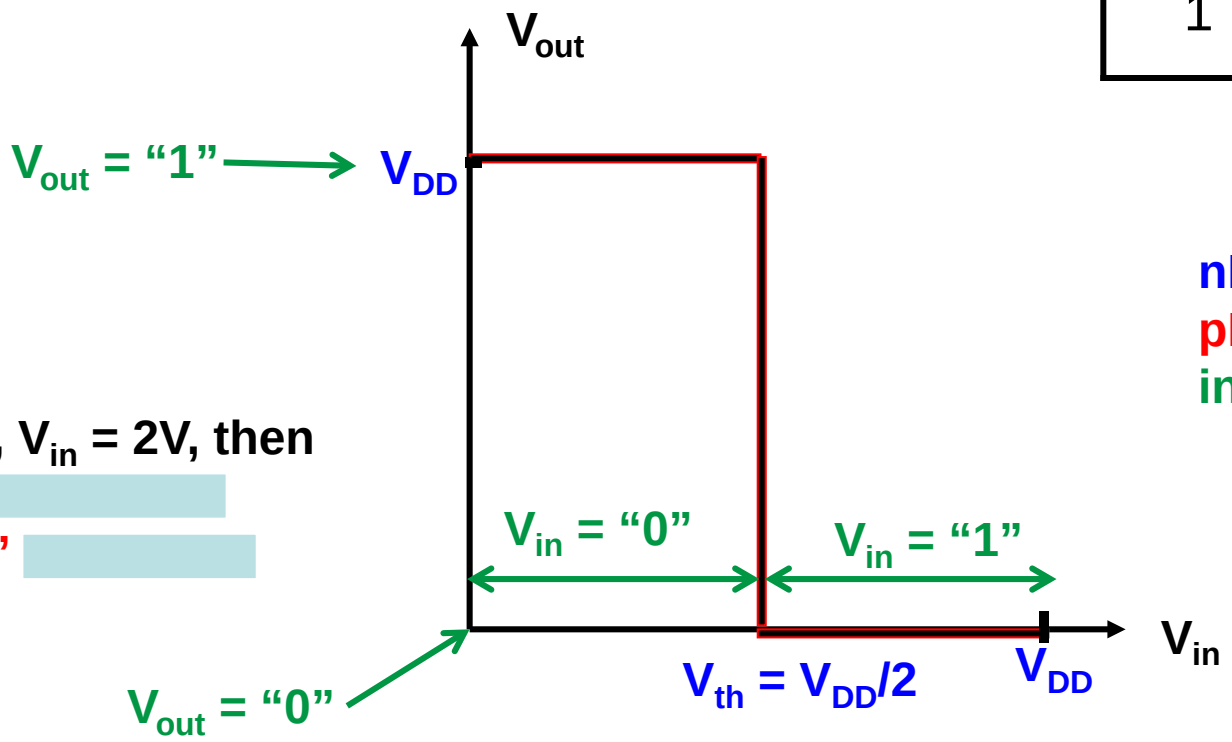
outline

- Voltage Transfer Characteristics (VTC)
- nMOS inverters
  - Resistive load inverter
  - Saturated enhancement load inverter
- CMOS inverter
  - CMOS VTC
  - Comparison between CMOS and MOS inverters
- Combinational CMOS logic gates (static)
- Ratioed Logic

Ideal Inverter: Voltage Transfer Characteristics (VTC)



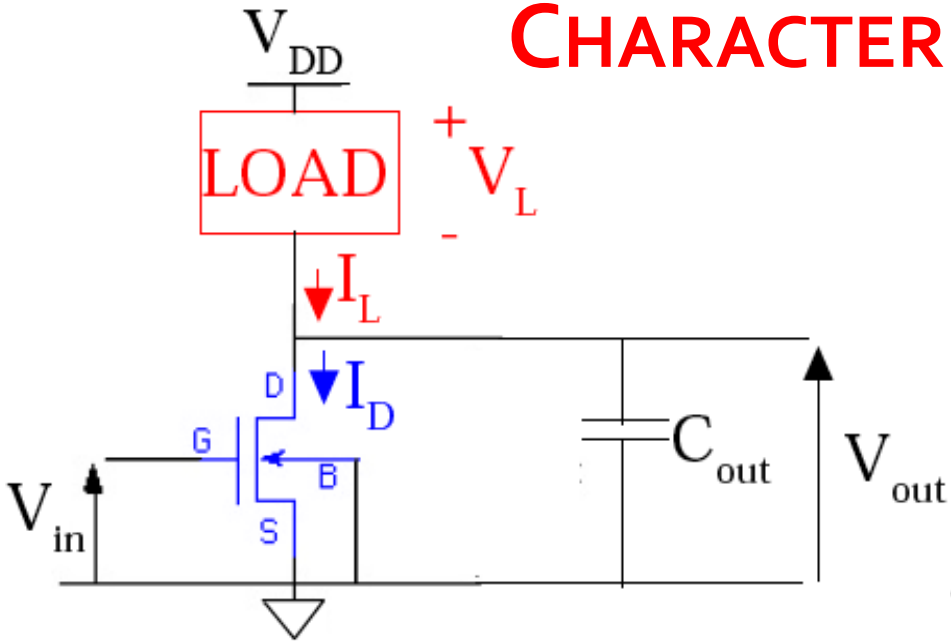
V_{in}	V_{out}
0	1
1	0

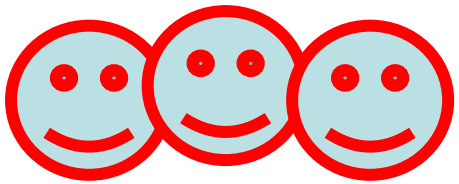


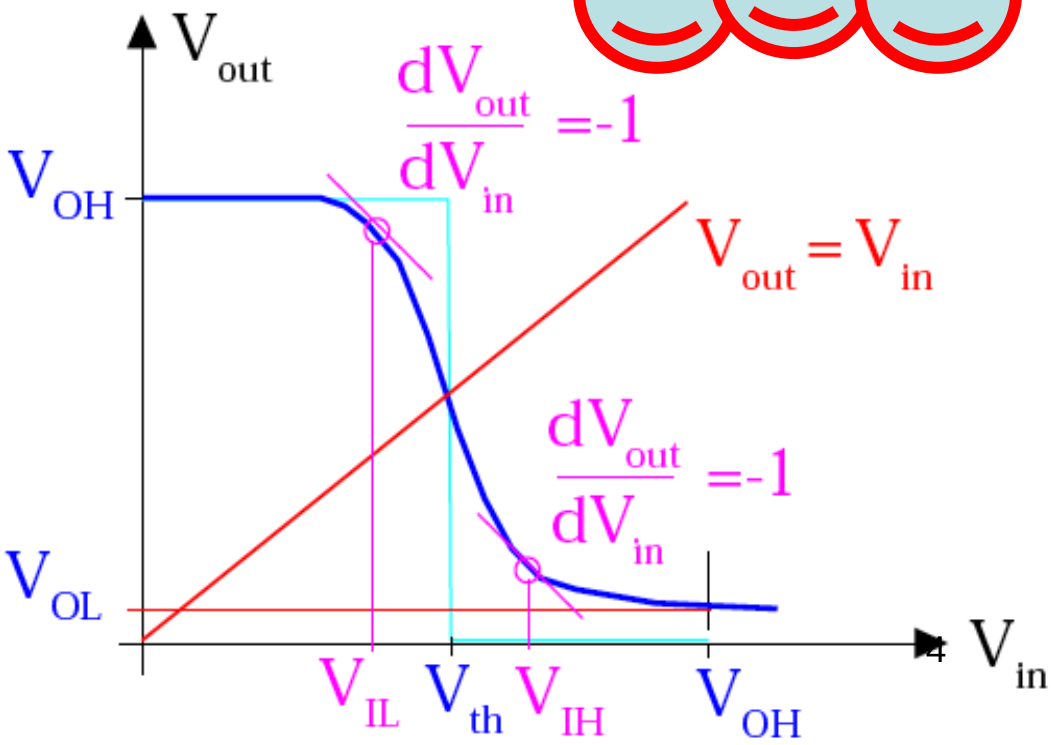
nMOSFET : V_{Tn}
pMOSFET : V_{Tp}
inverter: V_{th}

If V_{DD} = 5V, V_{in} = 2V, then
V_{in} is: "0"
V_{out} is : "1"

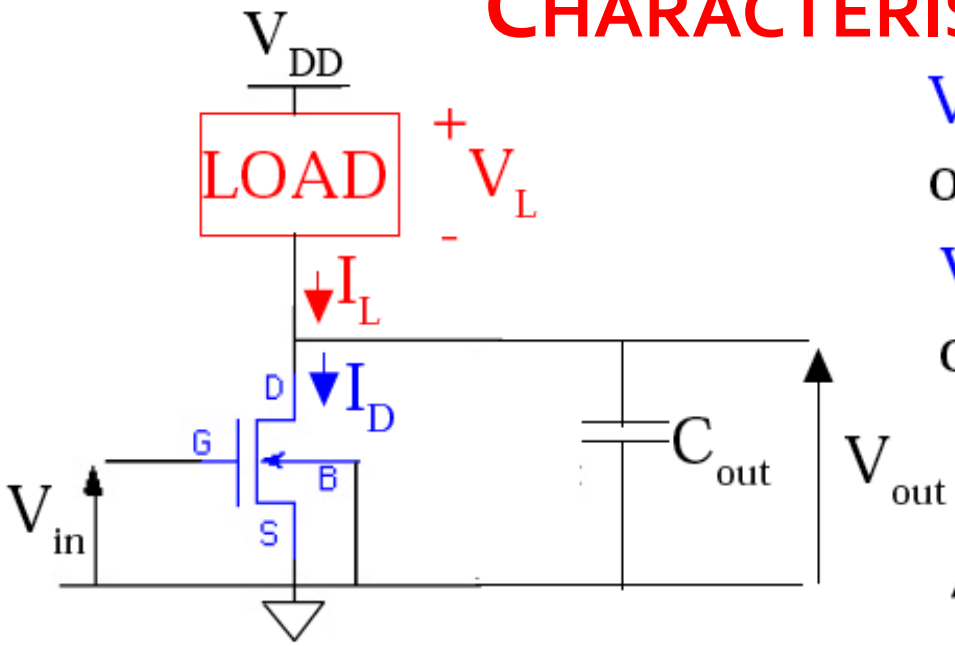
Actual Inverter's Voltage Transfer Characteristics (VTC)







Actual Inverter's Voltage Transfer Characteristics (VTC)



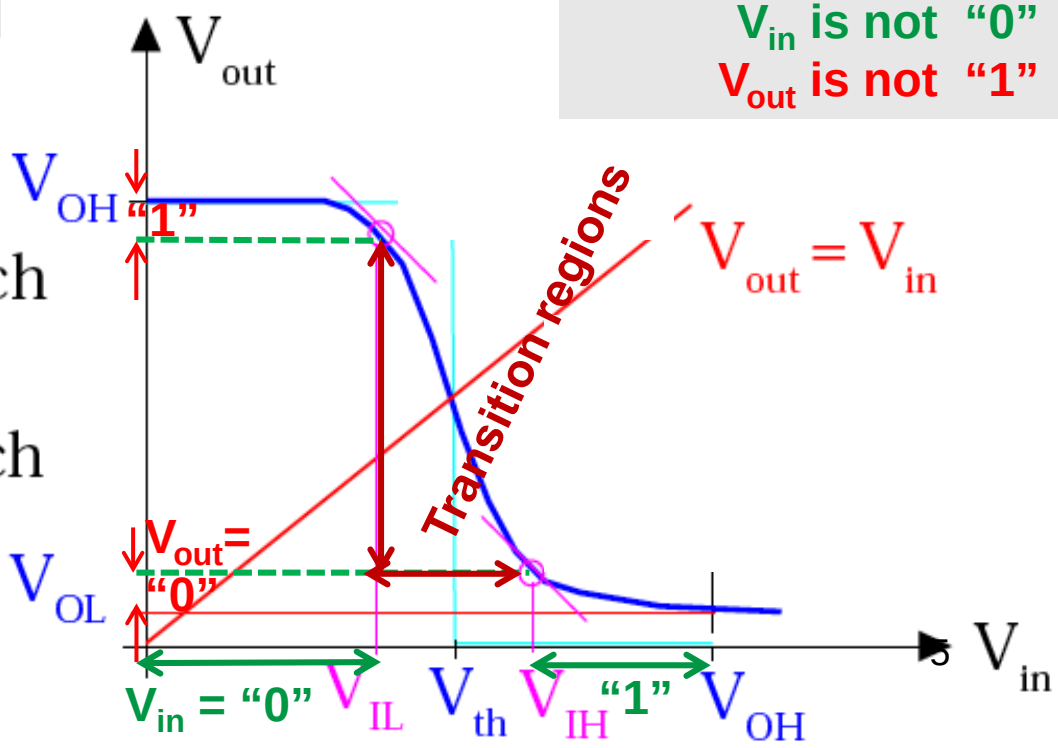
V_{OH} -> max output voltage when output is "1"

V_{OL} -> min output voltage when output is "0"

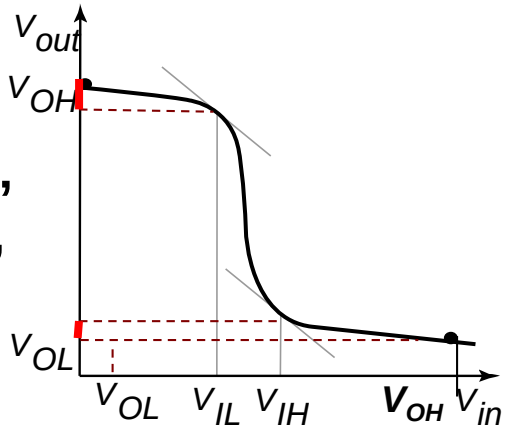
If V_{th} = 3V, V_{IL} = 2V, and V_{in} = 2.5V, then
V_{in} is not "0"
V_{out} is not "1"

V_{IL} -> max input voltage which can be interpreted as "0"

V_{IH} -> min input voltage which can be interpreted as "1"

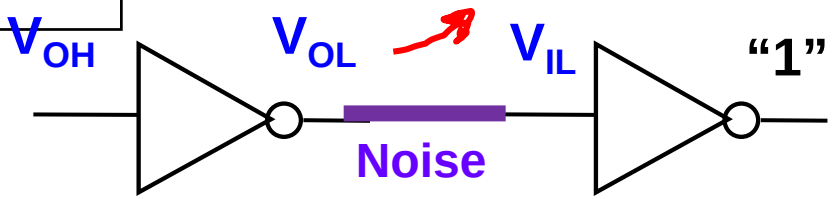


V_{OH}: max output voltage when output is “1”
V_{OL}: min output voltage when output is “0”
V_{IL}: max input voltage which can be interpreted as “0”
V_{IH}: min input voltage which can be interpreted as “1”



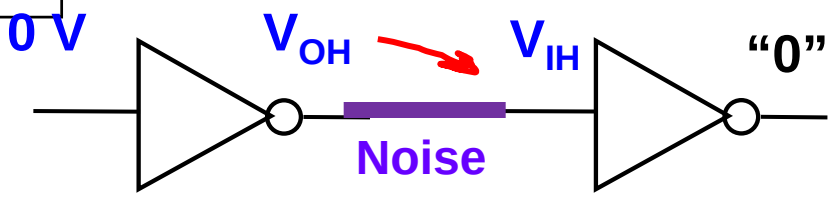
noise margin for “**low**” signals

$NM_L = V_{IL} - V_{OL}$



noise margin for “**high**” signals

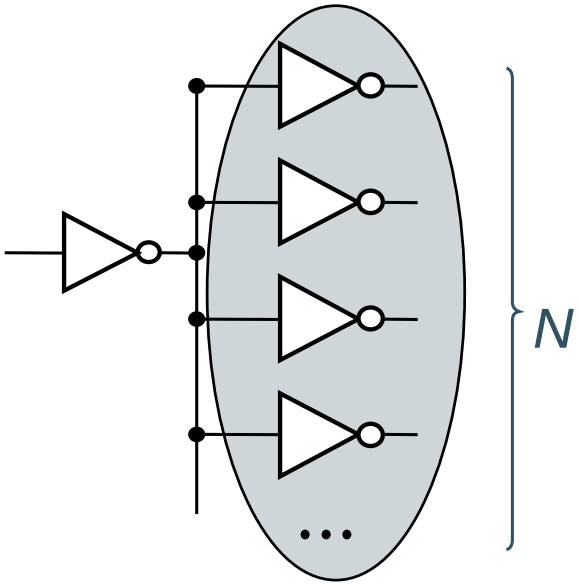
$NM_H = V_{OH} - V_{IH}$



- The regions of acceptable high and low voltages are delimited by V_{IH} and V_{IL} .

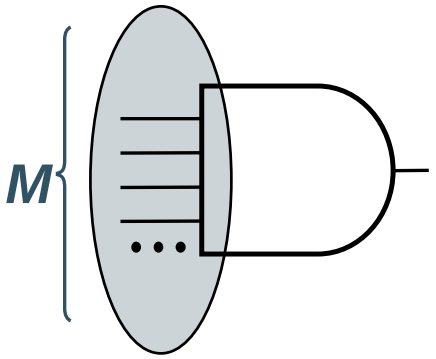
Fan-In and Fan-Out

- Complex digital operations are formed with a variety of gates interconnected to yield the desired logic function.
- Sometimes a number of inputs are connected to one gate input and output of a gate may be connected to a number of gates.
- Typical **fan-in** and **fan-out** numbers are 3.



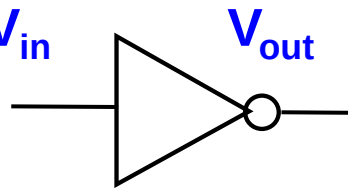
Fan-out *N*

- **Fan-out** : the max. number of load gates connected to the output of the driving gate without altering its performance
  - gates with large fan-out are slower
- **Fan-in** : the max. number of inputs to the gate without altering its performance
  - gates with large **fan-in** are bigger and slower

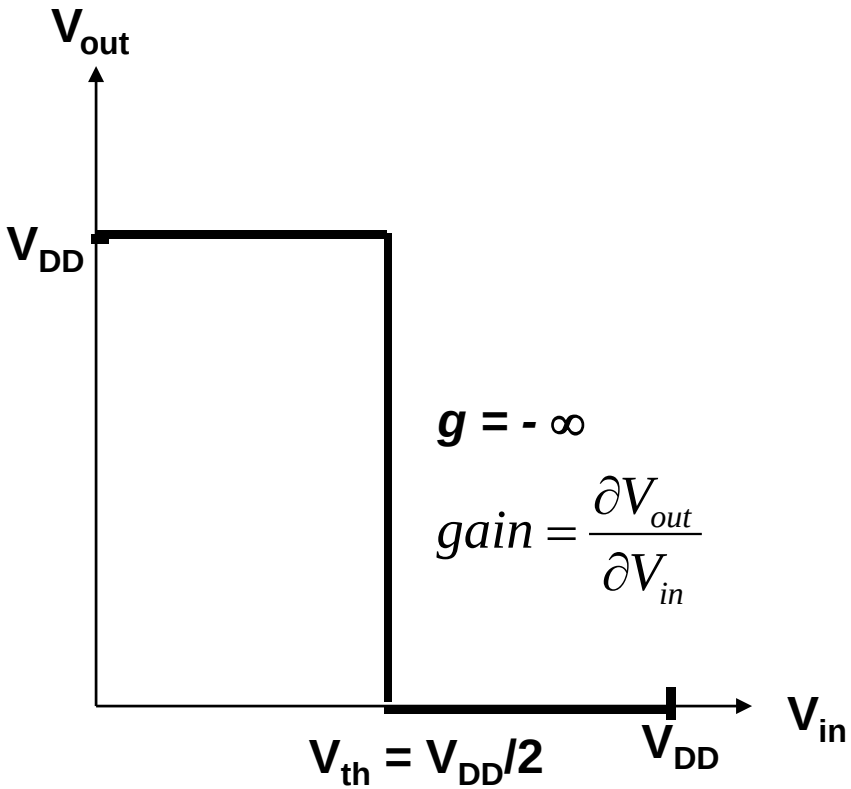


Fan-in *M*

The Ideal Inverter



- The ideal gate should have
  - infinite gain in the transition region
  - a gate threshold located in the middle of the logic swing
  - high and low noise margins equal to half the swing
  - input and output impedances of infinity and zero, respectively.



$g = -\infty$

$$gain = \frac{\partial V_{out}}{\partial V_{in}}$$

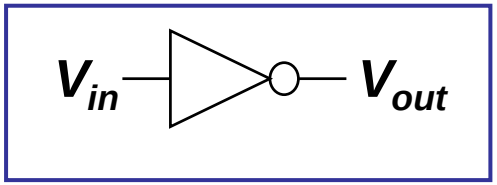
$R_i = \infty$

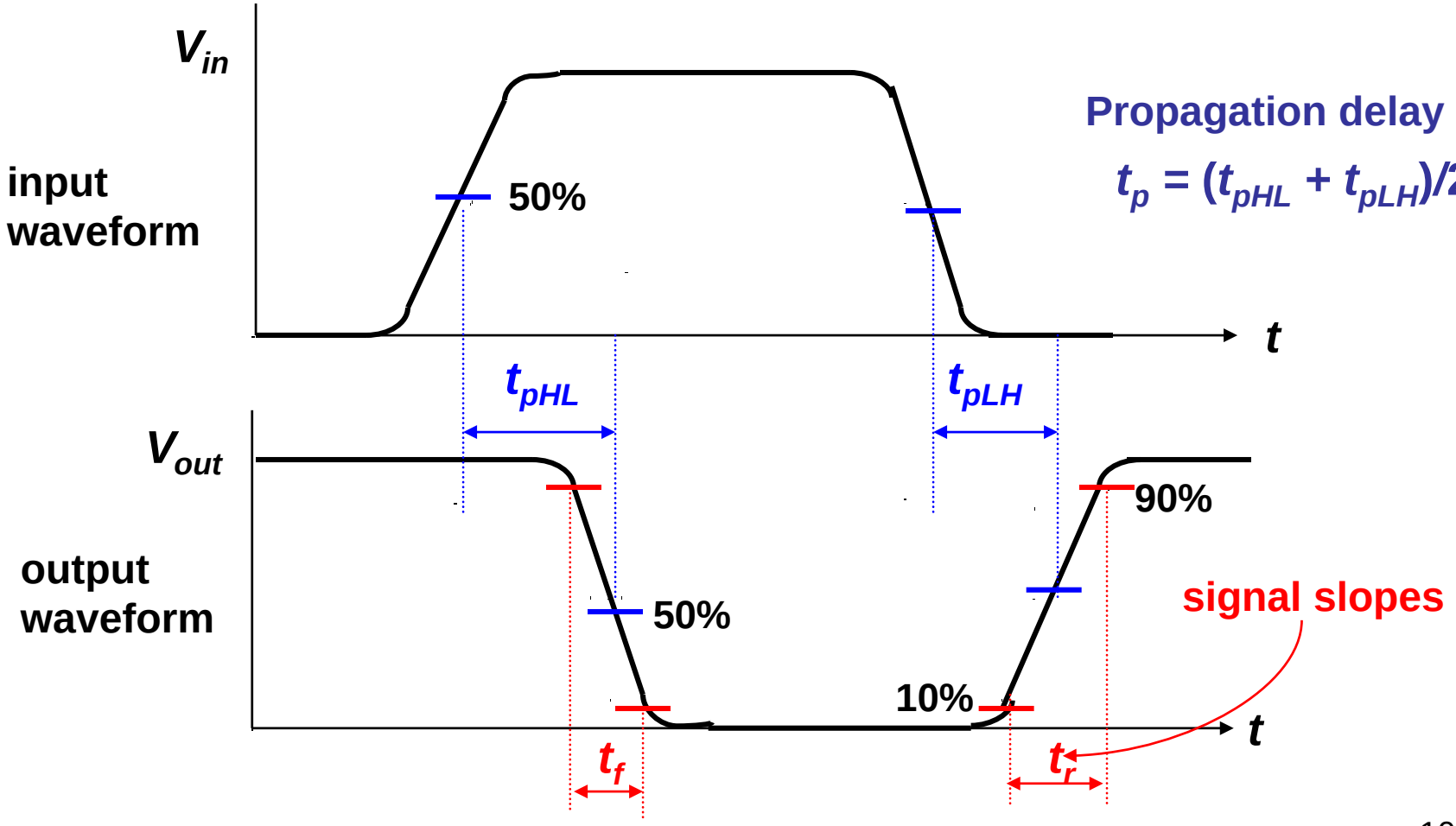
$R_o = 0$

Fan-out = ∞

$NM_H = NM_L = V_{DD}/2$

Delay Definitions



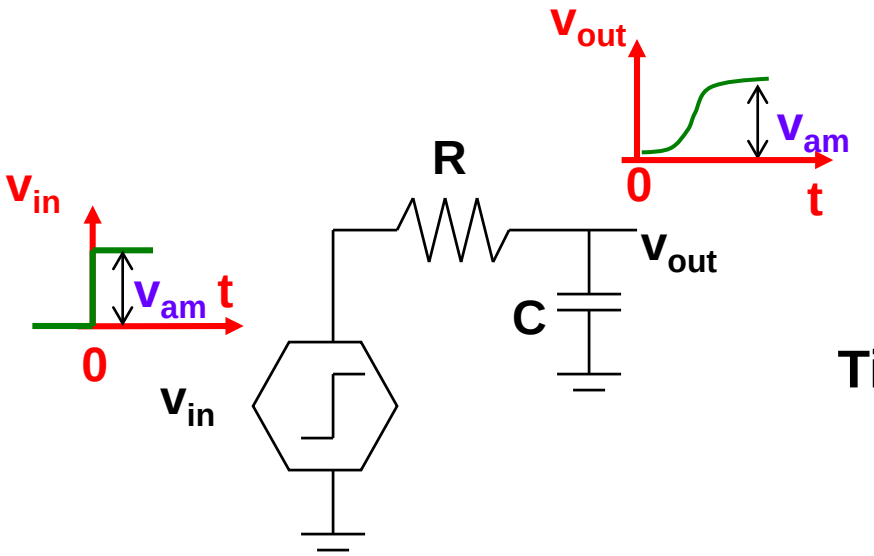


Propagation delay

$$t_p = (t_{pHL} + t_{pLH})/2$$

Modeling Propagation Delay

- Model circuit as first-order RC network



Abruptly rise

$v_{out}(t) = (1 - e^{-t/\tau})v_{am}$

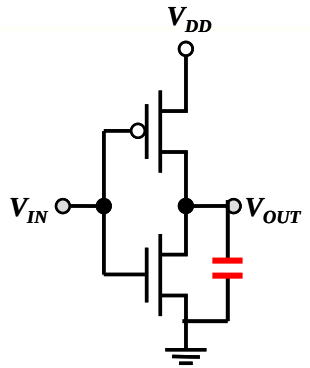
where $\tau = RC$

Time to reach 50% point ($v_{out}=v_{am}/2$) is
$t = \ln(2)\,\tau = 0.69\,\tau$

Time to reach 90% point is
$t = \ln(9)\,\tau = 2.2\,\tau$

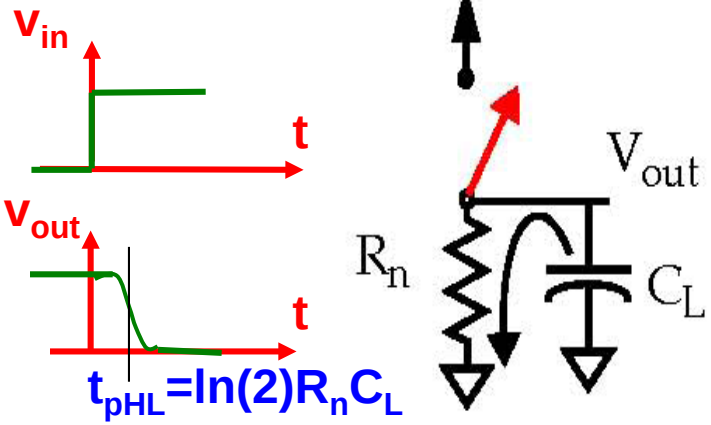
- **Matches the delay of an inverter gate.**

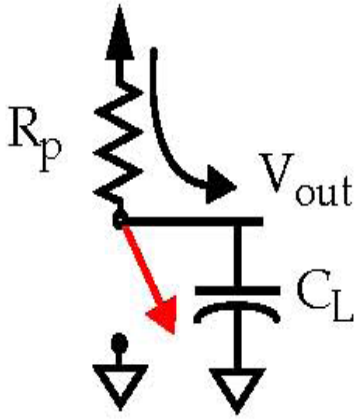
Dynamic CMOS Inverter Models

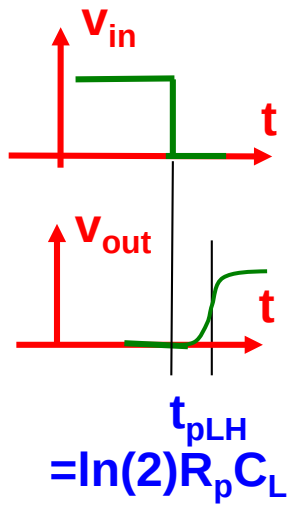


It is possible to approximate the transient response to an RC model.

The response is dominated by the output capacitance of the gate, C_L.







Load capacitance, C_L, is due to *diffusion*, *routing* and *downstream* gates.

The propagation delay assuming an instantaneous input transition is R_pC_L.

This indicates a fast gate is built by keeping either or both of R_p and C_L small.

R_p is reduced by increasing the W/L ratio.

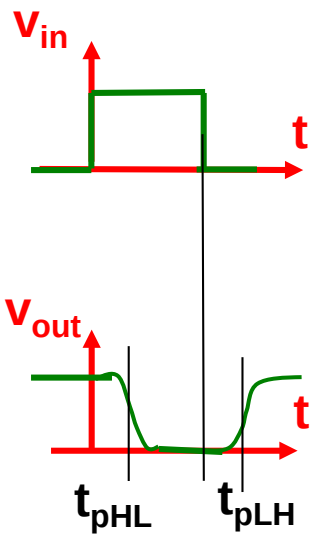
Bear in mind that, in reality, $R_{n/p}$ is a nonlinear function of the voltage across the transistor.

Propagation Delay: First-Order Analysis

Propagation delay is then computed using a first-order linear RC network model:

$$t_{pHL} = \ln(2)\, R_n C_L = 0.69\, R_n C_L$$

$$t_{pLH} = \ln(2)\, R_p C_L = 0.69\, R_p C_L$$



The propagation delay is the average of the two:

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L \left(\frac{R_n + R_p}{2} \right)$$

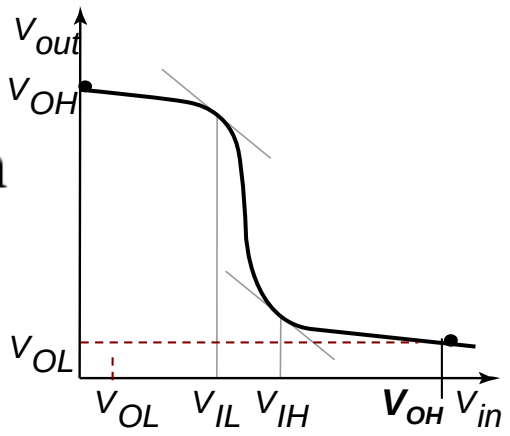
This indicates to make rise and fall times identical, it is necessary to make the "on" resistance of the NMOS and PMOS equal.

FIVE CRITICAL VOLTAGES: V_{OL}, V_{OH}, V_{IL}, V_{IH}, V_{th} determine:

--> DC Output Voltage Behavior

--> Noise Margins

--> Width and Location of Transition Region

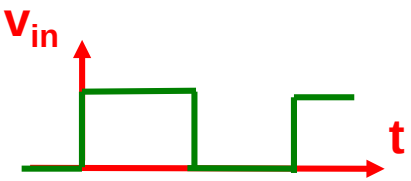


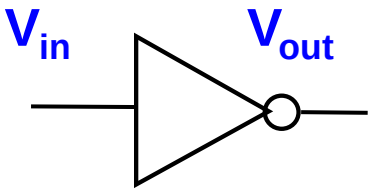
POWER DISSIPATION AND DIE AREA

Power Dissipation

P --> P_{DC}, $P_{dynamic}$

$$P_{DC} = V_{DD} I_{DC}$$





ASSUME: V_{in} = "1" 50% of Op Time, "0" 50% of Op Time

$$P_{DC} = \frac{V_{DD}}{2}\left[I_{DC}(V_{in} = "0") + I_{DC}(V_{in} = "1")\right]$$

DIE AREA --> MIN W x L and routing --> limited by design rules

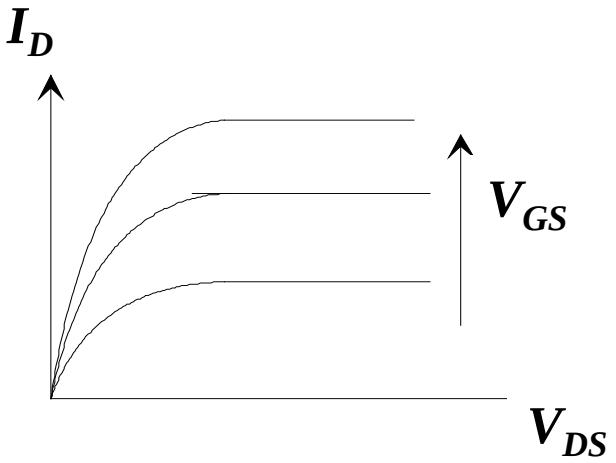
I_D vs. V_{DS} or V_{GS} Characteristics

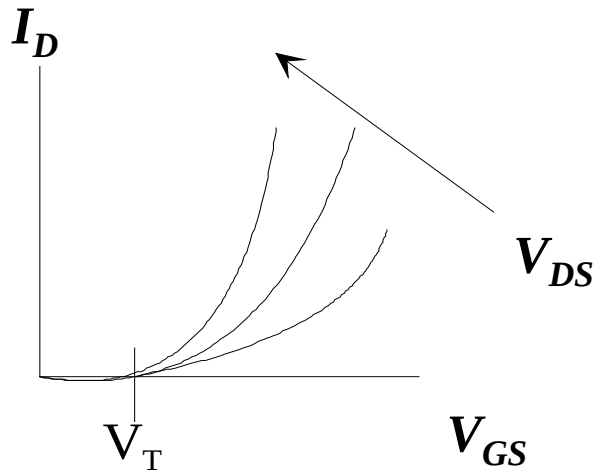
For $V_{DS} \le V_{GS} - V_T$ **&** $V_{GS} \ge V_T$,

$$I_D = \frac{\mu_n C_{Ox}}{2}\frac{W}{L}\left(2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right); \qquad \textbf{(1)}$$

for $V_{DS} \ge V_{GS} - V_T$ **&** $V_{GS} \ge V_T$,

$$I_{D,sat} = \frac{\mu_n C_{Ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2. \qquad (2)$$





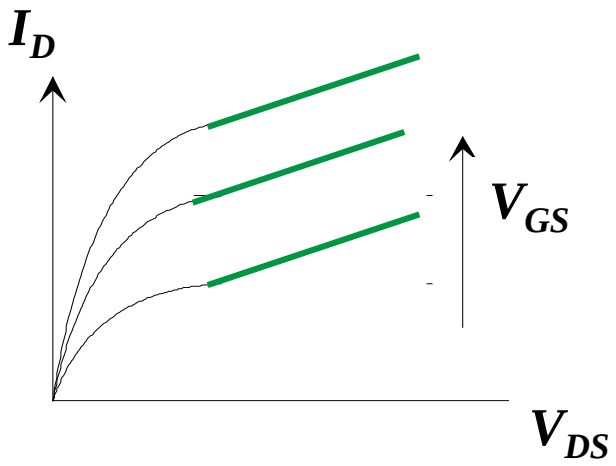
1. **The top graph is the output characteristics,**
2. **The lower one is the 'transfer characteristics'.**

I_D vs. V_{DS} or V_{GS} Characteristics

$$I_D = \frac{\mu_n C_{Ox}}{2}\frac{W}{L}\left(2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right) \qquad \textbf{(1)}$$

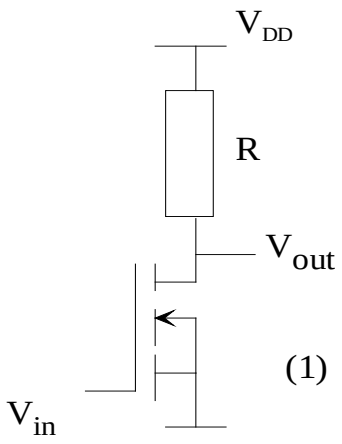
for $V_{DS} \geq V_{DS,sat}$

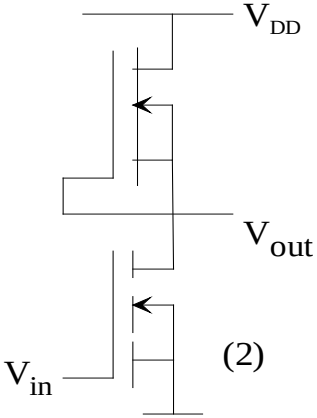
$$I_{D,sat} = \frac{\mu_n C_{Ox}}{2}\frac{W}{L-\Delta L}\left(V_{GS}-V_T\right)^2 \qquad (2)$$

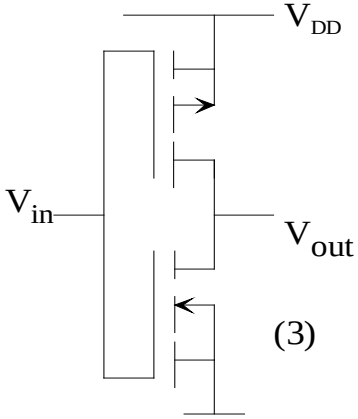


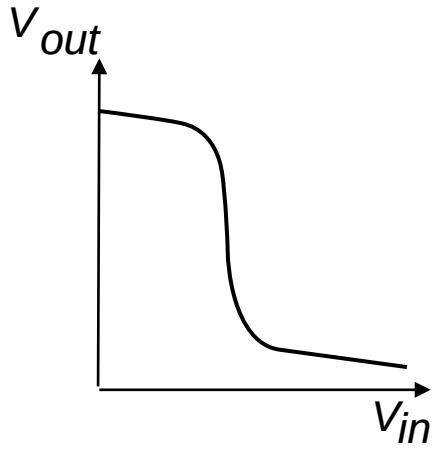
Channel length modulation

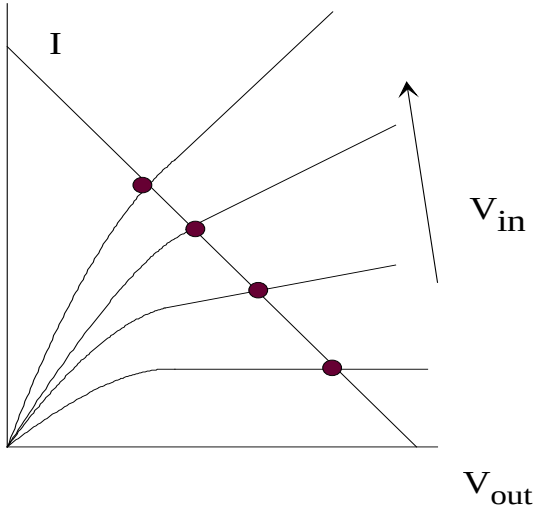
How to obtain VTC (V_{in} & V_{out})

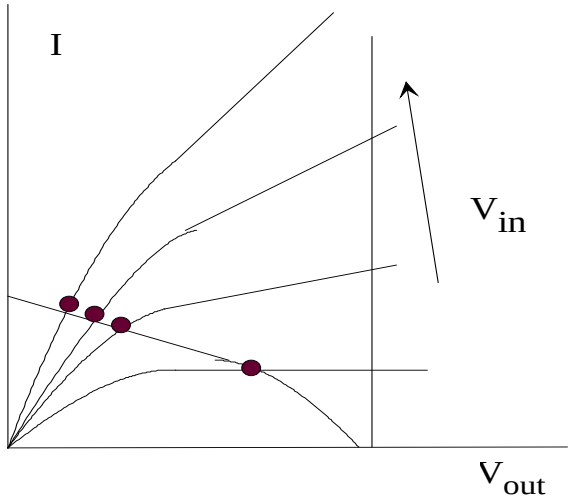


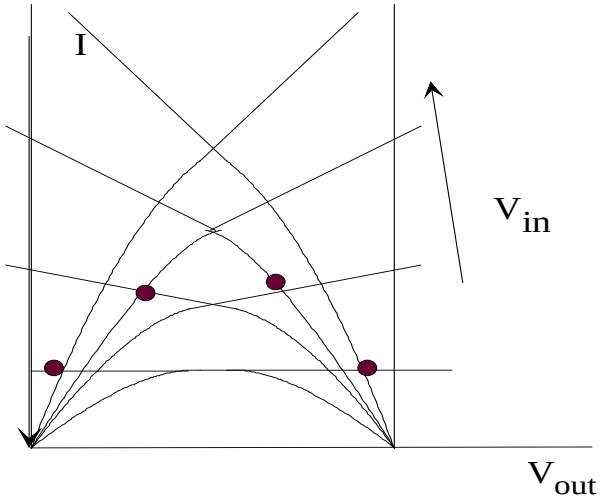












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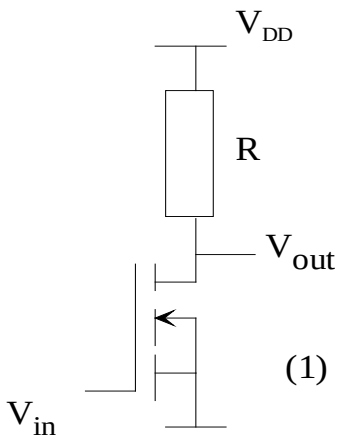
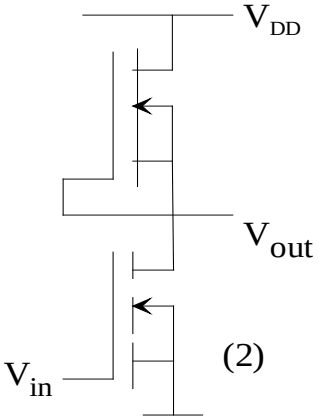
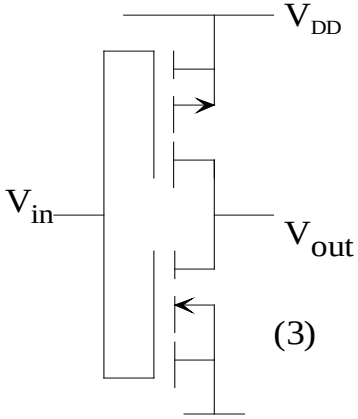
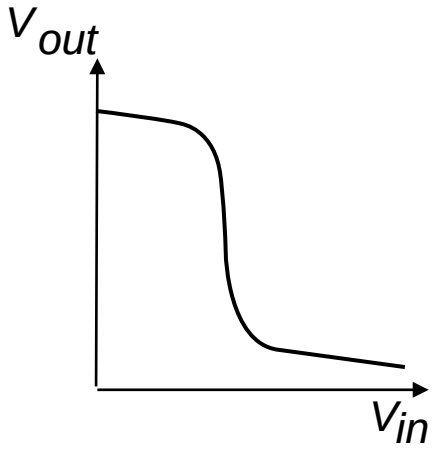
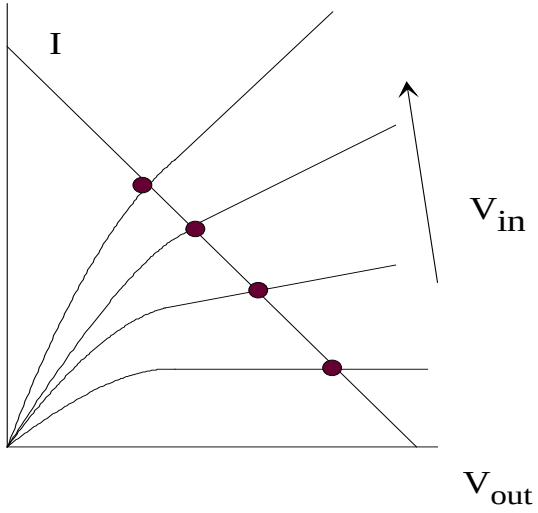


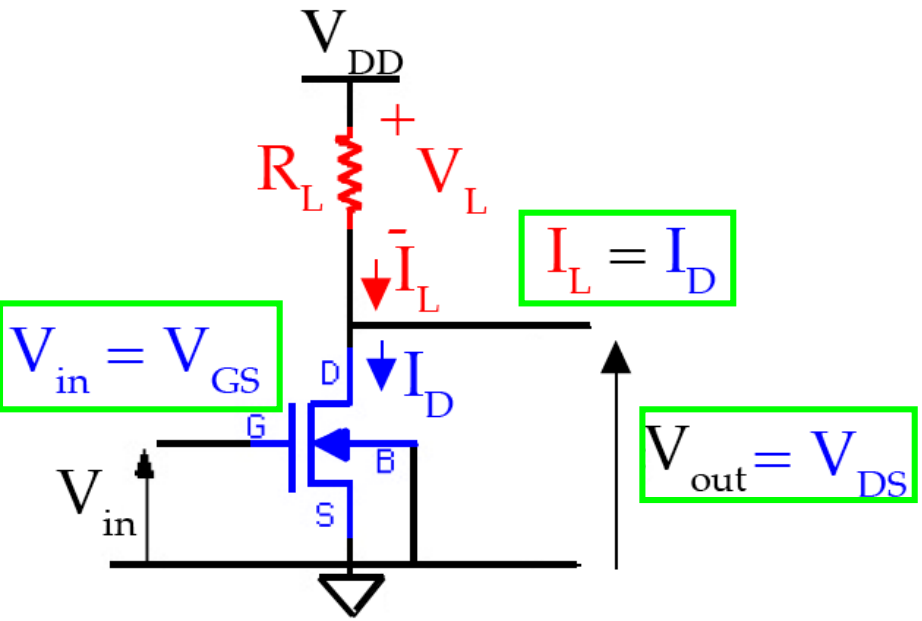








RESISTIVE-LOAD INVERTER



If $V_{in} > V_{T0n}$ and

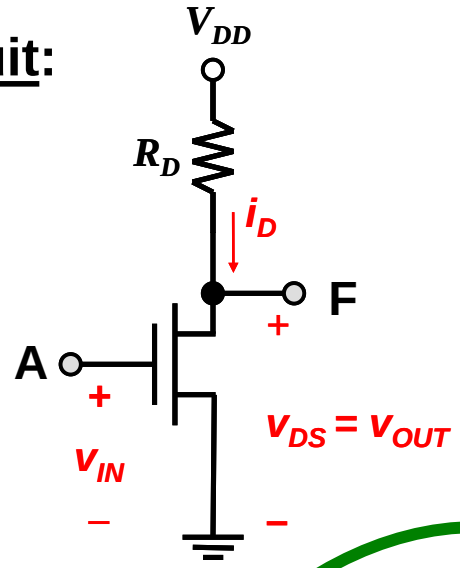
$V_{out} < V_{in} - V_{T0n}$, it is then in linear region.

If $V_{in} > V_{T0n}$ and

$V_{out} > V_{in} - V_{T0n}$, it is then saturation mode.

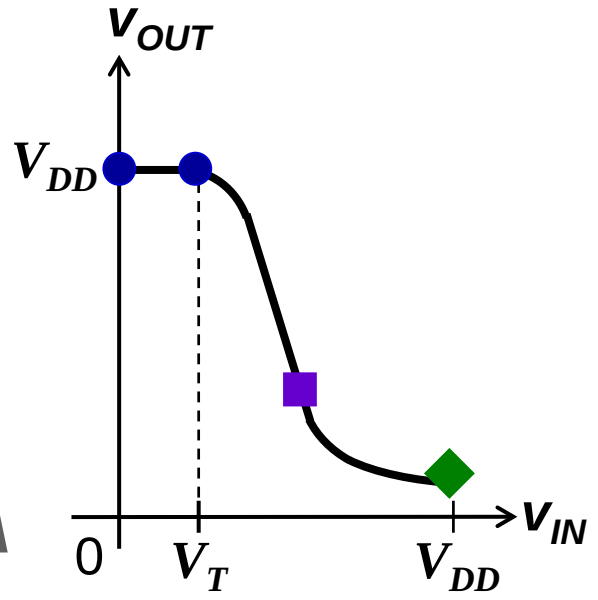
NMOS Inverter: Load Line

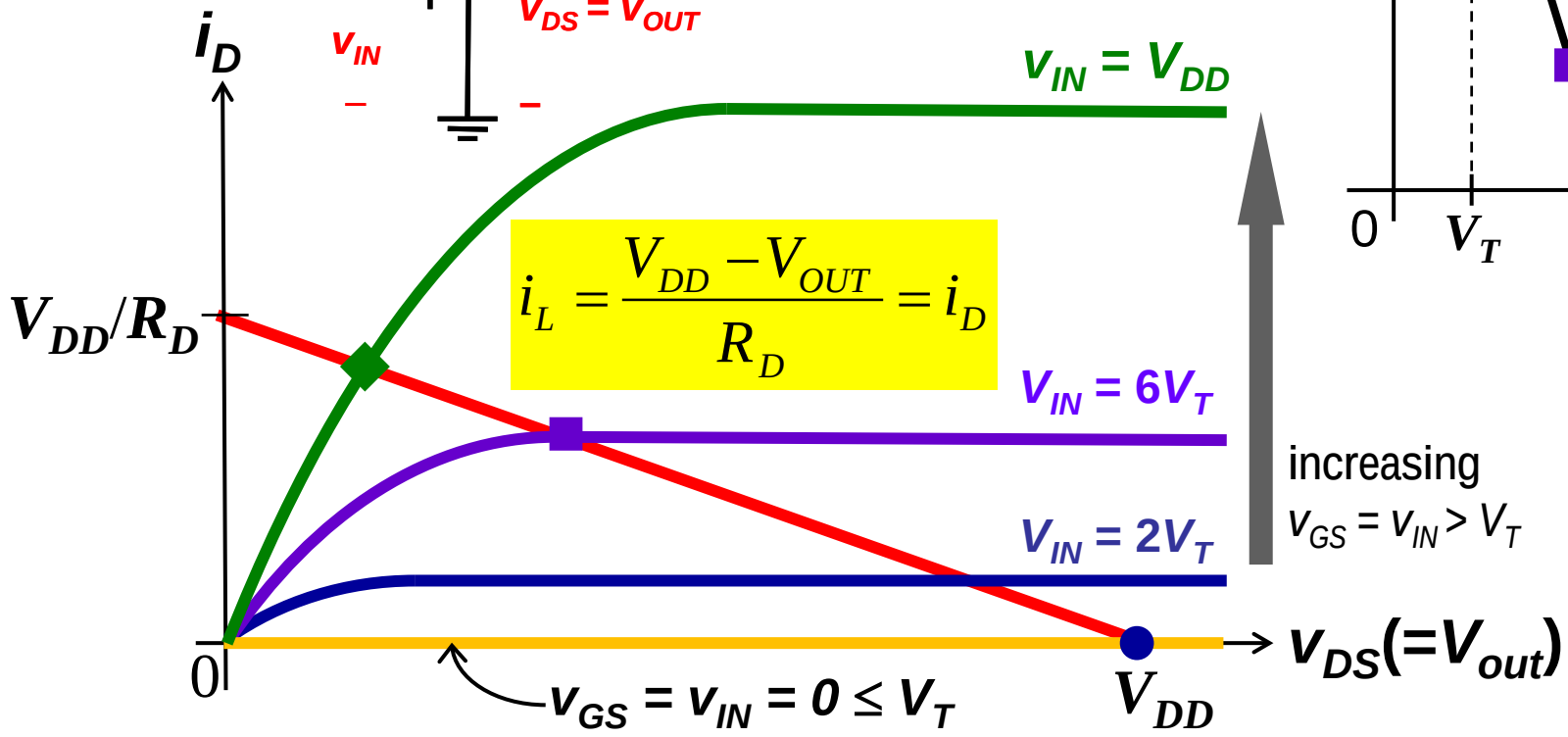
Circuit:



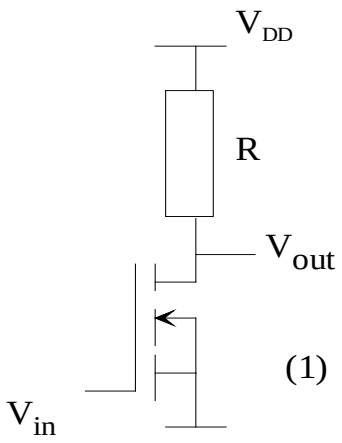
A	F
0	1
1	0

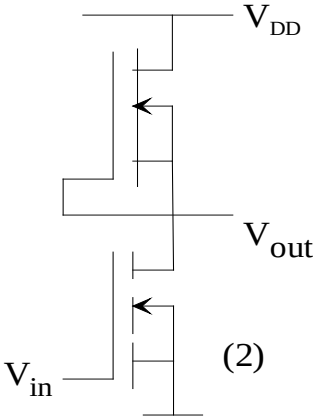
Voltage-Transfer Characteristics

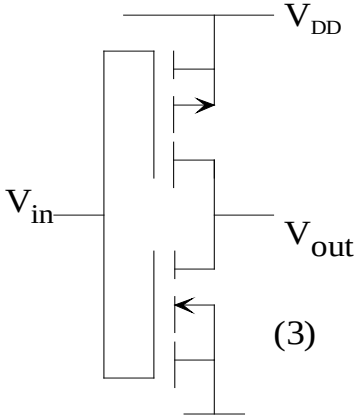


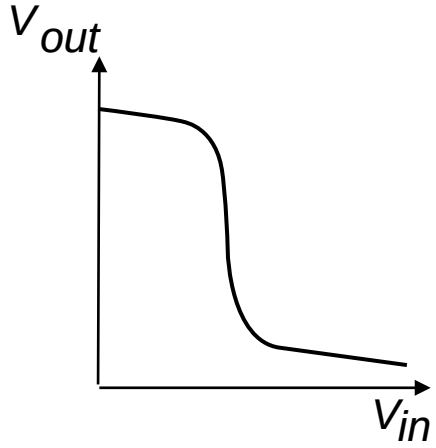


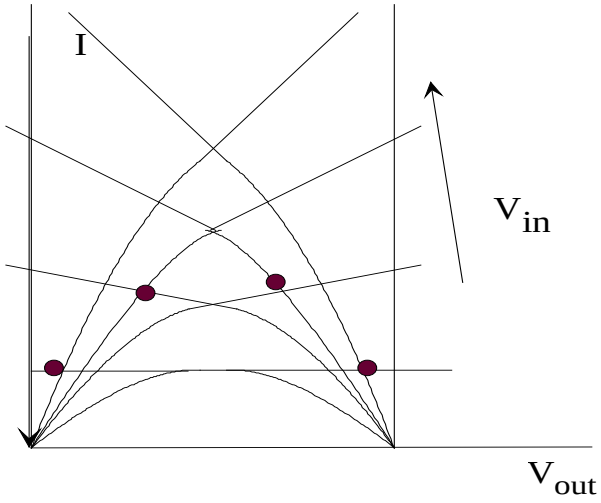
How to obtain VTC (V_{in} & V_{out})



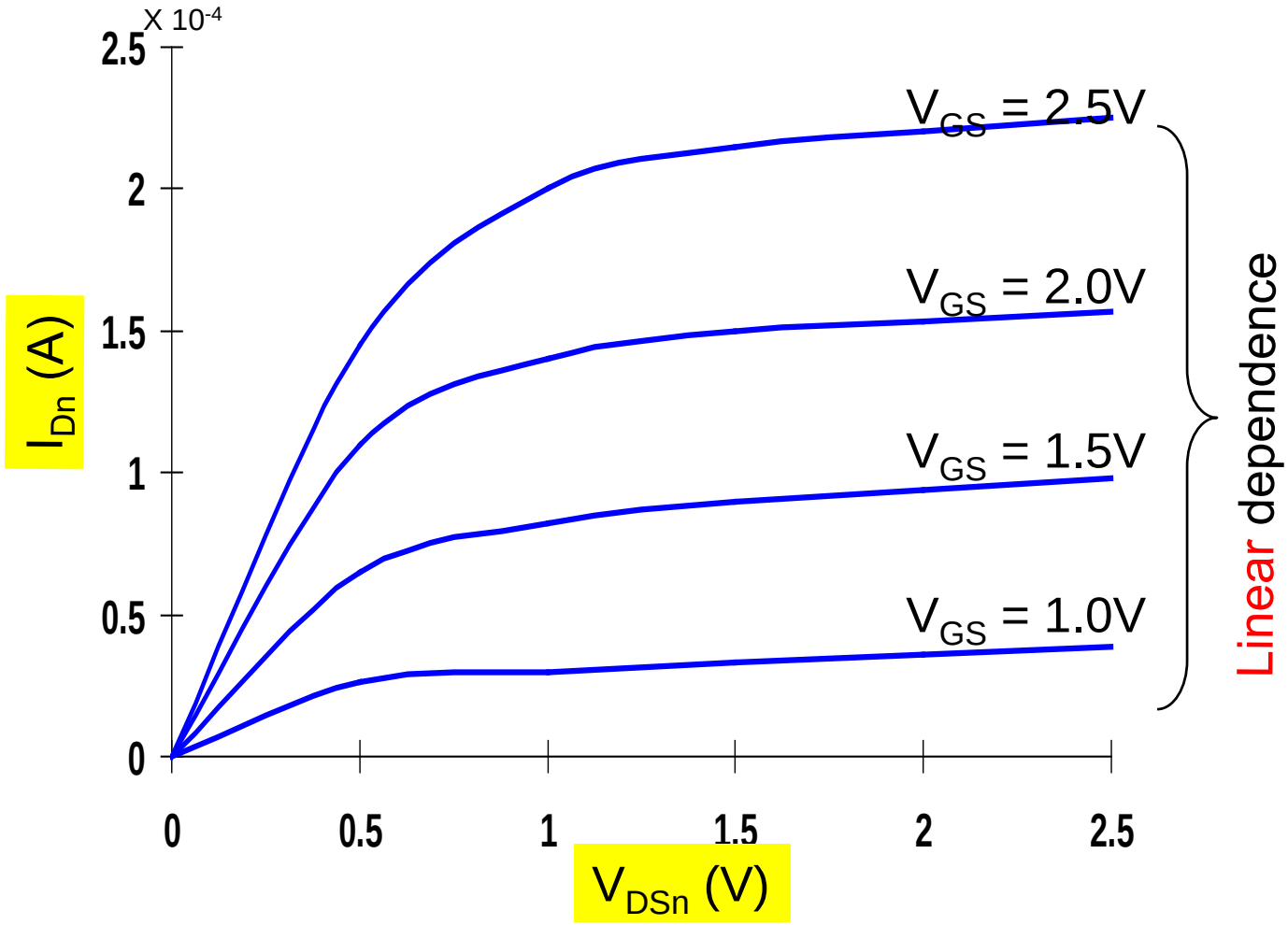








Review: I-V Plot (NMOS)

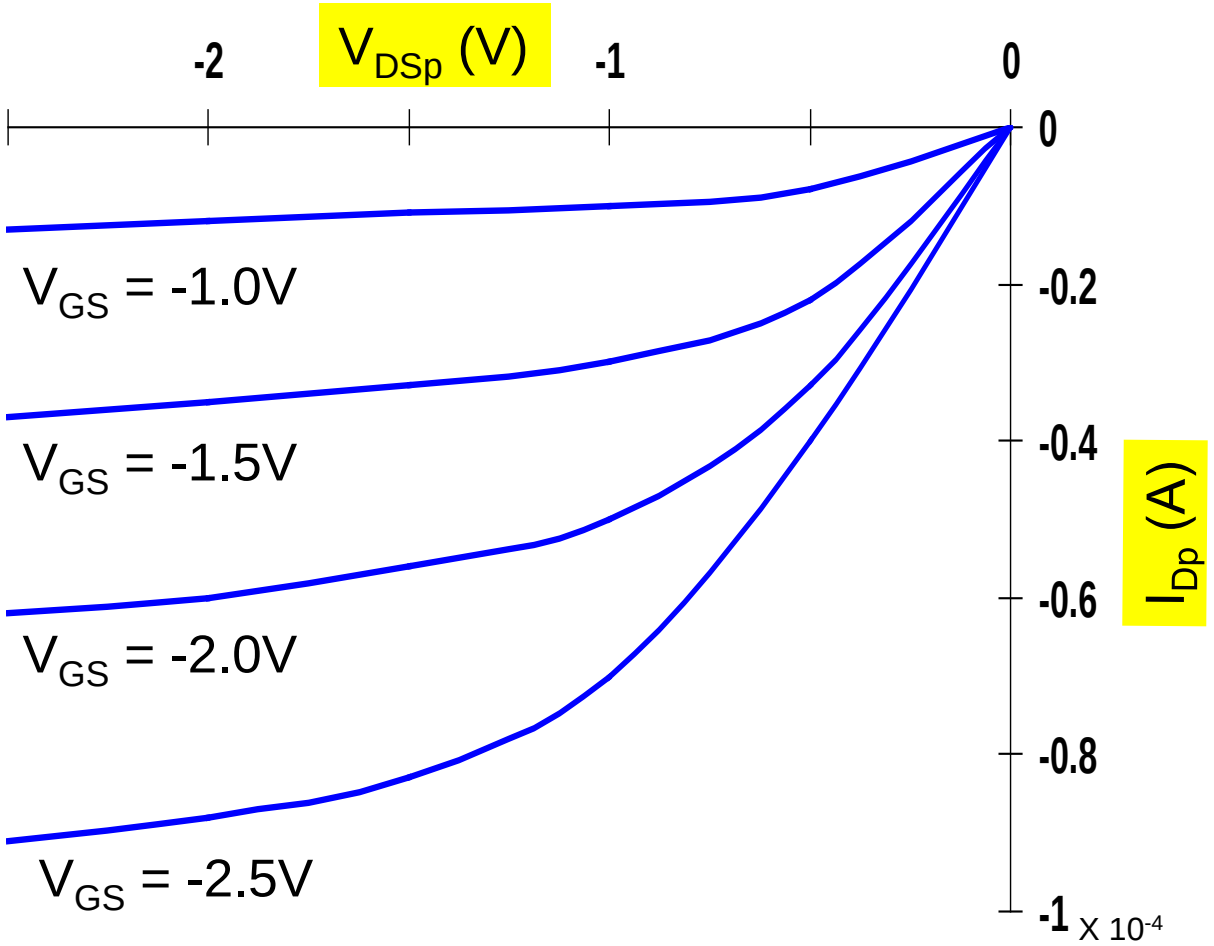


$I_{Dn} \sim V_{DSn}$

$V_{DD} = 2.5V, V_T = 0.4V$

Review: I-V Plot (PMOS)

- All polarities of all voltages and currents are reversed



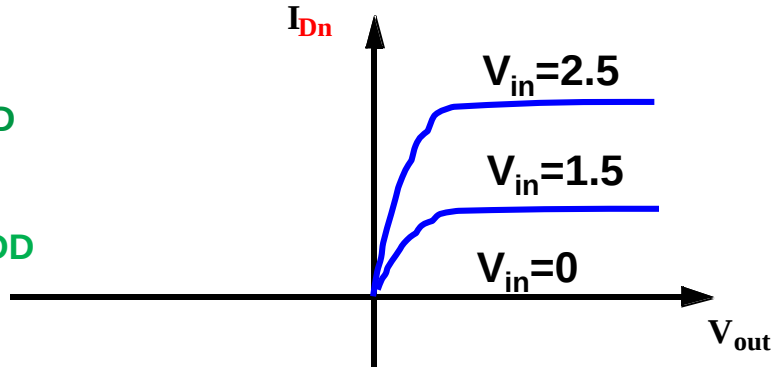
$I_{Dp} \sim V_{DSp}$

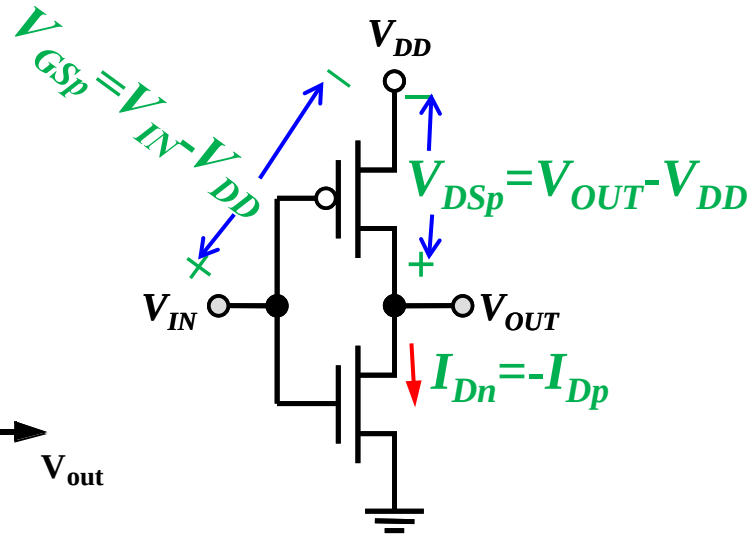
V_{DD} = 2.5V, V_T = -0.4V

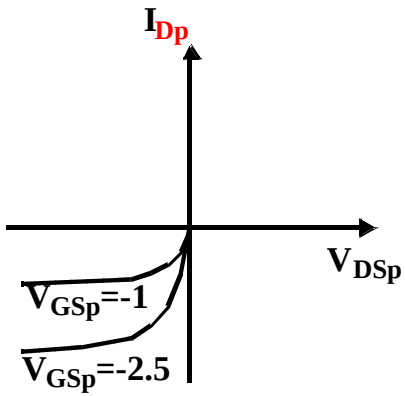
Transforming PMOS I-V Lines

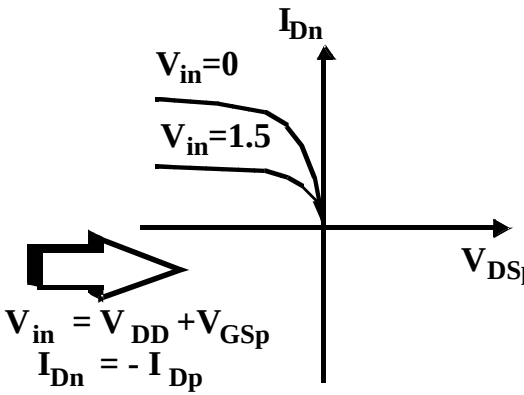
- Have a common coordinate set V_{in}, V_{out}, and I_{Dn}

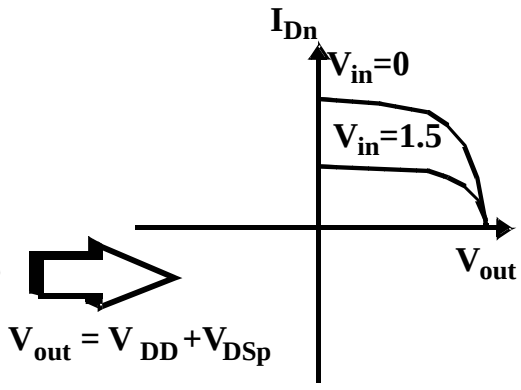
$I_{Dp} = -I_{Dn}$
$V_{GSn} = V_{in}$
$V_{GSp} = V_{in} - V_{DD}$
$V_{DSn} = V_{out}$
$V_{DSp} = V_{out} - V_{DD}$





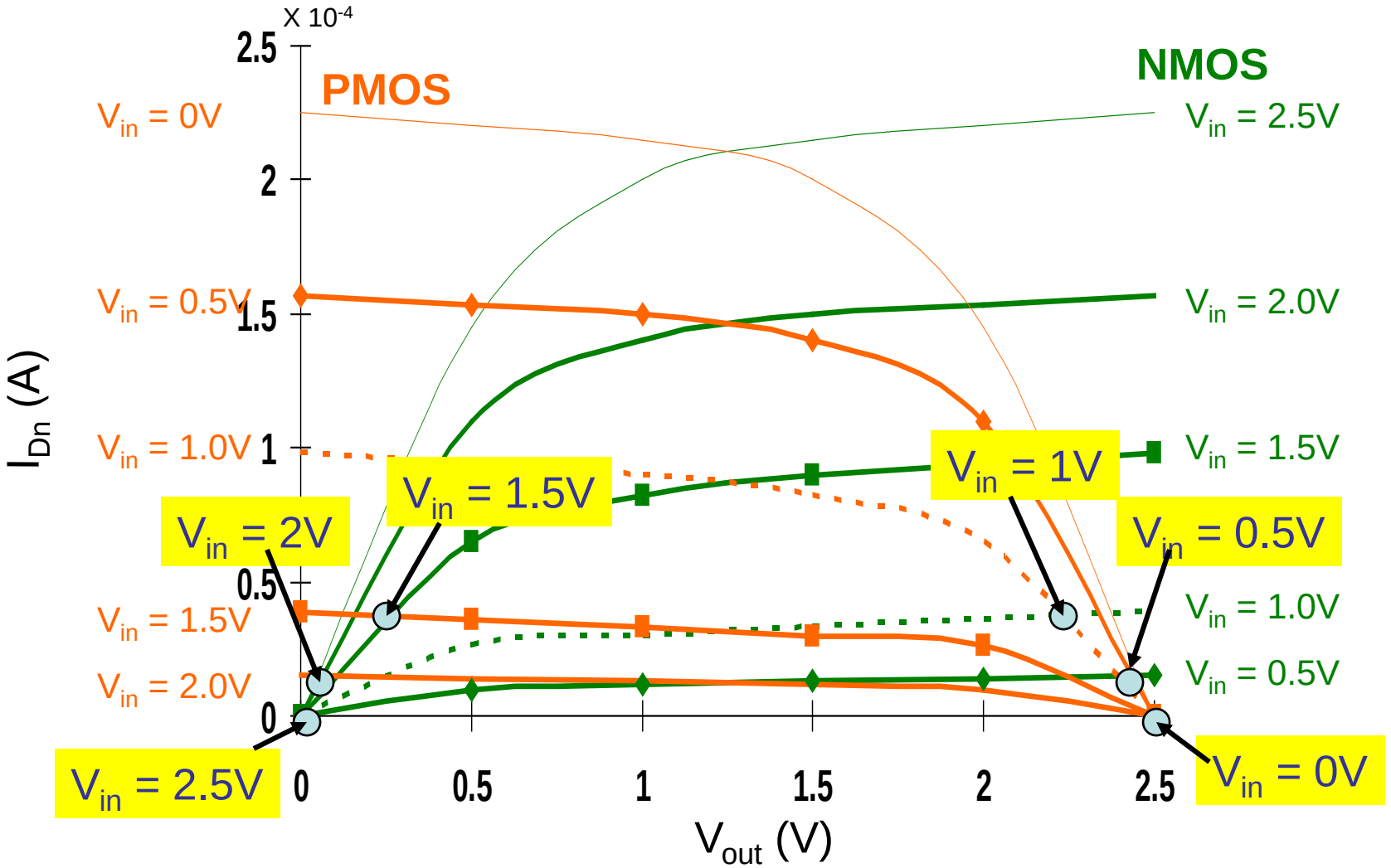






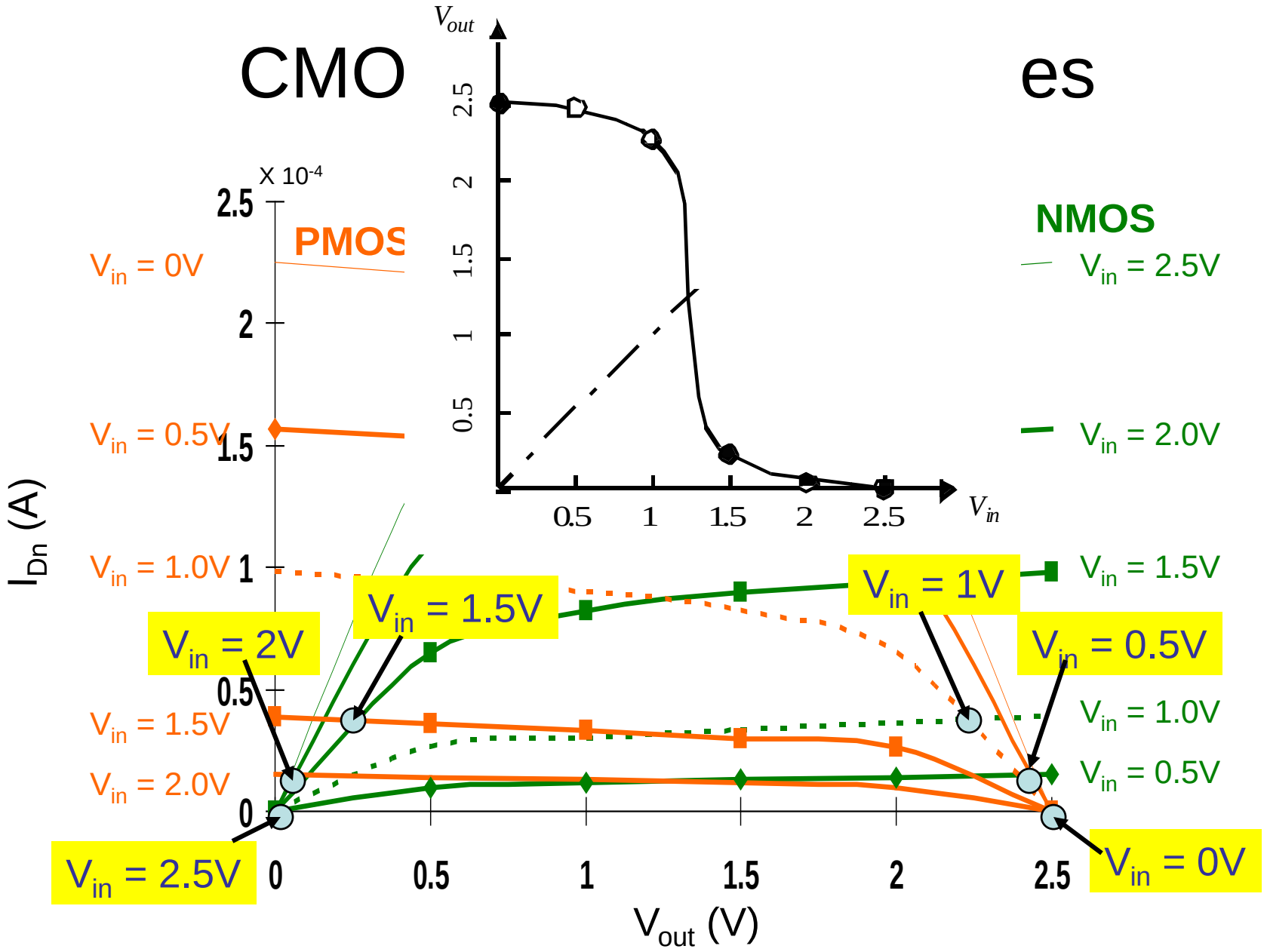
Mirror around x-axis **Horiz. shift over V_{DD}**

CMOS Inverter Load Lines



0.25um, $W/L_n = 1.5$, $W/L_p = 4.5$, $V_{DD} = 2.5V$, $V_{Tn} = 0.4V$, $V_{Tp} = -0.4V$

CMO es

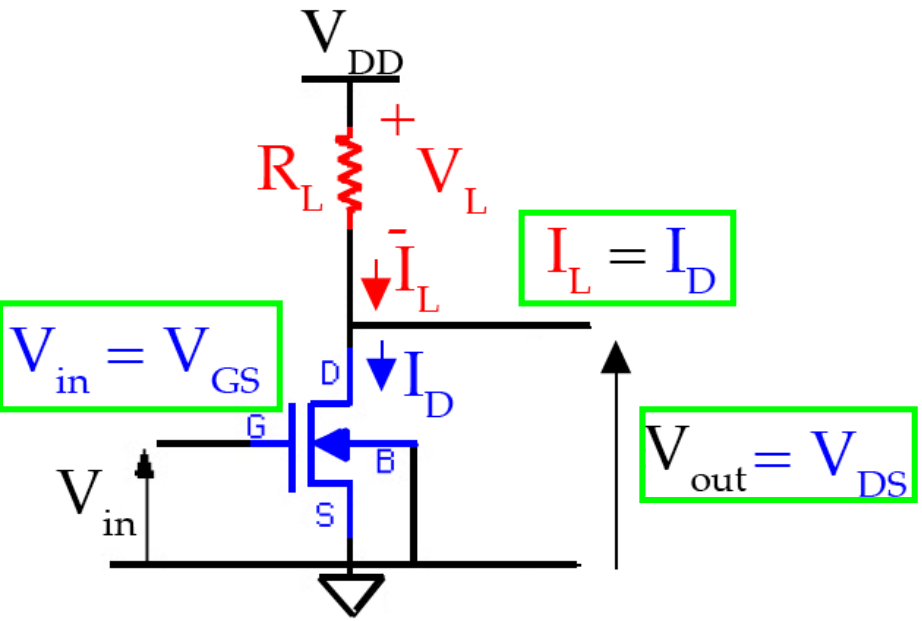


0.25um, W/L_n = 1.5, W/L_p = 4.5, V_{DD} = 2.5V, V_{Tn} = 0.4V, V_{Tp} = -0.4V

outline

- Voltage transfer characteristic (VTC)
- **nMOS inverters**
  - Resistive load inverter
  - Saturated enhancement load inverter
- CMOS inverter
  - CMOS VTC
  - Comparison of CMOS and MOS inverters
- Ratioed Logic
- Combinational CMOS logic gates (static)

RESISTIVE-LOAD INVERTER



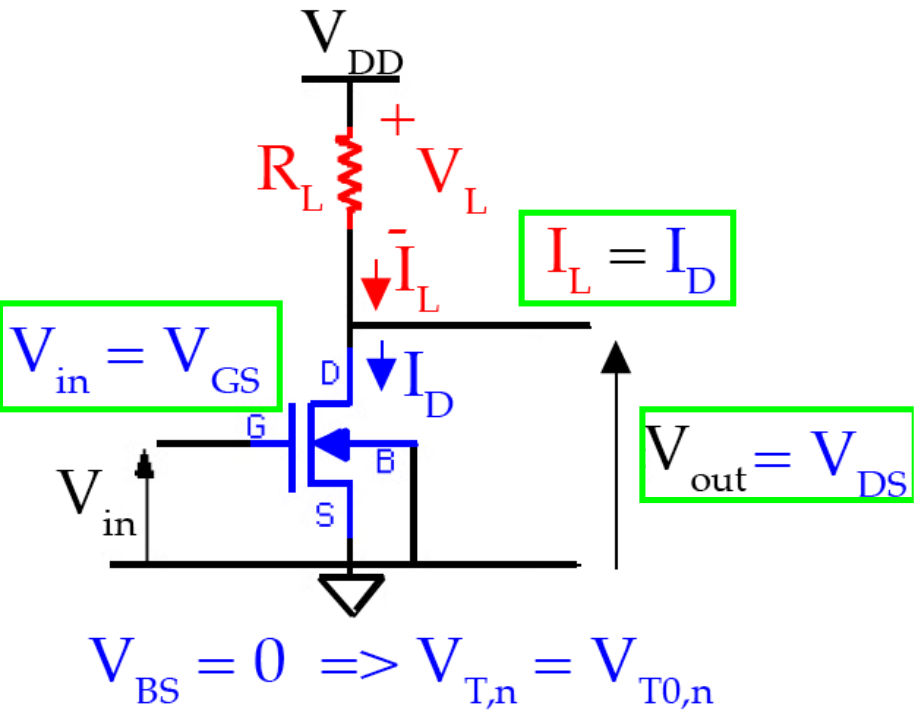
If $V_{in} > V_{T0n}$ and

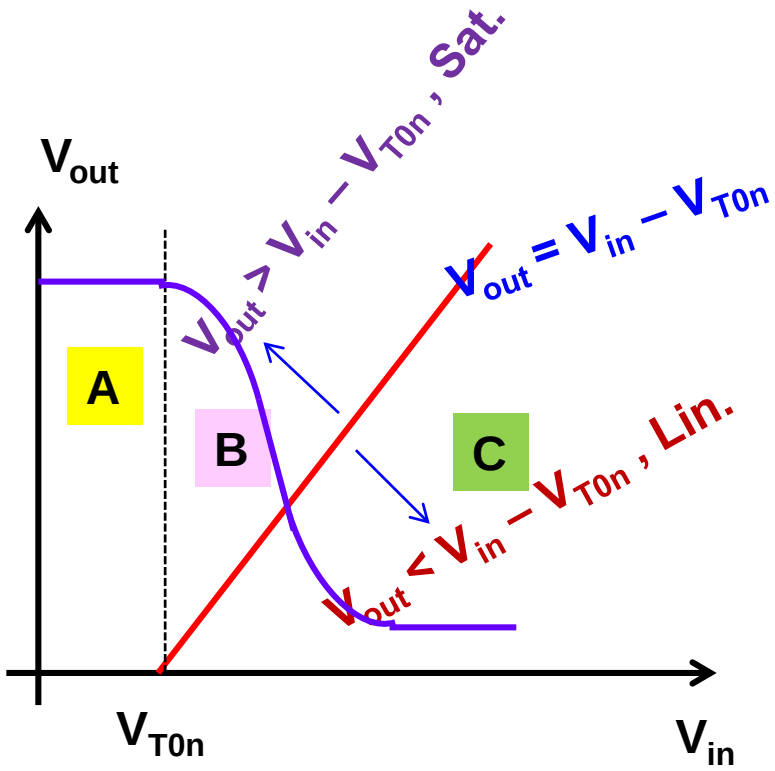
$V_{out} < V_{in} - V_{T0n}$, it is then in linear region.

If $V_{in} > V_{T0n}$ and

$V_{out} > V_{in} - V_{T0n}$, it is then saturation mode.

RESISTIVE-LOAD INVERTER



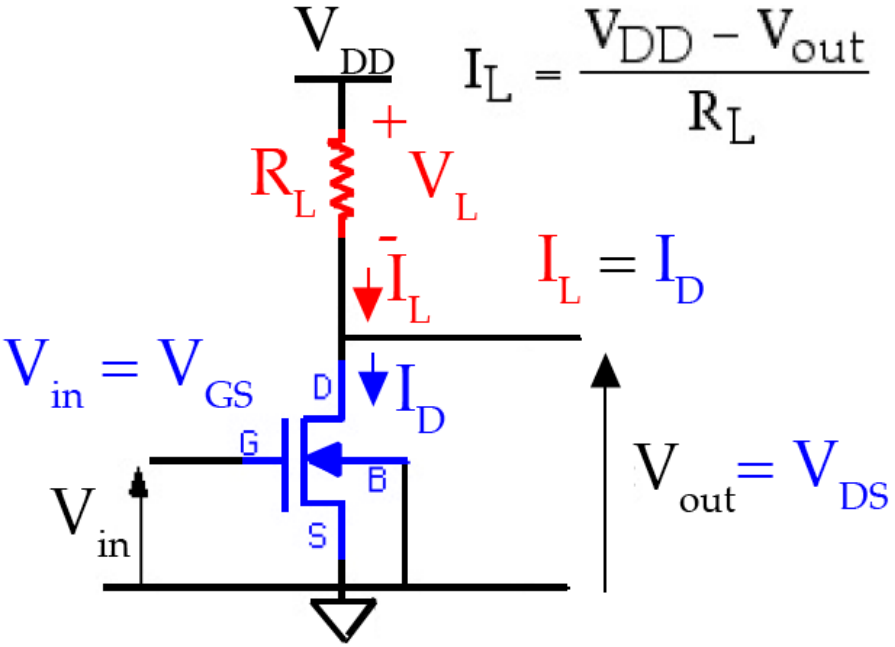


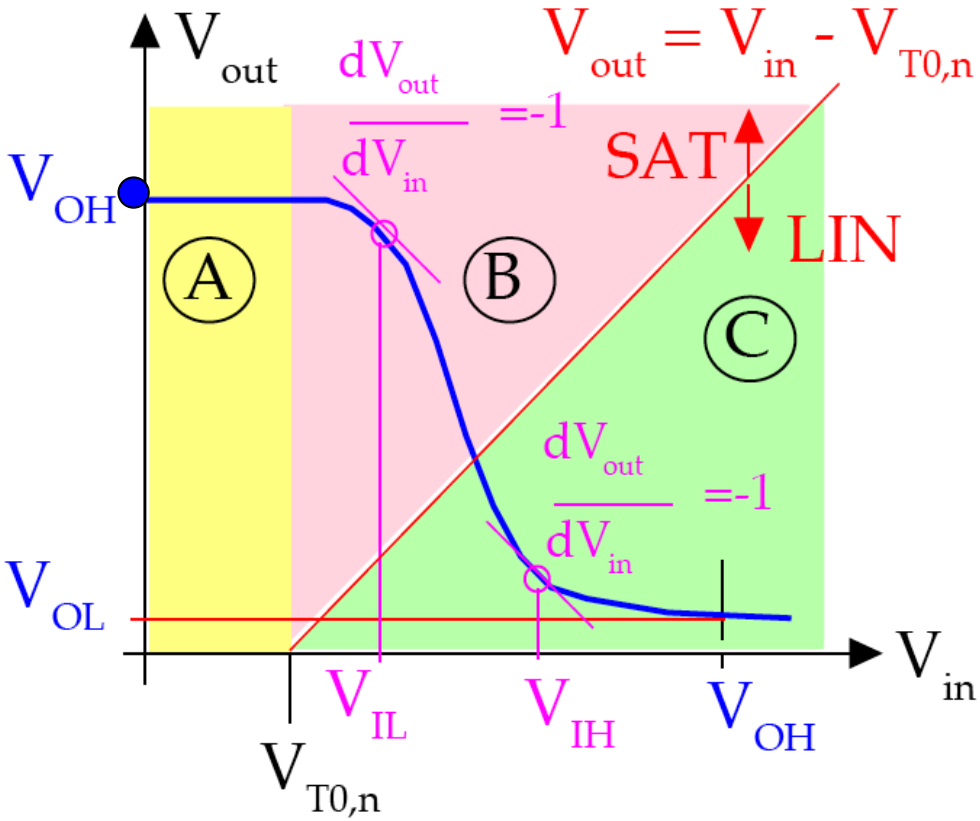
If $V_{in} > V_{T0n}$ and

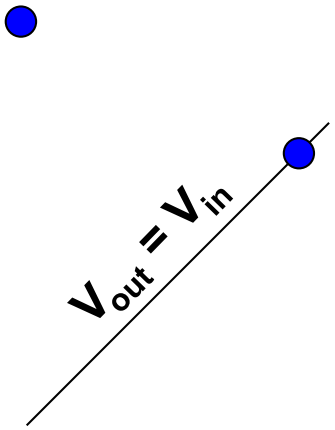
$V_{out} < V_{in} - V_{T0n}$, it is then in linear region.

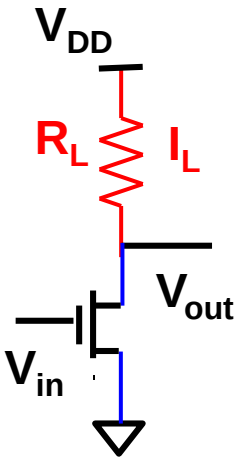
If $V_{in} > V_{T0n}$ and

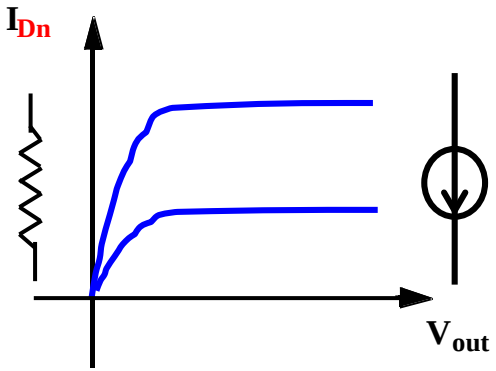
$V_{out} > V_{in} - V_{T0n}$, it is then saturation mode.

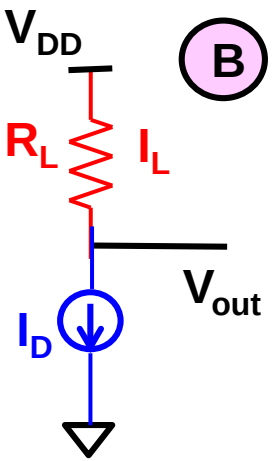

V DD
I L = V DD − V out / R L
+
R L
V L
-
I L
I L = I D
V in = V GS
D
I D
G
B
V in
S
V out = V DS

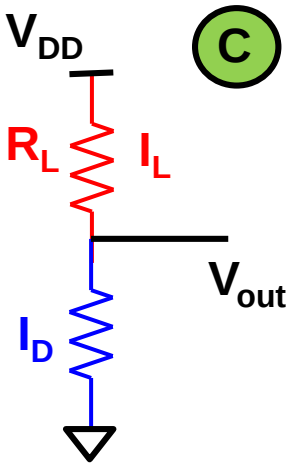

V out
dV out / dV in =-1
V out = V in - V T0,n
SAT
LIN
V OH
A
B
C
dV out / dV in =-1
V OL
V in
V IL
V IH
V OH
V T0,n

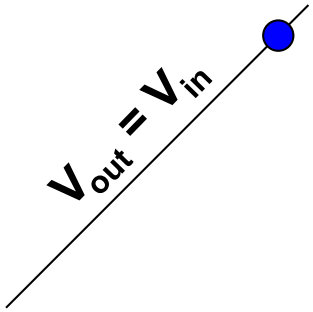

$V_{out} = V_{in}$


V_{DD}
R_L
I_L
V_{out}
V_{in}

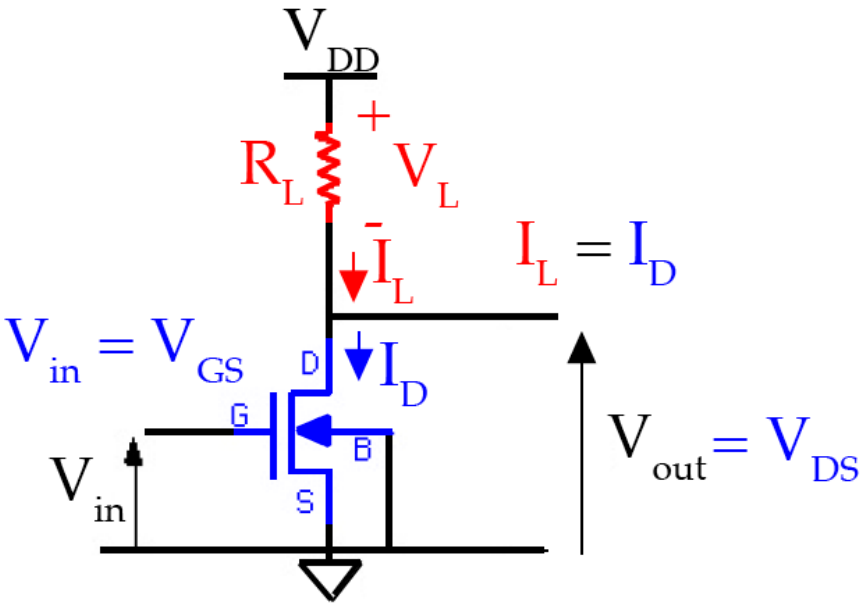

I_{Dn}
V_{out}


V_{DD}
B
R_L
I_L
V_{out}
I_D

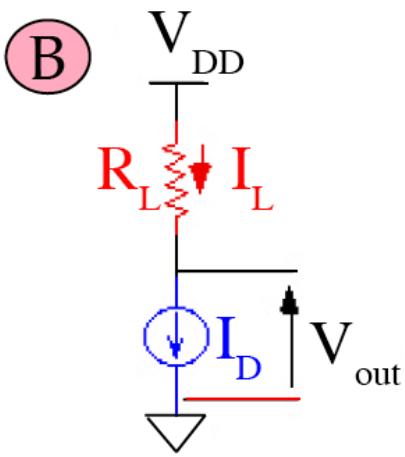

V_{DD}
C
R_L
I_L
V_{out}
I_D

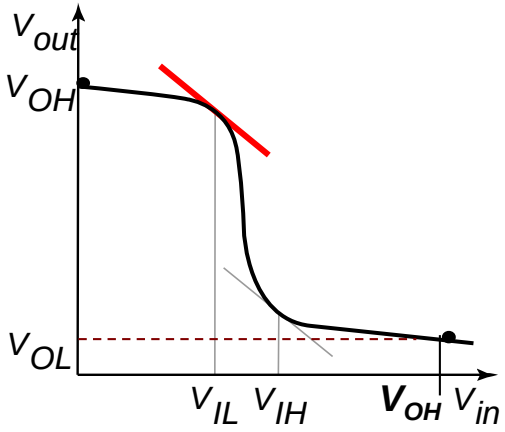

$V_{out} = V_{in}$

CALCULATION OF V_{IL}: B

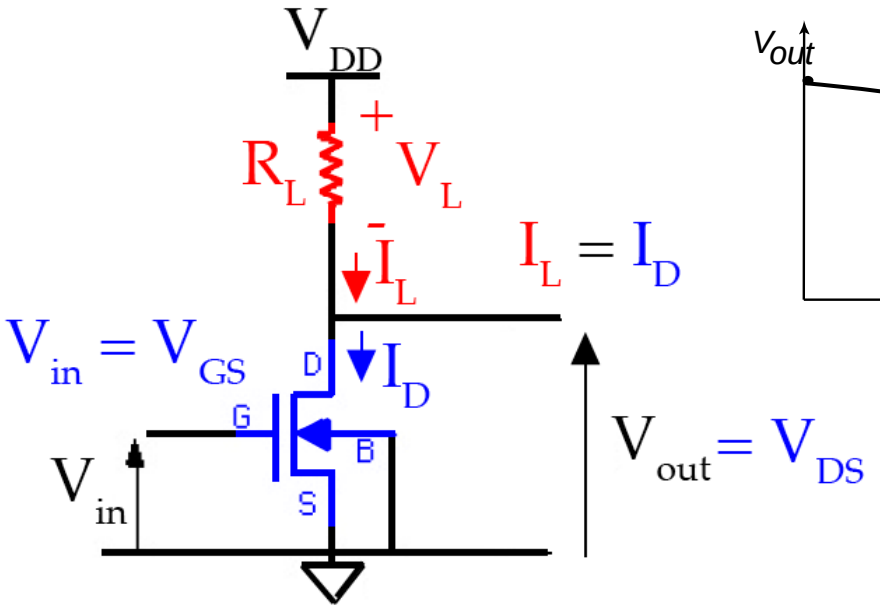


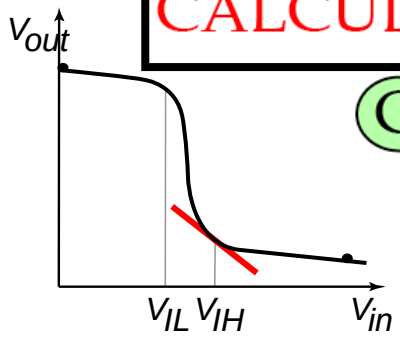
$$\frac{dV_{out}}{dV_{in}} = -1 \quad @\ V_{in} = V_{IL}^{-}$$



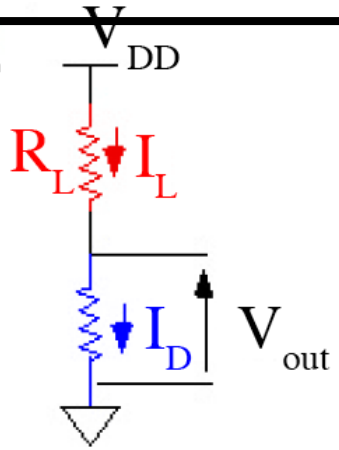


CALCULATION OF V_{IH}: C



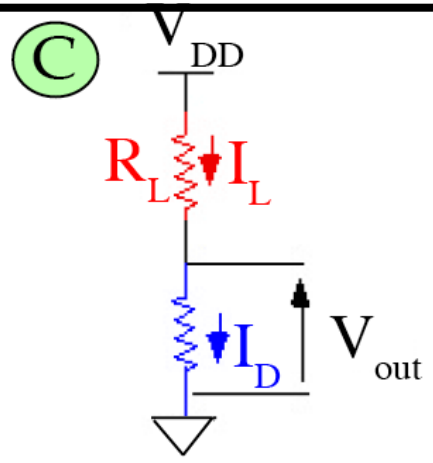


C



$$\frac{dV_{out}}{dV_{in}} = -1 \quad @\ V_{in} = V_{IH}$$

CALCULATION OF V_{IH}: C



Find $V_{out}(V_{in} = V_{IH})$:

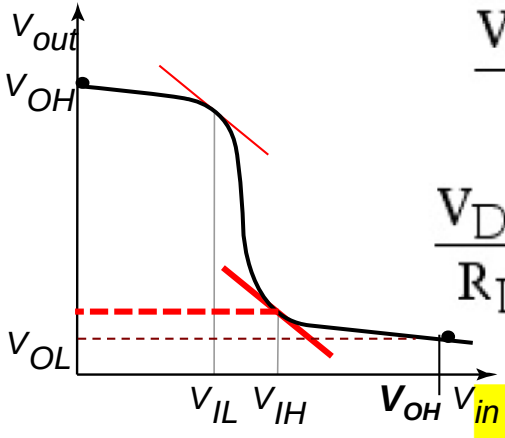
$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2}\left[2(V_{IH} - V_{T0,n})V_{out} - V_{out}^2\right]$$

where

$$V_{IH} = V_{T0,n} + 2V_{out} - \frac{1}{k_n R_L}$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2}\left[2(V_{T0,n} + 2V_{out} - \frac{1}{k_n R_L} - V_{T0,n})V_{out} - V_{out}^2\right]$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2}\left[3V_{out}^2 - \frac{2V_{out}}{k_n R_L}\right]$$



$$\frac{V_{DD}}{R_L} = \frac{3}{2}k_n V_{out}^2 \longrightarrow V_{out}(V_{in} = V_{IH}) = \sqrt{\frac{2}{3}\frac{V_{DD}}{k_n R_L}}$$

$$V_{IH} = V_{T0,n} + 2\sqrt{\frac{2}{3}\frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}$$

CALCULATION OF V_{th}:

$$V_{in} = V_{out} = V_{th} \Rightarrow V_{DS} = V_{GS} > V_{GS} - V_{T0,n} \longrightarrow \text{B}$$

SUMMARY - RESISTIVE LOAD INVERTER

$$V_{th} = V_{T0,n} - \frac{1}{k_n R_L} + \sqrt{\left(V_{T0,n} - \frac{1}{k_n R_L}\right)^2 + \frac{2V_{DD}}{k_n R_L} - V_{T0,n}^2}$$

$$V_{IL} = V_{T0,n} + \frac{1}{k_n R_L}$$

$$V_{IH} = V_{T0,n} + 2\sqrt{\frac{2}{3}\frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}$$

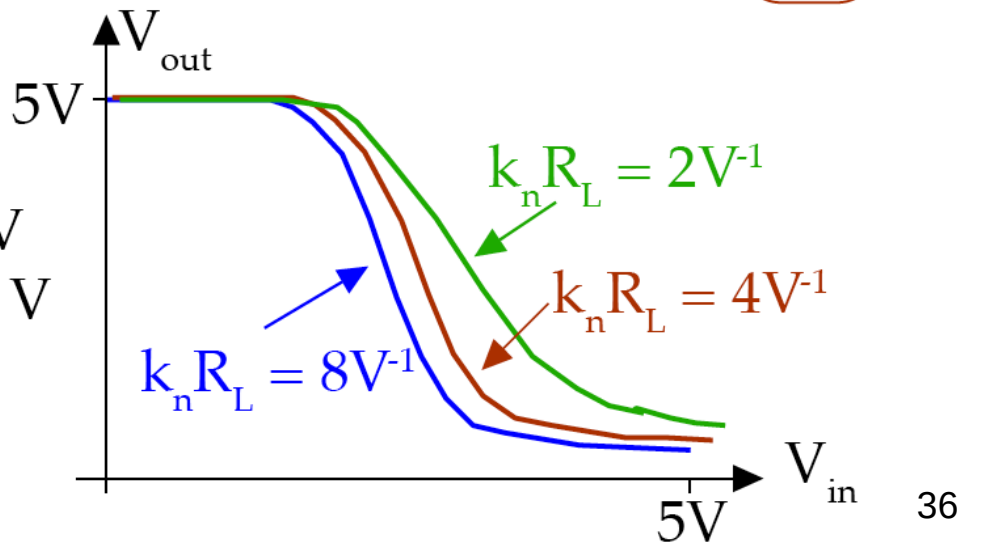
$$V_{OL} = V_{DD} - V_{T0,n} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0,n} + \frac{1}{k_n R_L}\right)^2 - \frac{2}{k_n R_L}V_{DD}}$$

$$V_{OH} = V_{DD}$$

$$k_n = C_{ox}\mu_n\left(\frac{W}{L}\right)_n$$

$V_{DD} = 5V$

$V_{T0,n} = 1\ V$



Disadvantages of NMOS Logic Gates

- Large values of $\boldsymbol{R_L}$ are required in order to
  - achieve a low value of V_{OL}
  - keep power consumption low

→ Large resistors are needed, but these take up a lot of space.

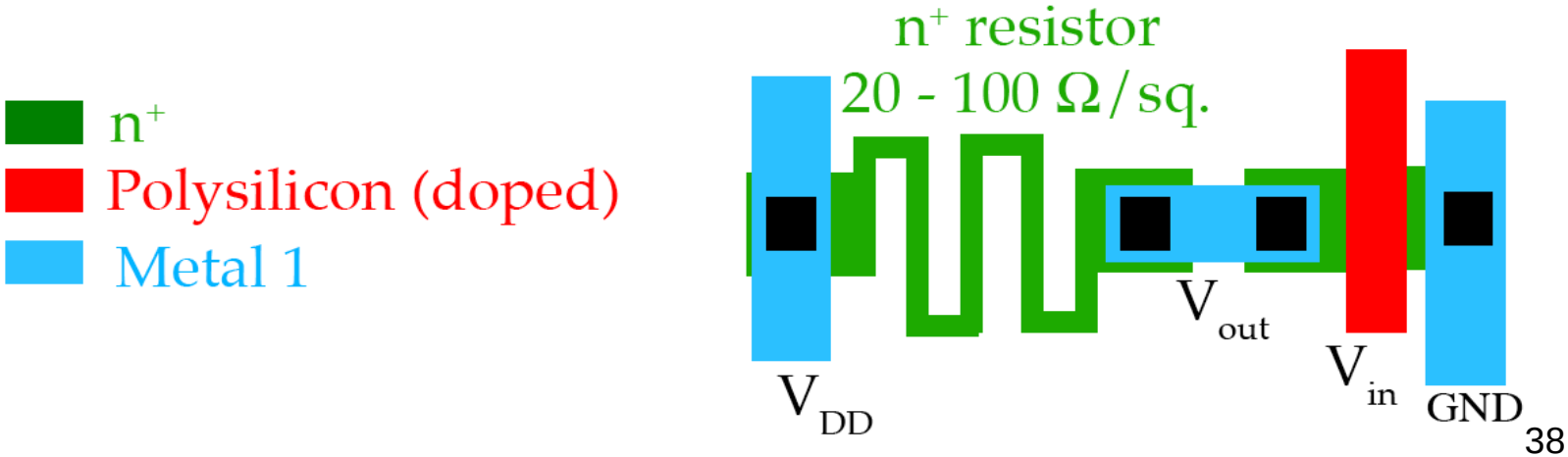
- One solution is to replace the resistor with an NMOSFET that is always on.

$$t_{pLH} = 0.69 R_L C_L \qquad t_{pHL} = 0.69 (R_L \,//\, R_{PND}) C_L$$

EXAMPLE 5.1 Cont.

$$\frac{W}{L}R_L = 2.05 \times 10^5 \Omega$$

(W/L) - RATIO	R_L [kΩ]	P_{DC}(average) [μW]
1	205.0	58.5
2	102.5	117.1
3	68.4	175.4
4	51.3	233.9
5	41.0	292.7
6	34.2	350.8



EXAMPLE 5.2

Consider a resistive-load inverter with

$V_{DD} = 5\ V,\ k_n' = 20\ \mu A/V^2,\ V_{T0n} = 0.8\ V,\ R_L = 200\ k\Omega,\ W/L = 2$

Calculate the critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) on the VTC and determine the noise margins.

$$V_{OH} = V_{DD} = 5\ V$$

$$k_n = k_n'(W/L) = 40\ \mu A/V^2 \Rightarrow k_n R_L = 8\ V^{-1}$$

$$\rightarrow V_{OL} = V_{DD} - V_{T0,n} + \frac{1}{k_n R_L} \pm \sqrt{\left(V_{DD} - V_{T0,n} + \frac{1}{k_n R_L}\right)^2 - \frac{2}{k_n R_L} V_{DD}}$$

$$V_{OL} = 0.147\ V$$

$$\rightarrow V_{IL} = V_{T0,n} + \frac{1}{k_n R_L}$$

$$V_{IL} = 0.925\ V$$

EXAMPLE 5.2 Cont.

Consider a resistive-load inverter with

$V_{DD} = 5\ V,\ k_n' = 20\ \mu A/V^2,\ V_{T0n} = 0.8\ V,\ R_L = 200\ k\Omega,\ W/L = 2$

Calculate the critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) on the VTC and determine the noise margins.

$$\rightarrow\ V_{IH} = V_{T0,n} + 2\sqrt{\frac{2}{3}\frac{V_{DD}}{k_n R_L} - \frac{1}{k_n R_L}}$$

$V_{IH} = 1.97\ V$

$V_{OH} = V_{DD} = 5\ V$

$V_{OL} = 0.147\ V$

$V_{IL} = 0.925\ V$

$NM_H = V_{OH} - V_{IH} = 5V - 1.97V = 3.03V$

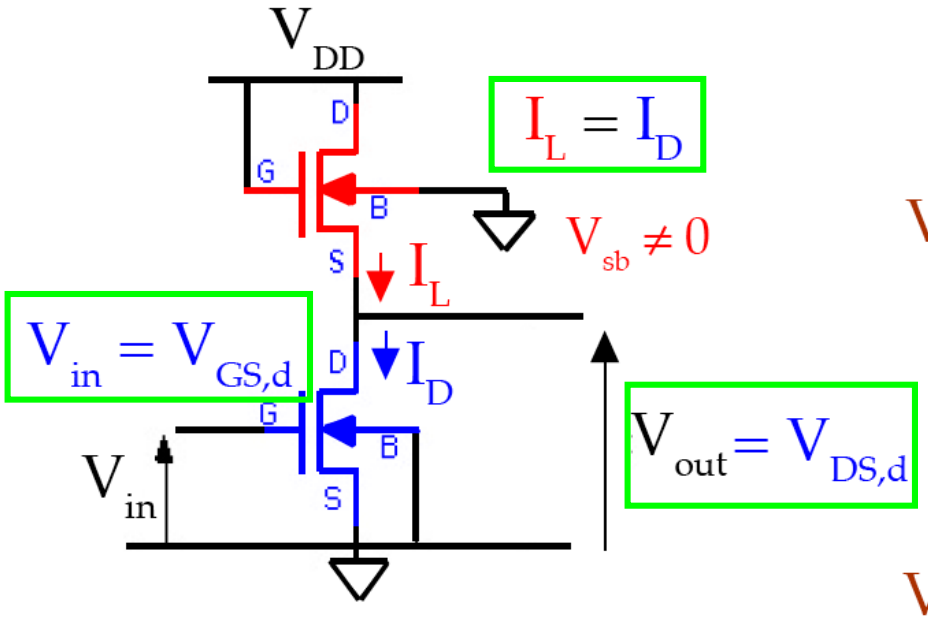
$NM_L = V_{IL} - V_{OL} = 0.93V - 0.15V = 0.78V$

GOOD DESIGN => $NM_L > V_{DD}/4 = 1.25\ V$

outline

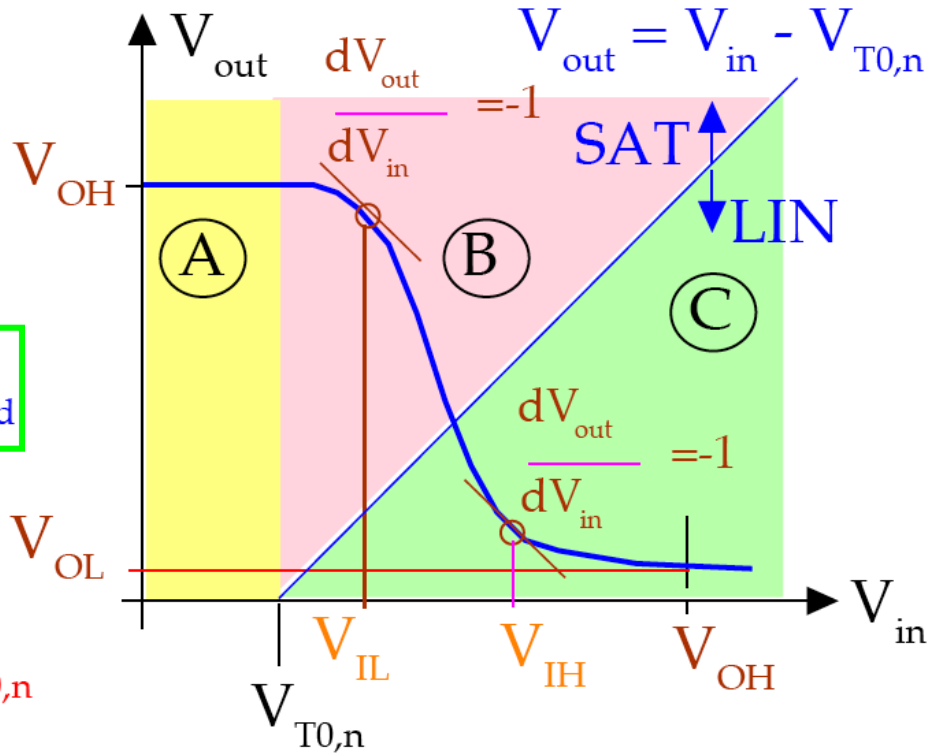
- Voltage transfer characteristic (VTC)
- **nMOS inverters**
  - Resistive load inverter
  - **Saturated enhancement load inverter**
- CMOS inverter
  - CMOS VTC
  - Comparison of CMOS and MOS inverters
- Ratioed Logic
- Combinational CMOS logic gates (static)

SATURATED ENHANCEMENT-LOAD INVERTER



$V_{BS,d} = 0 \Rightarrow V_{T,d} = V_{T0,n}$

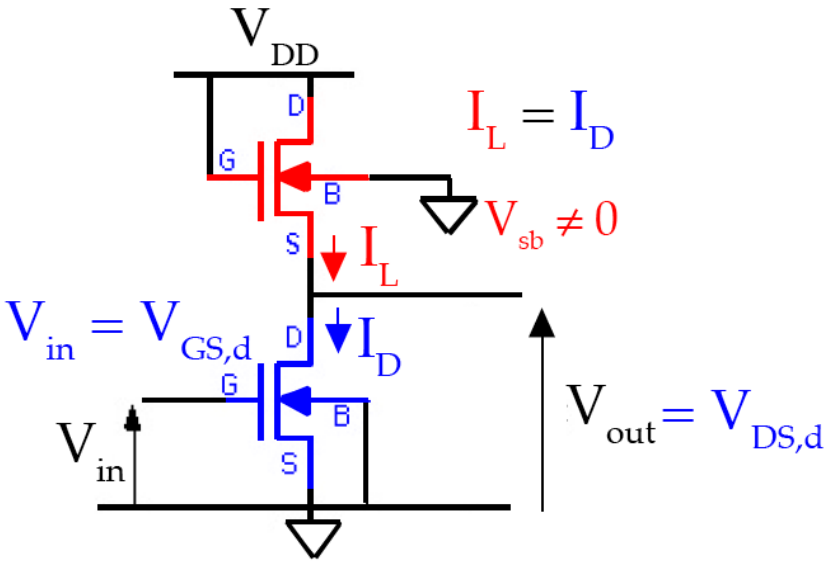
$V_{BS,L} = -V_{out} < 0 \Rightarrow V_{T,L} \neq V_{T0,n}$

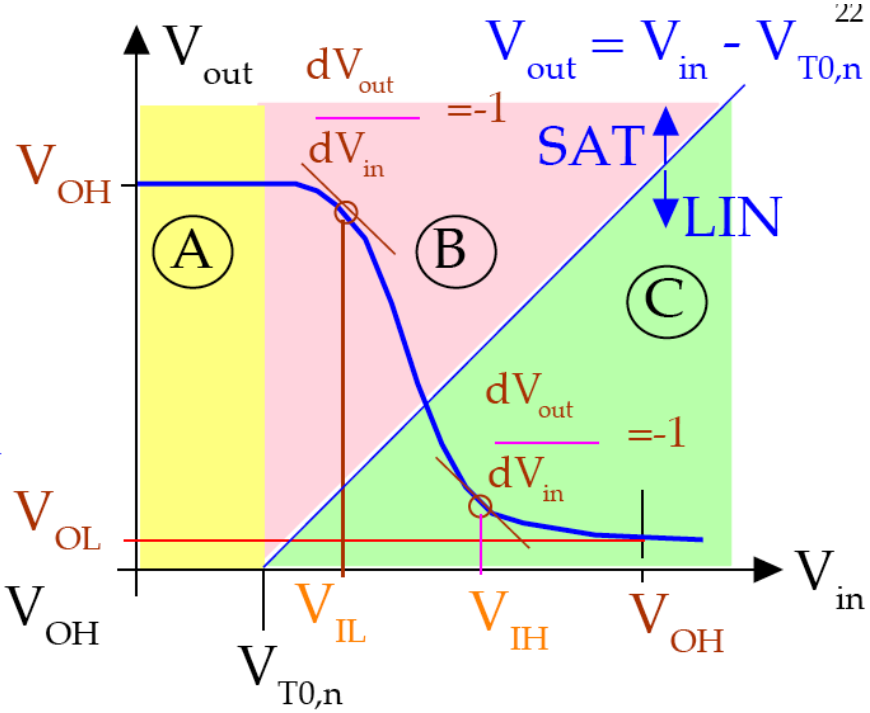


LOAD:

$V_{GS,L} = V_{DS,L} \Rightarrow V_{DS,L} > V_{GS,L} - V_{T,L}$ SAT cond. is ALWAYS SATISFIED

$$I_L = \frac{k'_n}{2}\left(\frac{W}{L}\right)_L \left(V_{GS,L} - V_{T.L}\right)^2 = \frac{k'_n}{2}\left(\frac{W}{L}\right)_L \left(V_{DD} - V_{out} - V_{T.L}\right)^2$$





Load -> Sat, Driver -> Cutoff (A) V_{OH}

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_L\left(V_{DD}-V_{out}-V_{T.L}\right)^2=0$$

Load -> Sat, Driver -> Sat (B) V_{IL}

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_L\left(V_{DD}-V_{out}-V_{T.L}\right)^2=\frac{k_n'}{2}\left(\frac{W}{L}\right)_d\left(V_{in}-V_{T0,n}\right)^2$$

Load -> Sat, Driver -> Lin (C) V_{IH}, V_{OL}

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_L\left(V_{DD}-V_{out}-V_{T.L}\right)^2=\frac{k_n'}{2}\left(\frac{W}{L}\right)_d\left(2[V_{in}-V_{T0,n}]V_{out}-V_{out}^2\right)$$

$V_{OH} < V_{DD}$

$V_{OL} > 0$

outline

- Voltage transfer characteristic (VTC)
- **nMOS inverters**
  - Resistive load inverter
  - Saturated enhancement load inverter
- CMOS inverter
  - CMOS VTC
  - Comparison of CMOS and MOS inverters
- Combinational CMOS logic gates (static)
- Ratioed Logic