outline

- Voltage transfer characteristic (VTC)
- nMOS inverters
  - Resistive load inverter
  - Saturated enhancement load inverter
  - Depletion load inverter
- CMOS inverter
  - CMOS VTC
  - Comparison of CMOS and MOS inverters
- Combinational CMOS logic gates (static)
- **Ratioed Logic**

(material developed by Prof. Cezhou Zhao
with slides from other sources)

CMOS inverter

If $V_{T0n} = - V_{T0p}$

$$\frac{(W/L)_n}{(W/L)_p} = \frac{\mu_p}{\mu_n}$$

1.

$V_{OH} = V_{DD}$

$V_{OL} = 0$

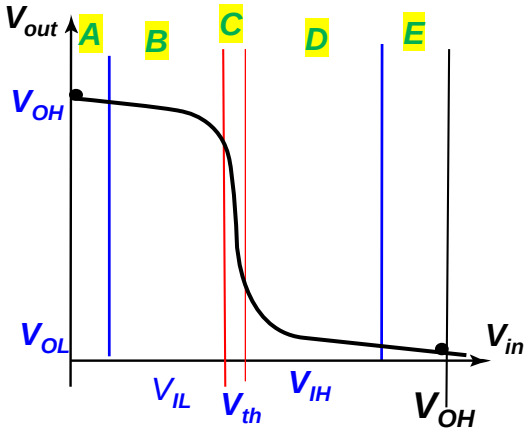
$V_{th} = V_{DD}/2$

2. Ratioless

$$V_{IL} = \frac{1}{8}(3\,V_{DD} + 2\,V_{T0})$$

$$V_{IH} = \frac{1}{8}(5\,V_{DD} - 2\,V_{T0})$$

3. $P_{DC} \approx 0$



nMOS inverter

Recall

$$\rightarrow V_{th} = V_{T0,n} - \frac{1}{k_n R_L} + \sqrt{\left(V_{T0,n} - \frac{1}{k_n R_L}\right)^2 + \frac{2V_{DD}}{k_n R_L} - V_{T0,n}^2}$$

1.

$$\rightarrow V_{IL} = V_{T0,n} + \frac{1}{k_n R_L}$$

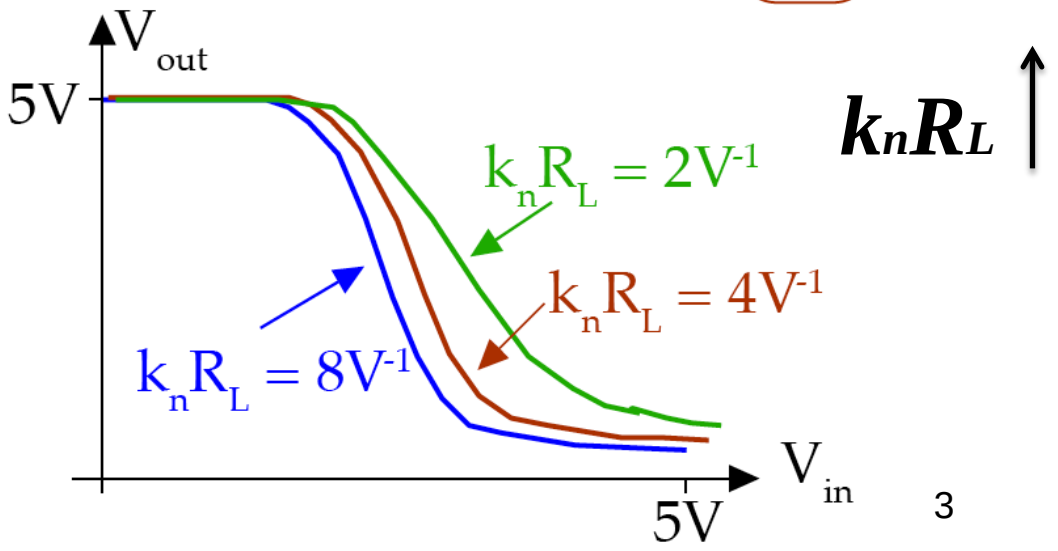
$$\rightarrow V_{IH} = V_{T0,n} + 2\sqrt{\frac{2}{3}\frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}$$

2. Ratioed

$$\rightarrow V_{OL} = V_{DD} - V_{T0,n} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0,n} + \frac{1}{k_n R_L}\right)^2 - \frac{2}{k_n R_L}V_{DD}}$$

$$\rightarrow V_{OH} = V_{DD}$$

$$k_n = C_{ox}\mu_n\left(\frac{W}{L}\right)_n$$

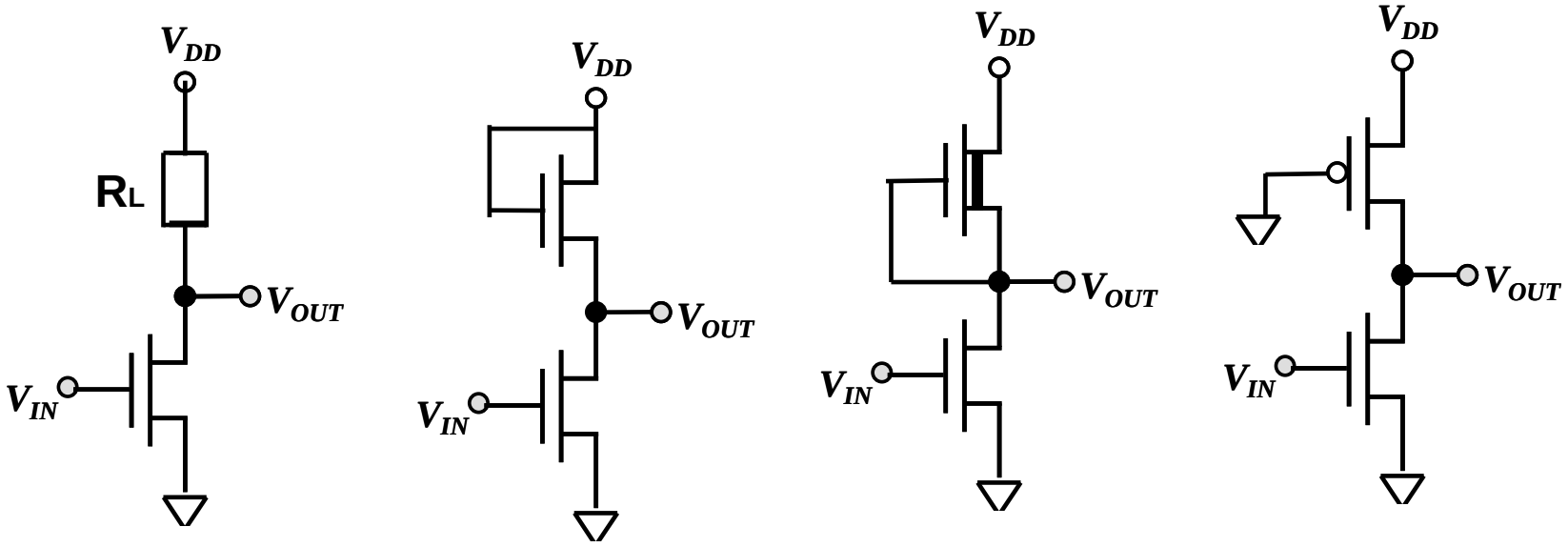


3.

$$P_{DC} = \frac{V_{DD}}{2}\frac{V_{DD} - V_{OL}}{R_L}$$

$k_n R_L \uparrow$

Ratioed Inverters

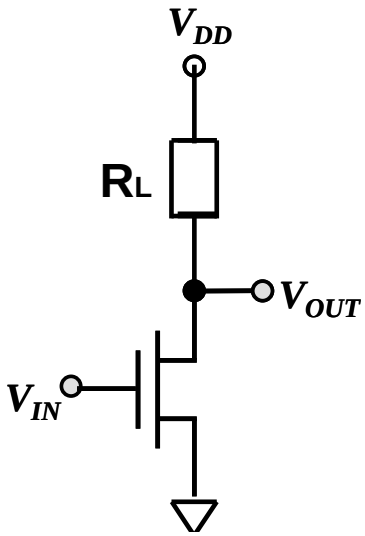


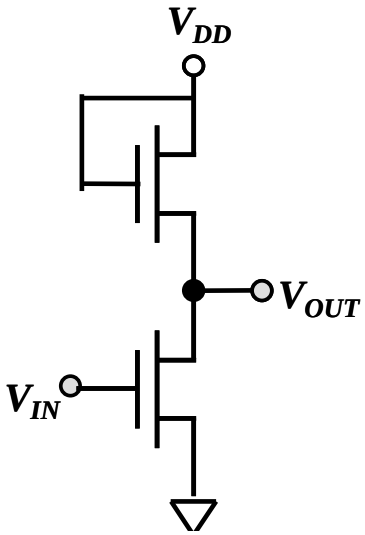
Resistive load **Depletion load NMOS** **Pseudo-NMOS**

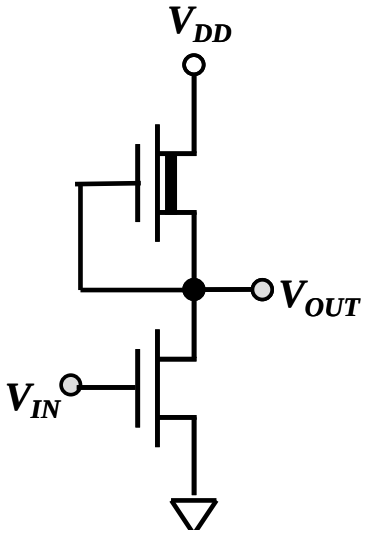
This logic style is called ratioed because care must be taken in scaling the impedances properly.

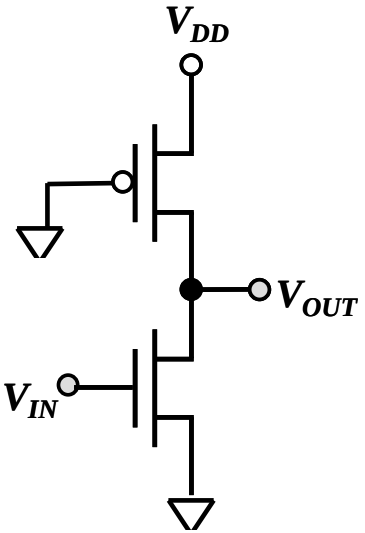
Note that full complementary CMOS is ratioless, since the output signal do not depend on the size of the transistors.

$k_n R_L \uparrow$ $\qquad k_n = C_{ox}\mu_n\left(\frac{W}{L}\right)_{n,Driver} \uparrow$









Resistive load **Depletion load NMOS** **Pseudo-NMOS**

$$R_L = \frac{V_{DD} - V_{out}}{I_L}$$

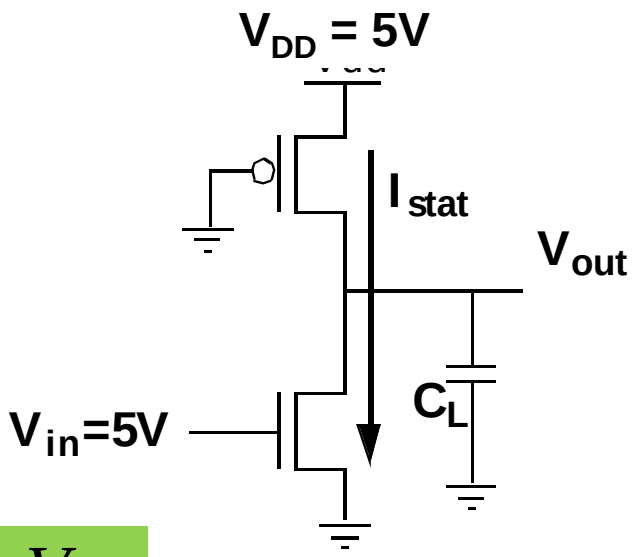
$$R_L = \frac{V_{DD} - V_{out}}{I_{Dn}} \propto \frac{V_{DD} - V_{out}}{(W/L)_{n,Load}}$$

$$R_L = \frac{V_{DD} - V_{out}}{I_{Dp}} \propto \frac{V_{DD} - V_{out}}{(W/L)_{p,Load}}$$

$R_L \uparrow \longrightarrow (W/L)_{Load} \downarrow$

Static Power Consumption

- However, static power consumption makes it impossible to use in large circuits (except in address decoders when majority of outputs are high). A minimum sized gate consumes 1mW !

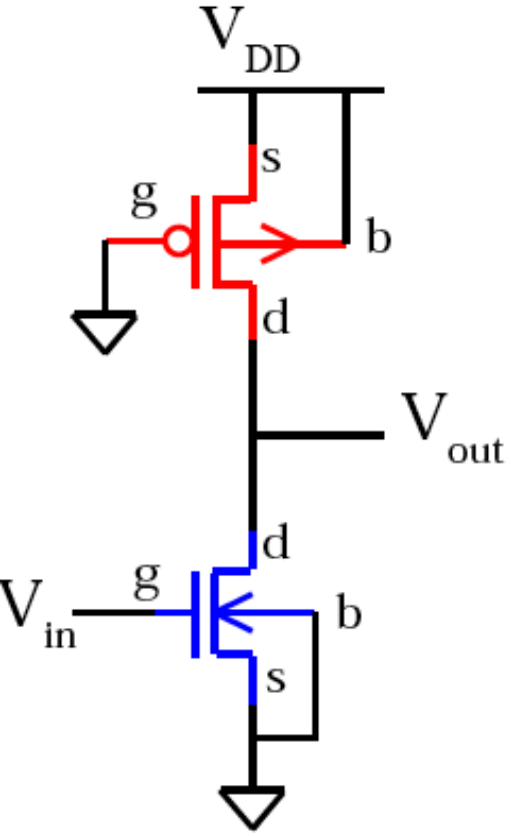


$$P_{DC} = \left(\frac{V_{DD}}{2}\right) I_{stat} = \frac{V_{DD}}{2}\frac{V_{DD} - V_{OL}}{R_L}$$

$V_{OL} \neq 0$

Wasted energy …
Should be avoided in almost all cases,
but could help reducing energy in others (e.g. sense amps)

Pseudo-nMOS Inverter



$V_{DSp} = V_{out} - V_{DD}$

$V_{GSp} = -V_{DD} < V_{T0p}$ => pMOS load always turned ON

$V_{DSp} > V_{GSp} - V_{T0p}$ (LIN)

$V_{out} > -V_{T0p}$

$V_{DSp} < V_{GSp} - V_{T0p}$ (SAT)

$0 \le V_{out} < -V_{T0p}$

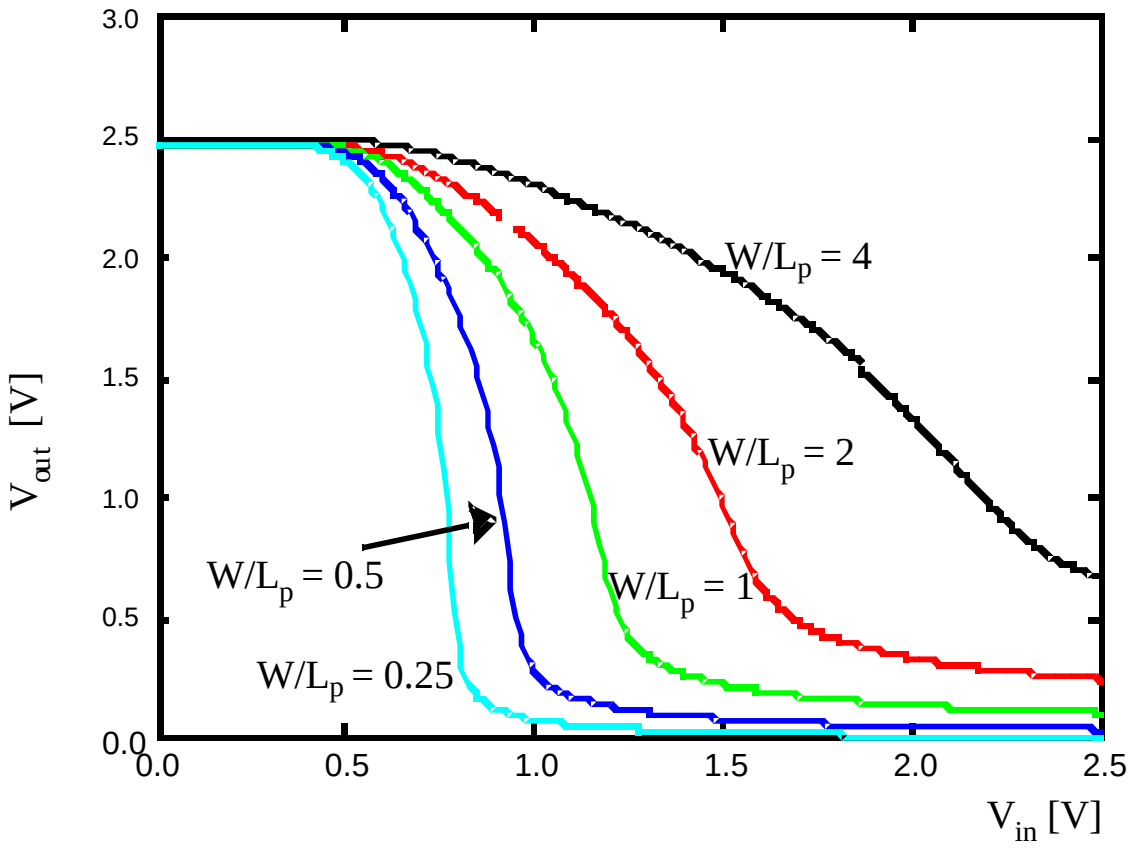
$|I_{Dn}| = |I_{Dp}|$

$V_{in} = V_{GSn}$

$V_{out} = V_{DSn} = V_{DSp} + V_{DD}$

$V_{OH} = V_{DD}$
$V_{OL} > 0$
$P_{DC} > 0$

Pseudo-NMOS VTC

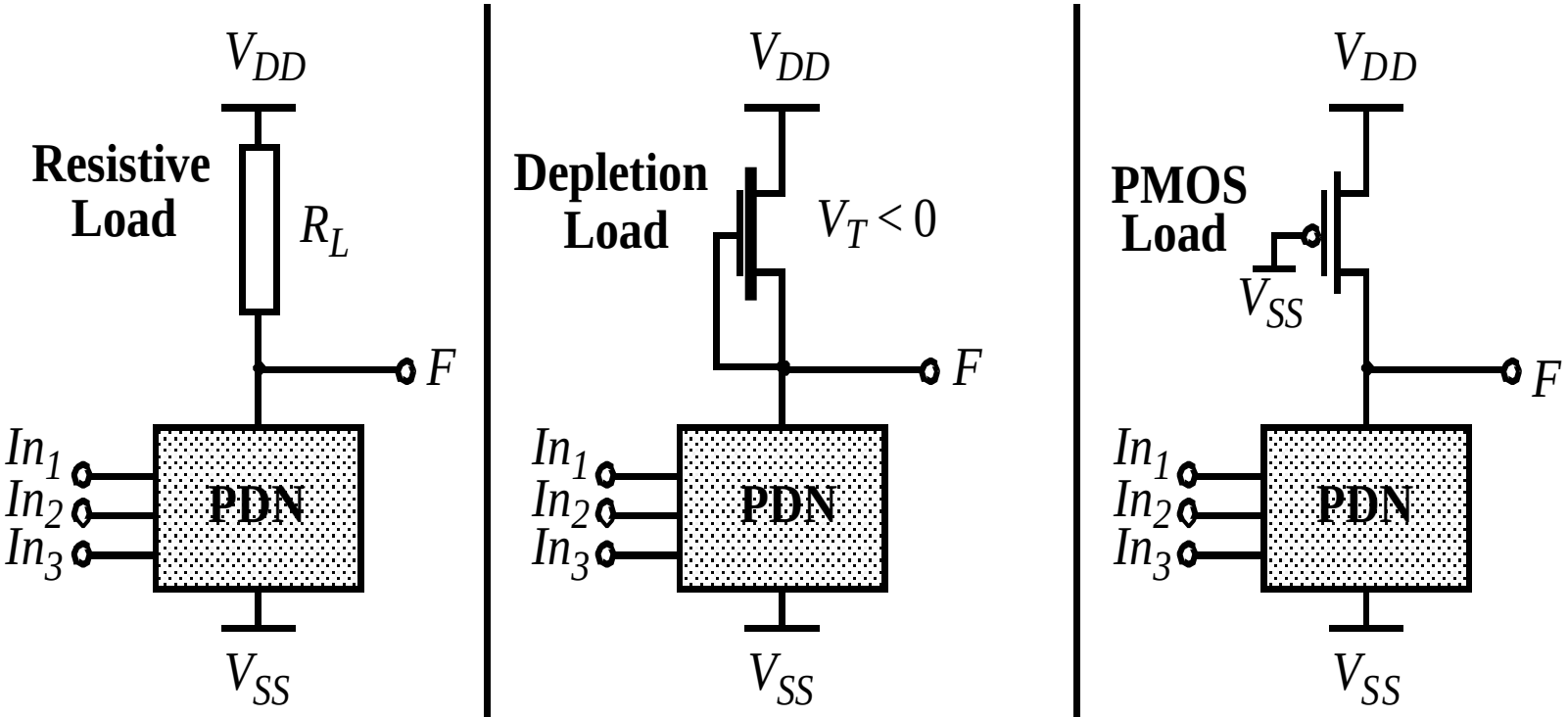


Nominal device:

$$\frac{W}{L_n} = \frac{0.5\mu}{0.25\mu} = 2$$

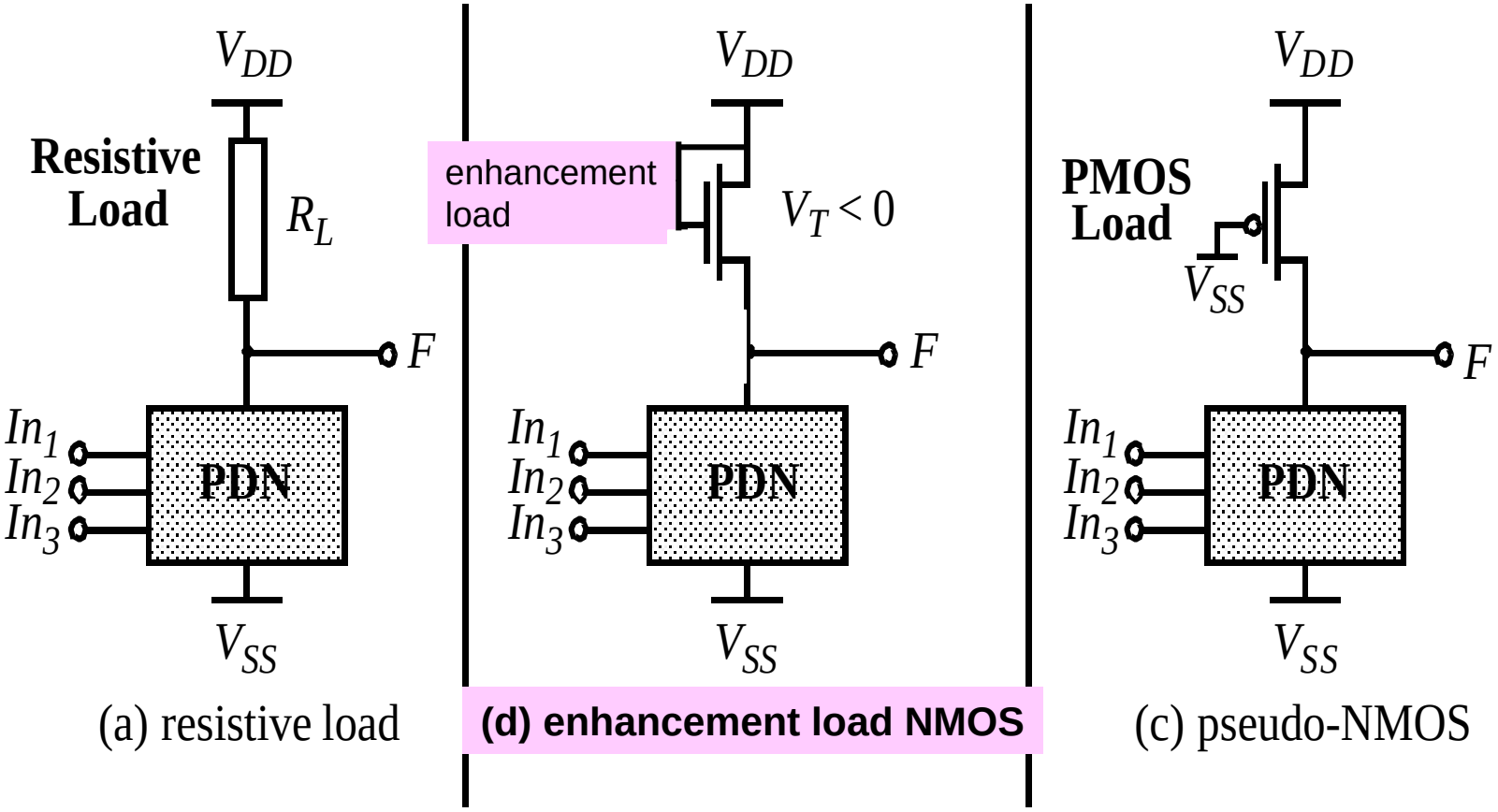
$$R_L \uparrow \longrightarrow (W/L)_{Load} \downarrow$$

Ratioed Logic



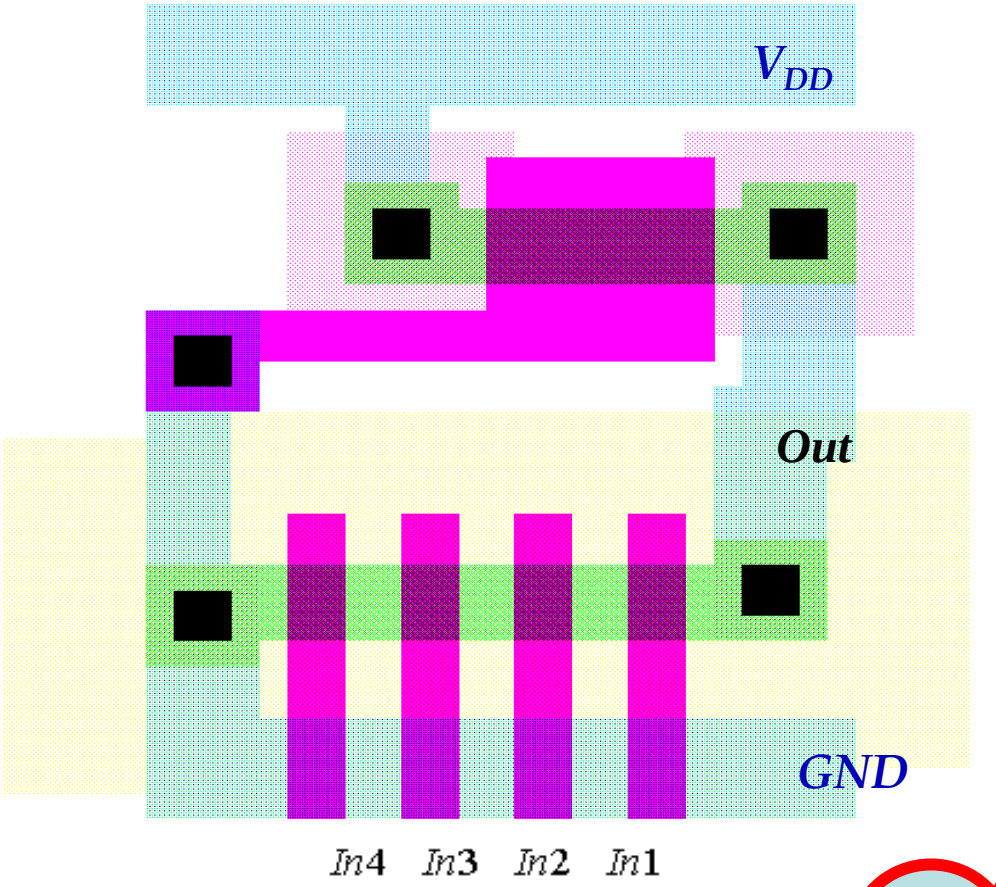
Here, the logic function is built in the PDN and used in combination with a SIMPLE load device.

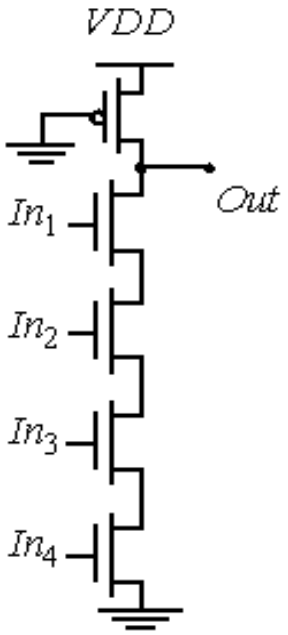
Ratioed Logic



Here, the logic function is built in the PDN and used in combination with a SIMPLE load device.

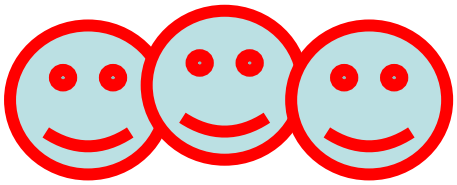
Pseudo-NMOS NAND Gate





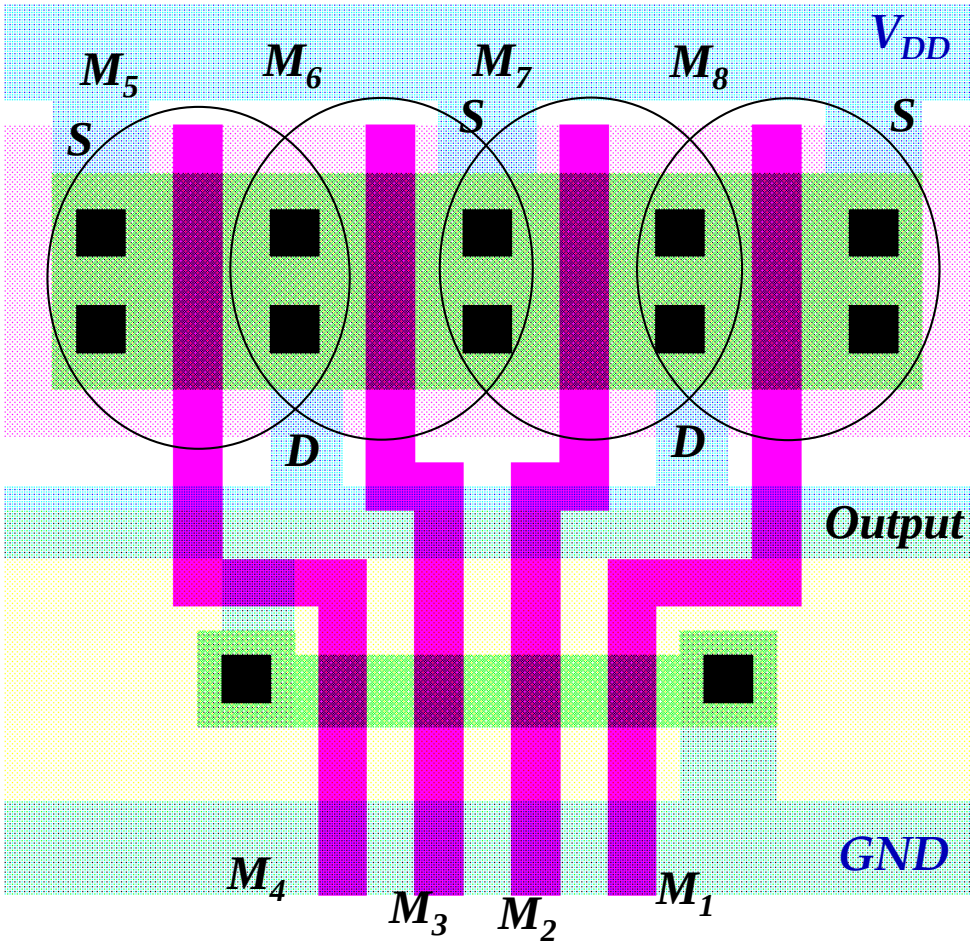
$$k_n = C_{ox}\mu_n (W/L)_{n,Driver}$$

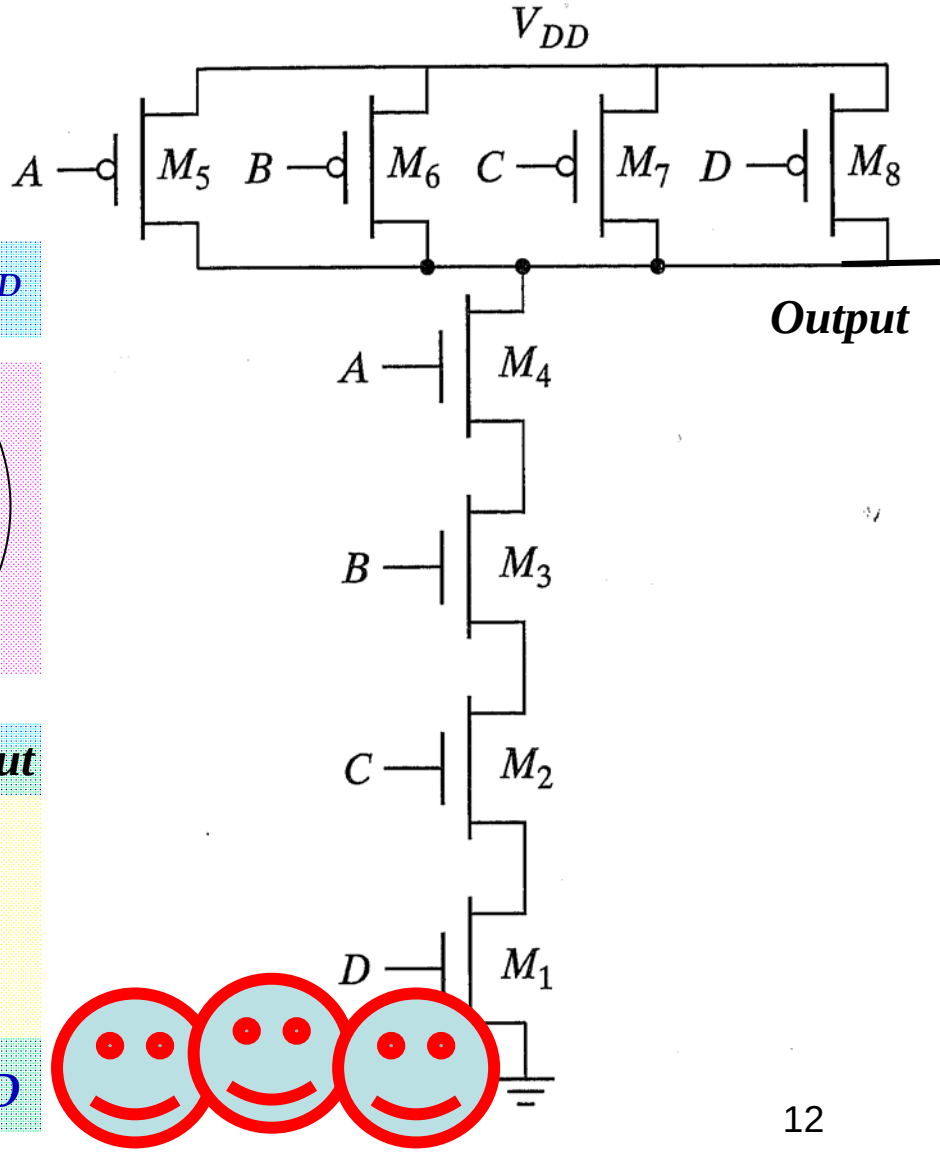
$R_L \uparrow \longrightarrow (W/L)_{Load} \downarrow$



CMOS NAND Gate

$$\mu_n (W/L)_n = 4\mu_p (W/L)_p$$





Comparison of CMOS and MOS

CMOS	MOS
Zero static power dissipation $V_{OL} = 0$	Power is dissipated with output "0" $V_{OL} \neq 0$
Power dissipated during logic transition	Power dissipated during logic transition
Requires 2N devices for N inputs Process more complex	Require N+1 devices for N inputs Maybe nMOS process only
CMOS encourages regular layout styles Ratioless	Depletion, load and different driver transistors create irregularity in layout Ratioed