MOS Capacitor – (I) energy band & bias; (II) electrostatics

(material originally developed by Professor Cezhou Zhao)

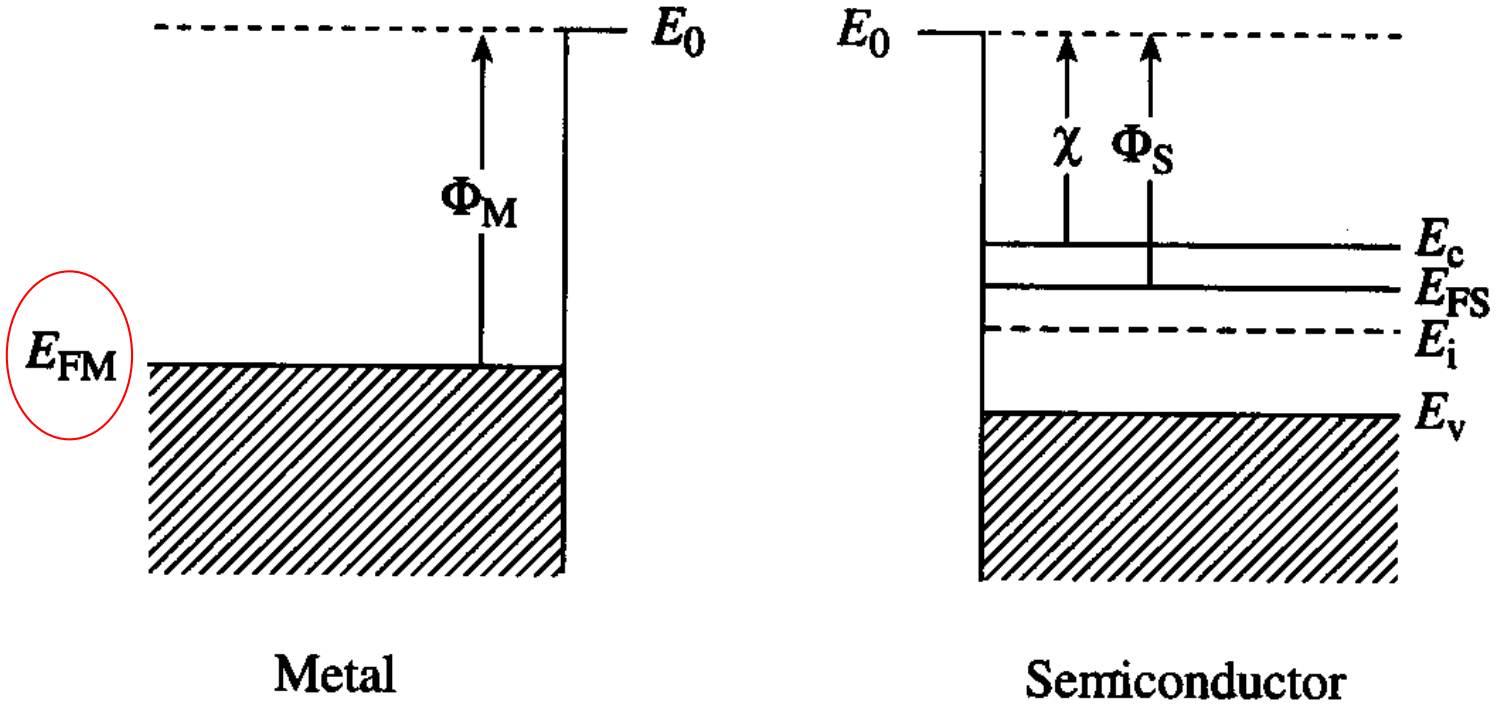
MOS Capacitor

OUTLINE

- Physical Structure of MOS Capacitor
- Energy Band Diagram of MOS Structure
- Effects of Applied Voltage
  - **operation modes** & **capacitance**
- Non-Ideal MOS Capacitors

Work Function

E_0: vacuum energy level



Φ_M : metal work function

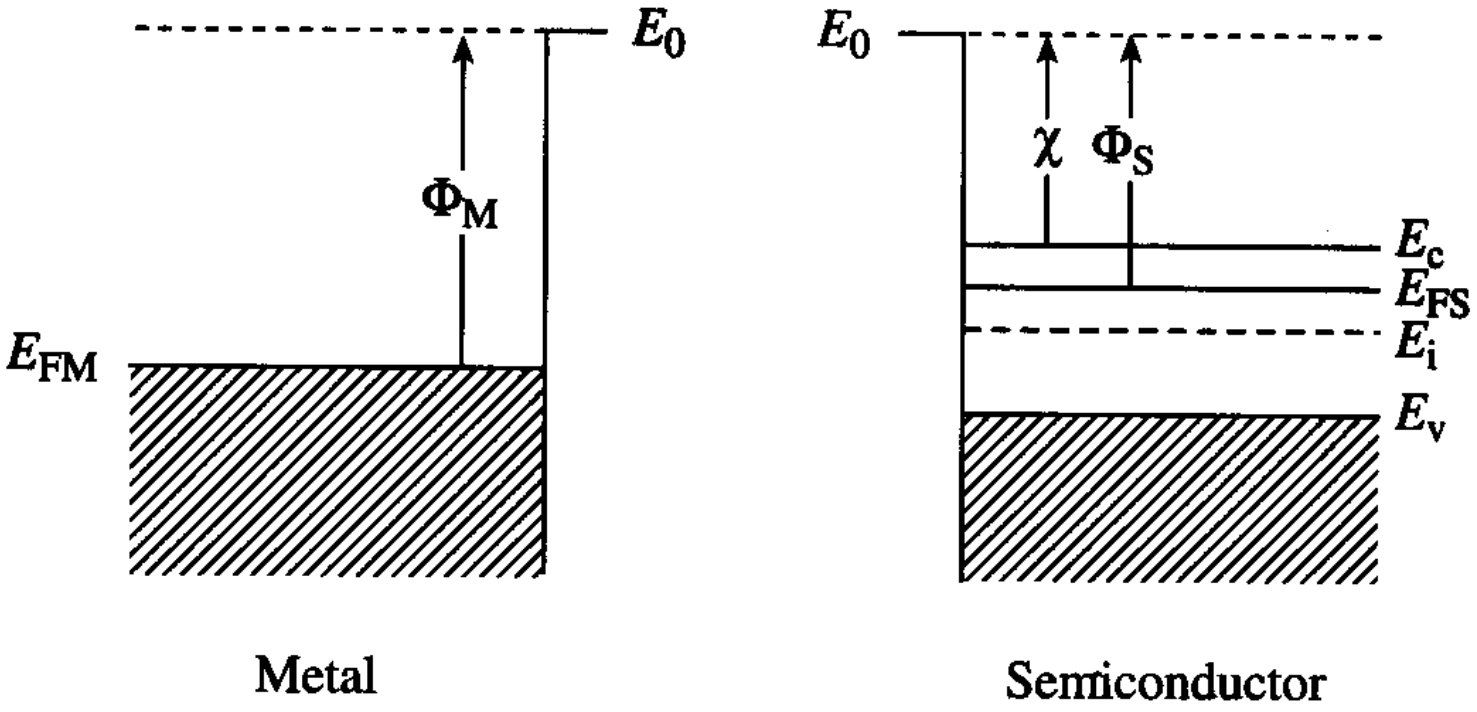
Φ_S : semiconductor work function

χ : electron-affinity

chi

Work Function

E_0: vacuum energy level



Φ_M: metal work function

Φ_{Al} = 4.28eV Φ_{Au} = 5.1eV

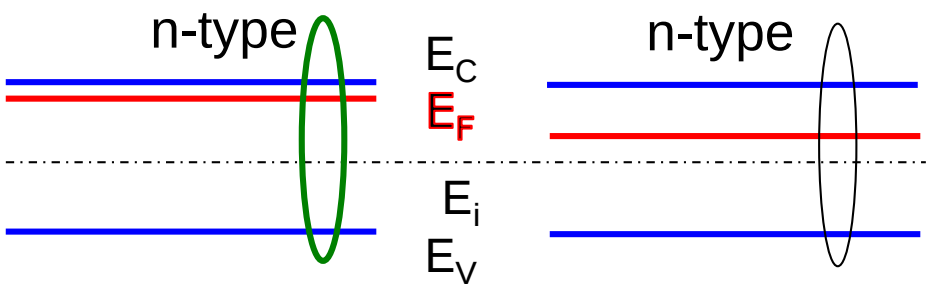
Φ_S: semiconductor work function

χ : electron-affinity

Electron concentration & E_C-E_F

Heavily doped

Lightly doped

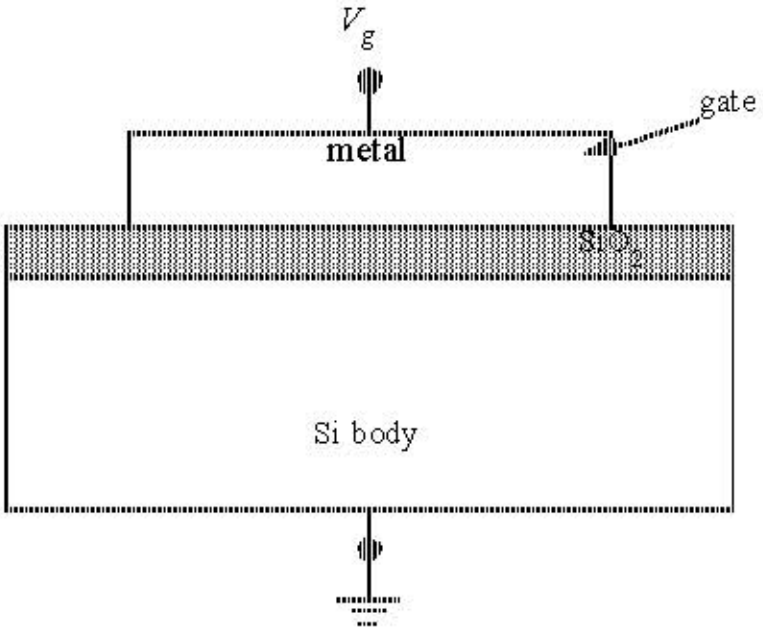


More electrons

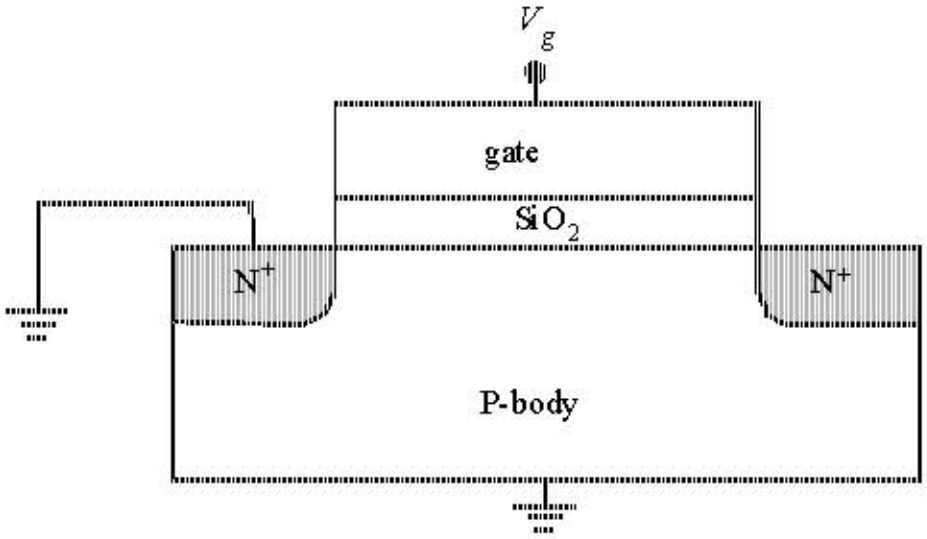
Less electrons

MOS Capacitors

MOS: Metal-Oxide-Semiconductor



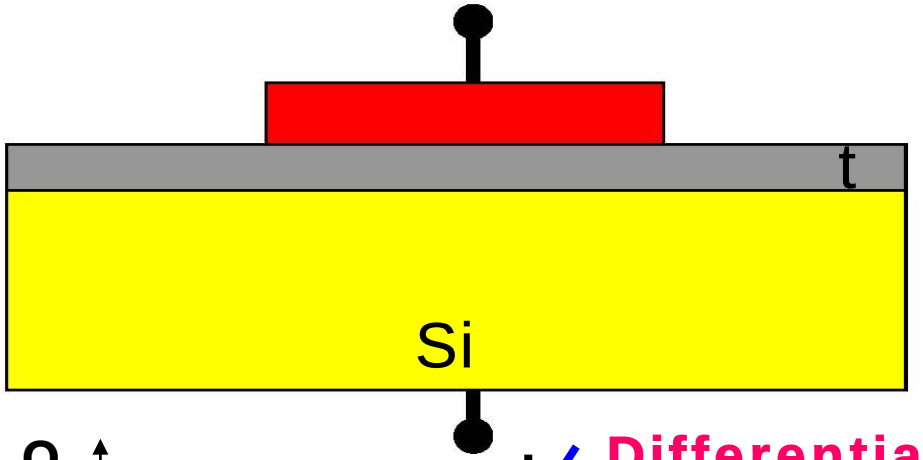
MOS capacitor



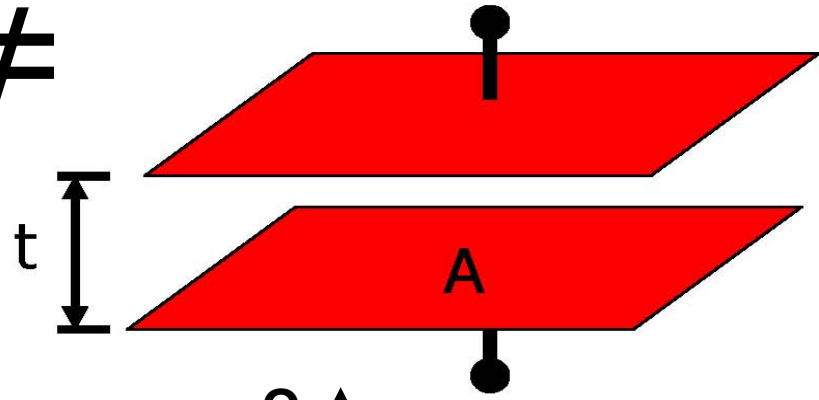
MOS transistor

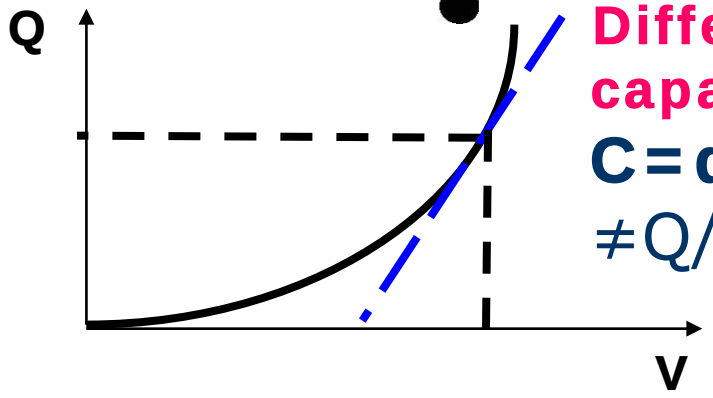
MOS Capacitor

parallel-plate capacitor



≠

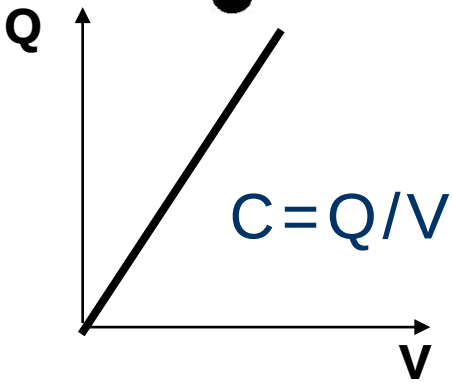




Differential capacitance:

C = dQ / dV

≠Q/V



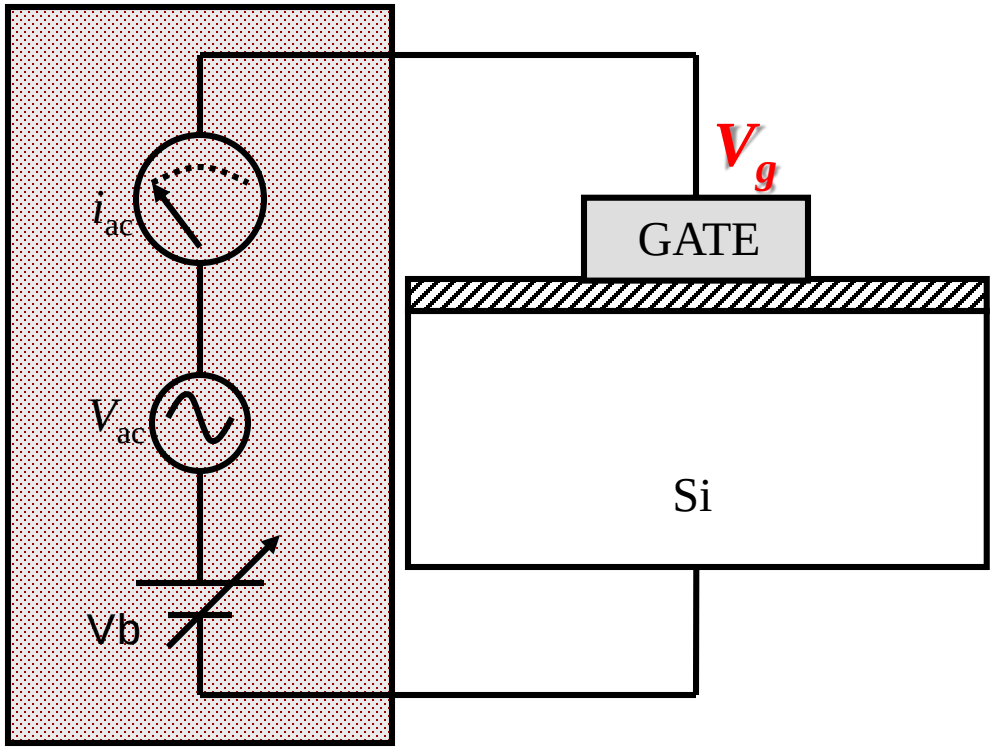
- Definition:

$$C = \frac{\varepsilon A}{t_{ox}} = \frac{\varepsilon_r \varepsilon_0 A}{t_{ox}}$$

$\varepsilon_{r,SiO2} = 3.9$, $\varepsilon_{r,Si} = 11.9$, $\varepsilon_o = 8.85 \times 10^{-14}$ F/cm

epsilon

MOS Capacitance Measurement



C-V Meter MOS Capacitor

- V_b: dc biasing voltage and scanned slowly
- V_{ac}: small ac signal
- $\boldsymbol{V_g = V_b + V_{ac}}$

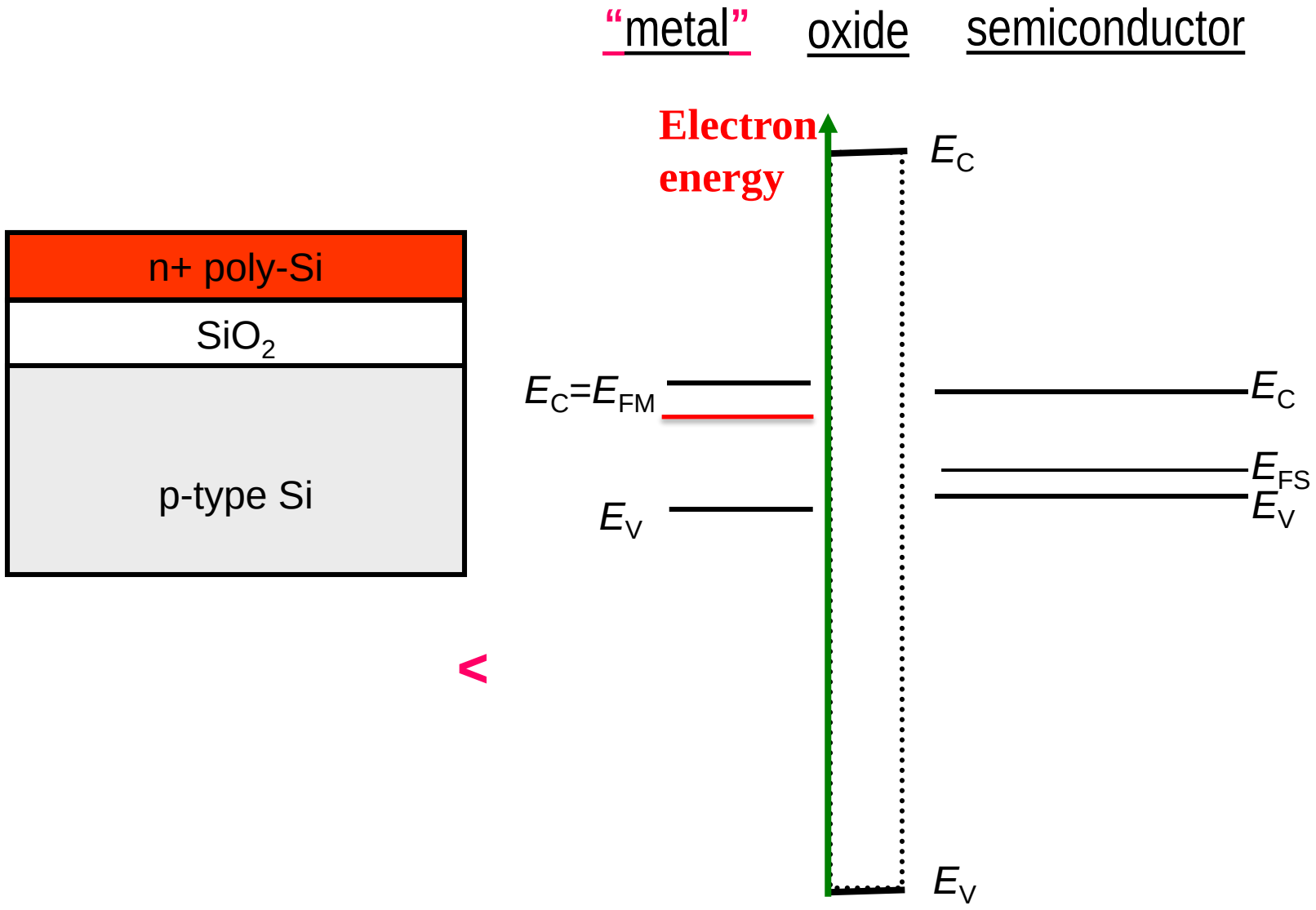
$$C = \left|\frac{dQ_{GATE}}{dV_g}\right| = \left|\frac{dQ_s}{dV_g}\right| = \left|\frac{dQ_s}{dV_{ac}}\right|$$

- Capacitive current due to V_{ac} is measured

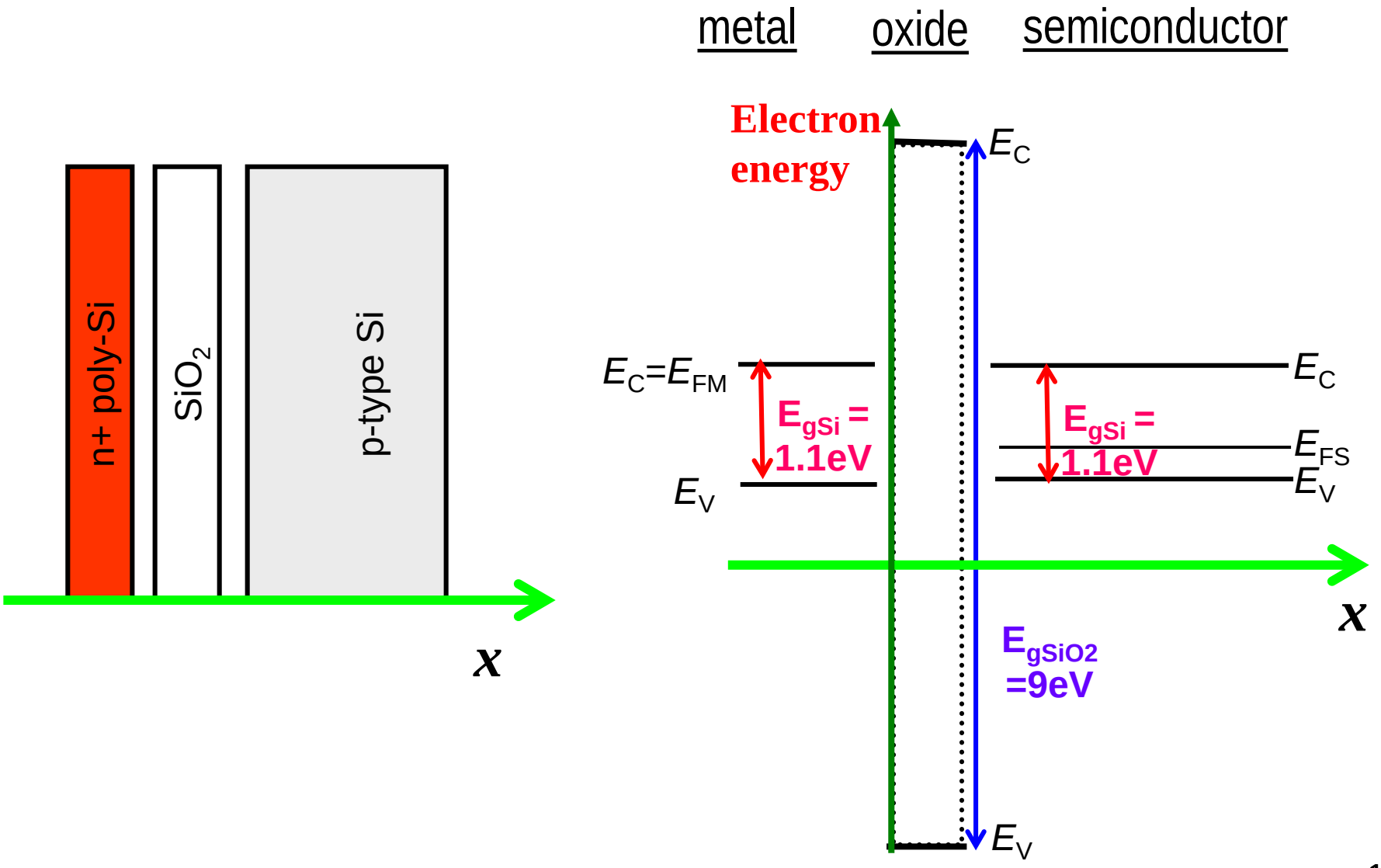
$$i_{ac} = C\frac{dV_{ac}}{dt}$$

$\boldsymbol{|V_b| >> |V_{ac}|}$

Poly-Si gate

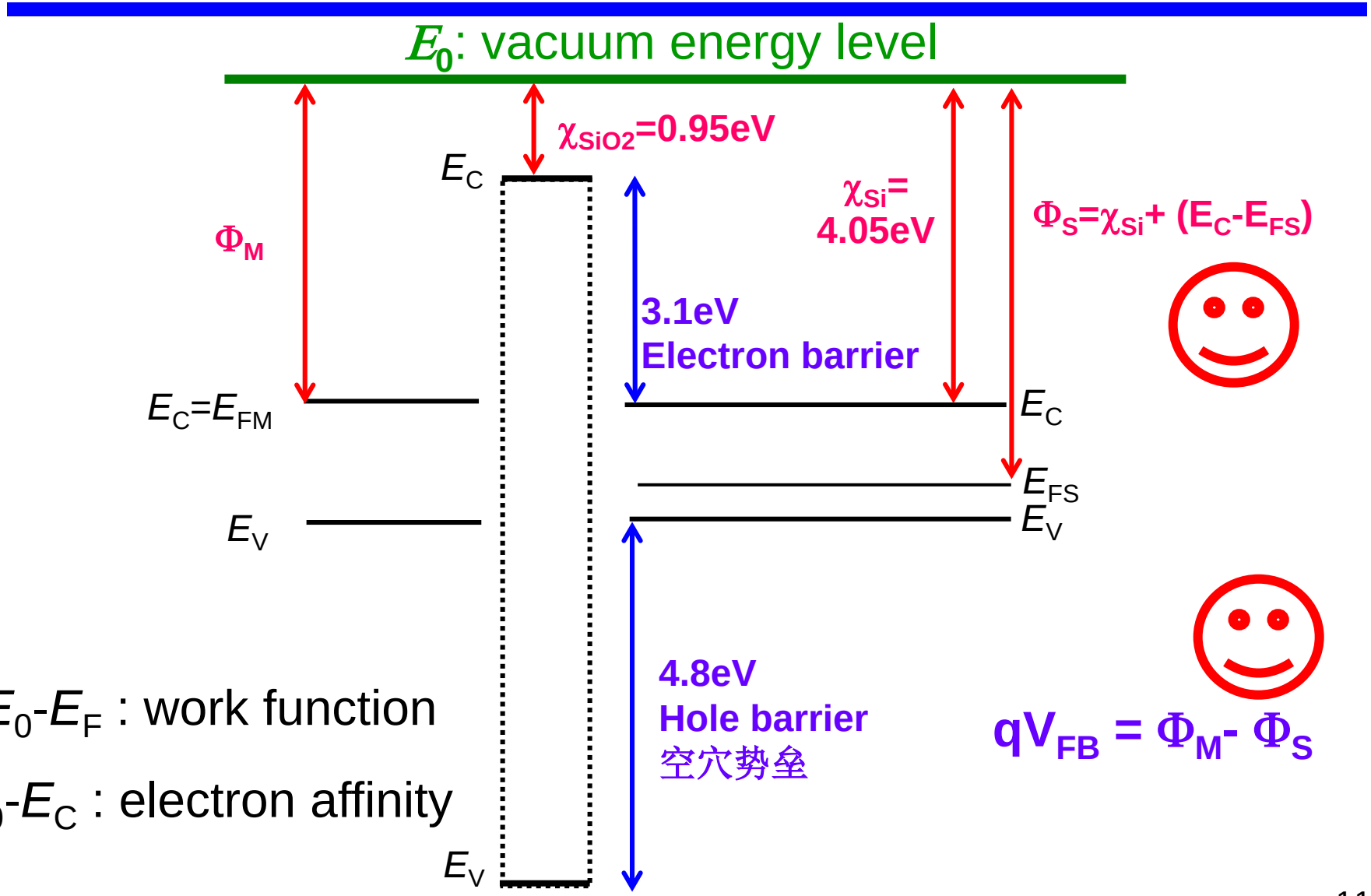

"metal"
oxide
semiconductor
Electron energy
E_C
n+ poly-Si
SiO_2
p-type Si
$E_C=E_{FM}$
E_V
E_C
E_{FS}
E_V
<
E_V

Coordinate system



χ_{Si} = 4.05 or 4.03 eV

Guidelines for Drawing MOS Band Diagrams



Guidelines for Drawing MOS Band Diagrams

1) Fermi level E_F is flat (constant with distance x) in the Si

- Since no current flows in the x direction, we can assume that equilibrium conditions prevail

2) **Band bending is linear in the oxide**

- No charge in the oxide => $d\mathcal{E}/dx = \rho/\varepsilon_{ox} = 0$, so $\mathcal{E}$ is constant
  => dE_C/dx is constant

$$\mathcal{E} = -\,dV/dx$$
$$E_C = -qV$$

Guidelines for Drawing MOS Band Diagrams

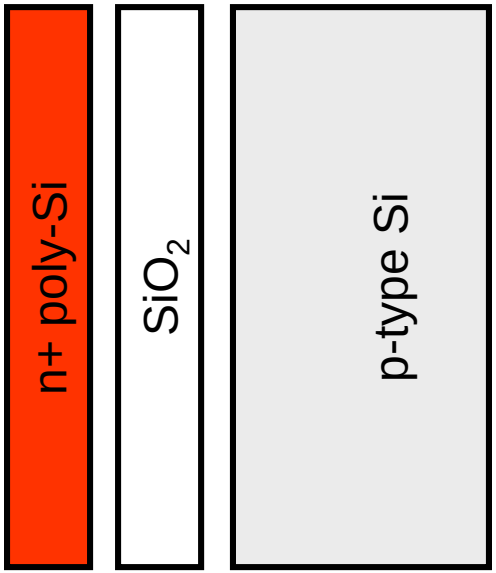
3) The barrier height for conduction-band electron flow from the Si into SiO_2 is 3.1 eV
   - This is equal to the electron-affinity difference (χ_{Si} and χ_{SiO2})

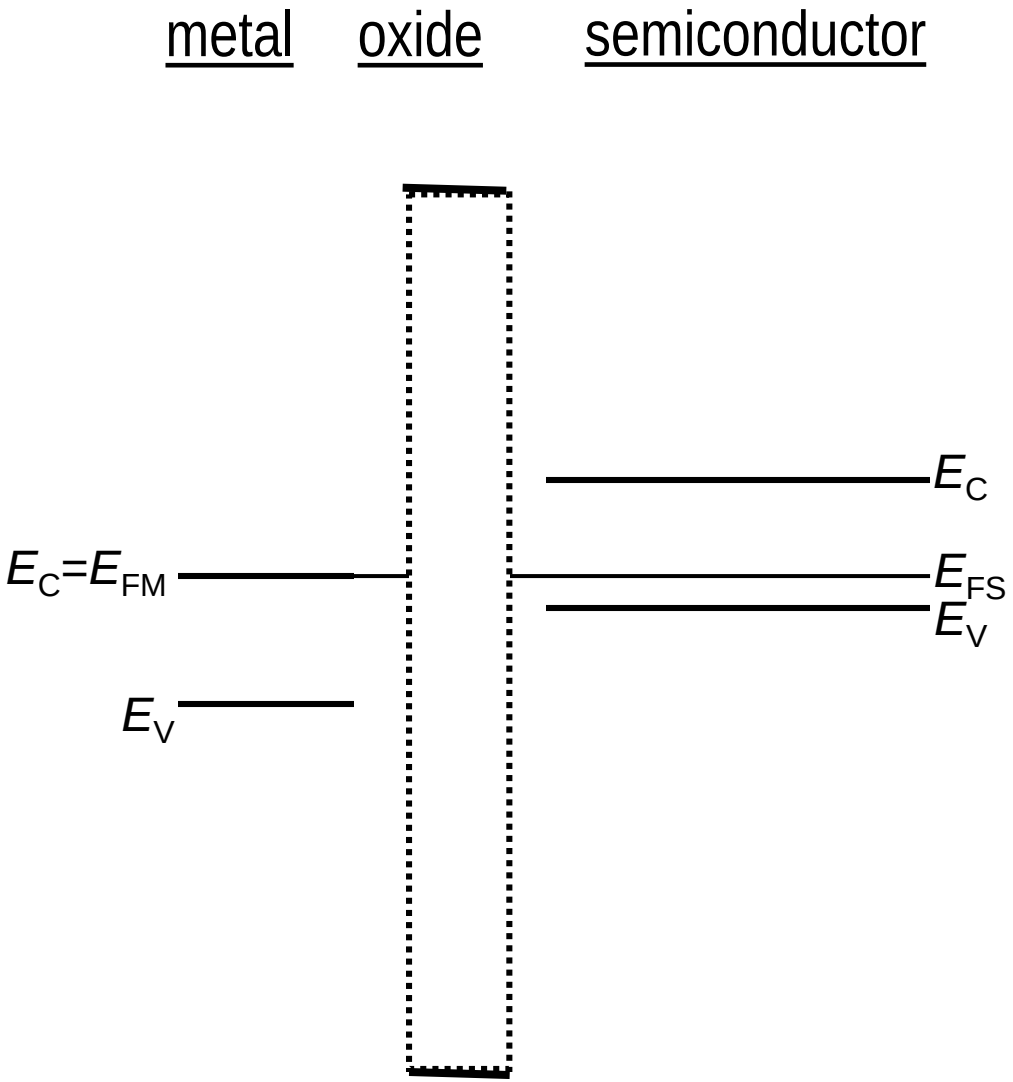
4) The barrier height for valence-band hole flow from the Si into SiO_2 is 4.8 eV

5) The vertical distance between the Fermi level in the metal, E_{FM}, and the Fermi level in the Si, E_{FS}, is equal to the applied gate voltage:

$$qV_G = E_{FS} - E_{FM}$$

MOS Equilibrium Energy-Band Diagram



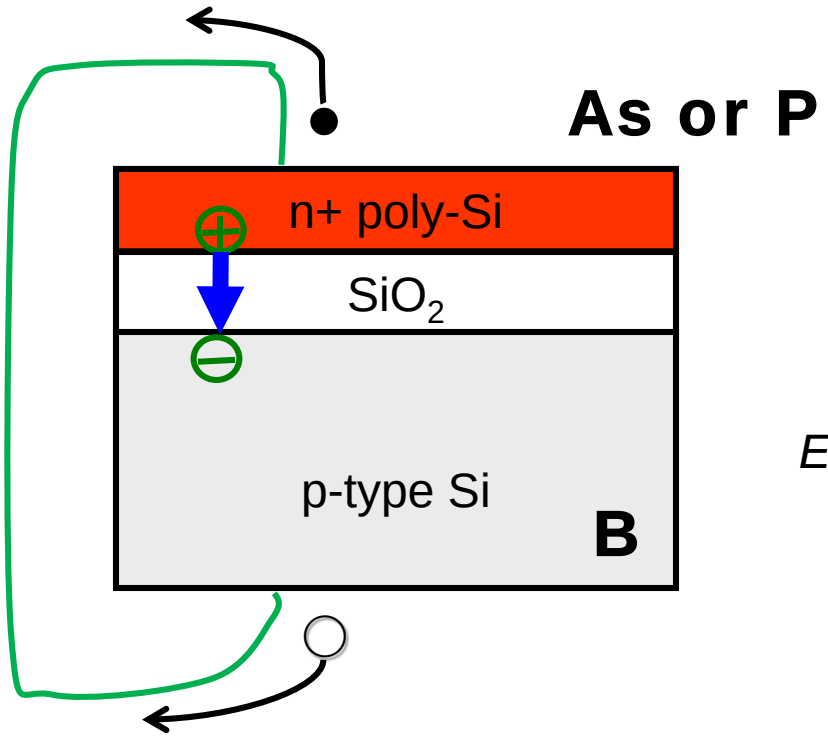


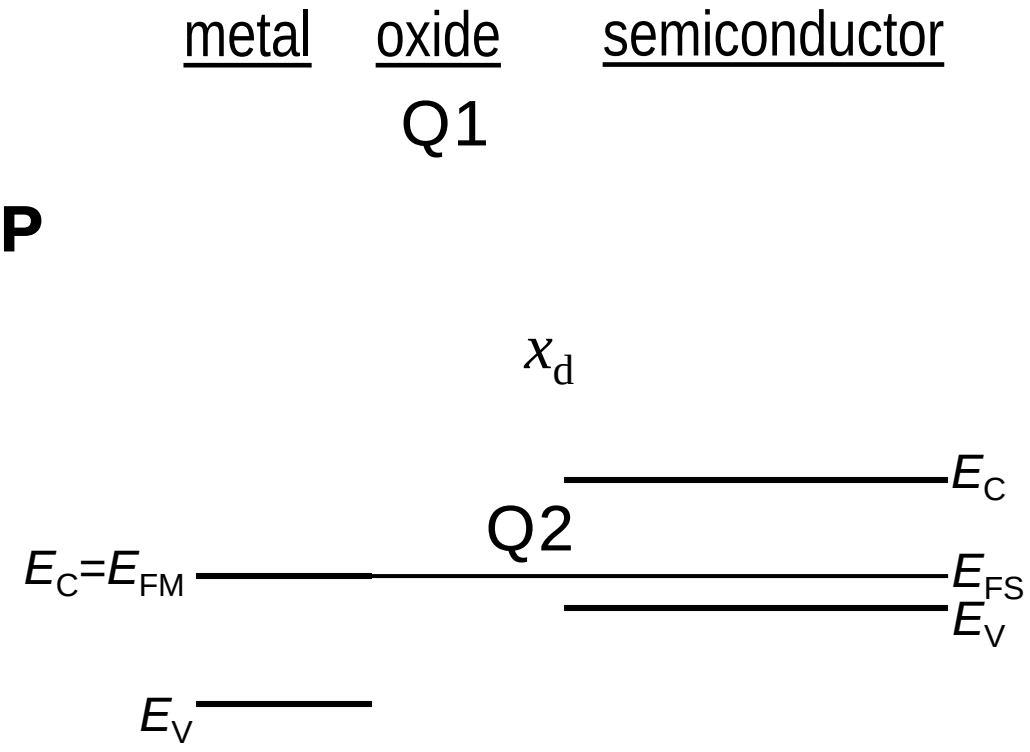
Guideline 1:

Fermi Level is flat.

MOS Equilibrium Energy-Band Diagram

Fermi Level is flat.





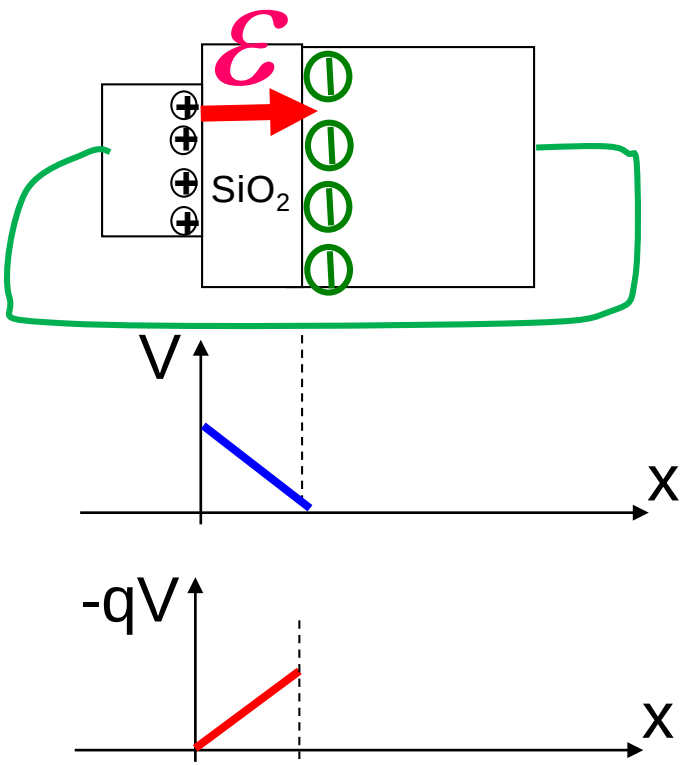
After contact, there are two questions: Q1 & Q2.

Q1: Carrier and ion in silicon

Guideline 2:

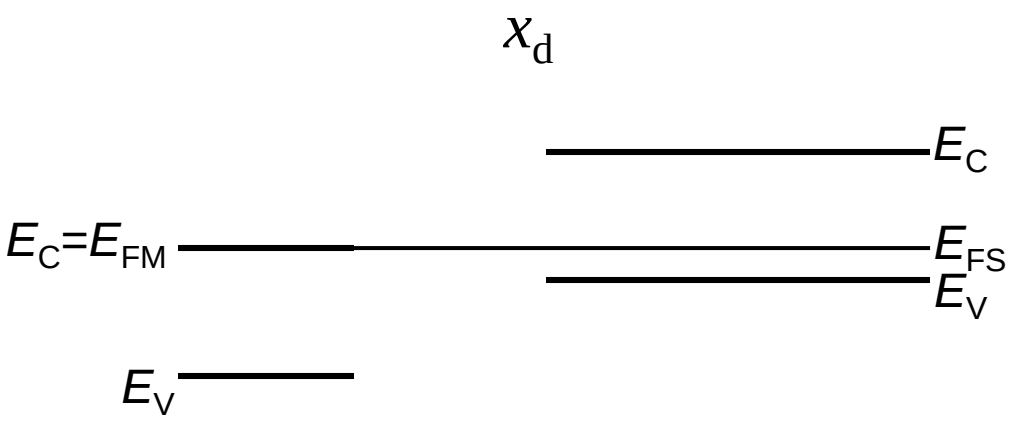
$\mathcal{E}=-dV/dx$

$E_C=-qV$



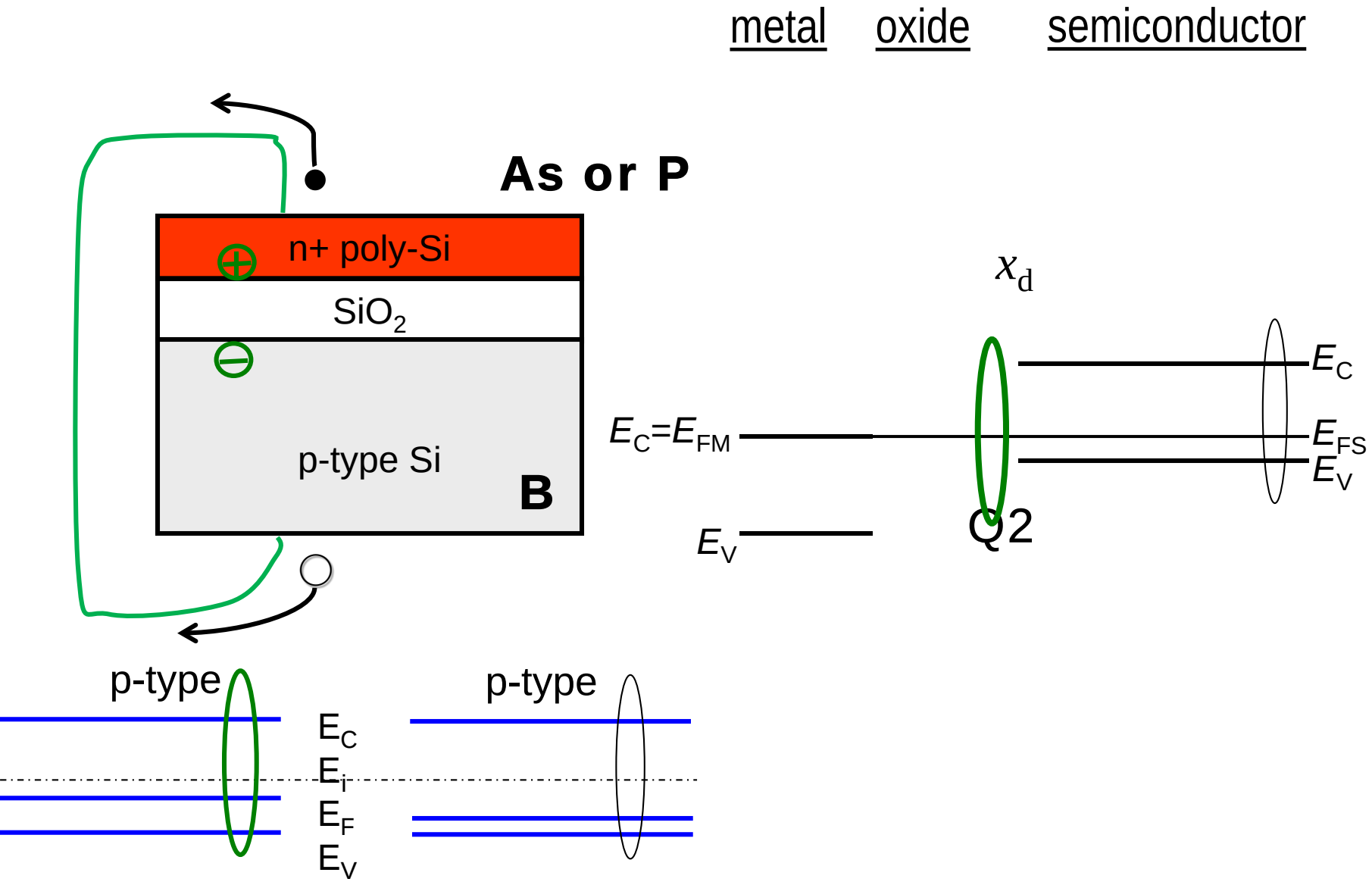
metal oxide semiconductor

Q1

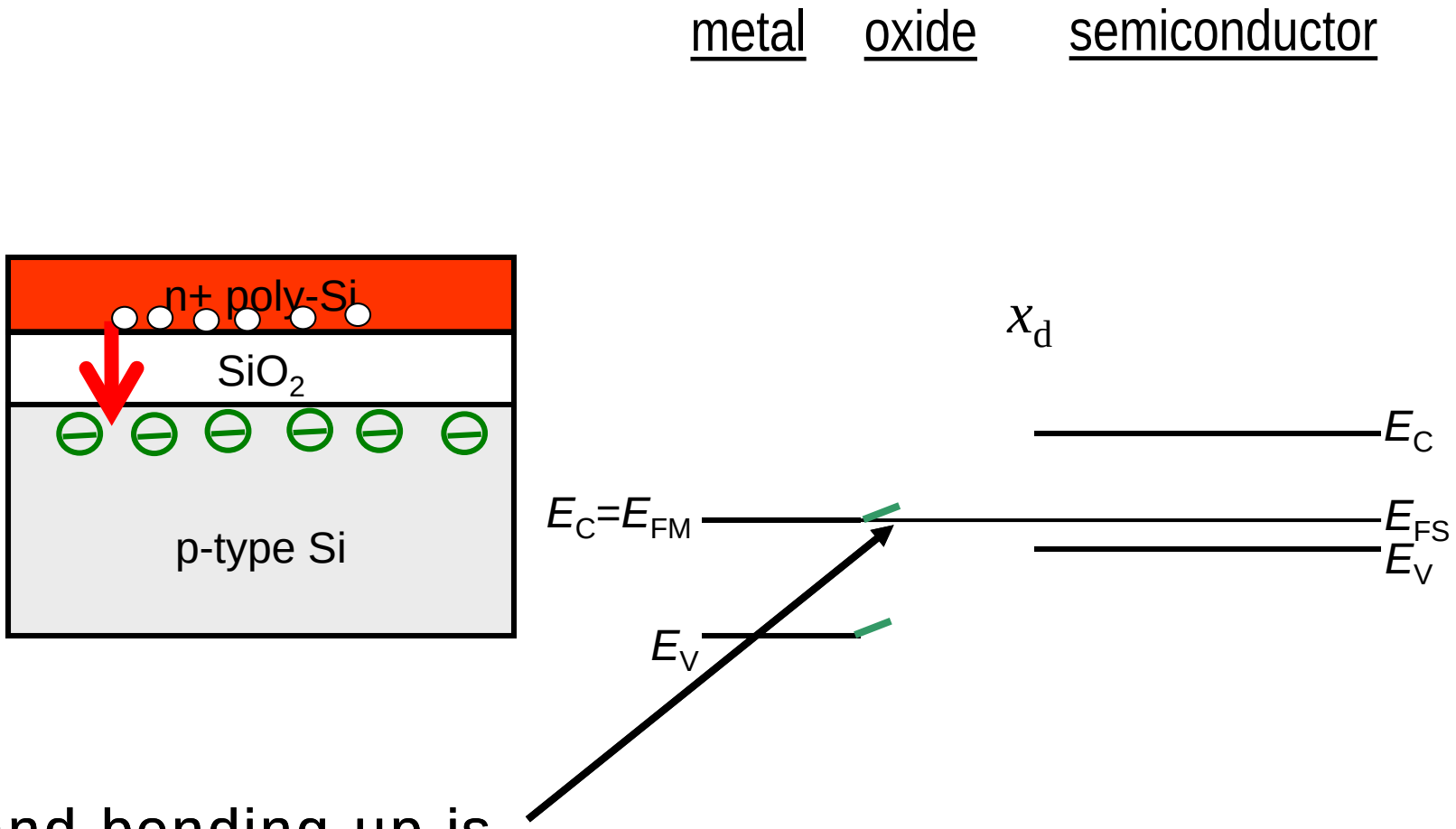


Q2: Carrier and ion in silicon

$n_0 p_0 = n_i^2$

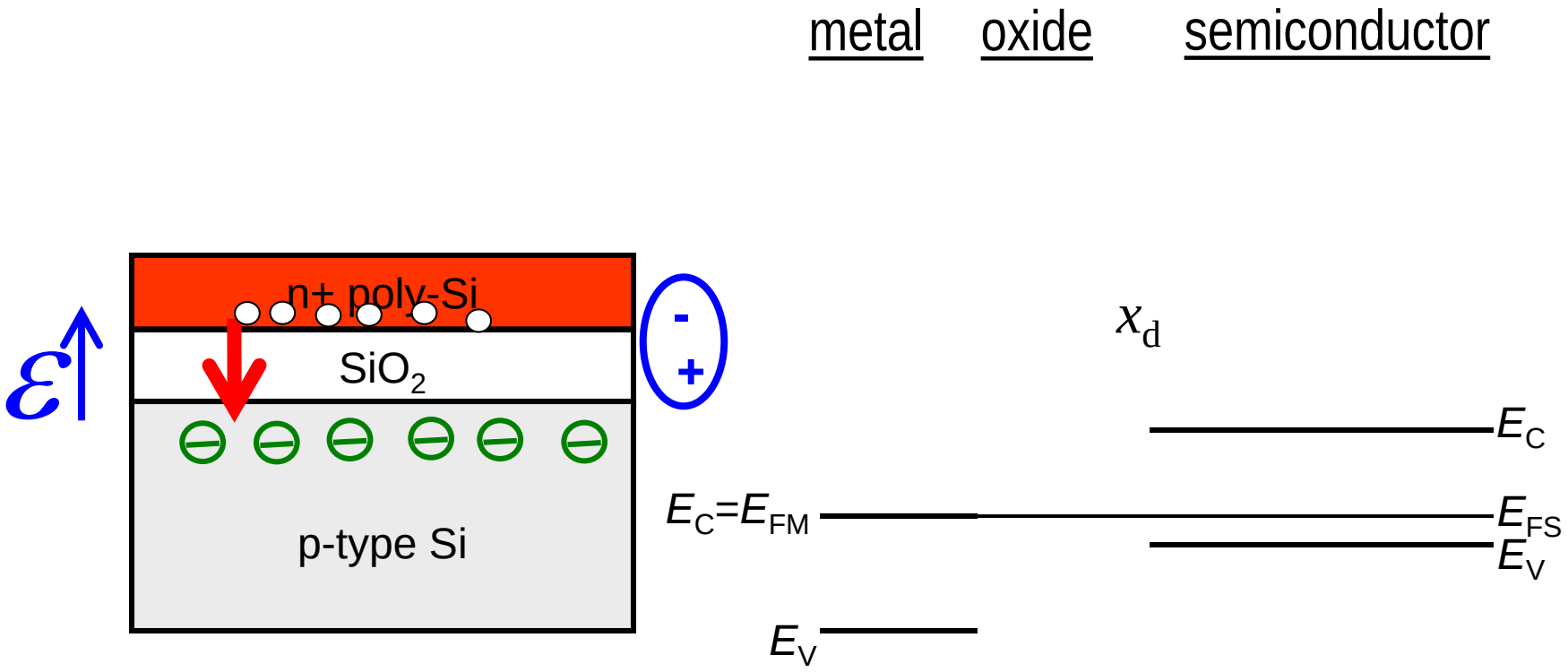


Poly-Si Depletion



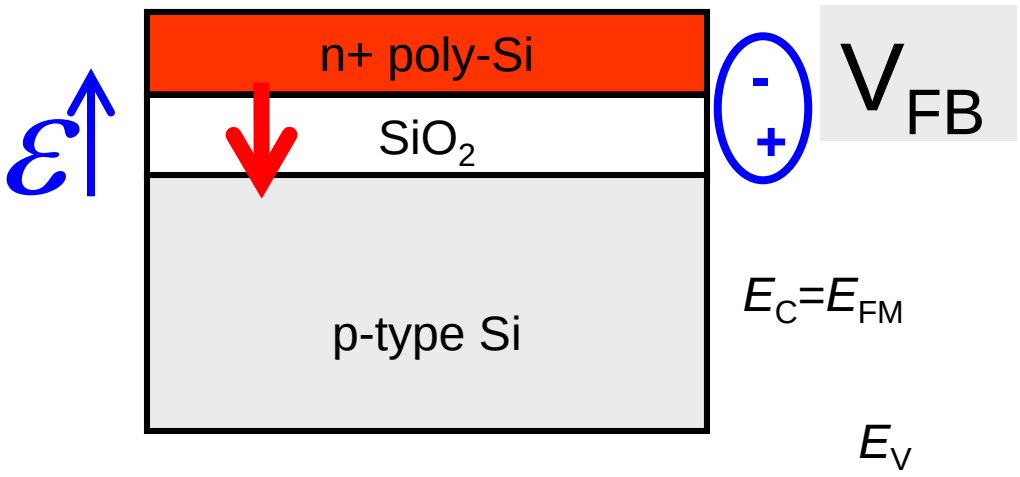
Band bending up is negligible because of heavy doping of poly-Si.

Flat-Band Voltage



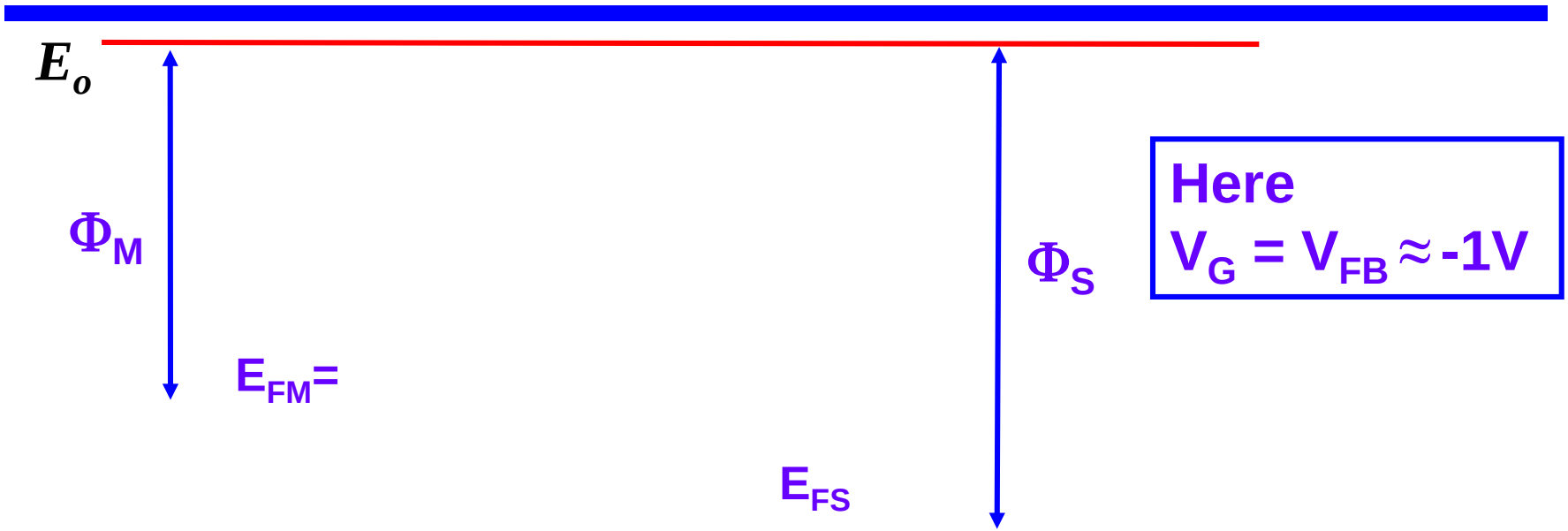
- The built-in potential can be “cancelled out” by applying a gate voltage that is equal in magnitude (but of the opposite polarity) as the built-in potential. This gate voltage is called the ***flatband voltage*** because the resulting potential profile is flat.

Flat-Band Voltage



- The built-in potential can be “cancelled out” by applying a gate voltage that is equal in magnitude (but of the opposite polarity) as the built-in potential. This gate voltage is called the ***flatband voltage*** because the resulting potential profile is flat.

Flat-Band Condition



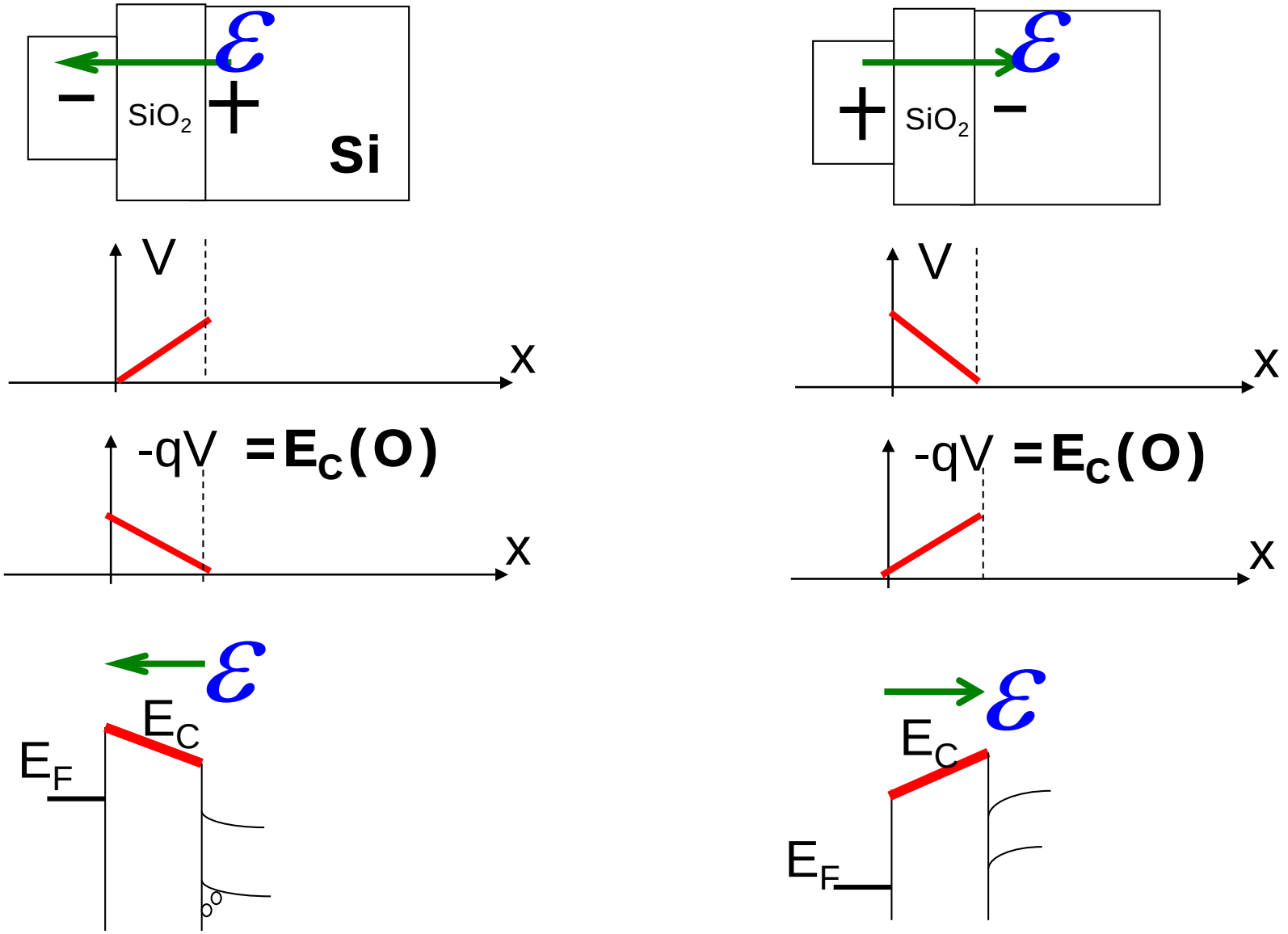
$qV_G = E_{FS} - E_{FM}$

$= \Phi_M - \Phi_S$

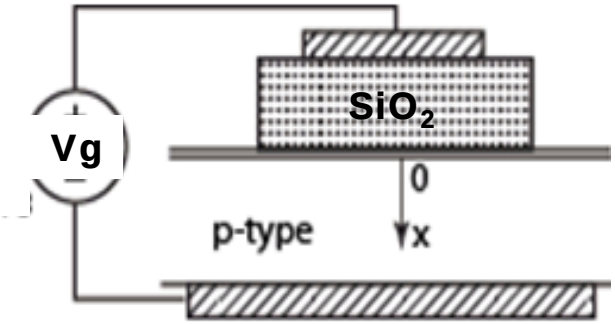
$V_G = V_{FB}$

$qV_{FB} = \Phi_M - \Phi_S$

$E_C(O)$ and **external** electric field direction



Effects of applied biases



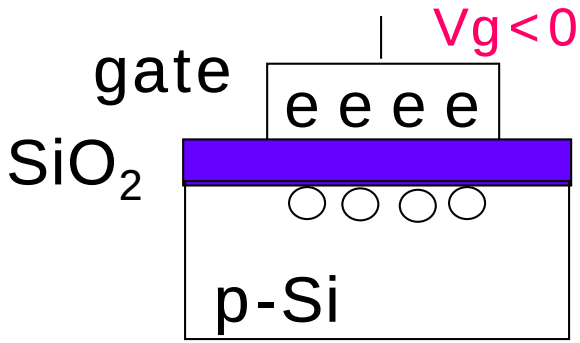
Vg increase from "-" to "+" :

1. $Vg < V_{FB} < 0$	Accumulation: Majority carriers
2. $Vg = V_{FB}$	Flatband
3. $V_m \geq Vg > V_{FB}$ including $Vg = 0$	Depletion: Majority carriers
4.1 $V_T > Vg > V_m$	Weak Inversion: Minority carriers
4.2 $Vg \geq V_T$	Strong Inversion: Minority carriers

What are V_{FB}, V_m and V_T?

1. Accumulation (p-type Si) : $Vg<V_{FB}<0$

Accumulation:
Majority carriers



- Physical process: Vg<0: holes **attracted** to the oxide/Si interface and accumulate there.
- Separation between “-” and “+” charges: oxide

1. Accumulation:

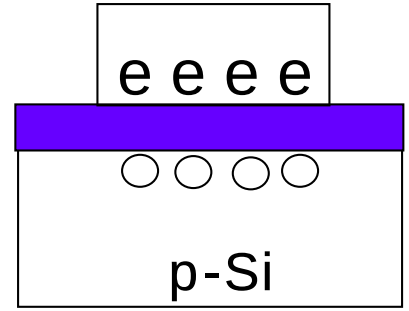
Energy band diagrams: Vg<0

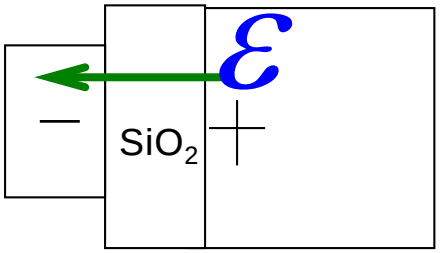
$qVg = E_{FS} - E_{FM}$

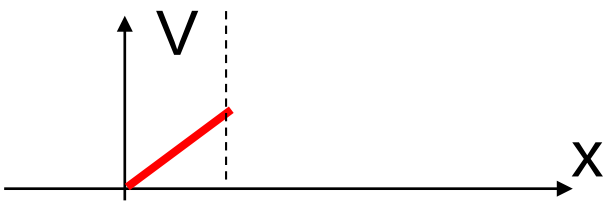
$Vg < 0$

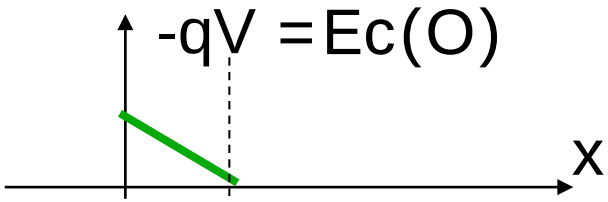
Two diagrams:
block charge density diagram & energy band diagram

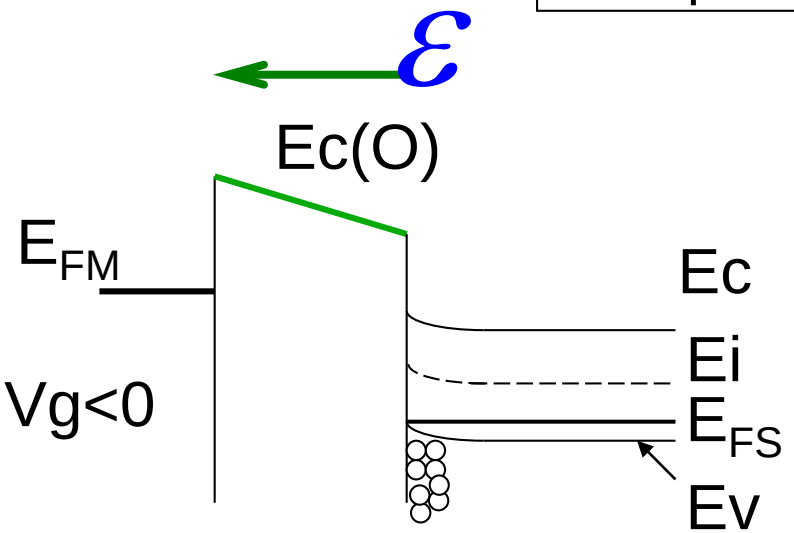
More negative: higher electron energy (band bending up)

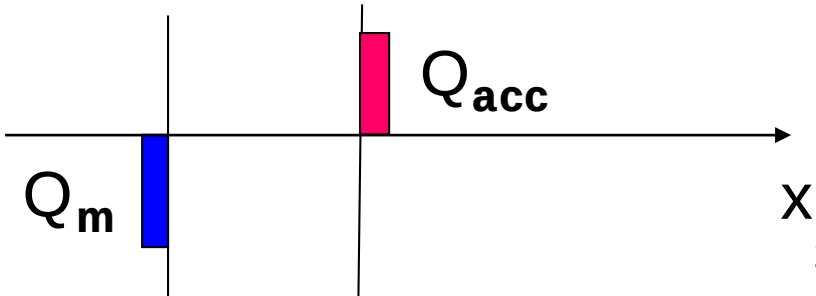












1. Accumulation:

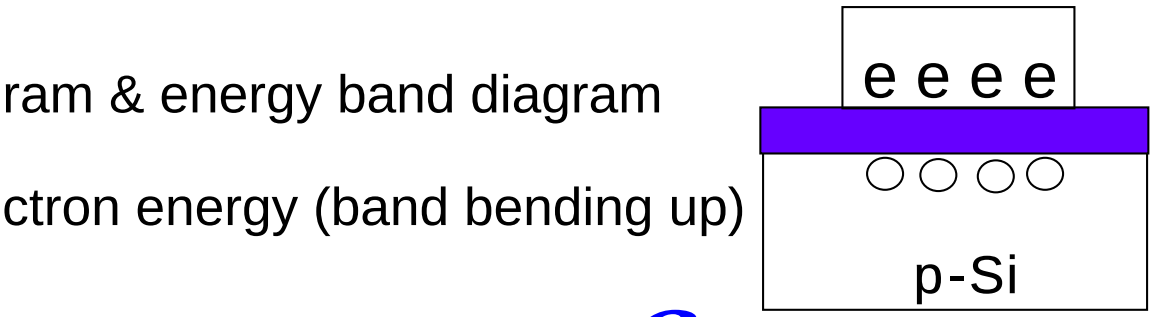
Energy band diagrams: Vg<0

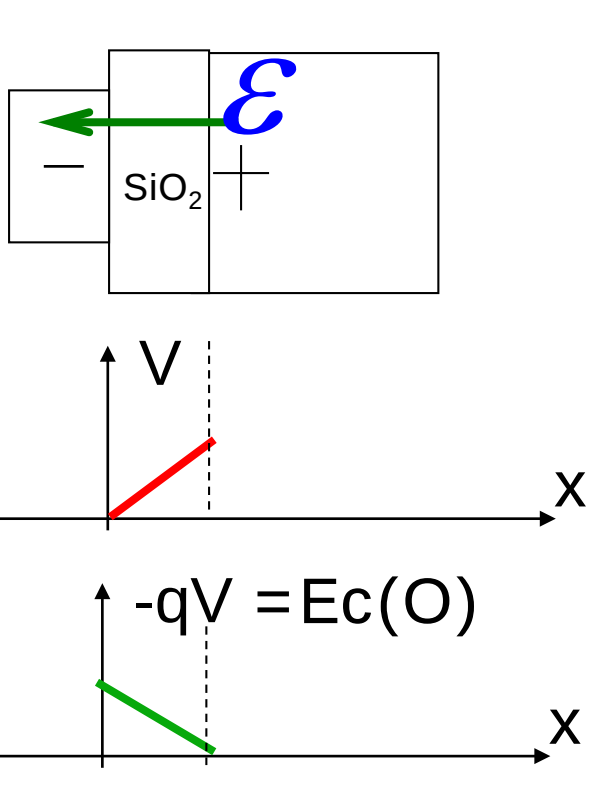
$qVg = E_{FS} - E_{FM}$

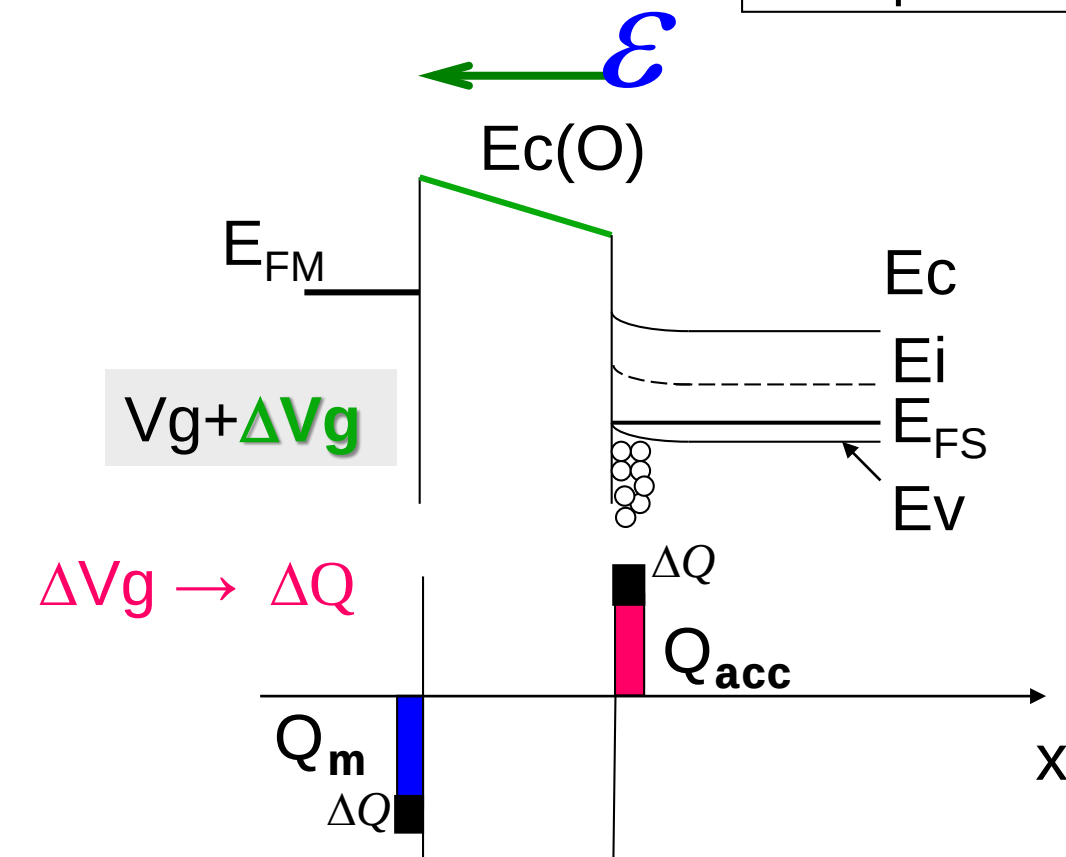
Vg < 0

Two diagrams:
block charge density diagram & energy band diagram

More negative: higher electron energy (band bending up)

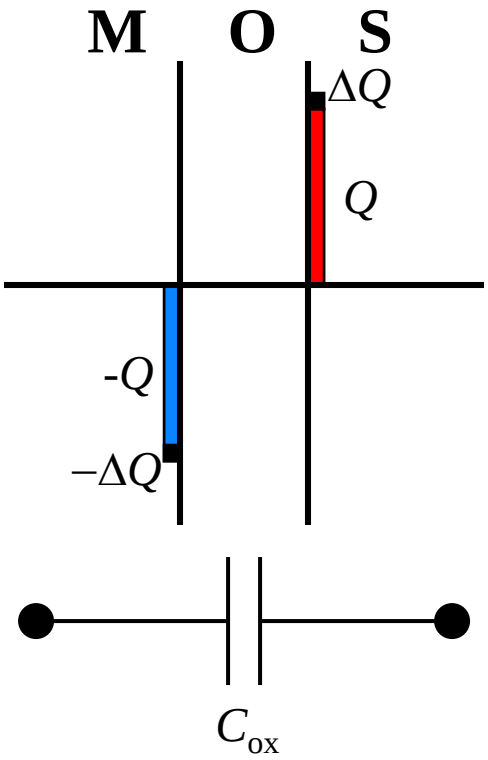






1. Capacitance in Accumulation

- As the gate voltage is varied, incremental charge is added/subtracted to/from the gate and substrate.
- The incremental charges are separated by the gate oxide.



$$C = \left| \frac{dQ_{acc}}{dV_g} \right| = C_{ox}$$

$$C = C_{ox} = \frac{\varepsilon_{ox} A}{t_{ox}} = \text{constant}$$

$\varepsilon_{r'ox}$=3.9 is the relative dielectric constant of the oxide, $\varepsilon_{ox}=\varepsilon_{r'ox}\varepsilon_o$, $\varepsilon_o=8.85\times10^{-12}$ F/m is the permittivity of free space, t_{ox} is the oxide thickness.

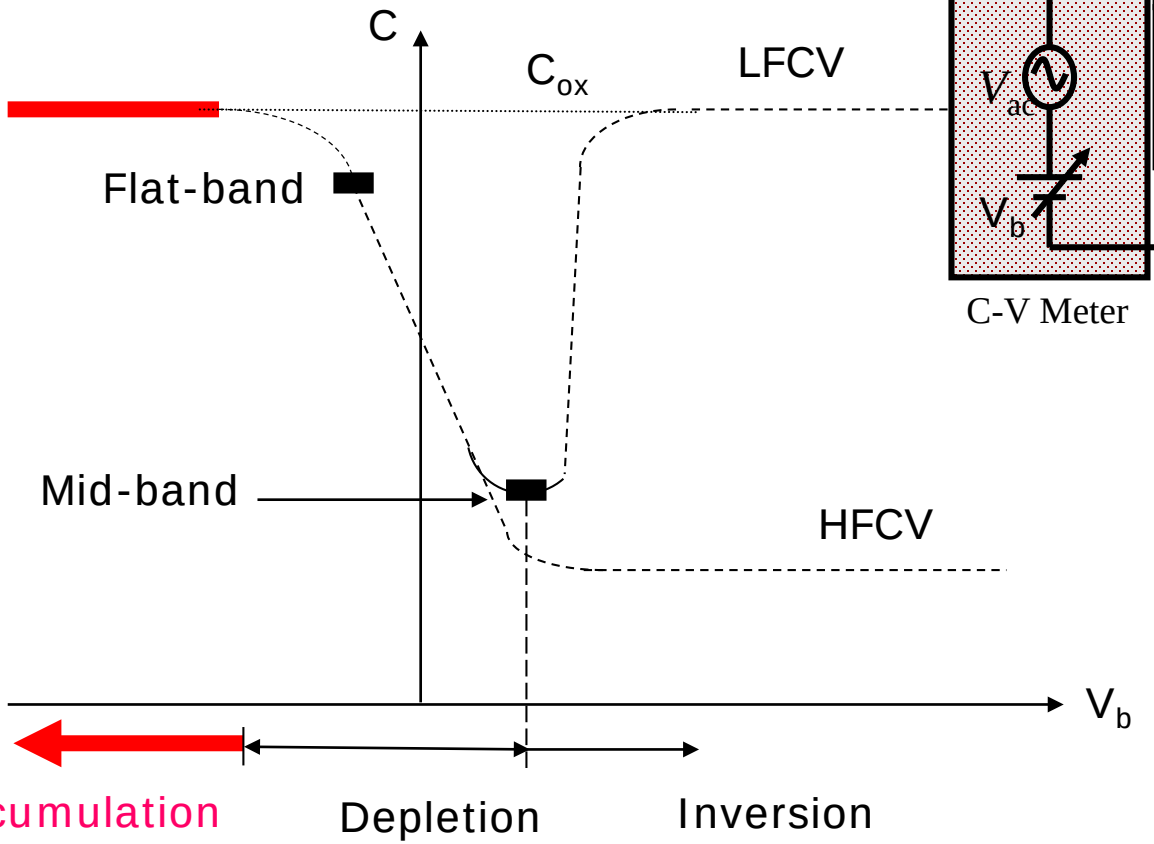
Normally, we consider the capacitance per unit area, so A=1

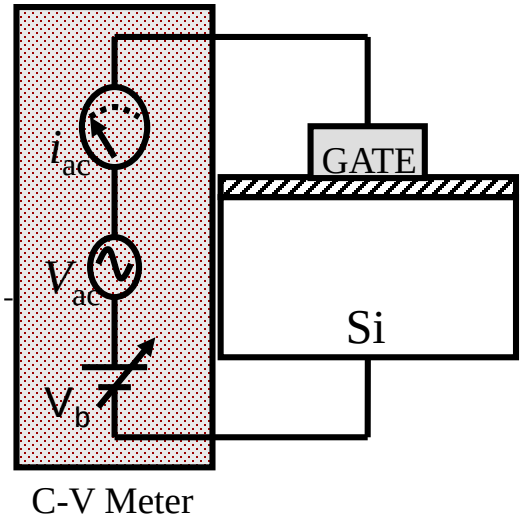
1. Accumulation:

Capacitance-voltage (C-V) characteristics

- Example: p-Si

$$C = C_{ox} = \frac{\varepsilon_{ox} A}{t_{ox}}$$

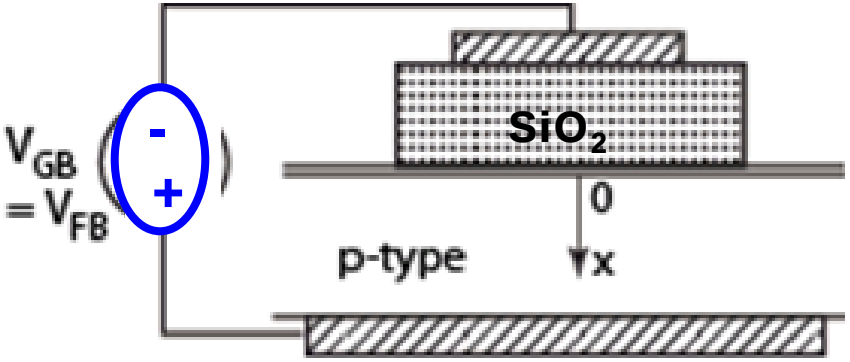


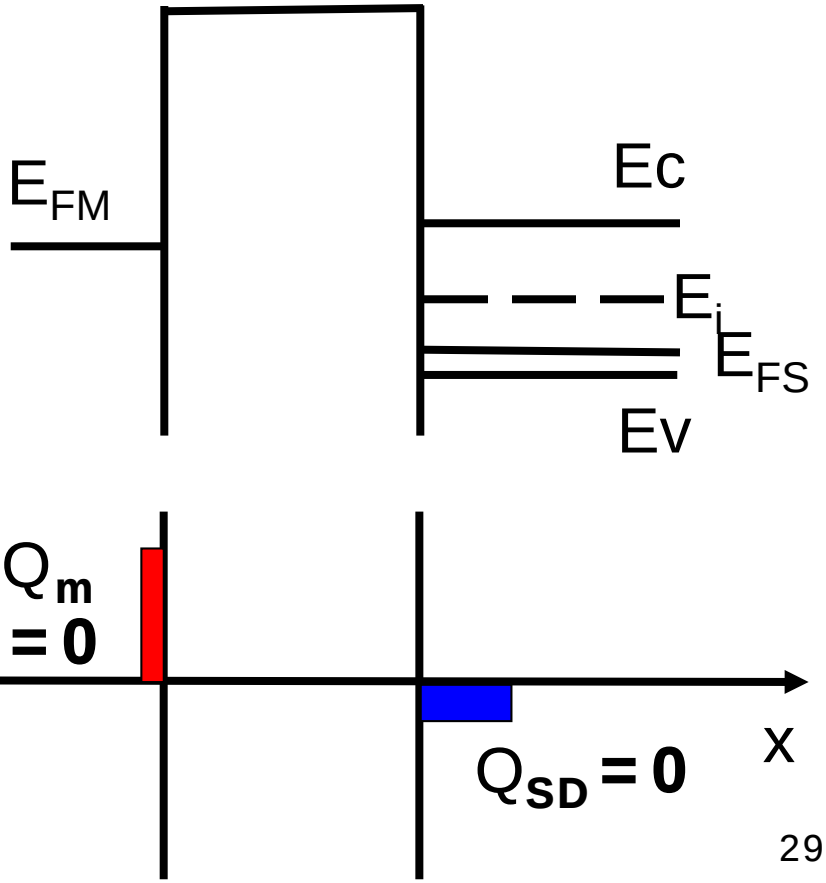


2. Flatband Voltage, V_{FB}

- The built-in potential can be "cancelled out" by applying a gate voltage that is equal in magnitude (but of the opposite polarity) as the built-in potential. This gate voltage is called the ***flatband voltage*** because the resulting potential profile is flat.

$Vg=V_{FB}$





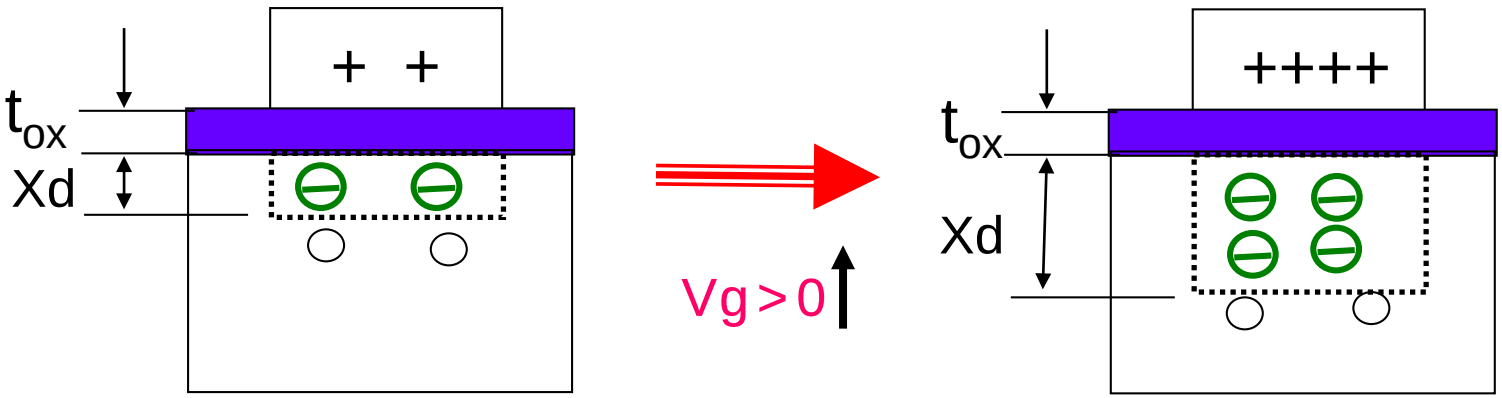
There is no net charge (*i.e.* $\rho(x)=0$) in the semiconductor under $V_{GB} = V_{FB}$.

3. Depletion: Vg > V_{FB}

- Physical process:
  - holes **repelled** from the interface
  - fixed negative charge left behind
  - More "+" charges on the gate, holes are pushed further from the interface, to expose more "-" space charges.

○: Hole

⊖ : B^-

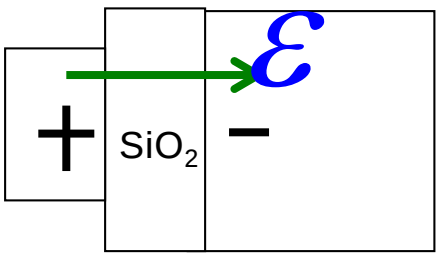


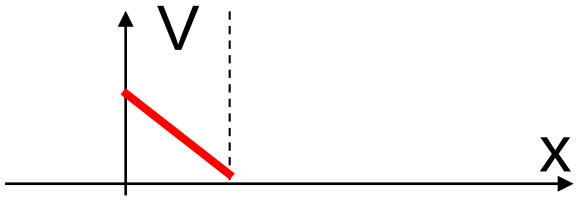
3. Depletion:

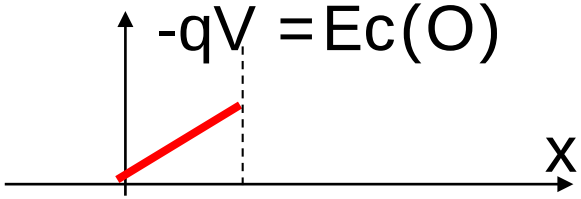
Energy band diagram: $Vg>V_{FB}$

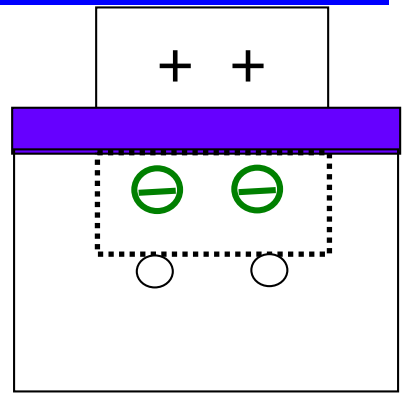
$qVg = E_{FS} - E_{FM}$

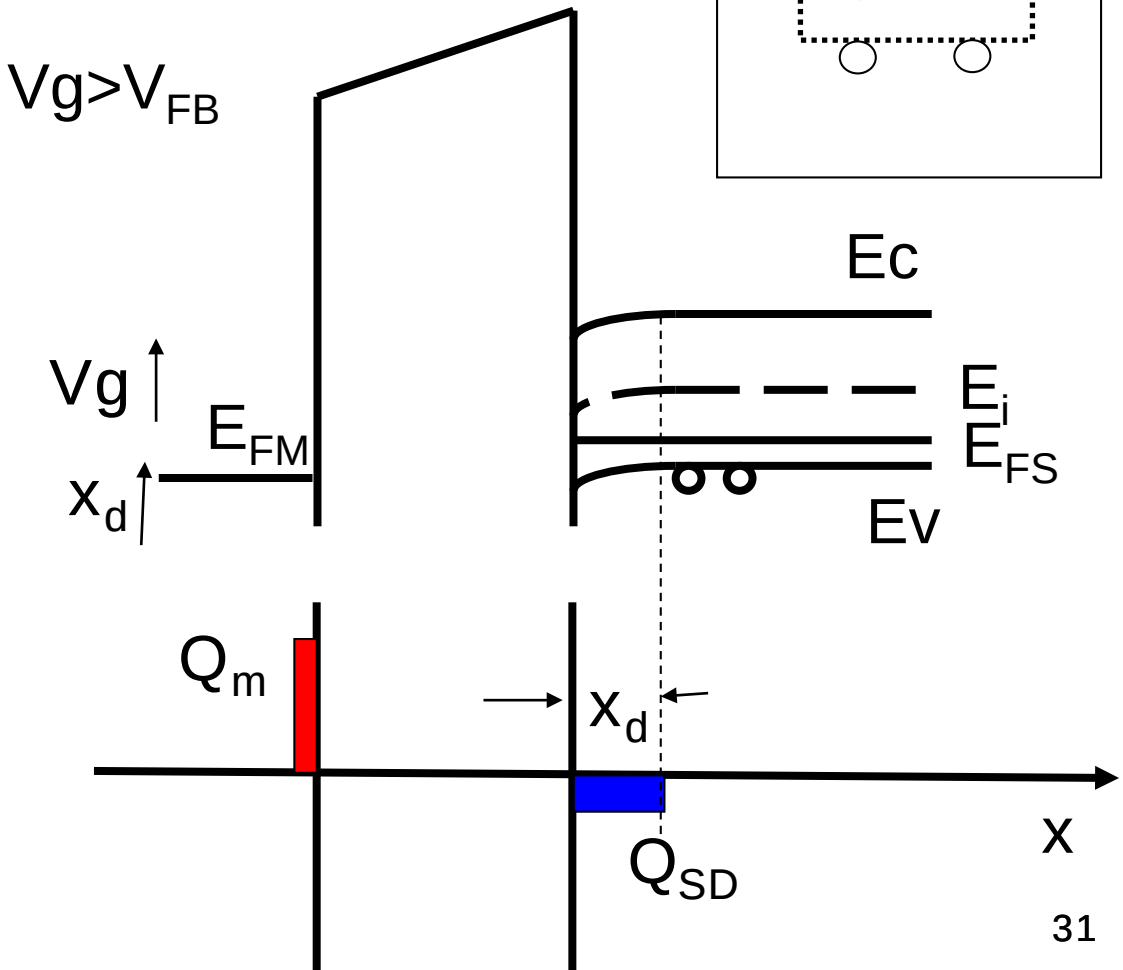
- The band is bent downward now.
- No mobile charges at the interface.









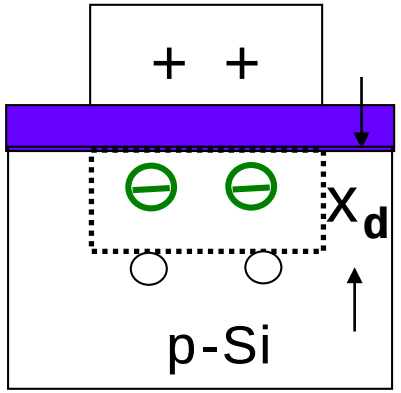


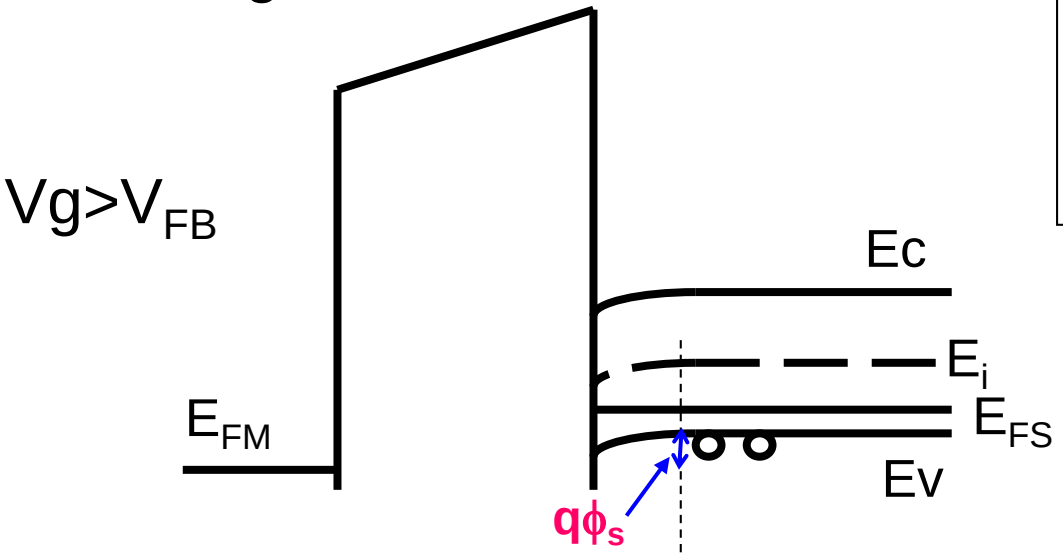
3. Depletion:

Energy band diagram: $Vg>V_{FB}$

$qVg = E_{FS} - E_{FM}$

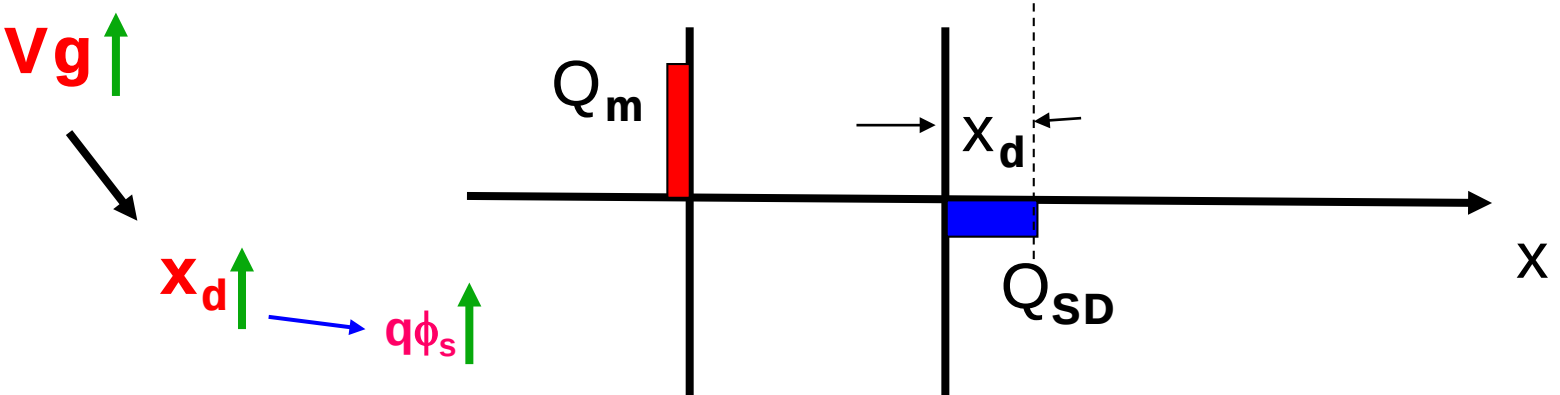
- The band is bent downward now.
- No mobile charges at the interface.





○ : Hole

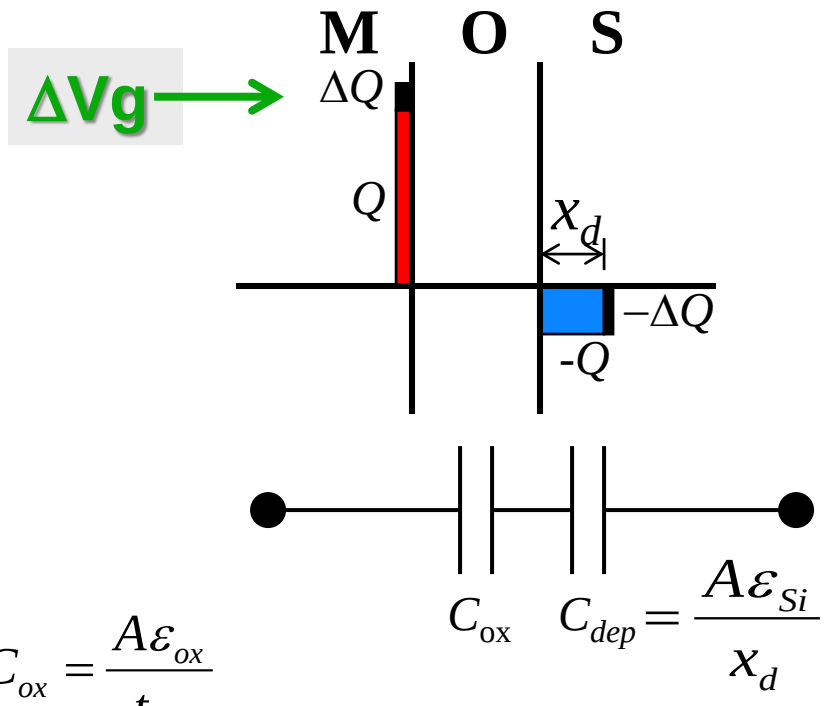
⊖ : **B⁻**



3. Capacitance in Depletion

- As the gate voltage is varied, the width of the depletion region varies.

→ Incremental charge is effectively added/subtracted at a depth x_d in the substrate.



$$C_{ox} = \frac{A\varepsilon_{ox}}{t_{ox}}$$

$$C = \left|\frac{dQ}{dV_G}\right|$$

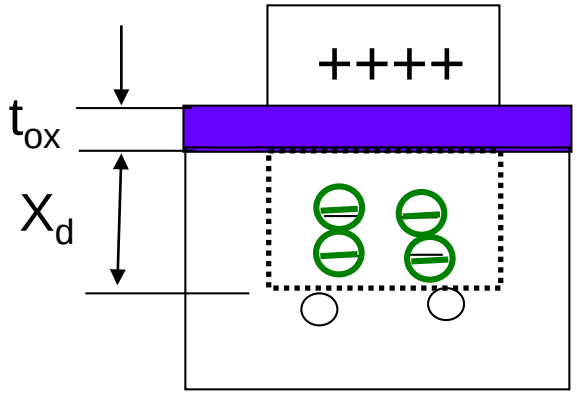
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} = \frac{1}{C_{ox}} + \frac{x_d}{A\varepsilon_{Si}}$$

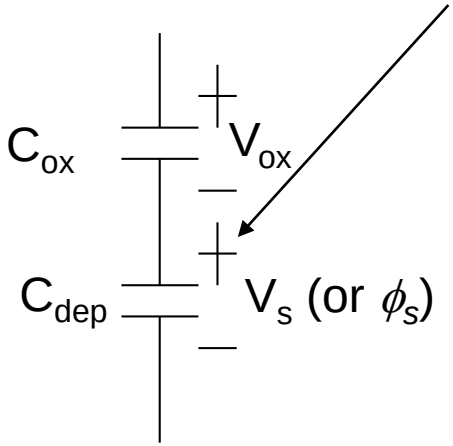
$\varepsilon_{r'Si} = 11.9$ is the relative dielectric constant of silicon, $\varepsilon_{Si} = \varepsilon_{r'Si}\varepsilon_o$.

$V_g \uparrow \rightarrow x_d \uparrow \rightarrow C \downarrow$

3. Depletion Capacitance

- Capacitance





$$C_{ox} = \frac{A\varepsilon_{ox}}{t_{ox}}$$

$$C_{dep} = \frac{A\varepsilon_{Si}}{x_d}$$

- When Vg increases, Xd increases and C_{dep} reduces. This in turn reduces C.
- Solving Poisson's equation, we have

$$x_d = \left(\frac{2\varepsilon_{Si} V_S}{qN_a} \right)^{1/2}$$

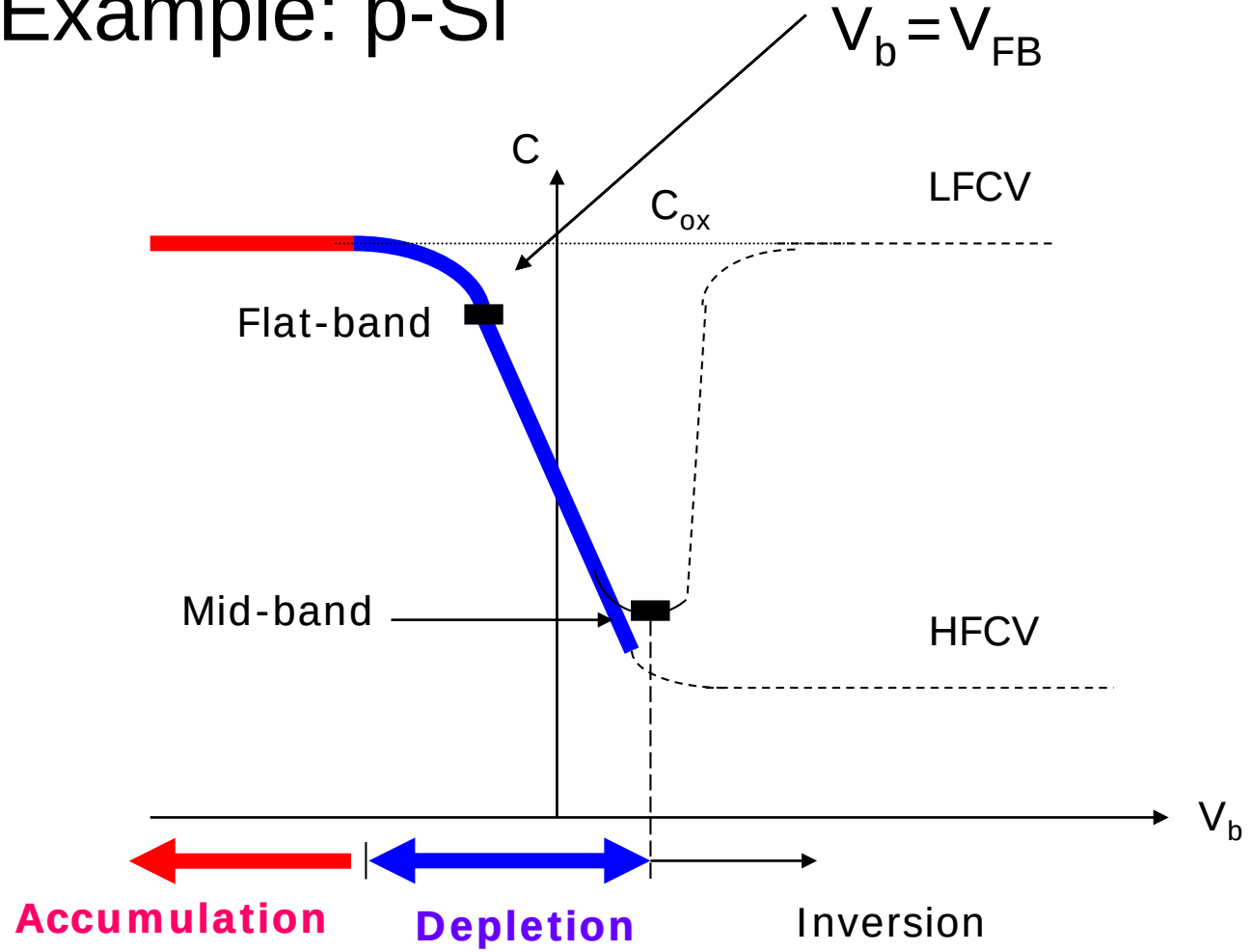
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} = \frac{1}{C_{ox}} + \frac{x_d}{A\varepsilon_{Si}}$$

$V_g \uparrow \rightarrow x_d \uparrow \rightarrow C \downarrow$

3. Depletion:

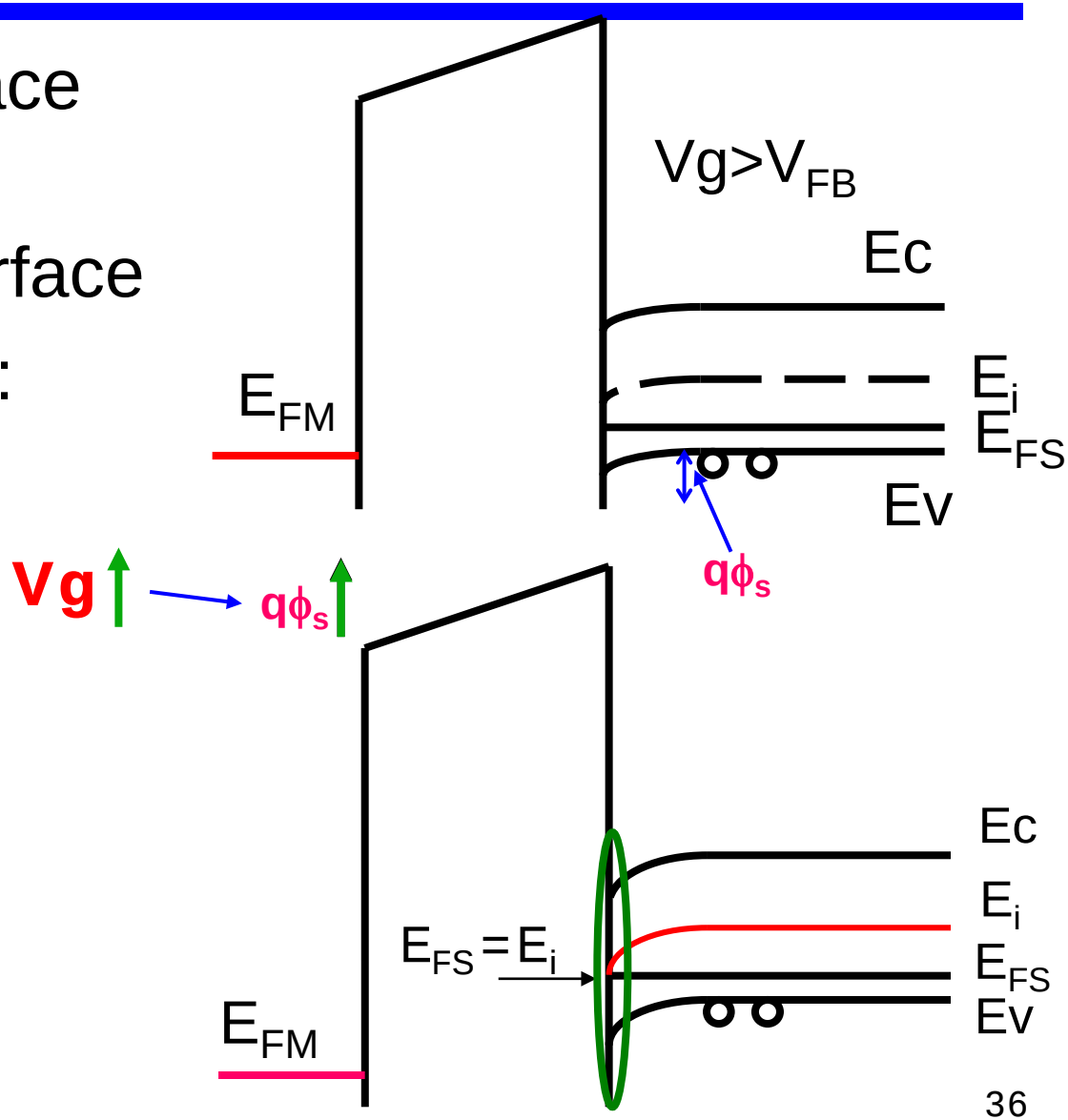
Capacitance-voltage (C-V) characteristics

- Example: p-Si



Midband: further increase Vg

- E_{FS} = Ei at interface
- Silicon becomes **"intrinsic"** at surface
- This is 'Midband': Vg=Vm



At the interface

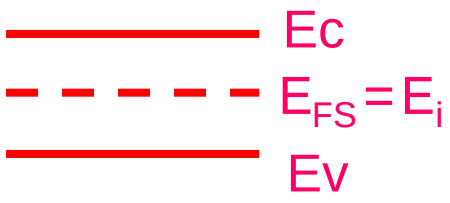
Ec

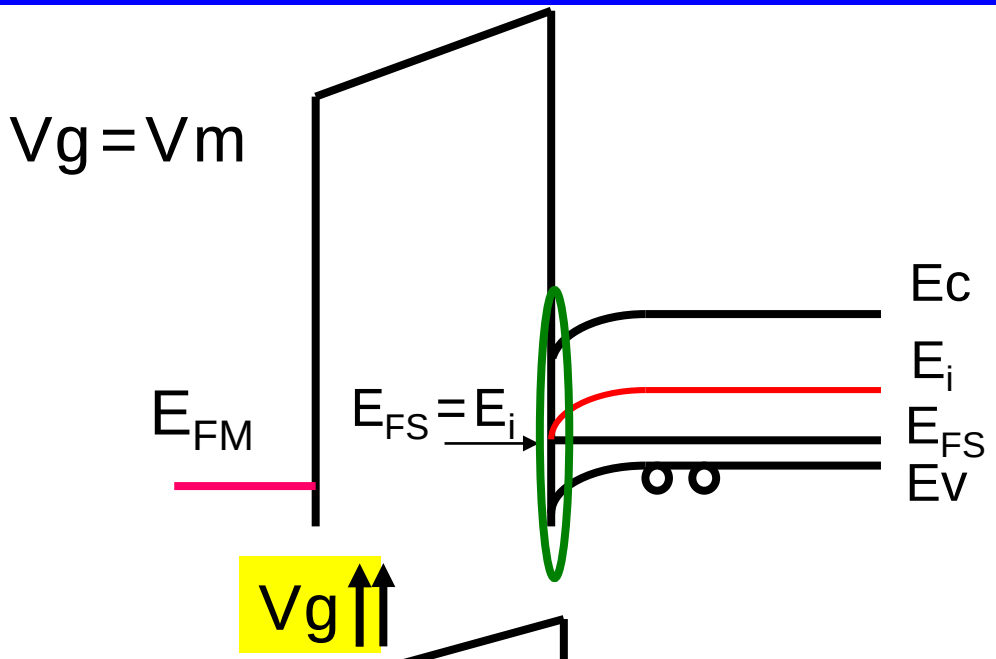
$E_{FS}=E_i$

Ev

Further increase Vg

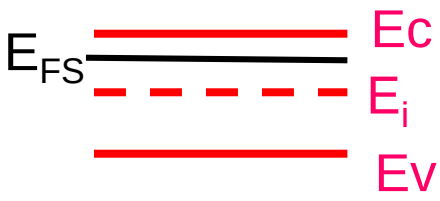
At the interface

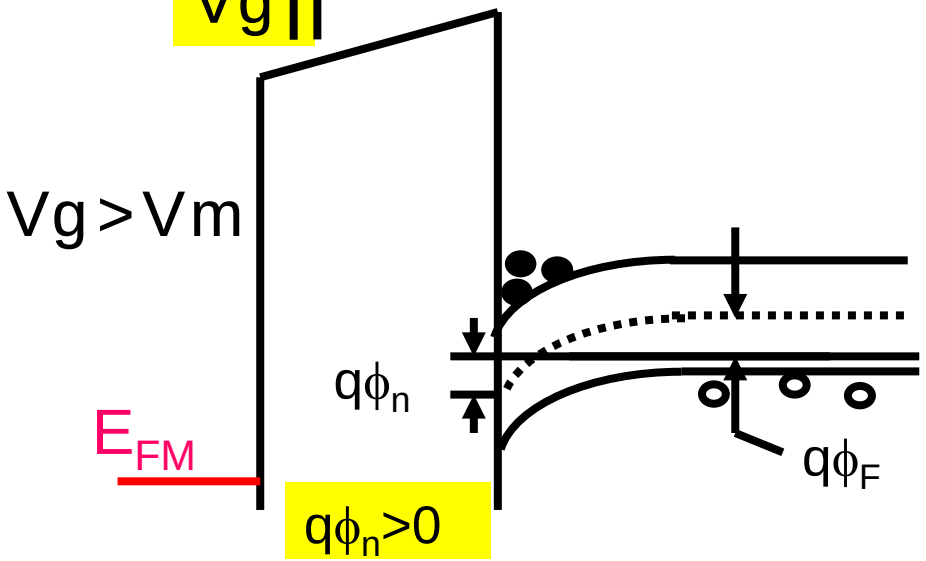




Vg↑↑

At the interface



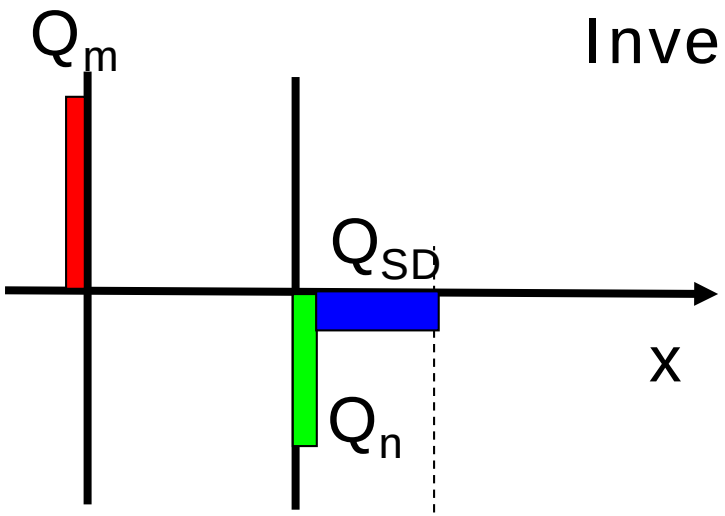


$qVg = E_{FS} - E_{FM}$

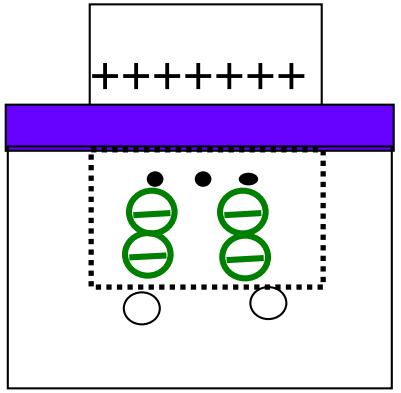
4. Energy band diagram: $Vg > V_m$

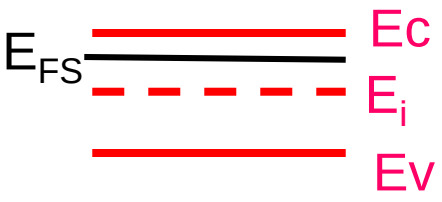
Vg ↑↑

As $Vg > Vm$, E_{FS} is at the up-half of the bandgap

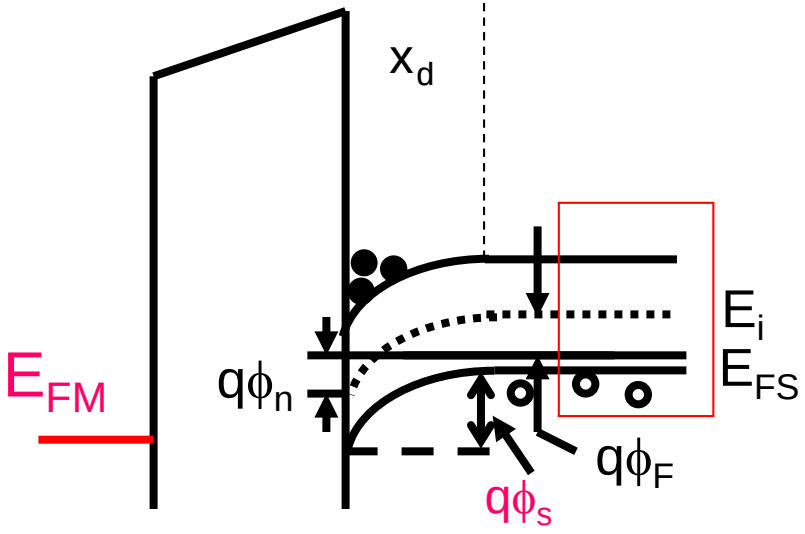


Inversion: Minority carriers





At the interface



surface potential

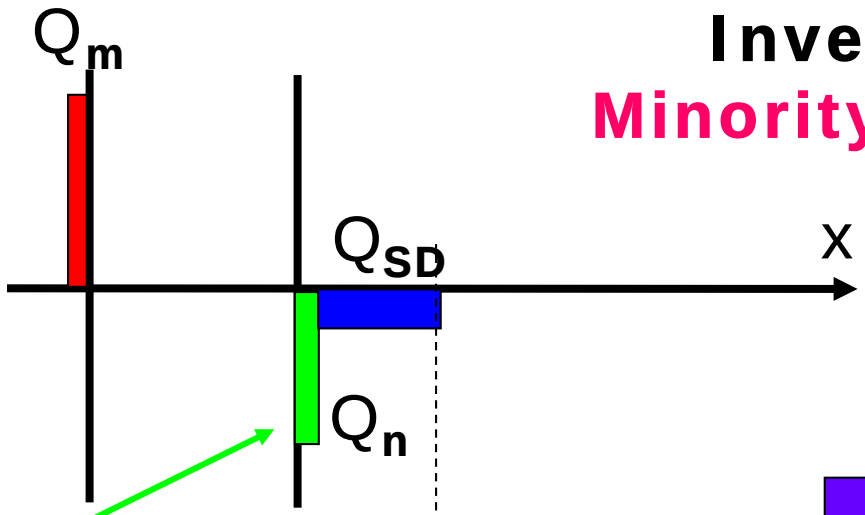
$\phi_s = \phi_F + \phi_n$

4. Energy band diagram: $Vg > V_m$

Vg ↑↑ → $q\phi_s$ ⇑⇑

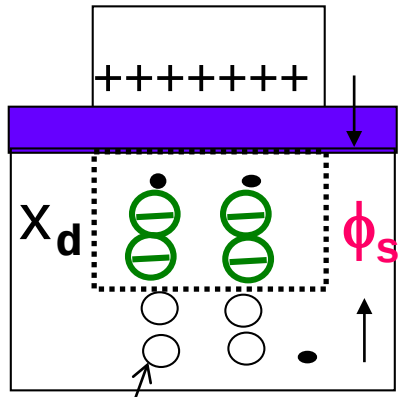
As Vg>Vm, E_{FS} is at the up-half of the bandgap.

Inversion:
Minority carriers



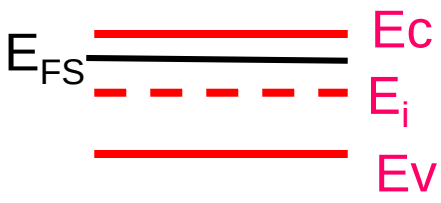
$$n = n_i \exp\left[\frac{(E_F - E_i)}{kT}\right]$$

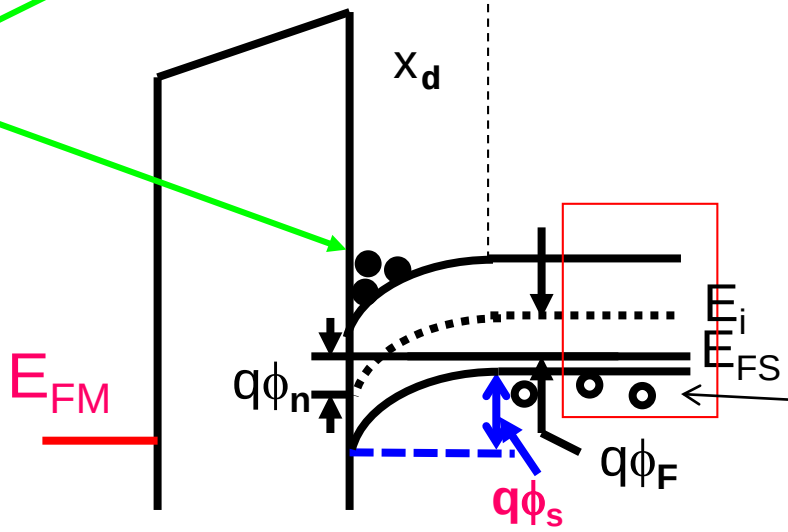
$$\Rightarrow n_s = n_i \exp\left[\frac{q\phi_n}{kT}\right]$$



$$np = n_i^2$$

At the interface





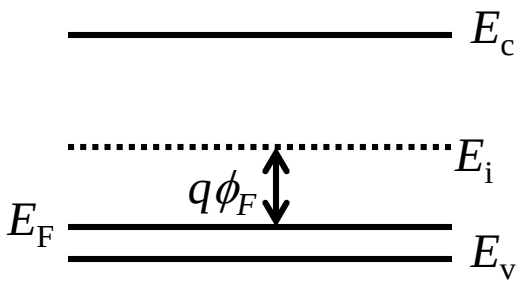
$$p = n_i \exp\left[\frac{q\phi_F}{kT}\right]$$

Bulk Semiconductor Potential, ϕ_F

$$q\phi_F \equiv E_i - E_F$$

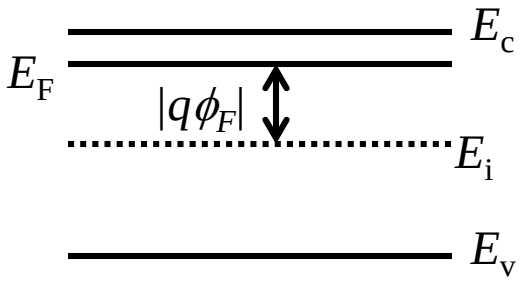
- p-type Si:

$$\phi_F = \frac{kT}{q}\ln(N_A / n_i) > 0$$



- n-type Si:

$$\phi_F = -\frac{kT}{q}\ln(N_D / n_i) < 0$$

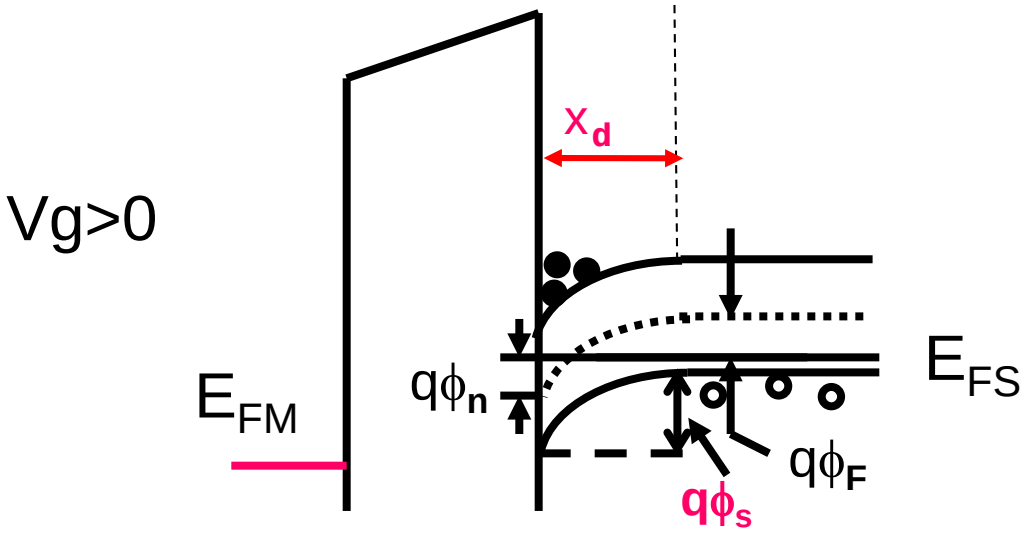


or $q\phi_F \equiv -(E_i - E_F)$

4. Inversion

$$p = n_i \exp\left[\frac{q\phi_F}{kT}\right]; \qquad n_s = n_i \exp\left[\frac{q\phi_n}{kT}\right]$$

- Physical process and band diagram
  - As Vg>Vm, E_{FS} is at the up-half of the bandgap.
  - Si near interface becomes n-type.
    - Many electrons (now majority carriers).
  - Weak Inversion: $0<\phi_n<\phi_F$ $(\phi_F < \phi_S < 2\phi_F)$
  - Strong Inversion: $\phi_n \geq \phi_F$ $(\phi_S \geq 2\phi_F)$, electron density at the interface ≥ hole density in Si bulk.
  - Vg for strong inversion: $\geq V_T$ 'threshold voltage'.



$\phi_s = \phi_F + \phi_n$

$Vg=Vm, \phi_n = 0$

$Vg=V_T, \phi_n = \phi_F$

$\rightarrow \phi_s = 2\phi_F$

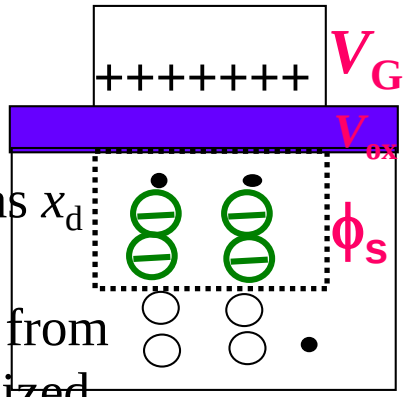
$\phi_s = \phi_F + \phi_n$

Maximum Depletion Depth, $x_{d,max}$

- As **V_G is increased above V_T**, ϕ_S and hence the depth of the depletion region (x_d) increases very slowly.

→ $\phi_s \approx 2\phi_F$

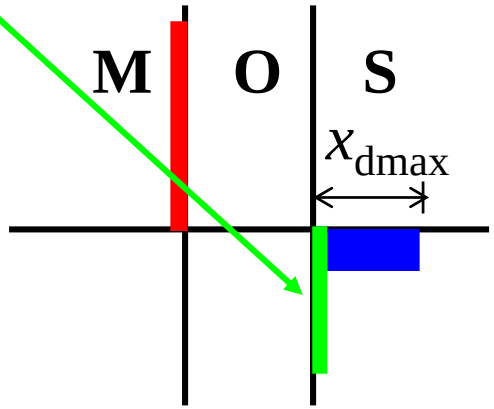
  - This is because n increases exponentially with ϕ_S, whereas x_d increases with the square root of ϕ_S. Thus, most of the incremental negative charge in the semiconductor comes from additional conduction electrons rather than additional ionized acceptor atoms, when n exceeds N_A



$$n_s = n_i \exp\left[\frac{q\phi_n}{kT}\right]; \qquad \phi_n = \phi_s - \phi_F$$

→ x_d can be reasonably approximated to reach a maximum value ($x_{d,max}$) for $V_G \geq V_T$.

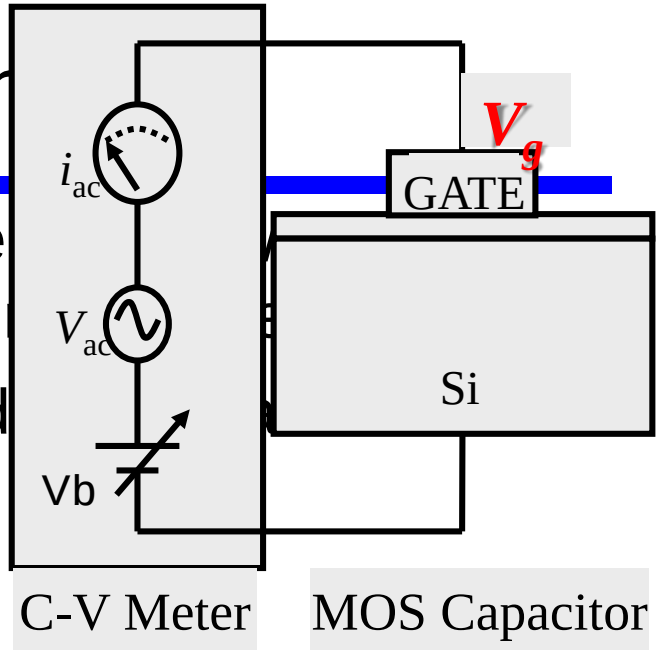
$$x_{d,\max} = \sqrt{\frac{2\varepsilon_{Si}\phi_s}{qN_A}} \approx \sqrt{\frac{2\varepsilon_{Si}(2\phi_F)}{qN_A}}$$

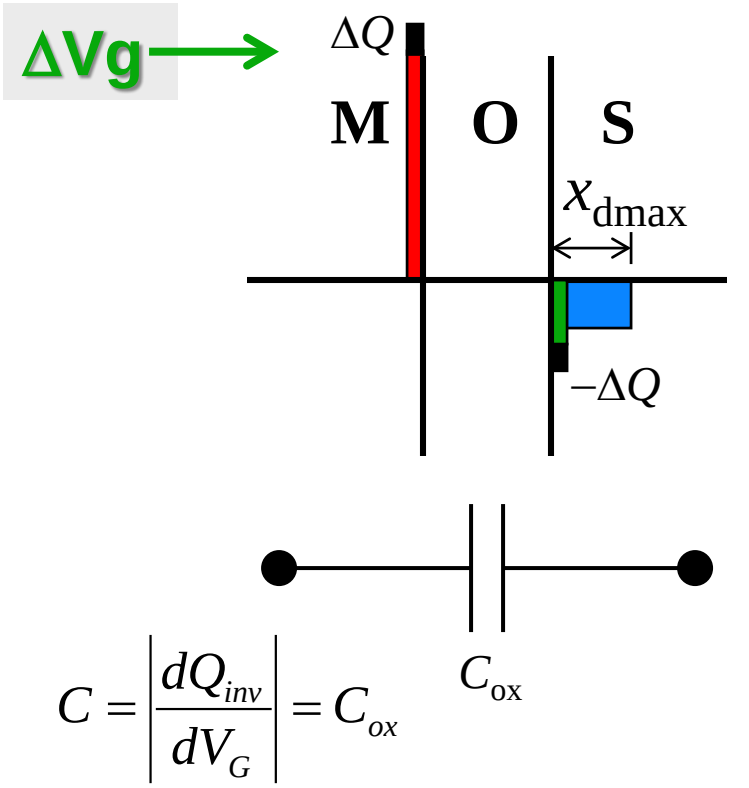


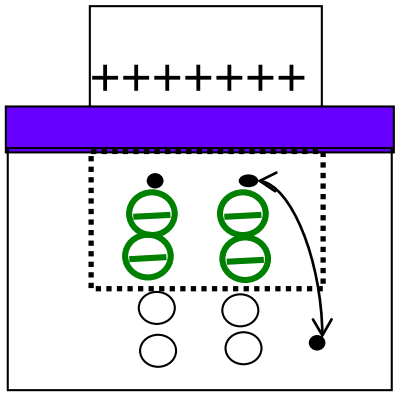
4. Capacitance in Inversion

CASE 1: Inversion-layer charge *can* be
quickly enough to respond to changes i

→ Incremental charge is effectively add
surface of the substrate.







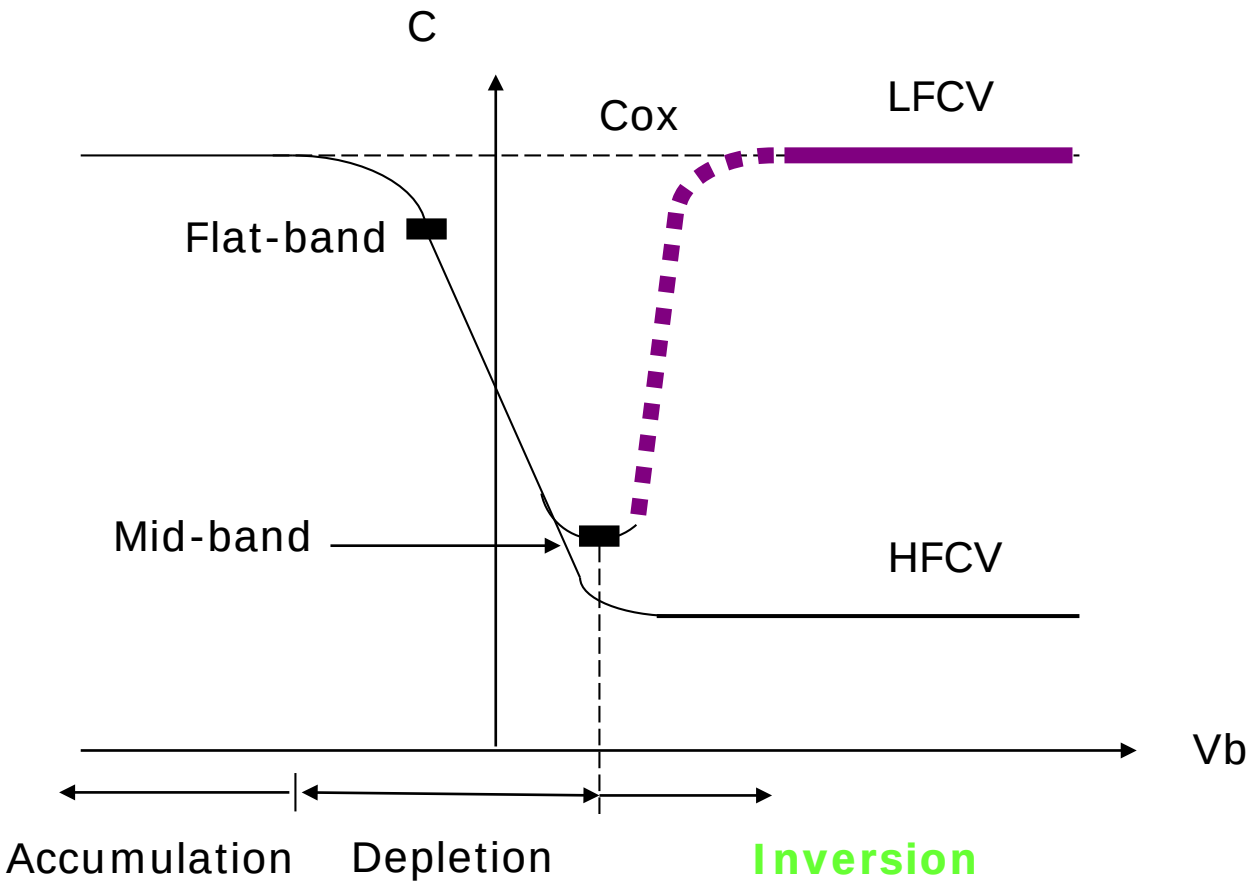
Electrons can respond to the change in Vac

4. Inversion:

C = dQ / dVac

CASE 1: Capacitance-voltage (C-V) characteristics

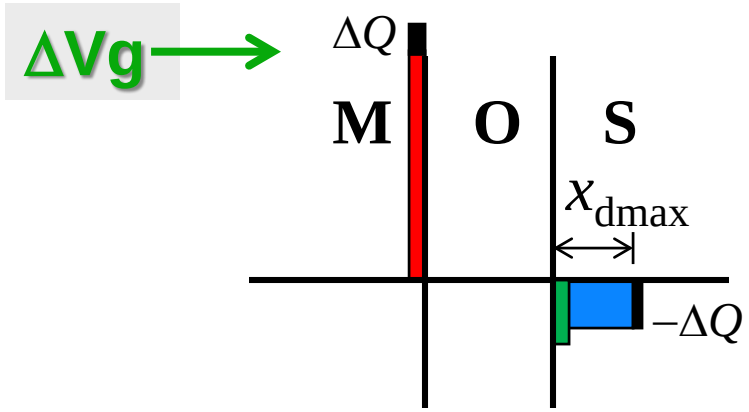
- Example: p-Si

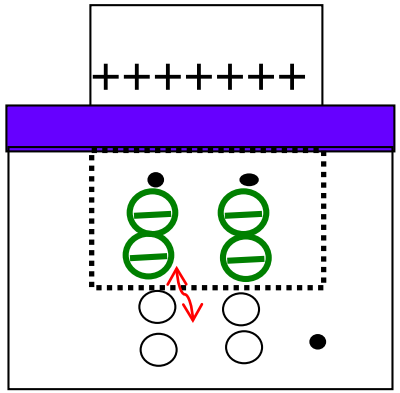


4. Capacitance in Inversion: HF

CASE 2: Inversion-layer charge *cannot* be supplied/removed quickly enough to respond to changes in the gate voltage.

→ Incremental charge is effectively added/subtracted at a depth x_{dmax} in the substrate.



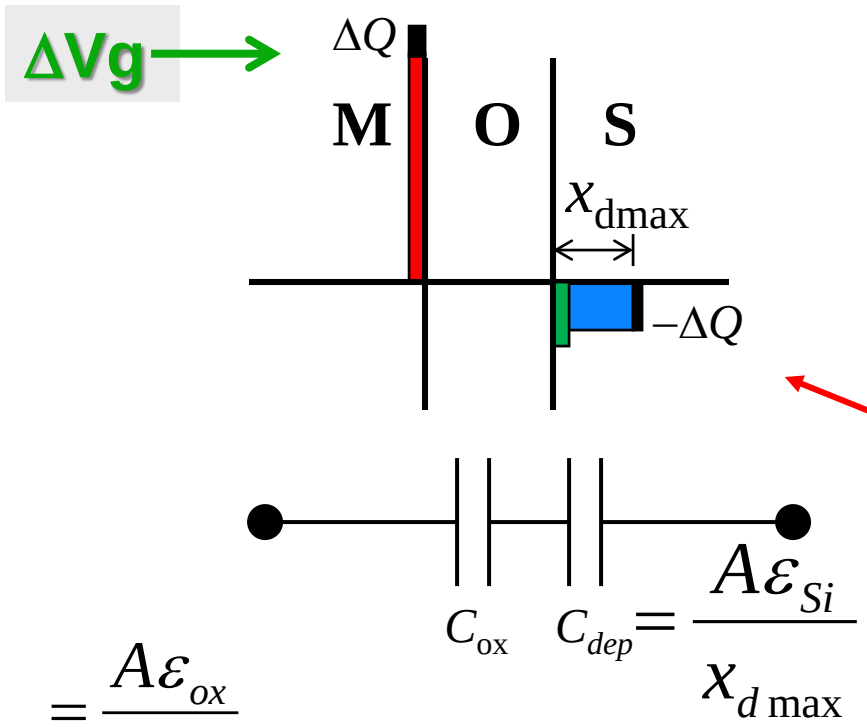


1. When Vac changes rapidly (e.g., 1MHz), electron creation cannot keep up.
2. Negative charges supplied by pushing holes away.

4. Capacitance in Inversion: HF

CASE 2: Inversion-layer charge *cannot* be supplied/removed quickly enough to respond to changes in the gate voltage.

→ Incremental charge is effectively added/subtracted at a depth x_{dmax} in the substrate.



$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

$$= \frac{1}{C_{ox}} + \frac{x_{d\,max}}{A\varepsilon_{Si}} \equiv \frac{1}{C_{min}}$$

1. When Vac changes rapidly (e.g., 1MHz), electron creation cannot keep up.
2. Negative charges supplied by pushing holes away.

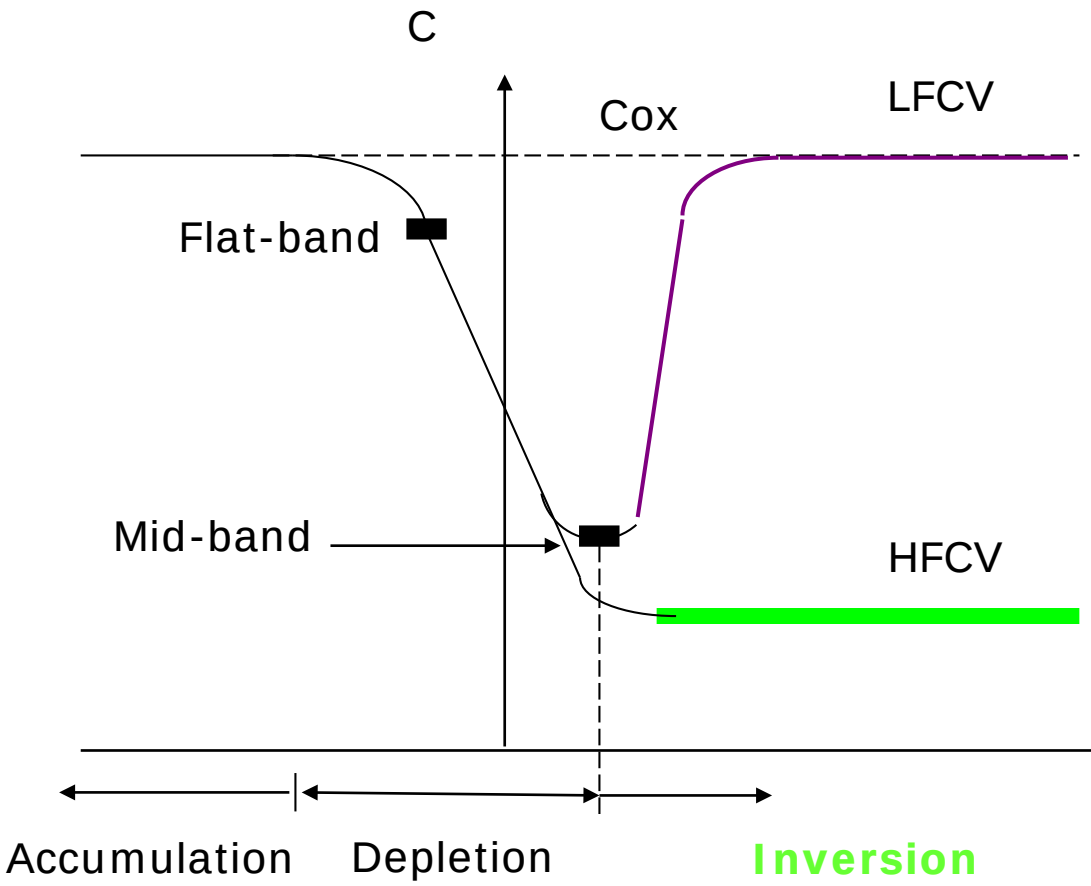
$$C_{ox} = \frac{A\varepsilon_{ox}}{t_{ox}}$$

4. Inversion

C=dQ/dVac

CASE 2: Capacitance-voltage (C-V) characteristics

- Example: p-Si

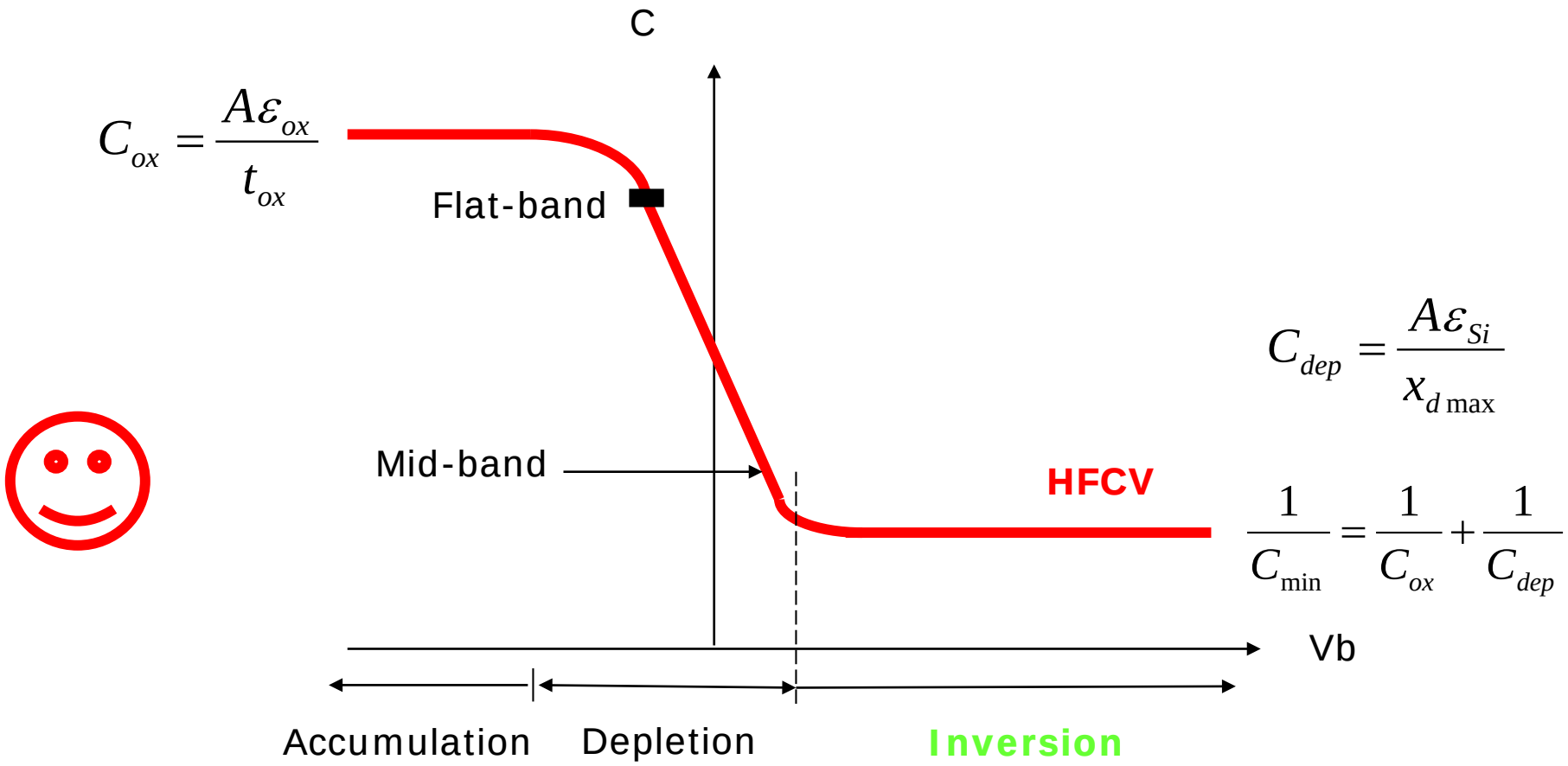


$$C_{dep} = \frac{\varepsilon_s}{x_{d\max}}$$

$$\frac{1}{C_{\min}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

Capacitance-voltage (C-V) characteristics

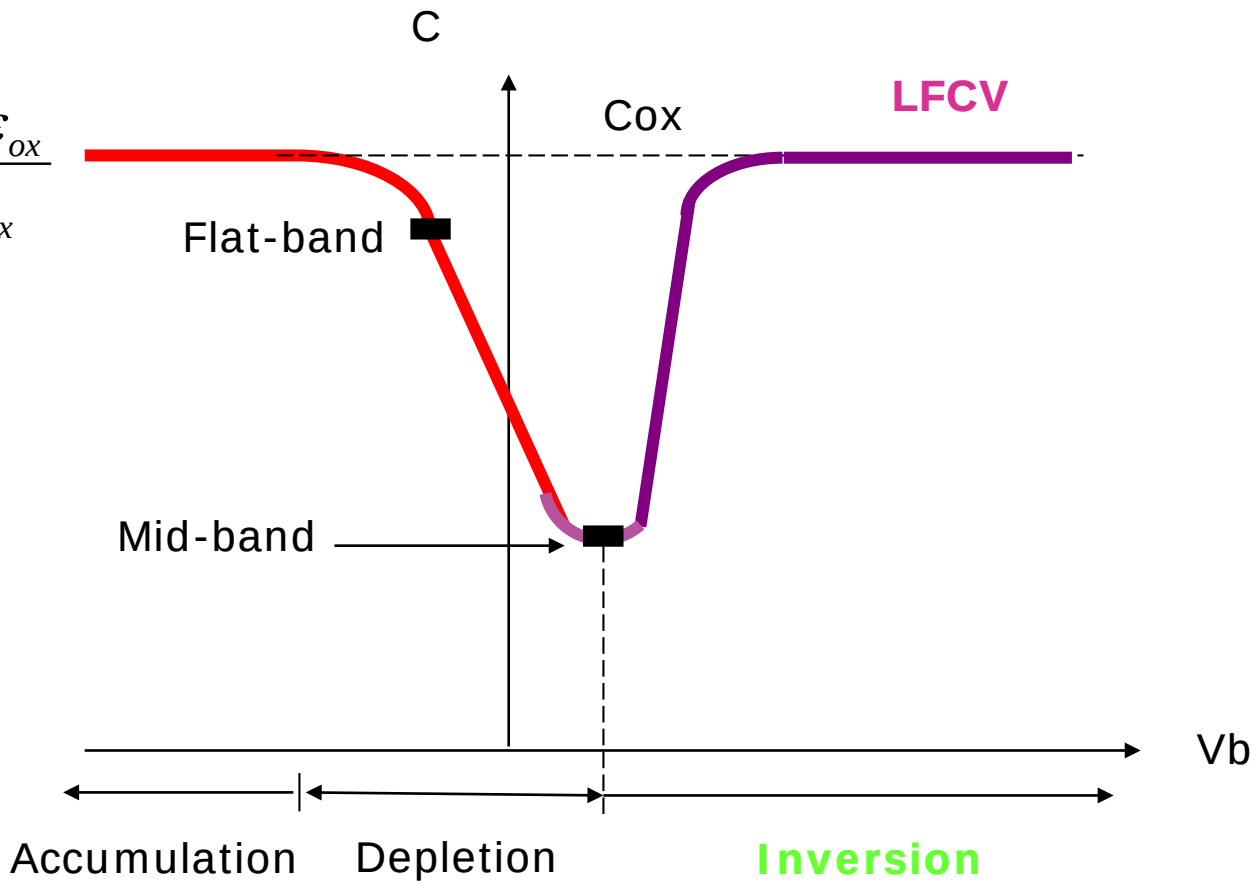
- Example: **p-Si**



Capacitance-voltage (C-V) characteristics

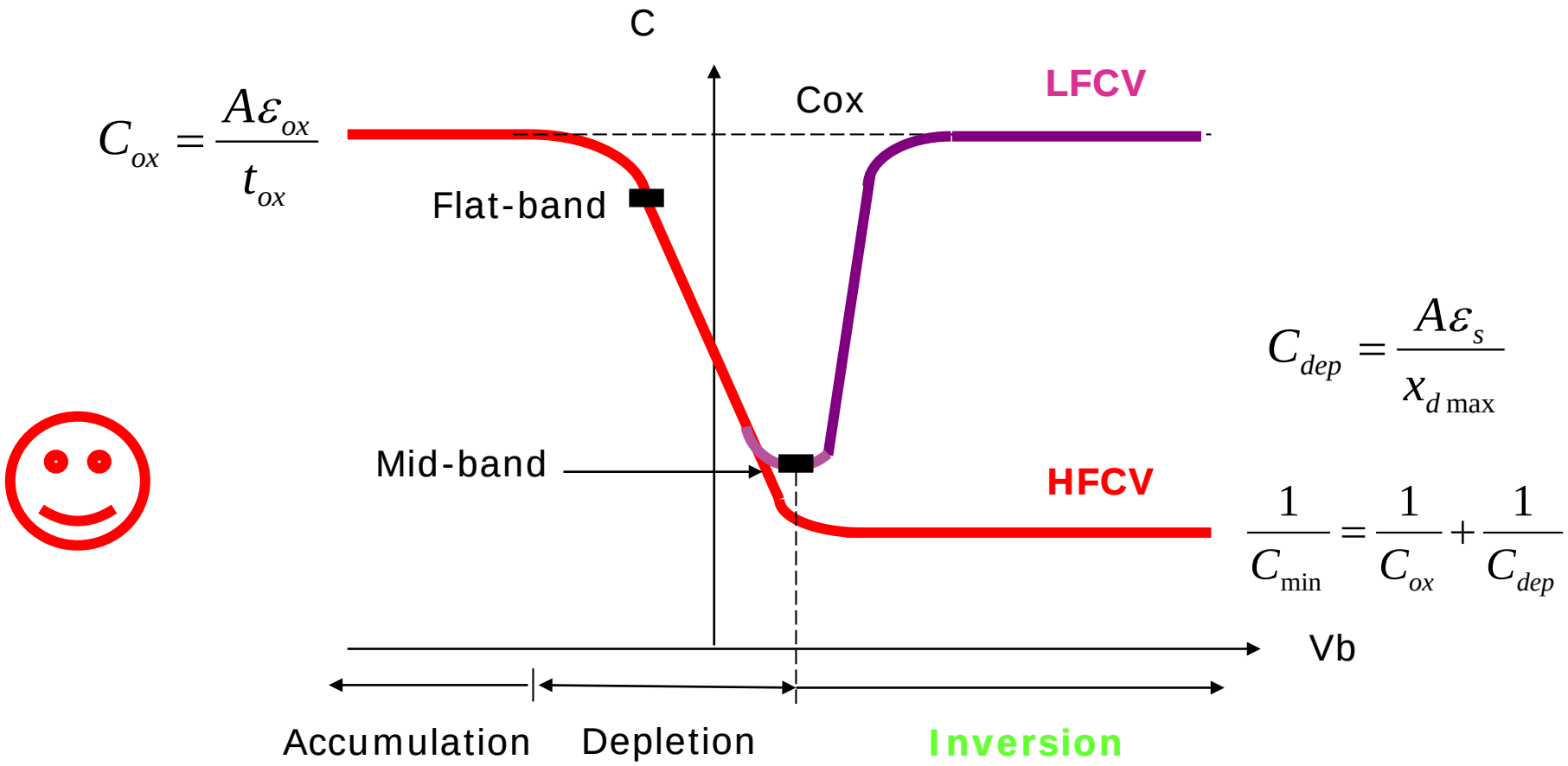
- Example: **p-Si**

$$C_{ox} = \frac{A\varepsilon_{ox}}{t_{ox}}$$



Capacitance-voltage (C-V) characteristics

- Example: **p-Si**

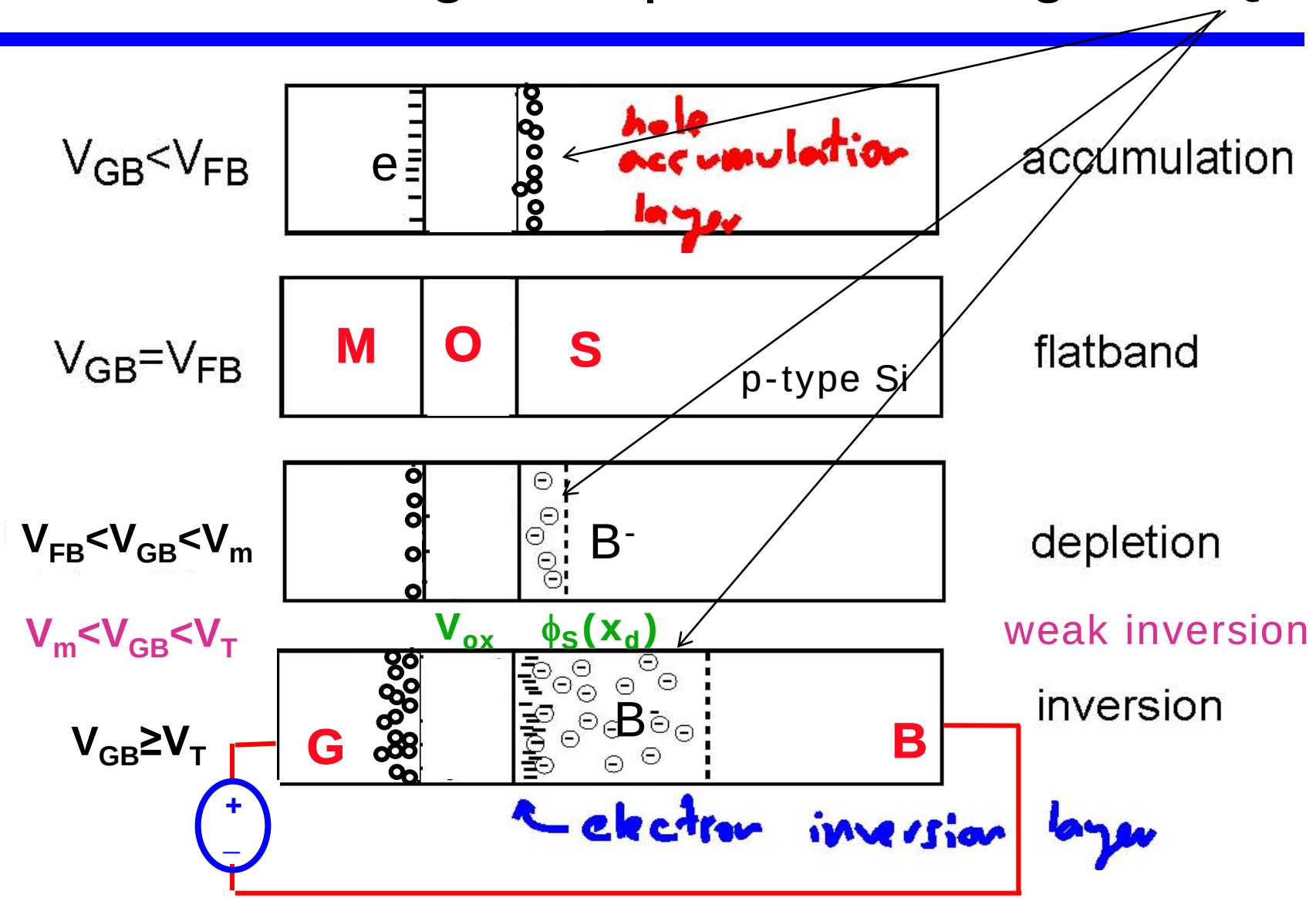


$$C_{ox} = \frac{A\varepsilon_{ox}}{t_{ox}}$$

$$C_{dep} = \frac{A\varepsilon_s}{x_{d\max}}$$

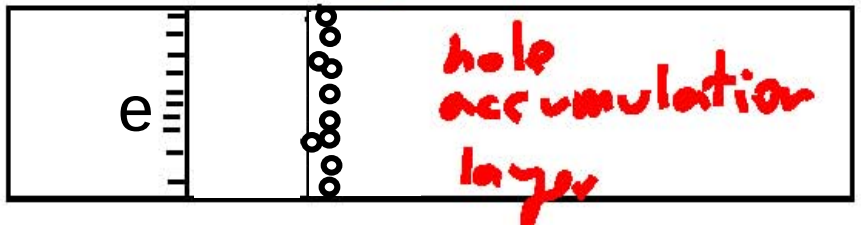
$$\frac{1}{C_{\min}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

Review: Voltage drops and charges

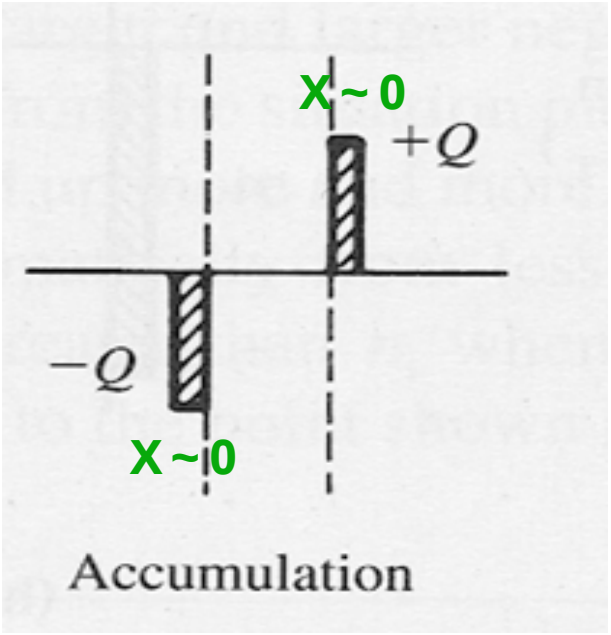


Review: Voltage drops and charges

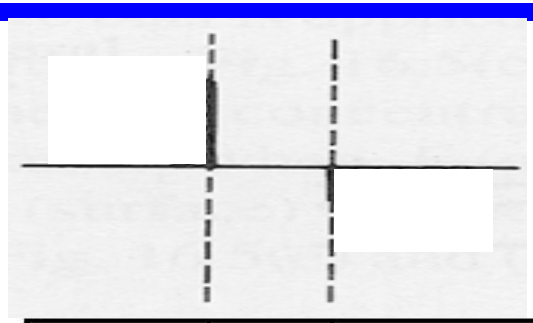
$V_{GB}<V_{FB}$



accumulation



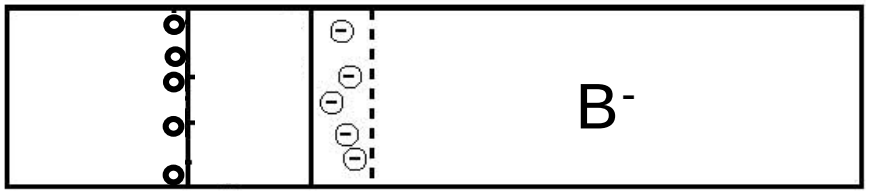
Review: Voltage drops and charges



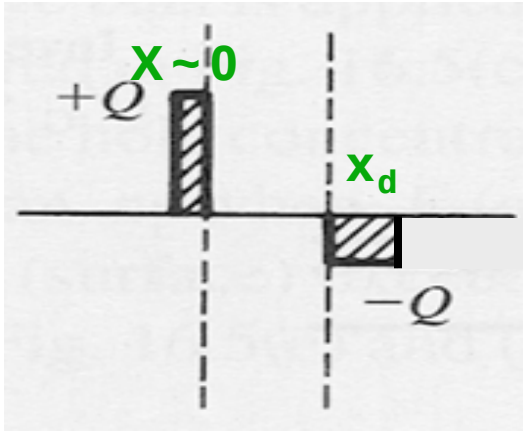
$V_{GB}=V_{FB}$

flatband

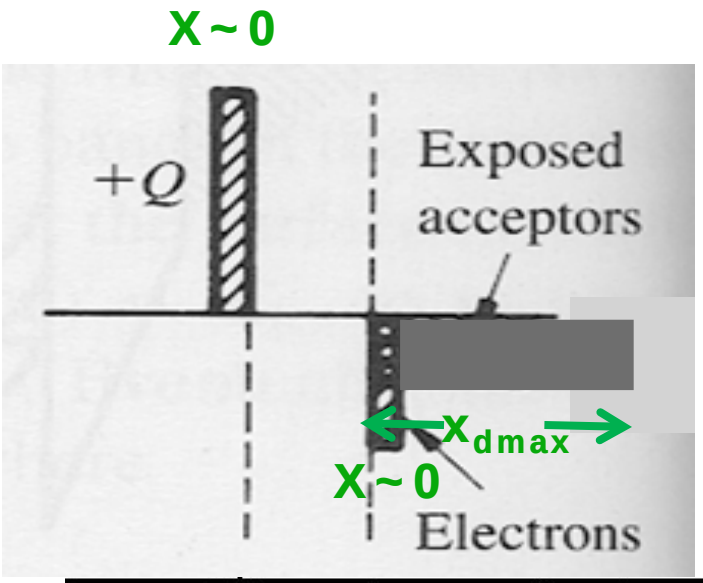
$V_{FB}<V_{GB}<V_m$



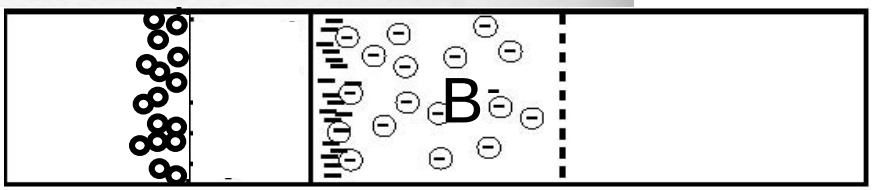
depletion



Review: Voltage drops and charges



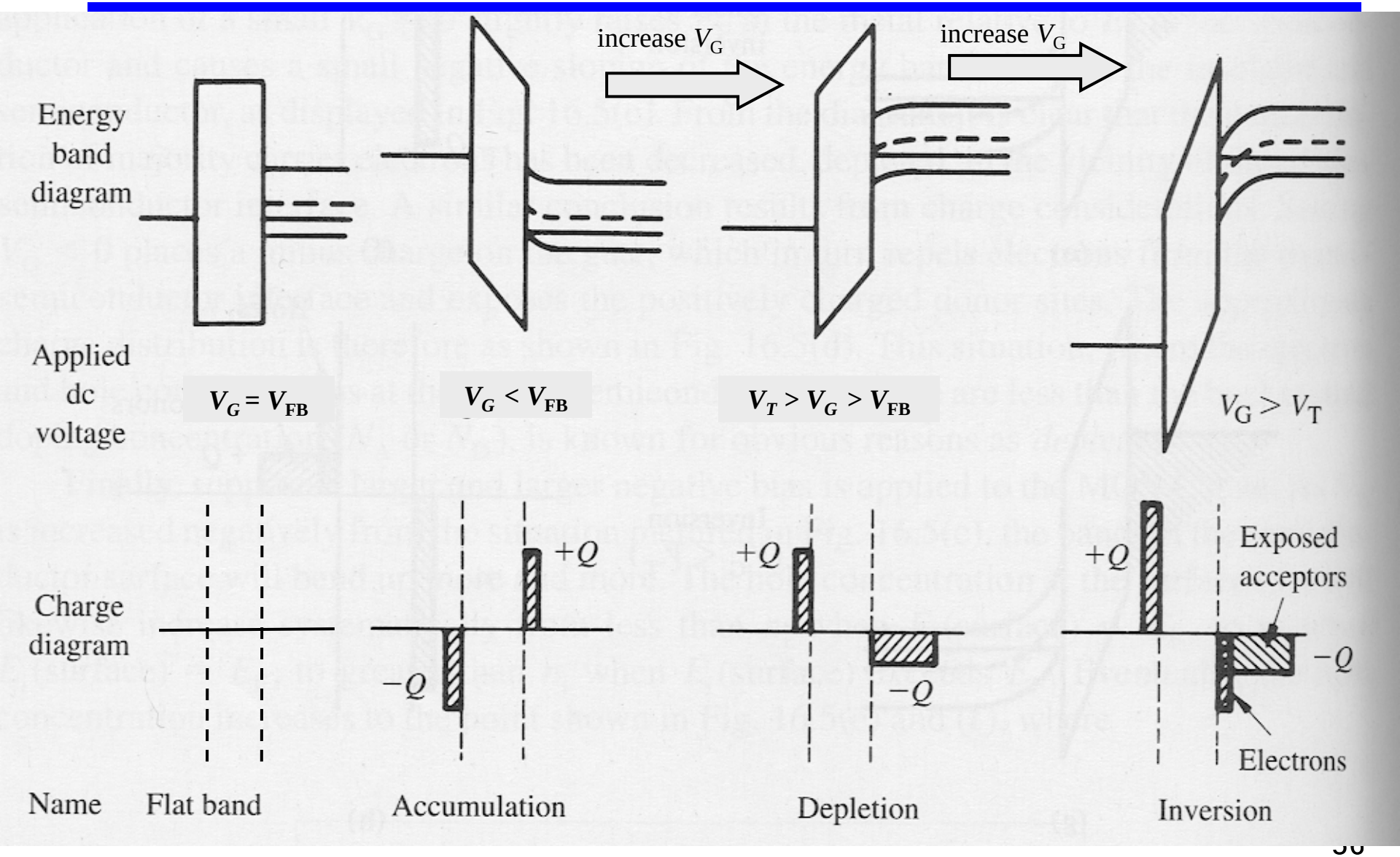
$V_{GB} \geq V_T$



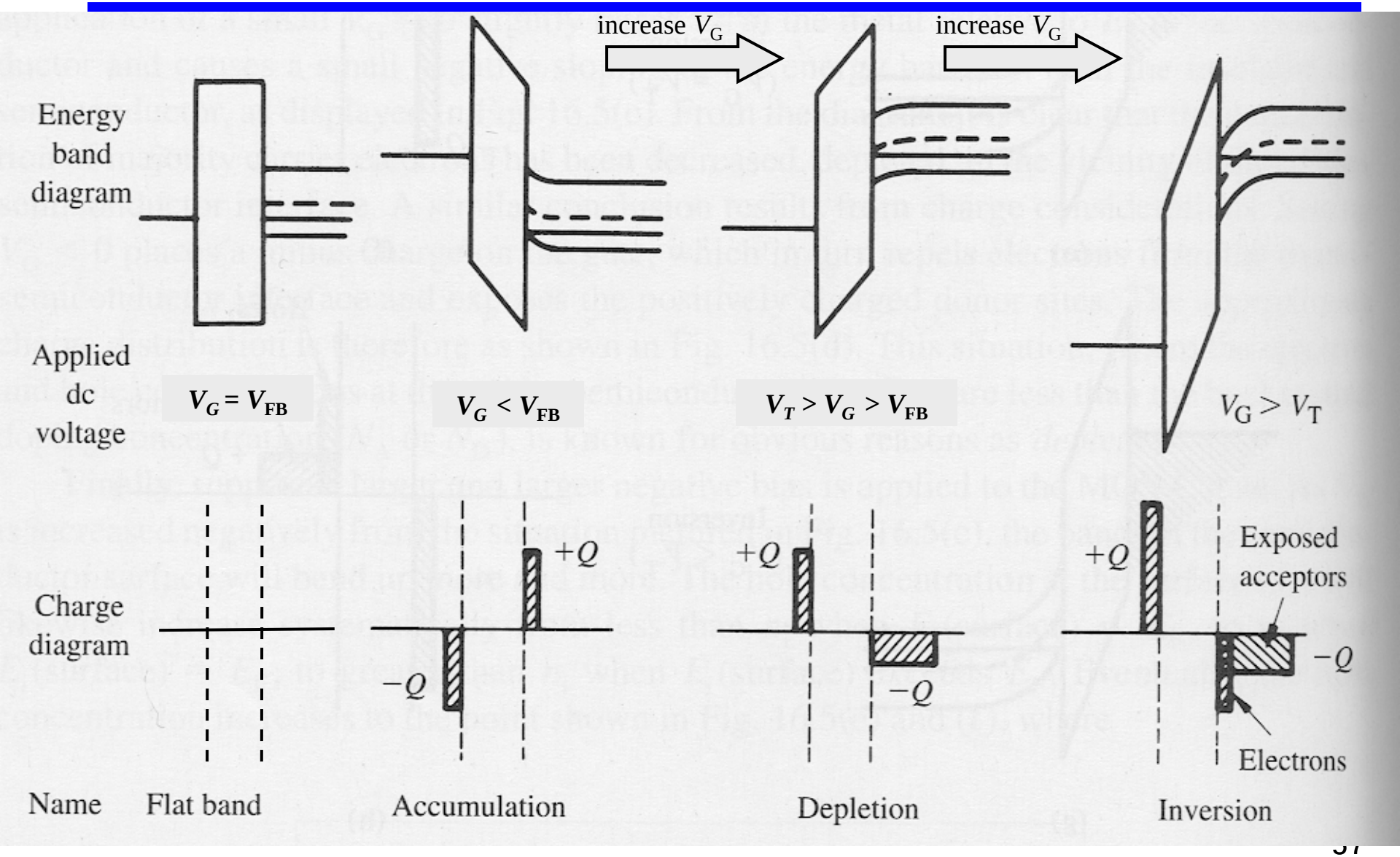
inversion

electron inversion layer

Review: Biasing Conditions for p-type Si

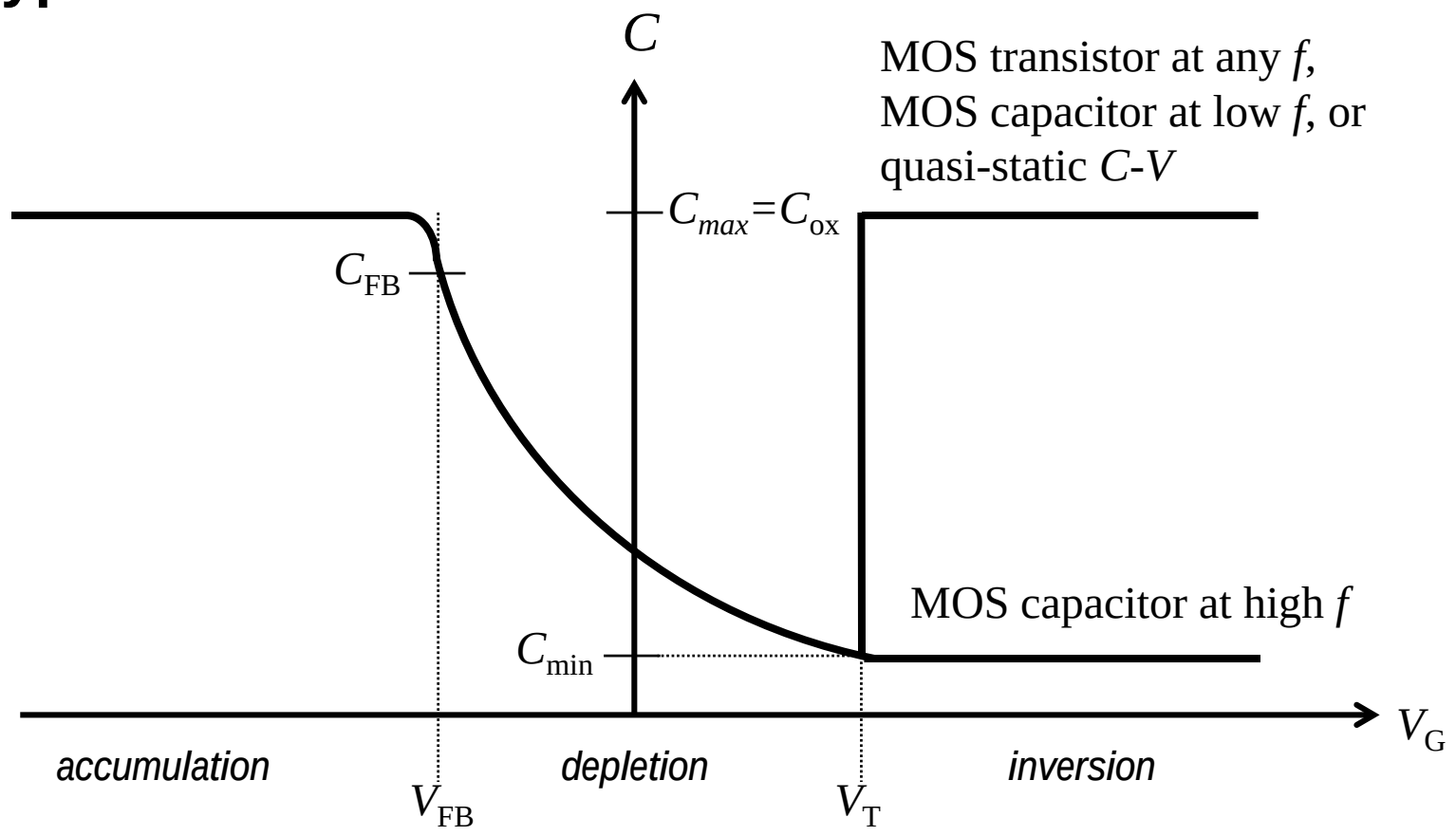


Review: Biasing Conditions for p-type Si



Capacitor *vs.* Transistor *C-V* (or LF *vs.* HF *C-V*)

p-type Si:



MOS Capacitor – MS contact

OUTLINE

- Metal-semiconductor contacts
- **MOS structure**
- MOS energy band diagram
- Effects of applied biases
- Non-Ideal MOS Capacitors

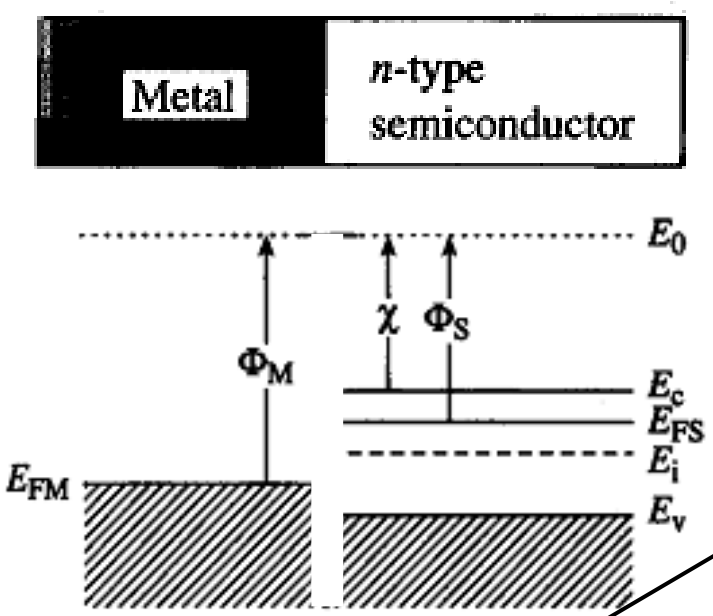
MOS Capacitor – MS contact

OUTLINE

- Physical Structure of MOS Capacitor
- Energy Band Diagram of MOS Structure
- Effects of Applied Voltage Biases
  - **operation modes** & **capacitance**
- **Appendix: Metal-semiconductor contact**

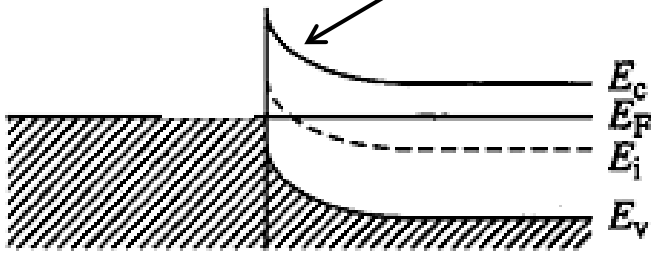
Ideal MS Contact: $\Phi_M > \Phi_S$, n-type

Band diagram instantly after contact formation:



Electron depletion

Equilibrium band diagram:

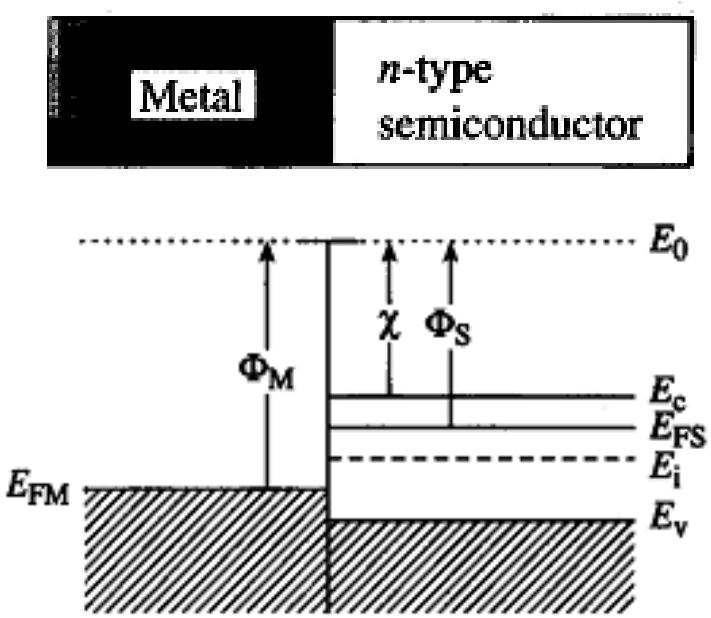


Schottky Barrier **:**

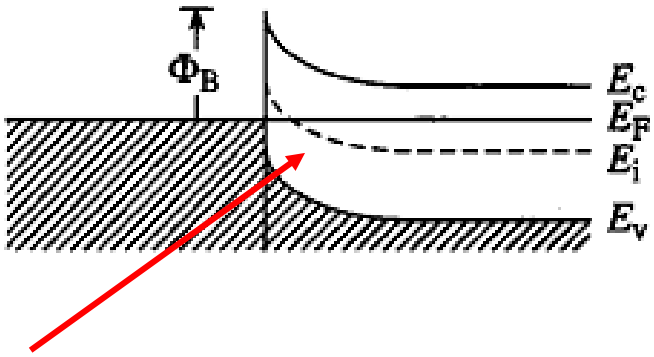
$$\Phi_{Bn} = \Phi_M - \chi$$

Ideal MS Contact: $\Phi_M > \Phi_S$, n-type

Band diagram instantly after contact formation:



Equilibrium band diagram:

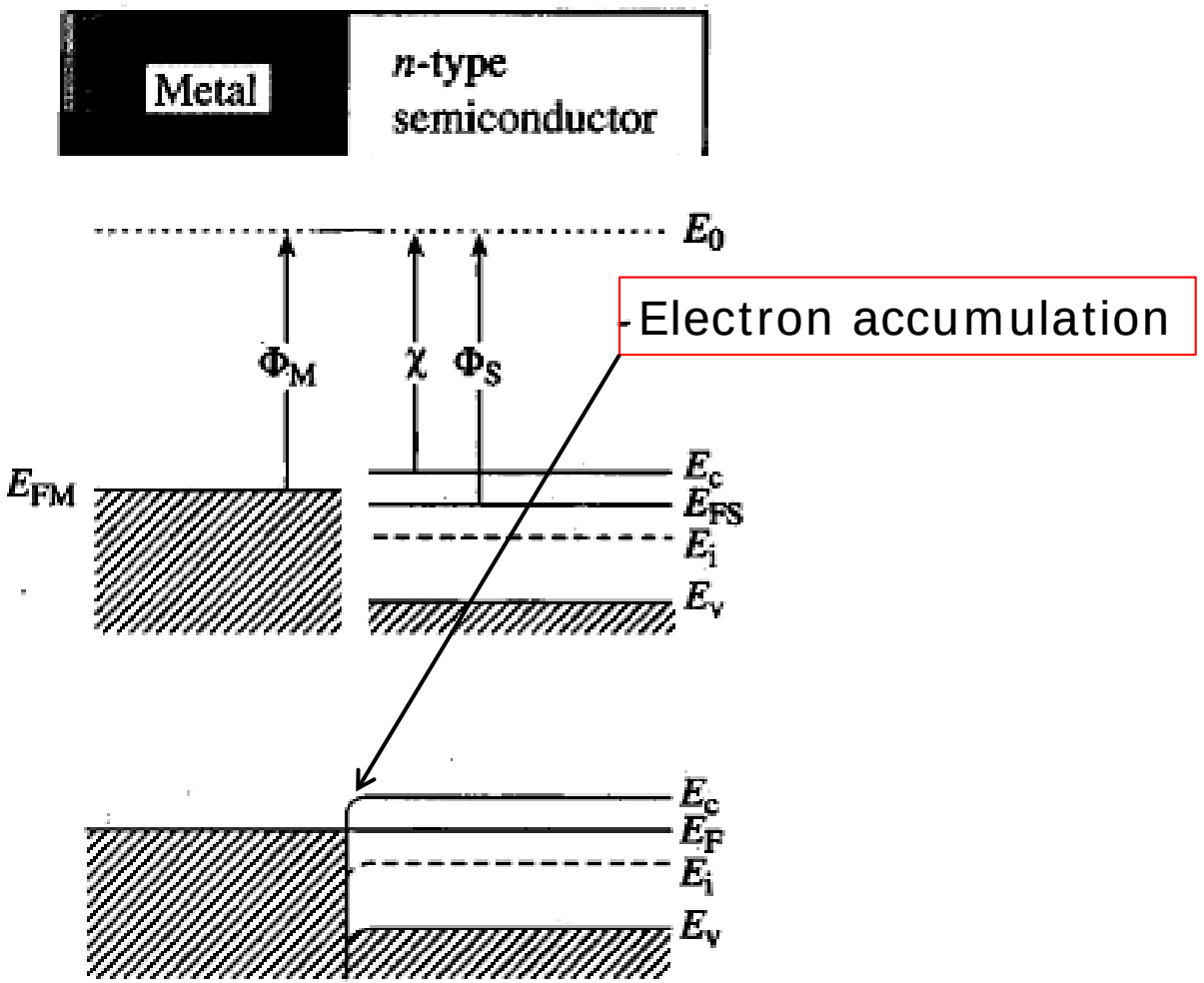


Schottky Barrier **:**

$$\Phi_{Bn} = \Phi_M - \chi$$

Ideal MS Contact: $\Phi_M < \Phi_S$, n-type

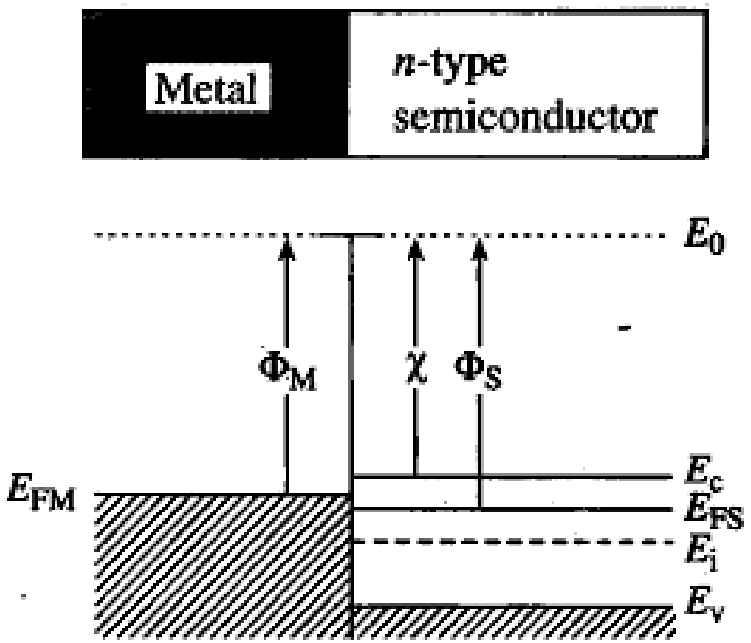
Band diagram instantly after contact formation:



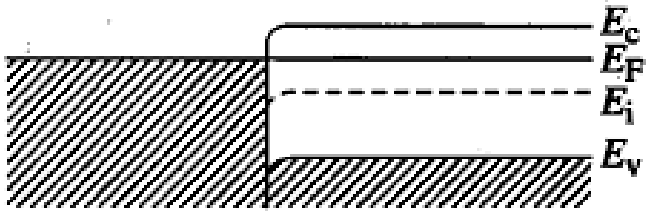
Equilibrium band diagram:

Ideal MS Contact: $\Phi_M < \Phi_S$, n-type

Band diagram instantly after contact formation:



Equilibrium band diagram:



Heavy doping is needed to form ohmic contact.

Metal-Semiconductor Contacts

There are 2 kinds of metal-semiconductor contacts:

- rectifying
  "Schottky diode"

- non-rectifying
  "ohmic contact"

Metal-Semiconductor Contacts

There are 2 kinds of metal-semiconductor contacts:

- rectifying
  "Schottky diode"

Polarity dependence

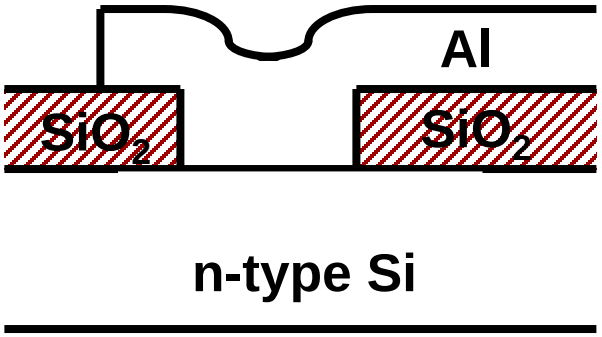
- non-rectifying
  "ohmic contact"

Polarity independence

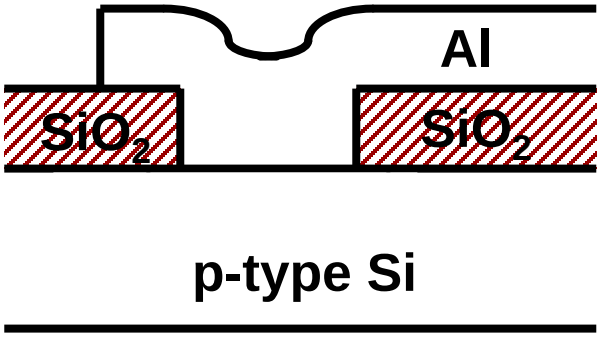
Electrical Contacts to Si

- In order to achieve a low-resistance (“ohmic”) contact between metal and silicon, the silicon must be heavily doped:

Metal contact to n-type Si



Metal contact to p-type Si



→ **To contact the body of a MOSFET, locally heavy doping is used.**

Forming Body Contacts

Open holes in oxide layer for body contacts after doping these regions