Xi'an Jiaotong-Liverpool University
西交利物浦大學

EEE109: Electronic Circuits

The Field Effect Transistor

Contents

- Study and understand the operation and characteristics of the various types of MOSFETs.
- Understand and become familiar with the dc analysis and design techniques of MOSFET circuits.
- Examine three applications of MOSFET circuits.
- Investigate current source biasing of MOSFET circuits, such as those used in integrated circuits.
- Analyze the dc biasing of multistage or multitransistor circuits.
- Understand the operation and characteristics of the junction field-effect transistor, and analyze the dc response of JFET circuits.

General Overview

MOSFET

- Metal-Oxide-Semiconductor Field Effect Transistor - MOSFET

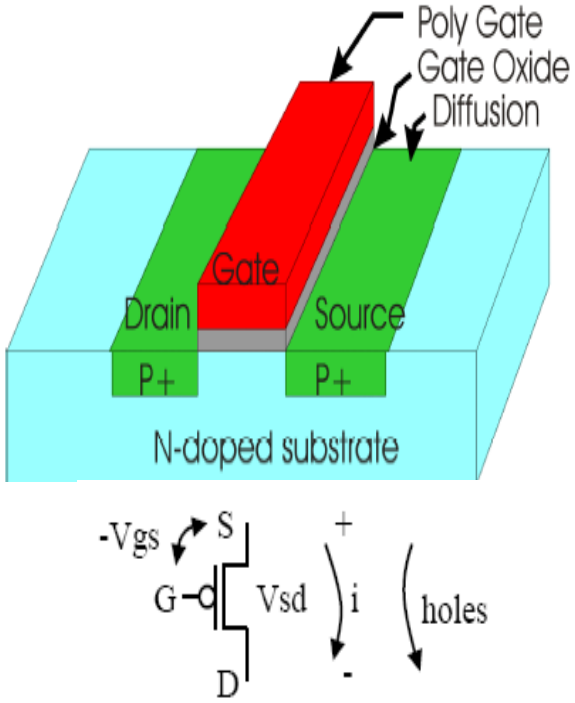
- **Current** is controlled by an electric field applied perpendicular to both semiconductor surface and to the direction of current.

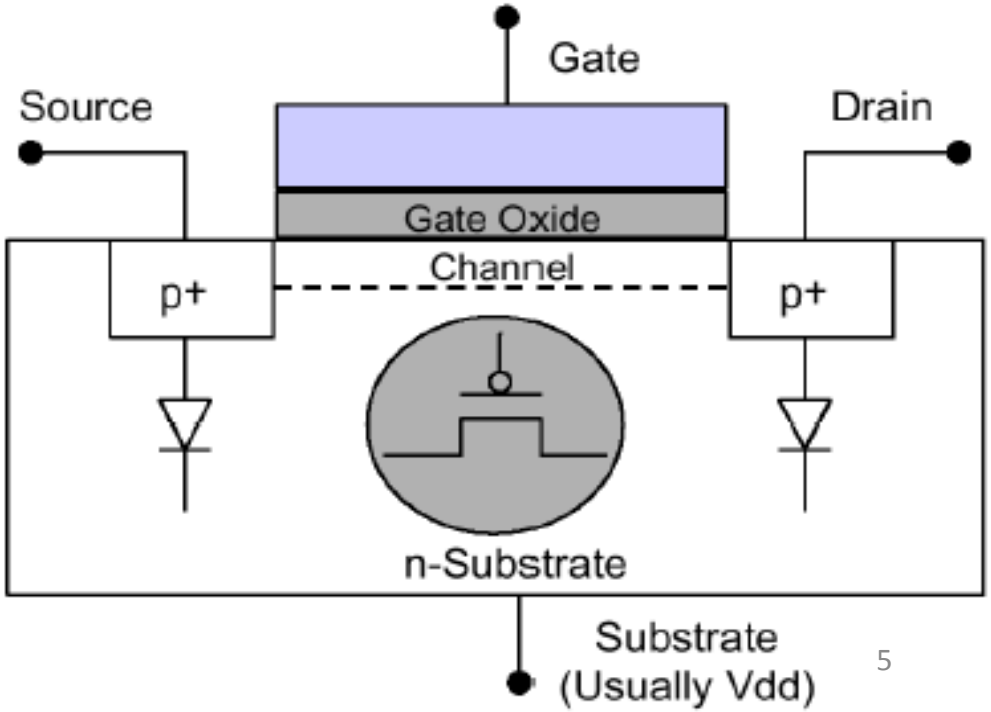
- **Field effect** – Phenomenon to control the current in the semiconductor by applying an electric field perpendicular to the surface.

- **The basic transistor principle**: ***The voltage between two terminals controls the current through the third terminal.***

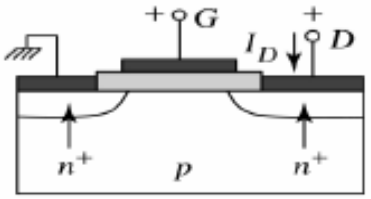
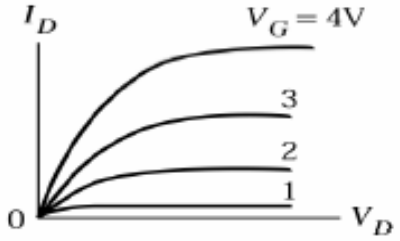
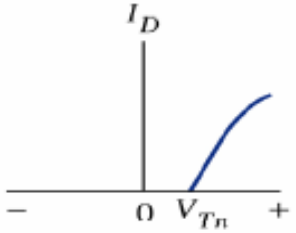
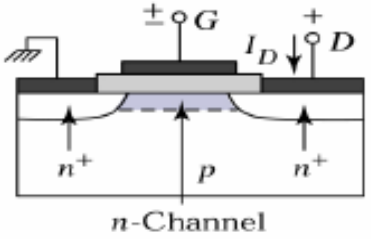
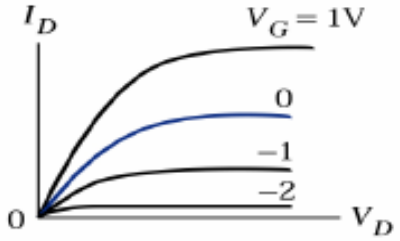
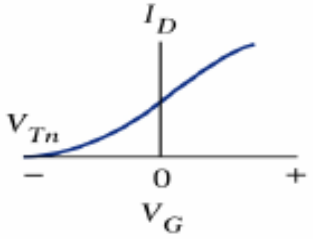
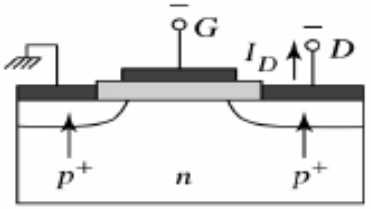
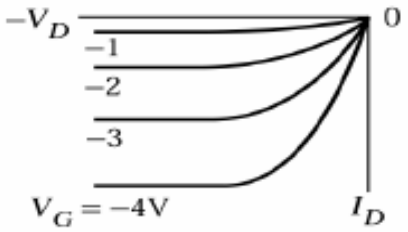
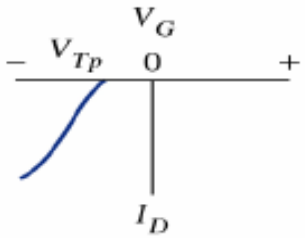
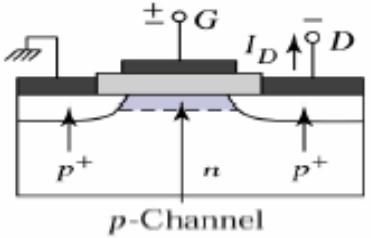
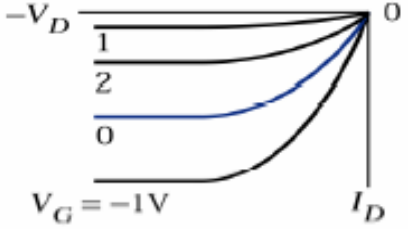
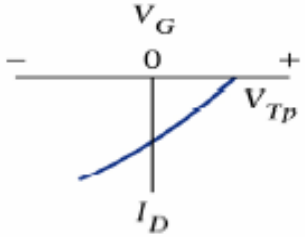
Types of Field-Effect Transistors

- MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor)
- Depletion and enhancement mode (Primary component in high-density VLSI chips such as memory chips and microprocessors)
- JFET (Junction Field-Effect Transistor) finds application especially in analog and RF circuit design
- MESFET (a MOSFET with no oxide)
- All device and circuit analysis are the same!

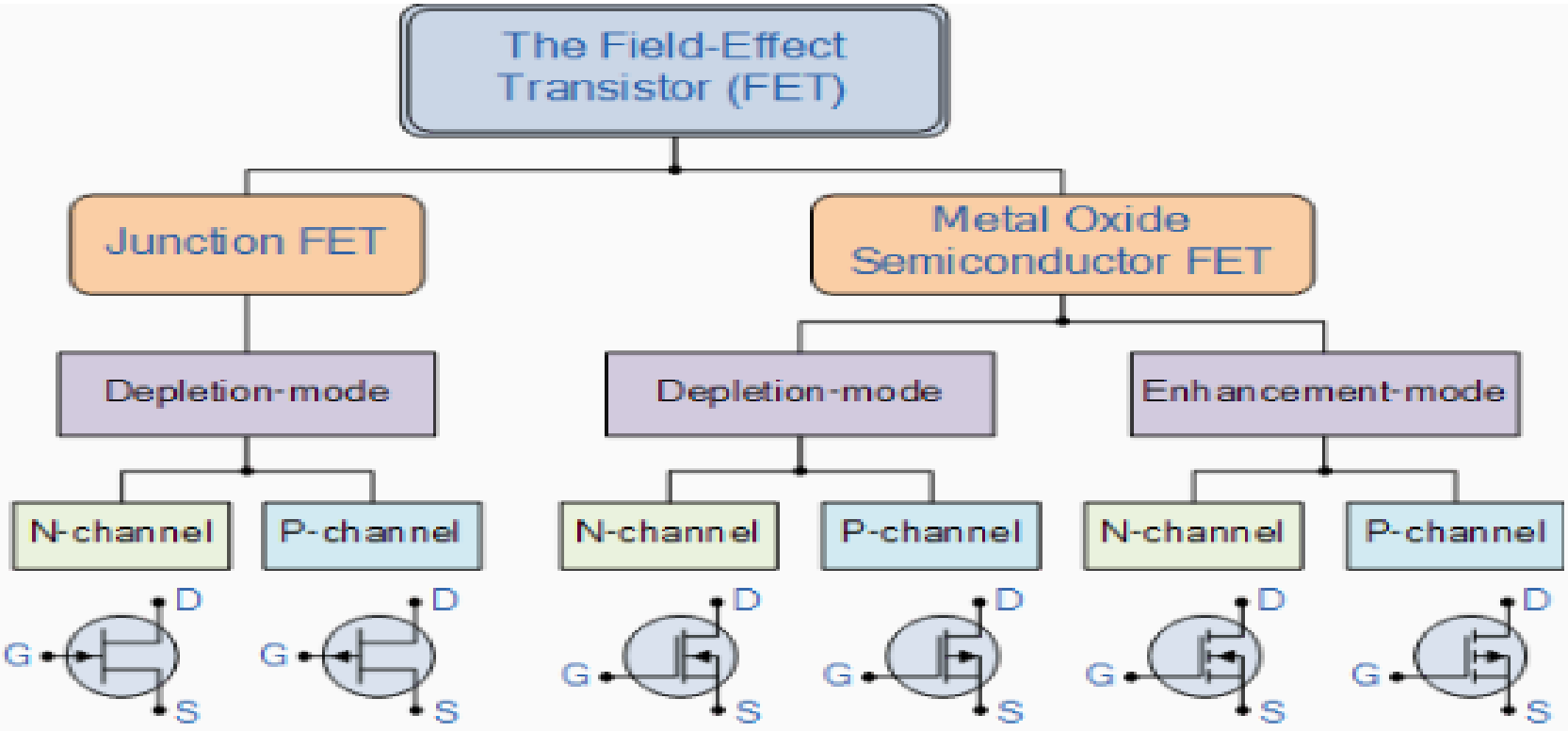




Types of MOSFETs

Type	Cross Section	Output Characteristics	Transfer Characteristics
n-Channel Enhancement (Normally Off)			
n-Channel Depletion (Normally On)			
p-Channel Enhancement (Normally Off)			
p-Channel Depletion (Normally On)			

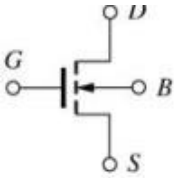
Field Effect Transistor Tree



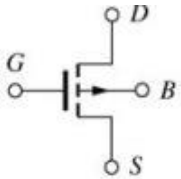
Biasing of the Gate for both the junction field effect transistor, (JFET) and the metal oxide semiconductor field effect transistor, (MOSFET) configurations are given as:

Type	Junction FET		Metal Oxide Semiconductor FET			
	Depletion Mode		Depletion Mode		Enhancement Mode	
Bias	ON	OFF	ON	OFF	ON	OFF
N-channel	0v	-ve	0v	-ve	+ve	0v
P-channel	0v	+ve	0v	+ve	-ve	0v

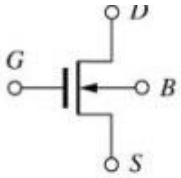
MOSFET Circuit Symbols



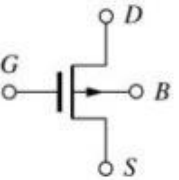
(a) NMOS enhancement-mode device



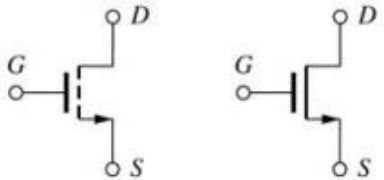
(b) PMOS enhancement-mode device



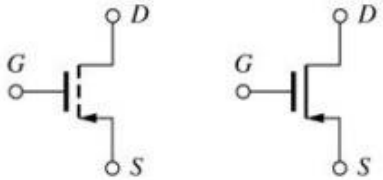
(c) NMOS depletion-mode device



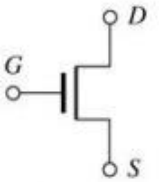
(d) PMOS depletion-mode device



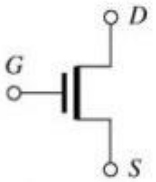
(e) Three-terminal NMOS transistors



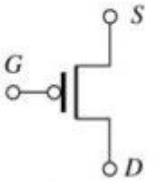
(f) Three-terminal PMOS transistors



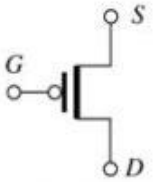
(g) Shorthand notation—NMOS enhancement-mode device



(h) Shorthand notation—NMOS depletion-mode device



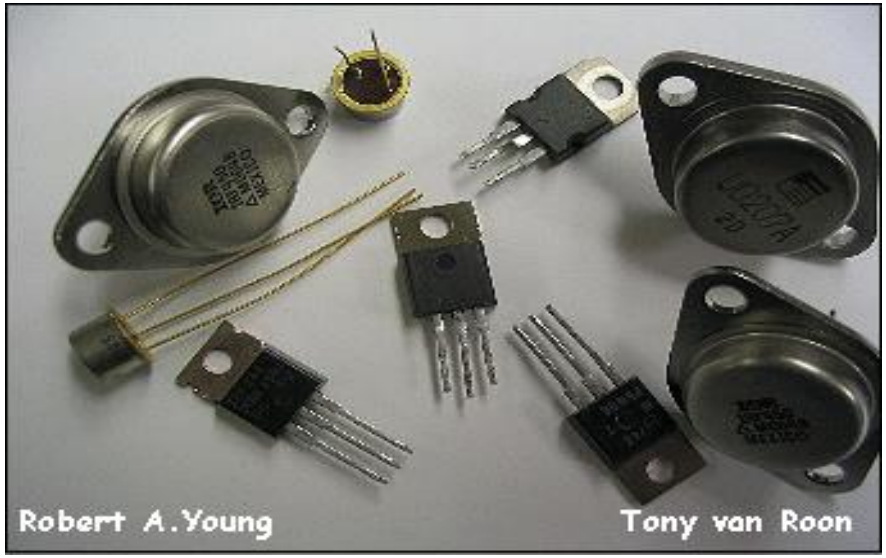
(i) Shorthand notation—PMOS enhancement-mode device

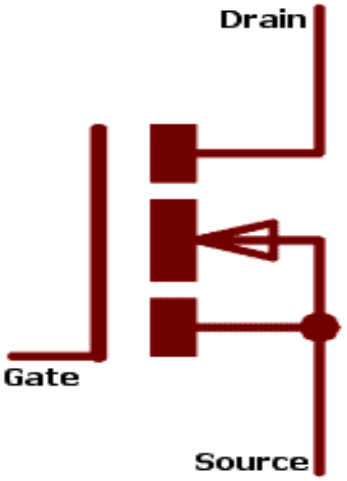


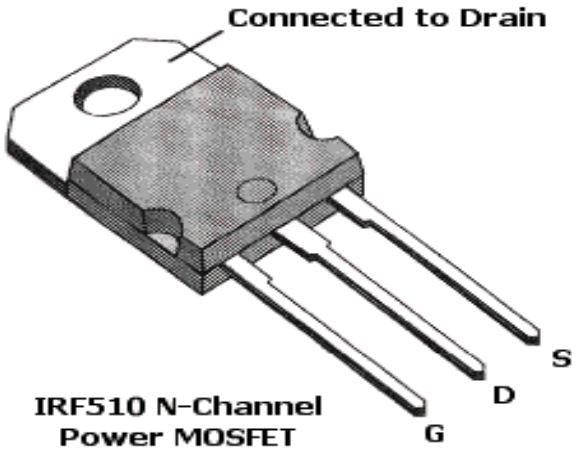
(j) Shorthand notation—PMOS depletion-mode device

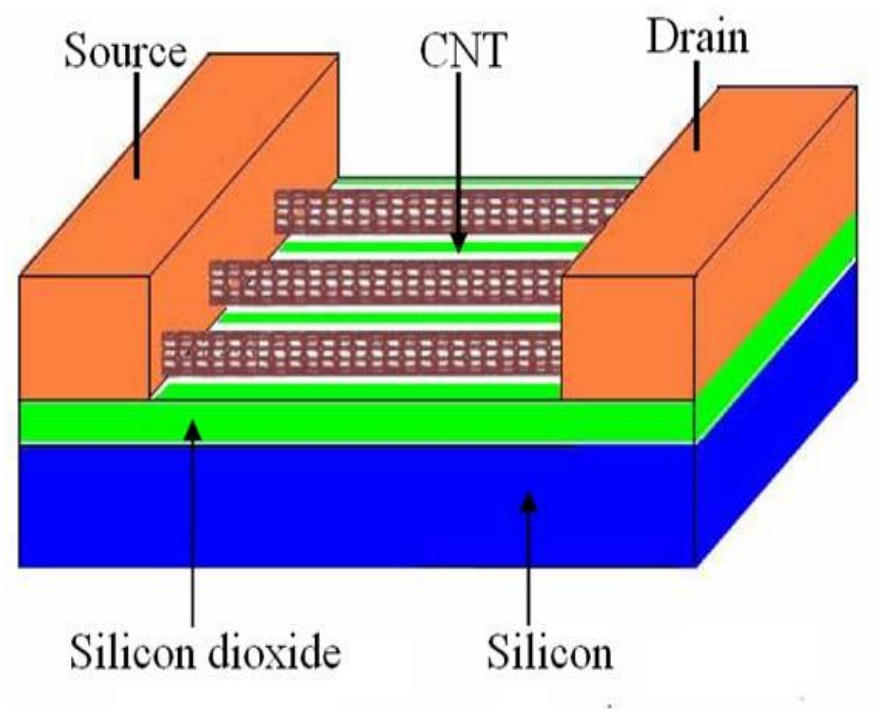
- (g) and(i) are the most commonly used symbols in VLSI logic design.
- MOS devices are symmetric.
- In NMOS, n^+ region at higher voltage is the drain.
- In PMOS p^+ region at lower voltage is the drain

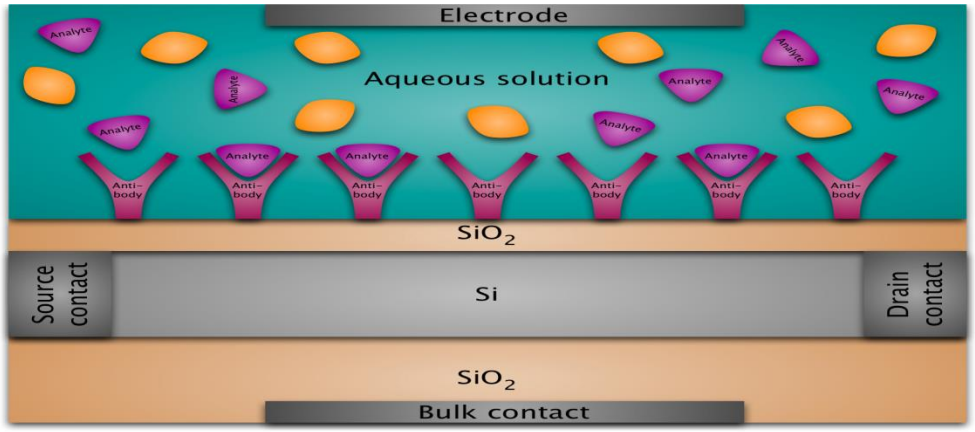
FETs

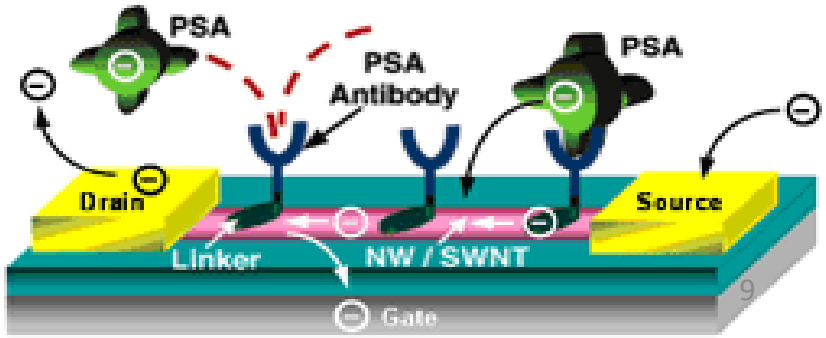

Robert A.Young
Tony van Roon


Drain
Gate
Source


Connected to Drain
S
D
G
IRF510 N-Channel
Power MOSFET


Source
CNT
Drain
Silicon dioxide
Silicon


Electrode
Aqueous solution
Analyte
Anti-body
SiO2
Source contact
Si
Drain contact
SiO2
Bulk contact


PSA
PSA Antibody
PSA
Drain
Source
Linker
NW / SWNT
Gate

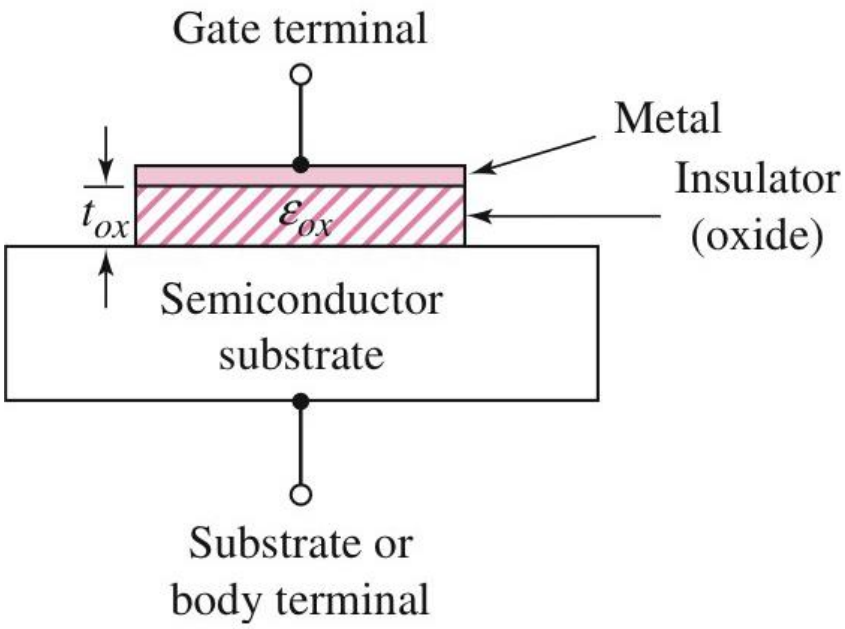
Two-Terminal MOS Structure

Basic Structure of MOS Capacitor

First electrode-Gate : Consists of low-resistivity material such as polycrystalline silicon

Second electrode- Substrate or Body: *n*- or *p*-type semiconductor

Dielectric-Silicon dioxide: stable high-quality electrical insulator between gate and substrate.

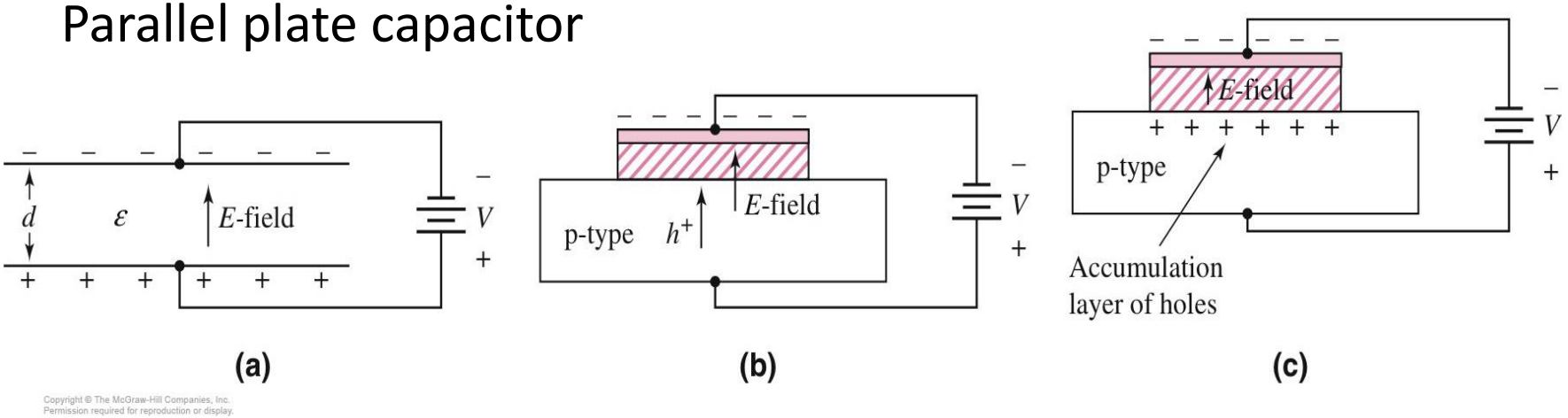


Copyright © The McGraw-Hill Companies, Inc.
Permission required for reproduction or display.

Heart of MOSFET!

MOS Capacitor Under Bias: Electric Field and Charge

Parallel plate capacitor



$C = \varepsilon A/d$

ε – permittivity

A – area of one plate

d – distance between plates

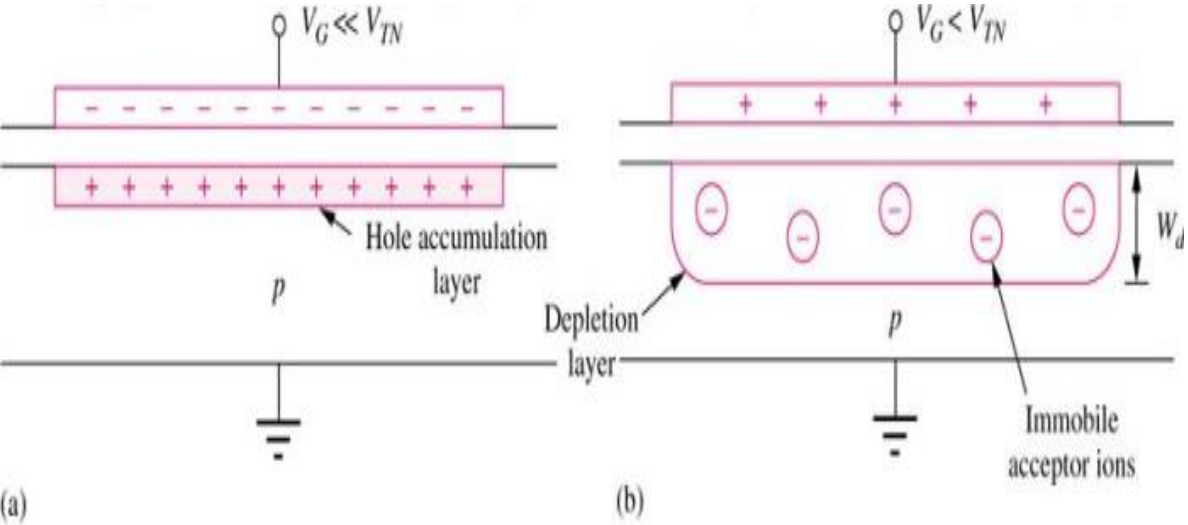
Negative gate bias:

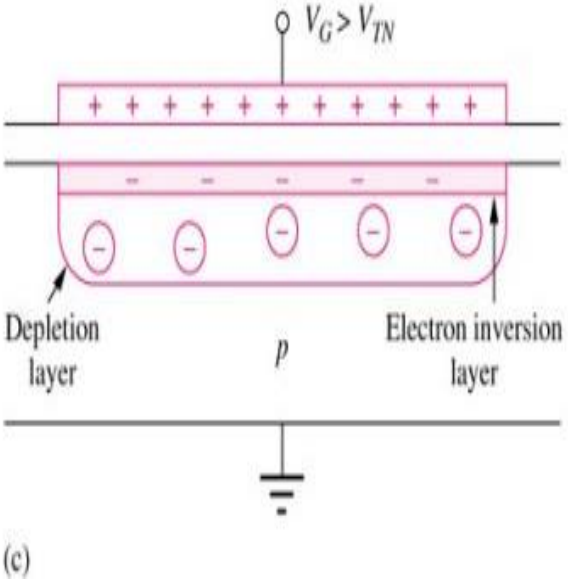
Holes attracted to gate

Positive gate bias:

Electrons attracted to gate

Substrate Conditions for Different Biases





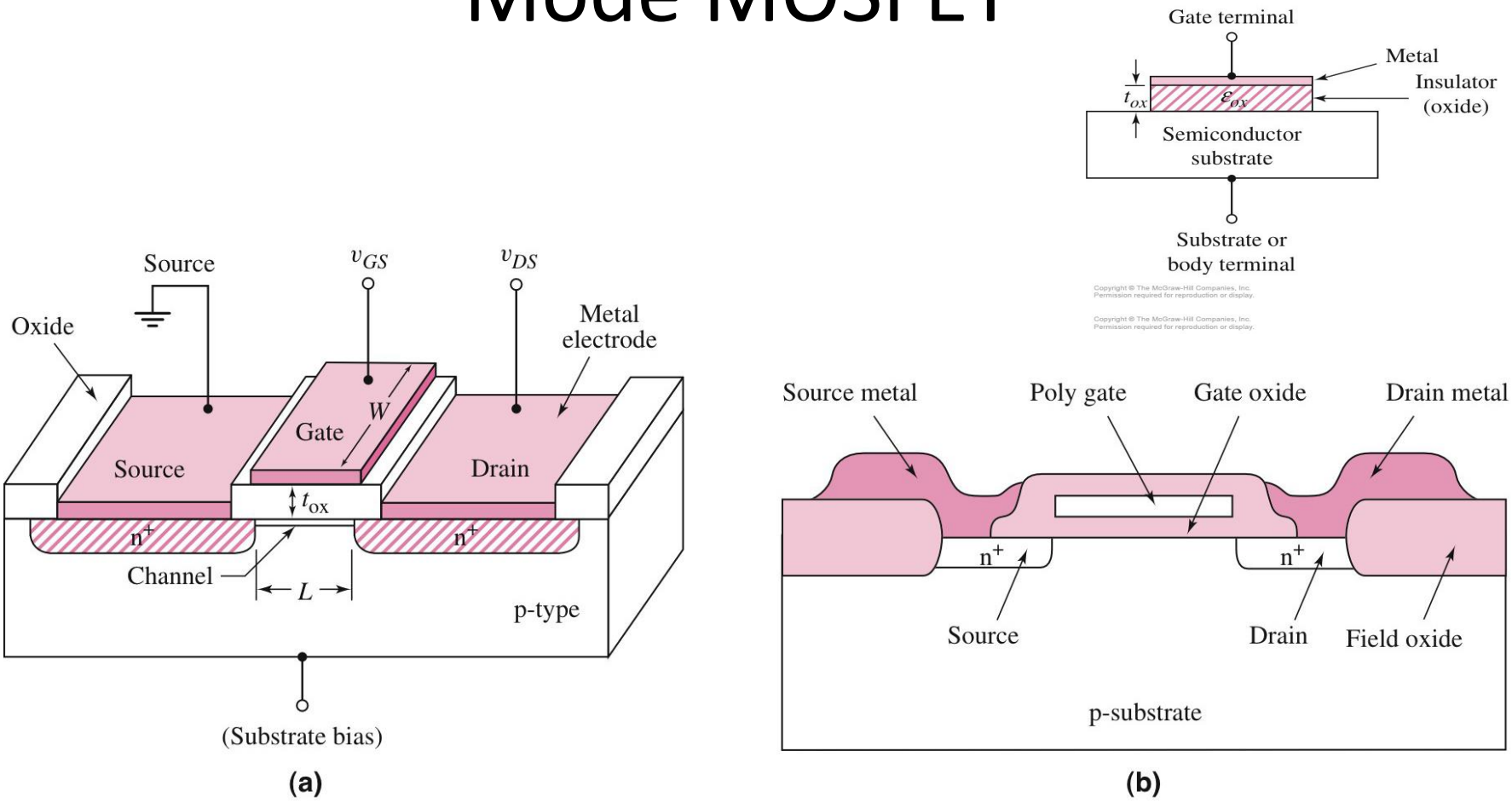
- Region of minority carrier electron inversion layer attracted to the oxide semiconductor surface!

n-Channel Enhancement-Mode MOSFET

Enhancement mode & n-Channel

- Enhancement-mode -> a voltage must be applied to the gate to create an inversion layer
- n-type substrate -> positive gate voltage
- p-type substrate -> negative gate voltage

Schematic of n-Channel Enhancement Mode MOSFET



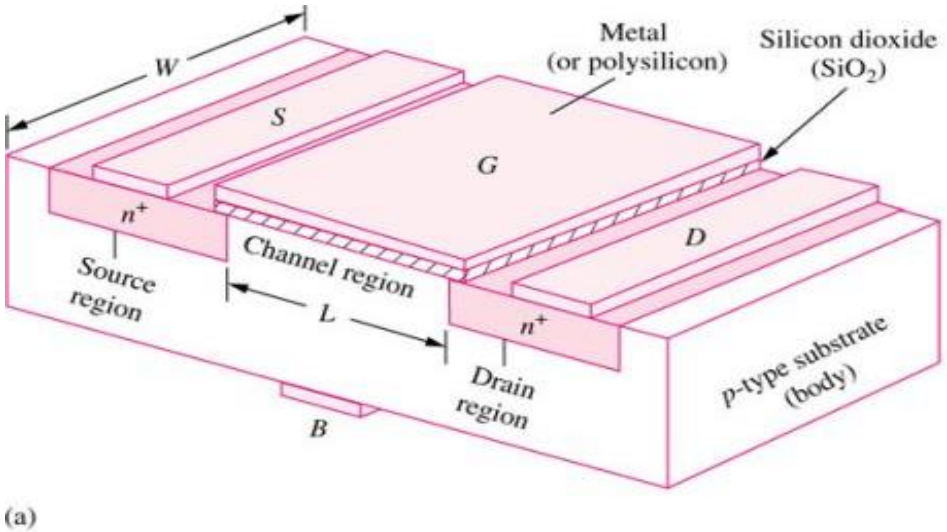
t_{ox} is typically on the order of 400 angstroms.

International System of Units

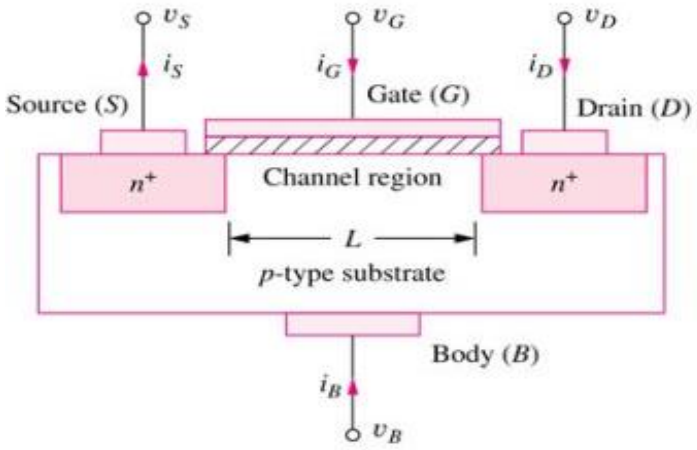
Standard prefixes for the SI units of measure

Multiples	**Name**		deca-	hecto-	kilo-	mega-	giga-	tera-	peta-	exa-	zetta-	yotta-
	Prefix		da	h	k	M	G	T	P	E	Z	Y
	Factor	10^0	10^1	10^2	10^3	10^6	10^9	10^{12}	10^{15}	10^{18}	10^{21}	10^{24}
Fractions	**Name**		deci-	centi-	milli-	micro-	nano-	pico-	femto-	atto-	zepto-	yocto-
	Prefix		d	c	m	μ	n	p	f	a	z	y
	Factor	10^0	10^{-1}	10^{-2}	10^{-3}	10^{-6}	10^{-9}	10^{-12}	10^{-15}	10^{-18}	10^{-21}	10^{-24}

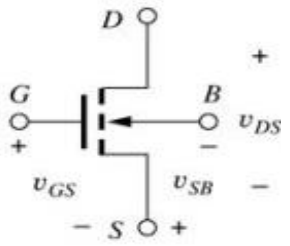
NMOS Transistor: Structure



(a)



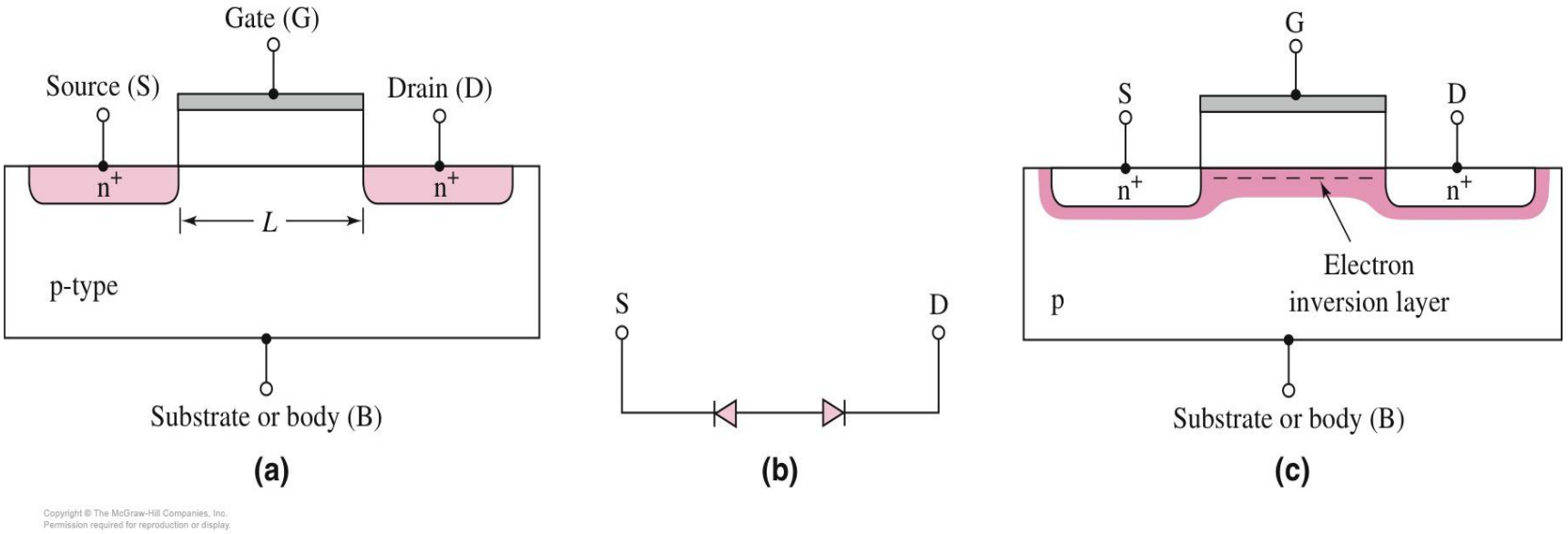
(b)



(c)

- 4 device terminals: Gate(G), Drain(D), Source(S) and Body(B).
- Source and drain regions form *pn* junctions with substrate.
- v_{SB}, v_{DS} and v_{GS} always positive during normal operation.
- v_{SB} always < v_{DS} and v_{GS} to reverse bias *pn* junctions

Basic Transistor Operation



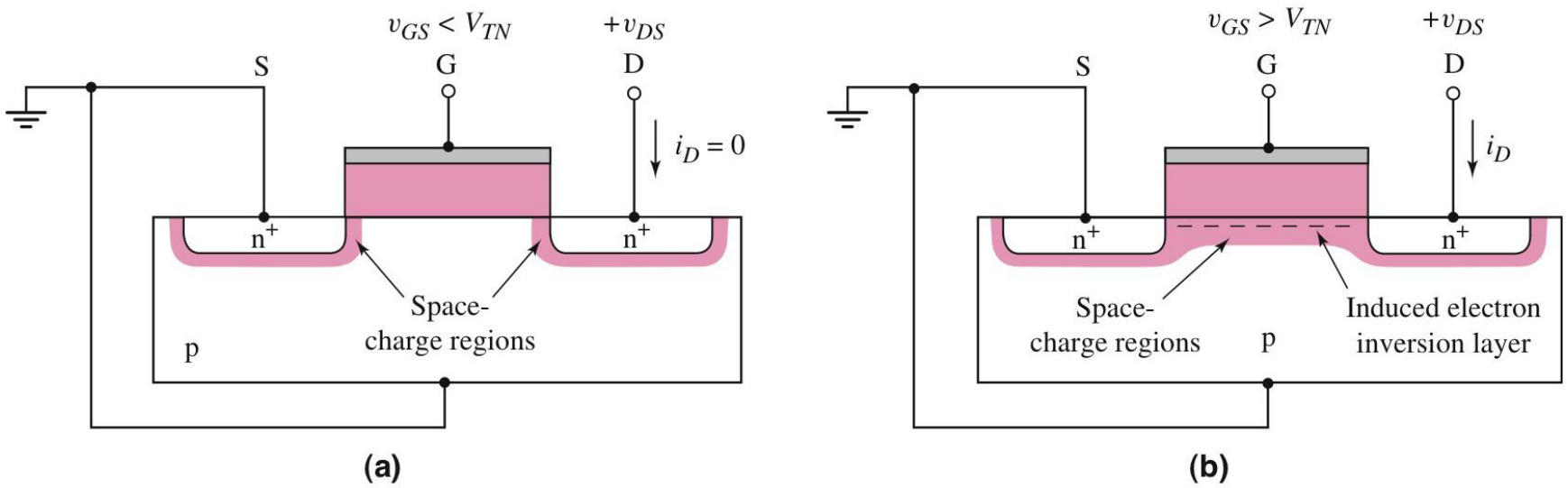
Before electron inversion layer is formed

After electron inversion layer is formed

The current in MOSFET is the result of the flow of charge in the inversion layer!

For NMOS, the carrier in the inversion layer is the electron!

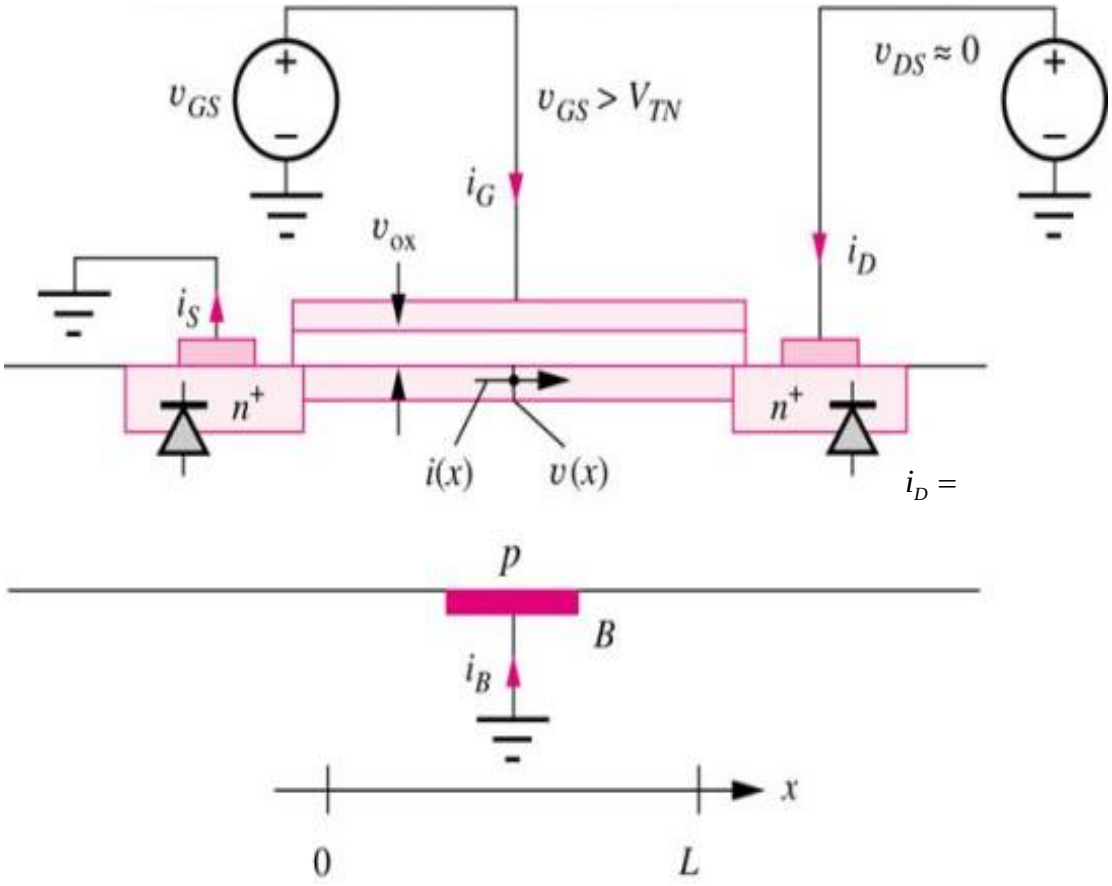
Basic Transistor Operation



Electrons flow from the source of the drain with an applied drain-to-source voltage!

The magnitude of current is a function of amount of charge in the inversion layer + a function of applied gate voltage.

NMOS Transistor: Triode Region Characteristics



for $v_{GS} - V_{TN} \geq v_{DS} \geq 0$

where, $K_n = K_n'W/L$

$K_n' = \mu_n C_{ox}''$ (A/V^2)

$C_{ox}'' = \varepsilon_{ox}/T_{ox}$

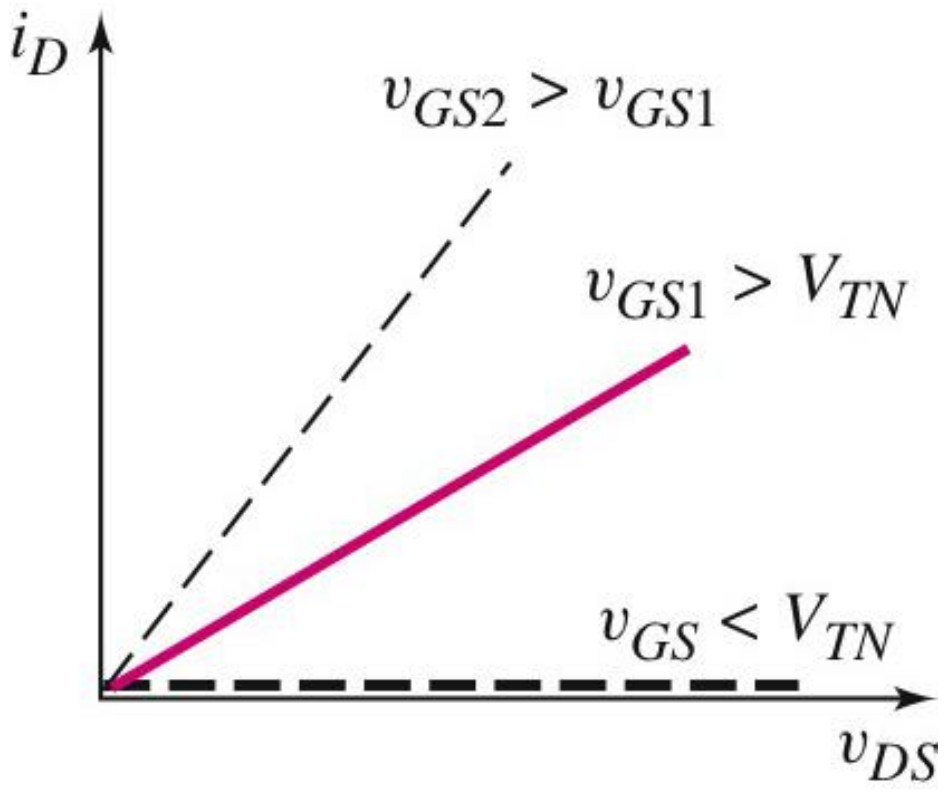
ε_{ox}=oxide permittivity

(F/cm)

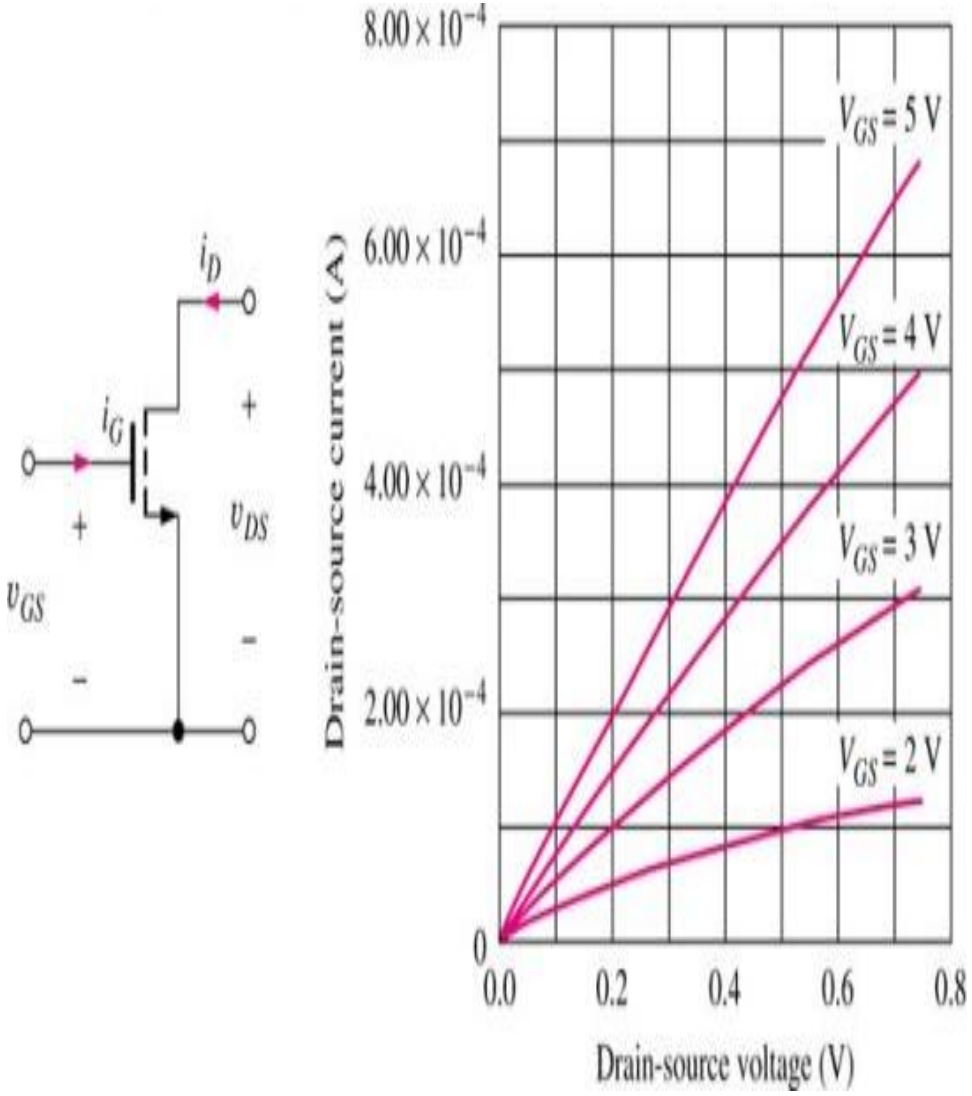
$T_{ox=}$oxide thickness (cm)

$$i_D = K_n \frac{W}{L}\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS}$$

Current Versus Voltage Characteristics: Enhancement-Mode nMOSFET



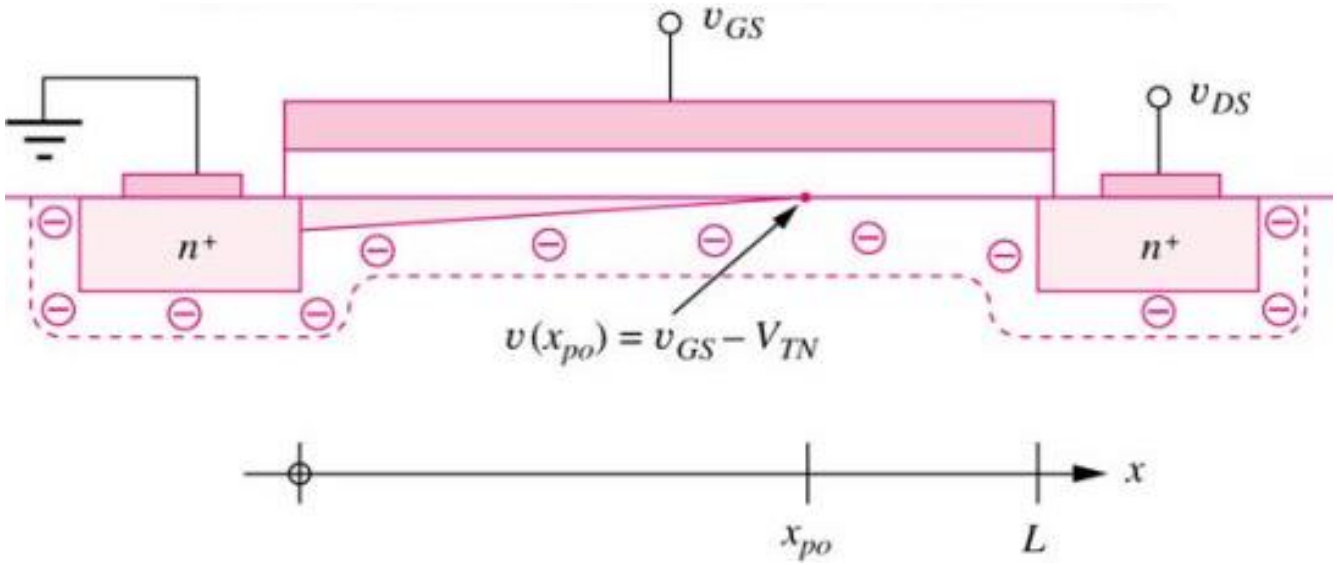
NMOS Transistor: Triode Region Characteristics (contd.)



- Output characteristics appear to be linear.
- FET behaves like a gate-source voltage-controlled resistor between source and drain with

$$R_{on} = \frac{1}{K_n' \frac{W}{L}\left(V_{GS} - V_{TN}\right)}$$

NMOS Transistor: Saturation Region (contd.)

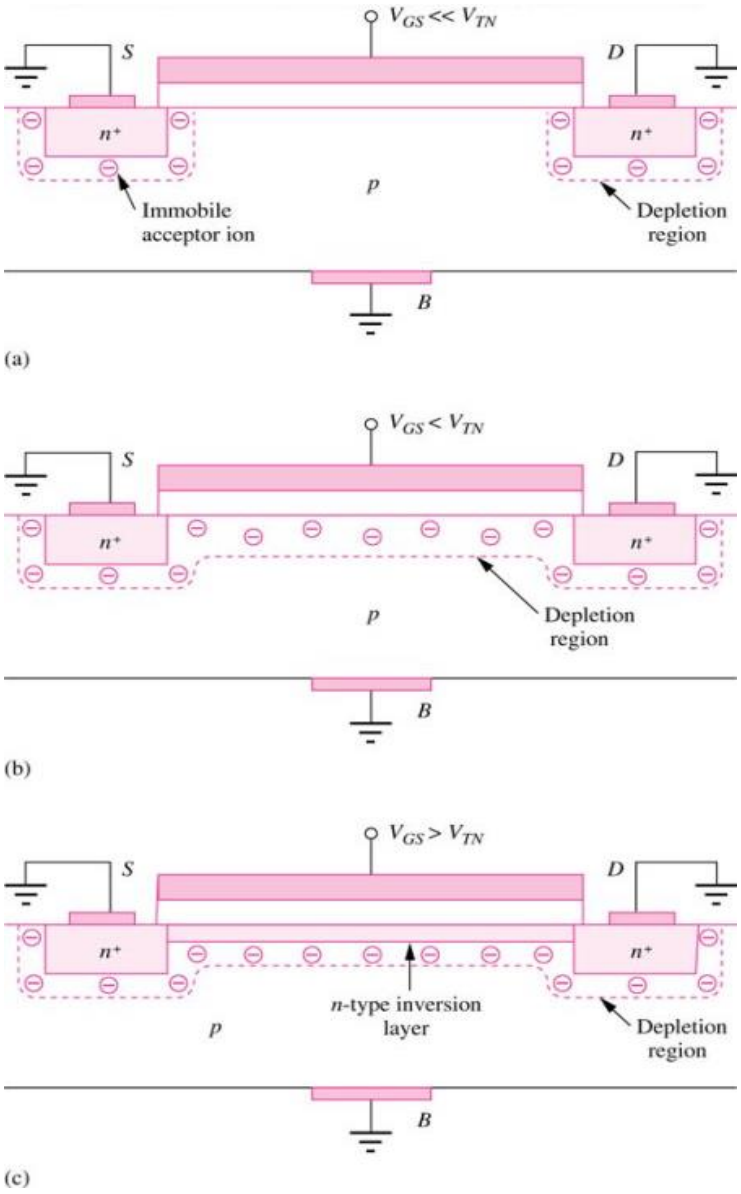


$$i_D = \frac{K_n}{2}\frac{W}{L}\left(v_{GS} - V_{TN}\right)^2 \quad \text{for} \quad v_{DS} \geq v_{GS} - V_{TN}$$

$$i_D \propto \left(v_{GS} - V_{TN}\right)^2 \text{ which quadratic function}$$

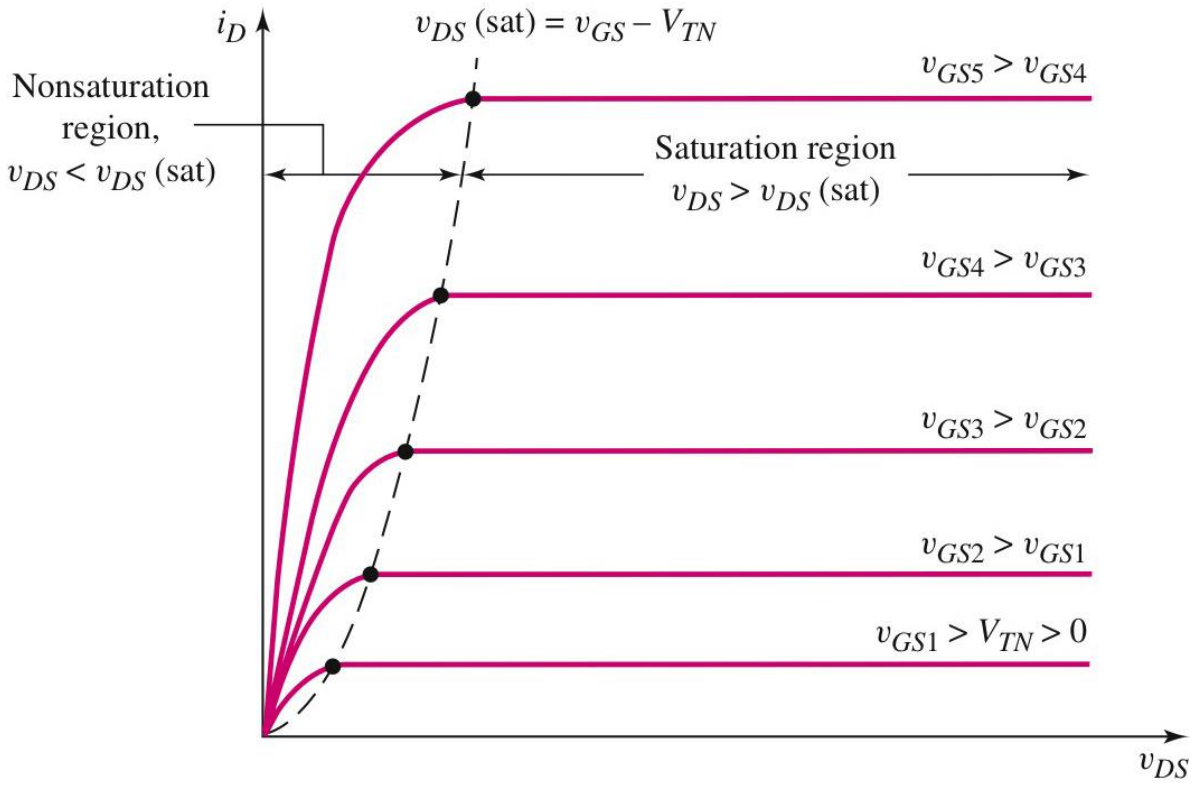
$v_{DSAT} = v_{GS} - V_{TN}$ is also called saturation or pinch-off voltage

NMOS Transistor: Qualitative I-V Behavior



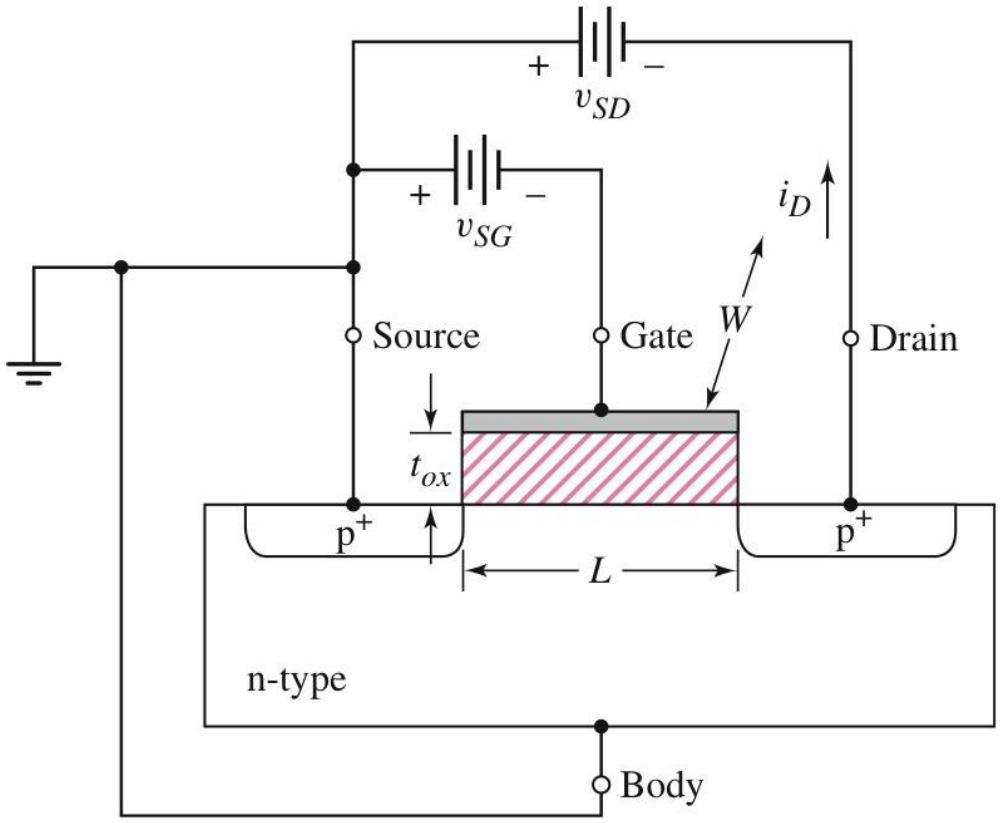
- $V_{GS}<<V_{TN}$: Only small leakage current flows.
- $V_{GS}<V_{TN}$: Depletion region formed under gate merges with source and drain depletion regions. No current flows between source and drain.
- $V_{GS}>V_{TN}$: Channel formed between source and drain. If $v_{DS}>0$,, finite i_D flows from drain to source.
- $i_B=0$ and $i_G=0$.

Family of i_D Versus v_{DS} Curves: Enhancement-Mode nMOSFET

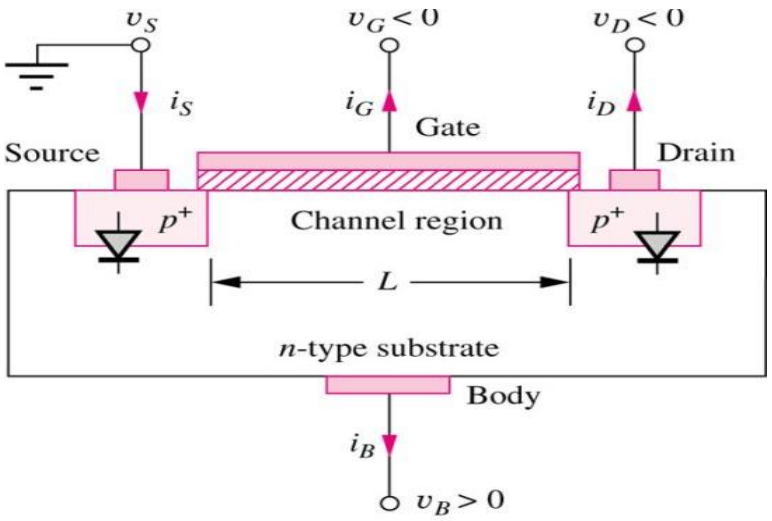


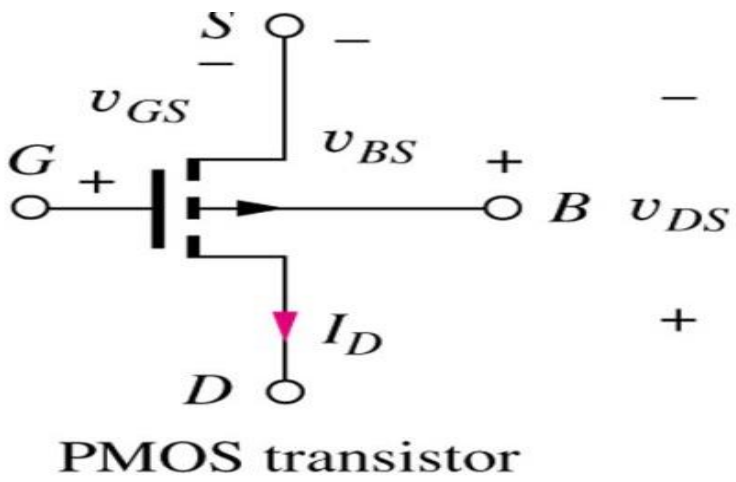
p-Channel Enhancement-Mode MOSFET

p-Channel Enhancement-Mode MOSFET



Enhancement-Mode PMOS Transistors: Structure

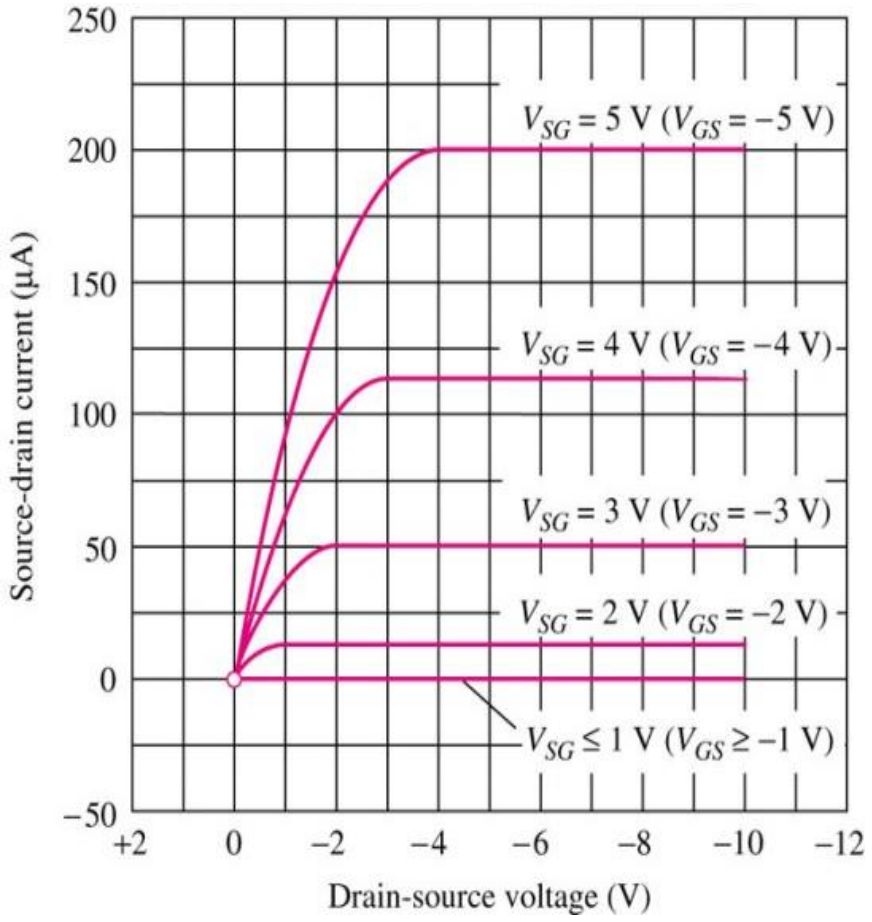




PMOS transistor

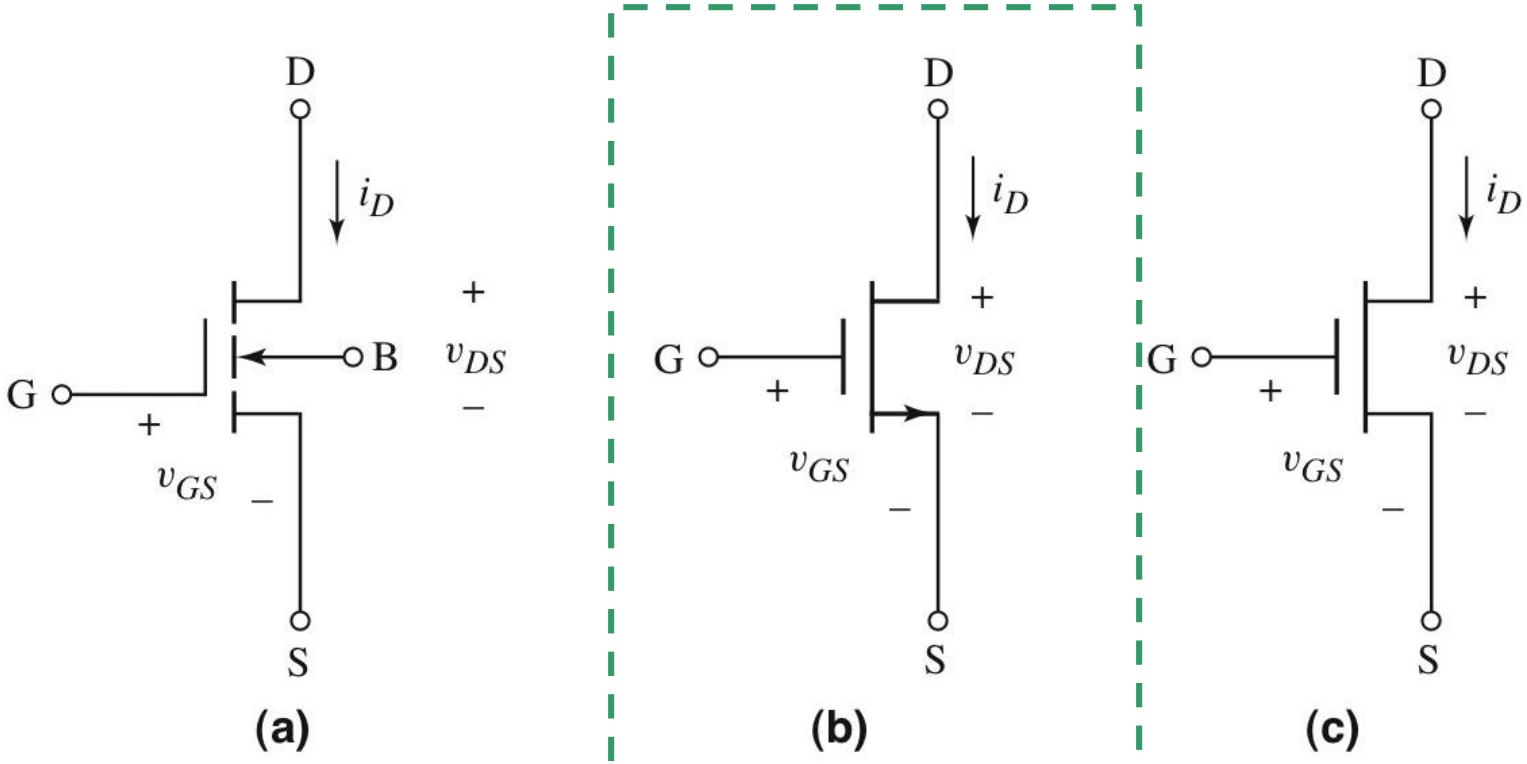
- *P*-type source and drain regions in *n*-type substrate.
- v_{GS}<0 required to create p-type inversion layer in channel region
- For current flow, $v_{GS<} v_{TP}$
- To maintain reverse bias on source-substrate and drain-substrate junctions, v_{SB} <0 and v_{DB} <0
- Positive bulk-source potential causes V_{TP} to become more negative

Enhancement-Mode PMOS Transistors: Output Characteristics

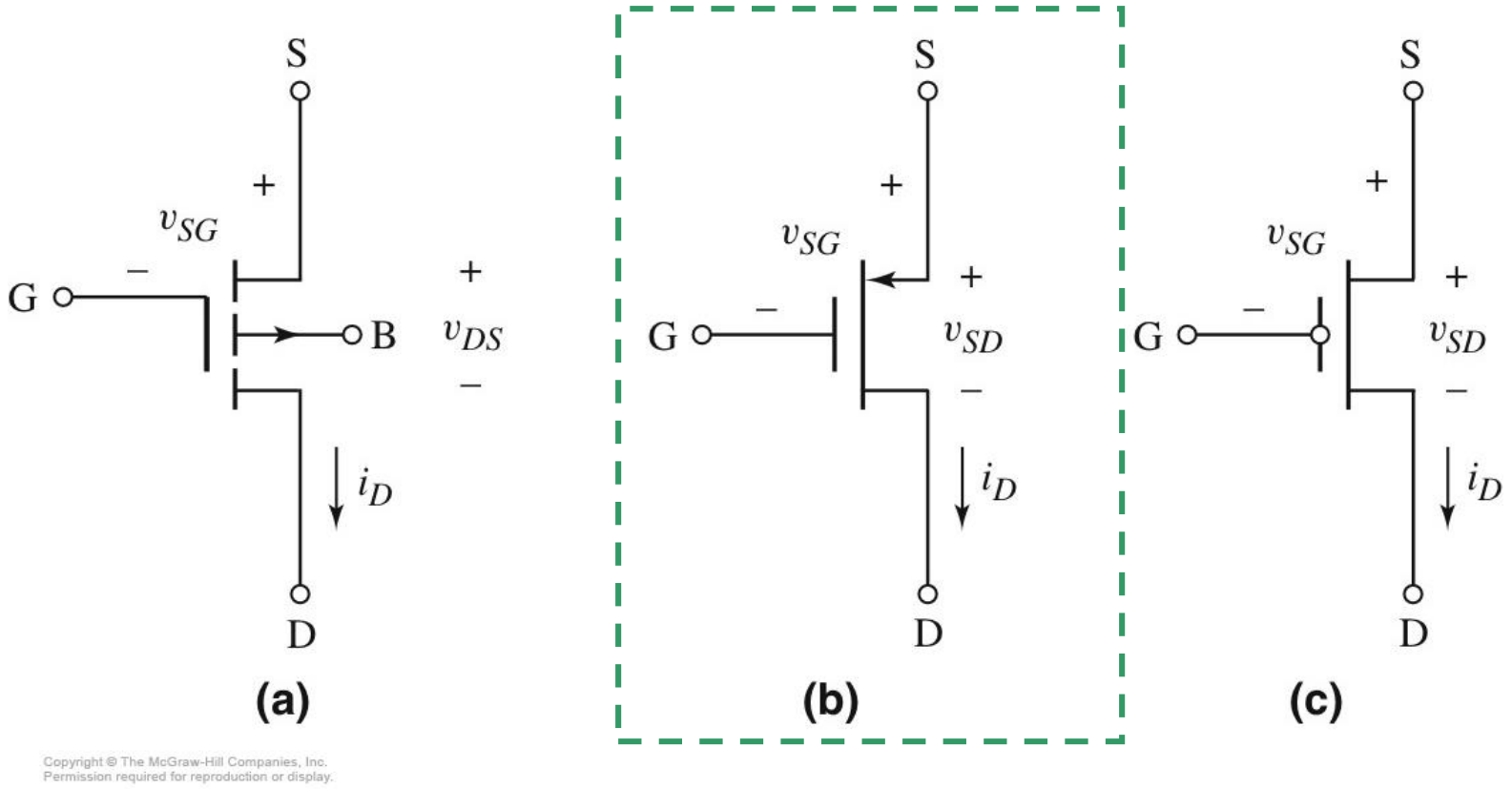


- For $V_{GS} \geq V_{TP}$, transistor is off.
- For more negative v_{GS}, drain current increases in magnitude
- PMOS is in triode region for small values of V_{DS} and in saturation for larger values.

Symbols for n-Channel Enhancement-Mode MOSFET

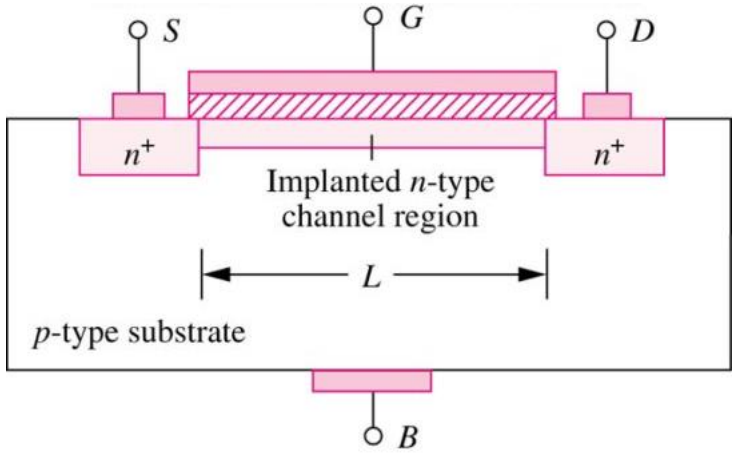


Symbols for p-Channel Enhancement-Mode MOSFET



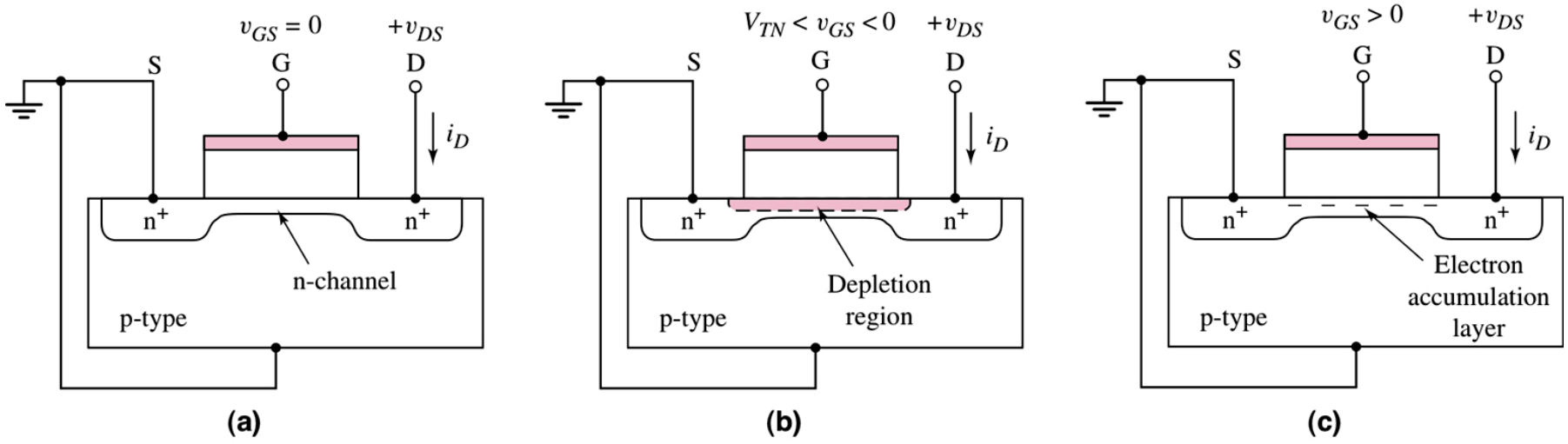
n-Channel Depletion-Mode MOSFET

Depletion-Mode MOSFETS

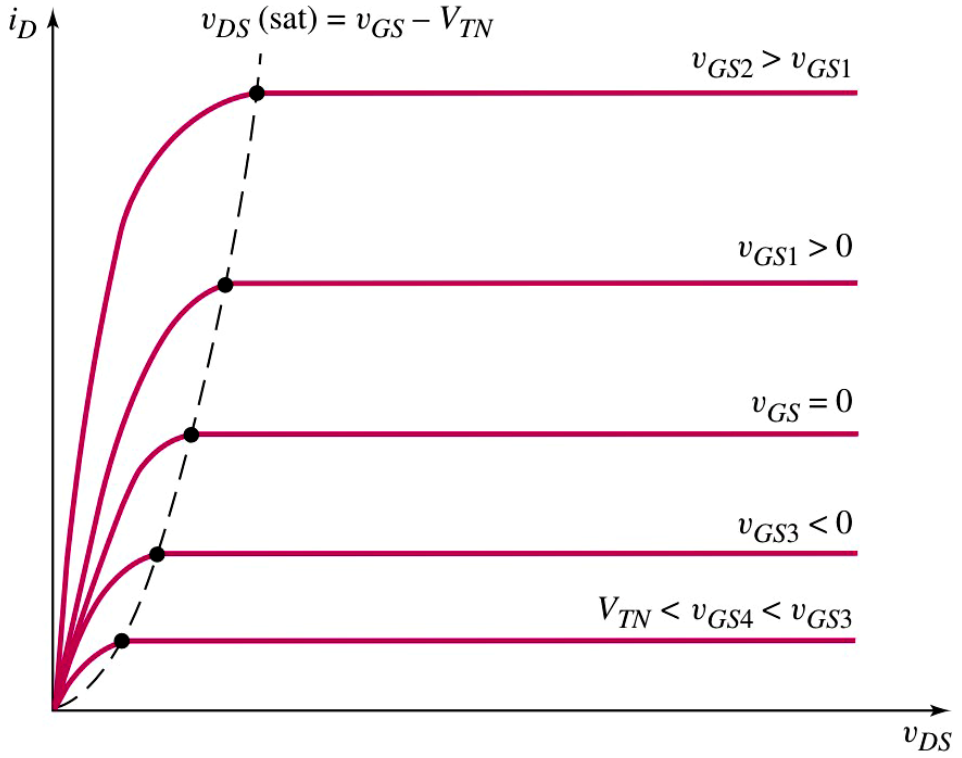


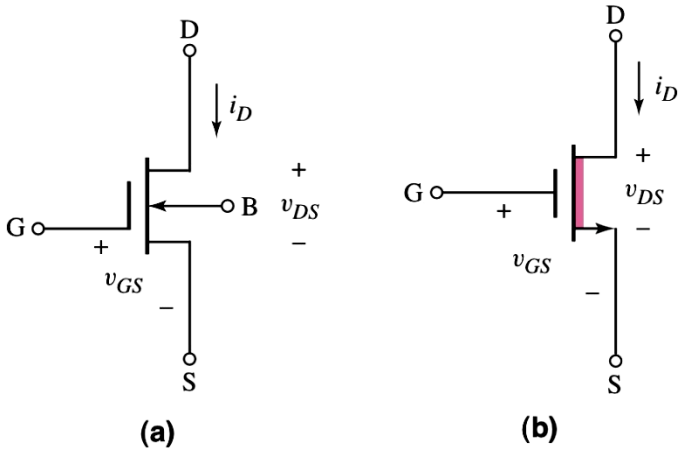
- NMOS transistors with $V_{TN} \leq 0$
- Ion implantation process used to form a built-in *n*-type channel in device to connect source and drain by a resistive channel
- Non-zero drain current for v_{GS}=0, negative v_{GS} required to turn device off.

n-Channel Depletion-Mode MOSFET



Family of i_D Versus v_{DS} Curves: Depletion-Mode nMOSFET

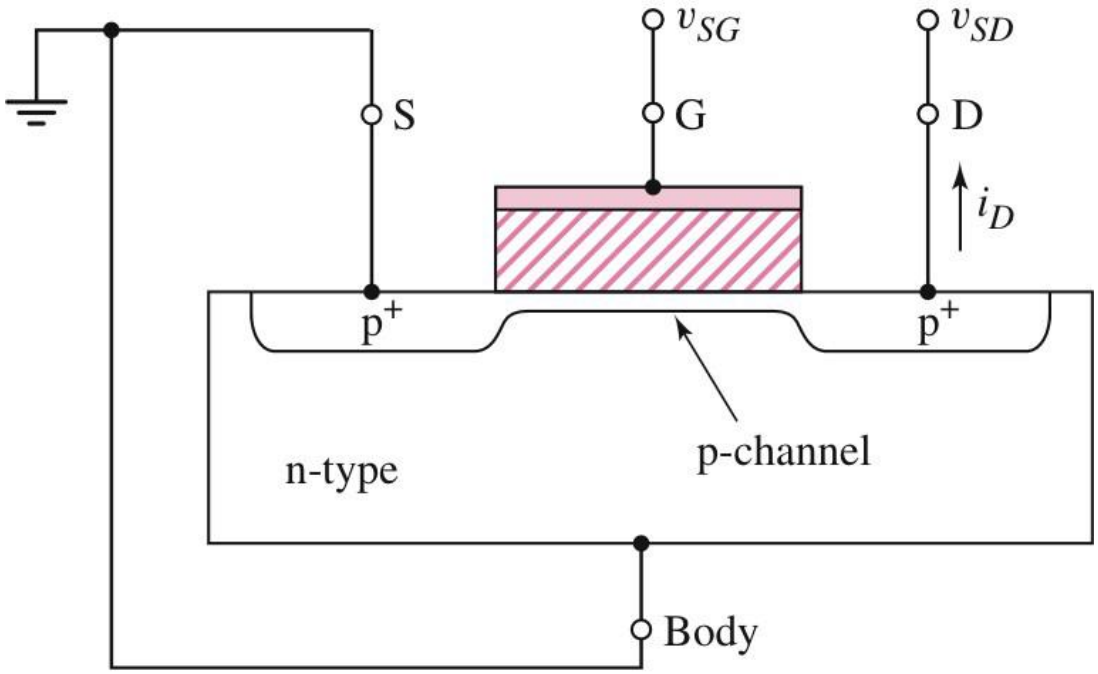


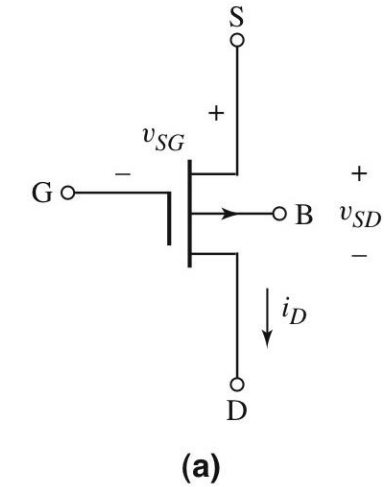


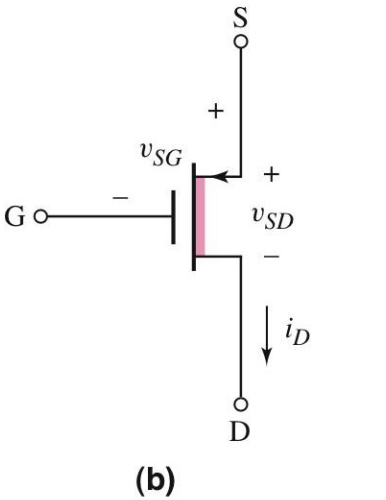
Symbols

p-Channel Depletion-Mode MOSFET

p-Channel Depletion-Mode MOSFET



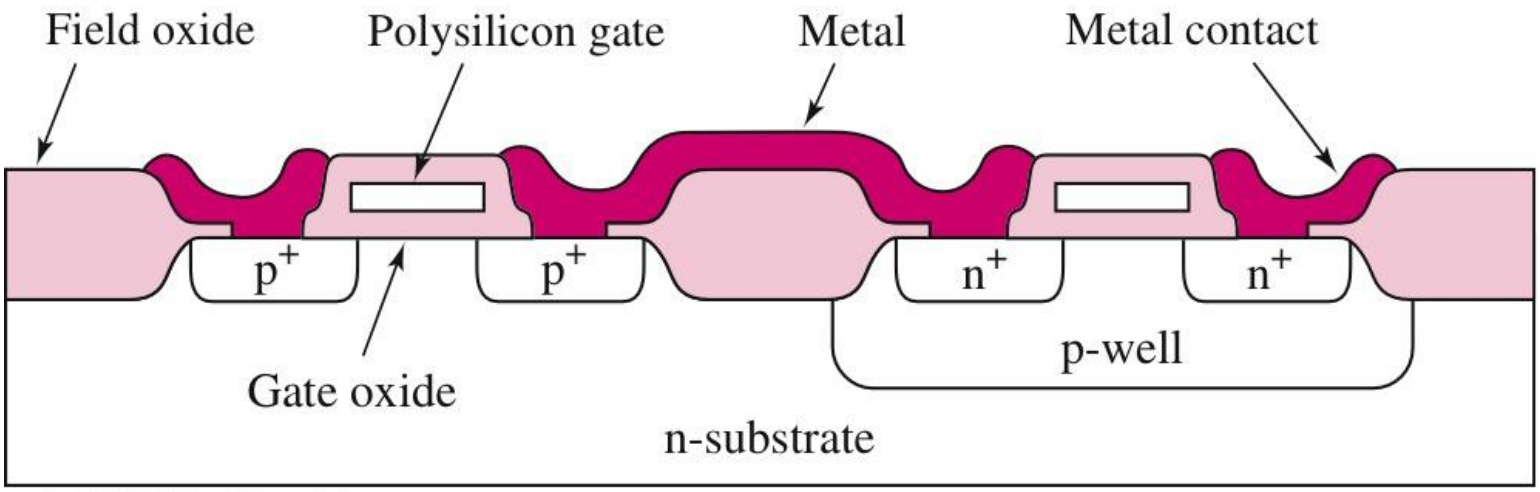




Symbols

Complementary MOSFETs (CMOS)

Cross-Section of nMOSFET and pMOSFET



Both transistors are used in the fabrication of CMOS circuitry.

Summary of I-V Relationships

Region	NMOS	PMOS
Nonsaturation	$v_{DS}<v_{DS}(sat)$ $i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$v_{SD}<v_{SD}(sat)$ $i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation	$v_{DS}>v_{DS}(sat)$ $i_D = K_n[v_{GS} - V_{TN}]^2$	$v_{SD}>v_{SD}(sat)$ $i_D = K_p[v_{SG} + V_{TP}]^2$
Transition Pt.	$v_{DS}(sat) = v_{GS} - V_{TN}$	$v_{SD}(sat) = v_{SG} + V_{TN}$
Enhancement Mode	$V_{TN} > 0V$	$V_{TP} < 0V$
Depletion Mode	$V_{TN} < 0V$	$V_{TP} > 0V$

Conduction Parameters

- NMOSFET $$K_n = \frac{W\mu_n C_{ox}}{L} = k_n^{'}\frac{W}{L}$$

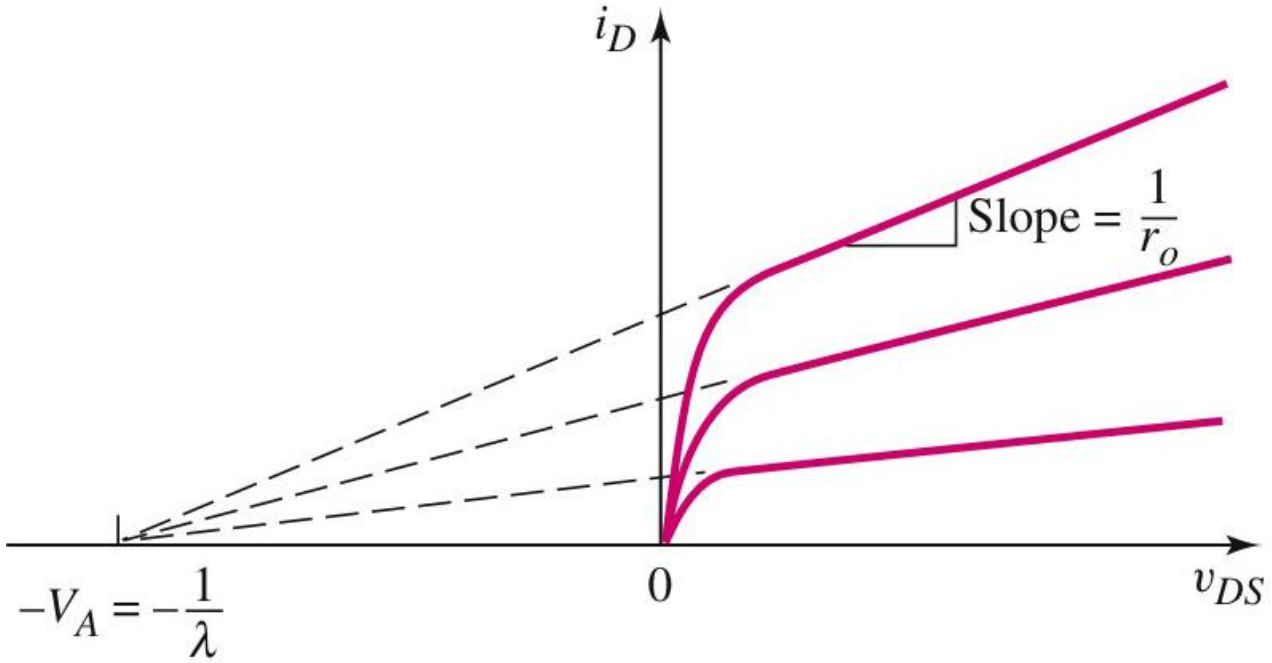
- PMOSFET $$K_p = \frac{W\mu_p C_{ox}}{L} = k_p^{'}\frac{W}{L}$$

where:

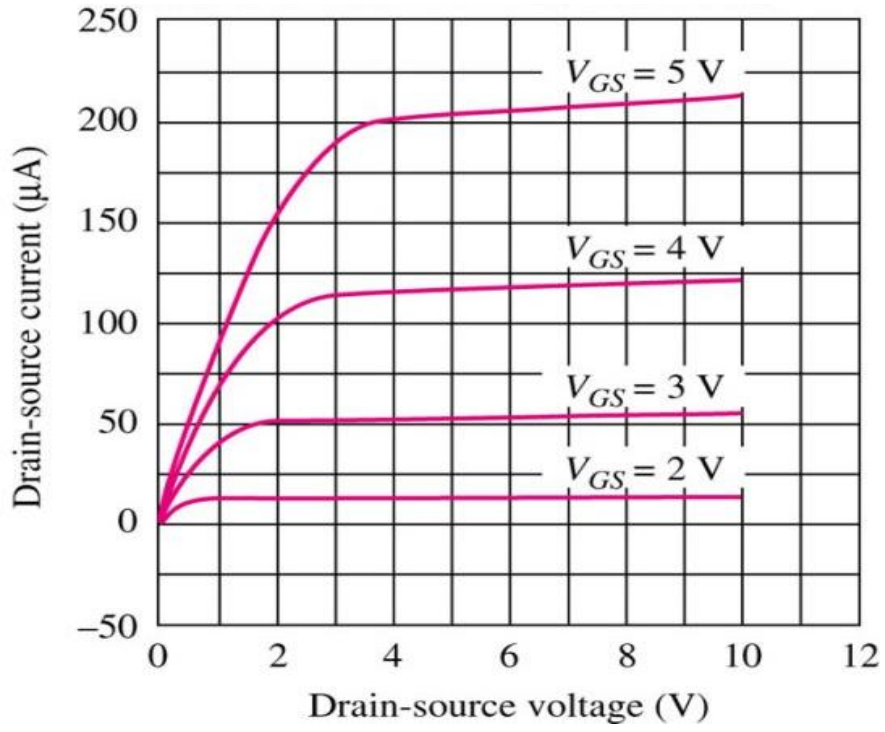
$$C_{ox} = \varepsilon_o / t_{ox}$$

Nonideal I-V Characteristics

Channel Length Modulation: Early Voltage



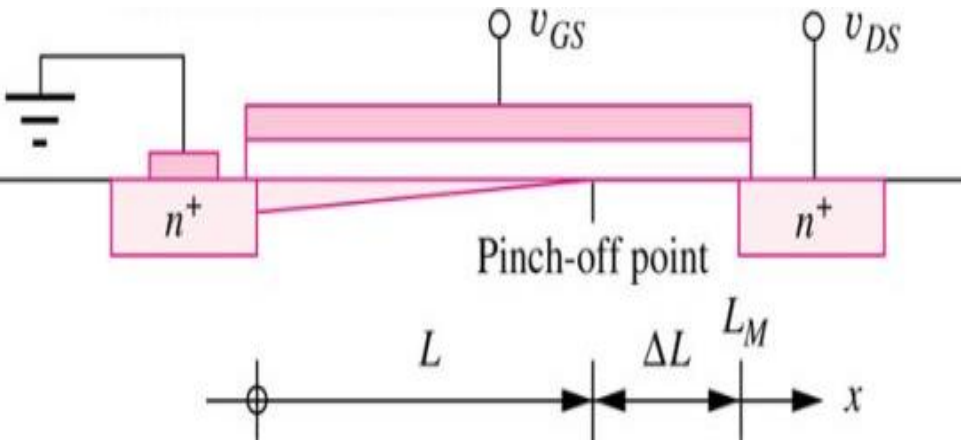
Channel-Length Modulation



- As v_{DS} increases above v_{DSAT}, length of depleted channel beyond **pinch-off point**, ΔL, increases and actual L decreases.
- i_D increases slightly with v_{DS} instead of being constant.

$$i_D = \frac{K_n}{2}\frac{W}{L}\left(v_{GS} - V_{TN}\right)^2\left(1 + \lambda v_{DS}\right)$$

λ= channel length modulation parameter



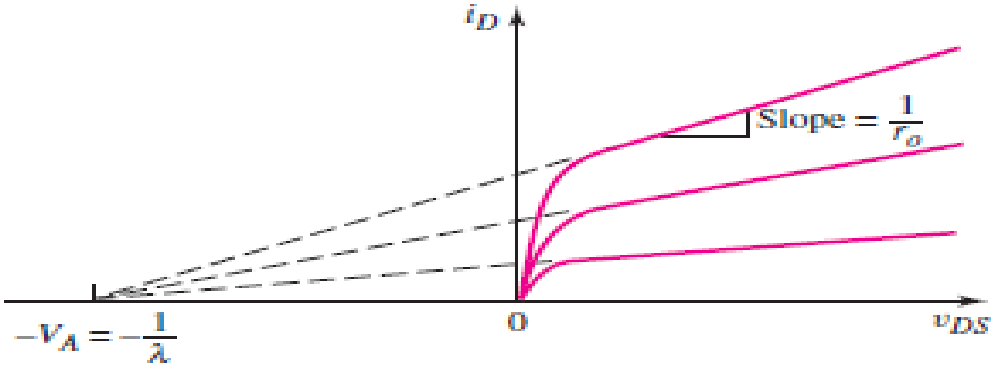


Figure 3.20 Family of i_D versus v_{DS} curves showing the effect of channel length modulation producing a finite output resistance

The parameters λ and V_A are related. From Equation (3.7), we have $(1 + \lambda v_{DS}) = 0$ at the extrapolated point where $i_D = 0$. At this point, $v_{DS} = -V_A$, which means that $V_A = 1/\lambda$.

The output resistance due to the channel length modulation is defined as

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=\text{const.}} \tag{3.8}$$

From Equation (3.7), the output resistance, evaluated at the Q-point, is

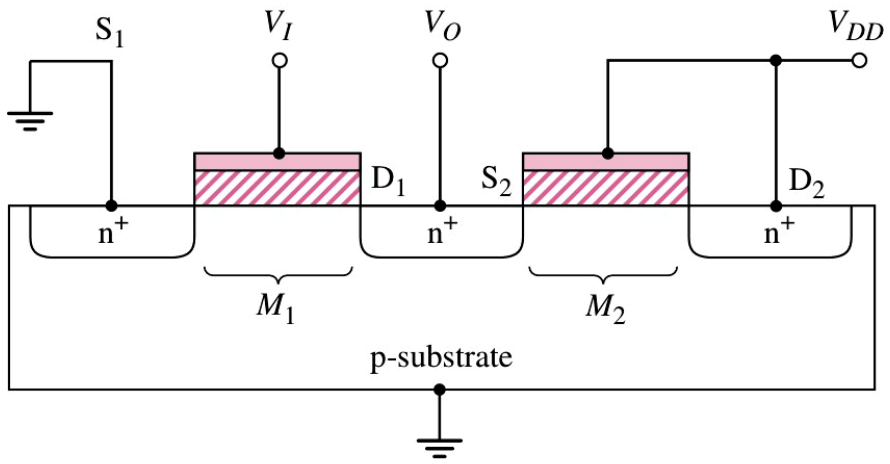
$$r_o = [\lambda K_n (V_{GSQ} - V_{TN})^2]^{-1} \tag{3.9(a)}$$

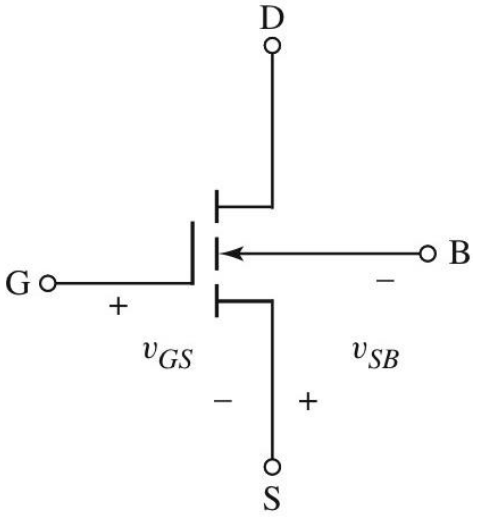
or

$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}} \tag{3.9(b)}$$

The output resistance r_o is also a factor in the small-signal equivalent circuit of the MOSFET, which is discussed in the next chapter.

Body Effect



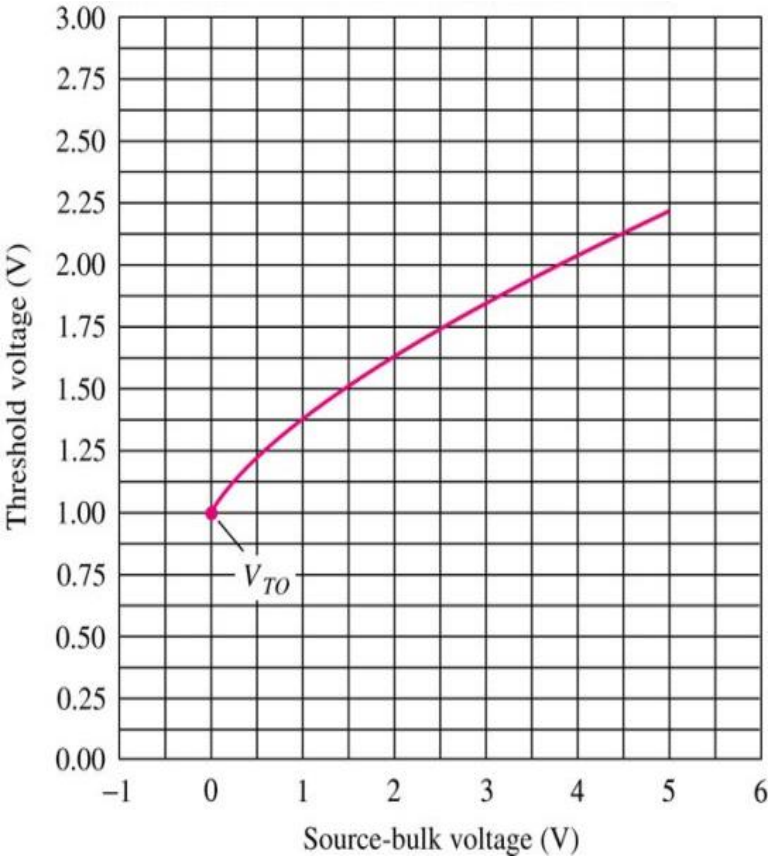


A zero or reverse-bias voltage exists across the source-substrate pn junction.

A change in the source-substrate junction voltage changes the threshold voltage.

Body Effect or Substrate Sensitivity

The assumption that the body lead is connected to the source lead. In integrated circuit design. In this case, any signal voltage on the source lead causes an a signal voltage between the body and source. The effect of this voltage is called the body effect.



This non-zero V_{SB} changes threshold voltage, causing substrate sensitivity to be modeled by:

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

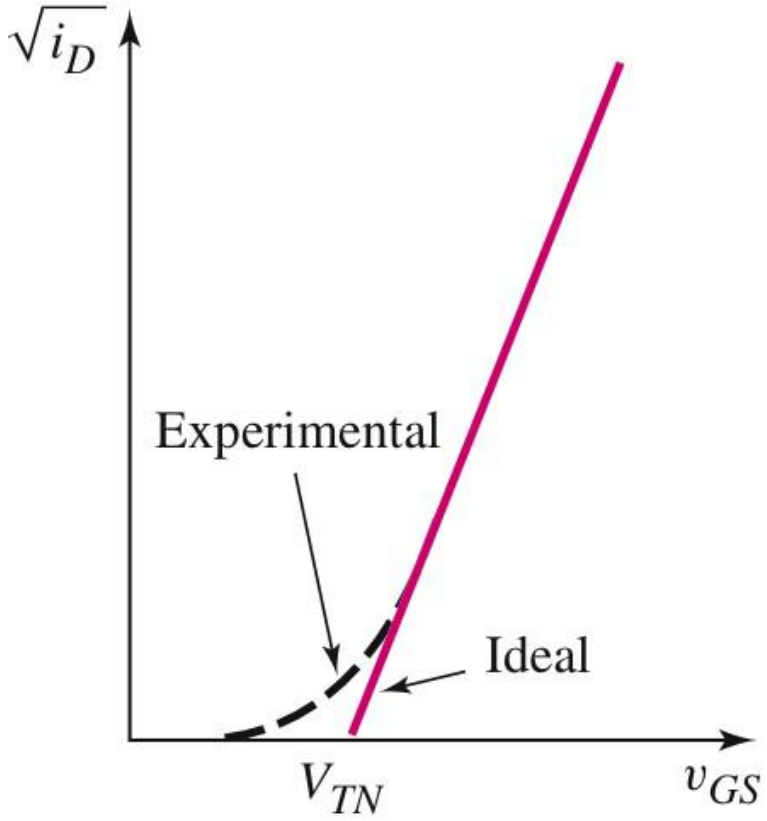
Where

V_{TO}= zero substrate bias for V_{TN} (V)

γ = body-effect parameter ( )

$2F_F$= surface potential parameter (V)

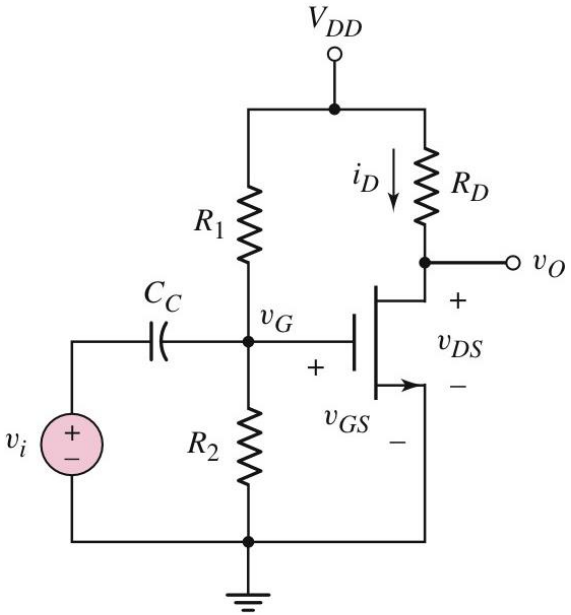
Subthreshold Condition

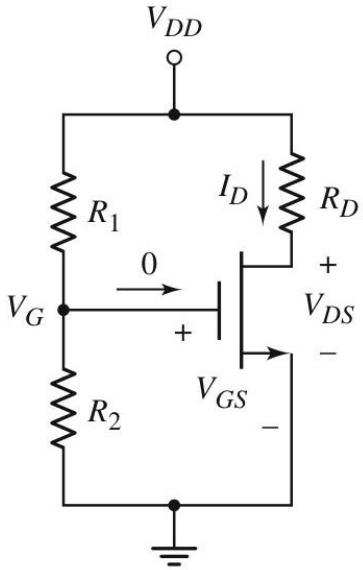


The drain current is non-zero; v_{GS} is slightly less than V_{TN}.

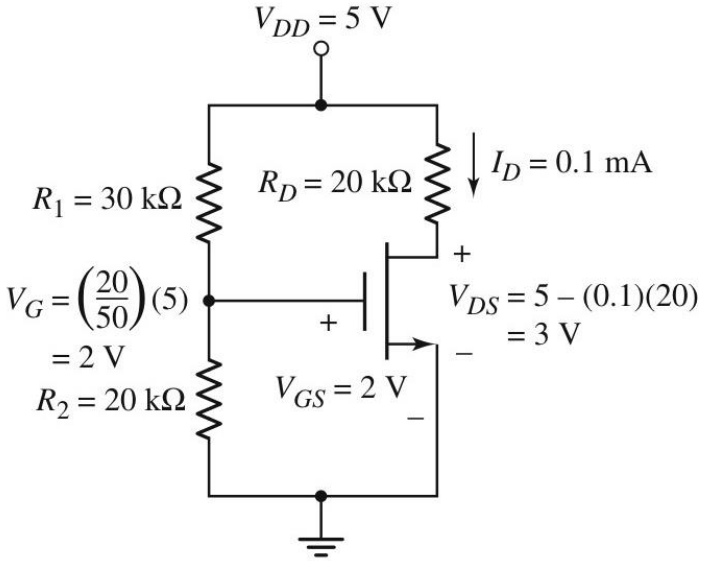
MOSFET DC Circuit Analysis

NMOS Common-Source Circuit



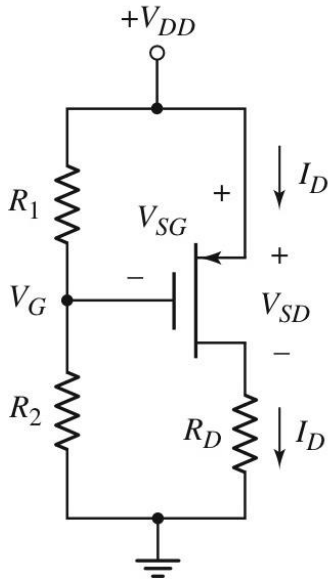


(a)

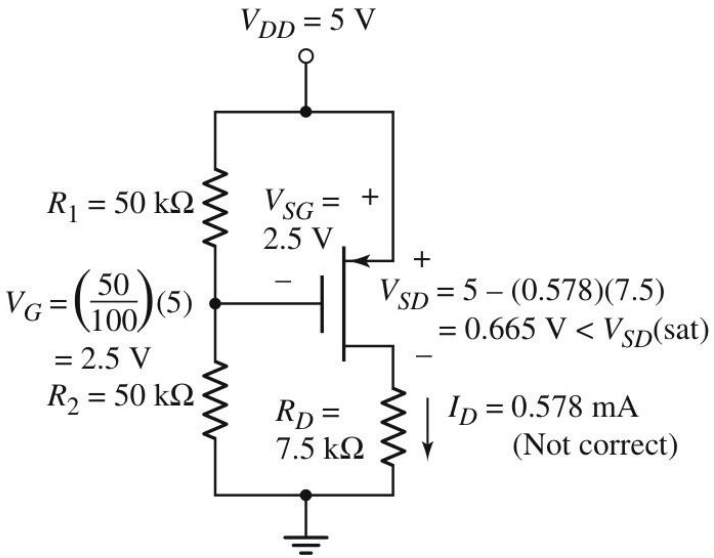


(b)

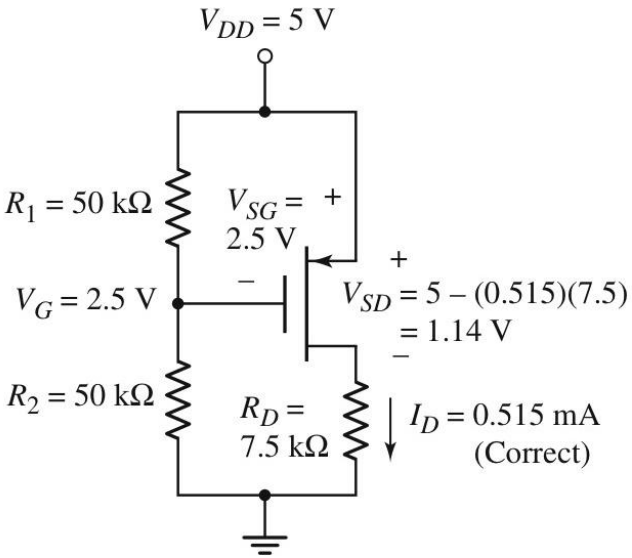
PMOS Common-Source Circuit



(a)

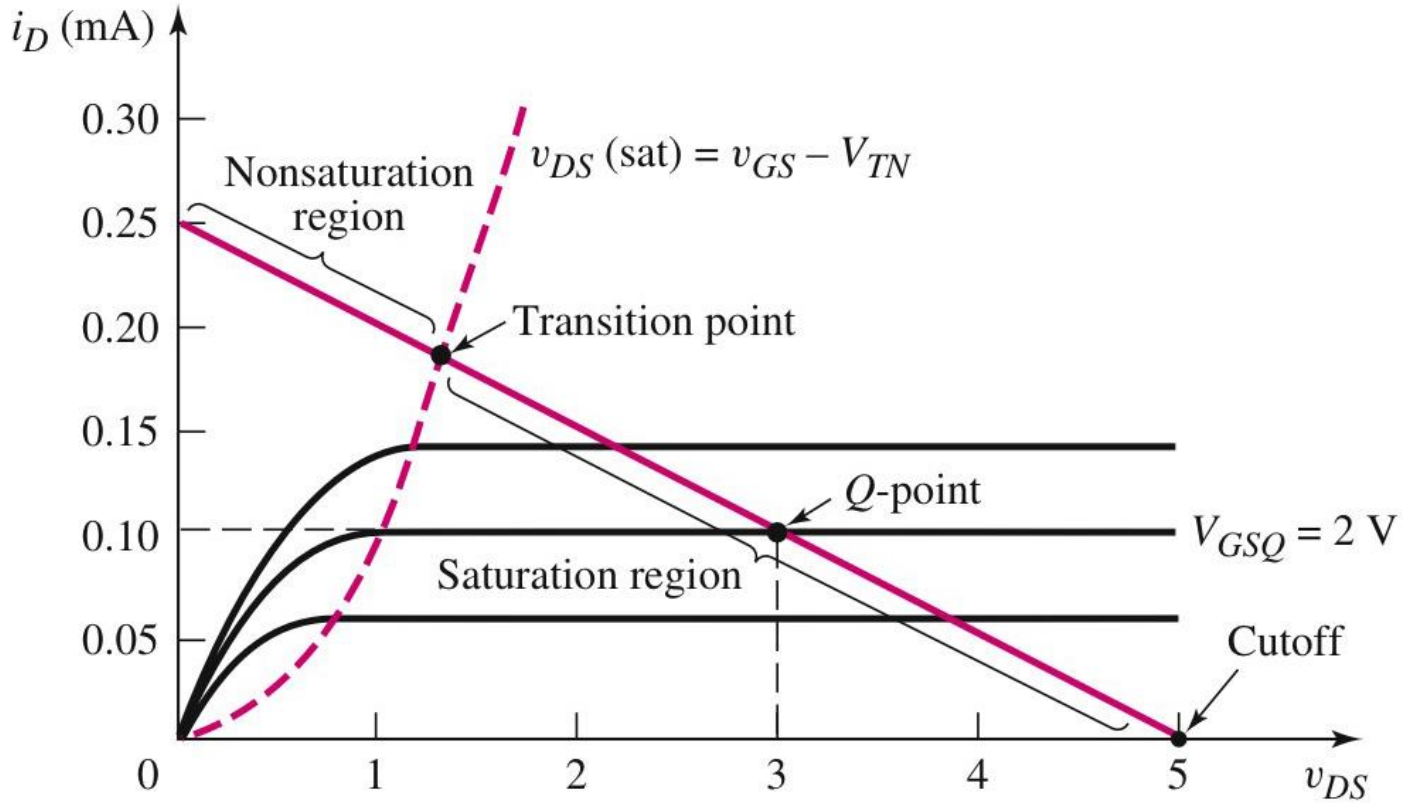


(b)



(c)

Load Line and Modes of Operation: NMOS Common-Source Circuit

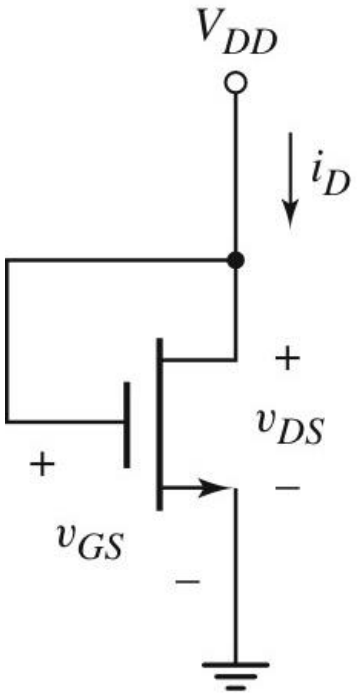


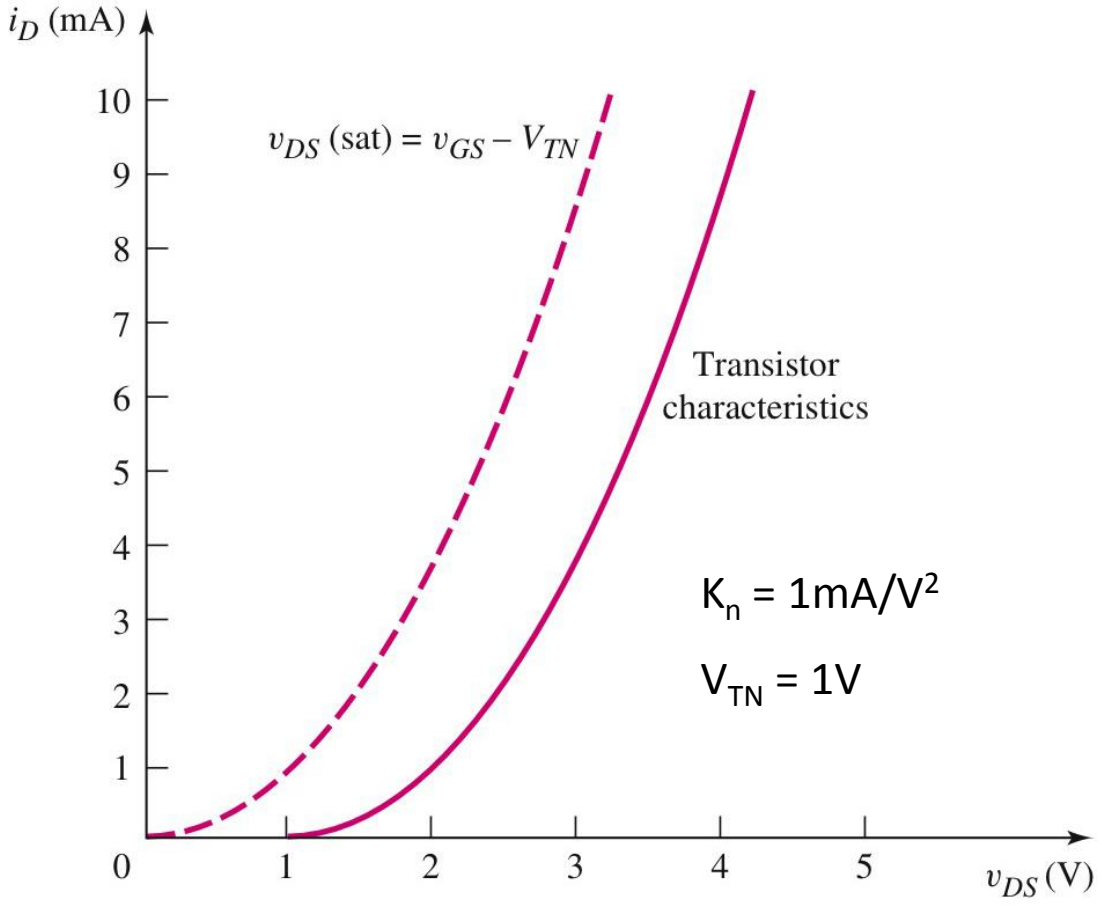
Problem-Solving Technique: NMOSFET DC Analysis

1. Assume the transistor is in saturation.
   a. $V_{GS} > V_{TN}$, $I_D > 0$, & $V_{DS} \geq V_{DS}(sat)$
2. Analyze circuit using saturation I-V relations.
3. Evaluate resulting bias condition of transistor.
   a. If $V_{GS} < V_{TN}$, transistor is likely in cutoff
   b. If $V_{DS} < V_{DS}(sat)$, transistor is likely in nonsaturation region
4. If initial assumption is proven incorrect, make new assumption and repeat Steps 2 and 3.

n-Channel Enhancement-Load Device

Enhancement Load Device



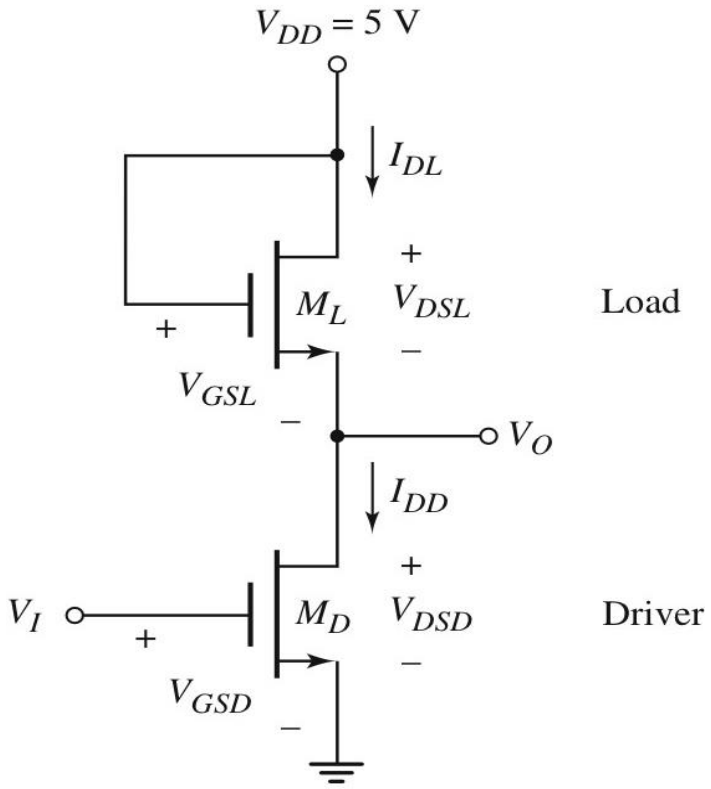


$K_n = 1mA/V^2$

$V_{TN} = 1V$

$$i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_{DS} - V_{TN})^2$$

Circuit with Enhancement Load Device and NMOS Driver

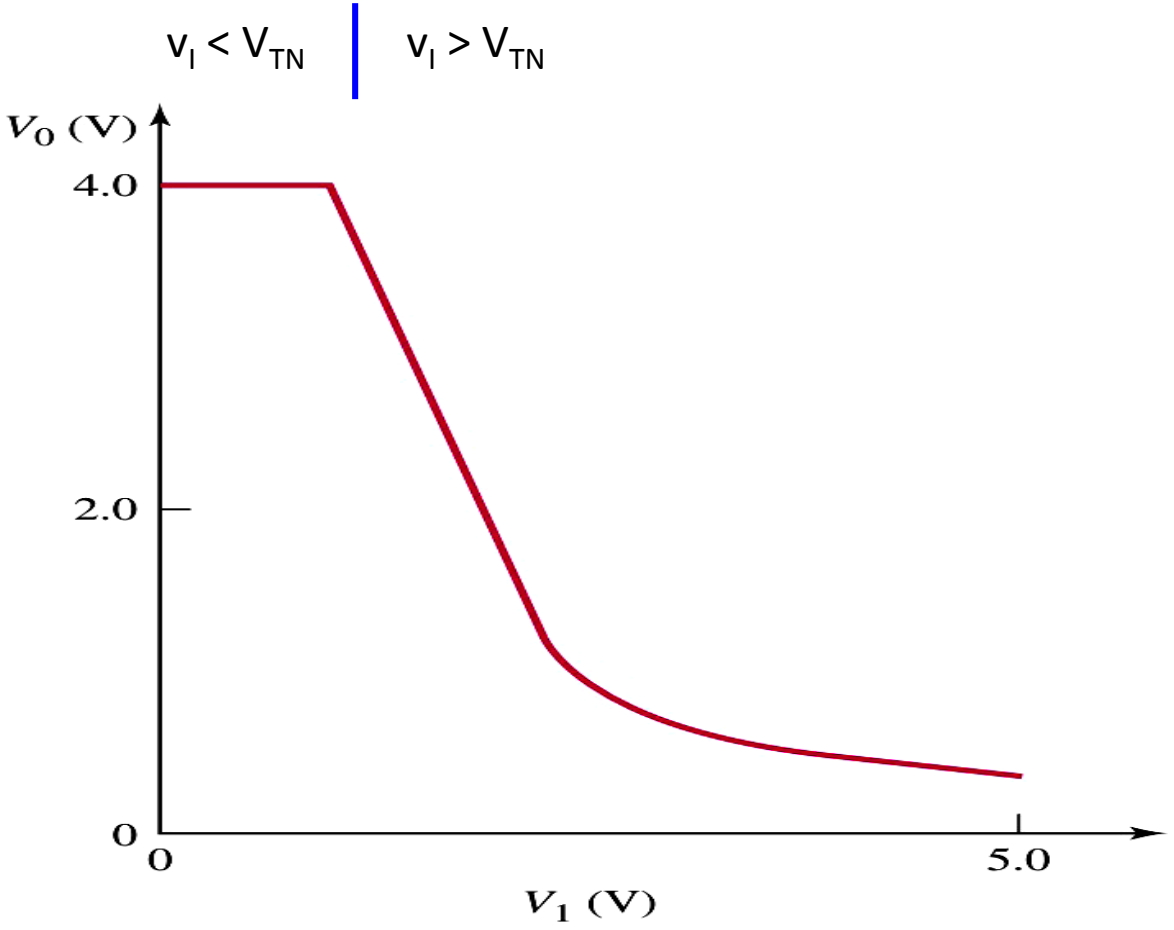


M_L is always in **saturation.**

M_D can be biased either in **saturation** or **nonsaturation** region.

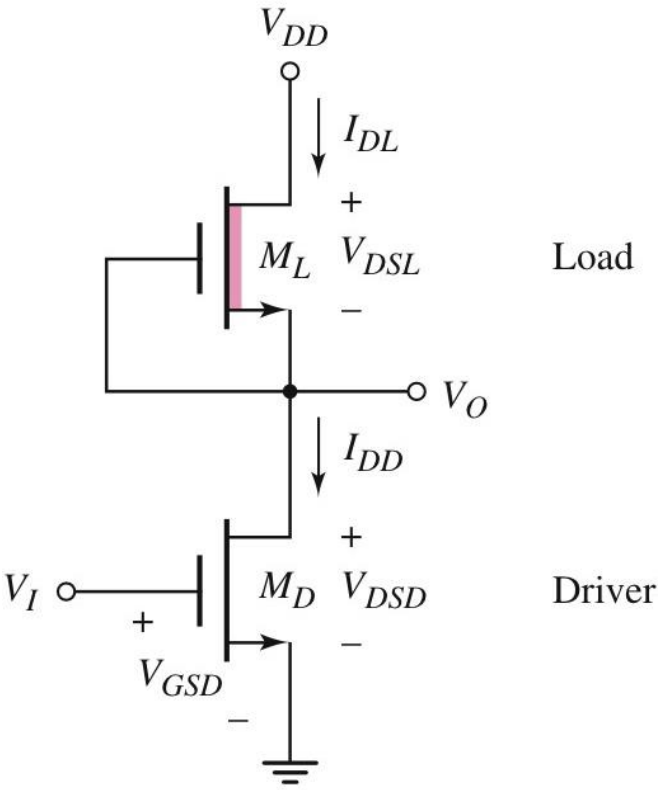
Voltage Transfer Characteristics:

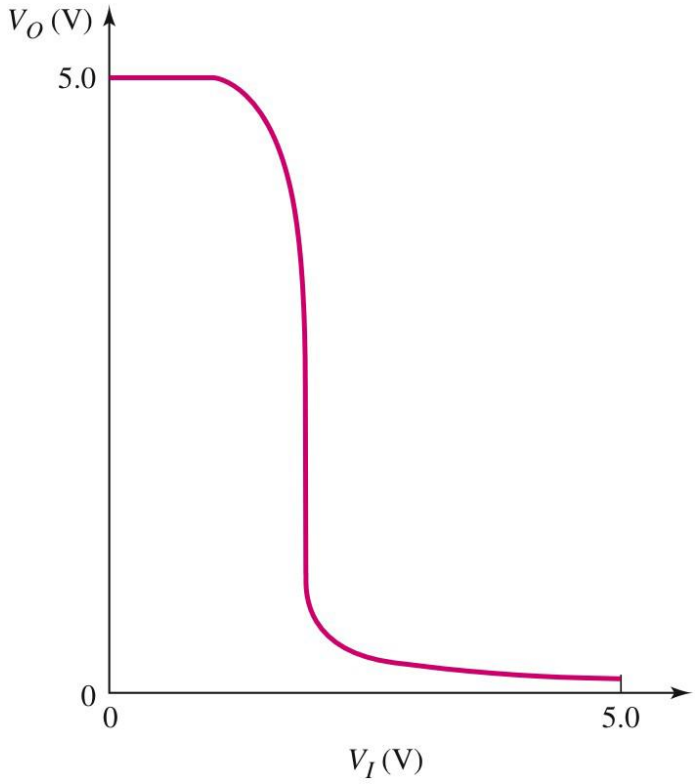
NMOS Inverter with Enhancement Load Device



n-Channel Depletion-Load Device

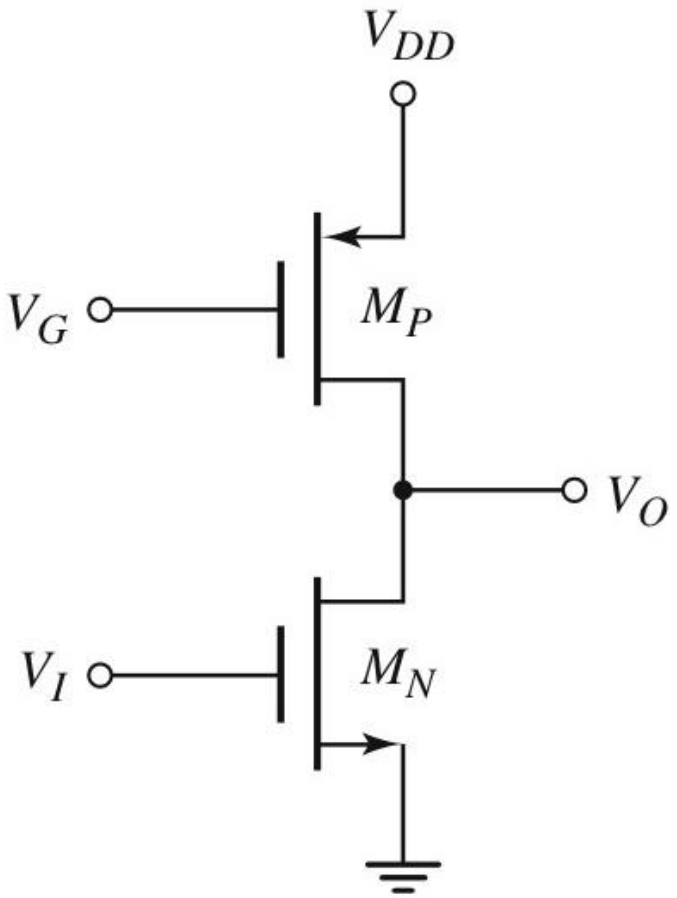
NMOS Inverter with Depletion Load Device

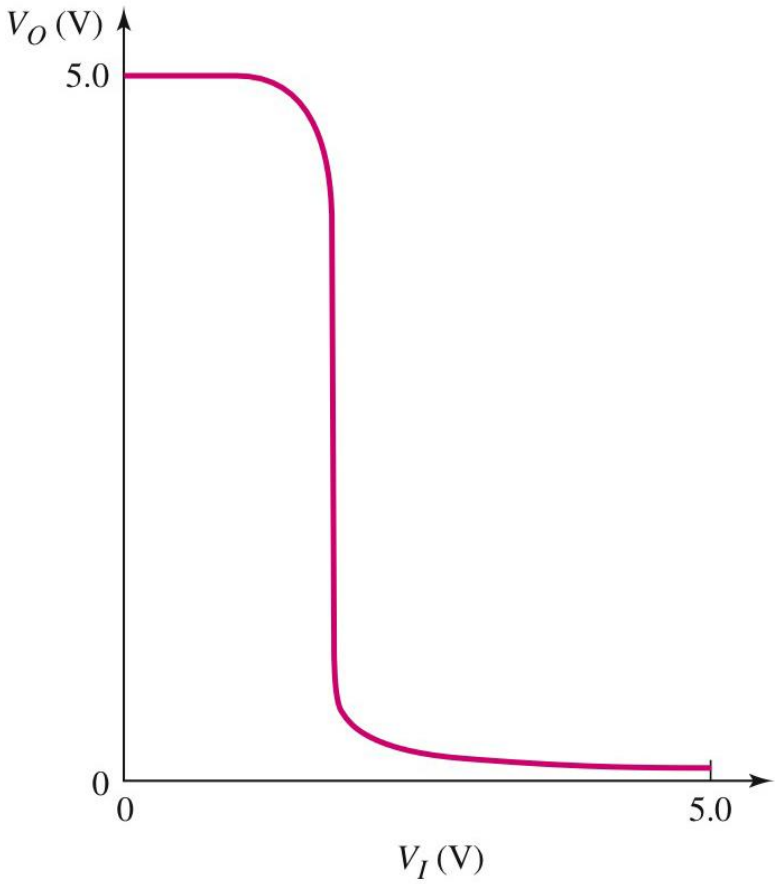




p-Channel Enhancement-Load Device

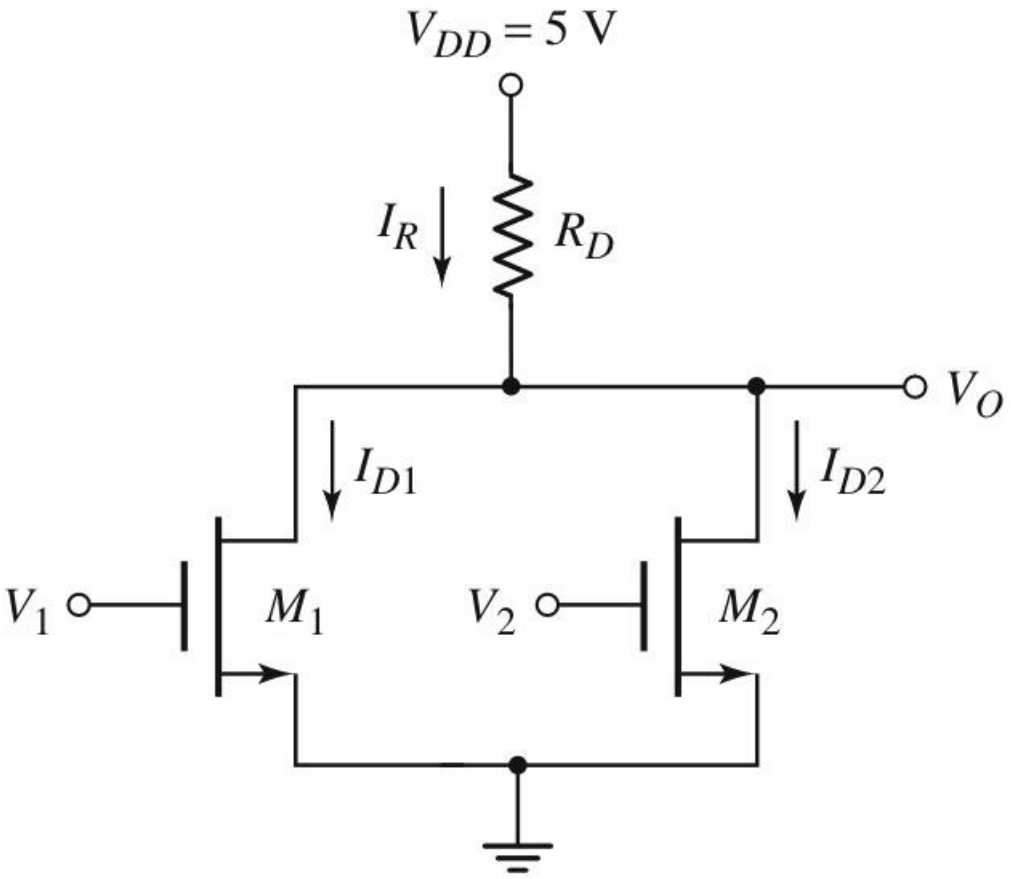
CMOS Inverter





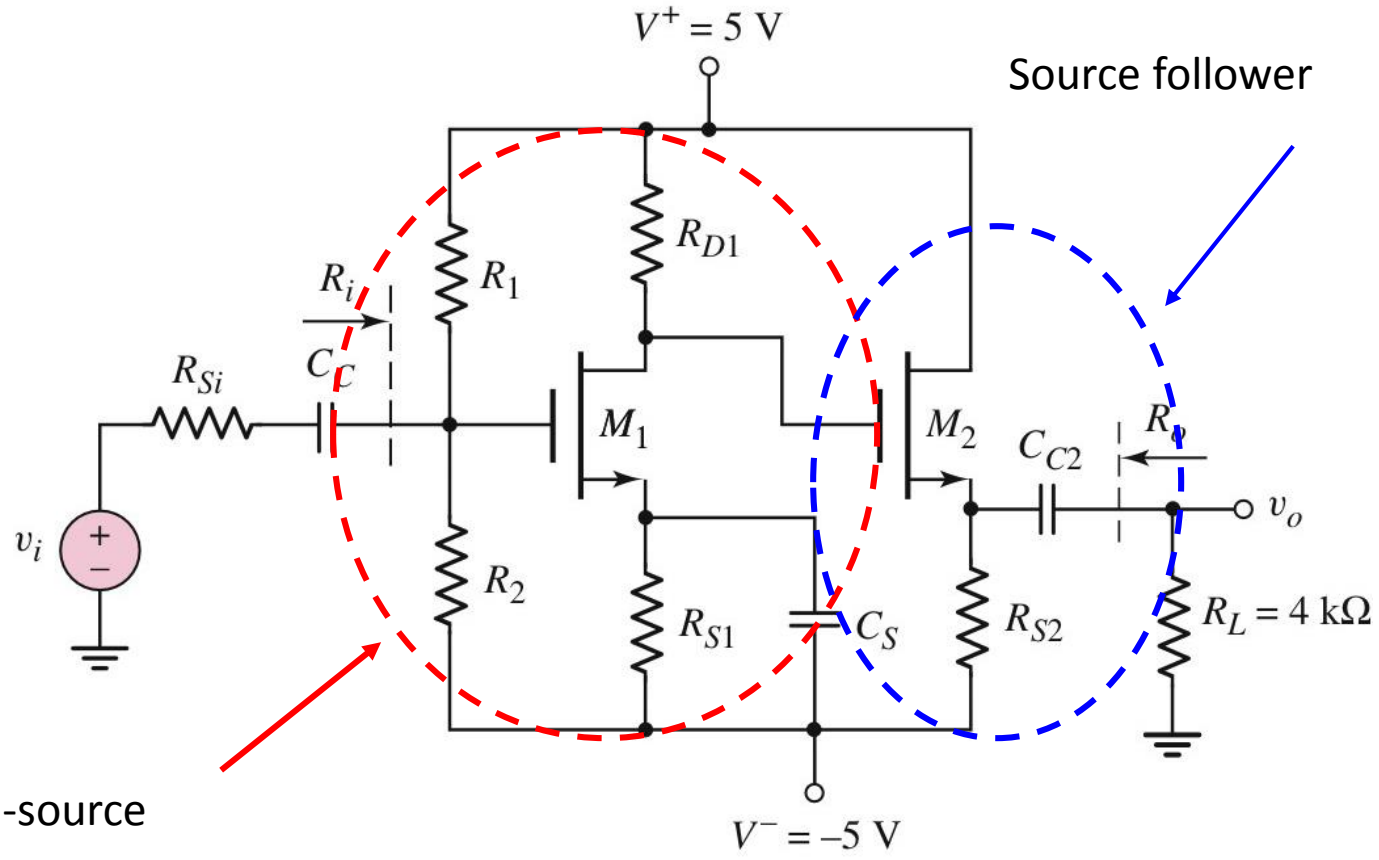
Basic MOSFET Applications

2-Input NMOS NOR Logic Gate



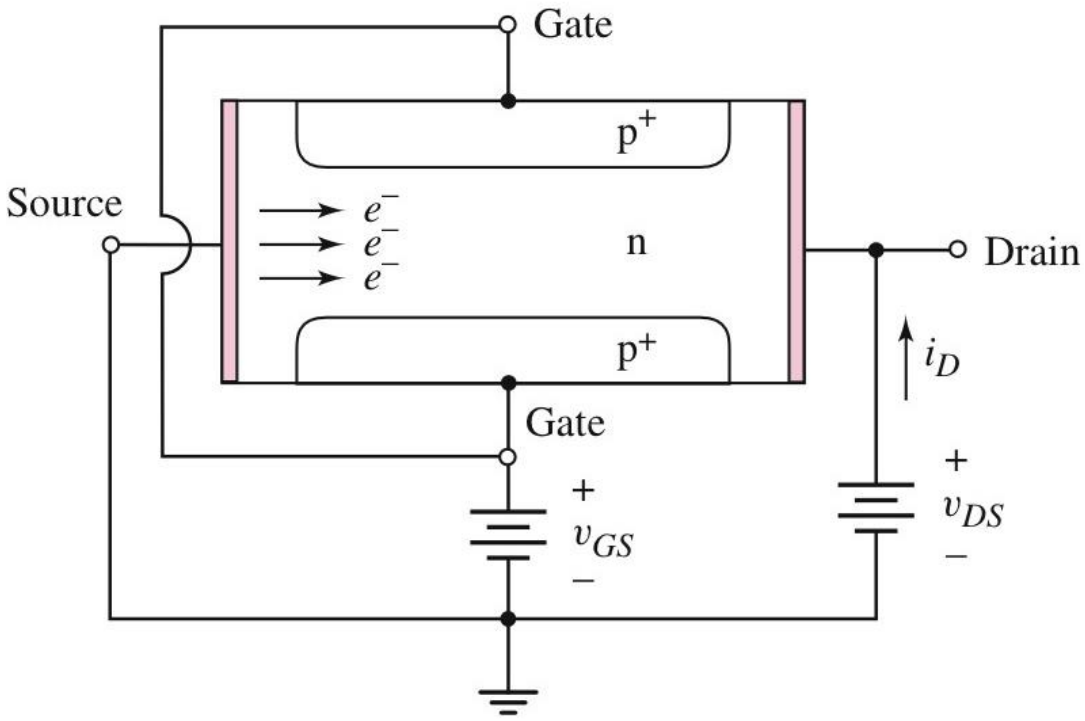
V_1 (V)	V_2 (V)	V_O (V)
0	0	High
5	0	Low
0	5	Low
5	5	Low

2-Stage Cascade Amplifier



Junction Field-Effect Transistor

Cross Section of n-Channel Junction Field Effect Transistor (JFET)

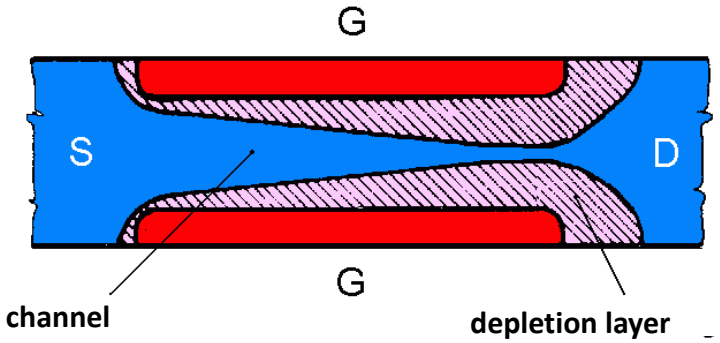


JUNCTION FET: depletion layers of pn-junctions close the channel

Most important parameter: pinch-off voltage

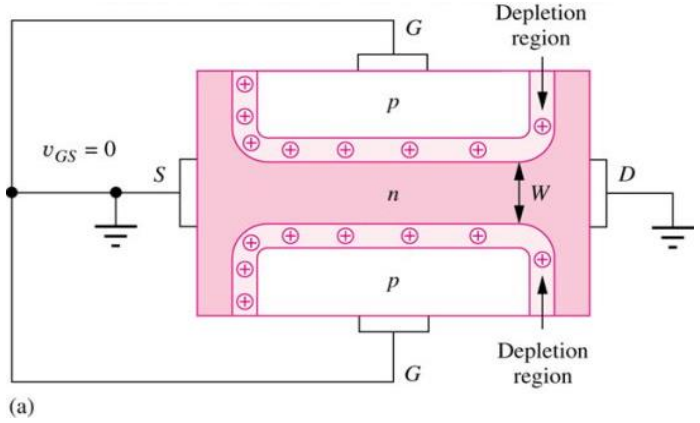
The JFET

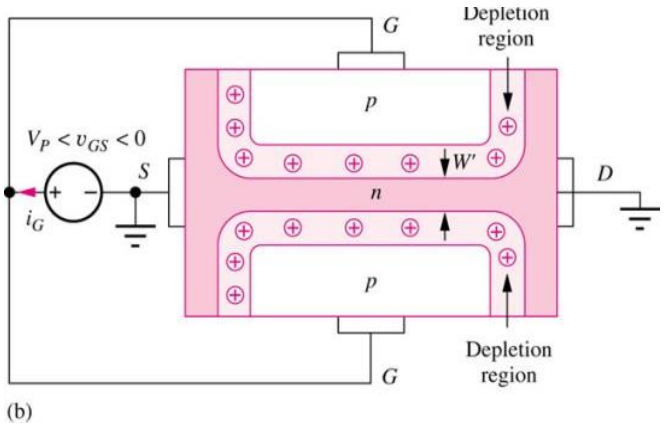
The width of the closed PN junction controls the conductivity of the channel

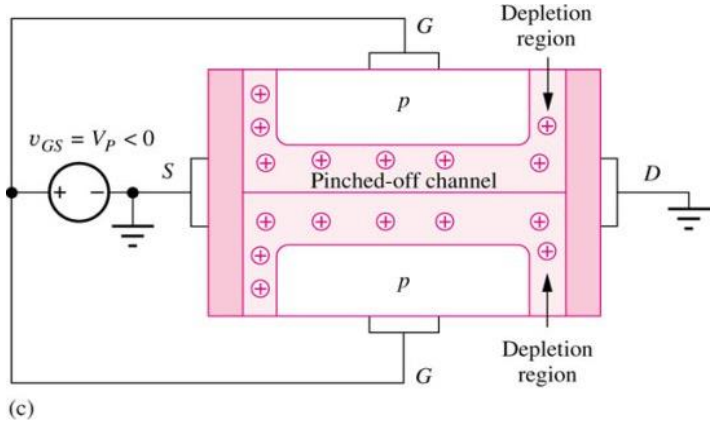


PN junction $\Rightarrow$ junction FET

JFET with Gate-Source Bias

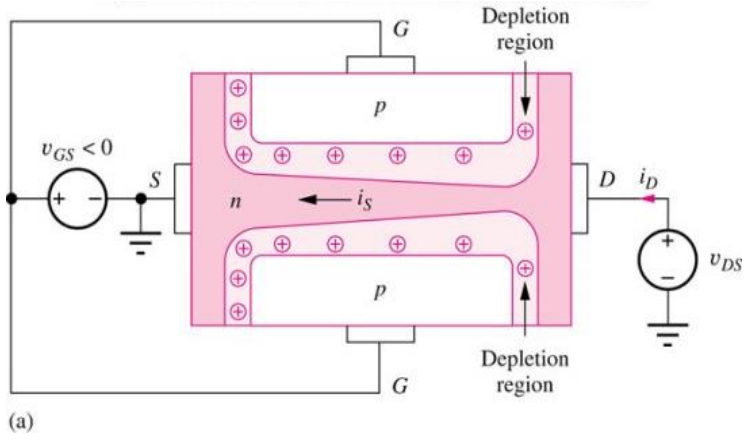


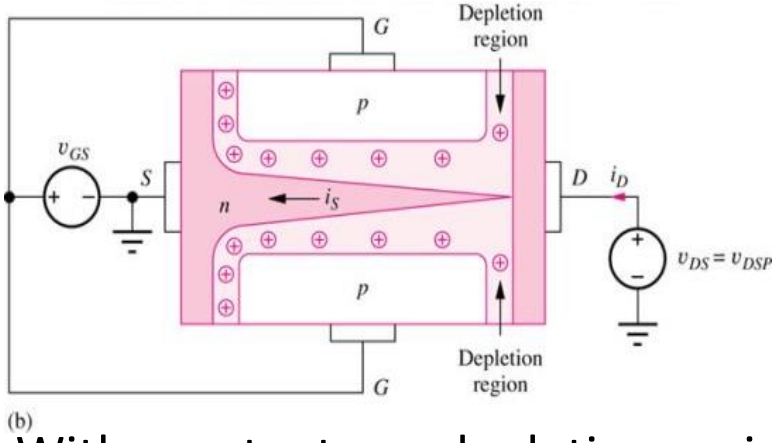


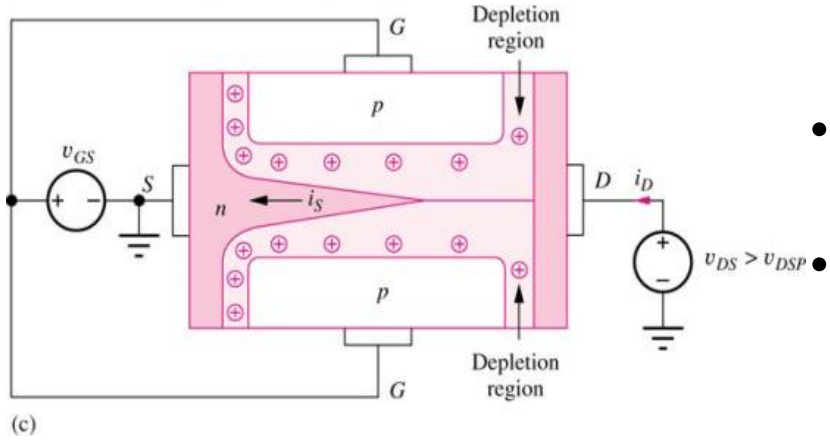


- v_{GS} =0, gate isolated from channel.
- $V_P < v_{GS} < 0$, W'<W, channel resistance increases, gate-source junction reverse-biased, i_G almost 0.
- $v_{GS} = V_P < 0$, channel region pinched-off, channel resistance infinite.

JFET Channel with Drain-Source Bias

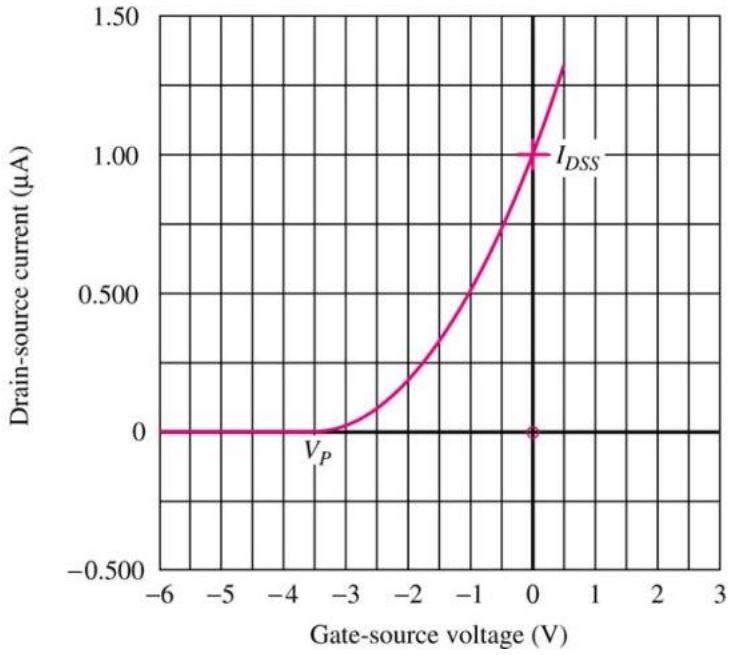




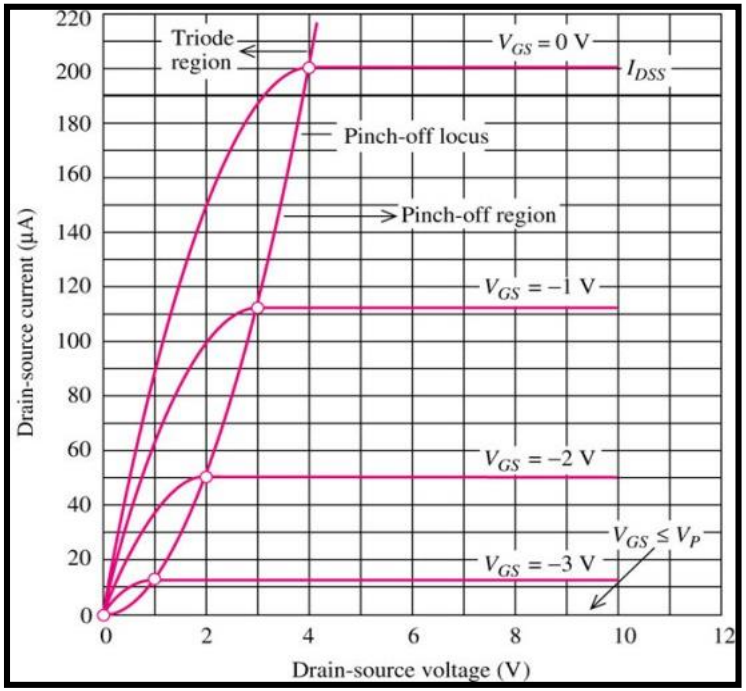


- With constant v_{GS}, depletion region near drain increases with v_{DS}.
- At $v_{DSP} = v_{GS} - V_P$,channel is totally pinched-off, i_D is saturated.
- JFET also suffers from channel length modulation like MOSFET at larger values of v_{DS}.

N-Channel JFET: *i-v* Characteristics



Transfer Characteristics



Output Characteristics

Chapter 3

- Study and understand the structure, operation and characteristics of MOSFETs.

- Understand and become familiar with the dc analysis and design techniques of MOSFET circuits.

- Examine three applications of MOSFET circuits.

- Investigate current source biasing of MOSFET circuits, such as those used in integrated circuits.

- Analyze the dc biasing of multistage or multi-transistor circuits.

- Understand the operation and characteristics of the junction field-effect transistor, and analyze the dc response of JFET circuits.