EEE104 – Digital Electronics (I)

Lecture 14

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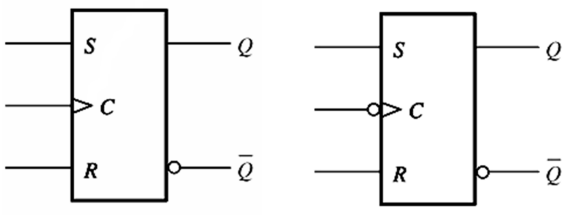
In This Session

Flip-Flops and Related Devices

- Latches
- Edge-Triggered Flip-Flops
- Flip-Flop Applications

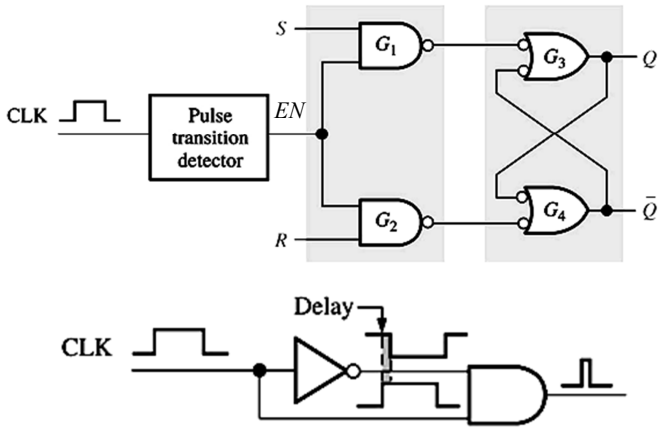
Edge-Triggered Flip-Flops

- An **edge-triggered** flip-flop changes state at the edges of a clock pulse.
- It is identified by a small triangle at the clock (C) input.
- It can be either rising-edge triggered or falling edge triggered (bubble at C input).

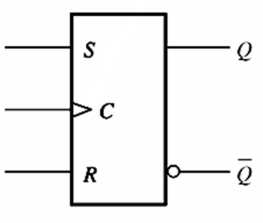


Edge-Triggered Flip-Flops

A Method of Edge-Triggering



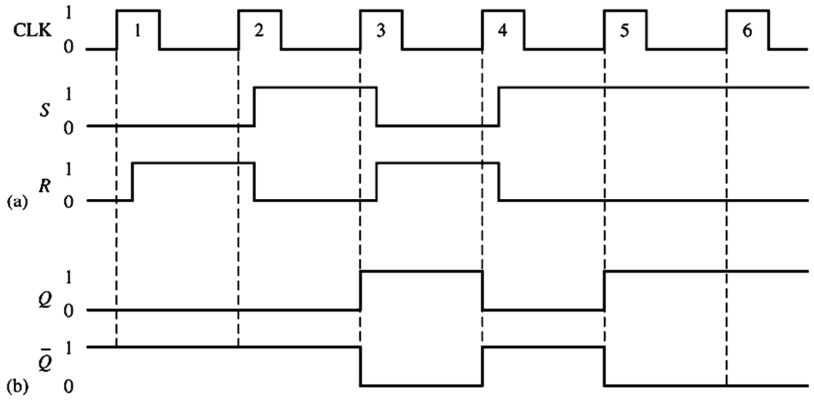
Edge-Triggered S-R Flip-Flops



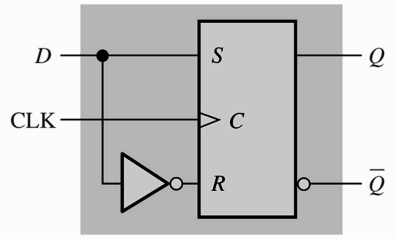
INPUTS S	R	CLK	OUTPUTS Q	$\overline{Q}$	COMMENTS
0	0	X	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

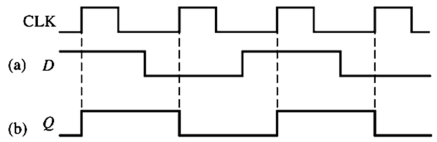
Edge-Triggered S-R Flip-Flops

An Example



Edge-Triggered D Flip-Flops

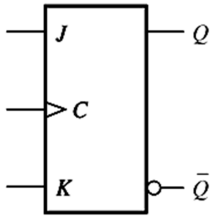




INPUTS D	CLK	OUTPUTS Q	$\overline{Q}$	COMMENTS
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

↑ = clock transition LOW to HIGH

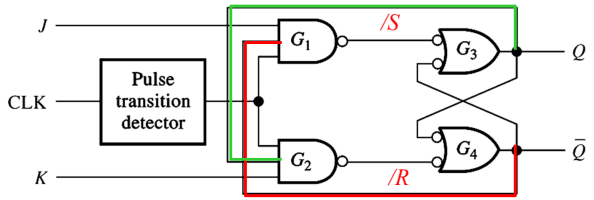
Edge-Triggered J-K Flip-Flops



- The J-K flip-flop is similar to the S-R flip-flop but has no invalid state.
- When J = 1 and K = 1, the output will be toggled at the rising edge of the clock.

INPUTS J	K	CLK	OUTPUTS Q	$\overline{Q}$	COMMENTS
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

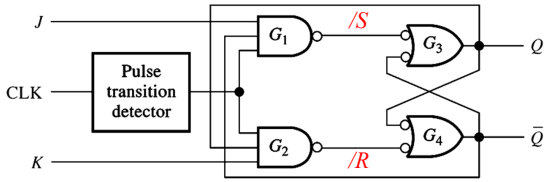
Edge-Triggered J-K Flip-Flops



The difference with its S-R counterpart:

- The Q output is fed back to the input of gate G_2.
- The /Q output is fed back to the input of gate G_1.

Edge-Triggered J-K Flip-Flops

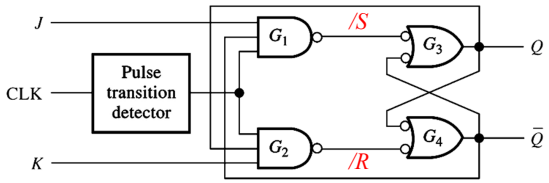


How does it work?

- When both J and K are LOW, /S and /R are HIGH. Q will not change.
- When J = 1 and K = 0, /R is HIGH and /S = Q at triggering edges of CLK. If Q = 0, it will be SET. If Q = 1, no change. So Q = 1.

$$/S = \overline{1 \cdot \bar{Q} \cdot 1} = Q$$

Edge-Triggered J-K Flip-Flops

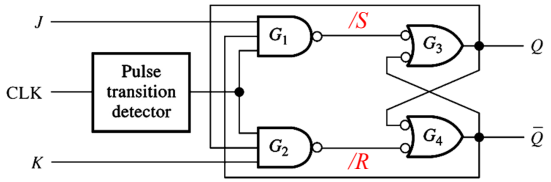


How does it work?

- When J = 0 and K = 1, /S is HIGH and /R = /Q at triggering edges of CLK. If Q = 1, it will be RESET. If Q = 0, /R is HIGH and no change at Q. So Q = 0.

$$/R = \overline{1 \cdot Q \cdot 1} = \bar{Q}$$

Edge-Triggered J-K Flip-Flops



How does it work?

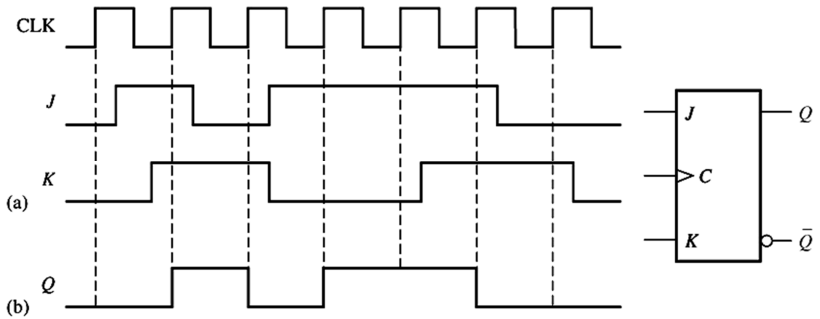
- When both J and K are HIGH, /Q functions as the SET signal and Q functions as the RESET signal. $/S = \overline{1 \cdot \bar{Q} \cdot 1} = Q$ $S = \bar{Q}$

  $/R = \overline{1 \cdot Q \cdot 1} = \bar{Q}$ $R = Q$

  - If Q = 1, it is ready to be reset.
  - If /Q = 1, it is ready to be set.

Edge-Triggered J-K Flip-Flops

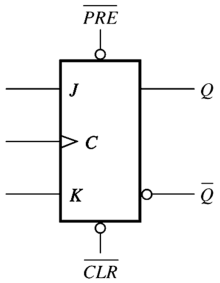
An Example



Edge-Triggered J-K Flip-Flops

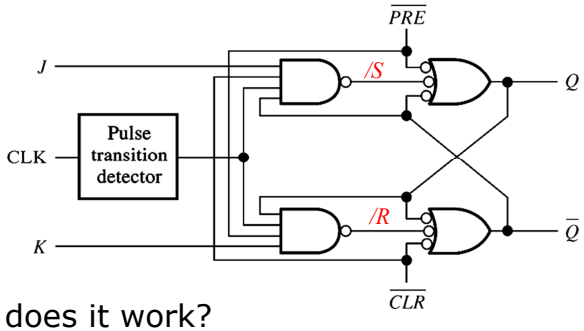
Asynchronous Preset and Clear Inputs

- **Synchronous** inputs affects the state of the flip-flop only on the triggering edge of the clock.
- **Asynchronous** inputs affect the state of the flip-flop independent of the clock.



- The Clear input is used to RESET the output.
- The Preset input is used to SET the output.

Edge-Triggered J-K Flip-Flops

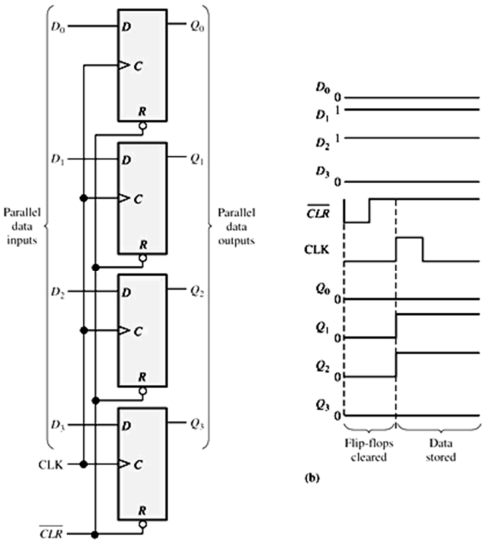


How does it work?

- When /CLR = 0 and /PRE = 1, /R = 0 and /S = 1. Q will be RESET.
- When /CLR = 1 and /PRE = 0, /R = 1 and /S = 0. Q will be SET.

Flip-Flop Applications

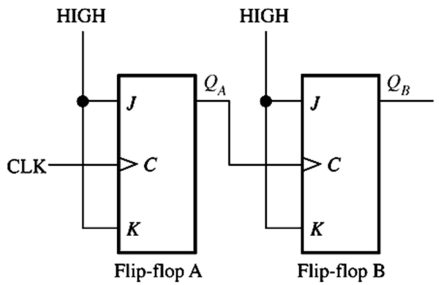
Parallel Data Storage

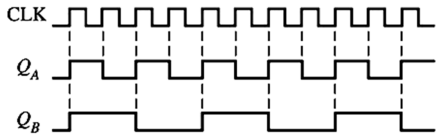


Flip-Flop Applications

Frequency Division

By connecting n flip-flops in this way, a frequency division of 2^n is achieved.





Flip-Flop Applications

Counting

Negative edge-triggered J-K flip-flops are used.