EEE205 – Digital Electronics (II)

Lecture 3

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In This Session

- More Powerful PLDs
  - Complex Programmable Logic Devices (CPLD)
  - Field Programmable Gate Arrays (FPGA)

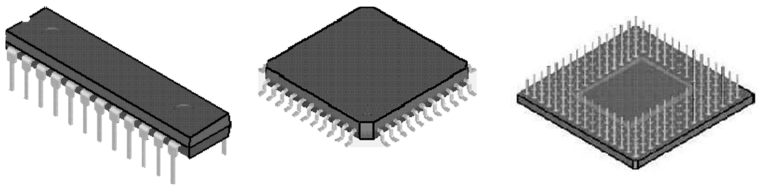
Programmable Logic Devices (PLDs)

Types

- SPLDs — up to 600 *equivalent gates* each.
- CPLDs — up to thousands of *equivalent gates* each.
- FPGAs — hundreds of thousands of *equivalent gates* each.

equivalent gates: 2-input NAND gates

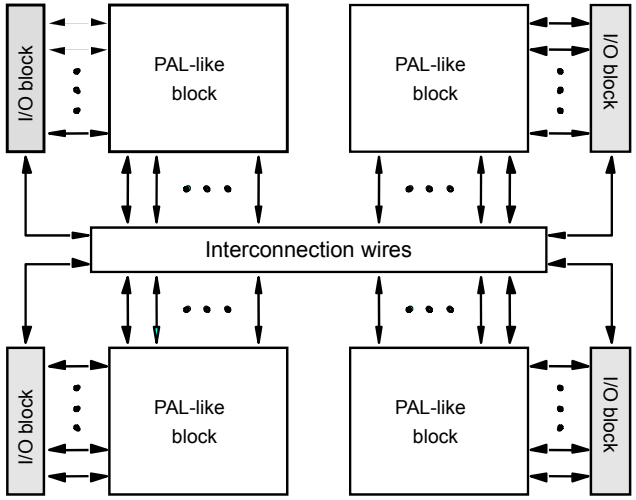
SPLD CPLD FPGA



Complex Programmable Logic Devices (CPLD)

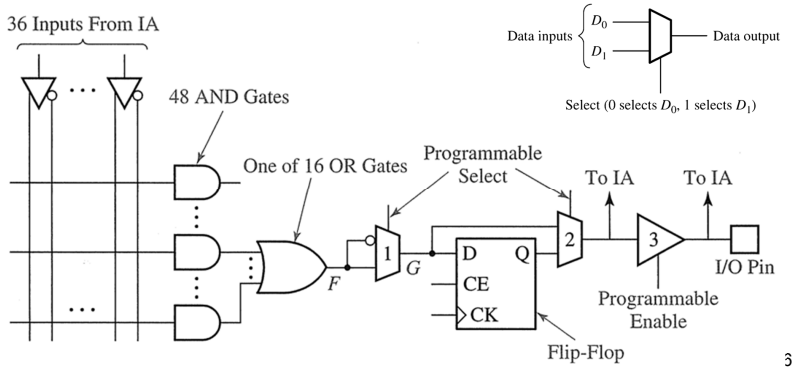
- A CPLD comprises multiple circuit blocks, each is similar to a PLA or a PAL and called a *PAL-like block*.
- These PAL-like blocks are connected to a set of *interconnection wires*.
- Each PAL-like block is also connected to a subcircuit called *I/O block*, which corresponds to the chip's input and output pins.

Complex Programmable Logic Devices (CPLD)



Complex Programmable Logic Devices (CPLD)

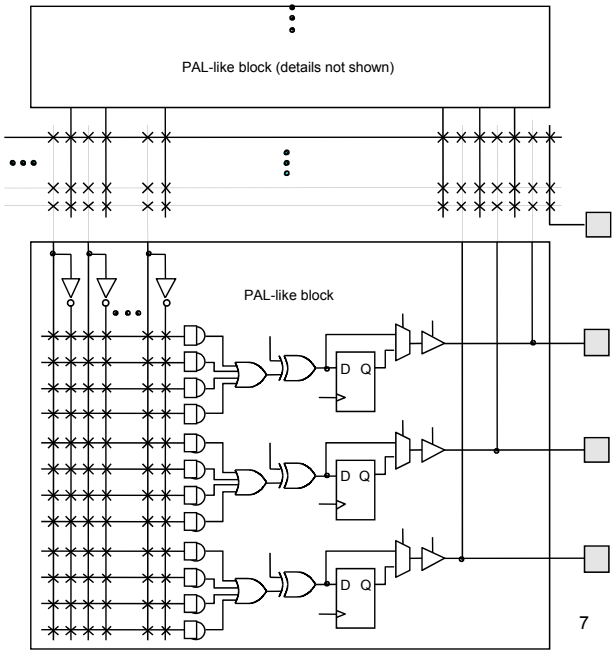
- Each PAL-like block includes multiple (typically 16) macrocells.
- A signal in one block can be used as an input to another block.



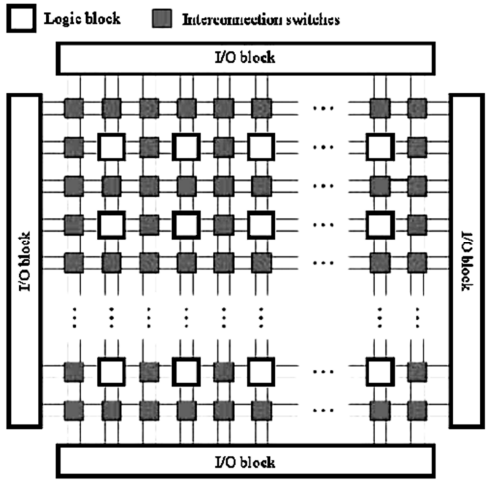
CPLDs

Example:

An I/O pin may be used as an input - the buffer must be disabled

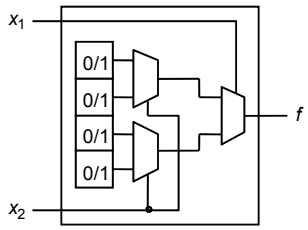


Field Programmable Gate Arrays (FPGA)



- An FPGA consists of an array of configurable logic blocks (CLBs).
- Interconnects are available between the CLBs.
- The CLBs are surrounded by I/O blocks.

Field Programmable Gate Arrays (FPGA)



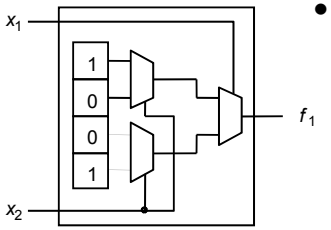
Configuration Logic Block (CLB):

- It often consists of an **LUT (lookup table)** that can generate any logic function — a truth-table based approach.
- Different from **AND-OR arrays** in SPLDs and CPLDs — an SOP Boolean-expression based approach.

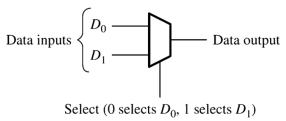
Field Programmable Gate Arrays (FPGA)

x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1

$f_1 = \bar{x}_1\bar{x}_2 + x_1x_2$

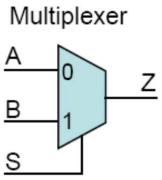


- An LUT contains storage cells, each stores an entry of the truth table.
- The outputs of such cells are multiplexed with the input variables as the data select.
- LUTs usually have 4-5 inputs in commercial FPGAs.



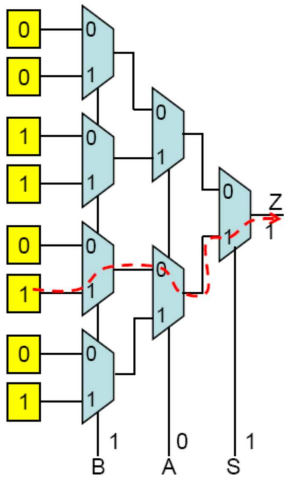
Field Programmable Gate Arrays (FPGA)

Example: an LUT to implement a multiplexer

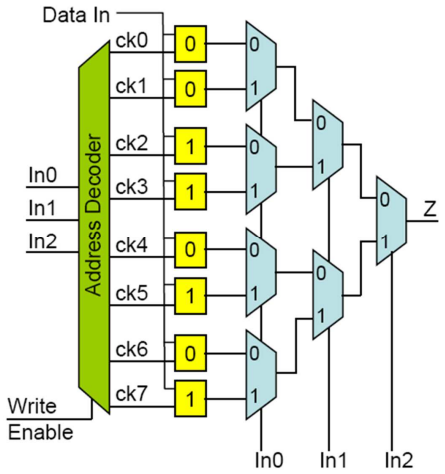


Truth table

S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



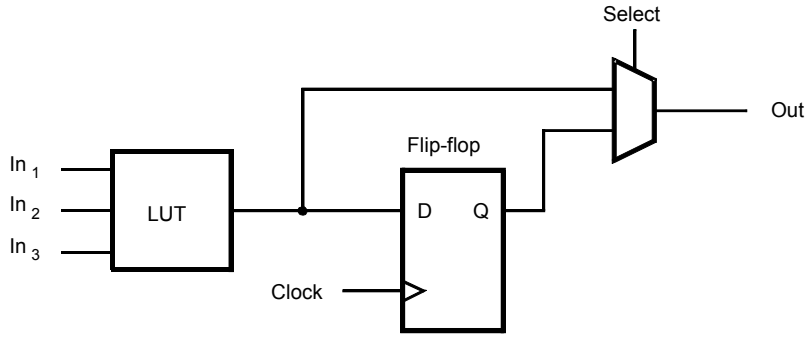
Field Programmable Gate Arrays (FPGA)



1. Normal LUT mode performs read operations.
2. Address decoder with write enable generates clock signals to latches for write operations.

Field Programmable Gate Arrays (FPGA)

Flip-flops may be included in an FPGA logic block to facilitate registered outputs.



Field Programmable Gate Arrays (FPGA)

A Programmed FPGA

- Each switch (X) in blue is turned on and each switch in black is turned off.
- The top row implements the function $f_1 = x_1x_2$ and $f_2 = \overline{x}_2x_3$.
- The bottom row produces $f = f_1 + f_2 = x_1x_2 + \overline{x}_2x_3$.

x_1	x_2	f_1
0	0	0
0	1	0
1	0	0
1	1	1

$f_1 = x_1x_2$

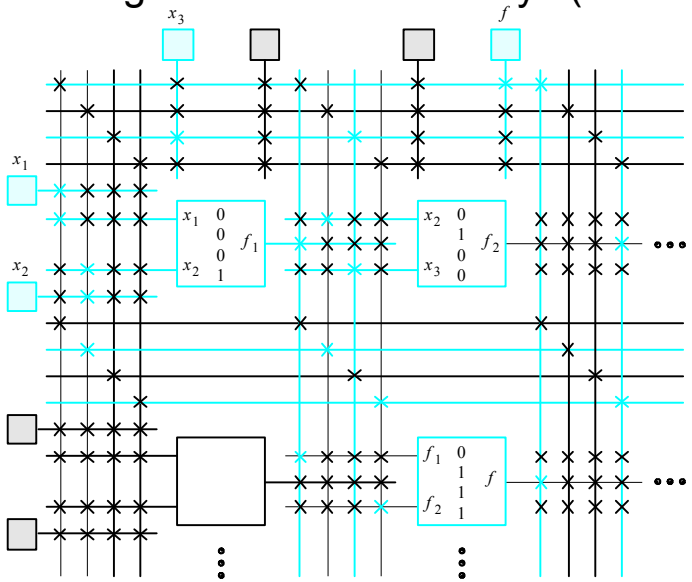
x_2	x_3	f_2
0	0	0
0	1	1
1	0	0
1	1	0

$f_2 = \overline{x}_2x_3$

f_1	f_2	f
0	0	0
0	1	1
1	0	1
1	1	1

$f_1 = f_1 + f_2$

Field Programmable Gate Arrays (FPGA)



Field Programmable Gate Arrays (FPGA)

Recent trend is to incorporate specialized cores:

1. RAMs – single-port, dual-port, FIFOs
   - 128 bits to over 36K bits per RAM
   - 4 to over 575 per FPGA
2. DSPs – 18x18-bit multiplier, 48-bit accumulator, etc.
   - up to 512 per FPGA
3. Microprocessors and/or microcontrollers
   - up to 2 per FPGA