EEE104 – Digital Electronics (I)

Lecture 15

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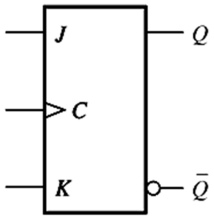
In This Session

- Counter Overview
- Asynchronous Counters

A Revision: J-K Flip-Flops



- When J = 1 and K = 1, the output will be toggled at the rising edge of the clock.

INPUTS			OUTPUTS		
J	K	CLK	Q	$\bar{Q}$	COMMENTS
0	0	↑	Q_0	$\bar{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	Q_0	Toggle

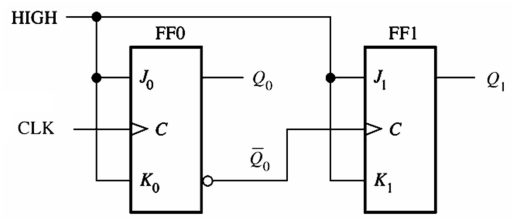
Counter Overview

A **counter** is a group of flip-flops connected together to perform counting operation.

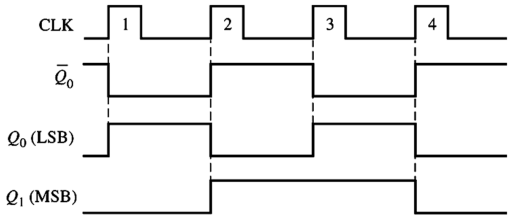
Categories:

- **Asynchronous counters**: each flip-flop is clocked by the output of the preceding flip-flop.
- **Synchronous counters**: all the flip-flops are clocked by the same clock input.

2-Bit Asynchronous Binary Counters

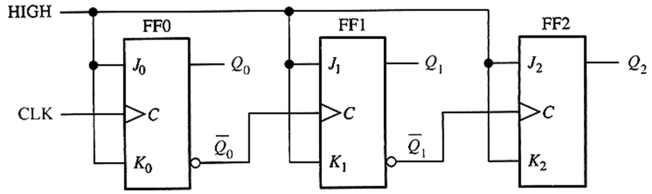


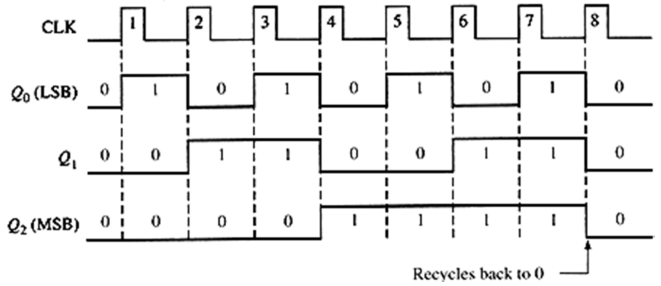
- J and K are HIGH for all flip-flops.
- FF1 is clocked by the $\overline{Q}_0$ output of FF0.



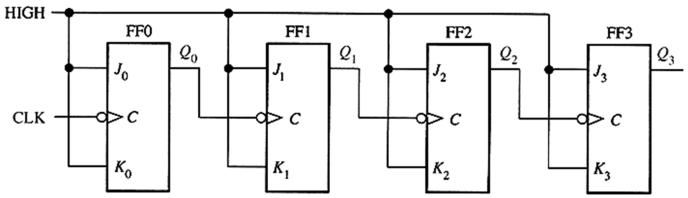
CLOCK PULSE	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0

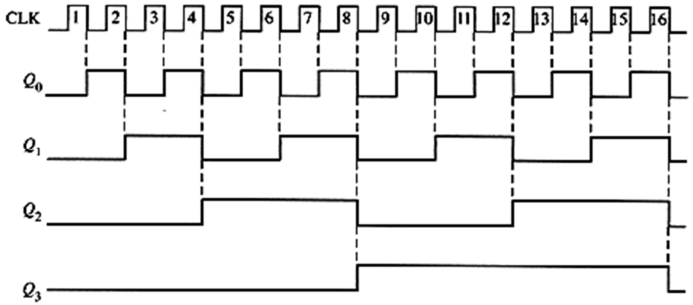
3-Bit Asynchronous Binary Counters





4-Bit Asynchronous Binary Counters

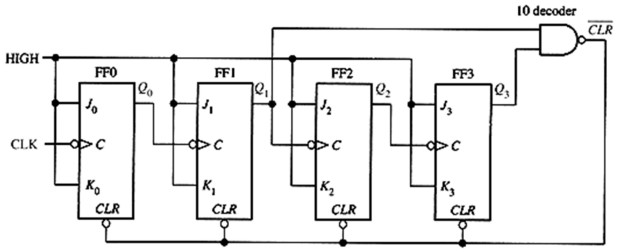




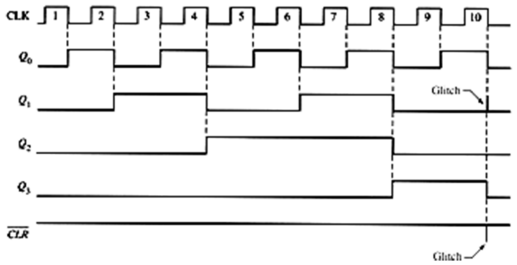
Asynchronous Decade Counters

- With n flip-flops, the maximum number of states of a counter is 2^n.
- A counter may be designed to go through less states or a **truncated** sequence, e.g. **decade counter** which counts from 0000 to 1001.
- The number of unique states that a counter will sequence through is called **modulus**.

Asynchronous Decade Counters

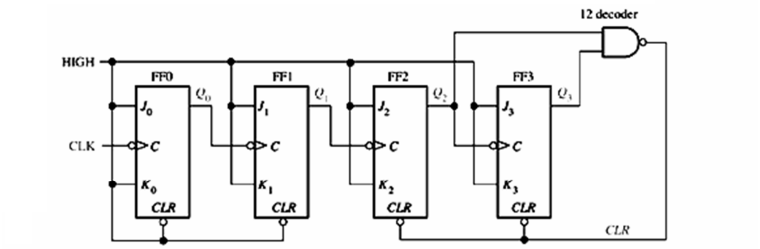


0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010

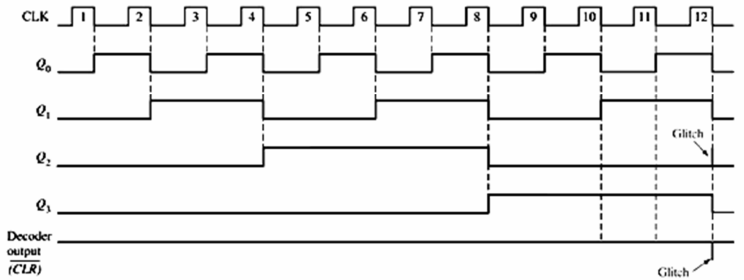


- Once state 1010 appears, the decoder will reset the counter.
- Only Q_1 and Q_3 used – Partial Decoding

Asynchronous Modulus-12 Counters

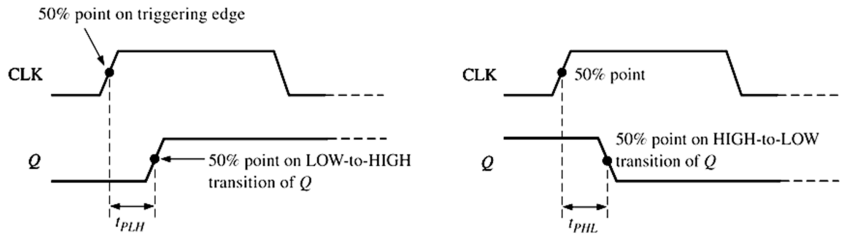


0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100



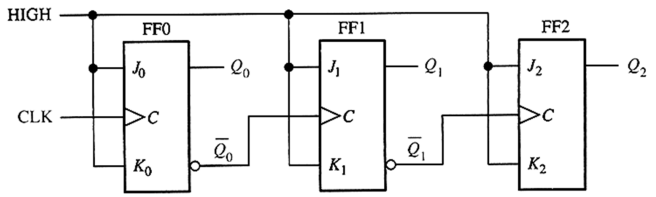
Cumulative Delay in Asynchronous Counters

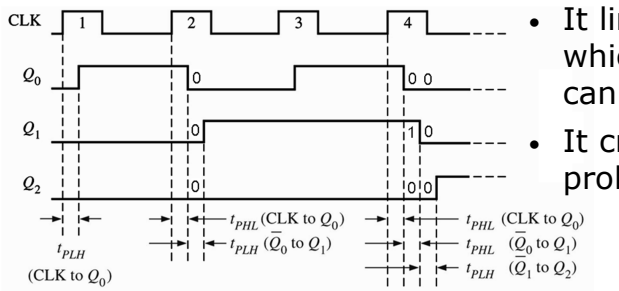
The **propagation delay time** is the time interval for the output to change after an input has been applied.



	74HC74A	74LS74A
t_{PHL}	17 ns	40 ns
t_{PLH}	17 ns	25 ns

Cumulative Delay in Asynchronous Counters



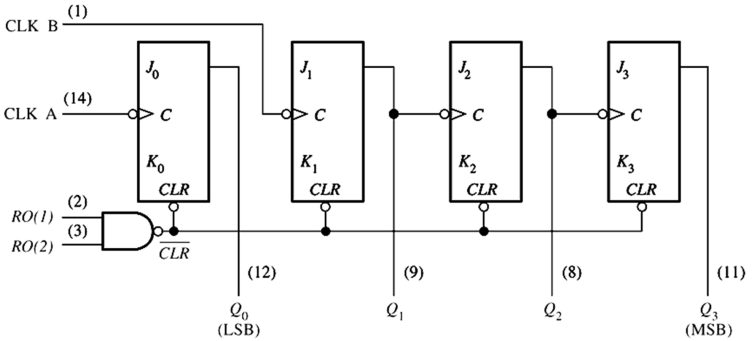


- It limits the rate at which the counter can be clocked.
- It creates decoding problems.

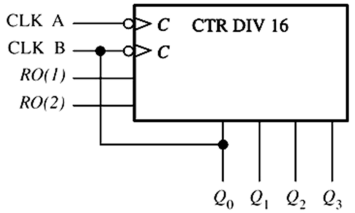
IC Asynchronous Counters

74LS93A

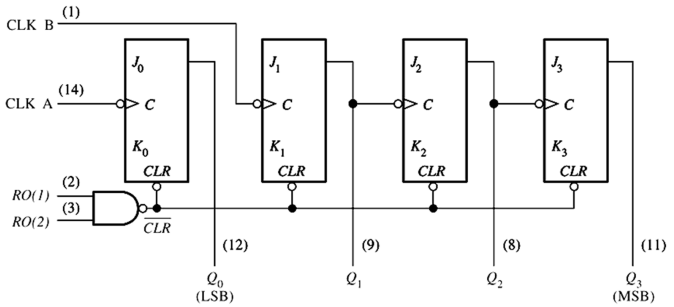
- Q_0 should be connected with CLK B when used as a counter.
- The NAND gate can be used as the decoder.



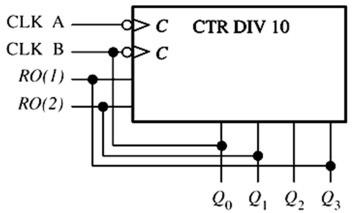
IC Asynchronous Counters



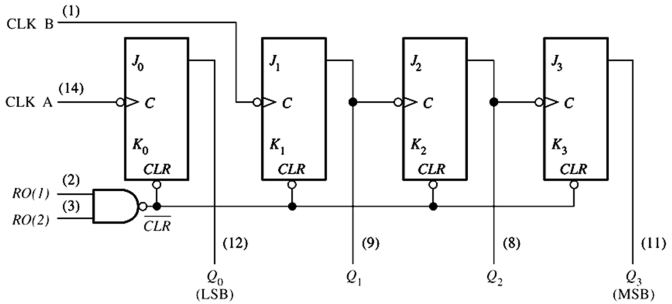
Modulus-16 counter



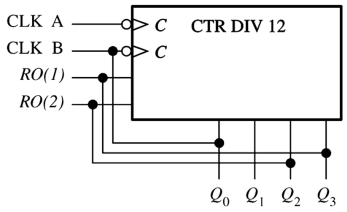
IC Asynchronous Counters



Decade counter



IC Asynchronous Counters



Modulus-12 counter