outline

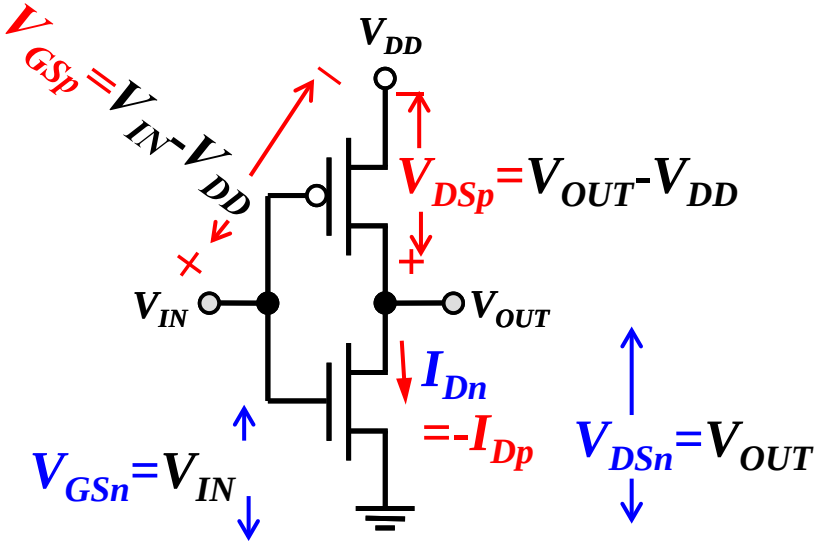
- Voltage transfer characteristic (VTC)
- nMOS inverters
  - Resistive load inverter
  - Saturated enhancement load inverter
  - Depletion load inverter
- **CMOS inverter**
  - CMOS VTC
  - Comparison of CMOS and MOS inverters
- Combinational CMOS logic gates (static)

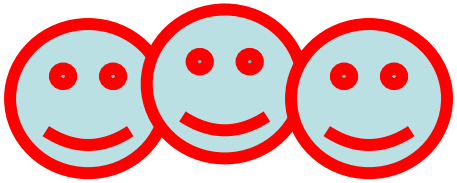
(material developed by Prof. Cezhou Zhao
with slides from other sources)

CMOS inverter

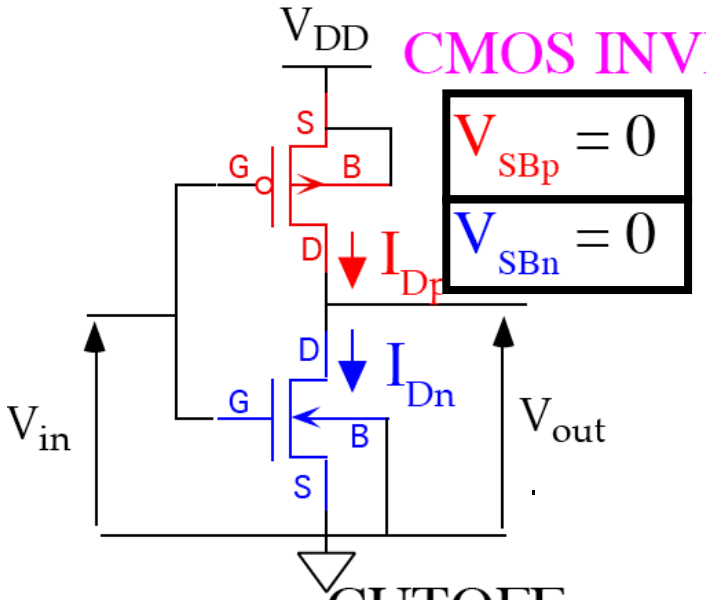
- Device parameters: V_{GSn}, V_{DSn}, I_{Dn}, V_{GSp}, V_{DSp}, and I_{Dp}
- Circuit parameters: V_{in}, V_{out}, and V_{DD}

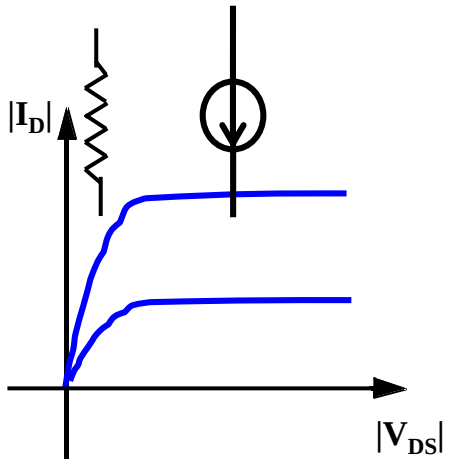
$$I_{Dp} = -I_{Dn}$$
$$V_{GSn} = V_{IN}$$
$$V_{GSp} = V_{IN} - V_{DD}$$
$$V_{DSn} = V_{OUT}$$
$$V_{DSp} = V_{OUT} - V_{DD}$$





CMOS INVERTER - STATIC CHARACTERISTICS

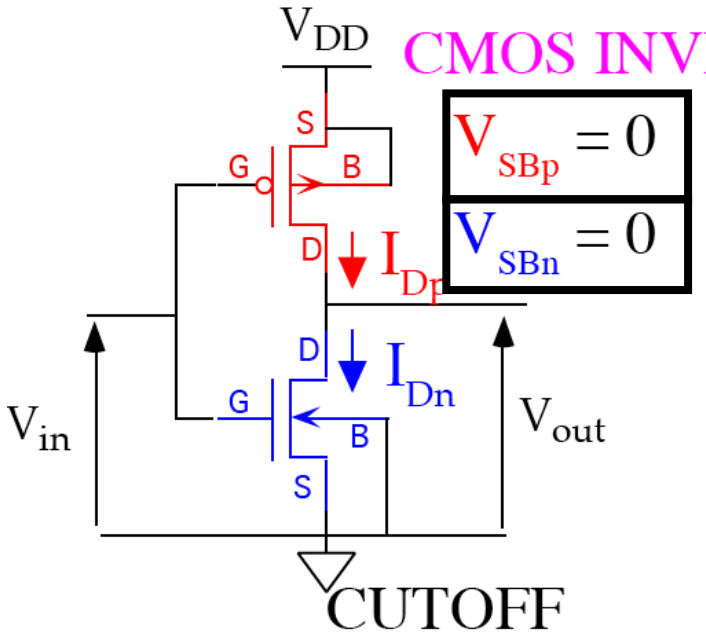




$|I_{Dp}| = |I_{Dn}|$
$V_{GSn} = V_{in}$
$V_{GSp} = V_{in} - V_{DD}$
$V_{DSn} = V_{out}$
$V_{DSp} = V_{out} - V_{DD}$

	CUTOFF	LINEAR	SATURATED
p-device	$V_{GSp} > V_{T0p}$	$V_{GSp} < V_{T0p}$ $V_{DSp} > V_{GSp} - V_{T0p}$	$V_{GSp} < V_{T0p}$ $V_{DSp} < V_{GSp} - V_{T0p}$
n-device	$V_{GSn} < V_{T0n}$	$V_{GSn} > V_{T0n}$ $V_{DSn} < V_{GSn} - V_{T0n}$	$V_{GSn} > V_{T0n}$ $V_{DSn} > V_{GSn} - V_{T0n}$

CMOS INVERTER - STATIC CHARACTERISTICS



$V_{SBp} = 0$

$V_{SBn} = 0$

$V_{out} = V_{in} - V_{T0n}$

$V_{out} = V_{in} - V_{T0p}$

$|I_{Dp}| = |I_{Dn}|$

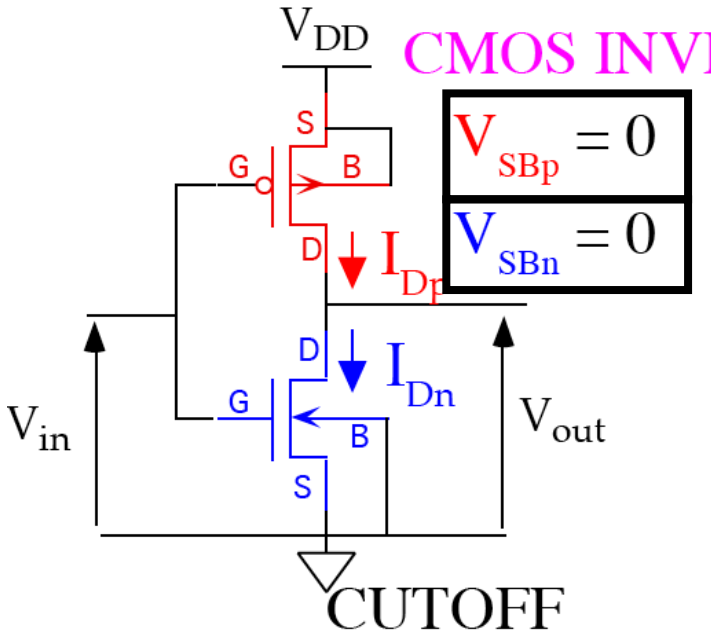
$V_{GSn} = V_{in}$

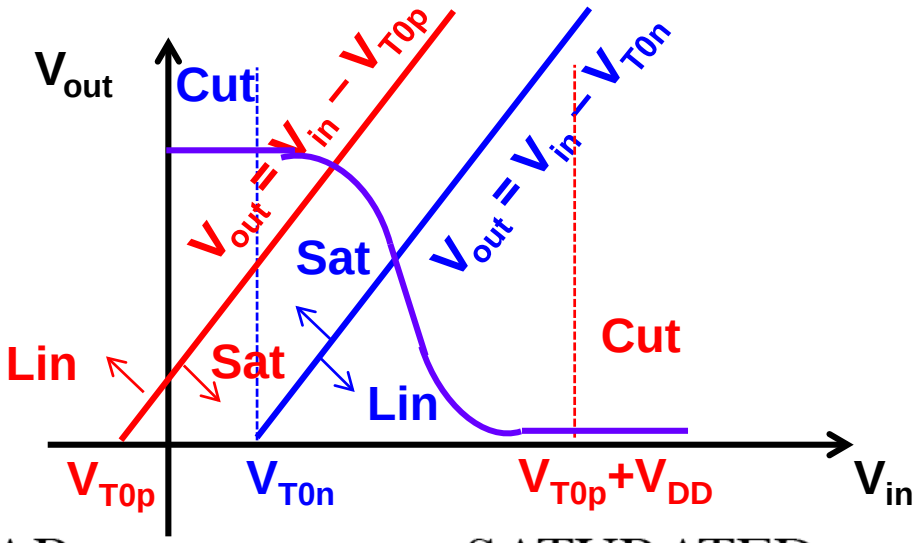
$V_{GSp} = V_{in} - V_{DD}$

$V_{DSn} = V_{out}$

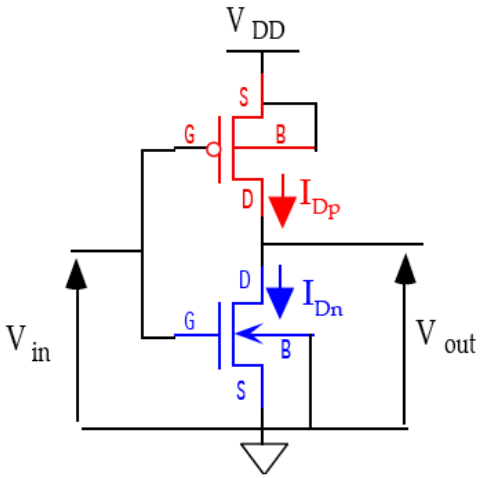
$V_{DSp} = V_{out} - V_{DD}$

	CUTOFF	LINEAR	SATURATED
p-device	$V_{GSp} > V_{T0p}$ $V_{in} > V_{T0p} + V_{DD}$	$V_{GSp} < V_{T0p}$ $V_{in} < V_{T0p} + V_{DD}$ $V_{DSp} > V_{GSp} - V_{T0p}$ $V_{out} > V_{in} - V_{T0p}$	$V_{GSp} < V_{T0p}$ $V_{in} < V_{T0p} + V_{DD}$ $V_{DSp} < V_{GSp} - V_{T0p}$ $V_{out} < V_{in} - V_{T0p}$
n-device	$V_{GSn} < V_{T0n}$ $V_{in} < V_{T0n}$	$V_{GSn} > V_{T0n}$ $V_{in} > V_{T0n}$ $V_{DSn} < V_{GSn} - V_{T0n}$ $V_{out} < V_{in} - V_{T0n}$	$V_{GSn} > V_{T0n}$ $V_{in} > V_{T0n}$ $V_{DSn} > V_{GSn} - V_{T0n}$ $V_{out} > V_{in} - V_{T0n}$

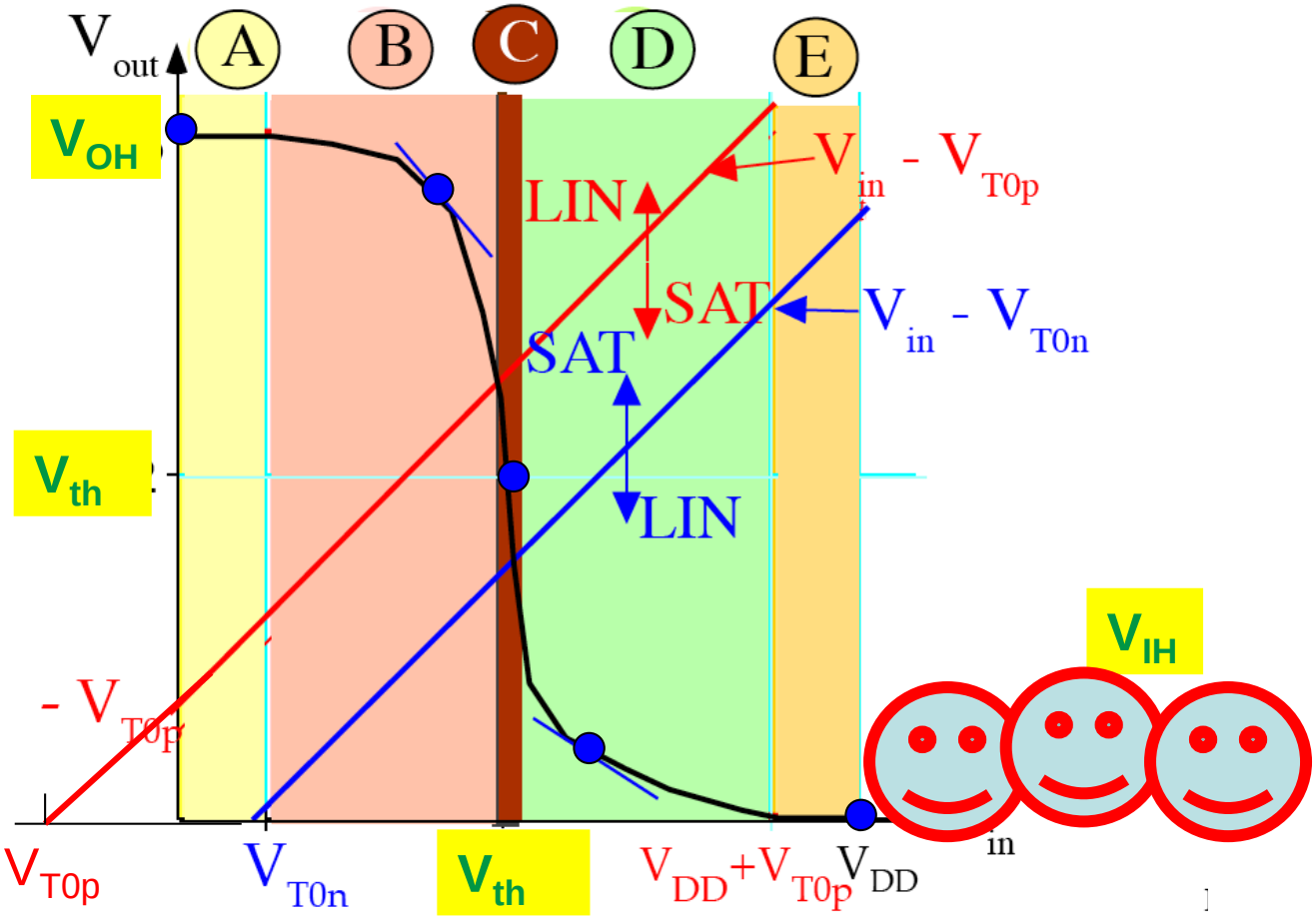




	CUTOFF	LINEAR	SATURATED
p-device	$V_{GSp} > V_{T0p}$ $V_{in} > V_{T0p} + V_{DD}$	$V_{GSp} < V_{T0p}$ $V_{in} < V_{T0p} + V_{DD}$ $V_{DSp} > V_{GSp} - V_{T0p}$ $V_{out} > V_{in} - V_{T0p}$	$V_{GSp} < V_{T0p}$ $V_{in} < V_{T0p} + V_{DD}$ $V_{DSp} < V_{GSp} - V_{T0p}$ $V_{out} < V_{in} - V_{T0p}$
n-device	$V_{GSn} < V_{T0n}$ $V_{in} < V_{T0n}$	$V_{GSn} > V_{T0n}$ $V_{in} > V_{T0n}$ $V_{DSn} < V_{GSn} - V_{T0n}$ $V_{out} < V_{in} - V_{T0n}$	$V_{GSn} > V_{T0n}$ $V_{in} > V_{T0n}$ $V_{DSn} > V_{GSn} - V_{T0n}$ $V_{out} > V_{in} - V_{T0n}$



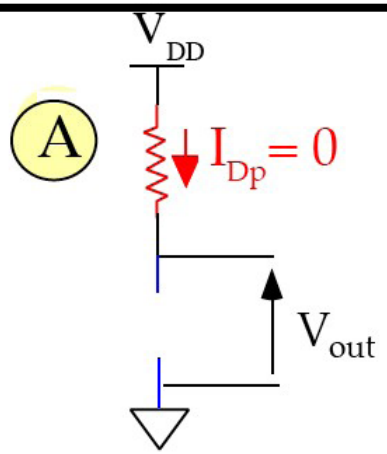
$|I_{Dp}| = |I_{Dn}|$
$V_{GSn} = V_{in}$
$V_{GSp} = V_{in} - V_{DD}$
$V_{DSn} = V_{out}$
$V_{DSp} = V_{out} - V_{DD}$



V_{OH}
V_{IL}
V_{th}
V_{th}
V_{IH}
V_{OL}

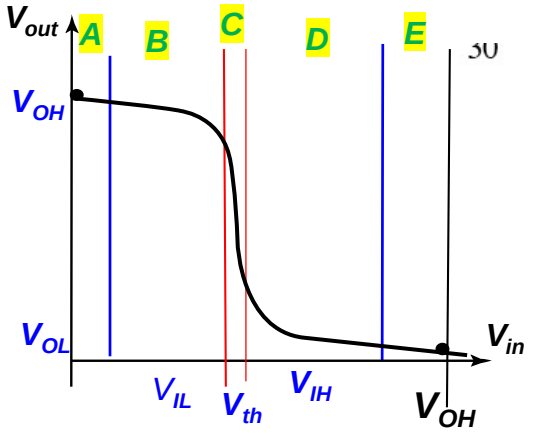
CALCULATE V_{OH}

$$V_{Out} = V_{OH} = V_{DD}$$



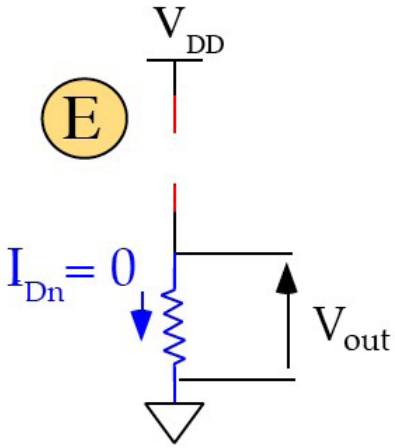
$$I_{Dp} = I_{Dn} = 0$$

$$I_{Dp} = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p [2(V_{GSp} - V_{T0p})V_{DSp} - V_{DSp}^2]$$



CALCULATE V_{OL}

$$V_{Out} = V_{OL} = 0$$



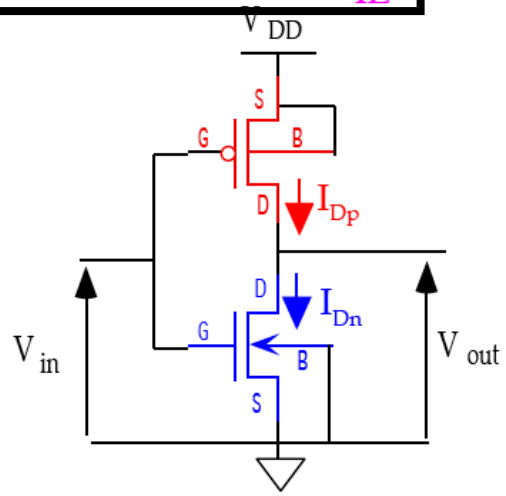
$$I_{Dp} = I_{Dn} = 0$$

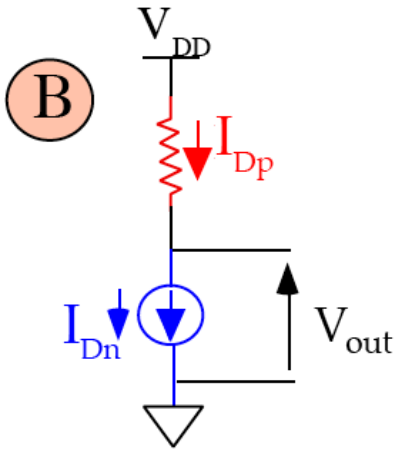
$$I_{Dn} = \frac{k_n'}{2}\left(\frac{W}{L}\right)_n [2(V_{GSn} - V_{T0n})V_{DSn} - V_{DSn}^2]$$

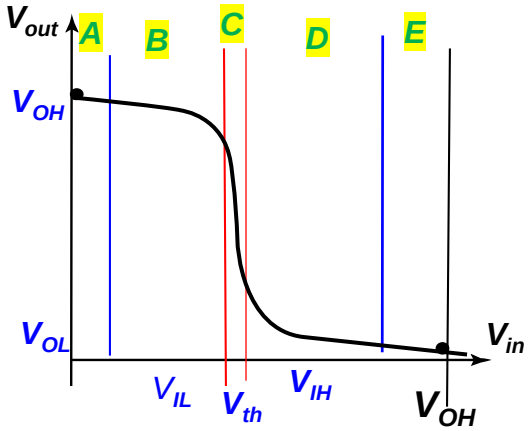
$k'_p = C_{ox}\mu_p$

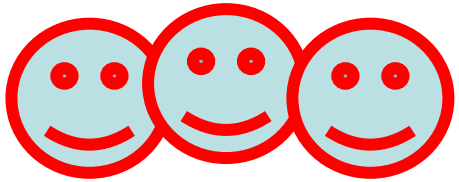
$k'_n = C_{ox}\mu_n$

CALCULATE V_{IL}







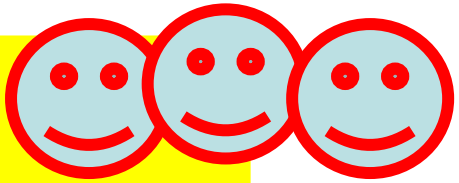


$$I_{Dp} = I_{Dn}$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n \left(V_{GSn} - V_{T0\,n}\right)^2 = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p \left[2\left(V_{GSp} - V_{T0\,p}\right)V_{DSp} - V_{DSp}^2\right]$$

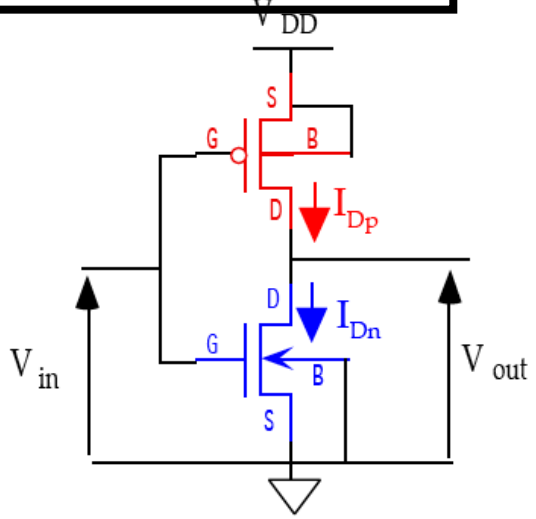
$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n (V_{in} - V_{T0n})^2$$

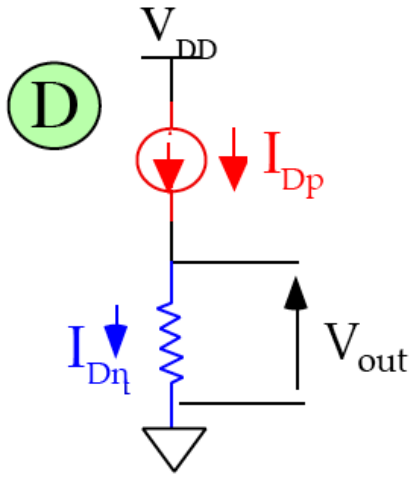
$$= \frac{k_p'}{2}\left(\frac{W}{L}\right)_p \left[2(V_{in} - V_{DD} - V_{T0p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right]$$

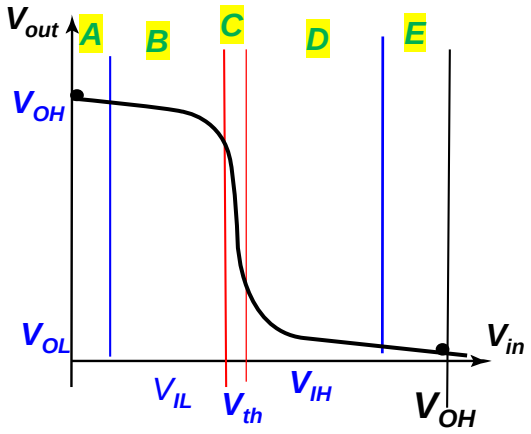


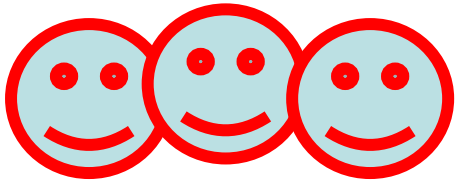
(5.59)

CALCULATE V_{IH}









$$I_{Dp} = I_{Dn}$$

$$\frac{k'_n}{2}\left(\frac{W}{L}\right)_n\left[2(V_{GSn}-V_{T0n})V_{DSn}-V_{DSn}^2\right]=\frac{k'_p}{2}\left(\frac{W}{L}\right)_p\left(V_{GSp}-V_{T0p}\right)^2$$

$$V_{GSn} = V_{in},\ V_{DSn} = V_{out},\ V_{GSp} = V_{in} - V_{DD}$$

$$\frac{k'_n}{2}\left(\frac{W}{L}\right)_n\left[2(V_{in}-V_{T0n})V_{out}-V_{out}^2\right]=\frac{k'_p}{2}\left(\frac{W}{L}\right)_p\left(V_{in}-V_{DD}-V_{T0p}\right)^2$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n\left[2(V_{in}-V_{T0\,n})V_{out}-V_{out}^2\right]=\frac{k_p'}{2}\left(\frac{W}{L}\right)_p\left(V_{in}-V_{DD}-V_{T0\,p}\right)^2 \quad (5.64)$$

DIFFERENTIATING wrt V_{in}

$$k_n'\left(\frac{W}{L}\right)_n\left[(V_{in}-V_{T0\,n})\frac{dV_{out}}{dV_{in}}+V_{out}-V_{out}\frac{dV_{out}}{dV_{in}}\right]=k_p'\left(\frac{W}{L}\right)_p\left(V_{in}-V_{DD}-V_{T0\,p}\right)$$

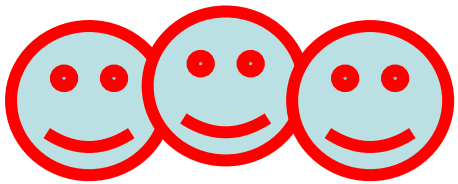
(V_{IH} above V_{in}; (-1) above $\frac{dV_{out}}{dV_{in}}$; (-1) above the second $\frac{dV_{out}}{dV_{in}}$; V_{IH} above V_{in})

$$k_n'\left(\frac{W}{L}\right)_n\left[-V_{IH}+V_{T0n}+2V_{out}\right]=k_p'\left(\frac{W}{L}\right)_p\left(V_{IH}-V_{DD}-V_{T0p}\right)$$

SOLVING FOR V_{IH}

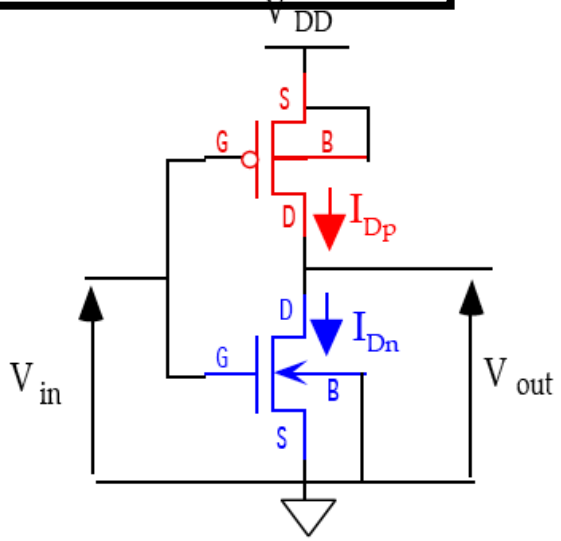
$$V_{IH}=\frac{V_{DD}+V_{T0\,p}+k_R(2V_{out}+V_{T0\,n})}{1+k_R} \quad (5.67)$$

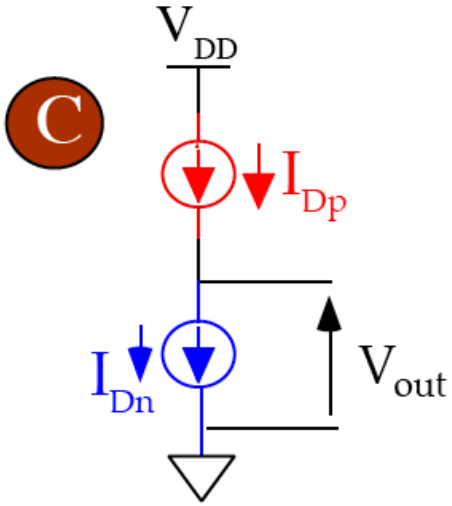
where $$k_R=\frac{k_n'(W/L)_n}{k_p'(W/L)_p}$$

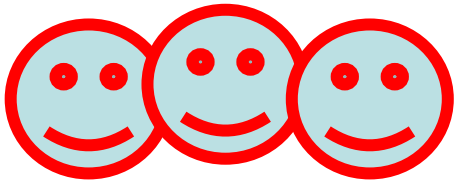


SOLVE Eqs. (5.64) and (5.67) for V_{out} and V_{IH}

CALCULATE V_{th}







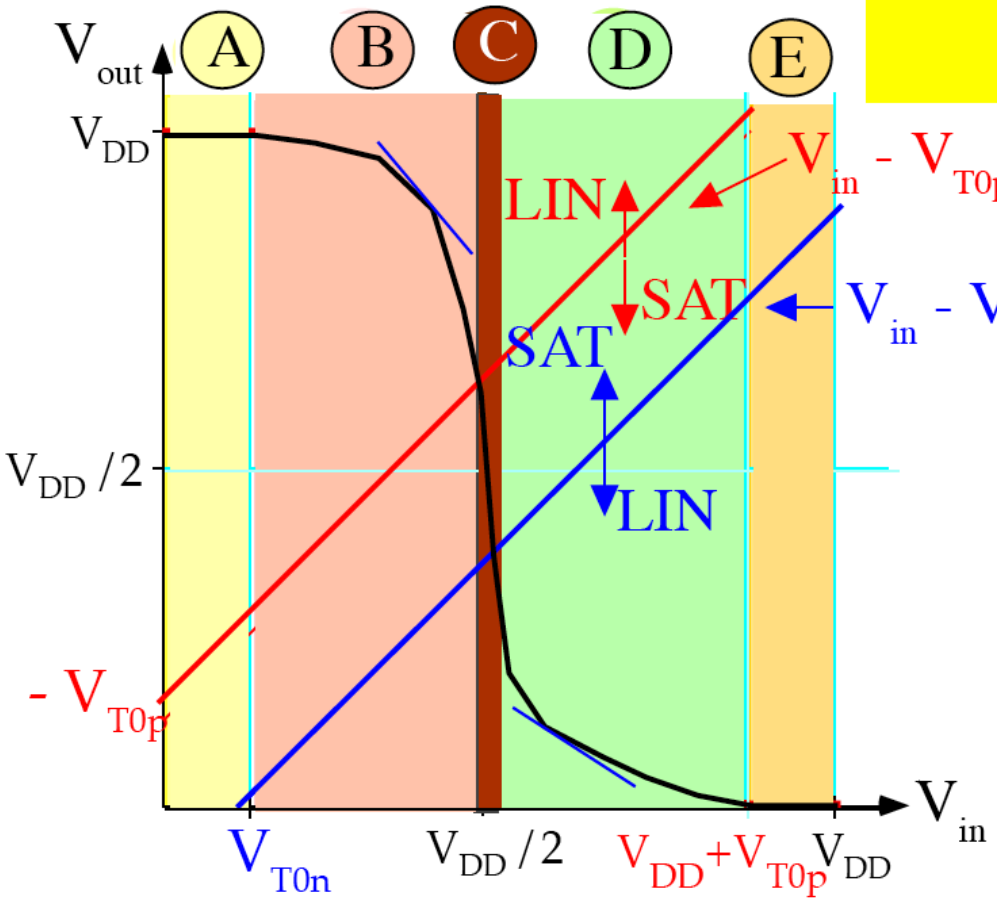
$$I_{Dp} = I_{Dn}$$

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n \left(V_{GSn} - V_{T0\,n}\right)^2 = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p \left(V_{GSp} - V_{T0\,p}\right)^2$$

$$\frac{k'_n}{2}\left(\frac{W}{L}\right)_n\left(V_{in}-V_{T0\,n}\right)^2=\frac{k'_p}{2}\left(\frac{W}{L}\right)_p\left(V_{in}-V_{DD}-V_{T0\,p}\right)^2$$

SOLVING for $V_{th}=V_{in}$

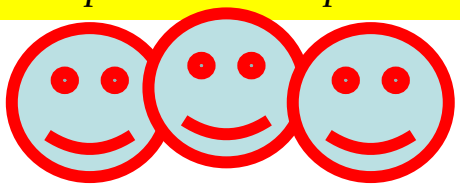
$$V_{in}=V_{th}=\frac{V_{T0\,n}+\sqrt{\frac{1}{k_R}}\left(V_{DD}+V_{T0\,p}\right)}{\left(1+\sqrt{\frac{1}{k_R}}\right)}$$



NOTE THAT

$$V_{th}=V_{in}=V_{out}$$

$$k_R=\frac{k'_n\left(W/L\right)_n}{k'_p\left(W/L\right)_p}=\frac{k_n}{k_p}$$



DESIGN OF CMOS INVERTERS

$$V_{th} = \frac{V_{T0n} + \sqrt{\frac{1}{k_R}}\left(V_{DD} + V_{T0p}\right)}{\left(1 + \sqrt{\frac{1}{k_R}}\right)}$$

SOLVING FOR k_R

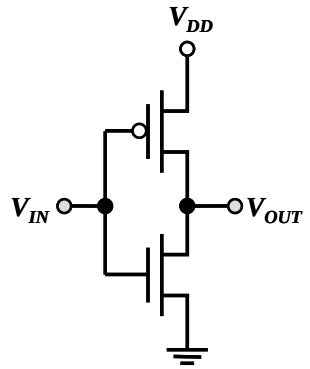
$$k_R = \left(\frac{V_{DD} + V_{T0p} - V_{th}}{V_{th} - V_{T0n}}\right)^2$$

FOR IDEAL INVERTER $V_{th} = \frac{1}{2}V_{DD}$

$$(k_R)_{ideal} = \left(\frac{0.5V_{DD} + V_{T0p}}{0.5V_{DD} - V_{T0n}}\right)^2$$

Recall

Threshold Voltage



- For p-type Si:

$$V_{T0n} = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\phi_F)}}{C_{ox}}$$

- For n-type Si:

$$V_{T0p} = V_{FB} + 2\phi_F - \frac{\sqrt{2qN_D\varepsilon_{Si}|2\phi_F|}}{C_{ox}}$$

1

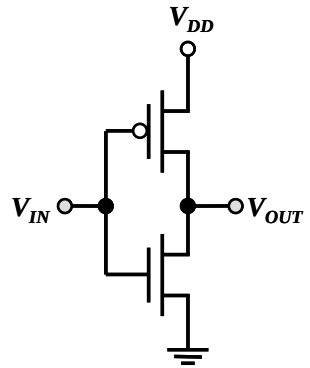
$$k_R = \frac{k'_n (W/L)_n}{k'_p (W/L)_p} = \frac{k_n}{k_p} = \frac{C_{ox}\mu_n (W/L)_n}{C_{ox}\mu_p (W/L)_p} = \frac{\mu_n (W/L)_n}{\mu_p (W/L)_p}$$

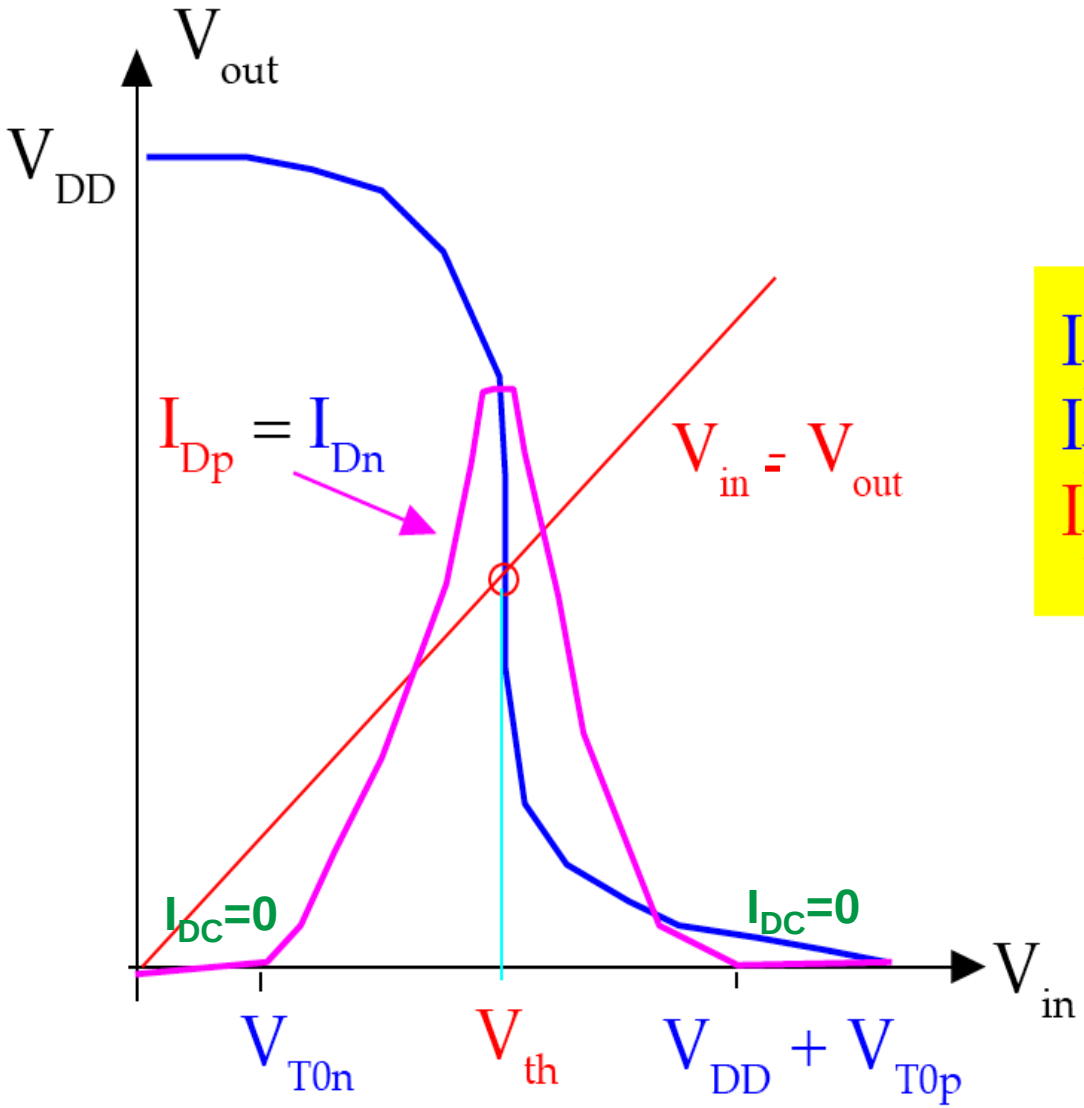
FOR SYMMETRIC INVERTER $V_{T0} = V_{T0n} = -V_{T0p}$ $\left(k_R\right)_{\text{inverter}}^{\text{symmetric}} = 1$

$$\frac{(W/L)_n}{(W/L)_p} = \frac{\mu_p}{\mu_n}$$

$k_n / k_p = 1$

POWER SUPPLY CURRENT VS V_{IN}

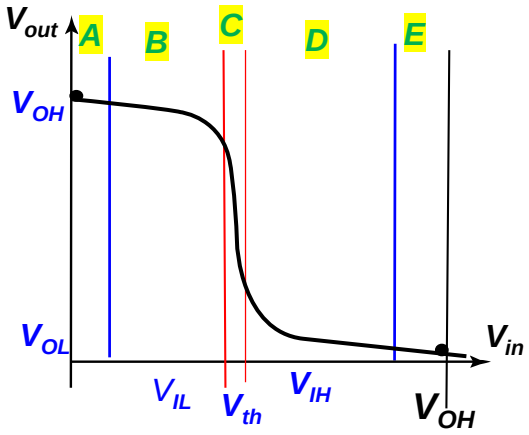




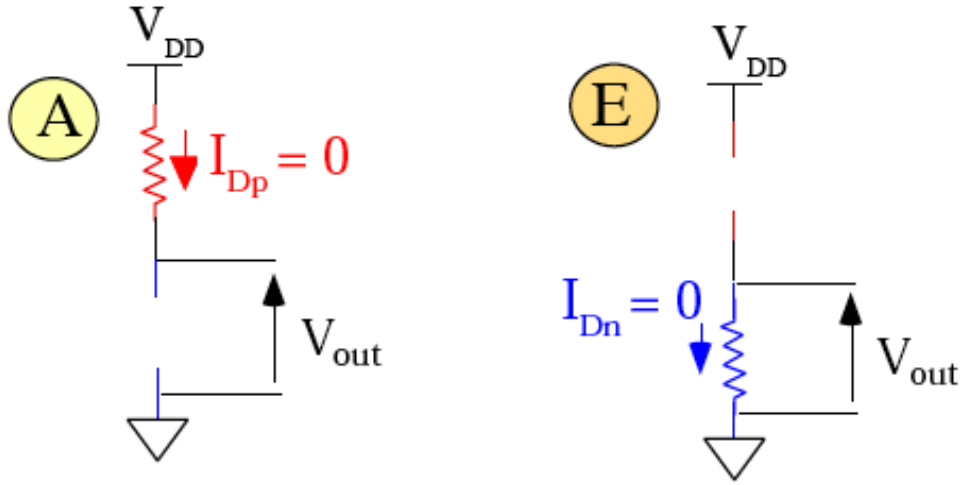
$I_D = 0,\ V_{in} < V_{T0n}$

$I_D = 0,\ V_{in} > V_{DD} + V_{T0p}$

$I_D = MAX,\ V_{in} = V_{th}$



POWER DISSIPATION CONSIDERATIONS



$$P_{DC} = \frac{V_{DD}}{2}\left[I_{DC}(V_{in} = "0") + I_{DC}(V_{in} = "1")\right] = \frac{P(V_{in} = 0) + P(V_{in} = 1)}{2}$$

WHEN $V_{in} = V_{OL}$: $\quad I_D = 0 \Rightarrow P(V_{in} = 0) = 0$

WHEN $V_{in} = V_{OH}$: $\quad I_D = 0 \Rightarrow P(V_{in} = 1) = 0$

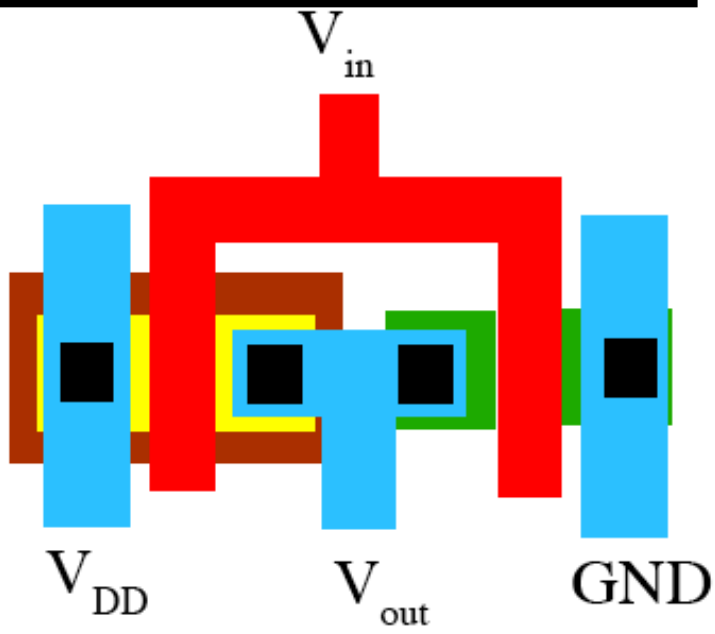
$$P_{DC} = 0$$

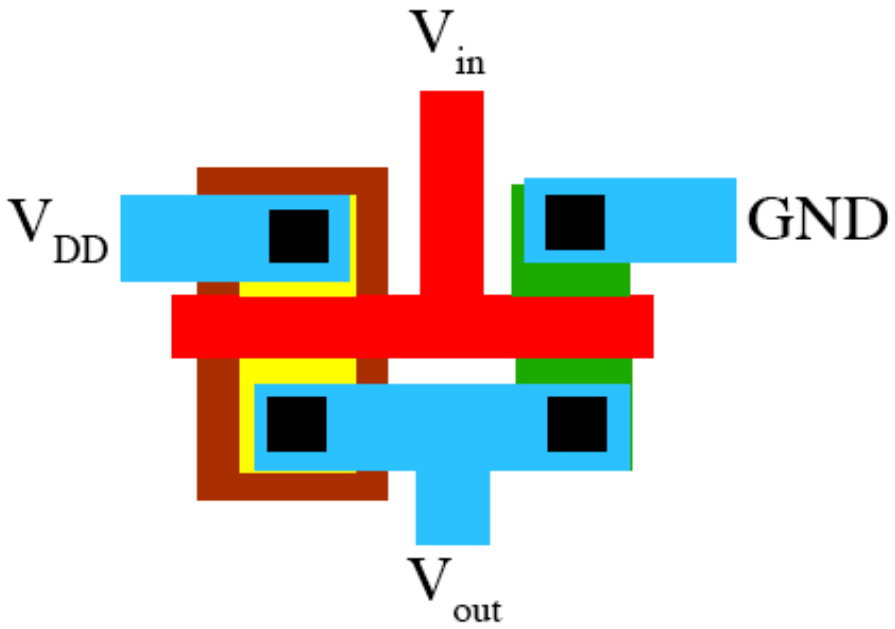
P_{DC} ≈ "0" because of subthreshold leakage

DIE AREA CONSIDERATIONS

COLOR LEGEND

- n-Well
- n^+
- Polysilicon
- p^+
- Metal 1
- Contact/via

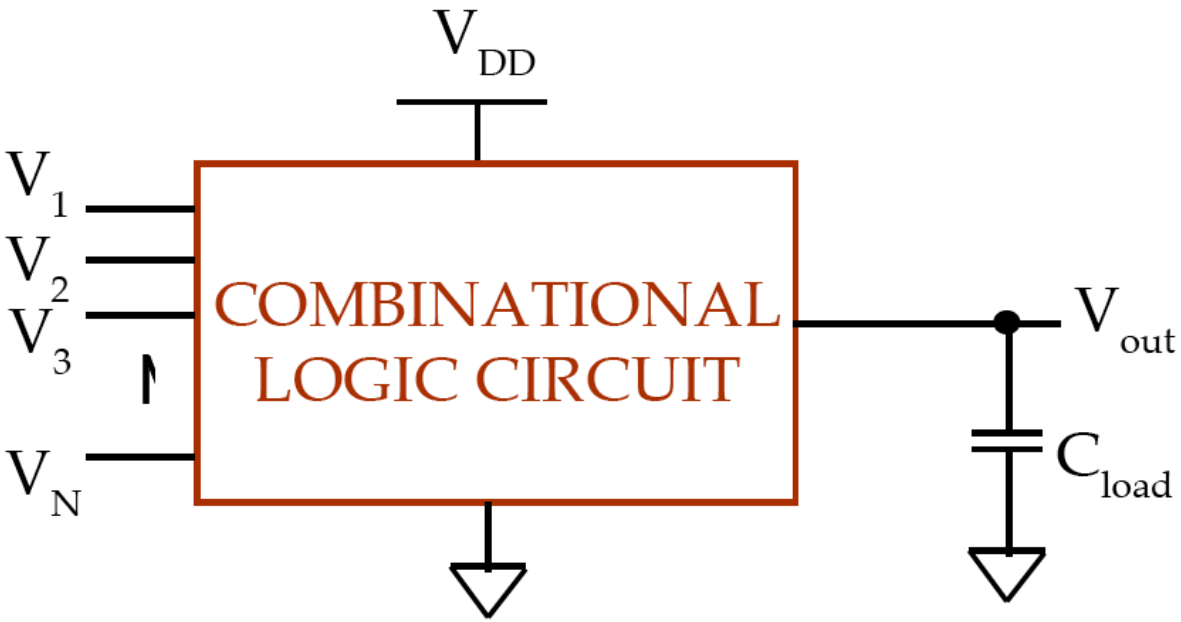




Smaller Area Layout

outline

- Voltage transfer characteristic (VTC)
- nMOS inverters
  - Resistive load inverter
  - Saturated enhancement load inverter
  - Depletion load inverter
- CMOS inverter
  - CMOS VTC
  - Comparison of CMOS and MOS inverters
- **Combinational CMOS logic gates (static)**
- Ratioed Logic

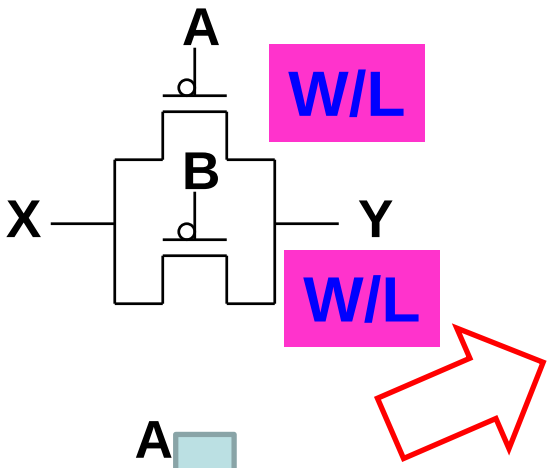


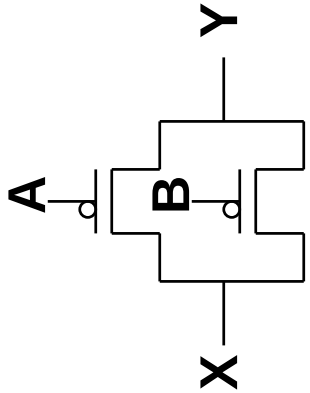
V_{out} is Boolean function of inputs , V_1, V_2, V_3, ..., V_N.

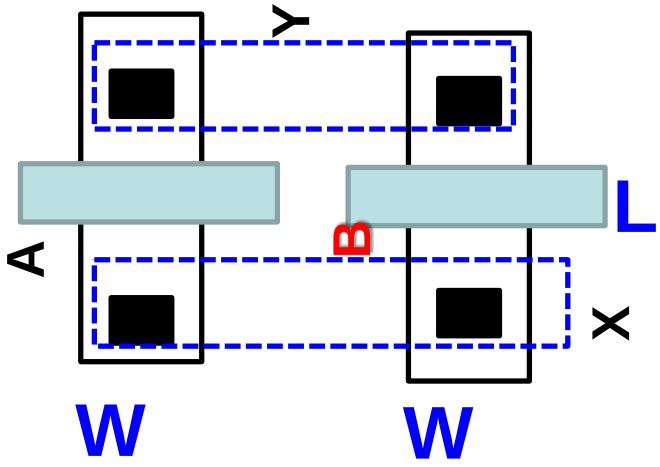
"1" => V_{DD}

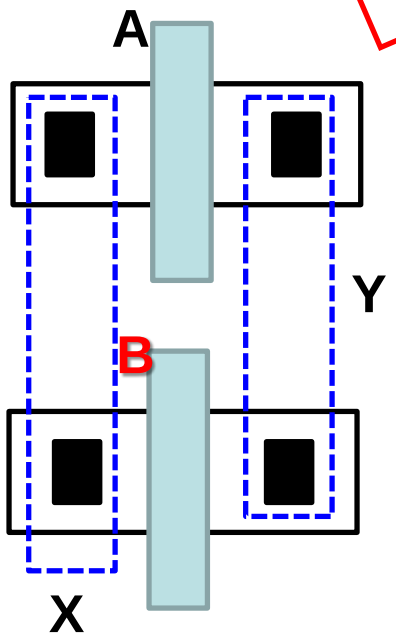
"0" => 0

MOS Transistors in Series/Parallel Connection

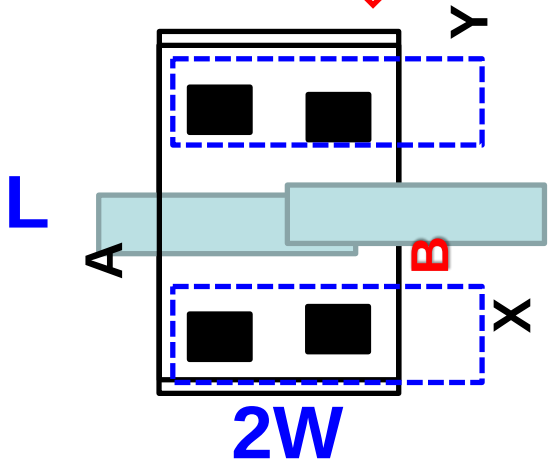


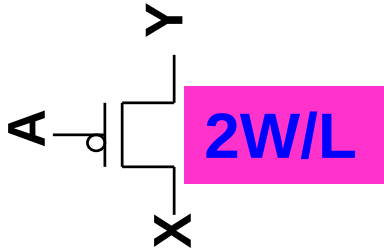




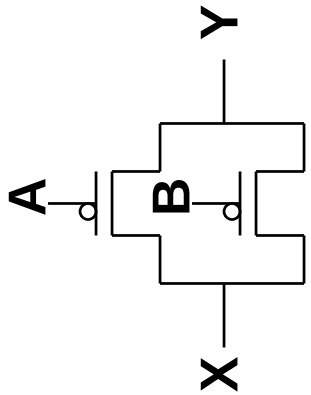


If $V_A = V_B$





MOS Transistors in Series/Parallel Connection

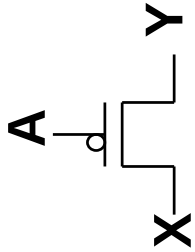


W/L W/L

$k_{n,eq} = 2k_{n,d}$

If $V_A = V_B$

Equivalent Circuit

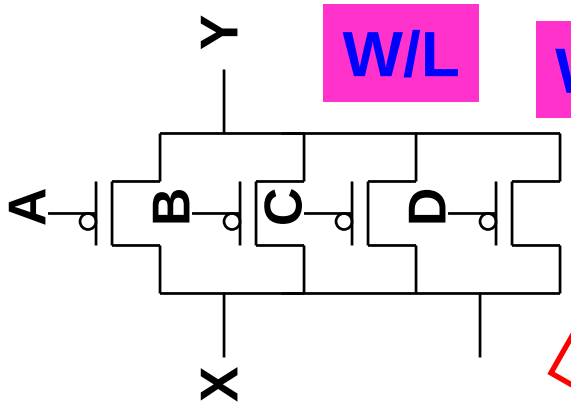


2W/L

$k_{n,d} = C_{ox}\mu_n(W/L)$

$k_{n,eq} = C_{ox}\mu_n(2W/L)$

MOS Transistors in Series/Parallel Connection

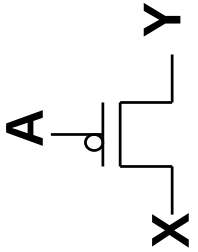


W/L W/L W/L W/L

$k_{n,eq} = 4k_{n,d}$

If $V_A = V_B = V_C = V_D$

Equivalent Circuit

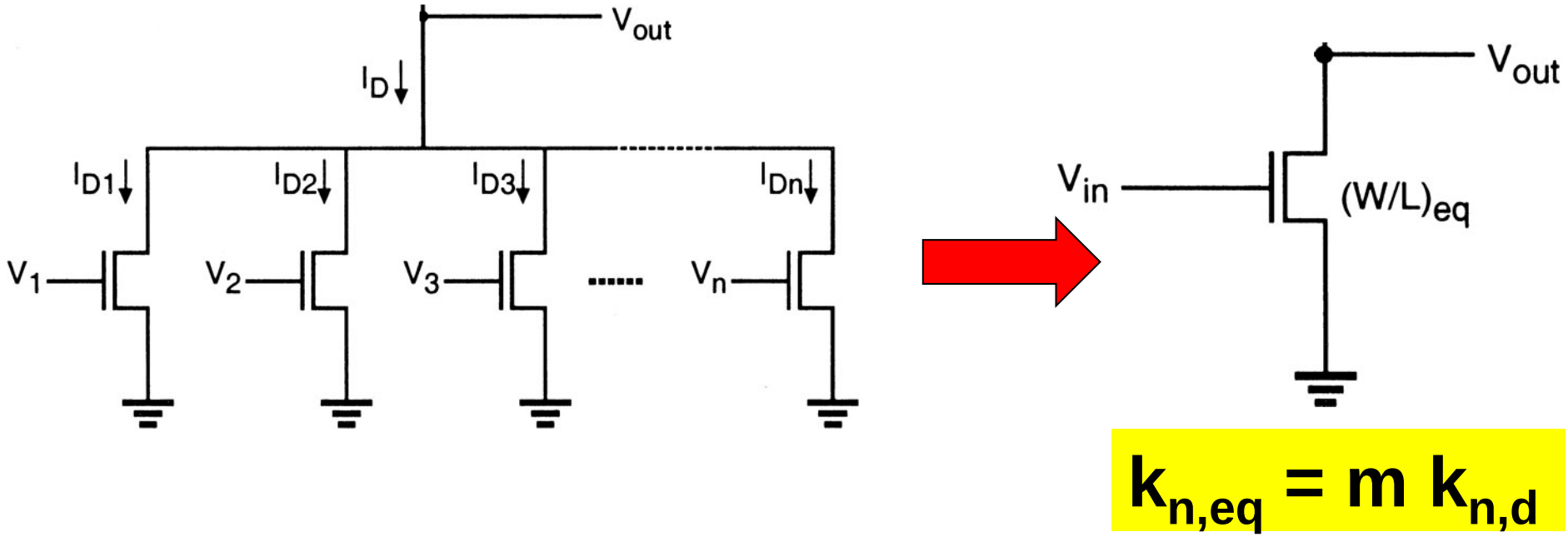


4W/L

$k_{n,d} = C_{ox}\mu_n(W/L)$

$k_{n,eq} = C_{ox}\mu_n(4W/L)$

$k_{n,d} = C_{ox}\mu_n(W/L)$ $k_{n,eq} = C_{ox}\mu_n(mW/L)$

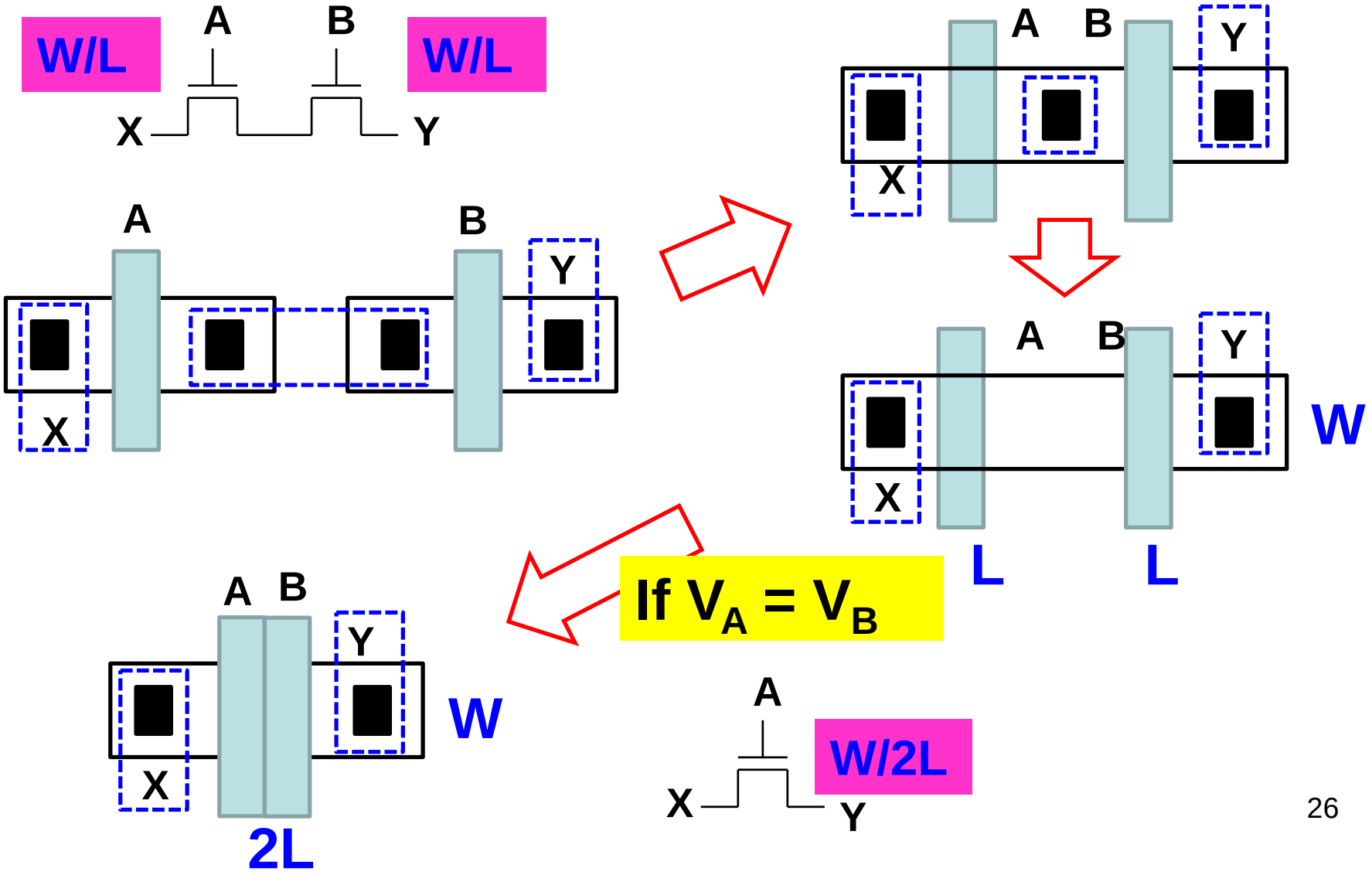


$k_{n,eq} = m\, k_{n,d}$

$$\left(\frac{W}{L}\right)_{eq} = \sum_{m(ON)} \left(\frac{W}{L}\right)_m = \frac{mW}{L},$$ if (1) the gates of m transistors have the same potential.

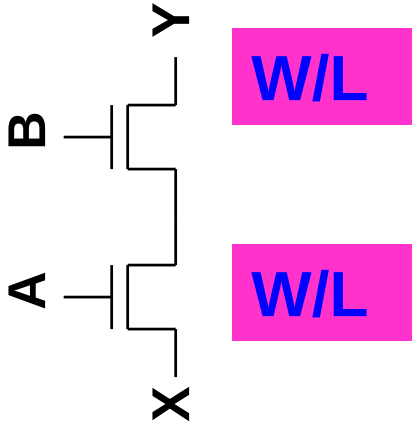
and (2) the (n - m) transistors are cut off.

MOS Transistors in Series/Parallel Connection



MOS Transistors in Series/Parallel Connection

$k_{n,eq} = k_{n,d}/2$

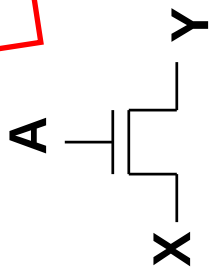


W/L

W/L

If $V_A = V_B$

$k_{n,d} = C_{ox}\mu_n(W/L)$

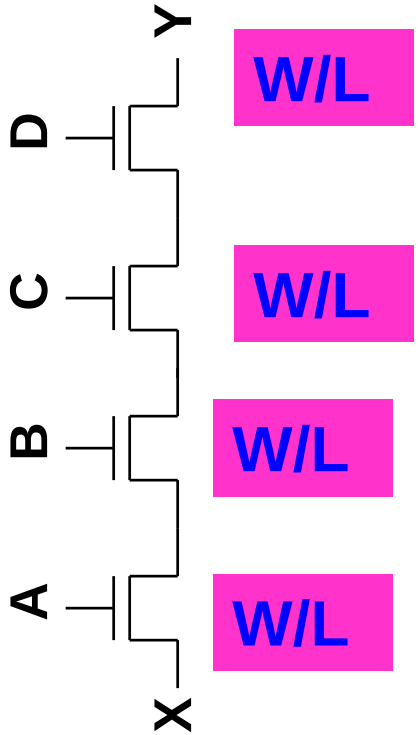


W/(2L)

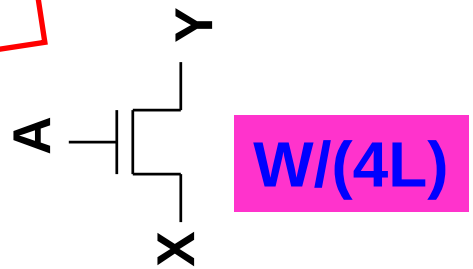
$k_{n,eq} = C_{ox}\mu_n W/(2L)$

MOS Transistors in Series/Parallel Connection

$k_{n,eq} = k_{n,d}/4$



If $V_A = V_B = V_C = V_D$



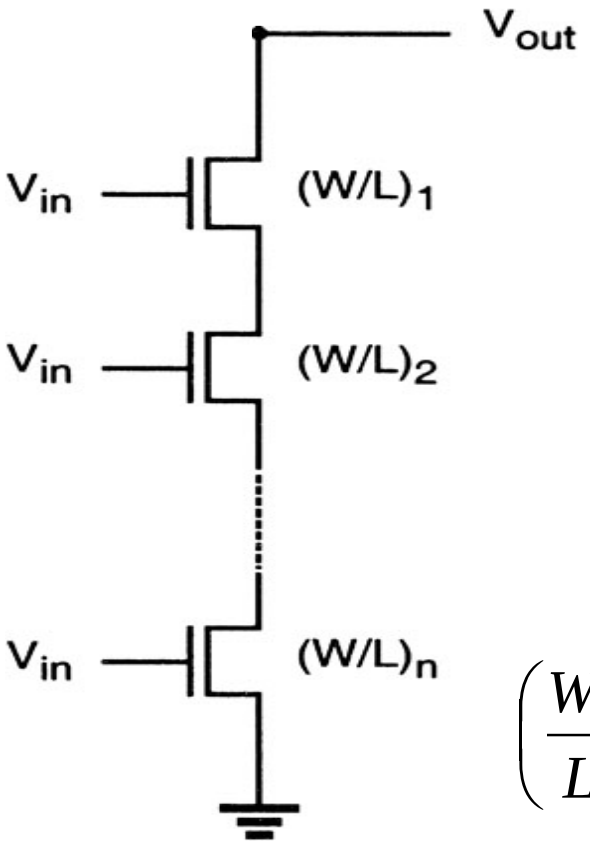
$k_{n,d} = C_{ox}\mu_n(W/L)$

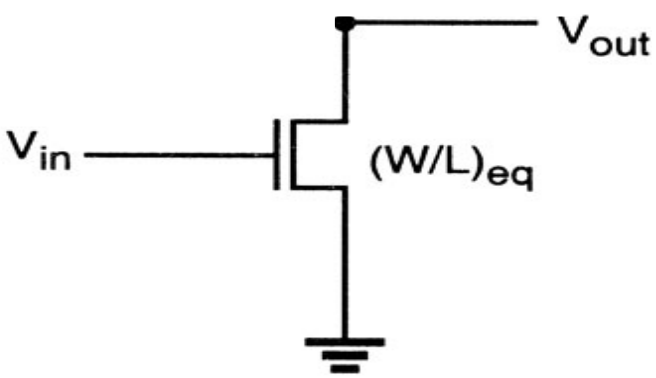
$k_{n,eq} = C_{ox}\mu_n W/(4L)$

$k_{n,d} = C_{ox}\mu_n(W/L)$

$k_{n,eq} = C_{ox}\mu_n W/(nL)$

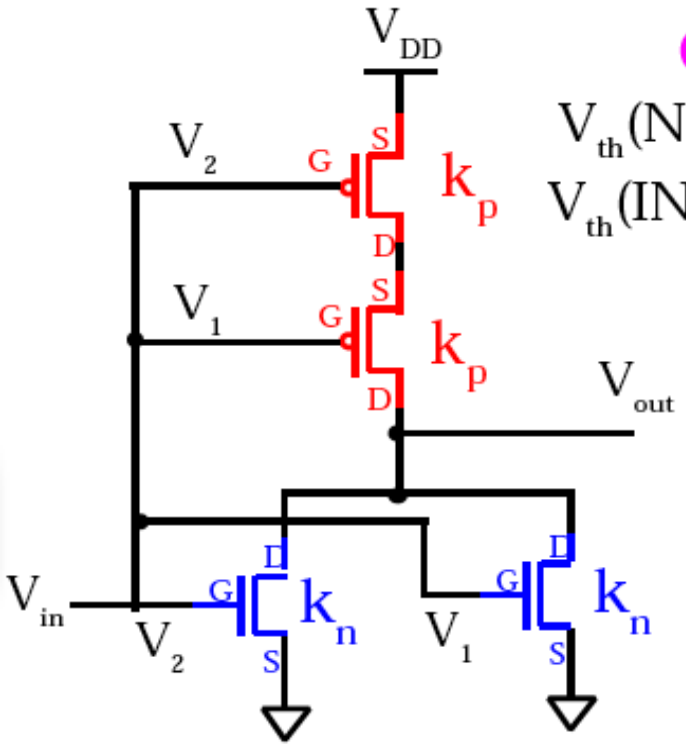
$k_{n,eq} = k_{n,d}/n$





$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{\sum_{n(ON)} \frac{1}{\left(\frac{W}{L}\right)_n}} = \left(\frac{W}{nL}\right)$$

CMOS NR2



$$V_{th}(NR2) => V_1 = V_2 = V_{out}$$

$$V_{th}(INV) = V_{in} = V_{out}$$

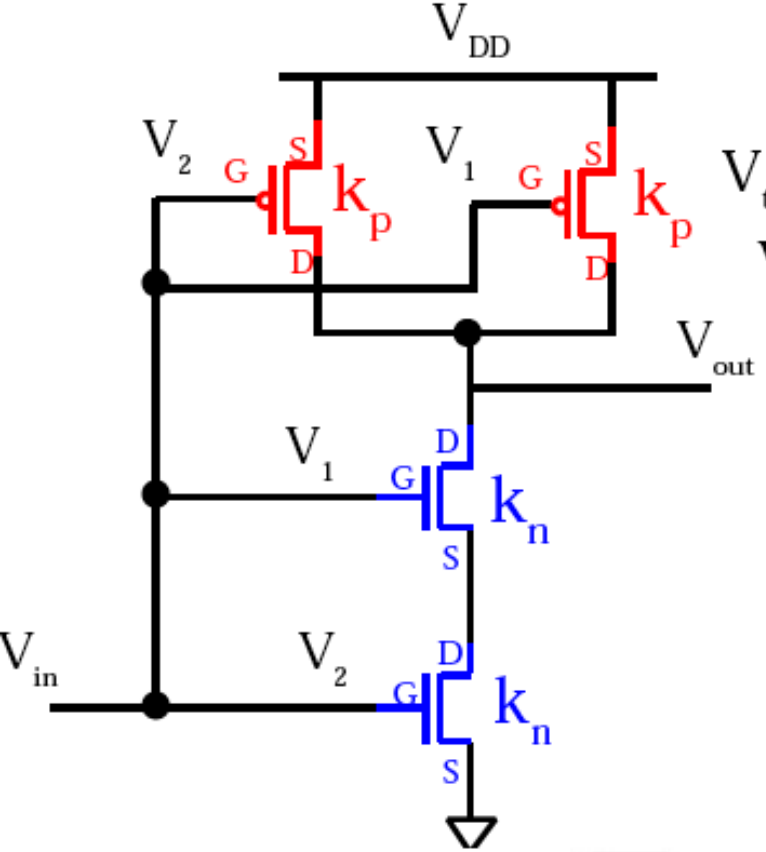
$$V_{th}(NOR2) = \frac{V_{Tn} + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}\left(V_{DD} + V_{Tp}\right)}{1 + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}}$$

Symmetrical EQUIV INV

$k_R = 1$

$k_p = 2^2 k_n$

$$2^2 \mu_n \left(\frac{W}{L}\right)_n = \mu_p \left(\frac{W}{L}\right)_p$$



CMOS ND2

$$V_{th}(ND2) => V_1 = V_2 = V_{out}$$

$$V_{th}(INV) = V_{in} = V_{out}$$

$$V_{th}(NAND2) = \frac{V_{Tn} + 2\sqrt{\frac{k_p}{k_n}}\left(V_{DD} + V_{Tp}\right)}{1 + 2\sqrt{\frac{k_p}{k_n}}}$$

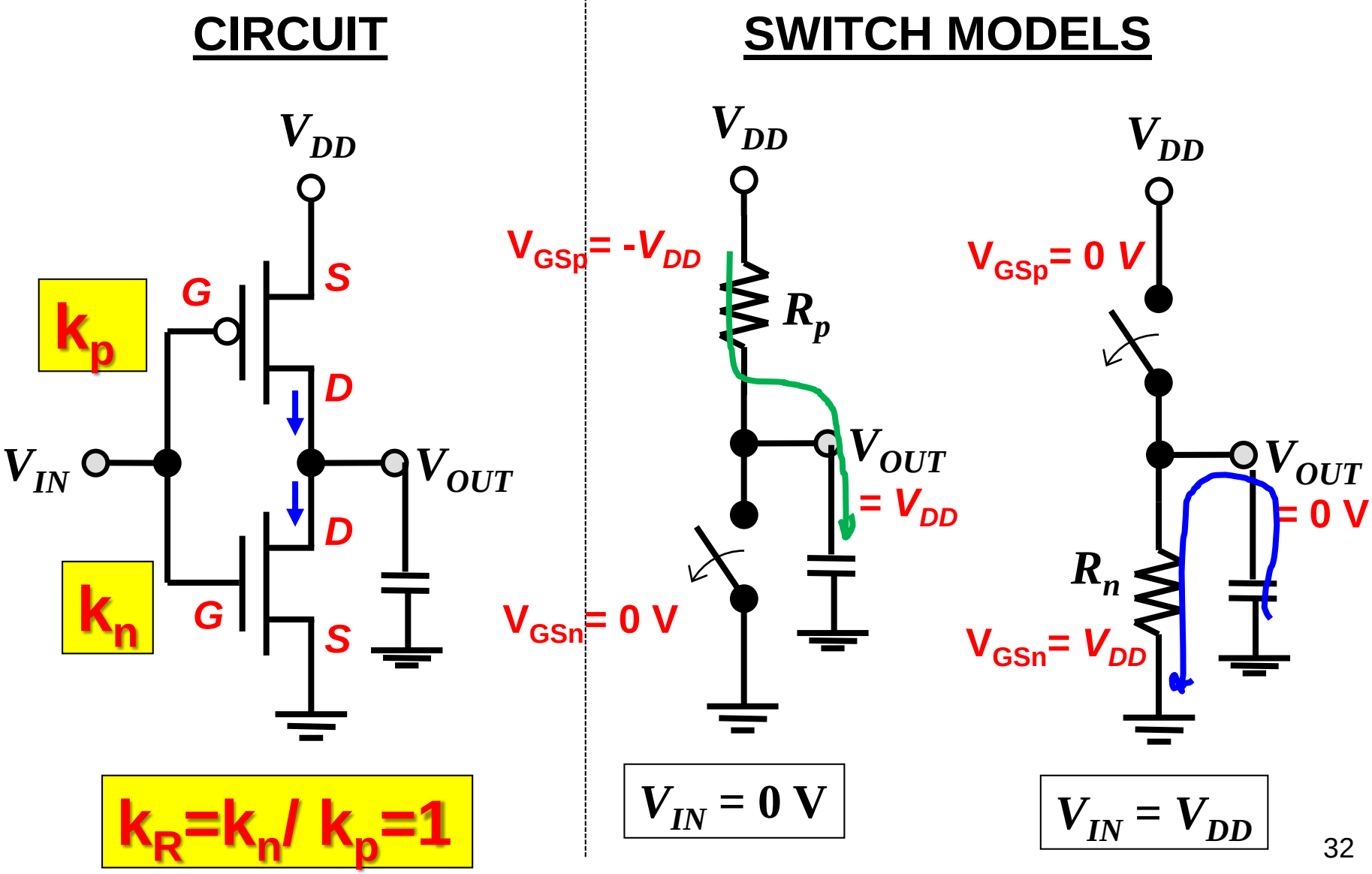
Symmetrical EQUIV INV

$k_R = 1$

$k_n = 2^2 k_p$

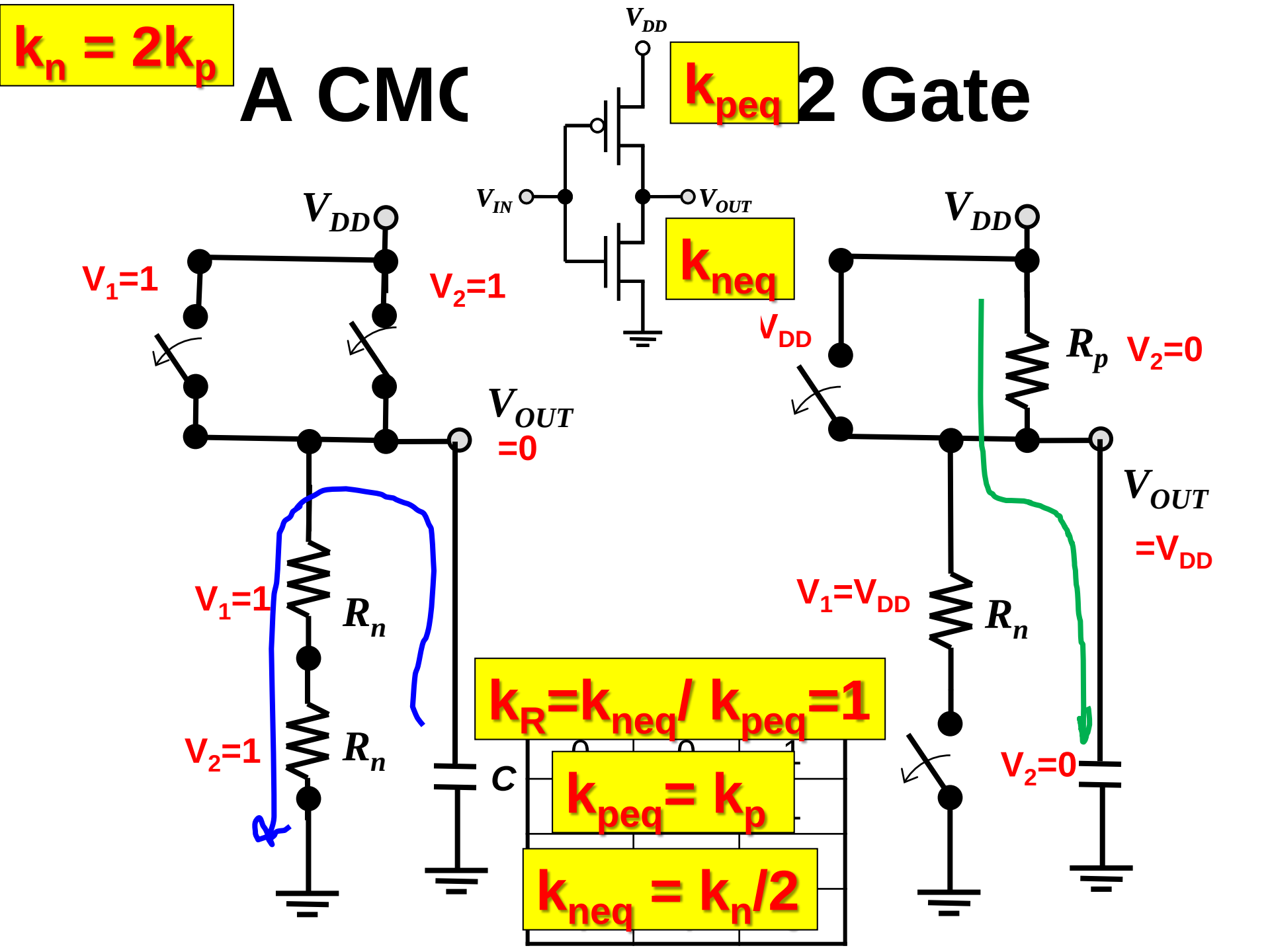
$$\mu_n\left(\frac{W}{L}\right)_n = 2^2 \mu_p\left(\frac{W}{L}\right)_p$$

The CMOS Inverter: Intuitive Perspective



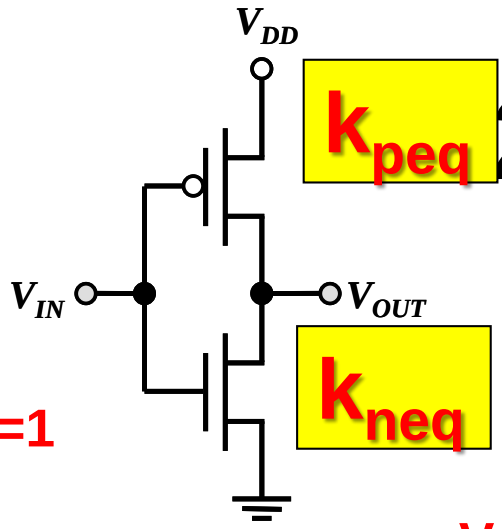
$k_n = 2k_p$

A CMC 2 Gate



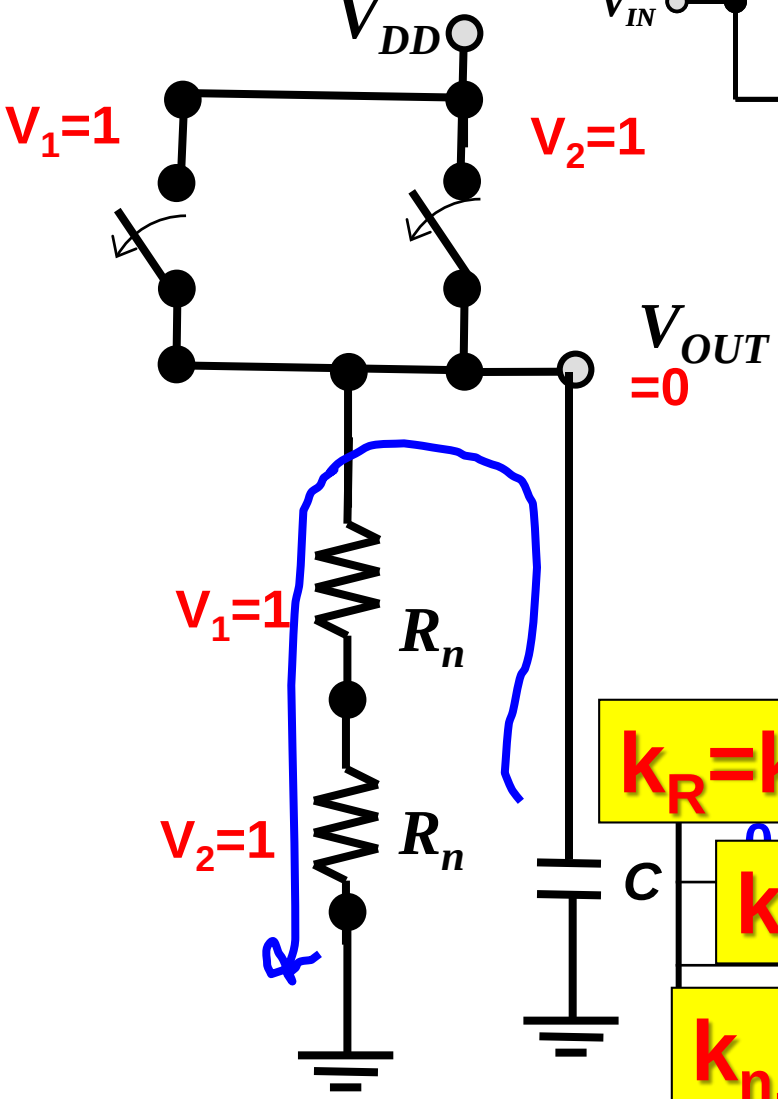
$k_n = 2^2 k_p$

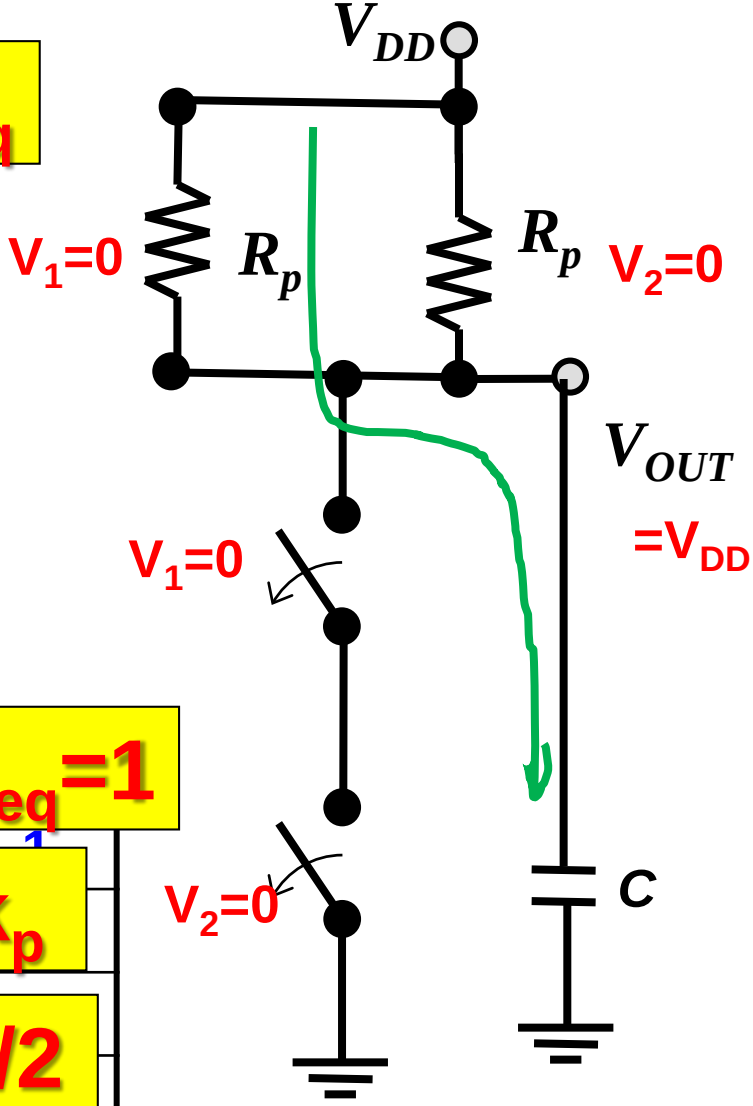
A CMC 2 Gate



k_{peq}

k_{neq}



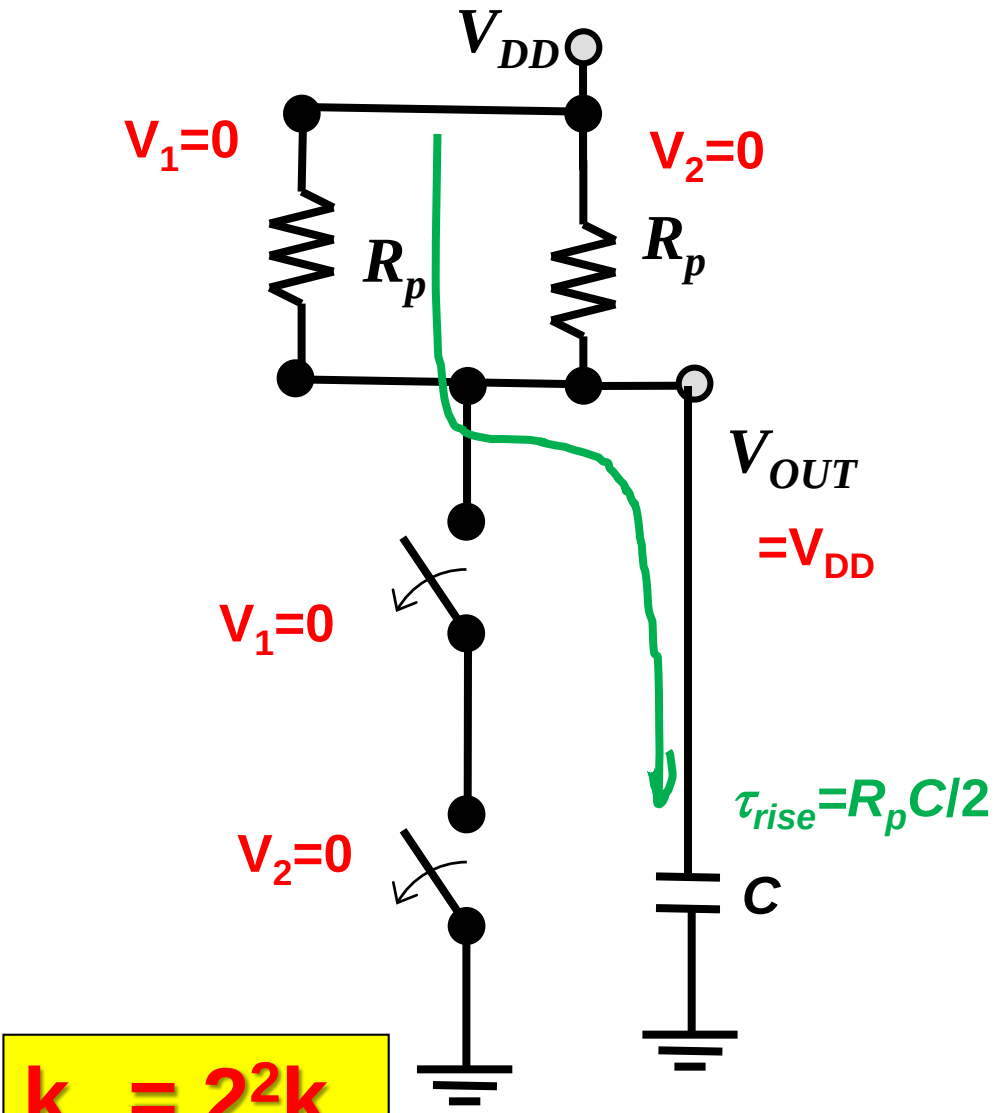


$k_R = k_{neq} / k_{peq} = 1$

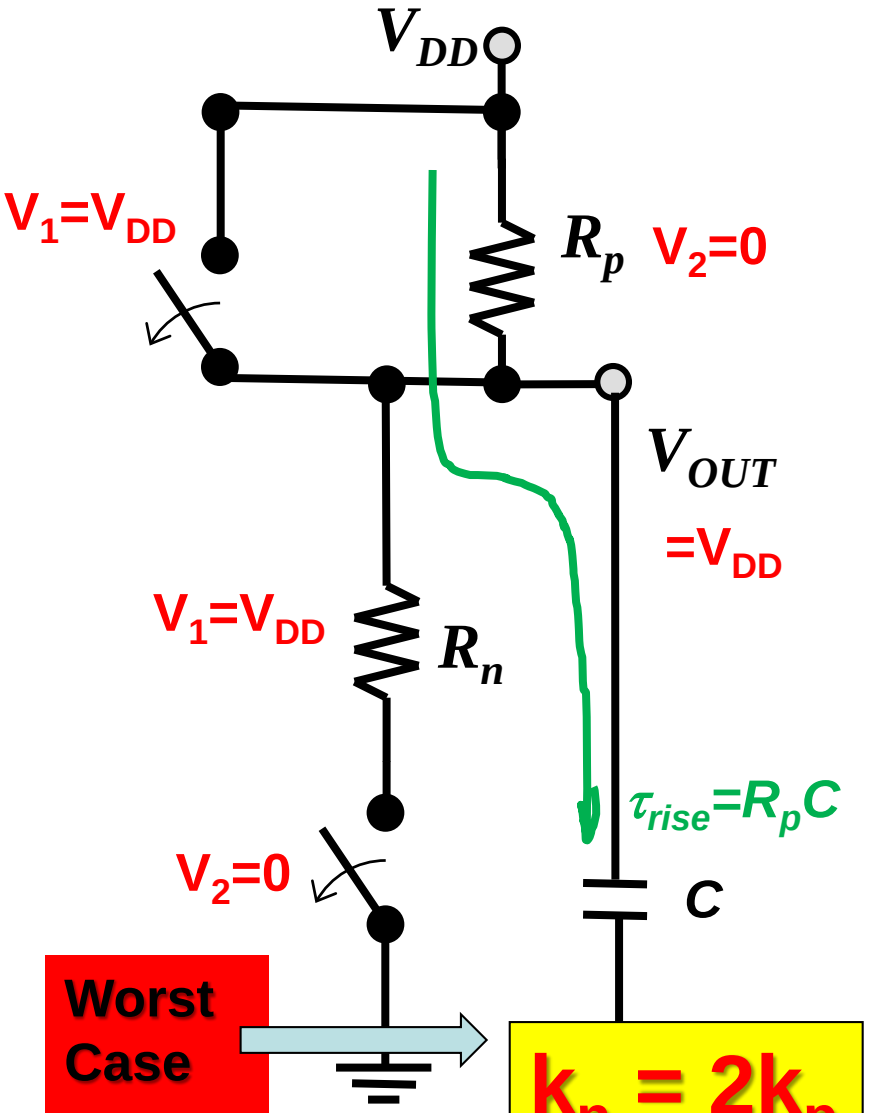
$k_{peq} = 2k_p$

$k_{n,eq} = k_n/2$

A CMOS NAND2 Gate



$k_n = 2^2 k_p$



Worst Case

$k_n = 2k_p$

NAND Gate (pMOS Channel Width)

To equalize the rise and fall time for the 'worst case' switching, for an M-input NAND gate,

$$k_{\mathrm{n}} = Mk_{\mathrm{p}} \quad \rightarrow \quad \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W_{\mathrm{n}}}{L_{\mathrm{n}}} = M\mu_{\mathrm{p}} C_{\mathrm{ox}} \frac{W_{\mathrm{p}}}{L_{\mathrm{p}}}$$

For a 2-input NAND gate, provided that $L_{\mathrm{n}} = L_{\mathrm{p}}$,

$$\mu_{\mathrm{n}} W_n = 2\mu_{\mathrm{p}} W_{\mathrm{p}}$$

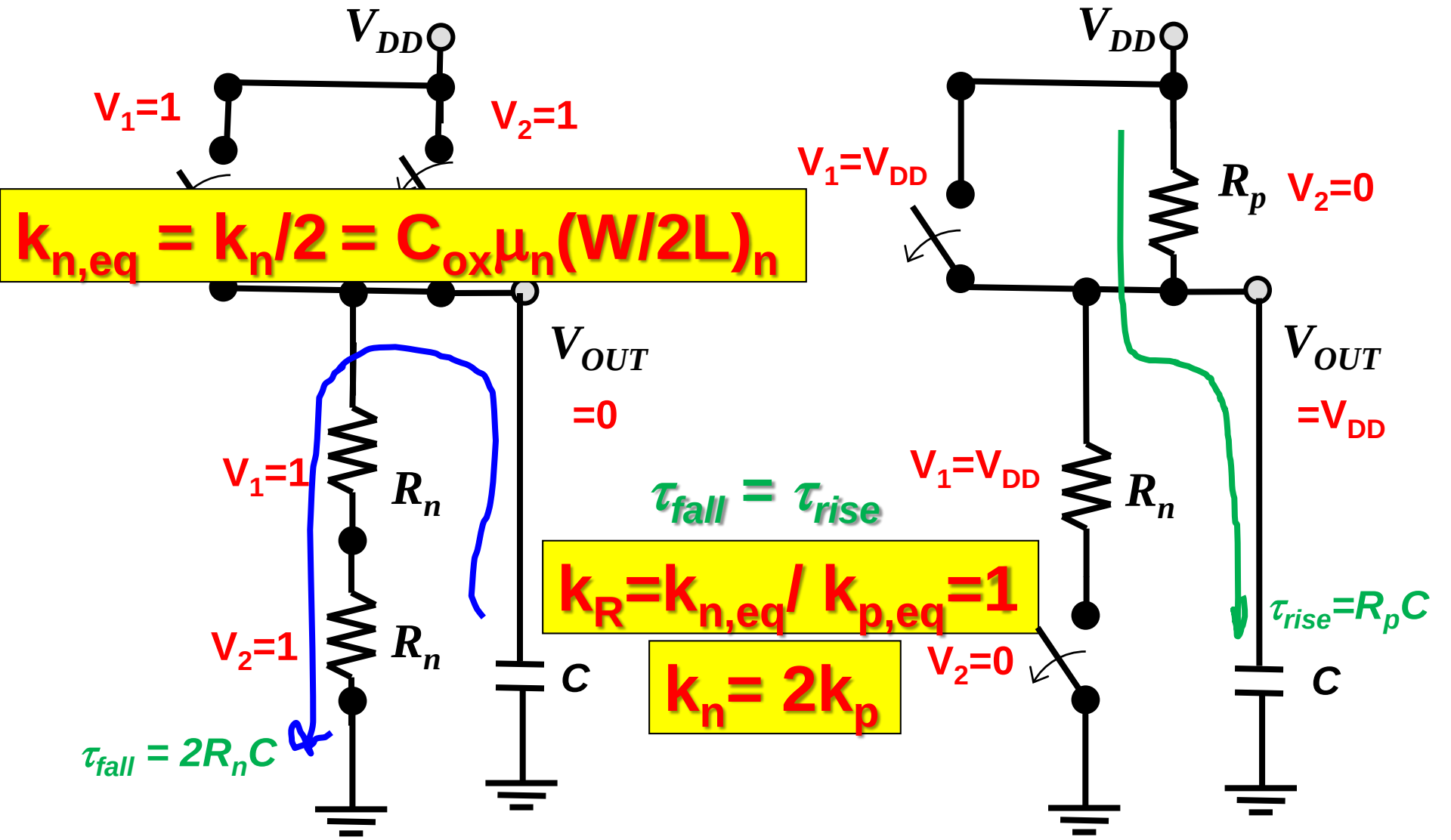
Let electron mobility be $0.1 \mathrm{m^2V^{-1}s^{-1}}$ and hole mobility be $0.05\ \mathrm{m^2V^{-1}s^{-1}}$, then

$$W_n = W_{\mathrm{p}}$$

~~$k_n = M^2\, k_p$~~ $\Rightarrow$ $W_n = \mathbf{2}W_{\mathrm{p}}$

A CMOS NAND2 Gate

$k_{p,eq} = k_p = C_{ox}\mu_p(W/L)_p$



$k_{p,eq} = 2k_p = C_{ox}\mu_p(2W/L)_p$

MOS NAND2 Gate