EEE104 – Digital Electronics (I)

Lecture 18

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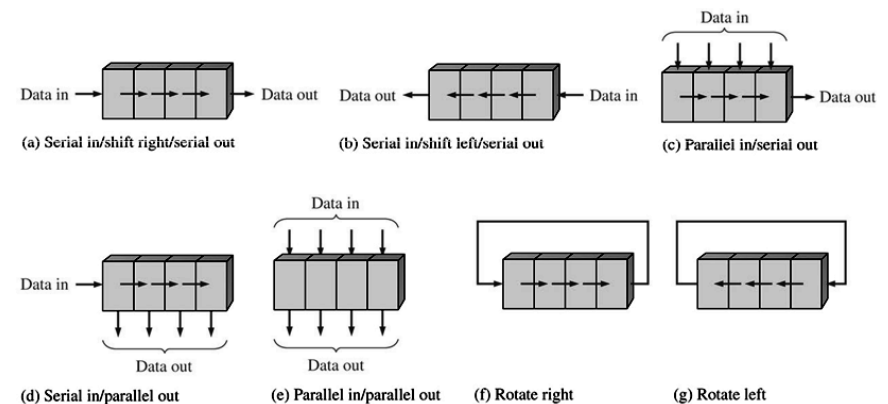
XJTLU

In This Session

- Shift Registers

Shift Registers

- A **shift register** is made up of a set of cascaded flip-flops which store and move data.

- Each flip-flop (a stage) stores one bit of the data.

- The data moves from stage to stage at the triggering edges of a clock signal.

Shift Registers

- Types of shift registers

(a) Serial in/shift right/serial out
(b) Serial in/shift left/serial out
(c) Parallel in/serial out
(d) Serial in/parallel out
(e) Parallel in/parallel out
(f) Rotate right
(g) Rotate left

Shift Registers

Applications of shift registers

1. To convert serial data to parallel data
A computer system commonly requires incoming data to be in parallel format. But frequently, these systems must communicate with external devices that send or receive serial data.

Shift Registers

Applications of shift registers

2. To produce time delay
The SI/SO shift register can be used as a time delay device. The amount of delay can be controlled by the number of registers and the clock frequency.
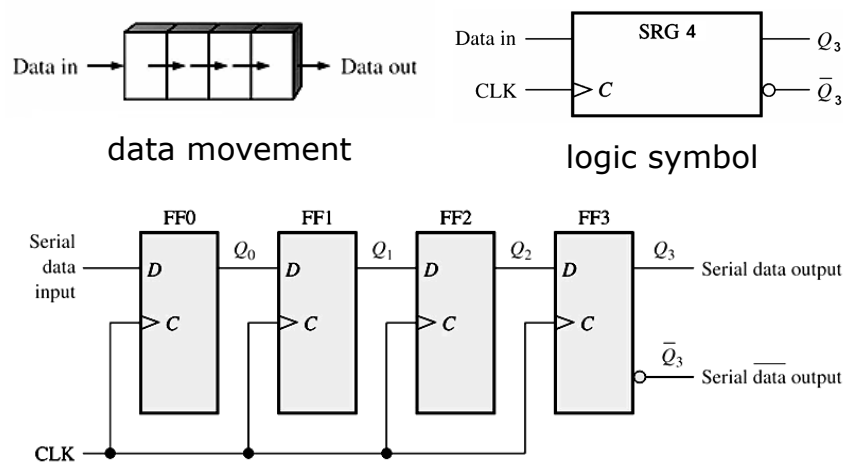
3. Hardware Division or Multiplication by Two
Many computers and microprocessors support instructions 'shift right' and 'shift left' for the data in a register, efficiently dividing or multiplying the data by two.
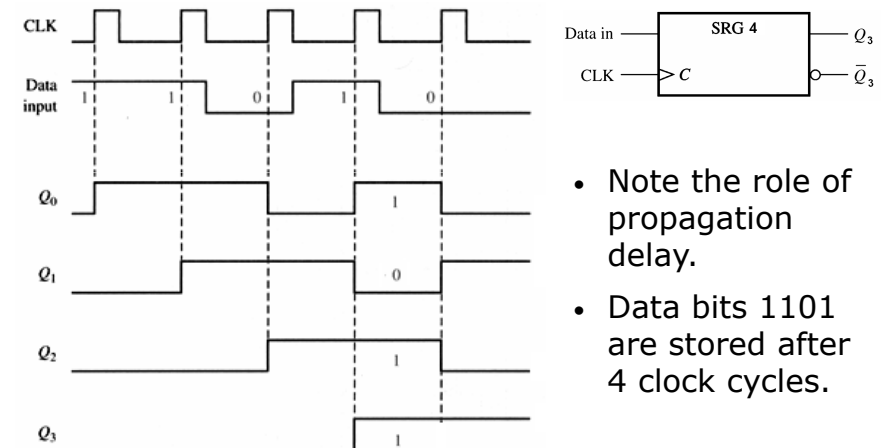
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0000 1100 (12)
0000 0110 (6)
0000 0011 (3)
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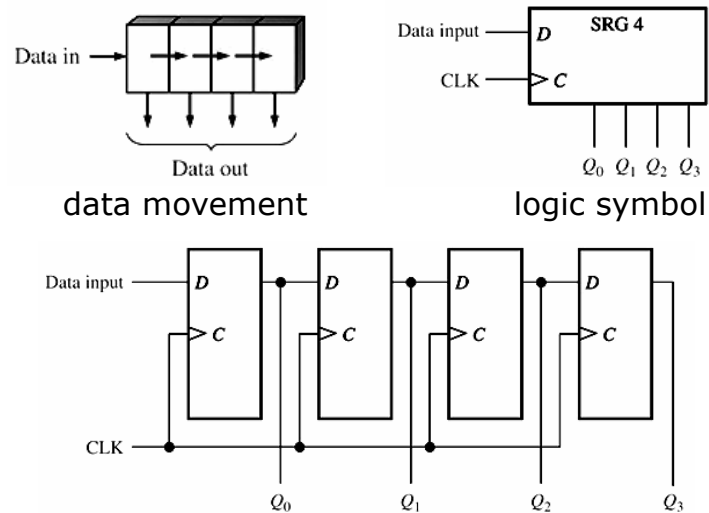
Serial In/Serial Out Shift Registers

data movement

logic symbol

Serial In/Serial Out Shift Registers

- Note the role of propagation delay.

- Data bits 1101 are stored after 4 clock cycles.

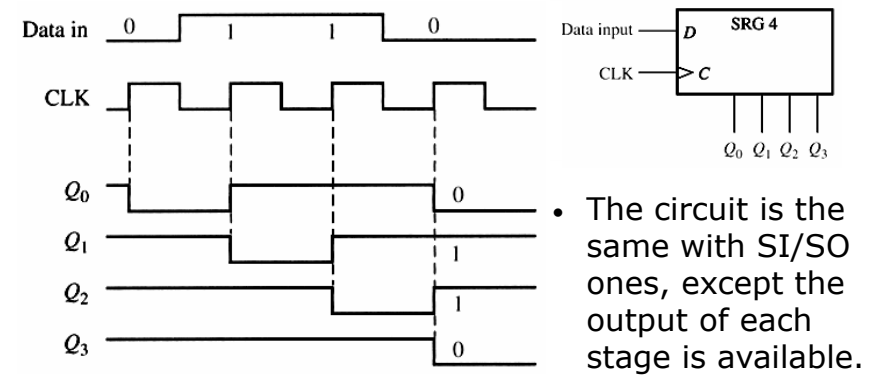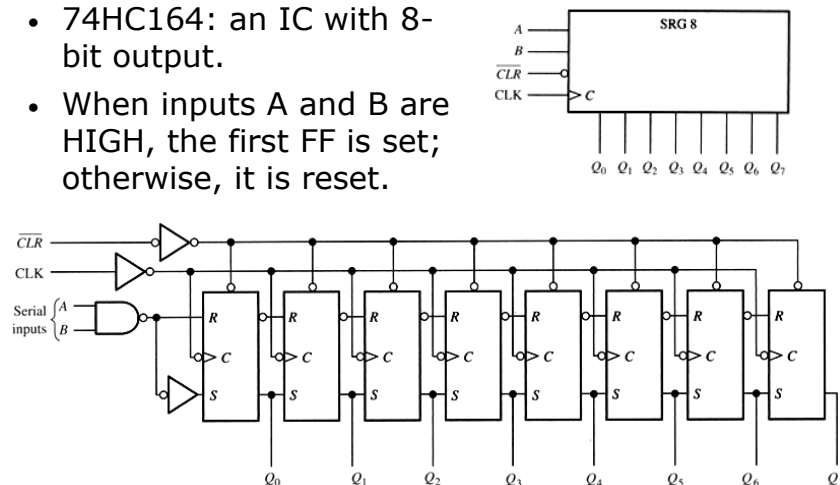## Serial In/Parallel Out Shift Registers

data movement | logic symbol

Serial In/Parallel Out Shift Registers

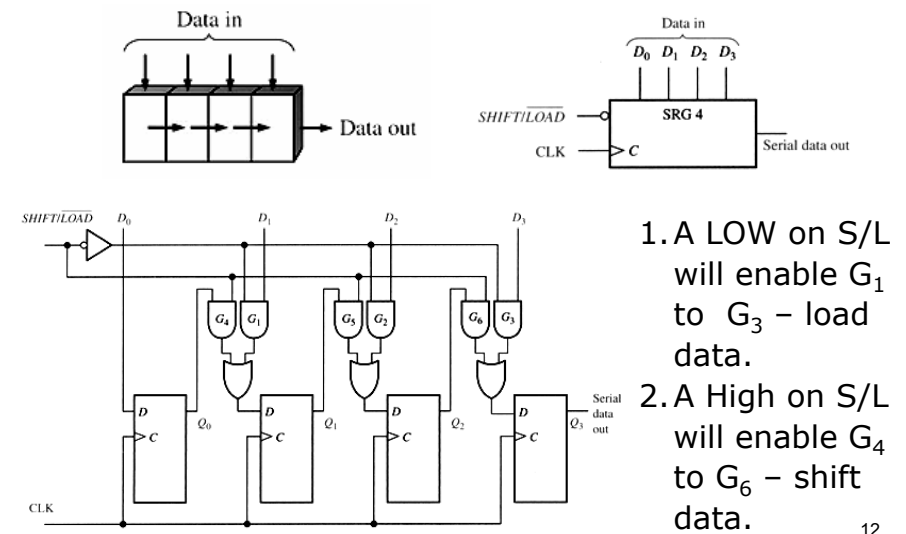- The circuit is the same with SI/SO ones, except the output of each stage is available.

Serial In/Parallel Out Shift Registers

- 74HC164: an IC with 8-bit output.
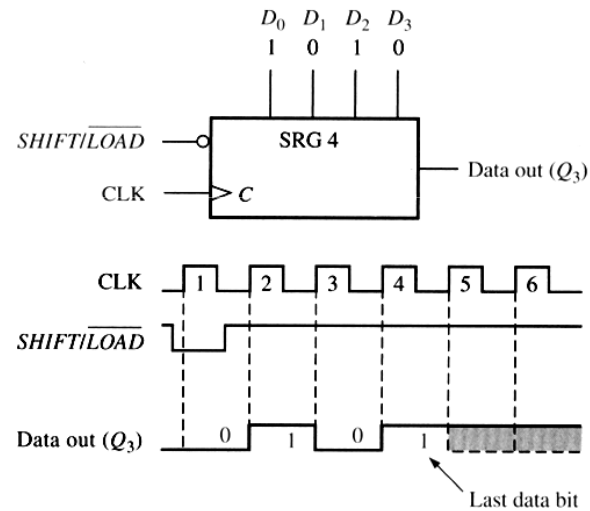- When inputs A and B are HIGH, the first FF is set; otherwise, it is reset.
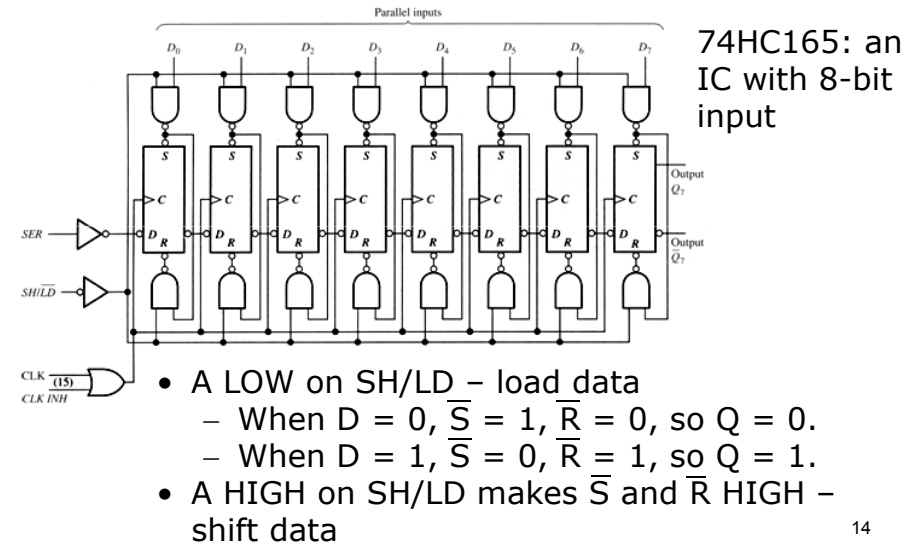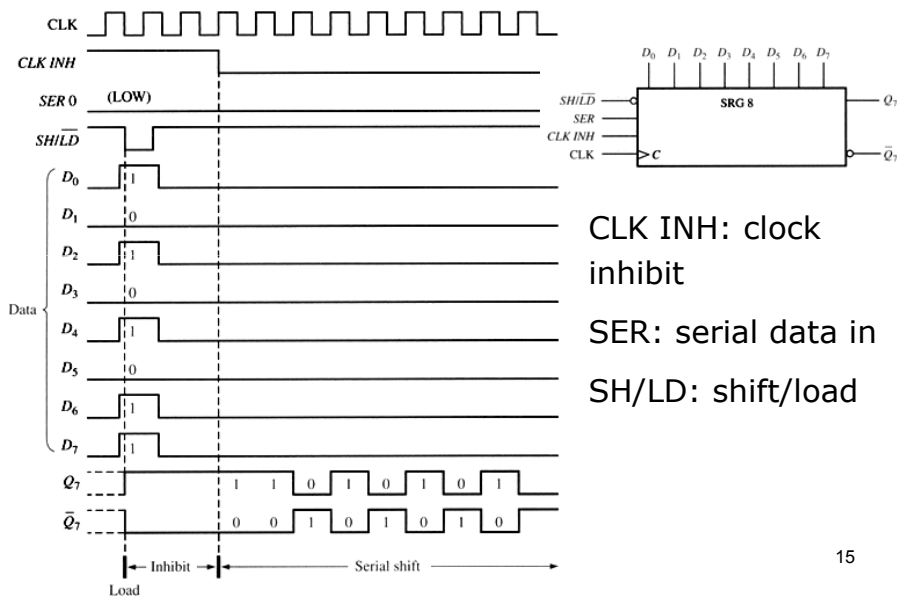
Parallel In/Serial Out Shift Registers

1. A LOW on S/L will enable G_1 to G_3 – load data.
2. A High on S/L will enable G_4 to G_6 – shift data.

Parallel In/Serial Out Shift Registers

D_0 D_1 D_2 D_3
1   0   1   0

$SHIFT/\overline{LOAD}$ —○ | SRG 4 | — Data out (Q_3)

CLK —▷ C

CLK 1 2 3 4 5 6

$SHIFT/\overline{LOAD}$

Data out (Q_3) 0 1 0 1

Last data bit

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Parallel In/Serial Out Shift Registers

Parallel inputs

D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7

SER

$SH/\overline{LD}$

Output Q_7
Output $\overline{Q_7}$

CLK (15)
CLK INH

74HC165: an IC with 8-bit input

- A LOW on SH/LD – load data
  – When D = 0, $\overline{S}$ = 1, $\overline{R}$ = 0, so Q = 0.
  – When D = 1, $\overline{S}$ = 0, $\overline{R}$ = 1, so Q = 1.
- A HIGH on SH/LD makes $\overline{S}$ and $\overline{R}$ HIGH – shift data

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Parallel In/Serial Out Shift Registers

CLK

CLK INH

SER 0 (LOW)

$SH/\overline{LD}$

D_0 1
D_1 0
D_2 1
D_3 0
D_4 1
D_5 0
D_6 1
D_7 1

Data

Q_7 1 1 0 1 0 1 0 1

$\overline{Q_7}$ 0 0 1 0 1 0 1 0

Inhibit — Serial shift

Load

D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7

$SH/\overline{LD}$ —○ | SRG 8 | — Q_7
SER
CLK INH
CLK —▷ C — ○ $\overline{Q_7}$

CLK INH: clock inhibit

SER: serial data in

SH/LD: shift/load

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Parallel In/Parallel Out Shift Registers

Data in

Data out

Parallel data inputs

D_0 D_1 D_2 D_3

D D D D
▷C ▷C ▷C ▷C

CLK

Q_0 Q_1 Q_2 Q_3

Parallel data outputs

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