EEE201: CMOS IC

PROBLEM CLASS 1

conductor substrate. The potential ϕ_{Fp} is the difference (in volts) between E_F and E_{Fi} and is given by

$$e\phi_{Fp} = E_F - E_{Fi} = -kT \ln\left(\frac{N_a}{n_i}\right) \tag{6.8a}$$

or

$$\phi_{Fp} = -V_t \ln\left(\frac{N_a}{n_i}\right) \tag{6.8b}$$

where N_a is the acceptor doping concentration and n_i is the intrinsic carrier concentration.

EXAMPLE 6.1

OBJECTIVE

Determine the potential ϕ_{Fp} in silicon at $T = 300$ K for (*a*) $N_a = 10^{15}$ cm^{-3} and (*b*) $N_a = 10^{17}$ cm^{-3}.

■ Solution

From Equation (6.8b), we have

$$\phi_{Fp} = -V_t \ln\left(\frac{N_a}{n_i}\right) = -(0.0259) \ln\left(\frac{N_a}{1.5 \times 10^{10}}\right)$$

so for (*a*) $N_a = 10^{15}$ cm^{-3},

$$\phi_{Fp} = -0.288 \text{ V}$$

and for (*b*) $N_a = 10^{17}$ cm^{-3},

$$\phi_{Fp} = -0.407 \text{ V}$$

■ Comment

This simple example is intended to show the order of magnitude of ϕ_{Fp} and to show, because of the logarithm function, that ϕ_{Fp} is not a strong function of substrate doping concentration.

Exercise Problem

EX6.1 Consider p-type silicon at $T = 300$ K. Determine the semiconductor doping concentration if $\phi_{Fp} = -0.340$ V. [7.54×10^{15} cm^{-3} = N_a, Ans]

EXAMPLE 6.2

OBJECTIVE

Calculate the maximum space charge width given a particular semiconductor doping concentration.

Consider silicon at $T = 300$ K doped to $N_a = 10^{16}$ cm^{-3}.

■ Solution

From Equation (6.8b), we have

$$\phi_{Fp} = -V_t \ln\left(\frac{N_a}{n_i}\right) = -(0.0259)\ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = -0.347 \text{ V}$$

Then the maximum space charge width is

$$x_{dT} = \left[\frac{4\epsilon_s|\phi_{Fp}|}{eN_a}\right]^{1/2} = \left[\frac{4(11.7)(8.85 \times 10^{-14})(0.347)}{(1.6 \times 10^{-19})(10^{16})}\right]^{1/2}$$

or

$$x_{dT} = 0.30 \times 10^{-4} = 0.30 \ \mu\text{m}$$

■ Comment

The maximum induced space charge width is on the same order of magnitude as pn junction space charge widths.

Exercise Problem

EX6.2 (*a*) Consider as oxide-to-p-type silicon junction at $T = 300$ K. The impurity doping concentration in the silicon is $N_a = 3 \times 10^{16}$ cm^{-3}. Calculate the maximum space charge width in the silicon. (*b*) Repeat part (*a*) for an impurity concentration of $N_a = 10^{15}$ cm^{-3}. [Ans. (*a*) 0.180 μm, (*b*) 0.863 μm]

EXAMPLE 6.3

OBJECTIVE

Calculate the metal–semiconductor work function difference ϕ_{ms} for a given MOS system and semiconductor doping.

For an aluminum–silicon dioxide junction, $\phi_m' = 3.20$ V and for a silicon–silicon dioxide junction, $\chi' = 3.25$ V. We can assume that $E_g = 1.12$ eV. Let the p-type doping be $N_a = 10^{14}$ cm^{-3}.

■ Solution

For silicon at $T = 300$ K, we can calculate ϕ_{Fp} as

$$\phi_{Fp} = -V_t \ln\left(\frac{N_a}{n_i}\right) = -(0.0259)\ln\left(\frac{10^{14}}{1.5 \times 10^{10}}\right) = -0.228 \text{ V}$$

Then the work function difference is

$$\phi_{ms} = \phi_m' - \left(\chi' + \frac{E_g}{2e} + |\phi_{Fp}|\right) = 3.20 - (3.25 + 0.56 + 0.288)$$

or

$$\phi_{ms} = -0.838 \text{ V}$$

■ Comment

The value of ϕ_{ms} will become more negative as the doping of the p-type substrate increases.

Exercise Problem

EX6.3 Calculate the metal–semiconductor work function difference ϕ_{ms} for an aluminum–silicon dioxide–silicon device if the silicon is p type and doped to a concentration of $N_a = 10^{16}$ cm^{-3}. Assume $T = 300$ K. (Ans. $\phi_{ms} = -0.957$ V)

Table 6.2 | Summary of equations for metal–semiconductor work function difference

p-type Silicon	n-type Silicon
Aluminum gate:	Aluminum gate:
$\phi_{ms} = \left[\phi'_m - \left(\chi' + \frac{E_g}{2e} + \lvert\phi_{Fp}\rvert\right)\right]$	$\phi_{ms} = \left[\phi'_m - \left(\chi' + \frac{E_g}{2e} - \phi_{Fn}\right)\right]$
n^+ polysilicon gate:	n^+ polysilicon gate:
$\phi_{ms} = -\left(\frac{E_g}{2e} + \lvert\phi_{Fp}\rvert\right)$	$\phi_{ms} = -\left(\frac{E_g}{2e} - \phi_{Fn}\right)$
p^+ polysilicon gate:	p^+ polysilicon gate
$\phi_{ms} = \left(\frac{E_g}{2e} - \lvert\phi_{Fp}\rvert\right)$	$\phi_{ms} = \left(\frac{E_g}{2e} + \phi_{Fn}\right)$

For the expressions listed, we have assumed that $E_F = E_c$ and $E_F = E_v$ in the n^+ and p^+ polysilicon gates, respectively.

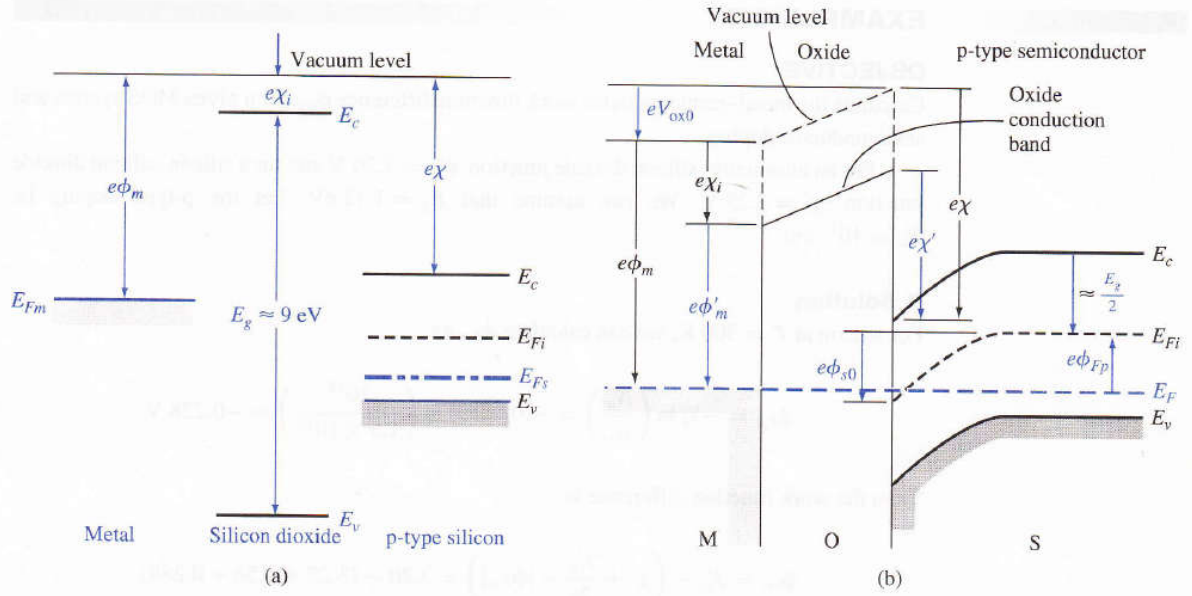


Figure 6.18 | (a) Energy levels in an MOS system prior to contact and (b) energy-band diagram through the MOS structure in thermal equilibrium after contact.

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} \qquad (6.28)$$

EXAMPLE 6.4

OBJECTIVE

Calculate the flat-band voltage for a MOS capacitor with a p-type semiconductor substrate.

Consider an MOS structure with a p-type semiconductor substrate doped to $N_a = 10^{16}$ cm^{-3}, a silicon dioxide insulator with a thickness of $t_{ox} = 500$ Å, and an n^+ polysilicon gate. Assume that $Q'_{ss} = 10^{11}$ electronic charges per cm^2.

■ Solution

The work function difference, from Figure 6.21, is $\phi_{ms} = -1.1$ V. The oxide capacitance can be found as

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{500 \times 10^{-8}} = 6.9 \times 10^{-8} \text{ F/cm}^2$$

The equivalent oxide surface charge density is

$$Q'_{ss} = (10^{11})(1.6 \times 10^{-19}) = 1.6 \times 10^{-8} \text{ C/cm}^2$$

The flat-band voltage is then calculated as

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} = -1.1 - \left(\frac{1.6 \times 10^{-8}}{6.9 \times 10^{-8}}\right) = -1.33 \text{ V}$$

■ Comment

The applied gate voltage required to achieve the flat-band condition for this p-type substrate is negative. If the amount of fixed oxide charge increases, the flat-band voltage becomes even more negative.

Exercise Problem

EX6.4 The silicon impurity doping concentration in an aluminum–silicon dioxide–silicon MOS structure is $N_a = 3 \times 10^{16}$ cm^{-3}. For an oxide thickness of $t_{ox} = 200$ Å and an oxide charge of $Q'_{ss} = 8 \times 10^{10}$ cm^{-2}, calculate the flat-band voltage. (Ans. $\phi_{ms} \approx -0.97$ V, $V_{FB} = -1.04$ V)

$$|Q'_{SD}(\text{max})| = eN_a x_{dT} \tag{6.30}$$

$$V_{TN} = \frac{|Q'_{SD}(\text{max})|}{C_{\text{ox}}} - \frac{Q'_{ss}}{C_{\text{ox}}} + \phi_{ms} + 2|\phi_{Fp}| \tag{6.34a}$$

$$V_{TN} = (|Q'_{SD}(\text{max})| - Q'_{ss})\left(\frac{t_{\text{ox}}}{\epsilon_{\text{ox}}}\right) + \phi_{ms} + 2|\phi_{Fp}| \tag{6.34b}$$

$$V_{TN} = \frac{|Q'_{SD}(\text{max})|}{C_{\text{ox}}} + V_{FB} + 2|\phi_{Fp}| \tag{6.34c}$$

DESIGN EXAMPLE 6.5

OBJECTIVE

Design the oxide thickness of an MOS system to yield a specified threshold voltage.

Consider an n^+ polysilicon gate and a p-type silicon substrate doped to $N_a = 5 \times 10^{16}$ cm^{-3}. Assume $Q'_{ss} = 10^{11}$ cm^{-2}. Determine the oxide thickness such that $V_{TN} = +0.40$ V.

Solution

From Figure 6.21, the work function difference is $\phi_{ms} \approx -1.15$ V. The other various parameters can be calculated as

$$\phi_{Fp} = -V_t \ln\left(\frac{N_a}{n_i}\right) = -(0.0259)\ln\left(\frac{5 \times 10^{16}}{1.5 \times 10^{10}}\right) = -0.389 \text{ V}$$

and

$$x_{dT} = \left(\frac{4\epsilon_s|\phi_{Fp}|}{eN_a}\right)^{1/2} = \left[\frac{4(11.7)(8.85 \times 10^{-14})(0.389)}{(1.6 \times 10^{-19})(5 \times 10^{16})}\right]^{1/2} = 0.142 \ \mu\text{m}$$

Then

$$|Q'_{SD}(\text{max})| = eN_a x_{dT} = (1.6 \times 10^{-19})(5 \times 10^{16})(0.142 \times 10^{-4})$$

or

$$|Q'_{SD}(\text{max})| = 1.14 \times 10^{-7} \text{ C/cm}^2$$

The oxide thickness can be determined from the threshold equation

$$V_{TN} = \left[|Q'_{SD}(\text{max})| - Q'_{ss}\right]\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2|\phi_{Fp}|$$

Then

$$0.40 = \frac{[1.14 \times 10^{-7} - (10^{11})(1.6 \times 10^{-19})]}{(3.9)(8.85 \times 10^{-14})} t_{ox} - 1.15 + 2(0.389)$$

which yields

$$t_{ox} = 272 \text{ Å}$$

Comment

The threshold voltage for this case is a positive quantity, which means that the MOS device is an enhancement-mode device; a gate voltage must be applied to create the inversion layer charge, which is zero for zero applied gate voltage.

Exercise Problem

EX6.5 Repeat Example 6.5 for the case when the gate material is aluminum.

(Ans. $\phi_{ms} \approx -0.98$ V, $t_{ox} = 212$ Å)

EXAMPLE 6.6

OBJECTIVE

Calculate the threshold voltage of an MOS system using an aluminum gate.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{14}$ cm^{-3}. Let $Q'_{ss} = 10^{10}$ cm^{-2}, $t_{ox} = 500$ Å, and assume the oxide is silicon dioxide. From Figure 6.21, we have that $\phi_{ms} = -0.83$ V.

■ Solution

We can start calculating the various parameters as

$$\phi_{Fp} = -V_t \ln\left(\frac{N_a}{n_i}\right) = -(0.0259)\ln\left(\frac{10^{14}}{1.5 \times 10^{10}}\right) = -0.228 \text{ V}$$

and

$$x_{dT} = \left(\frac{4\epsilon_s|\phi_{Fp}|}{eN_a}\right)^{1/2} = \left[\frac{4(11.7)(8.85 \times 10^{-14})(0.228)}{(1.6 \times 10^{-19})(10^{14})}\right]^{1/2} = 2.43\ \mu\text{m}$$

Then

$$|Q'_{SD}(\text{max})| = eN_a x_{dT} = (1.6 \times 10^{-19})(10^{14})(2.43 \times 10^{-4}) = 3.89 \times 10^{-9} \text{ C/cm}^2$$

We can now calculate the threshold voltage as

$$V_{TN} = (|Q'_{SD}(\text{max})| - Q'_{ss})\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2|\phi_{Fp}|$$

$$= [(3.89 \times 10^{-9}) - (10^{10})(1.6 \times 10^{-19})]\left[\frac{500 \times 10^{-8}}{(3.9)(8.85 \times 10^{-14})}\right]$$

$$- 0.83 + 2(0.228)$$

$$= -0.341 \text{ V}$$

■ Comment

In this example, the semiconductor is very lightly doped, which, in conjunction with the positive charge in the oxide and the work function potential difference, is sufficient to induce an electron inversion layer charge even with zero applied gate voltage. This condition makes the threshold voltage negative.

Exercise Problem

EX6.6 An MOS device has the following parameters: aluminum gate, p-type substrate with $N_a = 3 \times 10^{16}$ cm^{-3}, $t_{ox} = 250$ Å, and $Q'_{ss} = 10^{11}$ cm^{-2}. Determine the threshold voltage. (Ans. $\phi_{ms} \approx -0.97$ V, $V_{TN} = +0.292$ V)

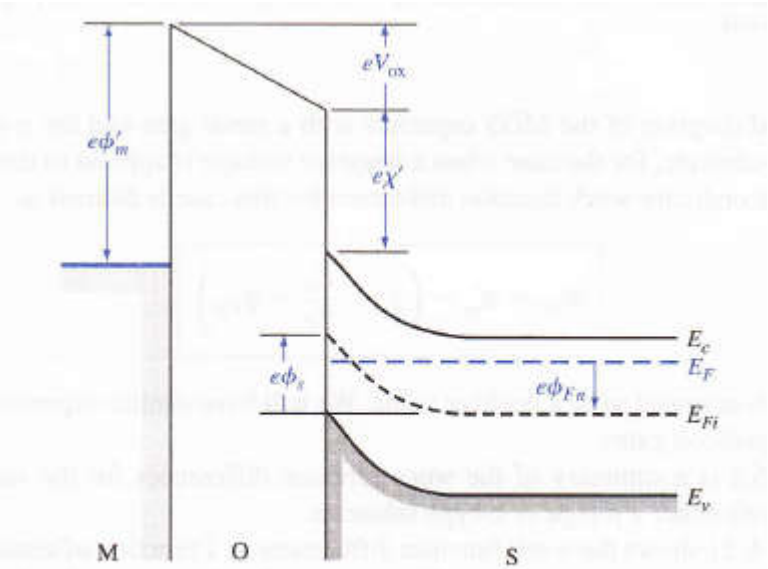


Figure 6.20 | Energy-band diagram through the MOS structure with an n-type substrate for a negative applied gate bias.

Figure 6.20 showed the energy-band diagram of the MOS structure with an n-type substrate and with an applied negative gate voltage. The threshold voltage for this case can be derived and is given by

$$V_{TP} = (-|Q'_{SD}(\max)| - Q'_{ss})\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} - 2\phi_{Fn} \tag{6.35}$$

where

$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} - \phi_{Fn}\right) \tag{6.36a}$$

$$|Q'_{SD}(\max)| = eN_d x_{dT} \tag{6.36b}$$

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{Fn}}{eN_d}\right)^{1/2} \tag{6.36c}$$

and

$$\phi_{Fn} = V_t \ln\left(\frac{N_d}{n_i}\right) \tag{6.36d}$$

DESIGN EXAMPLE 6.7

OBJECTIVE

Design the semiconductor doping concentration to yield a specified threshold voltage.

Consider an aluminum–silicon dioxide–silicon MOS structure. The silicon is n type, the oxide thickness is $t_{ox} = 650$ Å, and the trapped charge density is $Q'_{ss} = 10^{10}$ cm^{-2}. Determine the doping concentration such that $V_{TP} = -1.0$ V.

■ Solution

The solution to this design problem is not straightforward, since the doping concentration appears in the terms ϕ_{Fn}, x_{dT}, $Q'_{SD}(\text{max})$, and ϕ_{ms}. The threshold voltage, then, is a nonlinear function of N_d. Without a computer-generated solution, we resort to trial and error.

For $N_d = 2.5 \times 10^{14}$ cm^{-3}, we find

$$\phi_{Fn} = V_t \ln\left(\frac{N_d}{n_i}\right) = 0.252 \text{ V}$$

and

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{Fn}}{eN_d}\right)^{1/2} = 1.62\ \mu\text{m}$$

Then

$$|Q'_{SD}(\text{max})| = eN_d x_{dT} = 6.48 \times 10^{-9} \text{ C/cm}^2$$

From Figure 6.21,

$$\phi_{ms} = -0.35 \text{ V}$$

The threshold voltage is

$$V_{TP} = (-|Q'_{SD}(\text{max})| - Q'_{ss})\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} - 2\phi_{Fn}$$

$$= \frac{[-(6.48 \times 10^{-9}) - (10^{10})(1.6 \times 10^{-19})](650 \times 10^{-8})}{(3.9)(8.85 \times 10^{-14})} - 0.35 - 2(0.252)$$

which yields

$$V_{TP} = -1.006 \text{ V}$$

and is essentially equal to the desired result.

■ Comment

The threshold voltage is negative, implying that this MOS capacitor, with the n-type substrate, is an enhancement mode device. The inversion layer charge is zero with zero gate voltage, and a negative gate voltage must be applied to induce the hole inversion layer.

Exercise Problem

EX6.7 Consider an MOS device with the following parameters: p^+ polysilicon gate, n-type substrate, $t_{ox} = 220$ Å, and $Q'_{ss} = 8 \times 10^{10}$ cm^{-2}. Determine the required n-type doping concentration such that the threshold voltage is in the range $-0.50 \le V_{TP} \le -0.30$ V.

(Ans. By trial and error, we find for $N_d = 4 \times 10^{16}$ cm^{-3}, $\phi_{ms} \approx +1.10$ V, and $V_{TP} = -0.385$ V)

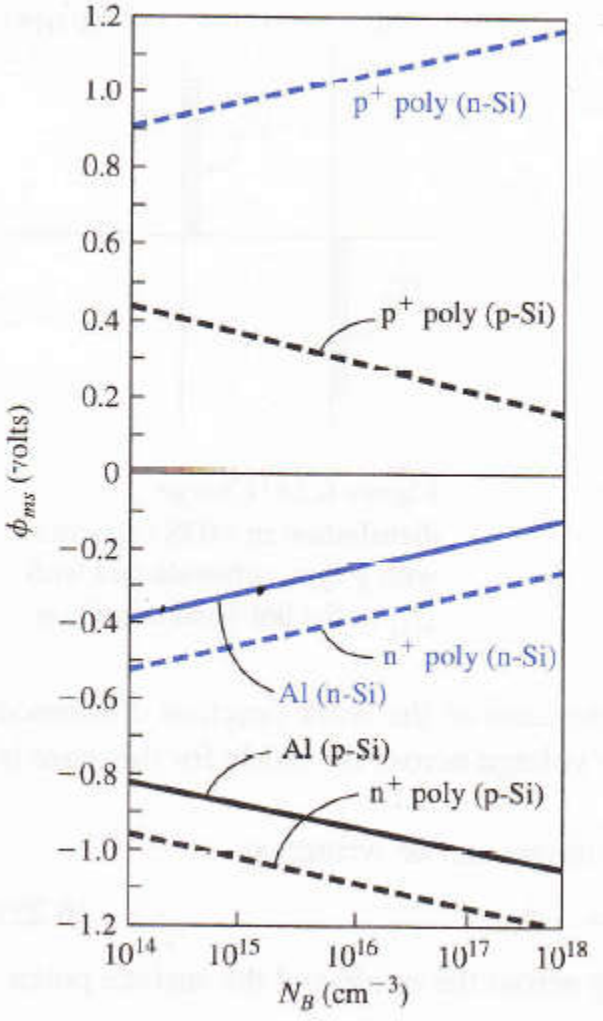


Figure 6.21 | Metal-semiconductor work function differences versus semiconductor doping concentration for aluminum, n^+ polysilicon, and p^+ polysilicon gates.

EXAMPLE 6.8

OBJECTIVE

Calculate the electric field in and the voltage across the oxide at a flat-band condition.

Assume that $Q'_{ss} = 8 \times 10^{10}$ cm^{-2} in silicon dioxide and assume the oxide thickness is $t_{ox} = 150$ Å.

■ Solution

The electric charge density at the interface is

$$Q'_{ss} = (1.6 \times 10^{-19})(8 \times 10^{10}) = 1.28 \times 10^{-8} \text{ C/cm}^2$$

The oxide electric field is then

$$\mathcal{E}_{ox} = \frac{-Q'_{ss}}{\epsilon_{ox}} = \frac{-1.28 \times 10^{-8}}{(3.9)(8.85 \times 10^{-14})} = -3.71 \times 10^4 \text{ V/cm}$$

Since the electric field across the oxide is a constant, the voltage across the oxide is then

$$V_{ox} = -\mathcal{E}_{ox} t_{ox} = -(-3.71 \times 10^4)(150 \times 10^{-8})$$

or

$$V_{ox} = 55.6 \text{ mV}$$

■ Comment

In the flat-band condition, an electric field exists in the oxide and a voltage exists across the oxide due to the Q'_{ss} charge.

Exercise Problem

EX6.8 Repeat Example 6.8 for the case when $Q'_{ss} = 1.2 \times 10^{11}$ cm^{-2} and $t_{ox} = 250$ Å.

(Ans. $\mathcal{E}_{ox} = -5.56 \times 10^4$ V/cm, $V_{ox} = 0.139$ V)

EXAMPLE 6.9

OBJECTIVE

Calculate C_{ox}, C'_{min}, and C'_{FB} for an MOS capacitor.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{16}$ cm^{-3}. The oxide is silicon dioxide with a thickness of 550 Å and the gate is aluminum.

■ Solution

The oxide capacitance is

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{550 \times 10^{-8}} = 6.28 \times 10^{-8} \text{ F/cm}^2$$

To find the minimum capacitance, we need to calculate

$$\phi_{Fp} = -V_t \ln\left(\frac{N_a}{n_i}\right) = -(0.0259) \ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = -0.347 \text{ V}$$

and

$$x_{dT} = \left(\frac{4\epsilon_s |\phi_{Fp}|}{eN_a}\right)^{1/2} = \left[\frac{4(11.7)(8.85 \times 10^{-14})(0.347)}{(1.6 \times 10^{-19})(10^{16})}\right]^{1/2} = 0.30 \times 10^{-4} \text{ cm}$$

Then

$$C'_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_{dT}} = \frac{(3.9)(8.85 \times 10^{-14})}{(550 \times 10^{-8}) + \left(\frac{3.9}{11.7}\right)(0.3 \times 10^{-4})} = 2.23 \times 10^{-8} \text{ F/cm}^2$$

We can note that

$$\frac{C'_{min}}{C_{ox}} = \frac{2.23 \times 10^{-8}}{6.28 \times 10^{-8}} = 0.355$$

The flat-band capacitance is

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\left(\frac{kT}{e}\right)\left(\frac{\epsilon_s}{eN_a}\right)}}$$

$$= \frac{(3.9)(8.85 \times 10^{-14})}{(550 \times 10^{-8}) + \left(\frac{3.9}{11.7}\right)\sqrt{(0.0259)\frac{(11.7)(8.85 \times 10^{-14})}{(1.6 \times 10^{-19})(10^{16})}}}$$

$$= 5.03 \times 10^{-8} \text{ F/cm}^2$$

We can also note that

$$\frac{C'_{FB}}{C_{ox}} = \frac{5.03 \times 10^{-8}}{6.28 \times 10^{-8}} = 0.80$$

■ Comment

The ratios of C'_{min} to C_{ox} and of C'_{FB} to C_{ox} are typical values obtained in C–V plots.

Exercise Problem

EX6.9 Consider an MOS device with the following parameters: aluminum gate, p-type substrate with $N_a = 3 \times 10^{16}$ cm^{-3}, $t_{ox} = 250$ Å, and $Q'_{ss} = 10^{11}$ cm^{-2}. Determine C'_{min}/C_{ox} and C'_{FB}/C_{ox}.

(Ans. $C'_{min}/C_{ox} = 0.294$, $C'_{FB}/C_{ox} = 0.761$)

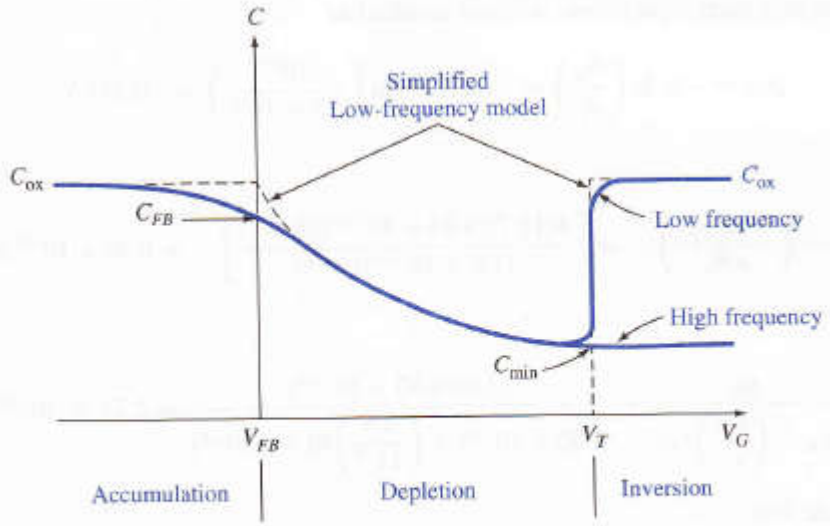


Figure 6.37 | Ideal low-frequency capacitance versus gate voltage of an MOS capacitor with a p-type substrate. Simplified ideal capacitance curve is shown by the dotted line.

$$C'_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_{dT}} \qquad (6.43)$$

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\left(\frac{kT}{e}\right)\left(\frac{\epsilon_s}{eN_a}\right)}} \qquad (6.45)$$

Flat-band capacitance

$$I_D = \frac{W}{L}\mu_n C_{ox}\left[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{6.51a}$$

or

$$I_D = \frac{W}{L}\frac{\mu_n C_{ox}}{2}\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right] \tag{6.51b}$$

$$K_n = \frac{W}{L}\frac{\mu_n C_{ox}}{2} \tag{6.52}$$

$$I_D = K_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right] \tag{6.55}$$

$$I_D = K_n(V_{GS} - V_{TN})^2 \tag{6.57}$$

Equation (6.55) describes the ideal current–voltage relationship of the n-channel MOSFET biased in what is called the *nonsaturation region* for $0 \le V_{DS} \le V_{DS}(\text{sat})$, and Equation (6.57) describes the ideal current–voltage relationship of the n-channel MOSFET biased in what is called the *saturation region* for $V_{DS} \ge V_{DS}(\text{sat})$. Figure 6.51 showed these characteristics.

We can use the *I–V* relations to experimentally determine the mobility and threshold voltage parameters. From Equation (6.51b), we can write, for very small values of V_{DS},

$$I_D = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_{TN})V_{DS} \tag{6.58}$$

Table 6.3 | Summary of ideal NMOS and PMOS current–voltage relationships

NMOS	PMOS
Transition point $V_{DS}(\text{sat}) = V_{GS} - V_{TN}$	**Transition point** $V_{SD}(\text{sat}) = V_{SG} + V_{TP}$
Nonsaturation bias $[V_{DS} \le V_{DS}(\text{sat})]$; $I_D = K_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$	**Nonsaturation bias** $[V_{SD} \le V_{SD}(\text{sat})]$; $I_D = K_p\left[2(V_{SG} + V_{TP})V_{SD} - V_{SD}^2\right]$
Saturation bias $[V_{DS} \ge V_{DS}(\text{sat})]$; $I_D = K_n(V_{GS} - V_{TN})^2$	**Saturation bias** $[V_{SD} \ge V_{SD}(\text{sat})]$; $I_D = K_p(V_{SG} + V_{TP})^2$

where K_p is the conduction parameter for the p-channel device and is defined as

$$K_p = \frac{W}{L}\frac{\mu_p C_{ox}}{2} = \frac{W}{L}\frac{k_p'}{2} \tag{6.61}$$

EXAMPLE 6.10

OBJECTIVE

Design the width of a MOSFET such that a specified current is induced for a given applied bias.

Consider an ideal n-channel MOSFET with parameters $L = 1.25\ \mu m$, $\mu_n = 650\,cm^2/V\text{-}s$, $C_{ox} = 6.9 \times 10^{-8}\ F/cm^2$, and $V_T = 0.65\ V$. Design the channel width W such that $I_D(sat) = 4\ mA$ for $V_{GS} = 5\ V$.

■ Solution

We have, from Equations (6.51) and (6.52),

$$I_D(sat) = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_{TN})^2$$

or

$$4 \times 10^{-3} = \frac{W(650)(6.9 \times 10^{-8})}{2(1.25 \times 10^{-4})} \cdot (5 - 0.65)^2 = 3.39W$$

Then

$$W = 11.8\ \mu m$$

■ Comment

The current capability of a MOSFET is directly proportional to the channel width W. The current handling capability can be increased by increasing W.

Exercise Problem

EX6.10 The parameters of an n-channel MOSFET are $\mu_n = 650\ cm^2/V\text{-}s$, $t_{ox} = 200\ Å$, $W/L = 50$, and $V_T = 0.40\ V$. If the transistor is biased in the saturation region, find the drain current for $V_{GS} = 1, 2$, and $3\ V$.

(Ans. $I_D = 1.01, 7.19$, and $19\ mA$)

EXAMPLE 6.11

OBJECTIVE

Determine the inversion carrier mobility from experimental results.

Consider an n-channel MOSFET with $W = 15\ \mu m$, $L = 2\ \mu m$, and $C_{ox} = 6.9 \times 10^{-8}$ F/cm^2. Assume that the drain current in the nonsaturation region for $V_{DS} = 0.10$ V is $I_D = 35\ \mu A$ at $V_{GS} = 1.5$ V and $I_D = 75\ \mu A$ at $V_{GS} = 2.5$ V.

■ Solution

From Equation (6.58), we can write

$$I_{D2} - I_{D1} = \frac{W \mu_n C_{ox}}{L}(V_{GS2} - V_{GS1})V_{DS}$$

so that

$$75 \times 10^{-6} - 35 \times 10^{-6} = \left(\frac{15}{2}\right)\mu_n(6.9 \times 10^{-8})(2.5 - 1.5)(0.10)$$

which yields

$$\mu_n = 773 \text{ cm}^2/\text{V-s}$$

■ Comment

The mobility of carriers in the inversion layer is less than that in the bulk semiconductor due to the surface scattering effect. We will discuss this effect in the next chapter.

Exercise Problem

EX6.11 Consider the n-channel MOSFET described in Example 6.11. Using the results obtained in the example, determine the threshold voltage of the MOSFET.
(Ans. $V_{TN} = 0.625$ V)

EXAMPLE 6.12

OBJECTIVE

Determine the conduction parameter and current in a p-channel MOSFET.

Consider a p-channel MOSFET with parameters $\mu_p = 300\ \text{cm}^2/\text{V-s}$, $C_{ox} = 6.9 \times 10^{-8}\ \text{F/cm}$, $(W/L) = 10$, and $V_{TP} = -0.65\ \text{V}$. Determine the conduction parameter K_p and find the maximum current at $V_{SG} = 3\ \text{V}$.

■ Solution

We have

$$K_p = \frac{W\mu_p C_{ox}}{2L} = \frac{1}{2}(10)(300)(6.9 \times 10^{-8})$$
$$= 1.04 \times 10^{-4}\ \text{A/V}^2 = 0.104\ \text{mA/V}^2$$

The maximum current occurs when the transistor is biased in the saturation region, or

$$I_D = K_p(V_{SG} + V_{TP})^2 = 0.104[3 + (-0.65)]^2 = 0.574\ \text{mA}$$

■ Comment

The conduction parameter, for a given width-to-length ratio, of a p-channel MOSFET is approximately one-half that of an n-channel MOSFET because of the reduced hole mobility value.

Exercise Problem

EX6.12 The maximum current in a p-channel MOSFET must be $I_D = 0.85\ \text{mA}$ at $V_{SG} = 3\ \text{V}$. If the transistor has the same electrical parameters as given in Example 6.12, determine the required width-to-length ratio of the transistor.

[Ans: $(W/L) = 14.6$]

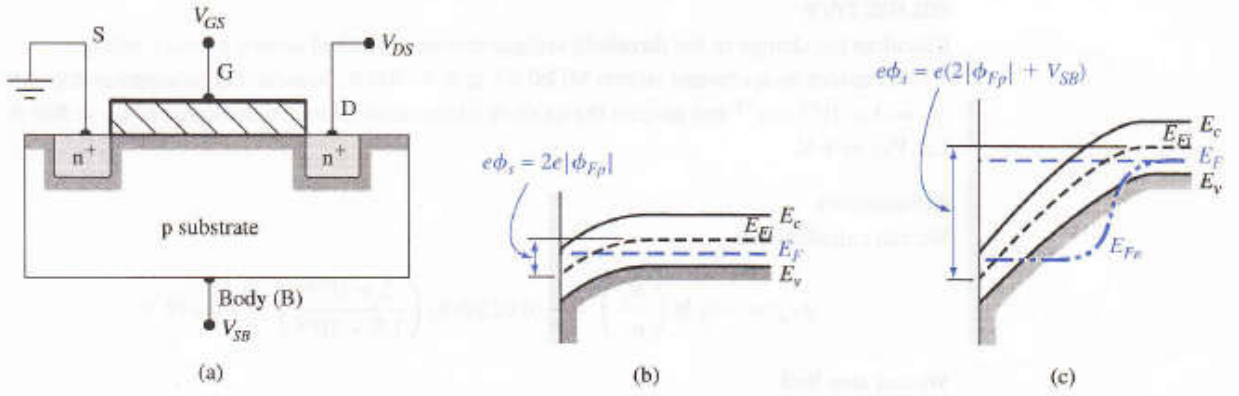


Figure 6.63 | (a) Applied voltages on an n-channel MOSFET. (b) Energy-band diagram at inversion point when $V_{SB} = 0$. (c) Energy-band diagram at inversion point when $V_{SB} > 0$ is applied.

When $V_{SB} = 0$, we had

$$Q'_{SD}(\text{max}) = -eN_a x_{dT} = -\sqrt{2e\epsilon_s N_a(2|\phi_{Fp}|)} \tag{6.84}$$

When $V_{SB} > 0$, the space charge width increases and we now have

$$Q'_{SD} = -eN_a x_d = -\sqrt{2e\epsilon_s N_a(2|\phi_{Fp}| + V_{SB})} \tag{6.85}$$

The change in the space charge density is then

$$\Delta Q'_{SD} = -\sqrt{2e\epsilon_s N_a}\left[\sqrt{2|\phi_{Fp}| + V_{SB}} - \sqrt{2|\phi_{Fp}|}\right] \tag{6.86}$$

To reach the threshold condition, the applied gate voltage must be increased. The change in threshold voltage can be written as

$$\boxed{\Delta V_T = -\frac{\Delta Q'_{SD}}{C_{ox}} = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}}\left[\sqrt{2|\phi_{Fp}| + V_{SB}} - \sqrt{2|\phi_{Fp}|}\right]} \tag{6.87}$$

where $\Delta V_T = V_T(V_{SB} > 0) - V_T(V_{SB} = 0)$. We may note that V_{SB} must always be positive so that, for the n-channel device, ΔV_T is always positive. The threshold voltage of the n-channel MOSFET will increase as a function of the source–substrate junction voltage.

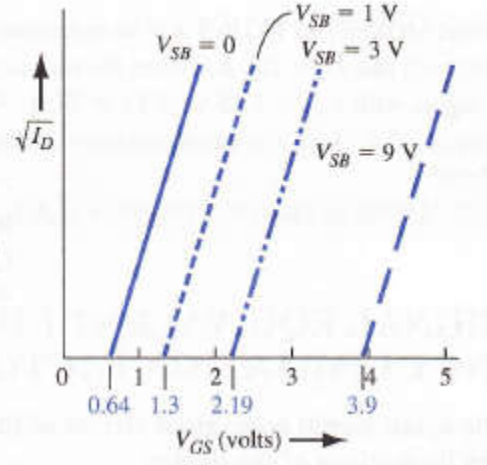


Figure 6.64 | Plots of $\sqrt{I_D}$ versus V_{GS} at several values of V_{SB} for an n-channel MOSFET.

EXAMPLE 6.13

OBJECTIVE

Calculate the change in the threshold voltage due to an applied source-to-body voltage.

Consider an n-channel silicon MOSFET at $T = 300$ K. Assume the substrate is doped to $N_a = 3 \times 10^{16}$ cm^{-3} and assume the oxide is silicon dioxide with a thickness of $t_{ox} = 500$ Å. Let $V_{SB} = 1$ V.

■ Solution

We can calculate that

$$\phi_{Fp} = -V_t \ln\left(\frac{N_a}{n_i}\right) = -(0.0259)\ln\left(\frac{3 \times 10^{16}}{1.5 \times 10^{10}}\right) = -0.376 \text{ V}$$

We can also find

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{500 \times 10^{-8}} = 6.9 \times 10^{-8} \text{ F/cm}^2$$

Then from Equation (6.87), we can obtain

$$\Delta V_T = \frac{[2(1.6 \times 10^{-19})(11.7)(8.85 \times 10^{-14})(3 \times 10^{16})]^{1/2}}{6.9 \times 10^{-8}} \times \{[2(0.376) + 1]^{1/2} - [2(0.376)]^{1/2}\}$$

or

$$\Delta V_T = 1.445(1.324 - 0.867) = 0.66 \text{ V}$$

■ Comment

Figure 6.64 shows plots of $\sqrt{I_D(\text{sat})}$ versus V_{GS} for various values of applied V_{SB}. The original threshold voltage, V_{T0}, is 0.64 V.

Exercise Problem

EX6.13 A silicon MOS device has the following parameters: $N_a = 10^{16}$ cm^{-3} and $t_{ox} = 200$ Å. Calculate (*a*) the body-effect coefficient $\gamma = \sqrt{2e\epsilon_s N_a}/C_{ox}$ and (*b*) the change in threshold voltage for (*i*) $V_{SB} = 1$ V and (*ii*) $V_{SB} = 2$ V.

[Ans. (*a*) $\gamma = 0.333$ V$^{1/2}$, (*b*) (*i*) $\Delta V_T = 0.156$ V, (*ii*) $\Delta V_T = 0.269$ V]

Example 7.1

Determine the total bias current on an IC due to subthreshold currents.

Assume there are 10^7 n-channel transistors on a single chip with a threshold voltage of V_T = 0.5 V, all biased at V_{GS} = 0 V and V_{DS} = 2 V. Assume the subthreshold current $I_{sub} = 10^{-10}$ A for each transistor for this bias condition. What happens to the total bias current on the IC if the threshold voltage is reduced to V_T = 0.25 V, all other parameters remaining the same? [Hint: $I_{sub} \propto \exp\left(\frac{q(V_{GS} - V_T)}{kT}\right)$]

Solution:

The total bias current is the bias current of each transistor times the number of transistors, or

$$I_{Total} = I_{sub} \times 10^7 = 10^{-10} \times 10^7 = 0.001A = 1\,\text{mA}$$

We can write

$$I_{sub} \approx I_0 \exp\left(\frac{q(V_{GS} - V_T)}{kT}\right)$$

So $$10^{-10} = I_0 \exp\left(\frac{0 - 0.5}{0.0259}\right) \quad \Rightarrow \quad I_0 = 0.0242$$

Now, if the threshold voltage changes to V_T = 0.25V, then the subthreshold current at V_{GS} = 0 becomes

$$I_{sub} \approx I_0 \exp\left(\frac{q(V_{GS} - V_T)}{kT}\right) = 0.0242 \times \exp\left(\frac{0 - 0.25}{0.0259}\right) = 1.56 \times 10^{-6}\ \text{A}$$

Now, the total bias current for this IC chip would be

$$I_{Total} = I_{sub} \times 10^7 = 1.56 \times 10^{-6} \times 10^7 = 15.6\ \text{A}$$

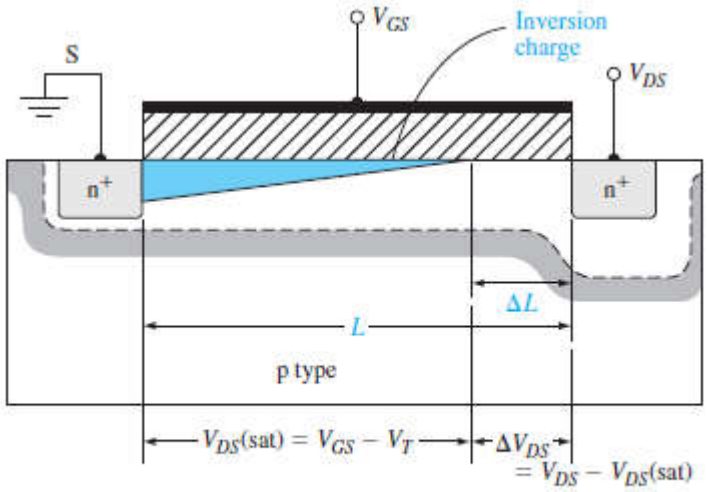


Figure 11.5 | Cross-section of an n-channel MOSFET showing the channel length modulation effect.

ΔL is the total space charge width minus the space charge width that exists when $V_{DS} = V_{DS}(\text{sat})$, or

$$\Delta L = \sqrt{\frac{2\epsilon_s}{eN_a}}\left[\sqrt{\phi_{fp} + V_{DS}(\text{sat}) + \Delta V_{DS}} - \sqrt{\phi_{fp} + V_{DS}(\text{sat})}\right] \qquad (11.4)$$

where

$$\Delta V_{DS} = V_{DS} - V_{DS}(\text{sat}) \qquad (11.5)$$

The applied drain-to-source voltage is V_{DS} and we are assuming that $V_{DS} > V_{DS}(\text{sat})$.

$$I_D' = \left(\frac{L}{L - \Delta L}\right) I_D \qquad (11.11)$$

$$I_D' = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot [(V_{GS} - V_T)^2 (1 + \lambda V_{DS})] \qquad (11.12)$$

Example 7.2

Objective: Determine the increase in drain current due to short channel modulation.

Consider an n-channel MOSFET with a substrate doping concentration of $N_a = 2 \times 10^{16}$ cm^{-3}, a threshold voltage of $V_T = 0.4$ V, and a channel length of $L = 1$ μm. The device is biased at $V_{GS} = 1$ V and $V_{DS} = 2.5$ V. Determine the ratio of actual drain current compared to the ideal value.

■ Solution

We find

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{2 \times 10^{16}}{1.5 \times 10^{10}}\right) = 0.3653 \text{ V}$$

$$V_{DS}(\text{sat}) = V_{GS} - V_T = 1.0 - 0.4 = 0.6 \text{ V}$$

and

$$\Delta V_{DS} = V_{DS} - V_{DS}(\text{sat}) = 2.5 - 0.6 = 1.9 \text{ V}$$

Using Equation (11.4), we determine

$$\Delta L = \sqrt{\frac{2\epsilon_s}{eN_a}}\left[\sqrt{\phi_{fp} + V_{DS}(\text{sat}) + \Delta V_{DS}} - \sqrt{\phi_{fp} + V_{DS}(\text{sat})}\right]$$

$$= \sqrt{\frac{2(11.7)(8.85 \times 10^{-14})}{(1.6 \times 10^{-19})(2 \times 10^{16})}}\left[\sqrt{0.3653 + 0.6 + 1.9} - \sqrt{0.3653 + 0.6}\right]$$

$$= 1.807 \times 10^{-5} \text{ cm}$$

or

$$\Delta L = 0.1807 \ \mu\text{m}$$

Then

$$\frac{I_D'}{I_D} = \frac{L}{L - \Delta L} = \frac{1}{1 - 0.1807} = 1.22$$

■ Comment

The actual drain current increases as the effective channel length decreases when the transistor is biased in the saturation region.

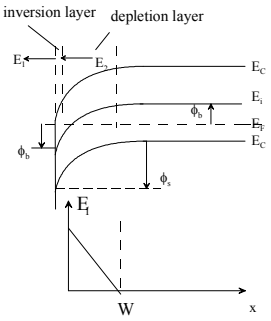
■ EXERCISE PROBLEM

Ex 11.1 An n-channel MOSFET has the same properties as described in Example 11.1 except for the channel length. The transistor is biased at $V_{GS} = 0.8$ V and $V_{DS} = 2.5$ V. Find the minimum channel length such that the ratio of actual drain current to the ideal drain current due to channel length modulation is no larger than 1.35.

(Ans. $0.869 = L$ 'sn$\forall$)

UoL past exam question 1

Draw an energy band diagram of an inverted p type silicon MOS capacitor. Show the Fermi level, indicate the surface potential, and draw a second diagram to indicate the variation of field with distance. Explain briefly for such a device the generation of electron-hole pairs. (11 marks)
Draw a cross-section of a metal oxide semiconductor field-effect transistor labelling the gate, source and drain electrodes. Also label the channel, substrate and indicate the depletion region in the structure. (11 marks)
Explain the symbol for an enhancement type *n* channel device. If the field strength normal to the silicon surface of such a device is $2*10^6 Vcm^{-1}$ estimate the applied gate voltage if the gate dielectric, made of silicon dioxide, has a thickness of 50nm. (11 marks)



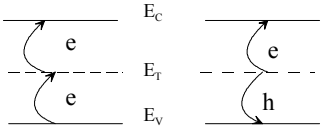


Fig.2

When the surface of silicon is oxidised, in oxygen at high temperatures, a hard uniform layer of silicon dioxide is produced. The uniformity can be controlled down to a few nanometers (nm) in thickness. Capacitors can be made by producing a metal electrode on top of the oxide. The band diagram, with a positive voltage on the metal, is shown in Fig.1. There is a bending of the bands. The fermi level stays flat so that the conduction band approaches it, and the surface becomes n type. The substrate is p type. The n type layer at the surface is called an 'inversion layer'. Behind the inversion layer is depletion region: the fermi level is around mid gap. Such a structure is called an MOS capacitor. With a negative voltage on the metal the layer at the surface consists of positive holes. The capacitance is approximately equal to that of a parallel plate capacitor with a dielectric thickness equal to that of the oxide. With a small positive voltage there will be no inversion layer: the surface will be depleted. With an ac signal applied the outside edge of the depletion layer oscillates, sweeping in and out mobile charge. The effective dielectric thickness is equal to the sum of the thickness of the oxide and the depletion layer. In inversion the capacitance depends on the rate of generation of electrons.

This is because the bulk material is p type, and is very deficient in electrons. The generation occurs in the depletion layer via intermediate levels in the band gap of the silicon. These levels are caused by trace amounts of gold or other heavy metals. In the Fig 2 the generation is shown in two different ways: by the transfer of electrons from the valence band to the conduction band via the traps, or by the alternate generation of an electron and a hole. These descriptions are exactly equivalent. This kind of generation also occurs in pn junctions. It is very important in the context of a wide range of field effect transistors (particularly MOSFETs and thin film transistors).

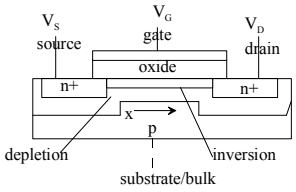
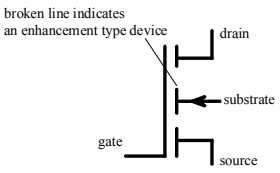


Figure 3 shows the structure of a typical n channel field effect transistor. The gate material may also be made of silicon and there may be a connection to substrate. The source will not always be at zero volts. There may also be an electrical connection to the substrate which may have a bias with respect to the source.

With no substrate connect and a positive gate voltage present which is sufficient to create an inversion layer, there will be conducting channel from source to drain. Generally the gate and drain are both positive and are applied with respect to the source. The positive drain draws the electrons and a channel current flows. Note that the sign of the current is into the drain and from the source.



With the gate-source voltage (V_{GS}) at zero volts there is no channel current. The whole of the drain voltage falls across the drain junction which is reverse biassed by this voltage. Off currents are associated with generation of electron-hole pairs as with the MOS capacitor. These currents are often as low as 10^{-14}A and can for some circuits be

neglected. The symbol for this kind of transistor is shown in Fig.4. The broken line indicates the absence of a conducting channel in the absence of sufficient gate voltage. The connection to the gate is created at the source end of the channel. This indicates which terminal is the source. The arrow points from the substrate which is p type to the n type channel. For a p type channel device the arrow points away from the transistor.

PROBLEM: The continuity of dielectric displacement gives $\varepsilon_S E_S = \varepsilon_{ox} E_{ox} \sim \varepsilon_{ox}(V_G/x_t)$ where V_G is the effective gate voltage.

$$V_G = x_t \varepsilon_S E_S / \varepsilon_{ox} = 5*10^{-10}*12*2*10^8/4 = 30*10^{-2}V = 0.3V$$

UoL past exam question 2

Explain why CMOS is generally preferred to other logic families and mention at least one application where this is not the case. (11 marks)

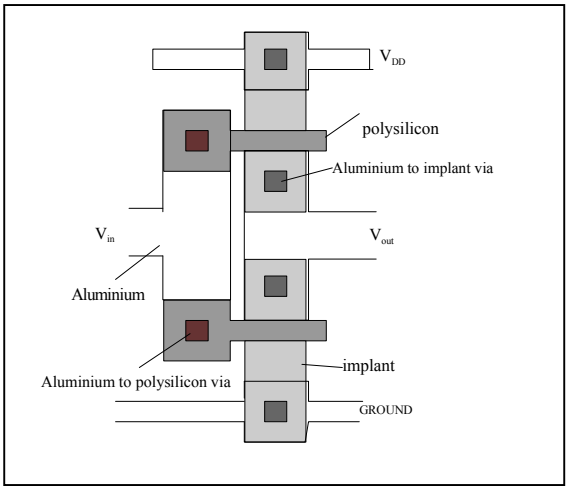
Describe the principles involved in the design and layout of a simple CMOS inverter. (11 marks)

Draw a labelled plan diagram of a CMOS inverter and use it to illustrate the design principles.(11 marks).

SOLUTION

CMOS is a very complex process and has very costly plant and processing. It is preferred although a large throughput is needed to justify such costs. It is particularly good with regard to power dissipation and speed. It eliminates the problem of low current when charging a driver via a high resistance load. It is therefore fast. It is less good for logic when this is complex and the drivers have to be arrayed. The need for a p channel device with every driver makes layout almost impossible.

The CMOS inverter is probably required to drive a second similar inverter or its equivalent. The gates of the n channel and p channel devices are both made with polysilicon and have to be connected together. This requires metal-polysilicon interconnect. The output, V_{DD} and ground lines are in metal because of the need for high conductivity. The two transistors are both drivers so that they would ideally be of the same aspect ratio and size. Because the hole mobility is less than the electron mobility, there is a mismatch in the values of β. A channel lengths or widths have to be changed to compensate. This means that the p channel device may have a wider channel. This is also true of any following inverter so that there is increase in the loading capacitance for the first inverter. The compensation is therefore in complete.



The CMOS system is designed to give a minimal stand-by current. This current can still be large with a large number of gates. This means that there will be a fall of V_{DD} down the rails and hence a reduction in speed.

In the diagram we show the aluminum interconnect between the polysilicon gates but not the compensation for the difference in mobility. The area of the two rails is reduced by making them minimum feature size. Note that the drain of n channel device is not common with the source of the p channel device because one is p^+ and the other is n^+. The circuit could be minimised by reducing the distance between the parallel rails.

UoL past exam question 3

3. a) Describe the structure and fabrication of a Metal Oxide Semiconductor capacitor and draw a band diagram for the operating modes of a p-type device. Explain the surface field effect. **10**

Solution: When the surface of silicon is oxidised, in oxygen at high temperatures, a hard uniform layer of silicon dioxide is produced. The uniformity can be controlled down to a few nanometers (nm) in thickness. Capacitors can be made by producing a metal electrode on top of the oxide (Fig. 1a)).

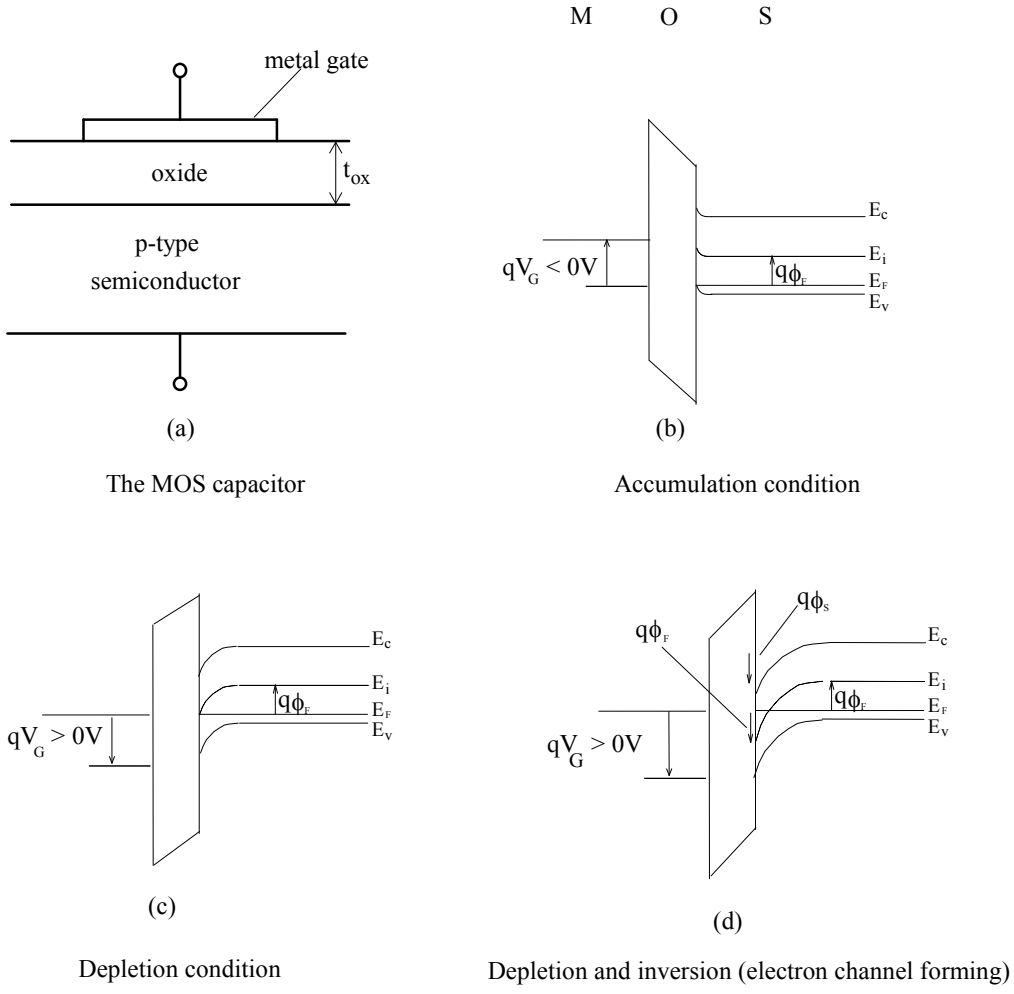


Fig. 1 Energy band diagrams for the operating modes of the p-type MOS-C.

The so called *surface field effect* is central to the understanding and engineering of the silicon dioxide (SiO_2) system and to the operation of the associated MOSFET device. The basic structure which illustrates the principle is the metal oxide semiconductor (MOS) capacitor. We assume first, an ideal system without work function differences or oxide charge.

- If a negative voltage is applied to the metal electrode, positively charged holes will be attracted to the opposite 'plate' of the capacitor formed by the oxide, to satisfy the need for charge neutrality. This *accumulation* condition is shown in Fig. 1b).

- Zero gate voltage gives the so-called 'flat-band' condition.

- Applying a small positive voltage however, will force holes away from the surface leaving a *depletion* region. That is to say, the semiconductor provides the necessary negative charge, with negative acceptor atoms. The energy bands will thus be bent as seen in Fig. 1c). Voltage is dropped across the semiconductor and the potential at the SiO_2/Si interface is referred to as the *surface potential*, ϕ_S. For depletion: $0 < \phi_S < 2\phi_F$.

- If a sufficiently large positive voltage is applied, the energy bands are bent sufficiently to approach the Fermi level and this predicts that the electron concentration is increasing. The surface thus "looks" n-type and is said to be inverted. This *inversion* condition is shown in Fig. 1d). Note that in inversion, the negative charge on that plate of the capacitor is made up of two components: inversion (electrons) and depletion (acceptors) charge. Further increase of voltage, will be satisfied by an increase in the inversion component and the depletion width remains about constant in width. It can be seen that inversion commences when the bands are bent by twice the Fermi potential, that is to say the surface potential is equal to twice the Fermi potential ($\phi_S = 2\phi_F$). For this condition, the minority carrier (electron) concentration at the surface is equal to the majority carrier (hole) concentration in the semiconductor bulk.

  With an ac signal applied, the outside edge of the depletion layer oscillates, sweeping in and out mobile charge. The effective dielectric thickness is equal to the sum of the thickness of the oxide and the depletion layer.

3. b) Define the threshold voltage (V_T) and derive an expression in terms of dimensions of the dielectric, the relative permittivity of gate and substrate materials and substrate doping concentration. **13**

Solution*:* The threshold voltage is the value of gate voltage ($V_G = V_T$) required to invert the semiconductor surface. The threshold voltage, V_T, can be derived for the simple case of a constantly doped substrate. According to the laws of electrostatics, the dielectric displacement (the product of permittivity and electric field) must be continuous across the SiO_2/Si interface, that is

$$\varepsilon_o \varepsilon_{ox} E_{ox} = \varepsilon_o \varepsilon_s E_s . \qquad (1)$$

The implicit assumption in Eq. (1) is that there is no significant amount of charge at the interface so that the semiconductor field is solely due to the acceptors. Therefore an ideal interface is assumed, and also the amount of free carriers is assumed to be very small compared to the charge associated with acceptors. For $\phi_F < \phi_s < 2\phi_F$ this is a very good approximation. Now the oxide field is given by

$$E_{ox} = \frac{V_G - \phi_s}{t_{ox}} \qquad (2)$$

where t_{ox} is the oxide thickness. The semiconductor field, as a function of the voltage across the semiconductor, ϕ_s is given by

$$E_S = \sqrt{\frac{2qN_A\phi_s}{\varepsilon_0 \varepsilon_s}} . \qquad (3)$$

Substituting Eqns. (2) and (3) into (1) gives the relationship between gate voltage and surface potential, ϕ_s:

$$V_G = \frac{\varepsilon_s}{\varepsilon_{ox}} t_{ox} \sqrt{\frac{2qN_A\phi_s}{\varepsilon_0\varepsilon_s}} + \phi_s \cdot \qquad (4)$$

The inversion or threshold voltage is defined as the value of V_G for which surface potential is

$$\phi_s = 2\phi_F = 2V_t \ell n\left[\frac{N_A}{n_i}\right], \qquad (5)$$

which gives requested relation for the threshold voltage:

$$V_T = t_{ox} \frac{\varepsilon_s}{\varepsilon_{ox}} \sqrt{\frac{2qN_A \cdot 2\phi_F}{\varepsilon_0\varepsilon_s}} + 2\phi_F,$$

where ϕ_F is Fermi potential, V_t = kT/q ~ 25 mV at 300K, k is Boltzmann's constant, T is absolute temperature and q is the electronic charge.

Note that the full expression for threshold voltage will take into account also the effects of fixed oxide charge (Q_f), interface (or surface) states (Q_{ss}) and the difference in work function between the metal (or poly-Si) gate and semiconductor (Φ_{MS}).

3. c) Calculate the threshold voltage for a p-type MOS structure if the gate oxide thickness is 20 nm and the substrate doping concentration is $2.5 \cdot 10^{16}$ cm^{-3}. Assume an ideal MOS capacitor and use the simplified formula derived in b) without taking into account oxide charges and work function difference. Comment on the value of threshold voltage if the thickness of the gate oxide decreases and substrate doping concentration increases. **10**

Solution:
For given doping concentration, the value of surface potential is:

$$\phi_s = 2\phi_F = 2V_t \ell n\left[\frac{N_A}{n_i}\right] = \frac{2}{40}\ln\left(\frac{2.5 \cdot 10^{22}}{1.45 \cdot 10^{16}}\right) = 2 \cdot 0.36 = 0.72V$$

The threshold voltage is then:

$$V_T = t_{ox} \frac{\varepsilon_s}{\varepsilon_{ox}} \sqrt{\frac{2qN_A \cdot 2\phi_F}{\varepsilon_0\varepsilon_s}} + 2\phi_F = 20 \cdot 10^{-9} \cdot \frac{11.9}{3.9} \sqrt{\frac{2 \cdot 1.6 \cdot 10^{-19} \cdot 0.72}{8.85 \cdot 10^{-12} \cdot 11.9}} + 0.72 = 1.17V \cdot$$

Since an approximate formula for threshold voltage is:

$$V_T \propto t_{ox}\sqrt{N_A}$$

it is evident that decrease of the gate oxide thickness will reduce V_T so the substrate doping can be increased for the same value of V_T.

UoL past exam question 4

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4. a) Explain the operation of a CMOS (Complementary Metal Oxide Semiconductor) inverter and state its main advantages and disadvantages. **8**

Solution:
(Detailed solution is given; students are expected to present key concepts/equations next to the points below)

The pMOS transistor is connected between V_{DD} and the output node, V_{out}, whereas the nMOS is connected between the output node, V_{out}, and the ground, GND. Also, the p-channel transistor has its source, substrate and V_{DD} connected, while the n-channel has its source, substrate and ground line connected. The structure of CMOS is symmetrical, each device having an equal and opposite effect.

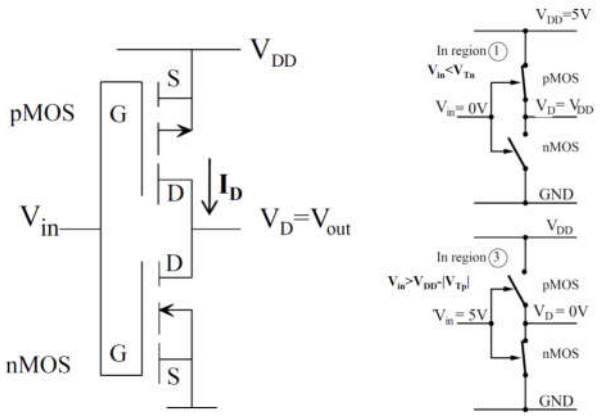


Fig. 4 A schematic of CMOS circuit and its operation as inverter. **(2pts)**

The principle of operation is as follows (refer also to the right part of Fig. 4): **(2pts)**

- for small values of the input voltage, ($V_{in}<V_{Tn}$, V_{Tn} – the threshold voltage for nMOST), the nMOS transistor is switched off, whereas the p channel transistor is *hard on* since the gate is negative with respect to V_{DD} ($V_{GSp}=V_G-V_{DD}<-V_{Tp}$, V_{Tp} is the threshold voltage of pMOST and it is negative so that the p-channel can be formed). As pMOST is switched on, it connects the output to V_{DD}, which refers to logic 1.
- for large values of the input voltage, $V_{in}>V_{DD}-|V_{Tp}|$, the pMOST is switched off, whereas the n-channel device is hard on (since $V_{in}>V_{Tn}$), and connects the output to GND = 0V, which refers to logic 0.

Advantages over other nMOS inverter configurations:

1. The steady-state power dissipation of the CMOS inverter is virtually negligible, except for small power dissipation due to leakage currents. **(1pts)**
2. The voltage transfer characteristics (V_{out} vs. V_{in}) exhibits a full output voltage swing between 0V and V_{DD}, and this transition is usually very sharp; the transfer characteristic resembles that of an ideal inverter. **(1pts)**

The key disadvantages are:

1. The CMOS process is more complex than the standard nMOS-only process as nMOS and pMOS transistors must be fabricated on the same chip side-by-side. This can be achieved by fabricating either n-type wells on a p-type wafer, or p-type wells on an n-type wafer. **(1pts)**

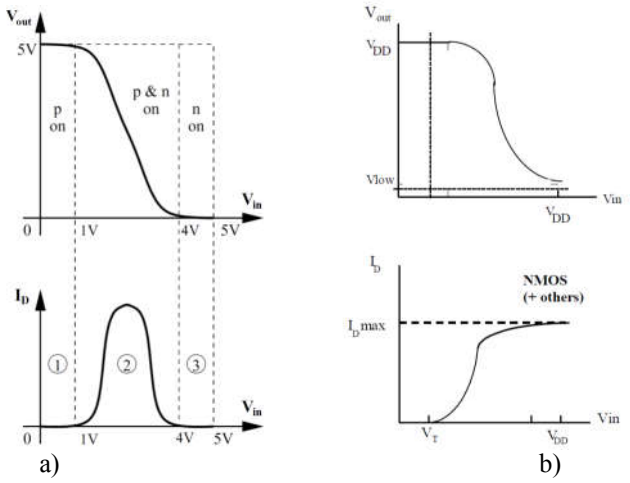
2. The close proximity of an nMOS and a pMOS transistor may lead to the formation of two parasitic bipolar transistors, causing a latch-up condition. This adds to complexity as additional guard rings must be built around the nMOS and pMOSTs. **(1pts)**

---

4. b) Is CMOS a ratioless or ratioed logic circuit? Explain your reasoning with the aid of diagrams. **8**

Solution:

For the nMOS inverters (Fig. 5b), $V_{oL} = V_{low}$ (low level of the output voltage or level of logic 0 at the output) is not zero, but depends on the ratio of the device constants of driver and load transistors $\beta_{driver}/\beta_{load}$. Such circuits are known as *ratioed* logic circuits. On the other hand, CMOS logic circuits do not have such a dependency (the output voltage swings from almost 0 to V_{DD}) (Fig. 5a) and are called *ratioless.* **(4pts)**



a) b) **(4pts)**

Fig. 5 An illustration of transfer and current characteristics for a) CMOS and b) nMOSFET inverters.

---

4. c) State the necessary condition to design a symmetrical inverter and derive the relationship between aspect ratios (width/length) for p- and n-MOSFET transistors for this case. Assume that threshold voltages for p- and n-MOSFETs are equal. **8**

Solution:

In order to build a symmetrical inverter the midpoint of the transfer characteristic must be centrally located, that is,

$$V_{in} = \frac{1}{2} V_{DD} = V_{out}. \qquad (1) \qquad \textbf{(2pts)}$$

For this condition both transistors are expected to work in the saturation mode. For transistor in saturation, $I_D = \frac{\beta}{2}(V_G - V_T)^2$), then:

$$I_{Dn} = I_{Dp} = \frac{\beta_n}{2}(\frac{V_{DD}}{2} - V_{Tn})^2 \equiv \frac{\beta_p}{2}(\frac{V_{DD}}{2} - V_{Tp})^2 . \qquad (2) \qquad \textbf{(2pts)}$$

If the threshold voltages are equal, the above condition for a symmetrical inverter is reduced to the condition of equality of their device constants $\beta_n = \beta_p$. (3) **(1pts)**

Hence:

$$\mu_n C_o(\frac{W}{L})_n = \mu_p C_o(\frac{W}{L})_p \qquad (\frac{W}{L})_p = \frac{\mu_n}{\mu_p}(\frac{W}{L})_n \approx 2.5(\frac{W}{L})_n \qquad (4) \qquad \textbf{(2pts)}$$

Therefore, in order to preserve symmetry of input/output voltages, the pMOS transistor should be 2.5 times wider than the nMOS of the same length. This ratio is the result of different mobility of positive and negative carriers as $\mu_n \sim 2.5\mu_p$ typically. **(1pts)**

---

4. d) Calculate the ratio $(W/L)_{pMOSFET}$ / $(W/L)_{nMOSFET}$ required to design a symmetric CMOS inverter. Assume the mobilities of electron and holes of μ_n = 545 cm^2/Vs and μ_p = 130 cm^2/Vs respectively, the threshold voltages for p- and n-MOSFETs equal to $V_{Tn} = |V_{Tp}| = 0.8$ V, and $V_{DD} = 3$ V. **9**

Solution:

The threshold voltage of the CMOS inverter is defined as voltage when $V_{TH}=V_{in}=V_{out}$. **(1pts)**

Looking at the transfer characteristics, this will be the case when $V_{in}=V_{DD}/2$, when both transistors (nMOST and pMOST) work in saturation. By equating the drain currents, the threshold voltage of the inverter is found as:

$$I_{Dn} = I_{Dp}$$

$$I_{Dn} = \frac{\mu_n C_o}{2}(\frac{W}{L})_n (V_{TH} - V_{Tn})^2 \equiv I_{Dp} = \frac{\mu_p C_o}{2}(\frac{W}{L})_p (V_{DD} - V_{TH} + V_{Tp})^2$$

$$\Rightarrow$$

$$V_{TH} = \frac{V_{Tn} + (V_{DD} - V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{(W/L)_p}{(W/L)_n}}\mu_n}{1 + \sqrt{\frac{\mu_p}{\mu_n}\frac{(W/L)_p}{(W/L)_n}}} \qquad \textbf{(3pts)}$$

The ratio $(W/L)_{pMOSFET}$ / $(W/L)_{nMOSFET}$ is then given as

$$\frac{(W/L)_p}{(W/L)_n} = \frac{(V_{TH} - V_{Tn})^2}{\frac{\mu_p}{\mu_n}(V_{DD} - V_{Tp} - V_{TH})^2} \qquad \textbf{(3pts)}$$

Since $V_{TH}=V_{DD}/2=1.5$V, then

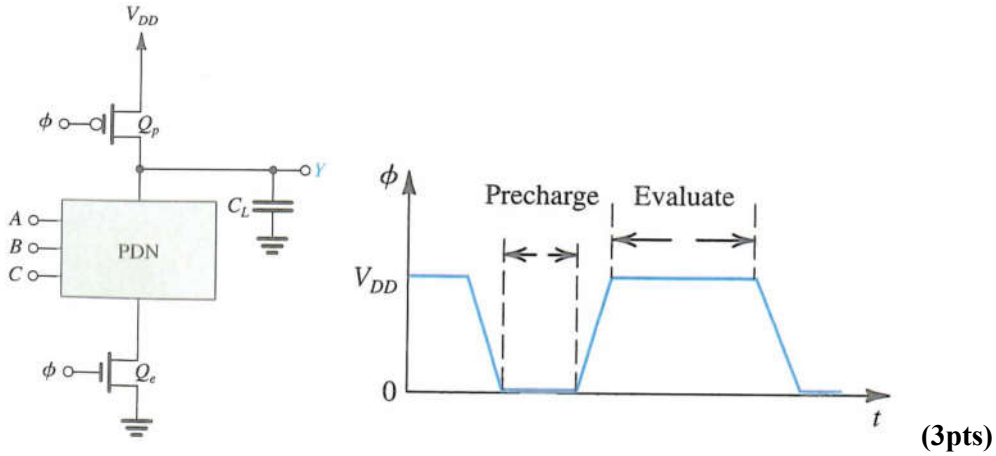
$$\frac{(W/L)_p}{(W/L)_n} = \frac{(1.5 - 0.8)^2}{\frac{130}{545}(3 - 0.8 - 1.5)^2} = 4.2 \qquad \textbf{(2pts)}$$

UoL past exam question 5

5. a) Describe the operation of a basic dynamic logic circuit with the aid of diagrams. What is the main difference between dynamic and static logic circuits? **14**

Solution:
(Detailed solution is given; students are expected to present key concepts next to the points below)

The basic dynamic-logic gate consists of a pull-down network (PDN) that realizes the logic function in exactly the same way as the PDN of a CMOS gate or a pseudo-nMOS gate. Here, however, there are two switches in series that are periodically operated by the clock signal ϕ whose waveform is shown in Fig. 6b. When ϕ is low, Q_p is turned on, and the circuit is said to be in the setup or *precharge phase*. When ϕ is high, Q_p is off and Q_e turns on, and the circuit is in the *evaluation phase*. Note that C_L denotes the total capacitance between the output node and ground. **(5pts)**



(3pts)

Fig. 6 a) Basic structure of dynamic-MOS logic circuit; b) waveform of the clock needed to operate the dynamic logic circuit.

During precharge, Q_p conducts and charges capacitance C_L so that, at the end of the precharge interval, the voltage at Y is equal to V_{DD}. Also during precharge, the inputs A, B and C are allowed to change and settle to their proper values. Observe that because Q_e is off, no path to ground exists.

During the evaluation phase, Q_p is off and Q_e is turned on. Now, if the input combination is one that corresponds to a high output, the PDN does not conduct (just as in a CMOS gate) and the output remains high at V_{DD}, thus $V_{oH}=V_{DD}$. Observe that *no low-to-high propagation delay is required*, thus $t_{PLH}=t_{rise}=0$. On the other hand, if the combination of inputs is one that corresponds to a low output, the appropriate nMOSTs in the PDN will conduct and establish a path between the output node and ground through the on transistor Q_e. Thus C_L will discharge through the PDN, and the voltage at the output node will reduce to $V_{oL}=0V$. The high-to-low propagation delay ($t_{pHL}=t_{fall}$) can be calculated from transient analysis taking into account an additional transistor Q_e in the series path to ground. This will increase the delay slightly; however note the reduction of capacitance at the output node as a result of the absence of the PUN (pull-up network). **(4pts)**

In a static logic circuit, every node has, at all times, a low-resistance path to V_{DD} or ground. In the same time, the voltage of each node is well defined at all times, and no node is left floating. Static circuits do not need *clocks* (i.e. *periodic timing signals*) for their operation, although clocks may be present for other purposes. In contrast, the *dynamic logic circuits rely on the storage of signal voltages on parasitic capacitances at certain circuit nodes*. Since charge will leak away with time, the circuits need to be periodically refreshed; thus the presence of a clock with a certain specified minimum frequency is essential. **(3pts)**

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5. b) State the key design considerations for this dynamic logic circuit. **5**

Solution:

Sizing of the PDN transistors follows the same procedure employed in the design of static CMOS. For Q_p, a (W/L) ratio is selected to be large enough to ensure that C_L will be fully charged during the precharge interval. Moreover, the size Q_p should be small so that the C_L will not be increased significantly. This is a *ratioless* form of MOS logic, where the output levels do not depend on the transistors' W/L ratios.

---

5. c) Discuss with the aid of circuit diagrams the stages in the development from the pseudo nMOS to domino logic gates. Briefly describe the operation of each of the circuit. **14**

Solution:

Development stages of CMOS digital circuits is illustrated in Fig.7, starting from a) a pseudo-nMOS inverter to e) domino CMOS logic gate.
A pseudo-nMOS inverter design (Fig. 7a) reduces the number of required transistors by using a suitable sized pMOST as load with its gate connected to ground. The problem of this circuit is increased static power dissipation.

(2pts)

A further improvement of this circuit involves operating the pMOST in a dynamic mode. The word 'dynamic' involves charging the gate of the pMOST prior to the arrival of a signal to driver (Fig. 7b). The charge is stored on the gate of the pMOS but gradually leaks away probably via the drain of an off transistor that originally delivered the charge in the first place. It minimises the power dissipation associated with a pMOST that is permanently hard on. **(2pts)**

The circuit of Fig. 7b is a simple example: in general there may well be a large number of nMOS devices in parallel (NOR configuration) each with a separate input as shown in Fig. 7c. This n channel driver network is the basis of the 'finite state machine' which can do very complex logic functions in an efficient way. **(1pts)**

In order to minimise current flow during the pre-charge time, and hence limit power dissipation, an additional nMOST can be added as in Fig. 7d. This is also operated by the pulse labelled PR (clock signal), but it switches off the current to ground through the n channel driver network. **(2pts)**

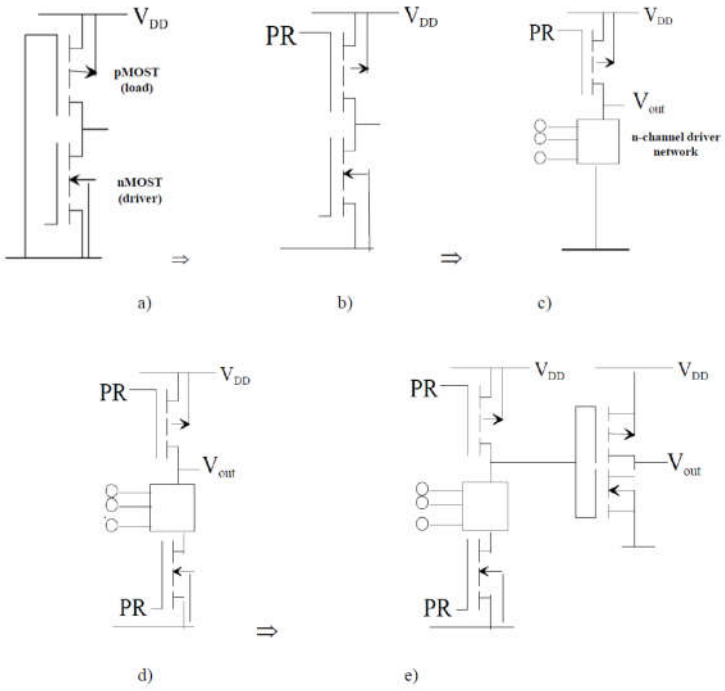

Fig. 7 **(5pts)**

Addition of a CMOS inverter leads to Domino Logic, in Fig. 7e. A whole series of domino type gates may be cascaded. By precharging them all it is possible to have a change in output as the first that ripples through the rest of the domino-type gates. Complications can arise with such an arrangement, however, because of the loading on the second by the first, the third by the second etc. As a way of isolating the gates it is important to include this standard CMOS inverter. It may seem to be a paradox to introduce new ideas to overcome disadvantage of CMOS only to reintroduce a CMOS inverter at a later stage, but it works. **(2pts)**

The array of NOR gates would require a large number of p channel devices if it was done in CMOS whereas using the single precharged pMOSFET greatly simplifies design.

UoL past exam question 6

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6. a) Define briefly intrinsic and extrinsic semiconductors. State the mass action law for semiconductors. **(8pts)**

Solution:

The intrinsic material is an undoped material, where the equilibrium number of electrons, n, and holes, p, are the same; at a given temperature, T:

$$n_0 = p_0 = n_i = const. \qquad (1) \qquad \textbf{(2pts)}$$

The constant in equation (1) is the so-called *intrinsic carrier concentration,* which is denoted as n_i:

$$n_i^2 = N_c N_v \exp(-\frac{E_g}{k_B T}) \qquad (2)$$

where k_B is the Boltzmann constant, Nc- the effective density of available states in the conduction band (N_c) and in the valence band (N_v); E_g- the forbidden energy gap. It follows that

$$n_0 p_0 = n_i^2. \qquad (3) \qquad \textbf{(4pts)}$$

This is the so-called *mass action law* for semiconductors.
The extrinsic semiconductors are doped msterials, either with elements from group V or III of periodic system, so that the conductivity of intrinsic silicon is greatly enhanced due to additional electrons (n-type) in conduction band or holes in the valence band (p-type). **(2pts)**

---

6. b) Calculate the resistivity of intrinsic and extrinsic silicon if the latter is doped by phosphorus to concentration of $2 \cdot 10^{17}$ cm^{-3}. The mobility of electrons is 0.15 $m^2V^{-1}s^{-1}$ and of holes 0.05 $m^2V^{-1}s^{-1}$. Is the extrinsic silicon p- or n-type semiconductor? **(7pts)**

Solution:

Since $n_0 = p_0 = n_i = const$, then $\rho = \frac{1}{\sigma} = \frac{1}{q(\mu_e n_0 + \mu_h p_0)} = \frac{1}{q n_i (\mu_e + \mu_h)} = 2.2 \cdot 10^3 \Omega m$, **(3pts)**

which is clearly a large value and means that intrinsic Si is quite a poor conductor of electricity (0.46×10^{-3} $(\Omega m)^{-1}$) at room temperature.

When doped with phosphorus $\rho = \frac{1}{\sigma} = \frac{1}{q \mu_e N_d} = \frac{1}{1.6 \cdot 10^{-19} \cdot 0.15 \cdot 2 \cdot 10^{23}} = 0.21 \cdot 10^{-3} \Omega m$, **(3pts)**

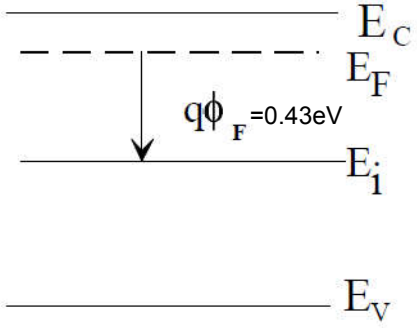
so, the conductivity is significantly increased (i.e. 4.8 $(k\Omega m)^{-1}$). **(1pt)**

6. c) Calculate the Fermi potential for extrinsic semiconductor in b). Illustrate the value with the aid of energy band diagram. **(5pts)**

Solution:

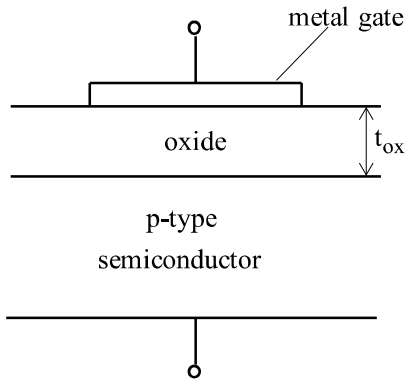
$$\phi_F = \frac{kT}{q}\ln(\frac{N_D}{n_i}) = 0.026\ln(2\cdot 10^{17}/1.45\cdot 10^{10}) = 0.427eV \approx 0.43eV$$

The energy band diagram:



6. d) Describe the additions that are needed to the extrinsic semiconductor in b) to fabricate an MOS capacitor. Explain the surface field effect. **(7pts)**

Solution:



(3pts)

An MOS capacitor is made by depositing oxide on top of p-Si, and then producing a metal electrode on top of the oxide as illustrated in figure above. The so called *surface field effect* is central to the understanding and engineering of the silicon dioxide (SiO_2) system and to the operation of the associated MOSFET device.

Applying a small positive voltage will force holes away from the surface leaving a *depletion* region. That is to say, the semiconductor provides the necessary negative charge, with negative acceptor atoms. Voltage is dropped across the semiconductor and the potential at the SiO_2/Si interface is referred to as the *surface potential*, ϕ_S. For depletion: $0 < \phi_S < 2\phi_F$. **(2pts)**

If a sufficiently large positive voltage is applied, the energy bands are bent sufficiently to approach the Fermi level and this predicts that the electron concentration is increasing. The surface thus "looks" n-type and is said to be inverted. Note that in inversion, the negative charge on that plate of the capacitor is made up of two components: inversion (electrons) and depletion (acceptors) charge. Further increase of voltage, will be satisfied by an increase in the inversion component and the depletion width remains about constant in width. The inversion commences when the bands are bent by twice the Fermi potential, that is to say the surface potential is equal to twice the Fermi potential ($\phi_S = 2\phi_F$). For this condition, the minority carrier (electron) concentration at the surface is equal to the majority carrier (hole) concentration in the semiconductor bulk. **(2pts)**

---

6. e) Calculate the semiconductor field for MOS capacitor structure in d) under strong inversion condition and assuming uniformly doped silicon. **(7pts)**

Solution:

$$\phi_F = \frac{kT}{q}\ln(\frac{N_D}{n_i}) = 0.026\ln(2\cdot 10^{17}/1.45\cdot 10^{10}) = 0.427eV \approx 0.43eV$$ **(2pts)**

$\phi s = 2\phi_F = 0.86$ eV (strong inversion condition) **(2pts)**

$$E_S = \frac{qN_A x_d}{\varepsilon_0 \varepsilon_s}$$
$$= \sqrt{\frac{2qN_A\phi_s}{\varepsilon_0\varepsilon_s}} = \sqrt{\frac{2\cdot 1.6\cdot 10^{-19}\cdot 2\cdot 10^{23}\cdot 0.86}{8.85\cdot 10^{-12}\cdot 11.9}} = 2.3\cdot 10^7 V/m$$ **(3pts)**

UoL past exam question 7

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7. a) Derive an expression for the current flowing down the channel of an n-MOSFET (Metal Oxide Semiconductor Field Effect Transistor) in terms of the gate and threshold voltages, in the saturation region (above 'pinch off'):

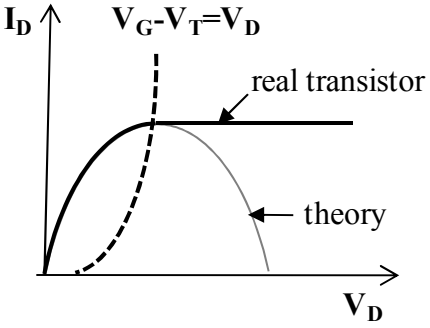
$$I_D = \mu C_o \frac{W}{2L}(V_G - V_T)^2 .$$ **(12pts)**

Solution:

(Detailed solution is given; students are expected to present key concepts/equations next to the points below)

For higher values of drain voltage, V_D ($V_D > V_G$, for nMOSFET), the equation

$$I_D = \mu C_o \frac{W}{L}[(V_G - V_T)V_D - \frac{V_D^2}{2}] \quad (1) \qquad \textbf{(2pts)}$$



needs to be modified. The peak of the parabola in figure on the left corresponds to the maximum current which then becomes independent of V_D. The current at the peak is determined by differentiating with respect to V_D and finding the maximum where the differential becomes zero:

$$\frac{dI_D}{dV_D} = \mu C_o \frac{W}{L}[(V_G - V_T) - V_D] \equiv 0 .$$ **(2pts)**

(2pts)

It is evident that dI_D/dV_D goes to zero for V_G-V_T=V_D which gives the locus of the pinch-off point. When substituted back into Eq. (1):

$$I_D = \mu C_o \frac{W}{2L}(V_G - V_T)^2 \qquad (2) \qquad \textbf{(5pts)}$$

which is called the *above 'pinch-off equation'*. Strictly speaking equation (2) only applies for V_G-V_T=V_D, but practically the electrical characteristic almost saturates above this point so that the equation is more generally applicable for *larger values of V_D*. The lower current part fits the below pinch condition (1), the higher flatter portion approximately obeys (2). The dividing line is (V_G-V_T)=V_D, which defines the pinch-off point on each of the characteristics.

(1pt)

---

7. b) Define the device constant in the equation in a). Which parameters can a designer vary and why? **(4pts)**

Solution: The quantity $\beta = \mu C_o \frac{W}{L}$ (where μ is the average carrier mobility, Co – gate oxide capacitance, W – width and L –length of the channel) is the drive or *device constant*. The designer can only vary W/L to change β. Other values are fixed during the process development.

7. c) Explain the meaning of the 'pinch-off' condition with the aid of a labelled cross-section of an n-MOSFET showing the channel and other regions. **(7pts)**

Solution:

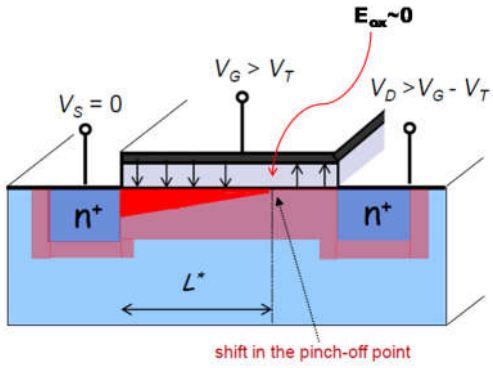


Fig. 1 The pinch-off for n-MOST. **(4pts)**

The pinch-off point in the channel corresponds to the edge of the drain depletion layer which, with increasing V_D extends down the channel, reducing its length (Fig. 1). The distribution of field across the channel is shown with black arrows in Fig. 1; the point of pinch-off refers to zero field. **(2pts)**

The rise in current above pinch-off is due to the reduction of L in equation $I_D = \mu C_o \frac{W}{2L}(V_G - V_T)^2$. **(1pts)**

7. d) The n-MOSFET in a) is fabricated in p-type silicon semiconductor substrate doped to $4 \cdot 10^{15}$ cm^{-3}, and has a threshold voltage of $V_T = 0.7$ V. Estimate the strength of the electric field in the gate dielectric at the threshold voltage, if the gate oxide thickness is 5 nm. **(5pts)**

Solution:

When the gate bias at n-MOSFET is equal to threshold voltage, the surface potential is given as twice Fermi potential (inversion condition), i.e.

$$\phi_s = 2\phi_F = 2V_t \ell n\left[\frac{N_A}{n_i}\right] =$$

$$= 2\frac{1.38 \cdot 10^{-23} \cdot 300}{1.6 \cdot 10^{-19}} \ln\left(\frac{4 \cdot 10^{15}}{1.45 \cdot 10^{10}}\right) = \quad \textbf{(2pts)}$$

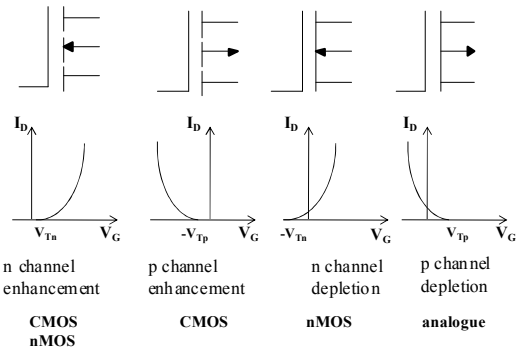
$$= 2 \cdot 0.324 = 0.648V$$

$$\sim 0.65V$$

Then, the oxide field is given as $E_{ox} = \frac{V_G - \phi_s}{t_{ox}} = \frac{0.7 - 0.65}{5 \cdot 10^{-9}} = 1 \cdot 10^7 V/m$. **(3pts)**

7. e) Explain the difference between enhancement and depletion type of MOSFETs. Sketch the symbols and transfer characteristics of these two types of devices for p- and n-channel transistors. **(5pts)**

Solution:



An *enhancement device* is one where a gate voltage is needed to form a channel. A *depletion device* is one where there is already a channel formed and it requires a gate voltage to turn it off. The symbols for n- and p-type MOST for both enhancement/depletion devices with corresponding transfer characteristics are shown in fig. on the left. Typical application for CMOS, nMOS and analogue circuits is outlined below each type of device.

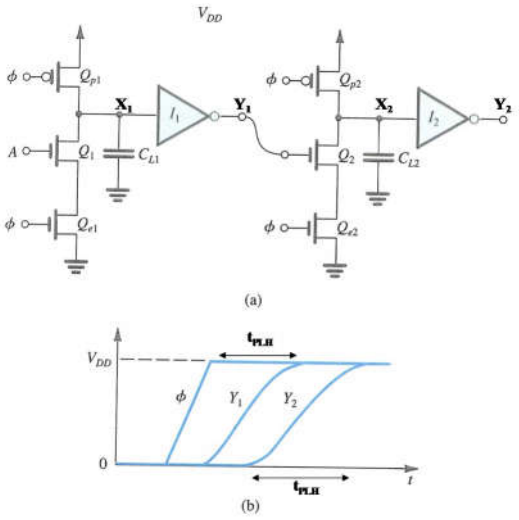
---

8. c) Explain in more detail the operation of domino logic. Draw the voltage waveforms during the evaluation phase for two single-input domino CMOS logic gates connected in cascade. **(10p)**

Solution: *(Detailed solution is given; students are expected to present key concepts next to the points below)*

At the end of precharge, X_1 will be at V_{DD}, Y_1 will be at 0V, X_2 will be at V_{DD}, and Y_2 will be at 0V. Assume A is high at the beginning of evaluation. Thus as ϕ goes up, capacitor C_{L1} will begin discharging, pulling X_1 down. Meanwhile, the low input at the gate of Q_2 keeps Q_2 off, and C_{L2} remains fully charged. When V_{X1} falls below the threshold voltage of inverter I_1, Y_1 will go up turning Q_2 on, which in turn begins to discharge C_{L2} and pulls V_{X2} low. Eventually, Y_2 rises to V_{DD}. **(2pts)**

It is clear that because the output of the domino gate is low at the beginning of evaluation, no premature capacitor discharge will occur in the subsequent gate in the cascade. As indicated in Fig. Q4.3b, output Y_1 will make a 0-to-1 transition $t_{PLH}=t_{rise}$ seconds after the rising edge of the clock. Subsequently, output Y_2 makes a 0-to-1 transition after another $t_{PLH}=t_{rise}$ interval. The propagation of the rising edge through a cascade of gates resembles closely placed dominos falling over, each toppling the next, which is the origin of the name *domino CMOS logic*. **(3pts)**



(5pts)

Fig. Q4.3 a) Two single-input domino CMOS logic gates connected in cascade;
b) waveforms during the evaluation phase.