IC Fab.Tech. OUTLINE

- Thin Film Formation
- Photolithography and Ecthing
- Doping
- **IC Resistor**
- **Sheet Resistance** 方块电阻
- **Diode**
- nMOSFET: Process Flow
- nMOSFET: Fab. and Layout
- nMOSFET: Layout Rules

IC Fabrication Techniques

OUTLINE

- **IC Resistor**
- Sheet Resistance
- Diode

Reference Reading

- **Chapter 5 + Handout + www**

Process Flow Example #1: Resistor

< 10μm x 1μm

(10^{-7} cm^2)

Integrated R

（集成电阻）

~1cm x 1mm

(10^{-1} cm^{-2})

Discrete R (离散电阻)

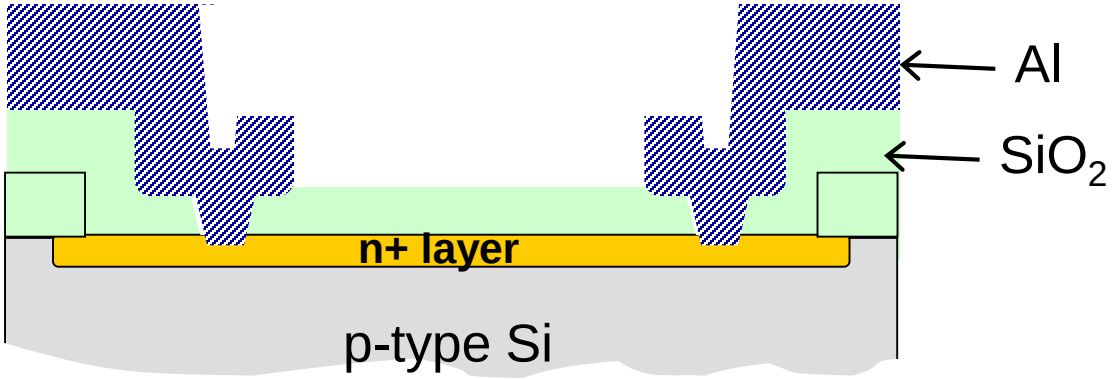
Process Flow Example #1: Resistor

< 10μm x 1μm

(10^{-7} cm^2)

Integrated R

（集成电阻）



~1cm x 1mm

(10^{-1} cm^{-2})

Discrete R (离散电阻)

Process Flow Example #1: Resistor

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(10^{-7} cm^2)

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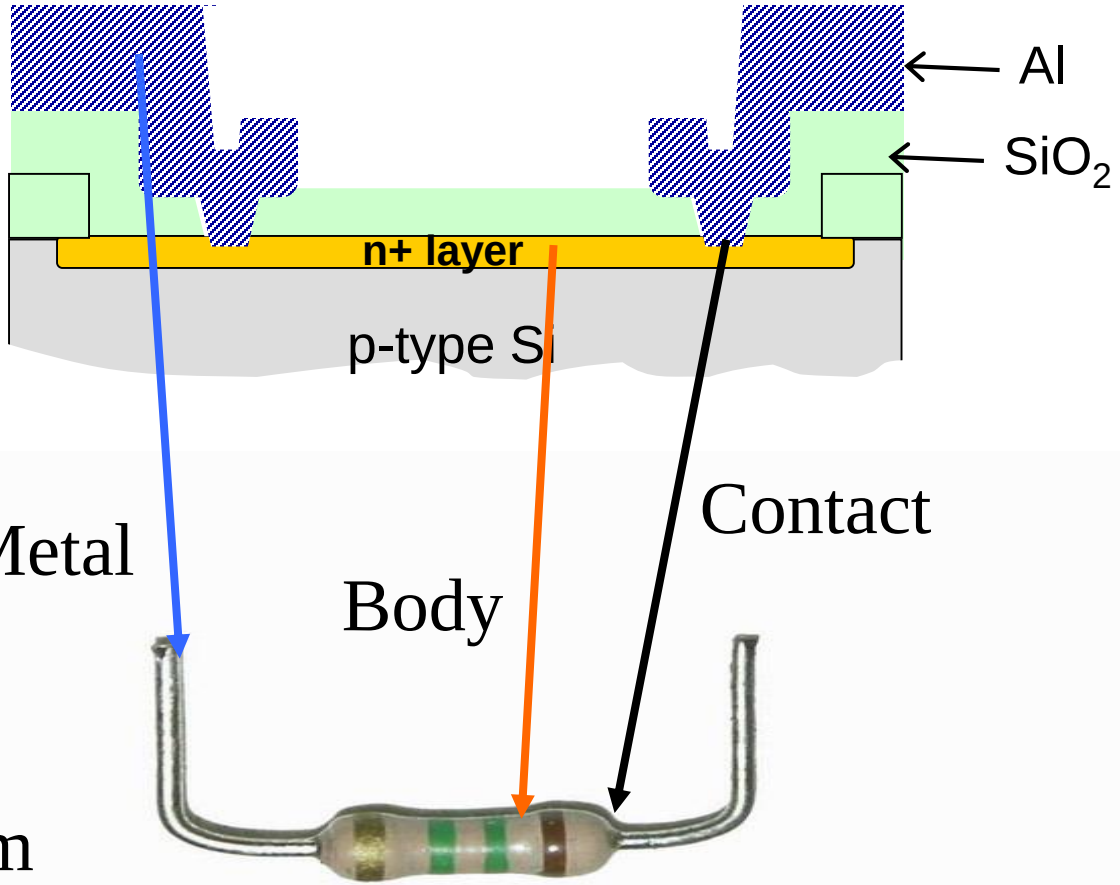
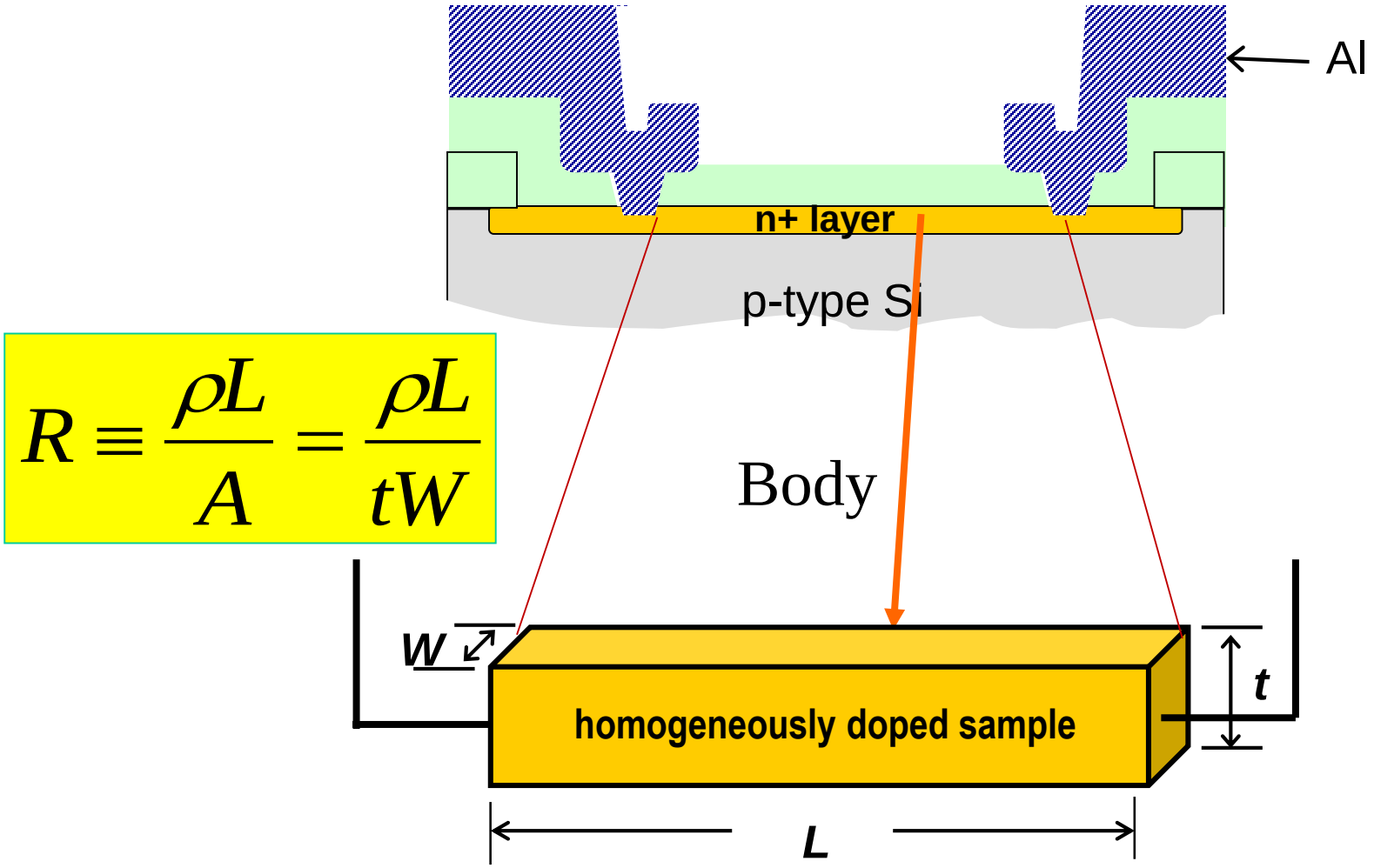


~1cm x 1mm

(10^{-1} cm^{-2})

Discrete R (离散电阻)

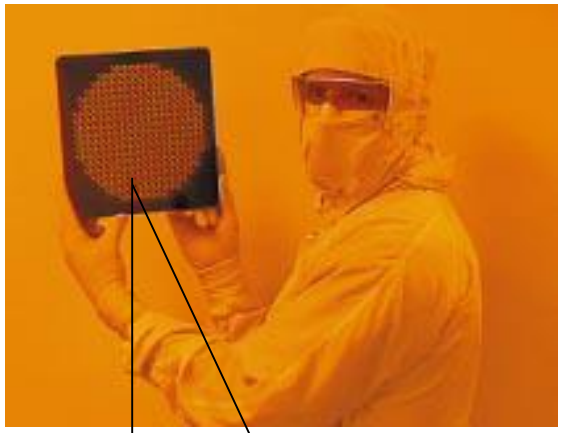
Process Flow Example #1: Resistor

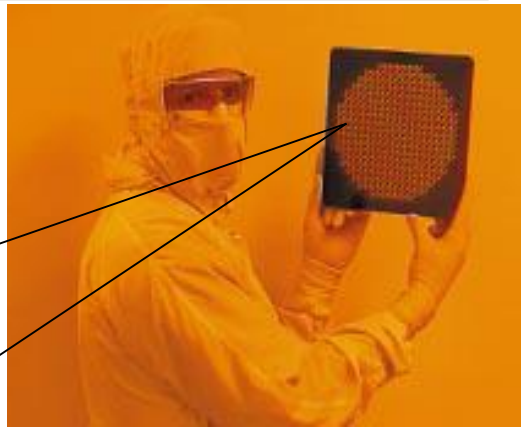


$$R \equiv \frac{\rho L}{A} = \frac{\rho L}{tW}$$

Process Flow Example #1: Resistor

3 mask3





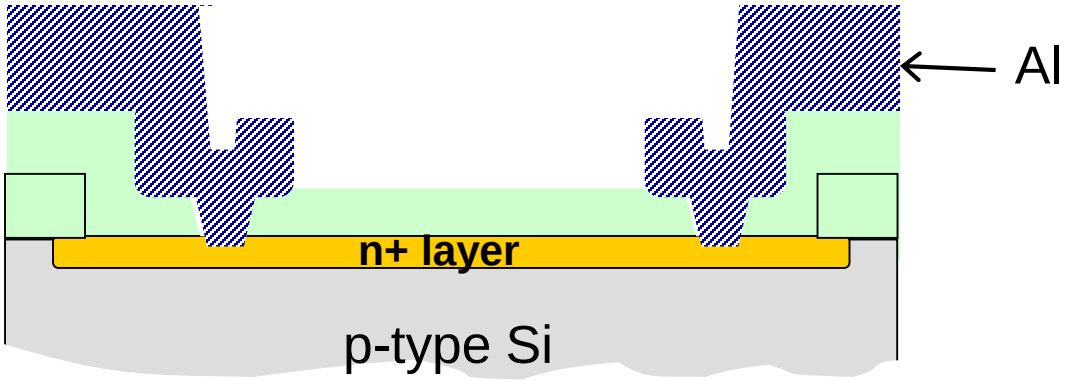
Mask 1 for "body"

Mask 3 for "metal"

Mask 2 for "contact"

Process Flow Example #1: Resistor

A -- A

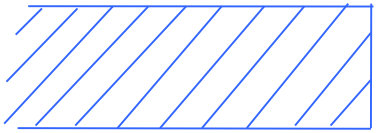


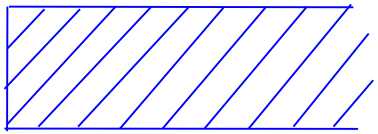
Layout:

negative resist

Oxide mask (dark field)
or Active mask

Contact mask (dark field)



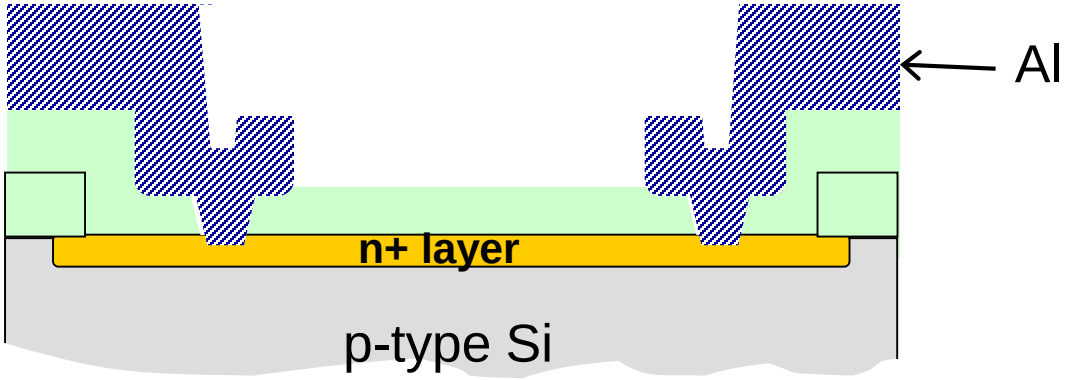


Al mask (clear field)

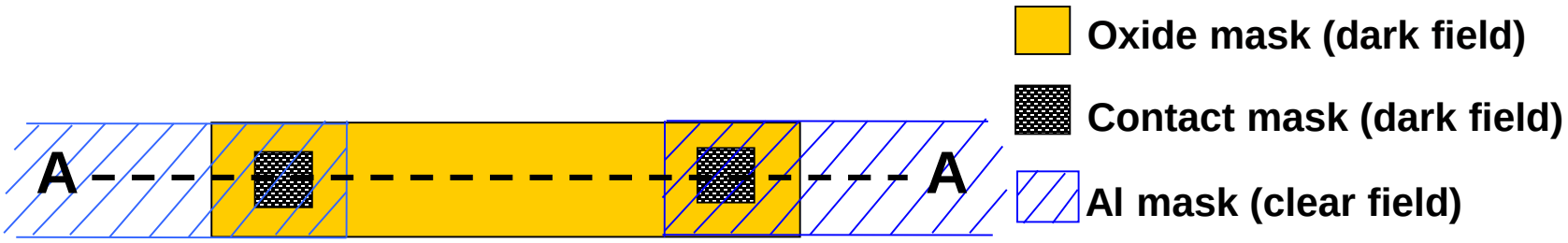
positive resist

Process Flow Example #1: Resistor

A -- A



Patterns transfer to wafer:



Process Flow Example #1: Resistor

Three-mask process:

Starting material: p-type wafer with $N_A = 10^{16}$ cm^{-3}

Step 1: grow 500 nm of SiO_2

Step 2: pattern oxide using the oxide mask (dark field)

Step 3: implant phosphorus and anneal to form an n-type layer with $N_D = 10^{20}$ cm^{-3} and depth 100 nm

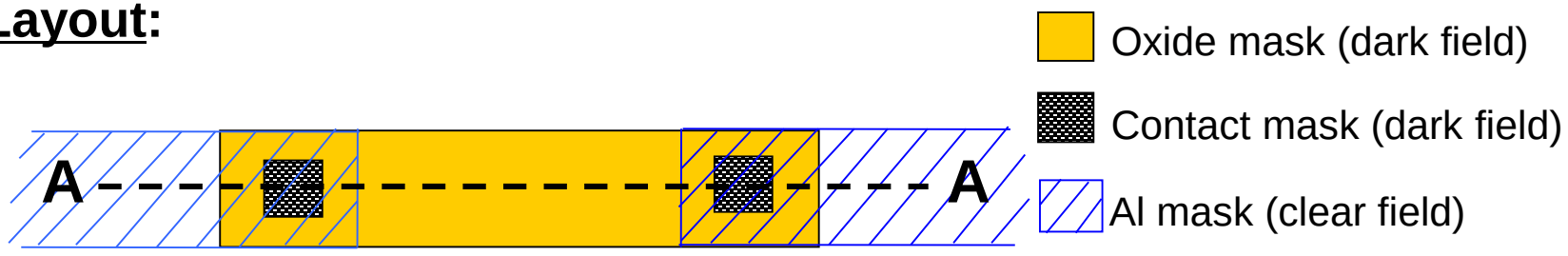
Step 4: deposit oxide to a thickness of 500 nm

Step 5: pattern deposited oxide using the contact mask (dark field)

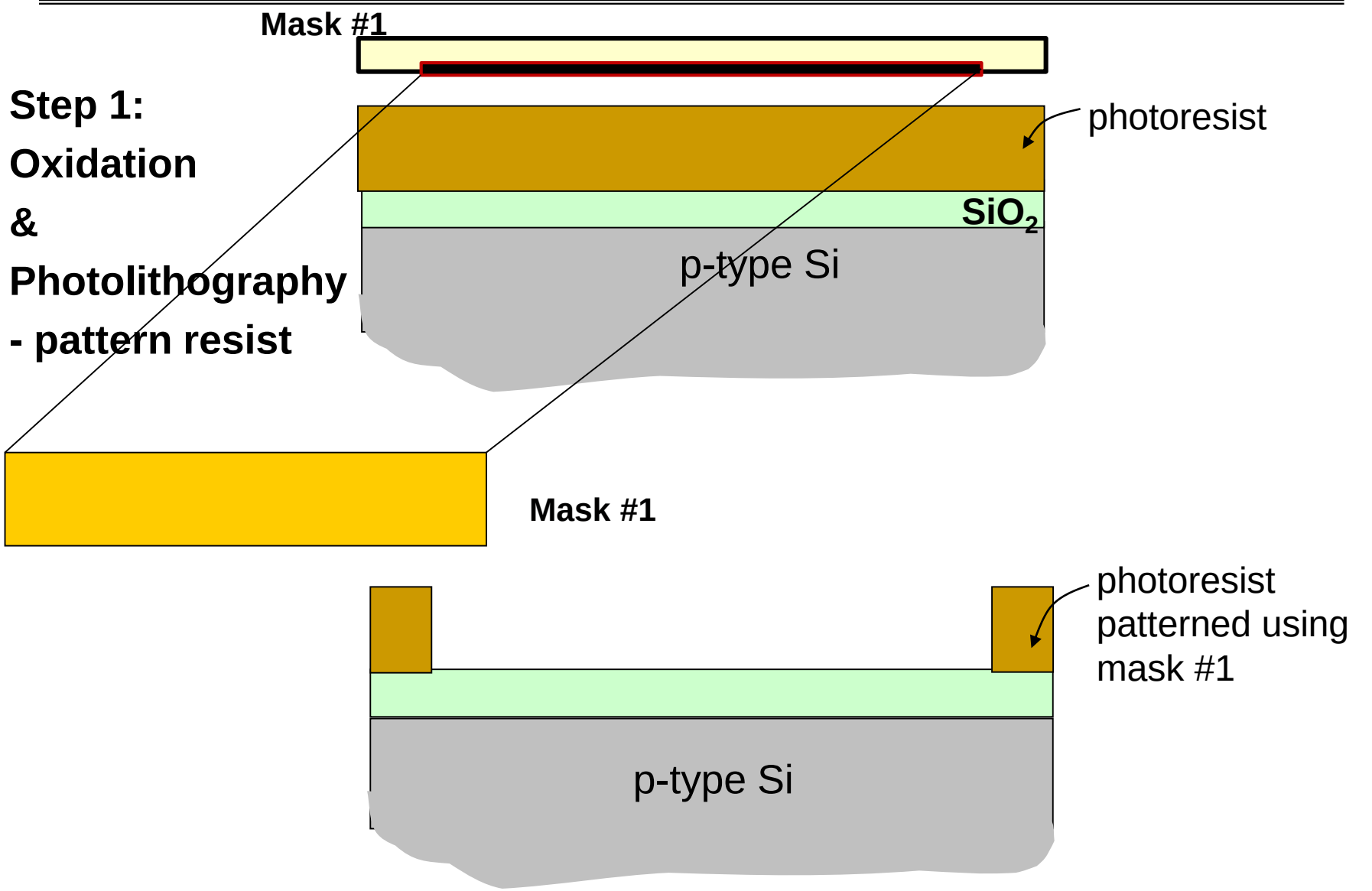
Step 6: deposit aluminum to a thickness of 1 μm

Step 7: pattern using the aluminum mask (clear field)

Layout:



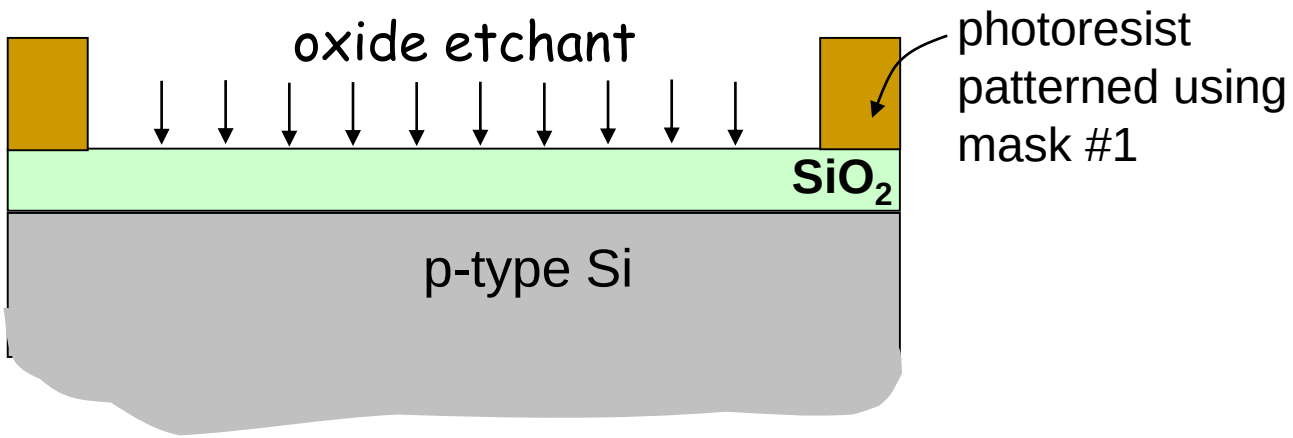
A-A Cross-Section: oxidation, photolithography & etching



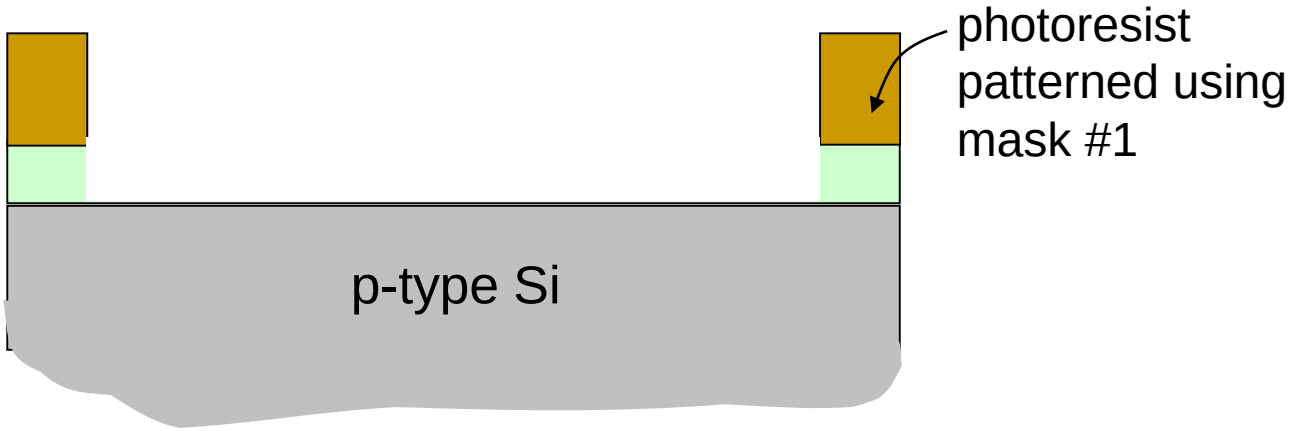
A-A Cross-Section: oxidation, photolithography & etching

Step 2:

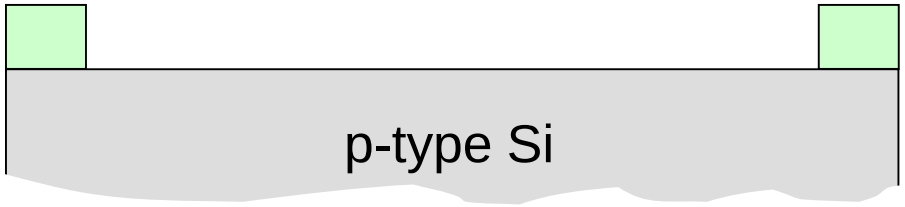
Pattern oxide



$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

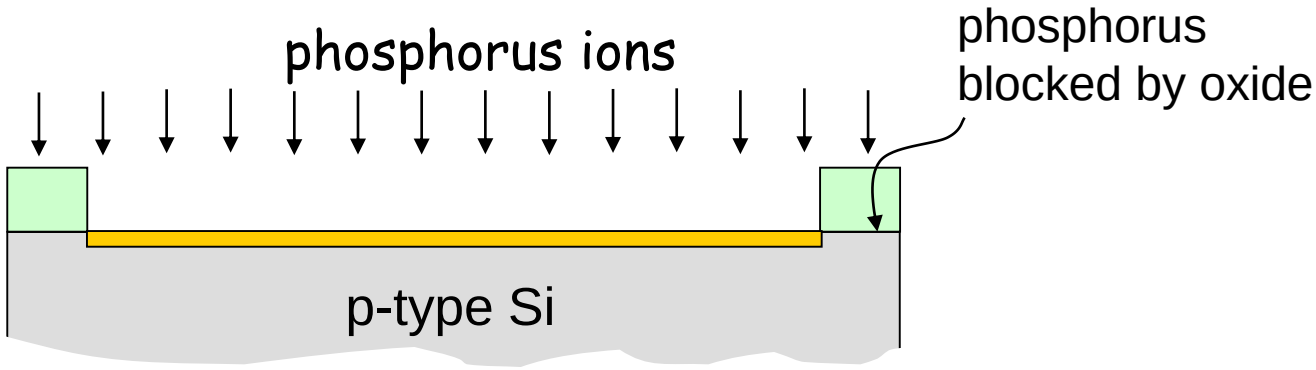


A-A Cross-Section: doping & annealing

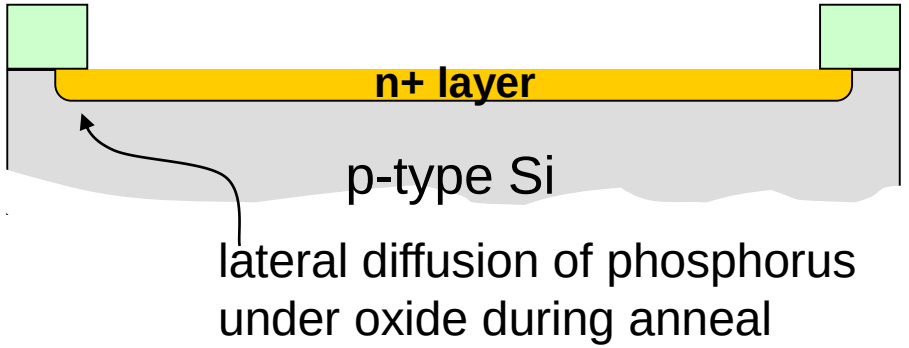


Step 3: Implant & Anneal

phosphorus implant:

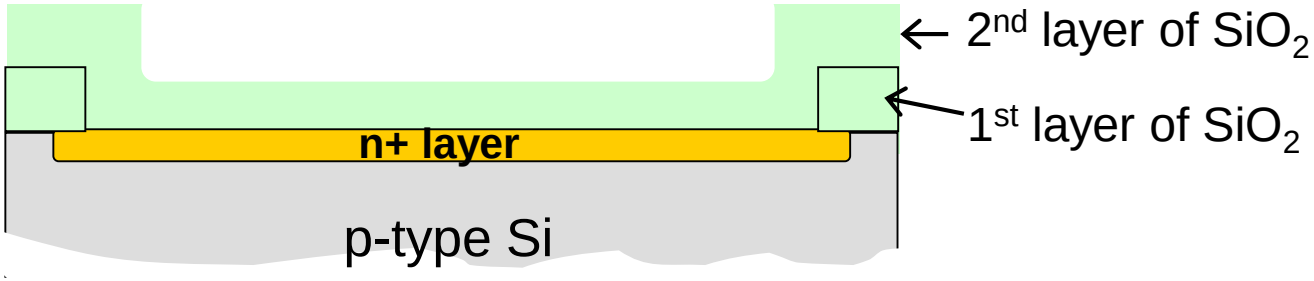


after anneal of phosphorus implant:



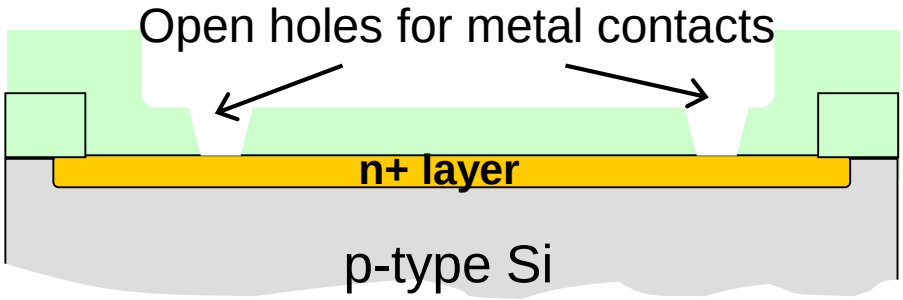
A-A Cross-Section: Metal contact

Step 4: Deposit 500 nm oxide



Mask #2

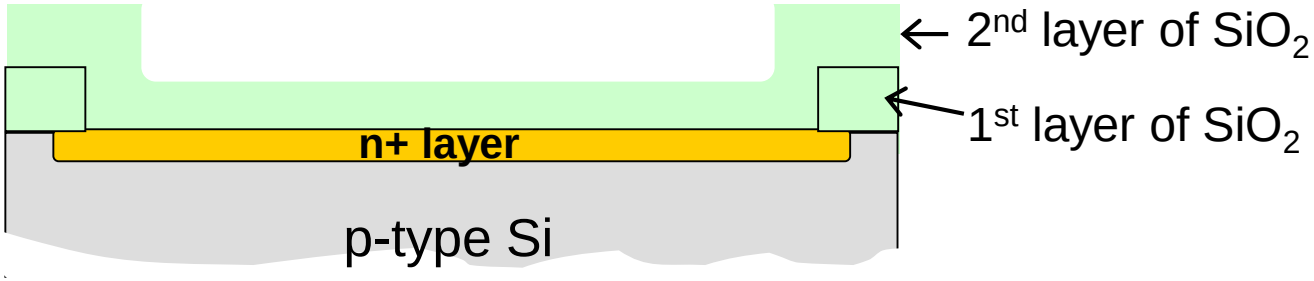
Step 5: Pattern oxide



deposition, photolithography & etching

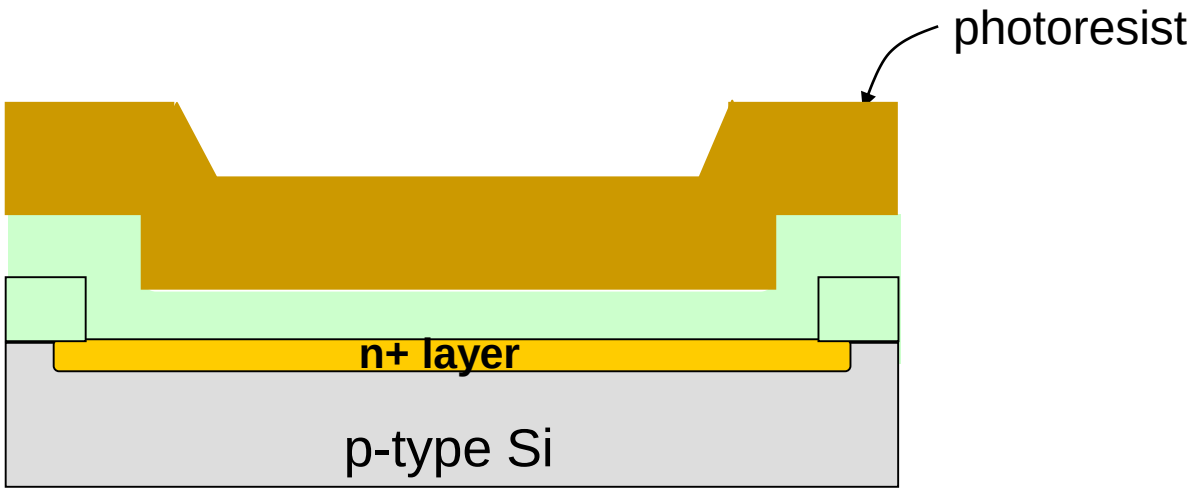
A-A Cross-Section: Metal contact

Step 4: Deposit 500 nm oxide



Step 5:

Pattern oxide

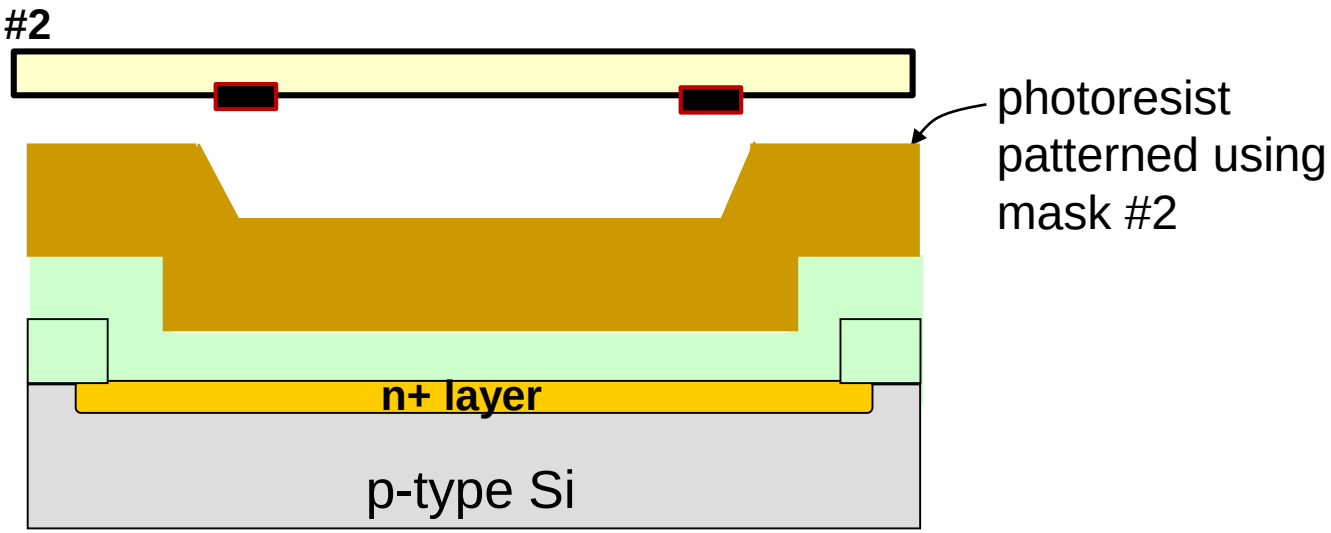


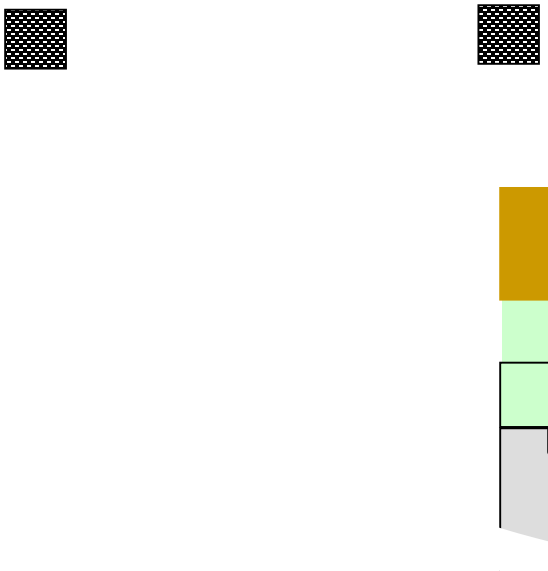
Mask #2

A-A Cross-Section: Metal contact

Step 5:

Pattern oxide

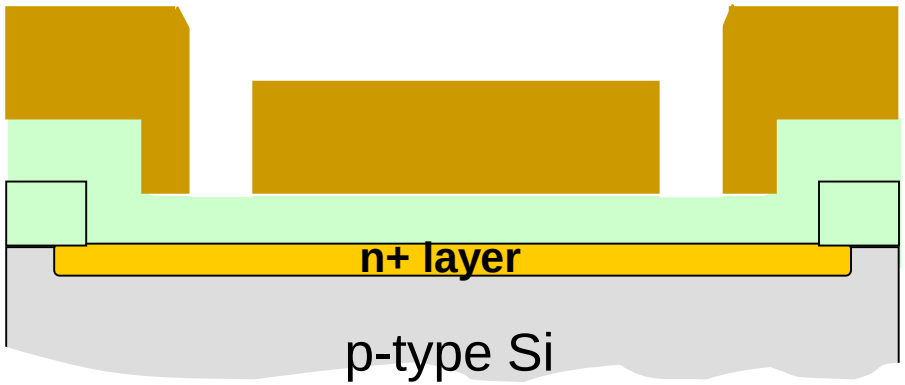


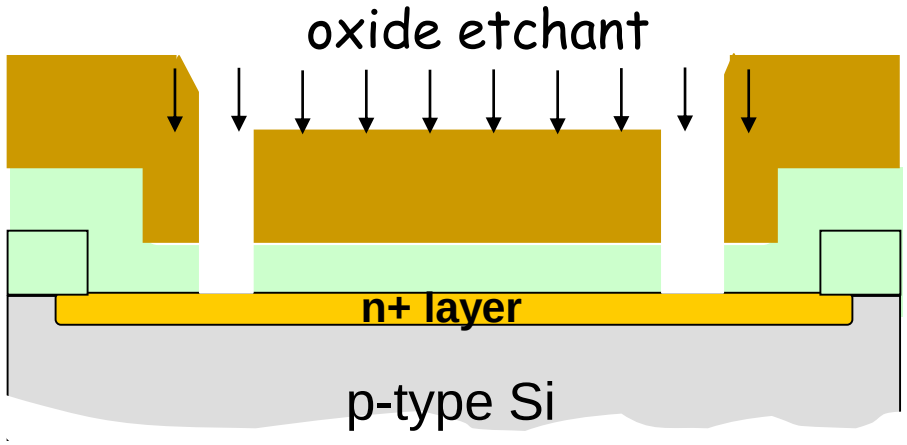


A-A Cross-Section: Metal contact

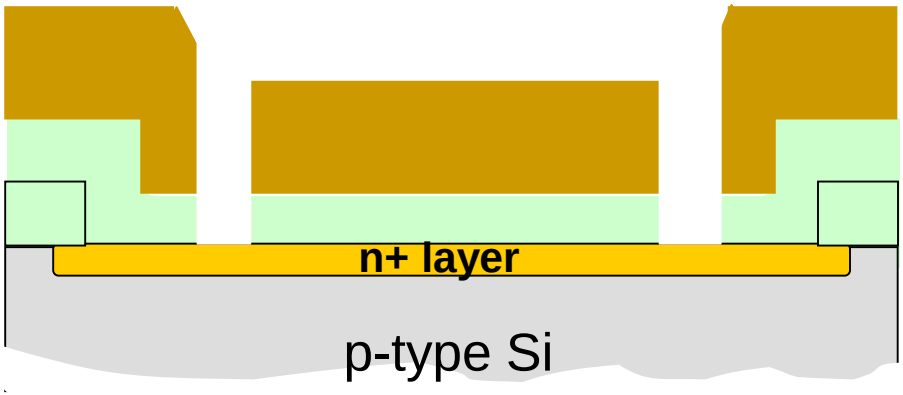
Step 5:

Pattern oxide



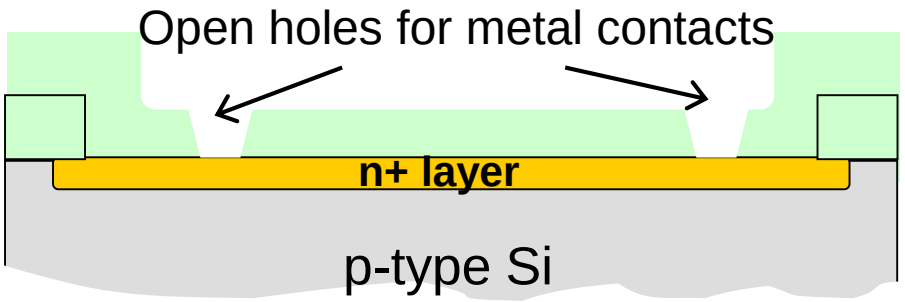


A-A Cross-Section: Metal contact



Step 5:

Pattern oxide



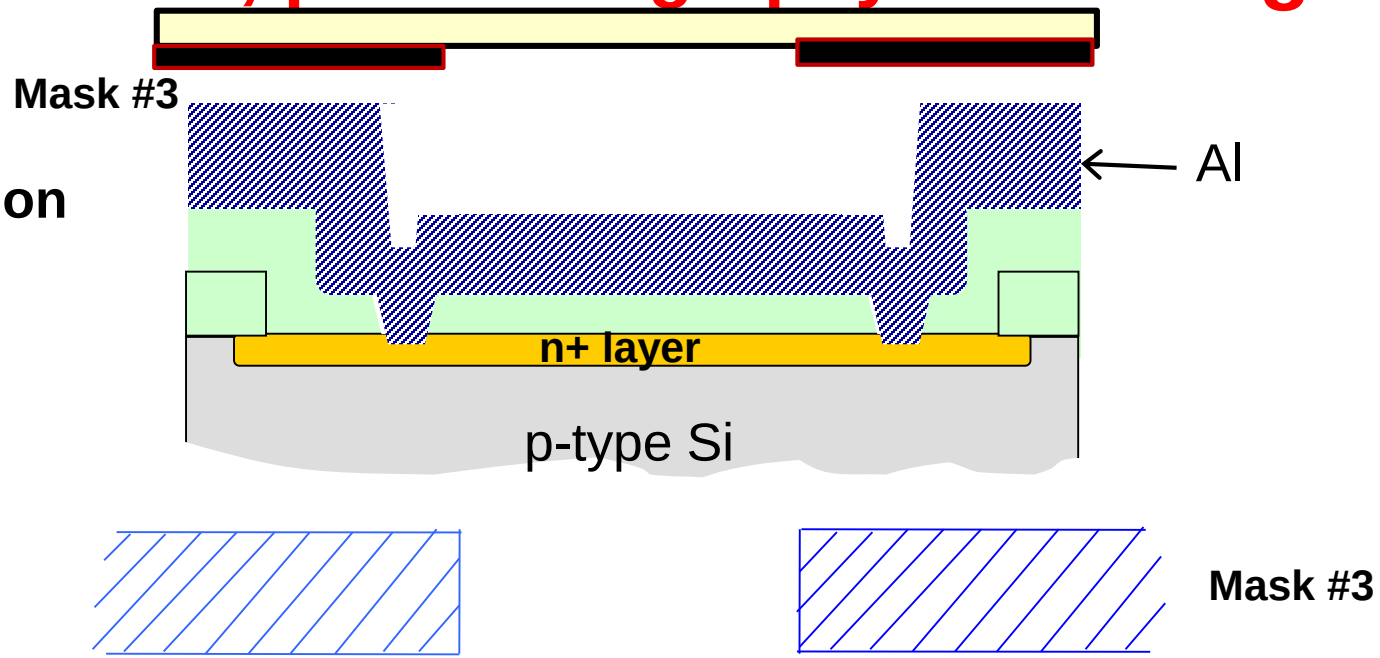
deposition, photolithography & etching

A-A Cross-Section: metallization

deposition, photolithography & etching

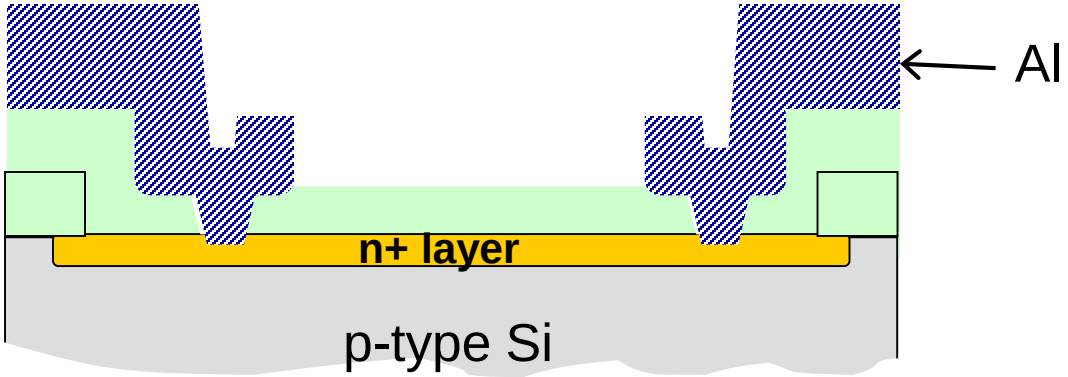
Step 6:

Al deposition

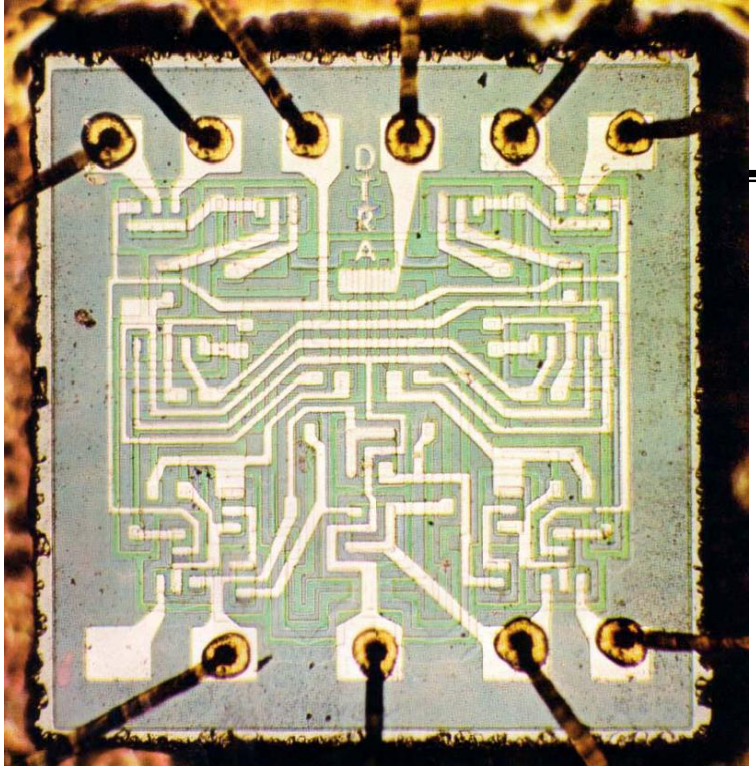


Step 7:

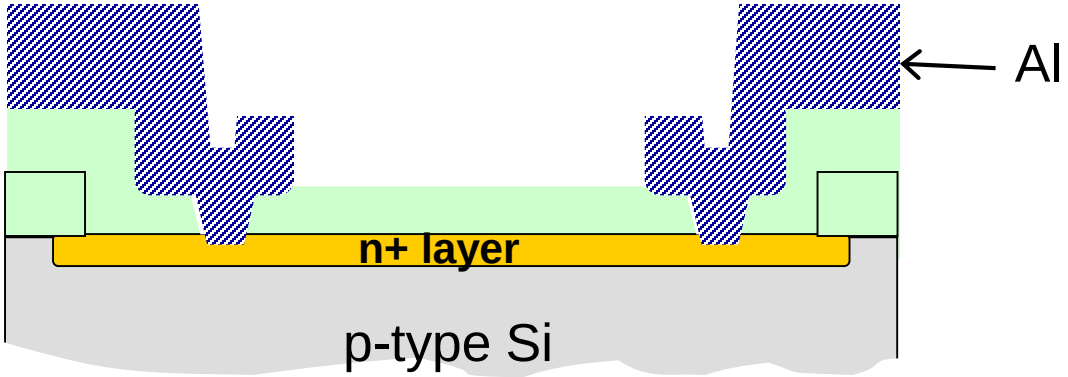
Pattern metal



Summary

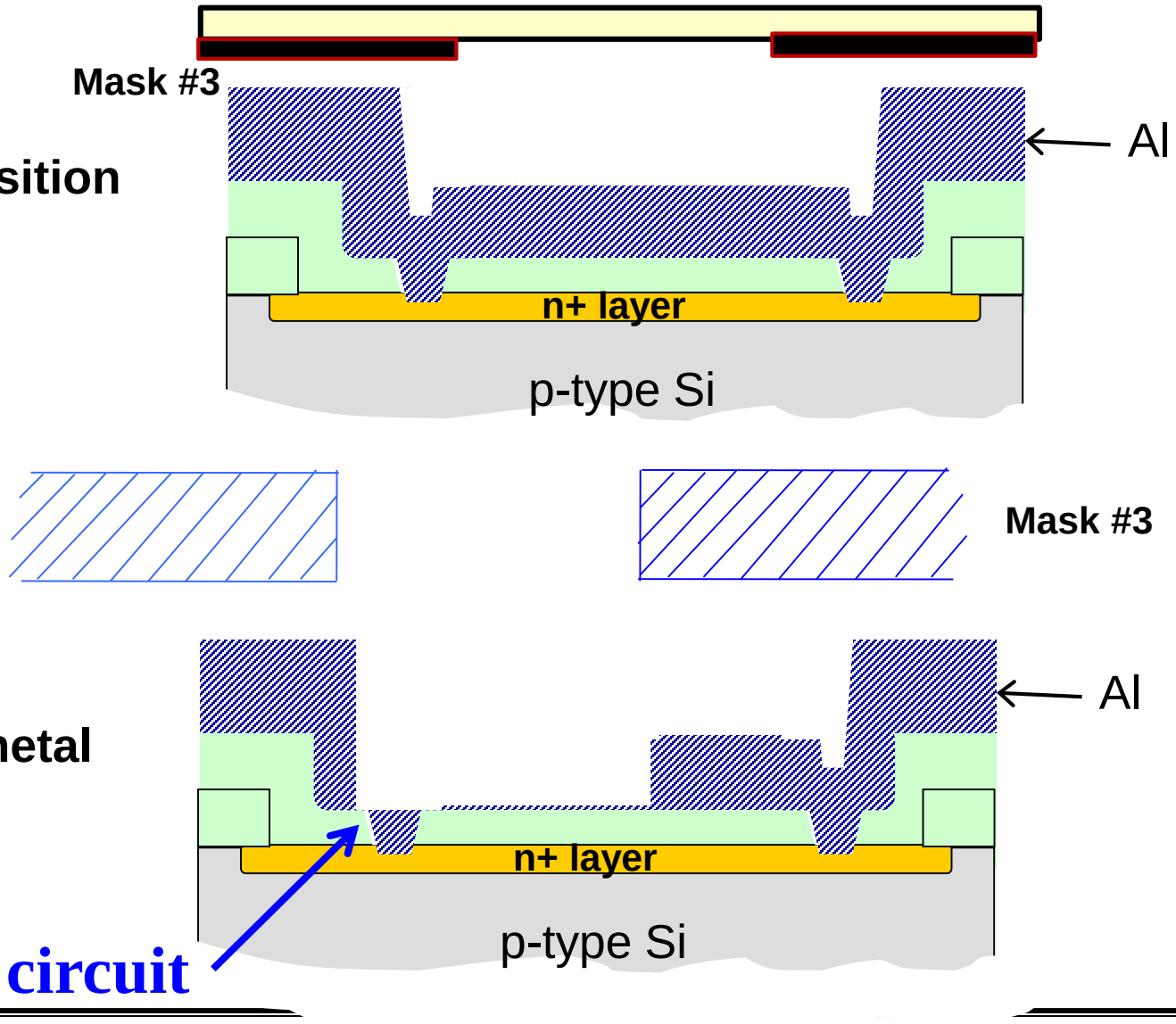


After 7 steps



Layer-to-Layer Alignment

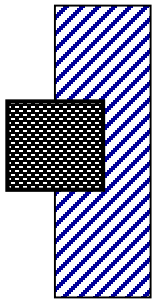
对准



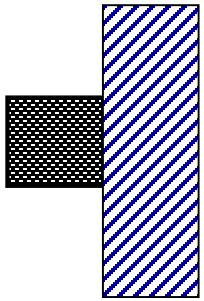
Importance of Layer-to-Layer Alignment

Example: metal line to contact hole

对准



→ marginal contact

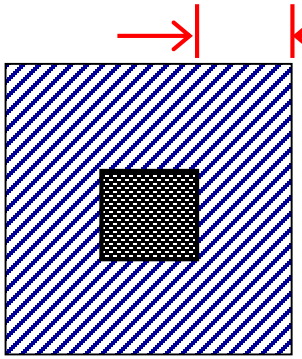


→ no contact!

Example of Design Rule:

If the minimum feature size is 2λ, then the safety margin for overlay error is λ.

对不准



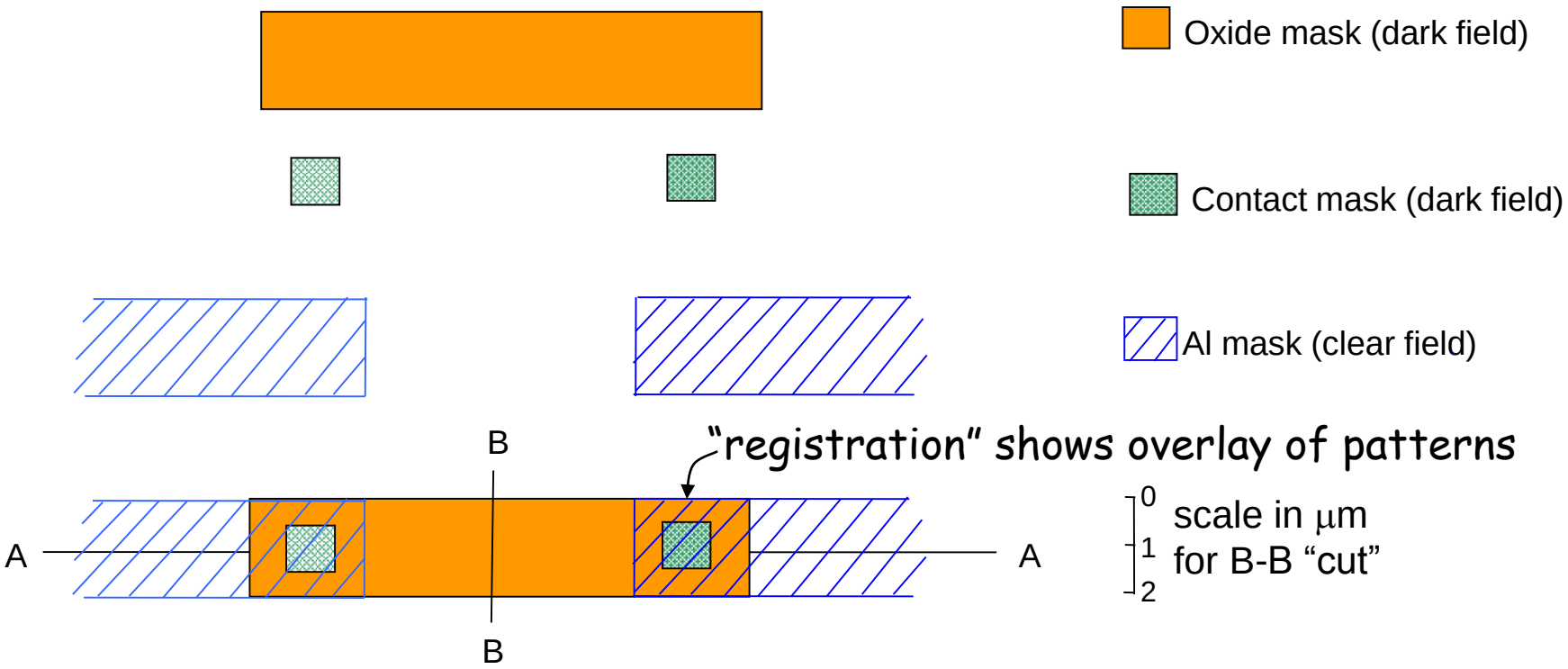
safety margin to allow for misalignment

→ **<u>Design Rules are needed</u>:**

- Interface between designer & process engineer
- Guidelines for designing masks

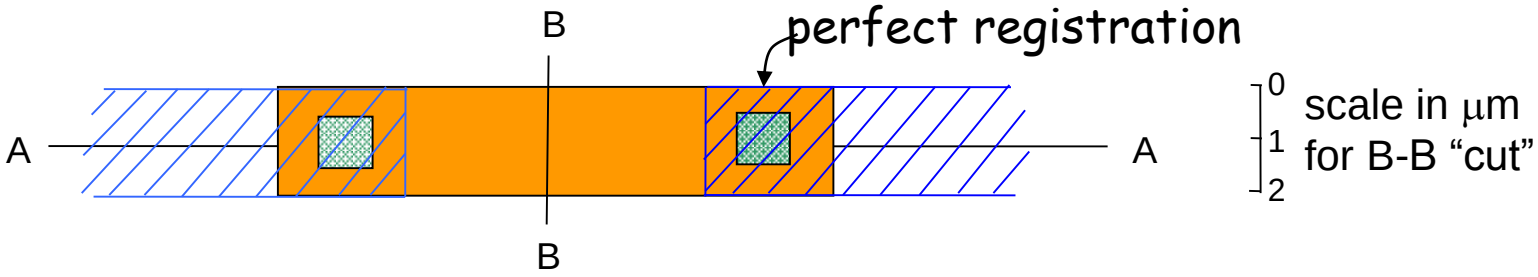
IC RESISTOR MASK LAYOUTS – REGISTRATION OF EACH MASK

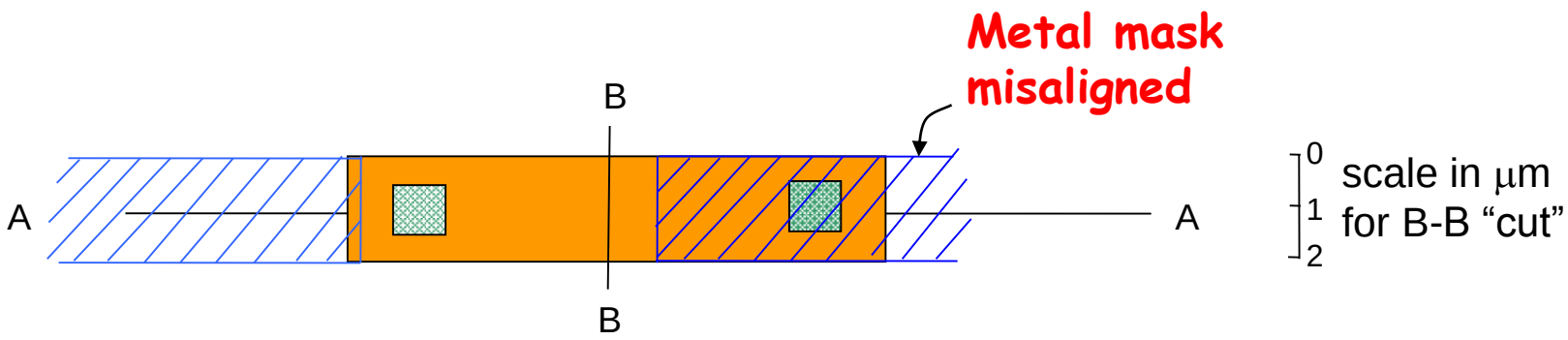
Registration of mask patterns is critical → show separate layouts to avoid ambiguity



Registration of one mask to the next (also called "alignment" and "overlay") is a crucial aspect of lithography

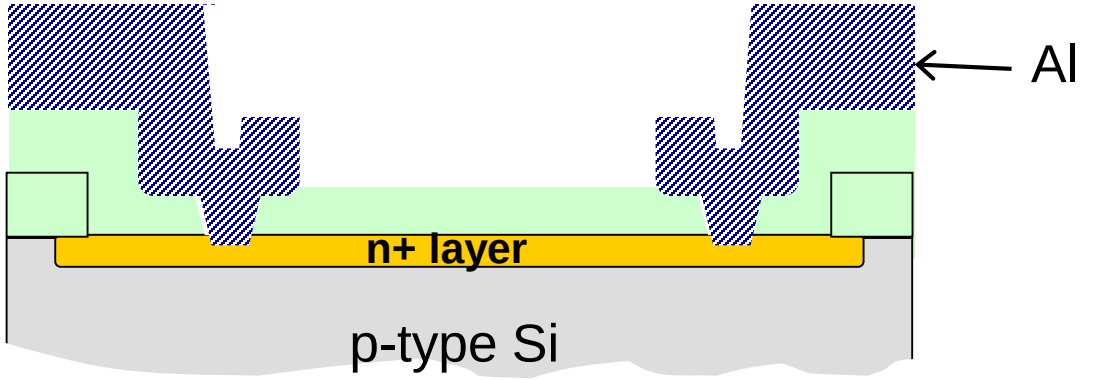
Same Layout but with misregistration (misalignment)

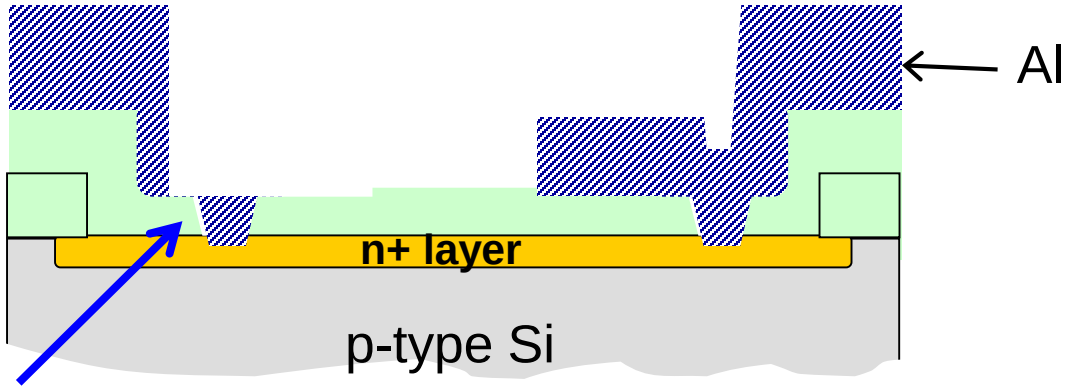




Lets look again at cross-section A-A to understand the consequence of this misalignment.

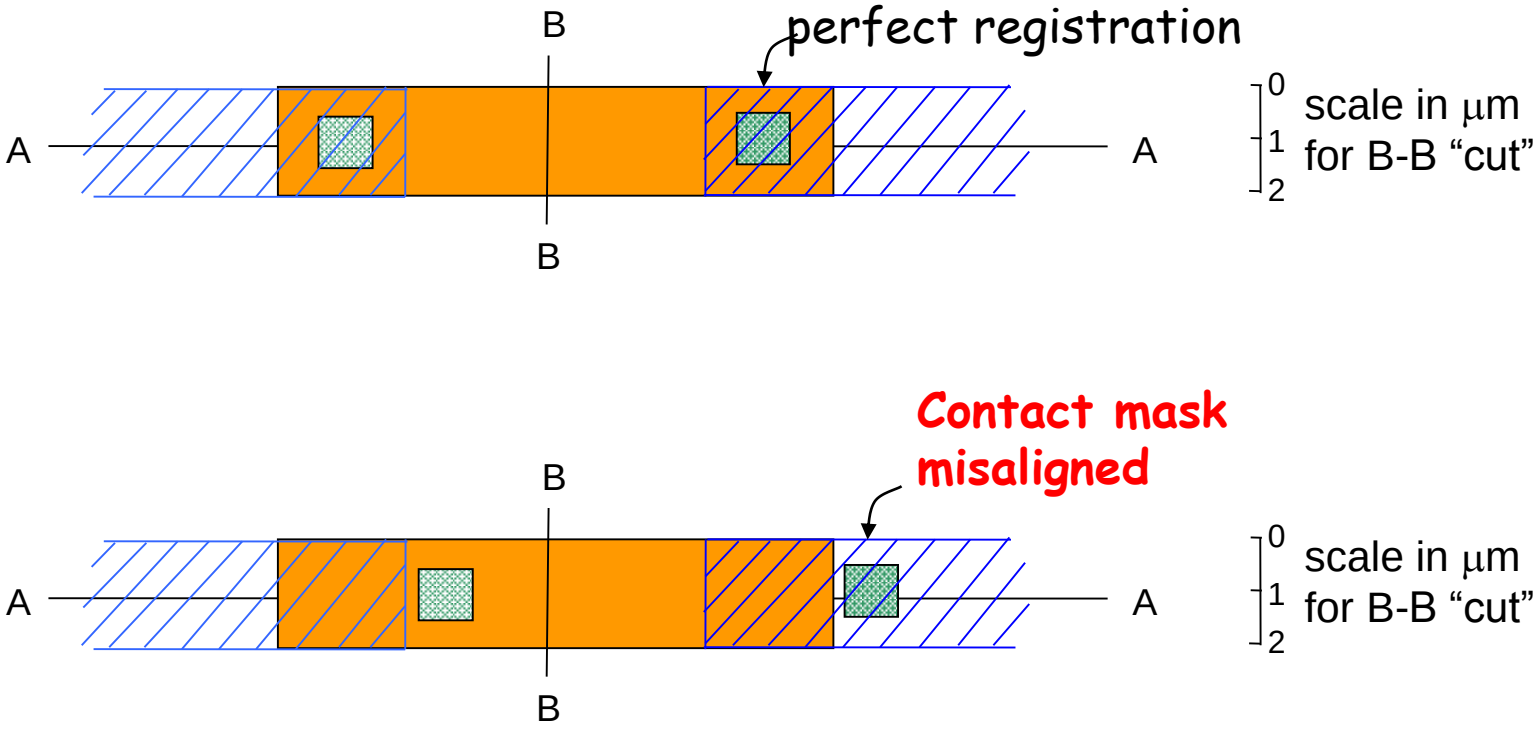
A-A Cross-Section: metallization





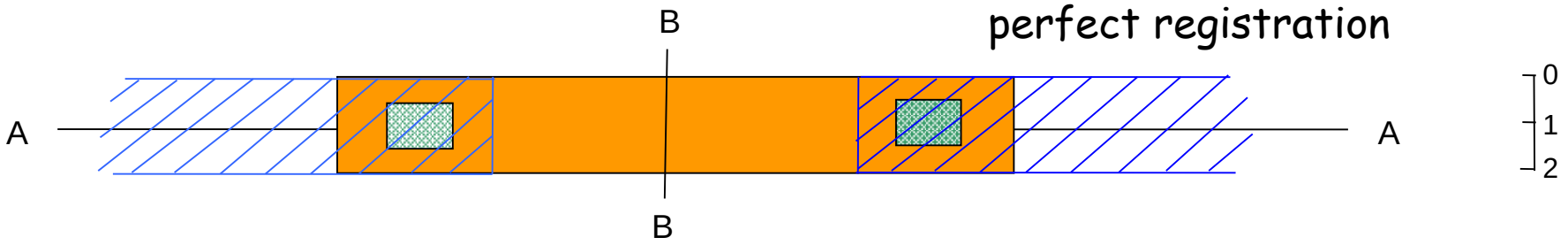
Open circuit

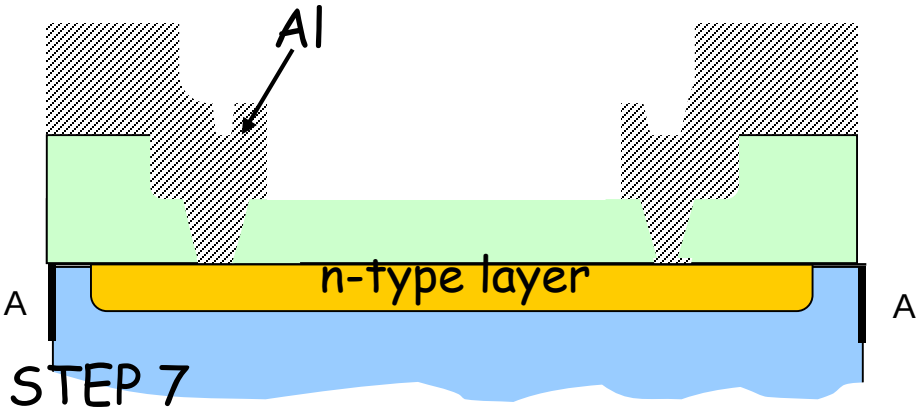
Same Layout but with misregistration (misalignment)



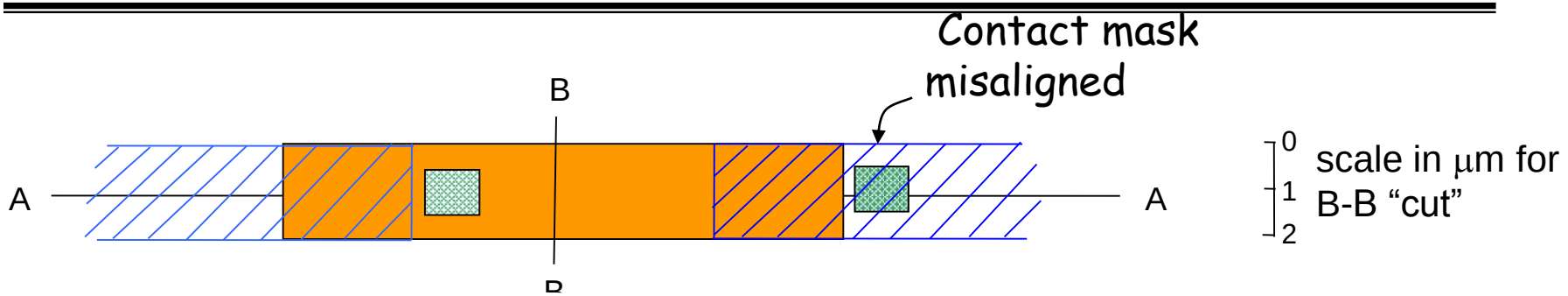
Lets look again at cross-section A-A to understand the consequence of this misalignment.

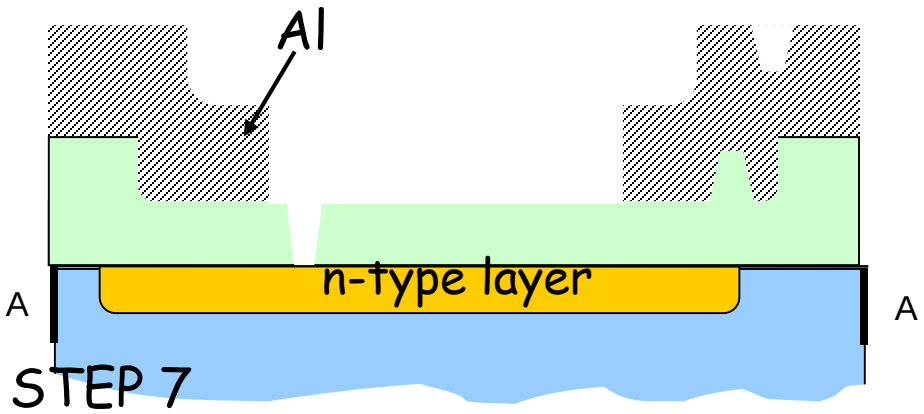
Layout with no misregistration (misalignment)





Layout with misregistration (misalignment)



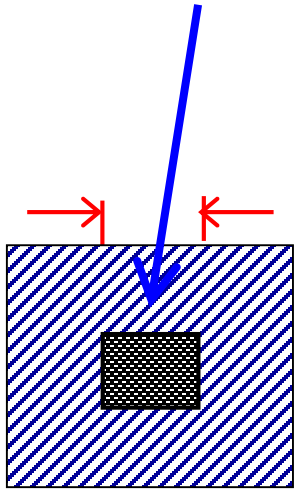


This resistor is a dud … an open circuit !!

Thus we need safety margins in layout which take into account the possible tolerances in fabrication. Each process has a set of "**design rules**" which specify the safety margins.

Example of Design Rule: MOSIS Implementation

- **A minimum feature size is** System



Using 2λ to stand for the minimum feature size

the smallest dimension that can be produced.

Intel & IBM: **2λ = 32nm → 22nm**

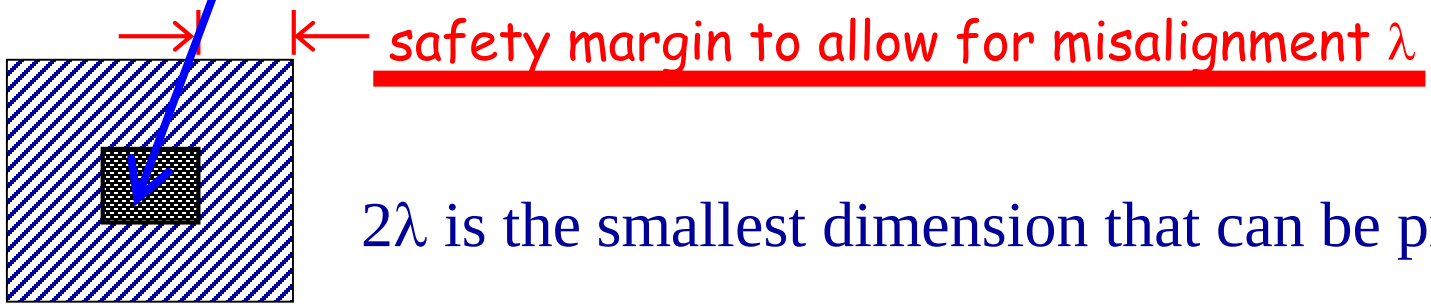
SMIC (中芯国际)： **2λ = 65nm**

XJTLU: **2λ = 1μm**

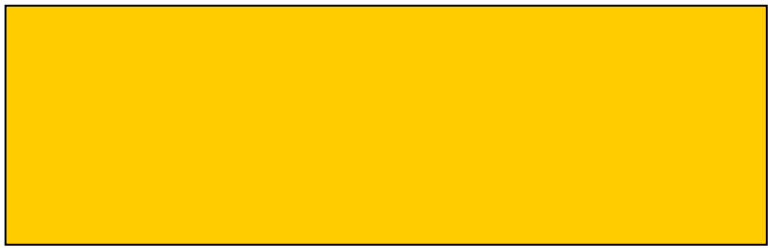
XTLU: **2λ = 10μm**

Example of Design Rule: MOSIS implementation

- If the **minimum feature size is 2λ**, then the minimum active area width is 3λ, the minimum metal width is 3λ, and the safety margin for overlay error is λ.

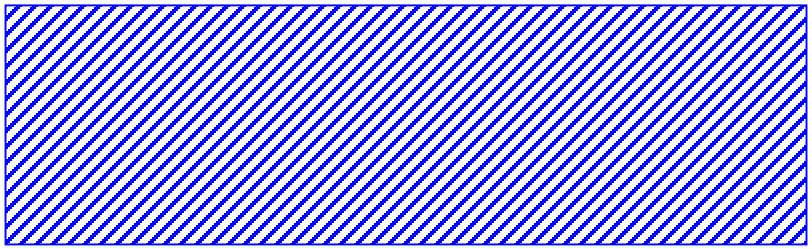


2λ is the smallest dimension that can be produced.



the minimum active area width is 3λ.

For IC resistors, the width can be 2λ.



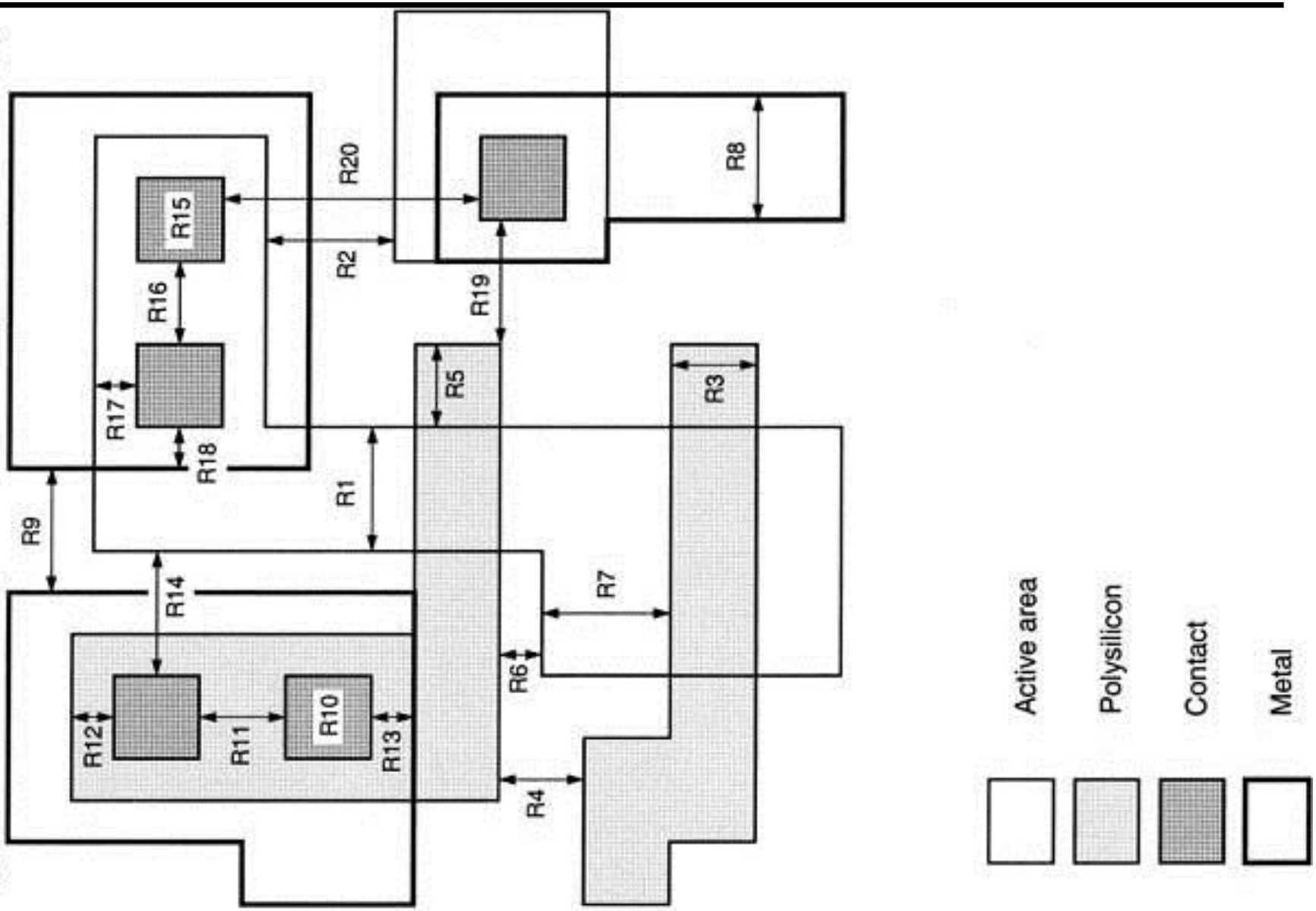
the minimum metal width is 3λ.

MOSIS Layout Design Rules (sample set)

Rule number	*Description*	*λ-Rule*
	Active area rules	
R1	Minimum active area width	3λ
R2	Minimum active area spacing	3λ
	Polysilicon rules	
R3	Minimum poly width	2λ
R4	Minimum poly spacing	2λ
R5	Minimum gate extension of poly over active	2λ
R6	Minimum poly-active edge spacing (poly outside active area)	1λ
R7	Minimum poly-active edge spacing (poly inside active area)	3λ
	Metal rules	
R8	Minimum metal width	3λ
R9	Minimum metal spacing	3λ
	Contact rules	
R10	Poly contact size	2λ
R11	Minimum poly contact spacing	2λ
R12	Minimum poly contact to poly edge spacing	1λ
R13	Minimum poly contact to metal edge spacing	1λ
R14	Minimum poly contact to active edge spacing	3λ
R15	Active contact size	2λ
R16	Minimum active contact spacing (on the same active region)	2λ
R17	Minimum active contact to active edge spacing	1λ
R18	Minimum active contact to metal edge spacing	1λ
R19	Minimum active contact to poly edge spacing	3λ
R20	Minimum active contact spacing (on different active regions)	6λ

MOSIS layout design rules

MOSIS layout design rules



IC Fabrication Techniques

OUTLINE

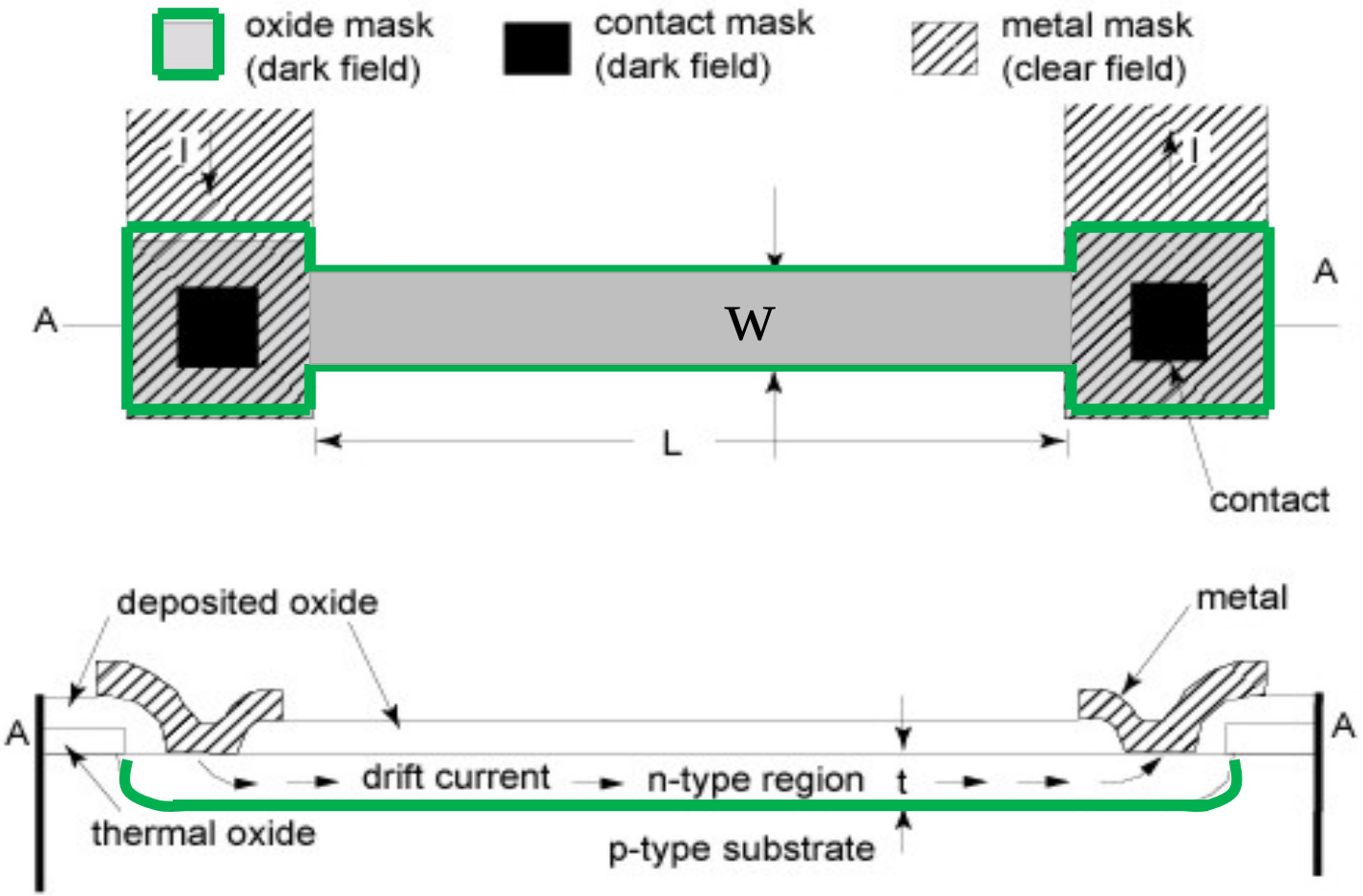
- IC Resistor
- **Sheet Resistance**
- Diode

Reference Reading

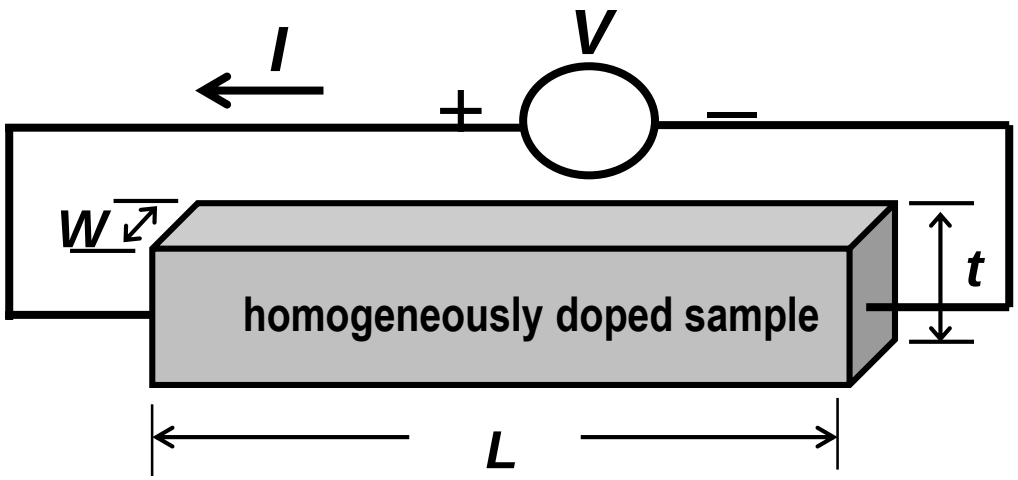
- **Chapter 5 + Liverpool Handout + www**

Using Sheet Resistance (Rs)

- **Ion-implanted (or "diffused") IC resistor**



Electrical Resistance



Resistance $$R \equiv \frac{V}{I} = \frac{\rho L}{A} = \frac{\rho L}{tW} = \boxed{\left(\frac{\rho}{t}\right)\left(\frac{L}{W}\right)}$$ (Unit: ohms)

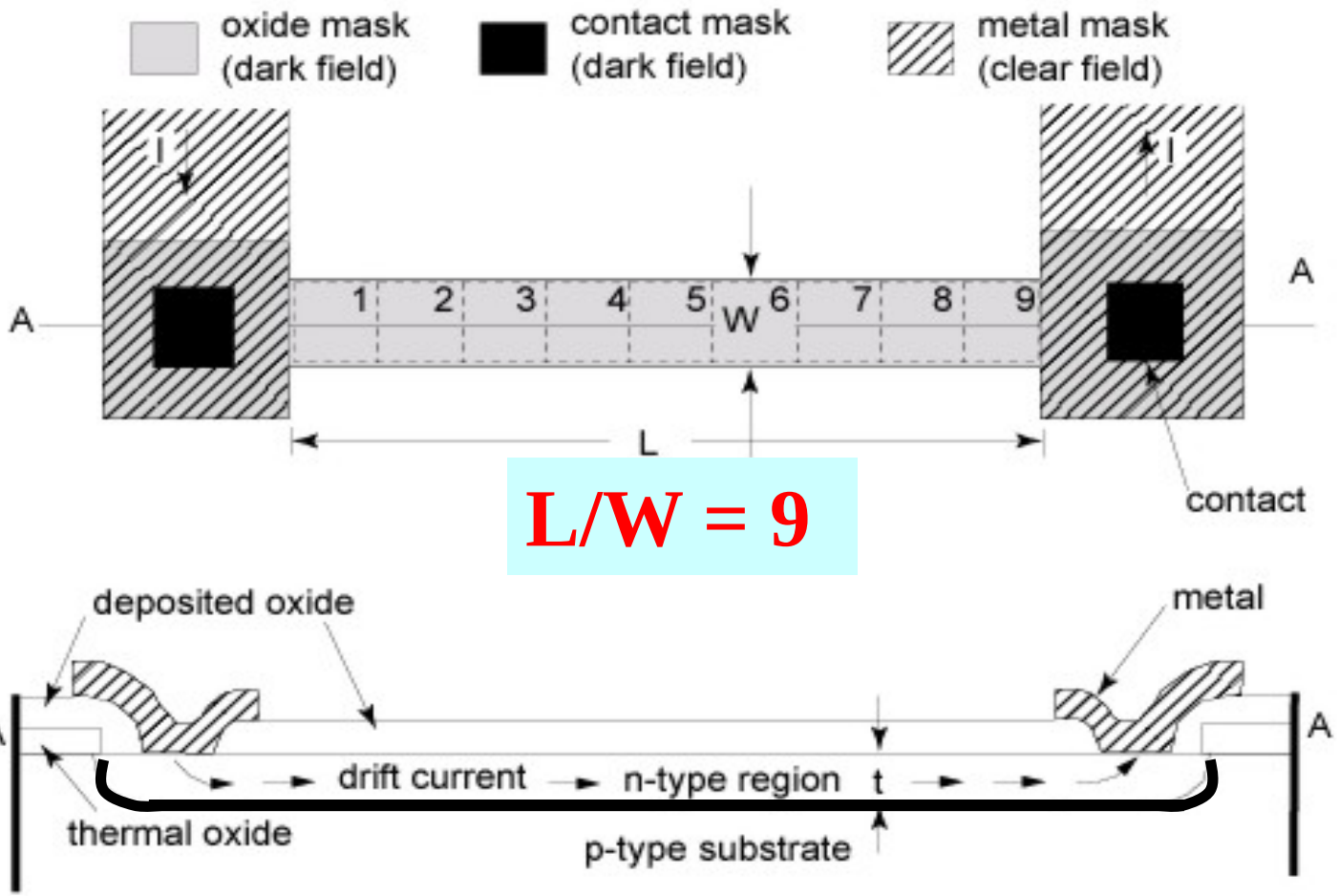
where ρ is the resistivity ($\Omega \cdot cm$)

Process

Mask

Using Sheet Resistance (Rs)

- **Ion-implanted (or "diffused") IC resistor**



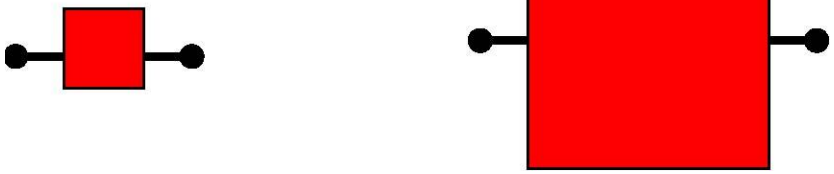
Concept of Sheet Resistivity

$$R = \rho L/A = (\rho/t)\,(L/W)$$

Sheet Resistivity (R_S) Ω/sq
or **Sheet Resistance**

# of Squares

$$R = Rs\,(L/W)$$

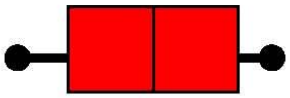


If L = W,

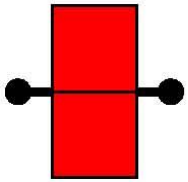
$R = R_s$

Number of Squares

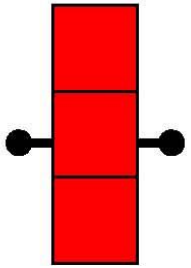
$R = R_S (L/W)$



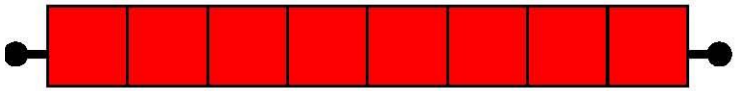
$R = 2R_S$



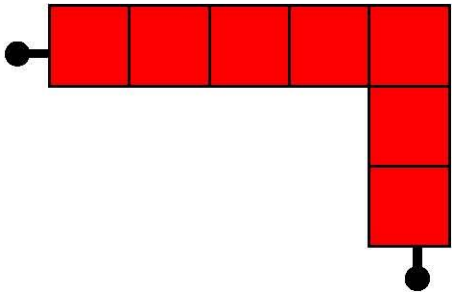
$R = R_S/2$



$R = R_S/3$

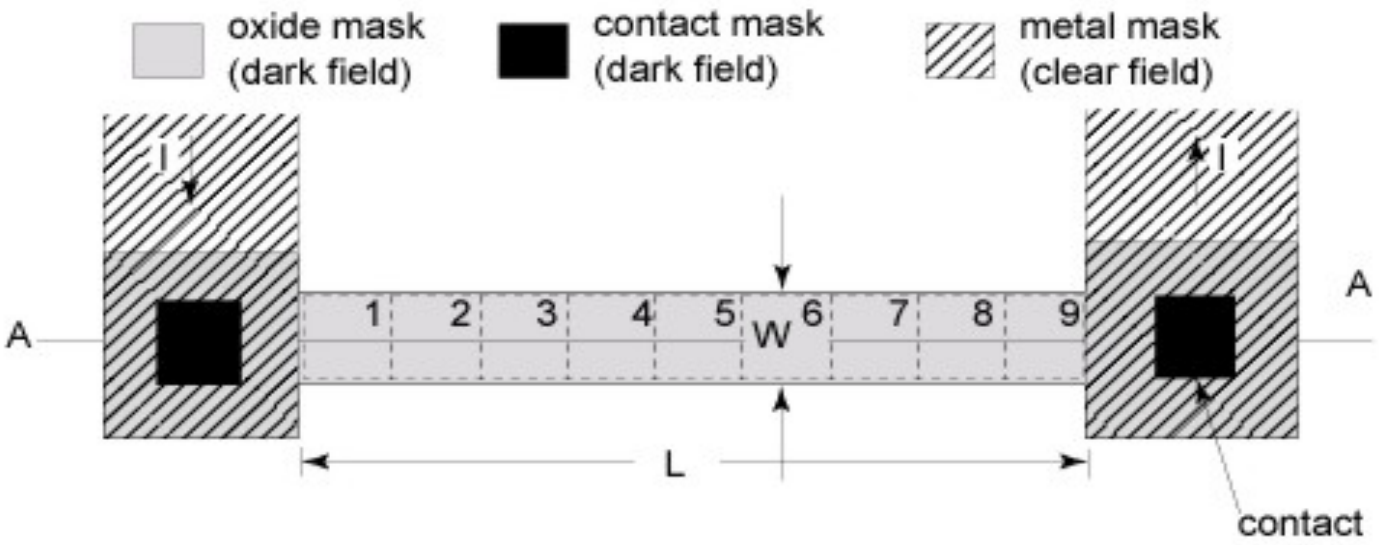


$R = 8R_S$



$R \approx 6.5R_S$

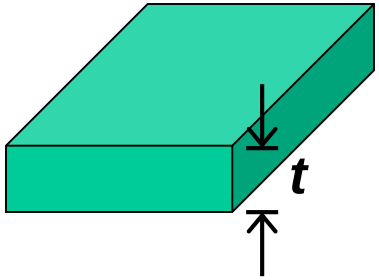
Using Sheet Resistance (Rs)



$$R = \left(\frac{\rho}{t}\right)\left(\frac{L}{W}\right) = R_S \frac{L}{W} \approx 9R_S$$

Integrated-Circuit Resistors

SL



The resistivity ρ and thickness ***t*** are fixed for each layer in a given manufacturing process

A circuit designer specifies the length ***L*** and width ***W***, to achieve a desired resistance ***R***

$$R = R_s\left(\frac{L}{W}\right)$$

fixed designable

Example: Suppose we want to design a 5 kΩ resistor using a layer of material with R_s = 200 Ω/□

Resistor layout (top view)

$W/L = 25$

Space-efficient layout

IC Fabrication Techniques

OUTLINE

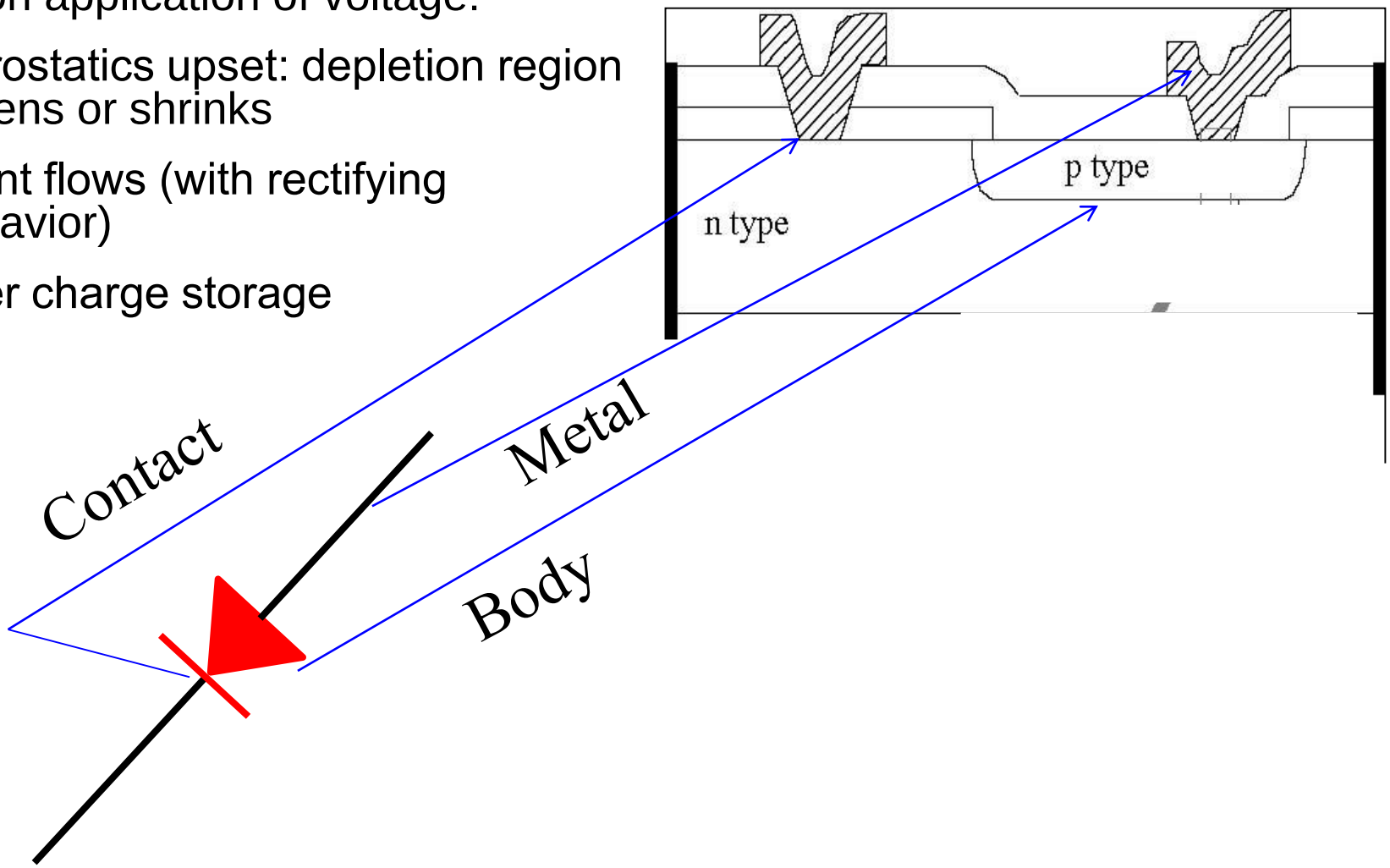
- IC Resistor
- Sheet Resistance
- **Diode**

Reference Reading

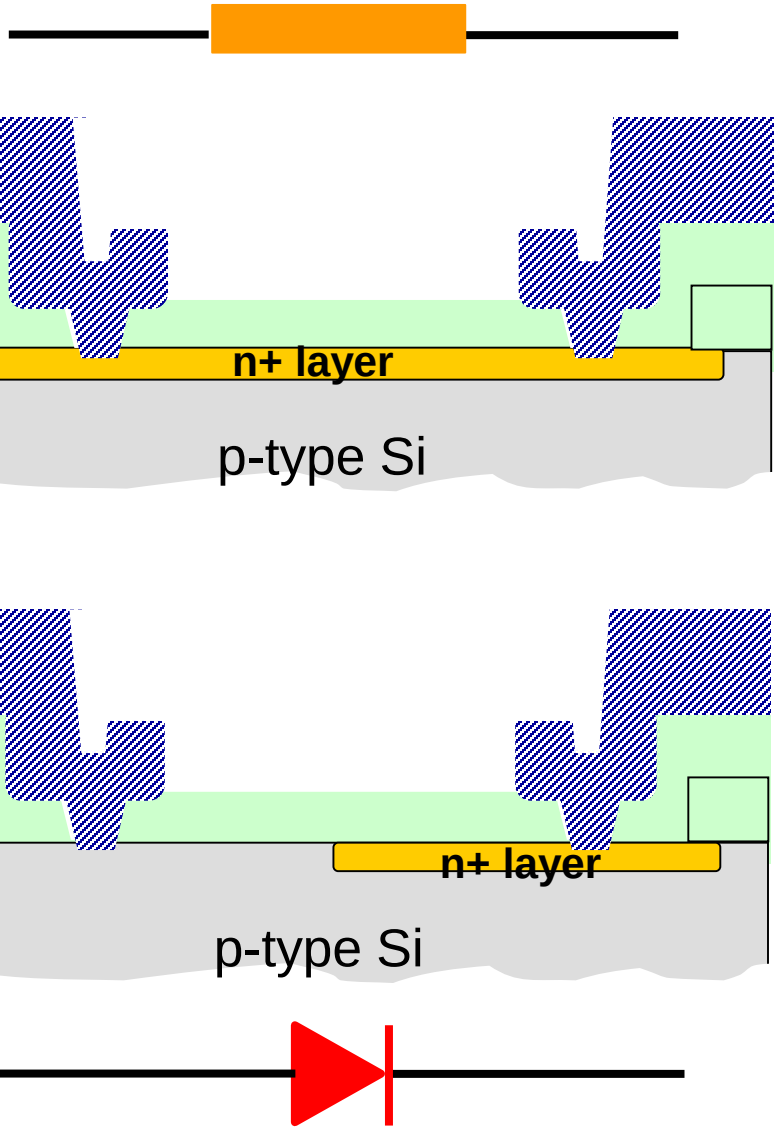
- **Chapter 5 + Handout + www**

Electrostatics of p-n junction in equilibrium

- Upon application of voltage:
- electrostatics upset: depletion region widens or shrinks
- current flows (with rectifying behavior)
- carrier charge storage

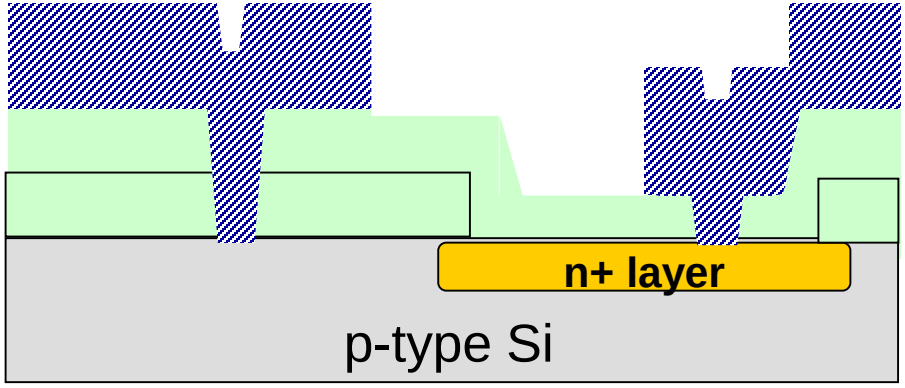


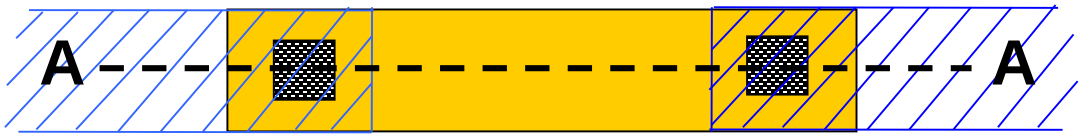
Process Flow Example #1: Resistor

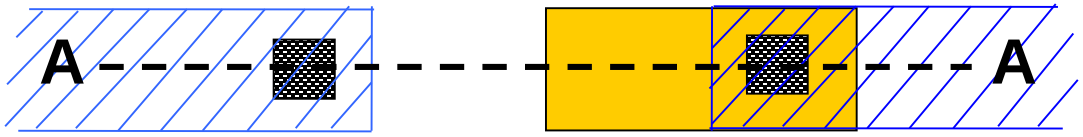


Process Flow Example #2: diode

A -- A







Oxide mask (dark field)

Contact mask (dark field)

Al mask (clear field)

Process Flow Example #1: Resistor

Three-mask process:

Starting material: p-type wafer with $N_A = 10^{16}$ cm^{-3}

Step 1: grow 500 nm of SiO_2

Step 2: pattern oxide using the oxide mask (dark field)

Step 3: implant phosphorus and anneal to form an n-type layer with $N_D = 10^{20}$ cm^{-3} and depth 100 nm

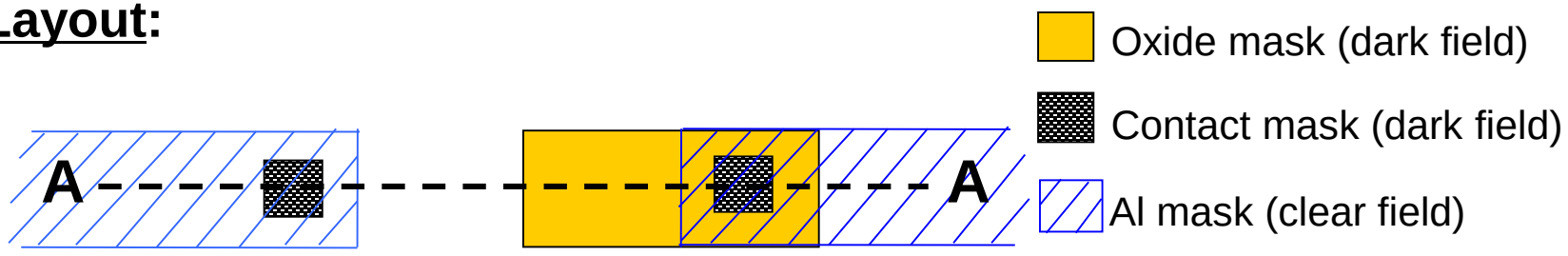
Step 4: deposit oxide to a thickness of 500 nm

Step 5: pattern deposited oxide using the contact mask (dark field)

Step 6: deposit aluminum to a thickness of 1 μm

Step 7: pattern using the aluminum mask (clear field)

Layout:



A-A Cross-Section: oxidation, photolithography & etching

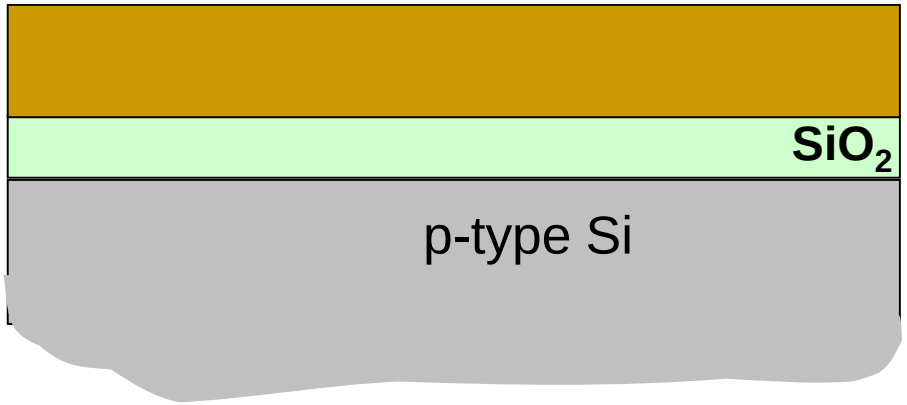
Step 1:

Grow oxide

Step 2:

Pattern oxide

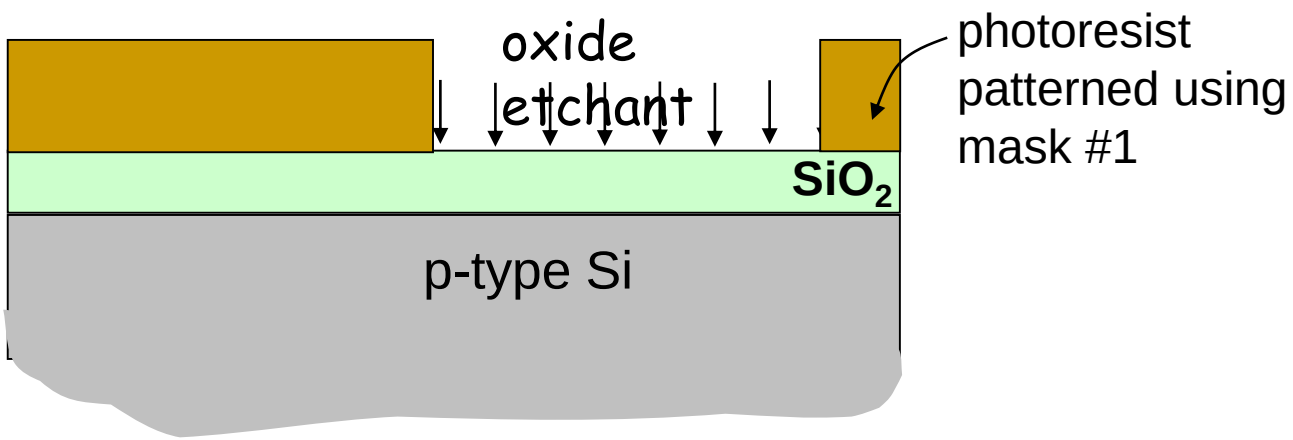
(active mask)



A-A Cross-Section: oxidation, photolithography & etching

Step 1:

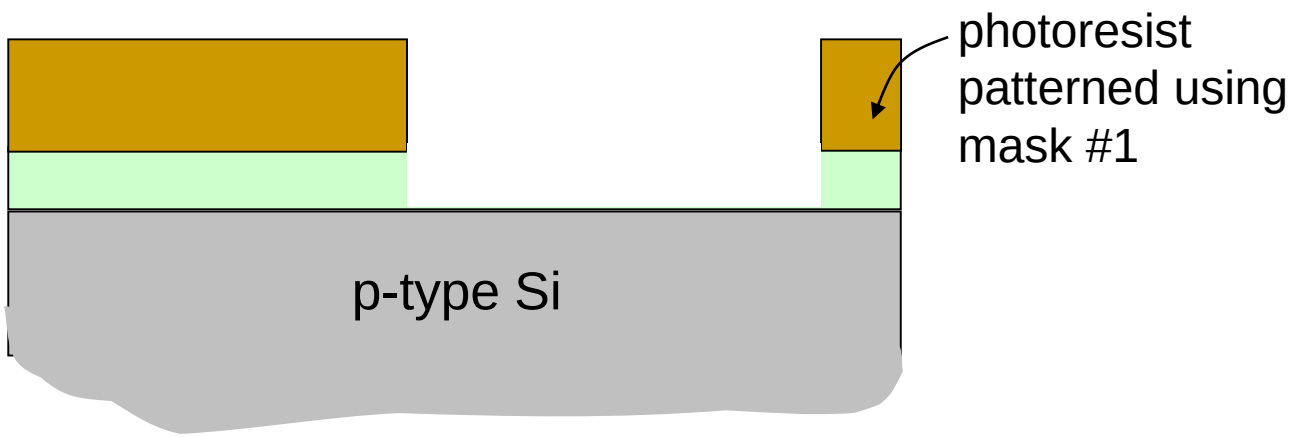
Grow oxide



Step 2:

Pattern oxide

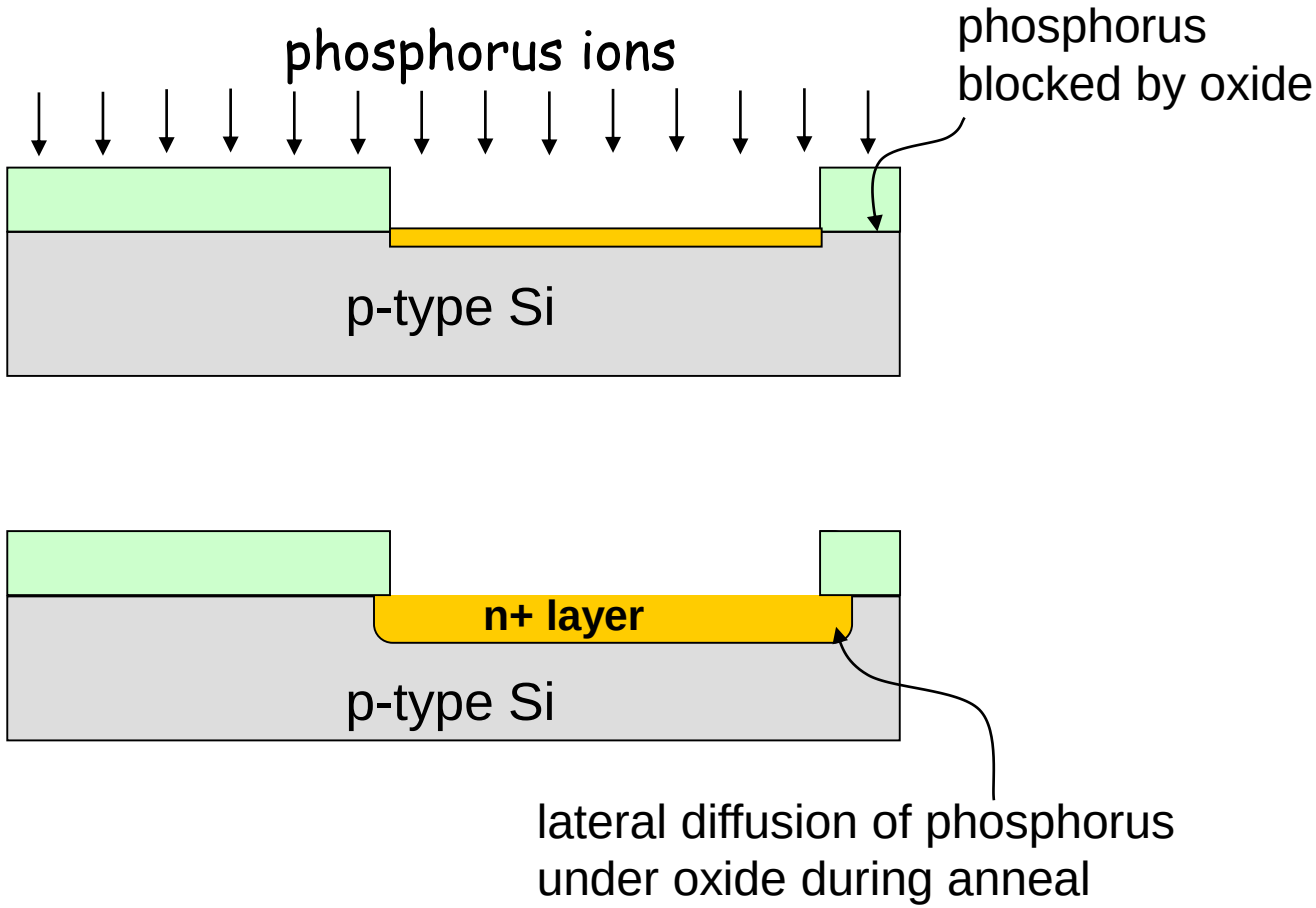
(active mask)



A-A Cross-Section: doping & annealing

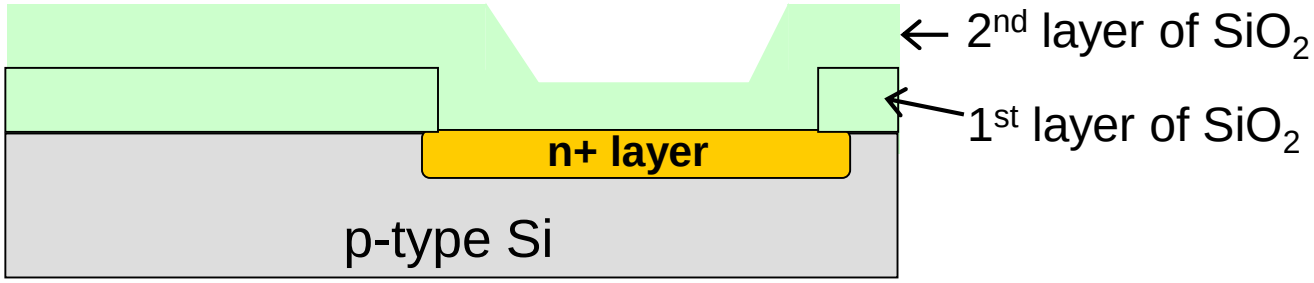
Step 3: Implant & Anneal

phosphorus implant:



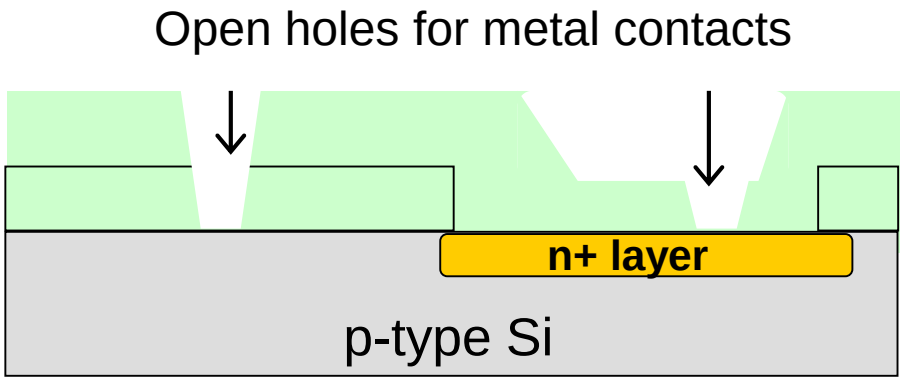
A-A Cross-Section: Metal contact

Step 4: Deposit 500 nm oxide



Step 5:

Pattern oxide (contact mask)



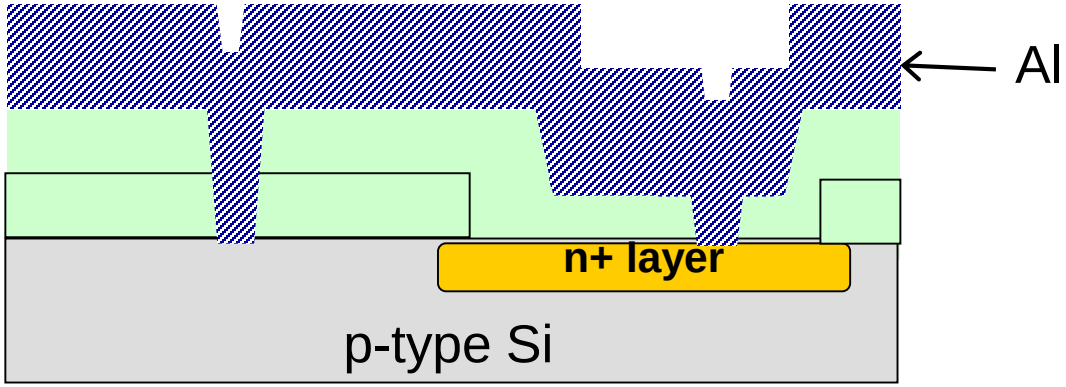
deposition, photolithography & etching

A-A Cross-Section: metallization

deposition, photolithography & etching

Step 6:

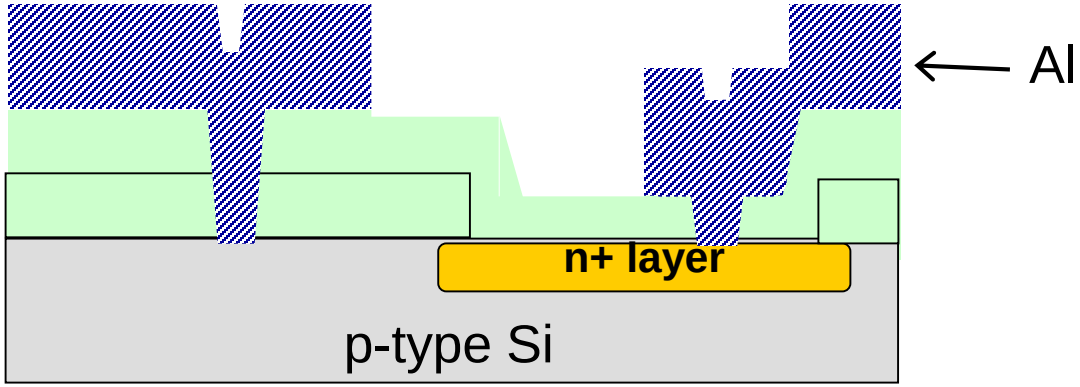
Al deposition



Step 7:

Pattern metal

(Metal mask)



Example of Design Rule: MOSIS

- R1: the minimum feature size is 2λ,
- R2: the minimum active area width is 3λ,
- R3: the minimum metal width is 3λ,
- R4: the safety margin for overlay error is λ,
- R5: the minimum active contact spacing on different active regions is 6λ.

Layout: