

**Lecture 12**  
*of*  
**EEE201**

# CMOS Digital Integrated Circuits

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## □ RAM & ROM

- memory architecture
- memory cells of SRAM & DRAM
- memory cell of EEPROM
- address decoder



# Circuits for Storing Digital Data

(access time & storage density)

- ❑ To process **digital data**, **combinational logic circuits** are needed to perform logic functions (e.g. addition, multiplication, multiplexing).
- ❑ It is equally important to have electronic circuits to store **digital data** either temporarily or for a long time. Such digital circuits are **memory circuits**.
  - Short **access time** is expected in retrieving the *stored* digital data.
  - High **density** of **storage capacity** is always preferred whenever possible because of the ever increasing amounts of digital data.

# Digital Memory Circuits

(RAM & ROM)

- ❑ The silicon CMOS technology that is good for realisation of **combinational logic circuits** in general can also be used to make **memory circuits**.
  - The semiconductor fabrication however may be modified for optimal manufacturing of memory circuits.
- ❑ There are two basic types of **memory circuits** which can be implemented using CMOS transistors for storing digital data electronically.
  - **random access memory (RAM)** – volatile
  - **read-only memory (ROM)** – non-volatile
  - A **volatile memory** loses its stored data when power is removed.

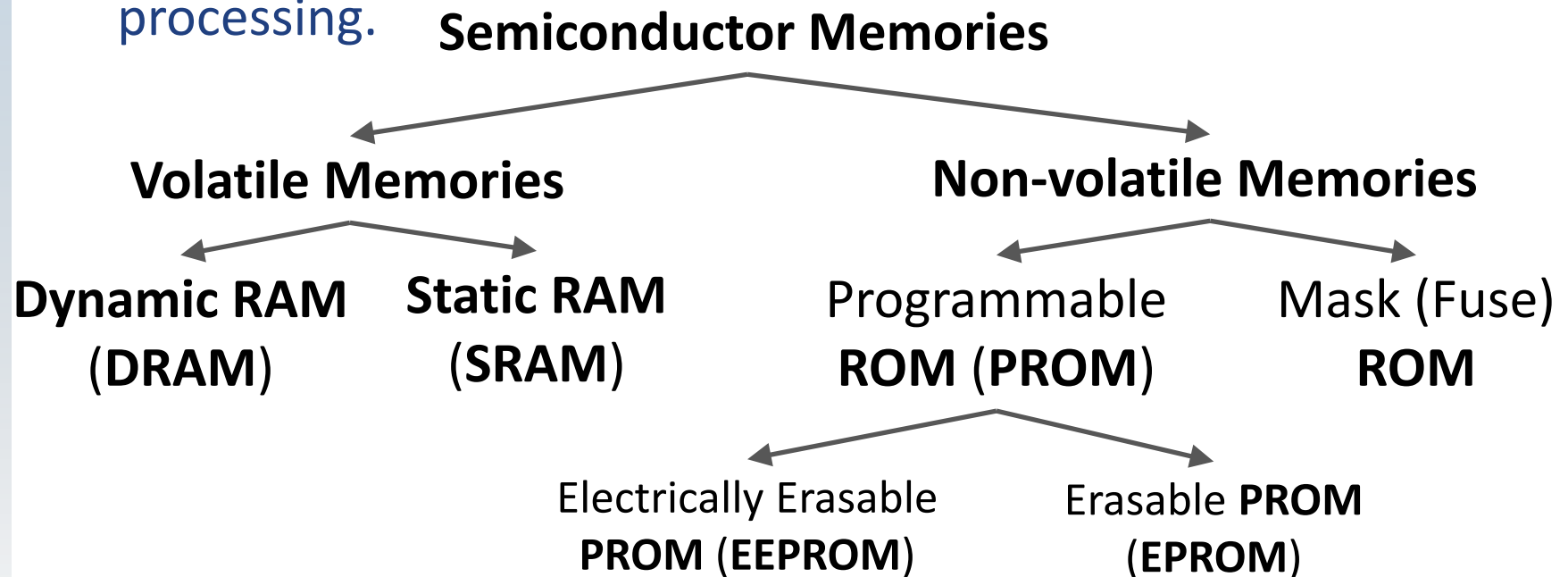


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# Semiconductor Memories

(memory types)

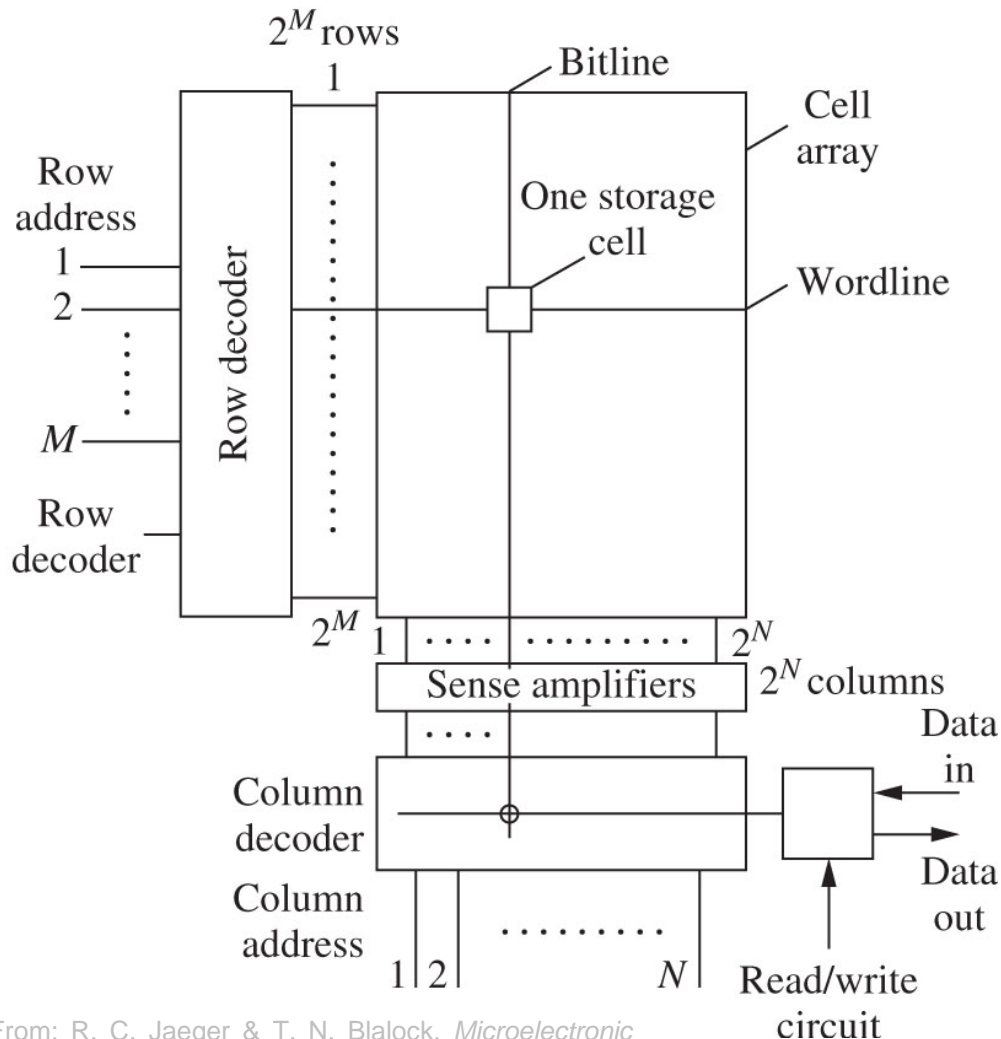
- ❑ Semiconductor memories are predominantly used for storing digital data with its fast electronic retrieval and processing.



- Among **EEPROM**, there are **flash memory**, ferroelectric RAM, magnetoresistive RAM, resistive RAM, phase-change RAM

# Memory Architecture

(random access memory)



❑ Both RAM and ROM share the same basic **memory architecture**.

➤ It consists of an array of **storage cells** with  $2^M$  columns and  $2^N$  rows.

➤ Each **storage cell** (or called **memory cell**) can store one **bit** of digital data.



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# Storage Cell or Memory Cell

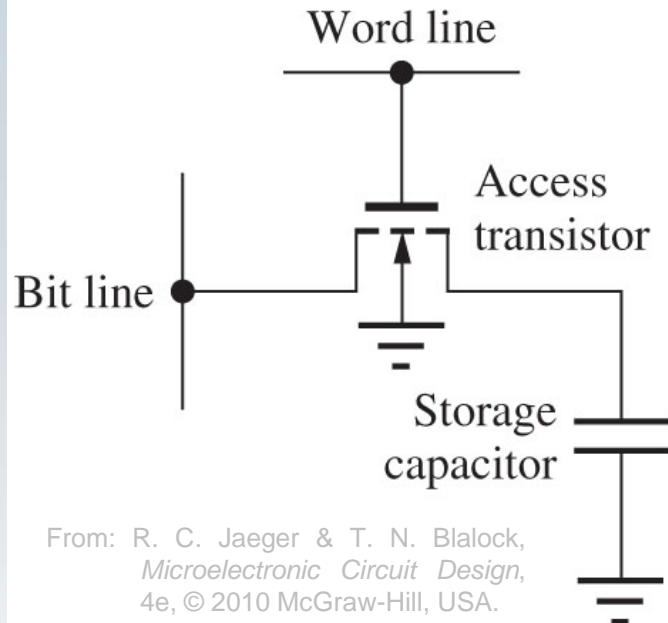
(varying from RAM to ROM)

- ❑ The **memory cell** varies from RAM to ROM.
- ❑ There are two types of RAM, namely **static RAM** (SRAM) and **dynamic RAM** (DRAM), and their **memory cells** are different.
  - The **SRAM** and **DRAM** have their trade-off in the **access time** and **memory density** (i.e. amounts of digital data stored per unit chip area). It is again performance and cost trade-off.
- ❑ Regardless the types of RAM or ROM, the **memory cell** uses typically the **voltage** or **charge** to store digital data.
  - **Information** must be *represented* by **physical states** when stored or processed.

# Memory Cell of Dynamic RAM

(one transistor & one capacitor)

- ❑ The **memory cell** of the **DRAM** typically consists of only two devices: a transistor and a capacitor.



From: R. C. Jaeger & T. N. Blalock,  
*Microelectronic Circuit Design*,  
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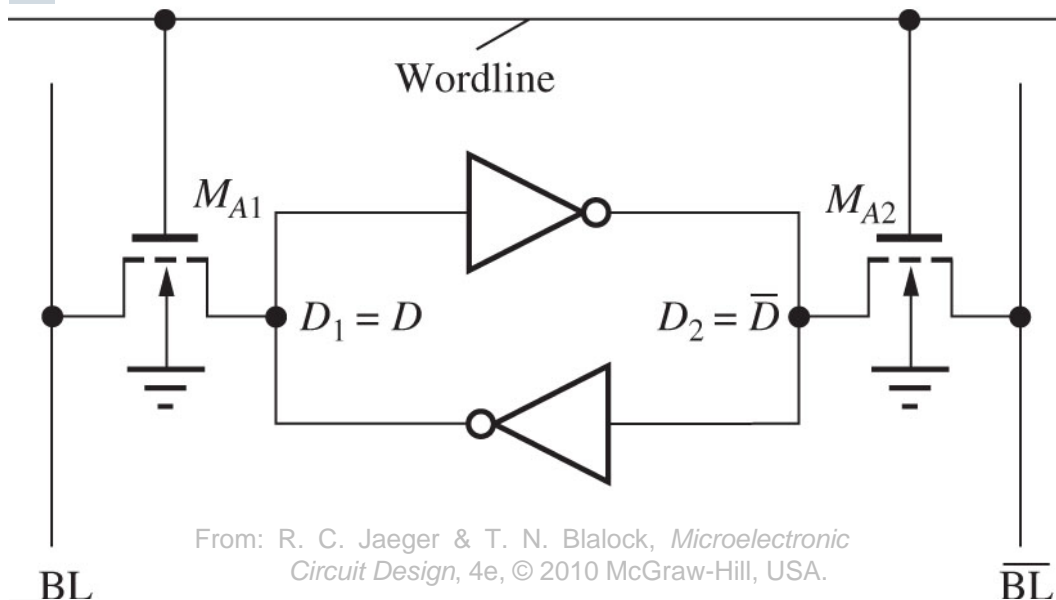
- The **charge** on the capacitor is used to store one bit of digital data.
- Since the **charge** on the capacitor *decays* with a finite time constant (about a few millisecond), a ***periodic refresh*** is needed to restore the charge so that the DRAM does not lose the memory.

- Using only two devices in each memory cell, DRAM can be of very high memory density.

# Memory Cell of Static RAM

(two inverters for bistable flip-flop)

- ❑ The **memory cell** of the **SRAM** consists of a basic bistable flip-flop circuit that needs only an applied DC voltage to retain its memory.
  - The bistable flip-flop circuit can be built by two **inverters**.



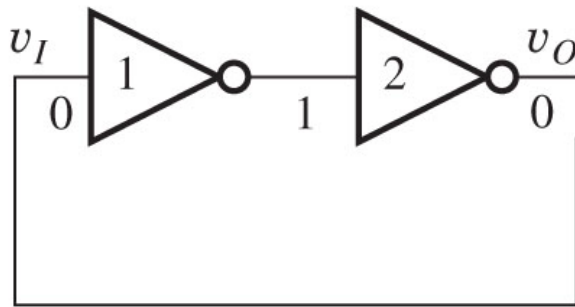
- Typically six transistors are used.
  - Compared with the DRAM, no refresh cycle is needed to retain the memory.
- ⇒ static



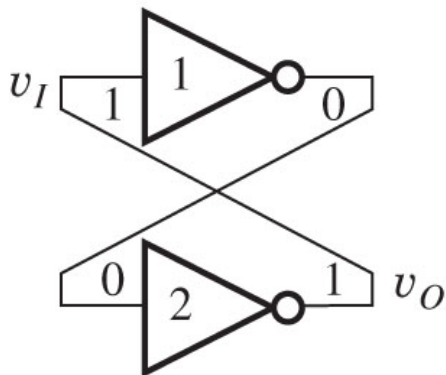
# Memory Cell of Static RAM

(cross-coupled inverter pair)

- ❑ The basic electronic storage part in the SRAM cell consists of two **inverters** connected in a loop.



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*Microelectronic Circuit Design*,  
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- The output of the second inverter is fed back to the input of the first inverter.
- It forms a logically stable configuration, having two stable states. It is therefore called a **bistable circuit**.
- The alternate representation in the form of a pair of **cross-coupled** inverters is often called a **latch**.
- The inverter **voltage transfer characteristics** can be used to study the circuit behaviour.



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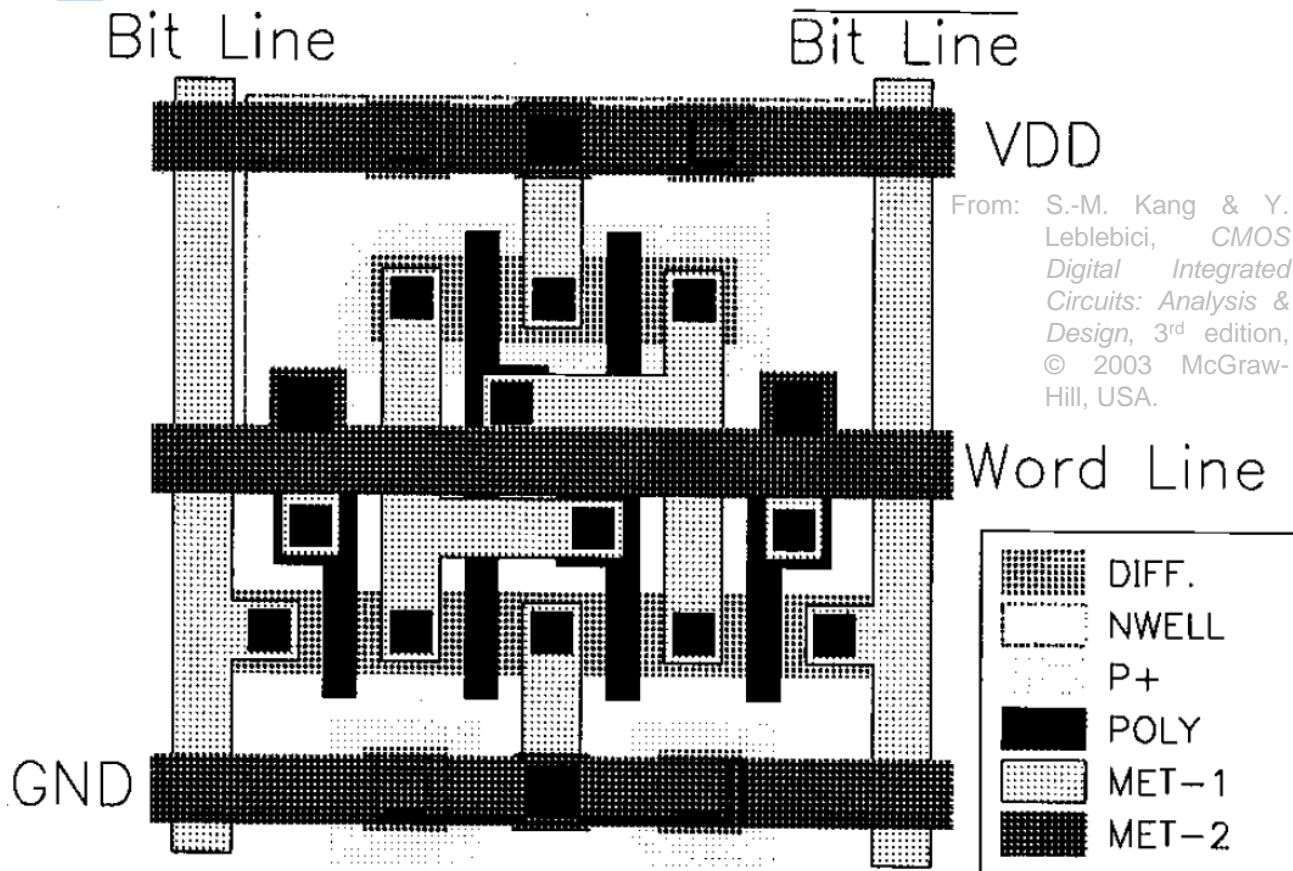
(six transistor implementation)

- A CMOS inverter logic gate is formed by one *p*-channel and one *n*-channel MOSFETs.
- Such an implementation is called a *six-transistor* (6T) **SRAM cell**.



# Memory Cell of Static RAM

(layout of 6T SRAM cell)



From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3<sup>rd</sup> edition, © 2003 McGraw-Hill, USA.

- The **6T SRAM cell** can be implemented with the IC layout as shown here.
- Note that the MOS transistor sizes are not optimised here.

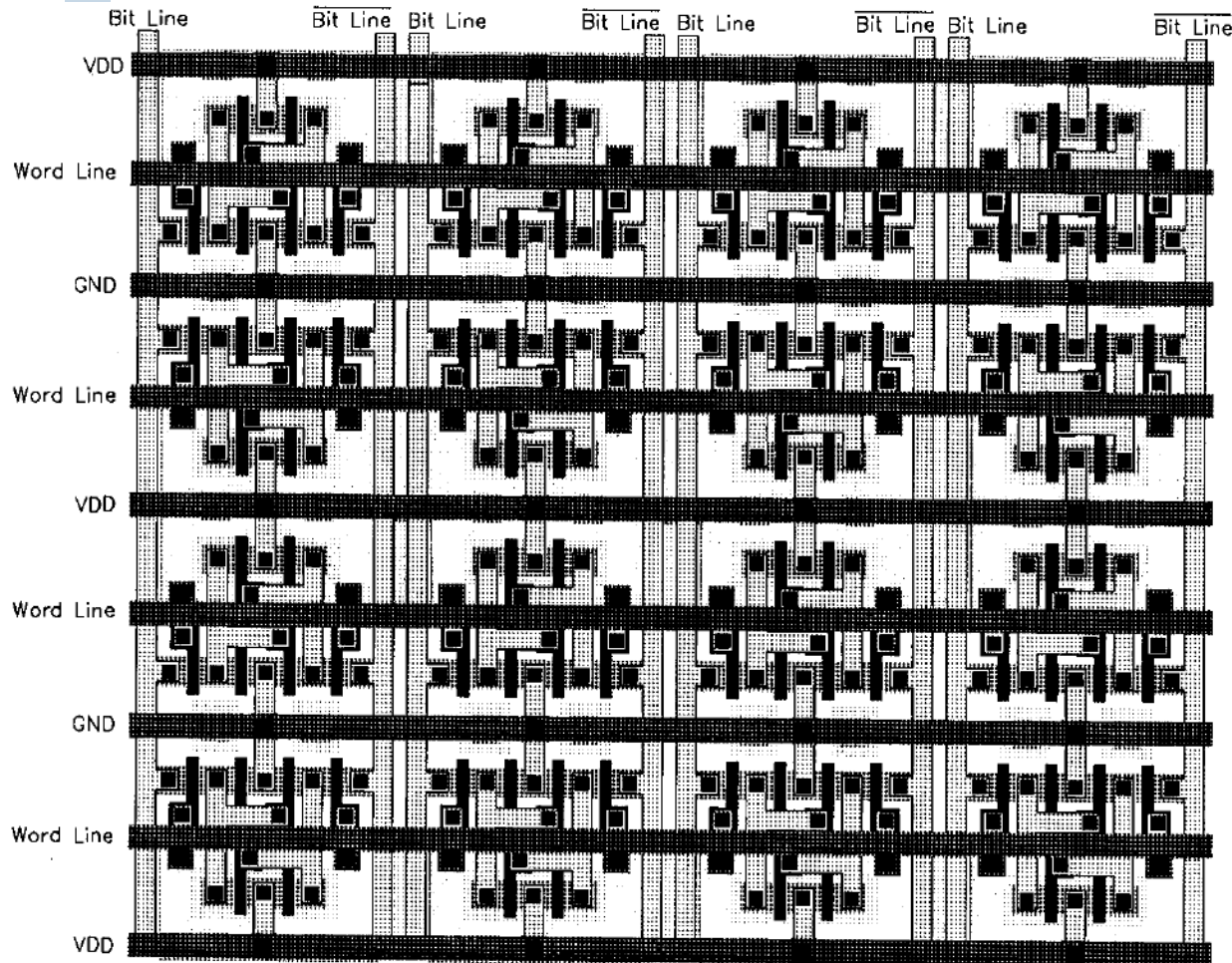
➤ Can you recognise the six transistors and determine their rough sizes?



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# Memory Cell of Static RAM

(layout of 6T SRAM cell)



- ❑ The 6T SRAM cell layout are duplicated in an array of  $2^M$  columns and  $2^N$  rows for storing  $2^{M+N}$  bits of digital data.
- ❑ The IC layout shown here is a 16-bit SRAM.

From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3<sup>rd</sup> edition, © 2003 McGraw-Hill, USA.



(sense amplifier)

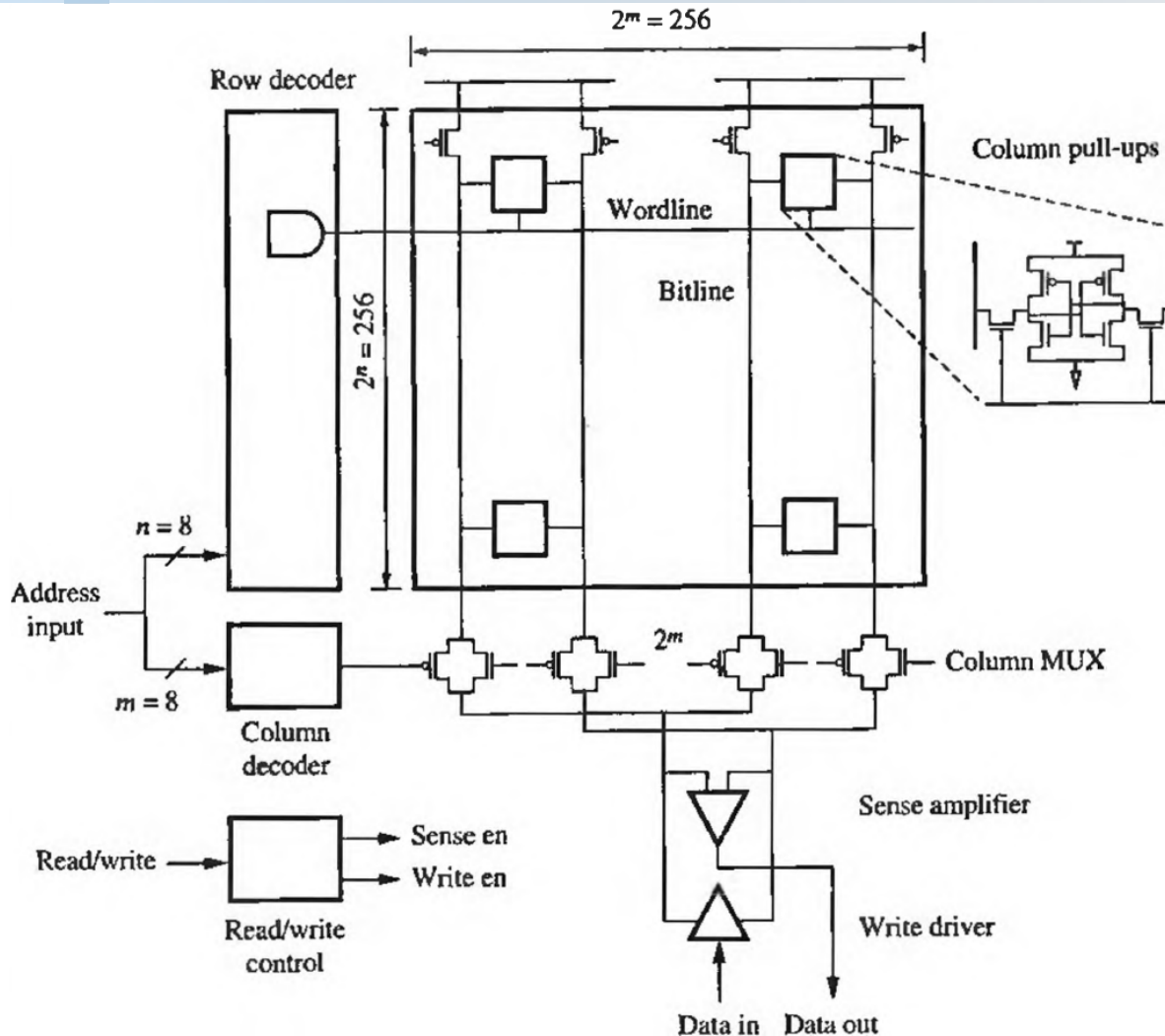
- The sense amplifier typically pre-charges the capacitors  $C_{BL}$  of the **bit line** (BL) to a voltage of half of the  $V_{DD}$ .
- When the **word line** (WL) is activated, voltage signals of the bistable circuit pass to  $C_{BL}$  via  $M_{A1}$  &  $M_{A2}$ .





# Memory Cell of Static RAM

(sense amplifier)

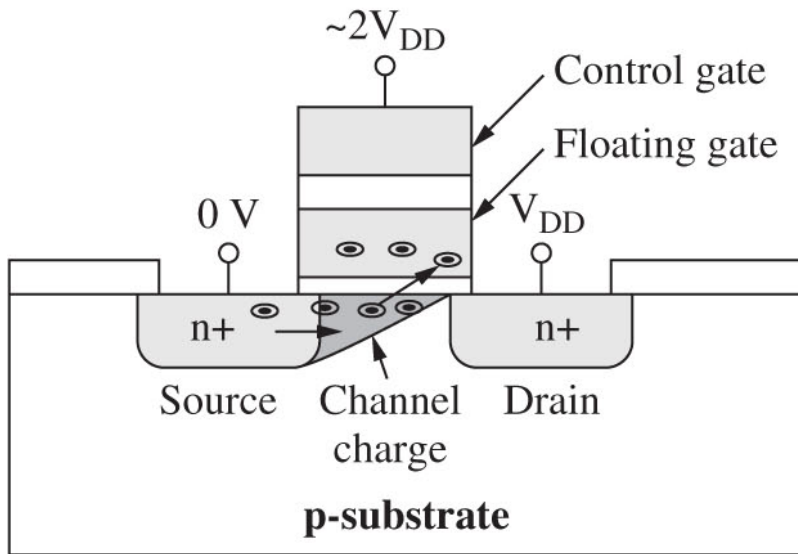


- The **sense amplifier** (and also the write driver) can be shared among multiple memory cells by using circuits to select the memory cells.

# Memory Cell of EEPROM

(electrically erasable programmable)

- ❑ In the case of the ROM, the **memory cell** can consist of only one device (e.g. transistor).



From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.

- ❑ In the electrically erasable programmable ROM (EEPROM), the device in the memory cell is a MOSFET with a control gate and a floating gate.
  - Charges (namely electrons) are stored in the floating gate.

- Such EEPROM is also known as **flash memory**, used in USB memory sticks.

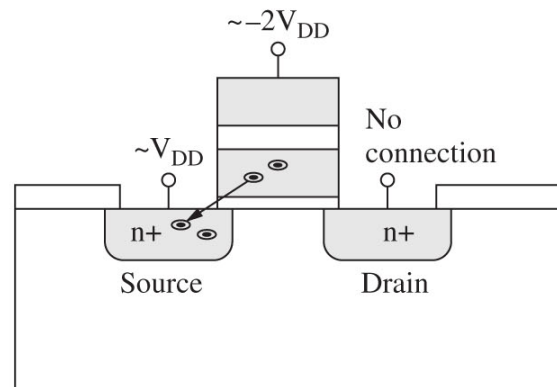
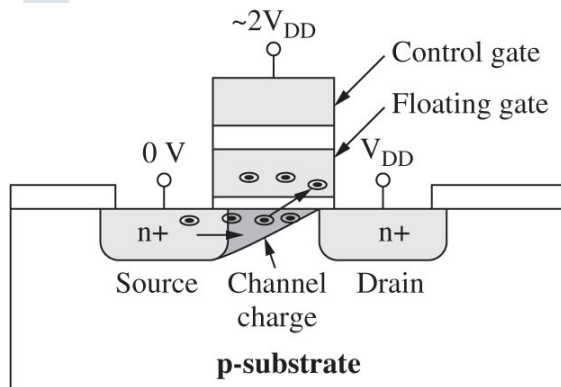


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# Memory Cell of EEPROM

(threshold voltage of MOS transistor)

- ❑ The presence of charges in the **floating gate** give different **threshold voltage**  $V_{Tn}$  *sensed* at the control gate of the MOS transistor.
  - Reading data involves *sensing* the  $V_{Tn}$  of the transistor.
- ❑ Erasure of data requires a voltage (+ve or -ve) of larger magnitude applied to the **control gate** to introduce or remove charges into or from the **floating gate**.



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*Microelectronic Circuit Design*,  
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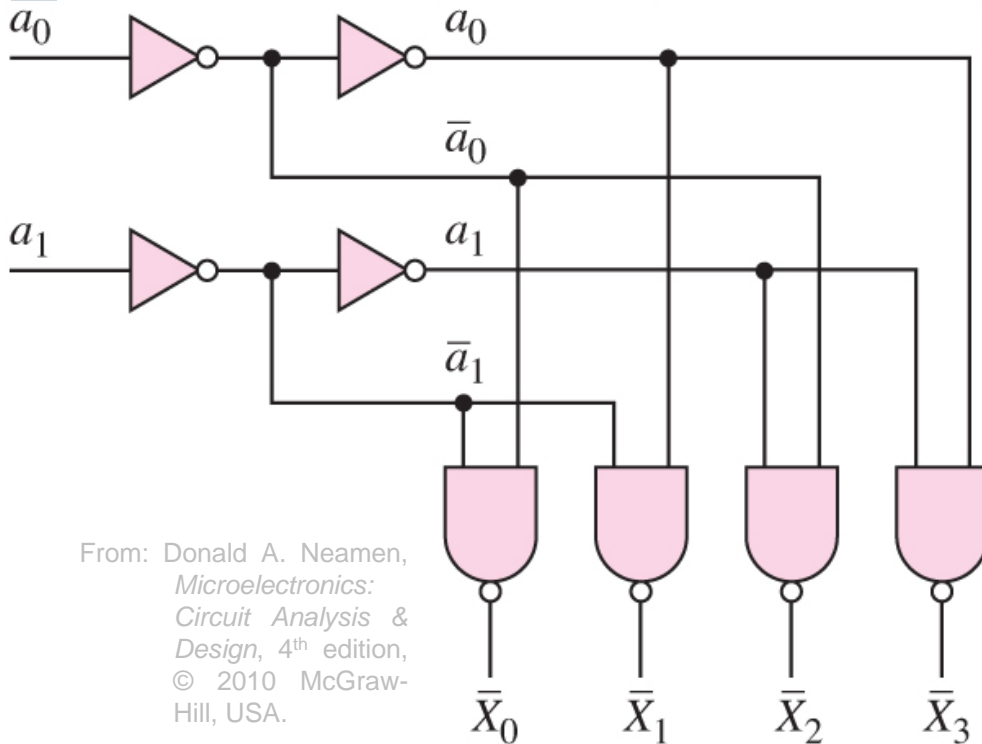
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# Address Decoder

(use combinational logic circuits)

- ❑ When the **memory cells** are arranged in an **array**, **address decoders** are needed to read/write data from/to specific cells.



From: Donald A. Neamen,  
*Microelectronics:  
Circuit Analysis &  
Design*, 4<sup>th</sup> edition,  
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Hill, USA.

- Address decoders are **combinational logic circuits** and can be implemented using basic logic gates.
- A 2-bit address decoder shown here can address four rows or columns.

# SRAM vs. DRAM

(memory density)

- ❑ It can be seen that the **SRAM** cell occupies relatively much chip area.
  - As a result, the memory size of the **SRAM** can be quite limited. A modern microprocessor has 25 MB SRAM.
  - $1 \text{ MB} = 1024 \text{ KB}$ ;  $1 \text{ KB} = \underline{1024} \text{ byte} = \underline{2^{10}} \text{ byte}$ ;  $1 \text{ byte} = 8 \text{ bit}$ . How many SRAM cells are needed for storing 25MB digital data?
- ❑ With only one transistor and one capacitor, the DRAM cell use up much less chip area than that of SRAM.
  - The DRAM can have very high memory density (e.g. 16 GB).  $1 \text{ GB} = 1024 \text{ MB}$ . But it has lower speed and larger power consumption.

# SRAM, DRAM & Flash Memory

(applications)

- ❑ With much faster read/write speed (typically 10 ns or less) of the **SRAM**, it is used as **cache memory** in microprocessors.
  - With its relatively lower cost but reasonable read/write speed, the **DRAM** is used as the main computational memory of the computer.
- ❑ The **flash memory** has only one transistor in the memory cell.
  - As a result, it has somewhat even higher memory density.
  - It is used for memory cards, USB memory sticks and solid-state drives.
  - However, its write speed can be very low ( $> 10 \mu\text{s}$ ).



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