The methods to determine flat-band voltage VFB in semiconductor of a MOS structure

Article · January 2010

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The methods to determine flat-band voltage V_{FB} in semiconductor of a MOS structure

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Abstract - One of the most important parameters of the MOS (metal-oxide-semiconductor) structure is the flat-band voltage V_{FB} in semiconductor. This voltage influences the threshold voltage V_T, which is the fundamental parameter of any MOS device. Hence, the V_{FB} voltage has a great practical importance and the precise and accurate determination of its value is very important.

In this paper, the measurement techniques for V_{FB} voltage determination are presented. Most of these methods are based on electric measurements of capacitance-voltage $C(V_G)$ characteristics of MOS structure. The results show considerable spread of V_{FB} values, which exceeds the tolerances allowed by the technology of modern, scaled down MOS integrated circuits.

Also, the photoelectric method of the V_{FB} voltage determination is described. This method, called LPT (Light Pulse Technique), is based on simultaneous illumination (modulated light) of the semitransparent gate and polarization of the substrate of the MOS structure. The expected accuracy of the LPT method is ± 10 mV, while the accuracy of above mentioned electric methods is rarely better than ± 50 mV.

There is no other method with an accuracy similar to the accuracy of the LPT method. It causes that, despite many advantages of the LPT method, the determination of the absolute accuracy of this method is still problematic.

I. INTRODUCTION

The flat-band voltage V_{FB} in semiconductor of a MOS structure in modern, scaled down devices plays significant role in determining the value of the threshold voltage V_T. The V_T voltage, being the most important parameter of any MOS transistor decides, for example, about power consumption of this transistor.

The V_{FB} voltage is the gate voltage required to make the energy bands in the semiconductor flat up to the semiconductor-dielectric interface, as schematically shown in Fig. 1.

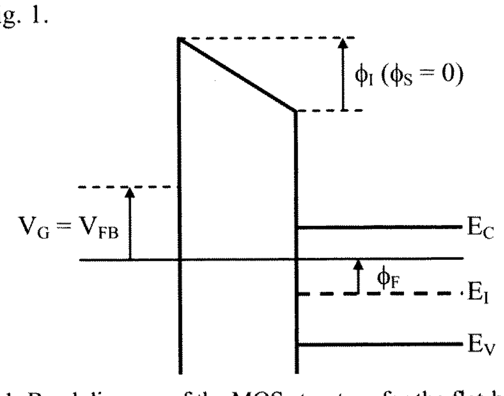

Fig. 1. Band diagram of the MOS structure for the flat-band state in semiconductor ($\phi_S = 0$).

The V_{FB} voltage is given by the well known formula [1]:

$$V_{FB} = \phi_{MS} - \frac{Q_{eff}}{C_{OX}} \tag{1}$$

where: ϕ_{MS} – contact potential difference in MOS structure [V], Q_{eff} – effective charge in dielectric [C/cm^2], C_{OX} – dielectric capacitance [F/cm^2].

The relative importance of the ϕ_{MS} and Q_{eff} values for the value of V_{FB}, given by (1), changes with time, as new technology is being introduced. The better control of the technological process is achieved, hence lower Q_{eff} values are typically obtained. With decreasing thickness of the dielectric layer the decreasing influence of the ratio Q_{eff}/C_{OX} on V_{FB} value is observed. It means, that the ϕ_{MS} factor dominates the V_{FB} value.

In this paper, different measurement techniques for flat-band voltage V_{FB} determination are discussed. A comparison between results obtained by these techniques is also given.

II. METHODS OF THE V_{FB} DETERMINATION

The methods of the flat-band voltage V_{FB} determination can be divided into three groups: computational and graphical both based on $C(V_G)$ characteristic measurement of MOS structure and photoelectric method, in which the light is a medium. Below the short description of five different methods is presented.

A. Comparative method

The comparative method is a classical procedure used for analyzing high frequency $C(V_G)$ characteristics of a MOS structure. This method consists in comparing an experimental $C(V_G)$ characteristic with a characteristic calculated for an ideal MOS capacitor. The calculations should be made for the same material and design parameters as in the case of the measured capacitor (e.g. doping concentration N_D, electric permittivity of the dielectric ε_{OX}, dielectric thickness t_{OX}, intrinsic concentration n_i). Also, the temperature T used in calculations should be equal to the temperature, in which the measurement was performed.

The flat-band state in semiconductor for an ideal MOS structure appears when the gate voltage $V_G = 0$, it means that the capacitance of the flat-band state C_{FB} is defined for zero bias of the structure. Hence, the shift between both theoretical and experimental characteristics for C_{FB} value a measure of flat-band voltage V_{FB} in semiconductor. This situation is schematically shown in Fig. 1.

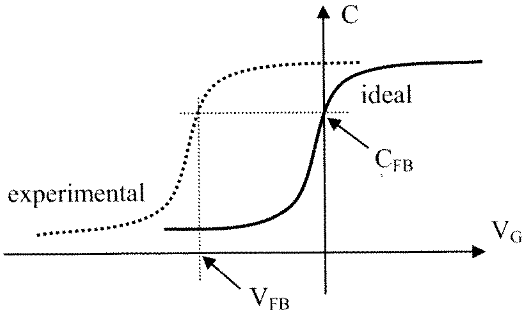

Fig. 2. The experimental and ideal $C(V_G)$ characteristics. The shift between them for C_{FB} capacitance indicates V_{FB} voltage.

The comparative method, although well presents the concept of the V_{FB} voltage, is time-consuming due to the calculation of the whole theoretical characteristic. The total accuracy of this method is relatively good and depends on accuracies of every parameter taken into account in the calculations.

B. Calculation C_{FB} method

In this method the experimental $C(V_G)$ characteristic measured on MOS structure and the value of the C_{FB} capacitance obtained by appropriate calculations is needed. The C_{FB} value is defined as [1]:

$$C_{FB} = \frac{C_{OX} \cdot C_{sFB}}{C_{OX} + C_{sFB}} \tag{2}$$

where: C_{sFB} – semiconductor surface capacitance [F/cm^2].

The C_{sFB} value is calculated as follows:

$$C_{sFB} = \frac{\varepsilon_s \varepsilon_0}{L_D} \tag{3}$$

where: ε_S – electric permittivity of the semiconductor, ε_0 – electric permittivity of the vacuum [F/cm], L_D – Debey's length [cm].

The L_D value can be expressed:

$$L_D = \sqrt{\frac{kT\varepsilon_s \varepsilon_0}{q^2 N_D}} \tag{4}$$

where: k – Boltzmann's constant [J/K], T – temperature [K], q – electron charge [C], N_D – doping concentration [1/cm^3].

All the components of (4) are usually known excluding the doping concentration N_D. The N_D value can be calculated by using two separate formulas, both based on $C(V_G)$ measurement.

One method uses the slope $(d/dV_G)\cdot(1/C^2)$ of the linear part of $1/C^2(V_G)$ characteristic and the N_D value is calculated by formula:

$$N_D = \frac{2}{q\varepsilon_s \varepsilon_0} / \left(|slope| \cdot A^2 \right) \tag{5}$$

where: A – gate area [cm^2].

The second method is an iterative method which uses values of the capacitances measured in the accumulation range C_{OX} and inversion range C_{MIN}. The N_D value is extracted from the formula [2]:

$$\frac{C_{sf}}{A} = \sqrt{\frac{q^2 \varepsilon_s \varepsilon_0 N_D}{2kT\left\{ 2\ln\left(\frac{N_D}{n_i}\right) - 1 + \ln\left(1.15 \cdot \left[\ln\left(\frac{N_D}{n_i}\right) - 1\right]\right)\right\}}} \tag{6}$$

where: n_i – intrinsic concentration [1/cm^3] and C_{sf} given as:

$$C_{sf} = \frac{C_{OX} \cdot C_{MIN}}{C_{OX} - C_{MIN}} \tag{7}$$

Obviously, small differences between N_D values obtained by (5) and (6) exist, as will be shown in Section IV.

In the literature one can find some formulas describing the intrinsic concentration n_i parameter [3-5]. In this work the following formula was used [5]:

$$n_i = 5.29 \cdot 10^{19} \left(\frac{T}{300} \right)^{2.54} \exp\left(-\frac{6726}{T} \right) \tag{8}$$

Finally, having measured $C(V_G)$ characteristic and having calculated C_{FB} value (using the same parameters of the structure) the V_{FB} value is given by the corresponding value of the gate voltage V_G for C_{FB} capacitance. Fig. 3 shows a schematic illustration of this method.

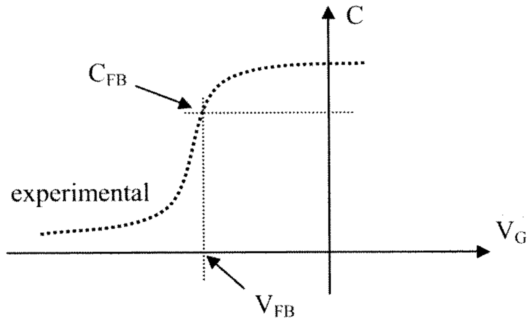

Fig. 3. The C_{FB} value placed on experimental $C(V_G)$ characteristic indicates the gate voltage $V_G = V_{FB}$ for flat-band state in semiconductor.

This method needs some calculations and as it was in the case of comparative method, the accuracy depends on accuracies of the components which determine the C_{FB} capacitance value.

C. Graphical $[(C_{OX}/C_{MOS})^2-1](V_G)$ method

Approximating the depletion range of the measured $C(V_G)$ characteristic the relationship between capacitance of the structure C_{MOS} and gate voltage V_G can be obtained [6]:

$$\left(\frac{C_{OX}}{C_{MOS}}\right)^2 - 1 = \frac{2C_{OX}{}^2}{qN_D\varepsilon_s\varepsilon_0}\left(V_G - V_{FB}\right) \quad (9)$$

This relation in a certain range is linear. Hence, making an extrapolation of this straight line and finding the point, at which extrapolated line intersect the $(C_{OX}/C_{MOS})^2$-1 = 0 axis the V_{FB} can be determined. The principle of this method is depicted in Fig. 4.

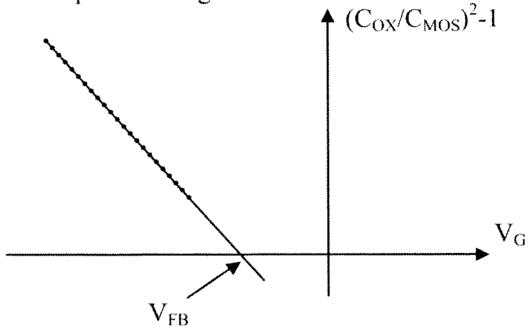

Fig. 4. The V_{FB} value is indicated by extrapolation of the linear part of the $[(C_{OX}/C_{MOS})^2-1](V_G)$ characteristic to the zero $[(C_{OX}/C_{MOS})^2-1]$ value.

The slope of the $[(C_{OX}/C_{MOS})^2-1](V_G)$ characteristic can be used to the determine of the doping concentration N_D.

This method does not need information about measured structure and the V_{FB} value is treated as an approximate value of this voltage. The simplifications are also made (e.g. constant doping concentration in the semiconductor, neglected influence of the surface trap charges) causing decrease of accuracy of this method.

D. Graphical f_1 and f_2 functions method

The fundamentals of this method were described in [7]. This method consists in measuring the $C(V_G)$ characteristic and afterward calculating two functions: f_1 which is a measure of the capacitance increment as an effect of changes of the gate voltage V_G, and f_2 which expresses the relation between structure capacitance C_{MOS} and capacitance in accumulation C_{OX}. These functions are given by following formulas:

$$f_1 = \frac{1}{\sqrt{\frac{3kT}{q}\frac{1}{C_{MOS}}\frac{dC_{MOS}}{dV_G}}} - 1 \quad (10)$$

$$f_2 = \frac{C_{MOS}}{C_{OX} - C_{MOS}} \quad (11)$$

Plotting both these functions in the same coordinate system the V_{FB} value can be determined as a point where functions f_1 and f_2 intersect. Also, the flat-band capacitance C_{FB} can be obtained by mapping this point on vertical axis for $V_G = 0$. The C_{FB} value obtained in this way allows to calculate the doping concentration N_D by using (2-4):

$$N_D = \frac{kT\varepsilon_s\varepsilon_0}{q^2 L_D{}^2} \quad (12)$$

Fig. 5 shows the dependence of both functions f_1 and f_2 on the gate voltage V_G.

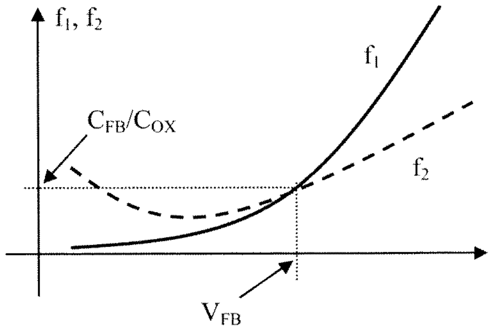

Fig. 5. The intersection point of the f_1 and f_2 functions indicates the V_{FB} value. Also, the C_{FB} capacitance for flat-band state in semiconductor can be determined.

E. Photoelectric LPT method

The LPT (Light Pulse Technique) method consists in illuminating the MOS structure with semitransparent metal gate by a series of light pulses (chopped light) and measuring the output signal from the structure [8,9]. This output current signal depends on the potential V_G applied to the MOS structure. The magnitude of these current pulses is a function of the semiconductor surface potential ϕ_S and when $\phi_S = 0$ then current pulses disappear. Thereby, finding the dependence of the magnitude of these current peaks (signal u) on the gate voltage V_G the determination of point at which current peaks disappear is possible. This point defines directly the flat-band voltage state in semiconductor ($V_G = V_{FB}$) [9] as shown schematically in Fig. 6.

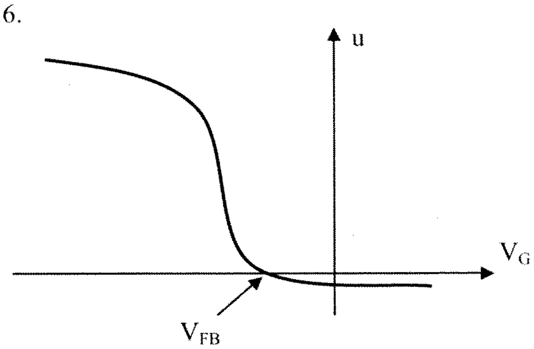

Fig. 6. The dependence of a measured signal u by the lock-in amplifier on V_G voltage. The point at which signal u intersects u = 0 axis indicates the V_{FB} value.

In contrast to above mentioned comparative and C_{FB} calculation methods the LPT method does not require any information about the investigated sample. The V_{FB} value is directly determined from measured characteristic $u(V_G)$ at point, where signal u changes sign.

The expected accuracy of the LPT method is ± 10 mV, while the accuracy of the V_{FB} determination methods based on measurement of the $C(V_G)$ characteristic is rarely better than ± 50 mV. It is the main goal of this paper to make a comparison between results obtained by different characterization techniques and find the total accuracy of each of them.

III. EXPERIMENTAL DETAILS

In this work measurements were made on Al–SiO_2–Si capacitors with semitransparent (t_{Al} = 35 nm) square (1x1 mm^2) gate. N-type substrates (ρ = 3-5 Ωcm) of <100> orientation were used. Wafers were thermally oxidized at temperature T = 1000 °C, in dry oxygen, to grow a SiO_2 layer of thickness t_{OX} = 20, 60 and 160 nm. Although SiO_2 layers of current technological interest are thinner than t_{OX} = 3 nm, we used thicker oxides to optimize the sensitivity of the applied electric and photoelectric methods.

Oxidized wafers were subsequently annealed in nitrogen for $t(N_2)$ = 120 min, at T = 1050 °C. The post metalization annealing was carried out for t = 20 min, at T = 450 °C in forming gas atmosphere.

All methods were used to obtain the V_{FB} value on each of measured structures to avoid differences in parameters of any structure.

IV. RESULTS AND DISCUSSION

To facilitate interpretation the methods of V_{FB} determination will be called by the same letters which were used in the subtitles in Section II.

Measurements of $C(V_G)$ characteristics on many MOS structures with three different dielectric layer thicknesses t_{OX} = 20, 60 and 160 nm were performed. In Fig. 7 an examples of such measurements are shown.

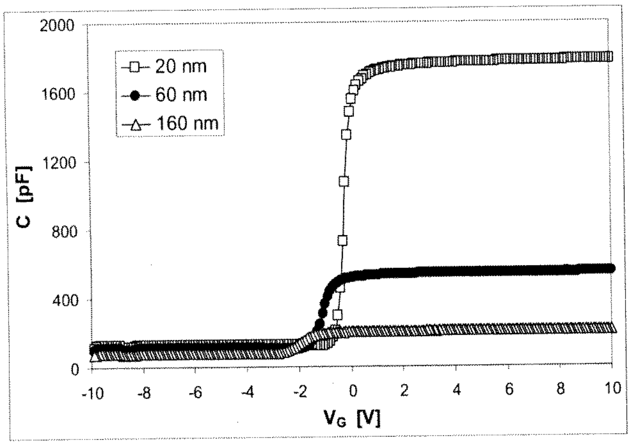

Fig. 7. Measured $C(V_G)$ characteristics for different dielectric thickness t_{OX} = 20, 60 and 160 nm.

Determination of the doping concentration N_D

Measurement results shown in Fig. 7 allow to determine the N_D values which will be used in V_{FB} calculations. The N_D values can be obtained by two different ways: from slope of $1/C^2(V_G)$ characteristic using (5) and from measured C_{OX} and C_{MIN} capacitance values using (6). The comparison between N_D values calculated by these formulas is shown in Table I. Also, the average values of the oxide charges Q_{eff} for each of dielectric thicknesses t_{OX} were estimated. As it is shown in Table I the Q_{eff} values are quite big, although they are stable and repeatable for all measured structures.

TABLE I
N_D VALUES CALCULATED FROM (5) AND (6)
T = 298 K, $n_i = 8.2\cdot10^9$ 1/cm^3, A = 0.01 cm^2

t_{OX} [nm]	20	60	160
C_{OX} [pF]	1777.88	545.19	208.11
C_{MIN} [pF]	113.60	97.58	73.31
Q_{eff} [C/cm^2]	$5.027\cdot10^{-8}$	$5.441\cdot10^{-8}$	$3.364\cdot10^{-8}$
Method	N_D [1/cm^3]		
Slope (5)	$1.144\cdot10^{15}$	$1.111\cdot10^{15}$	$9.753\cdot10^{14}$
$C_{OX}.C_{MIN}$ (6)	$1.150\cdot10^{15}$	$1.098\cdot10^{15}$	$9.876\cdot10^{14}$

The influence of such a small differences between N_D values calculated on the basis of (5) and (6) on V_{FB} value is negligible. From many measurements and calculations the following conclusions appear:

- the linear part of $1/C^2(V_G)$ characteristic is longer for structures with thicker dielectric layer. Hence the extrapolation of this line is more accurate (for measurements made with the same gate voltage V_G step), as shown in Fig. 8;
- the formula (6) is very sensitive to changes of C_{MIN} and C_{OX} values. Any mistake in determination of these values causes discrepancies between calculated N_D values. The influence of C_{MIN} is stronger on N_D value than influence of C_{OX};
- it is better to use formula (5). This manner of calculating N_D value does not require information about temperature T as in the case of formula (6). Additionally, allows to avoid mistakes in measurements of C_{OX} and C_{MIN} values.

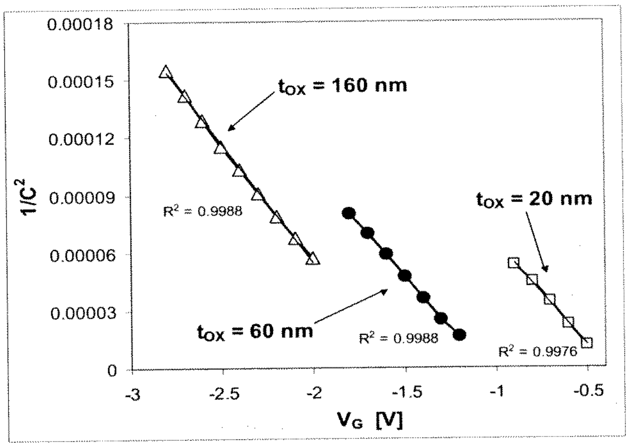

Fig. 8. Linear parts of measured $1/C^2(V_G)$ characteristics for structures with dielectric thickness t_{OX} = 20, 60 and 160 nm.

Also, for the comparison the N_D value for MOS structure (t_{OX} = 60 nm) was calculated. It was done by using method D described in Section II. The common point of f_1 and f_2 functions determines the C_{FB}/C_{OX} ratio and further N_D can be calculated by using (12). The obtained N_D value is equal to $1.035 \cdot 10^{15}$ and differs considerably (about 7%) from values shown in Table I for the same structure.

Determination of the flat-band voltage V_{FB}

All methods (A-E) described in Section II were applied to the same measured MOS structure.

To obtain V_{FB} by LPT method (E) the measurements of $u(V_G)$ characteristics for structures with different dielectric thickness t_{OX} were made. The examples of such measurements are shown in Fig. 9.

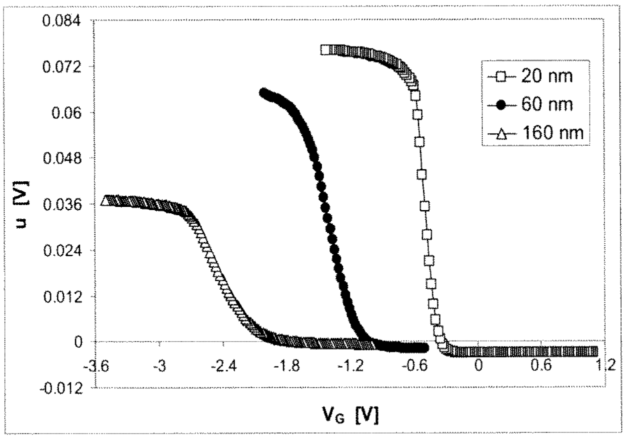

Fig. 9. Measured $u(V_G)$ characteristics for different dielectric thickness t_{OX} = 20, 60 and 160 nm.

As it is shown in Fig. 9 in the inversion region signals u reach a considerable value, decreasing with increasing V_G in the depletion region. At $V_G = V_{FB}$ the u value changes sign, becoming negative in the accumulation region. The absolute value of signal u in accumulation range and signal in inversion range are larger for structures with thinner t_{OX}. On the other hand the slope of signal u in depletion range is smaller for structures with thinner t_{OX}. These results were also confirmed by calculations of the theoretical $u(V_G)$ characteristics.

Because of small values of signal u in accumulation the precise determination of position of horizontal axis relative to measured signal is very important. In Fig. 10 the extension of vertical axis for small u values is presented.

It is clearly shown in Fig. 10 that any mistake in position of the horizontal axis can significantly change the obtained V_{FB} value. For structures with higher thickness of dielectric layer t_{OX} the bigger mistake in V_{FB} value can be made by inappropriate horizontal axis position. In this work the position of u = 0 axis was verified by calculations of theoretical signals.

The precision and the reproducibility of the V_{FB} voltage determination (point, at which measured signal changes sign) are very good (± 5 mV). The only problem is to define the absolute accuracy of the LPT method.

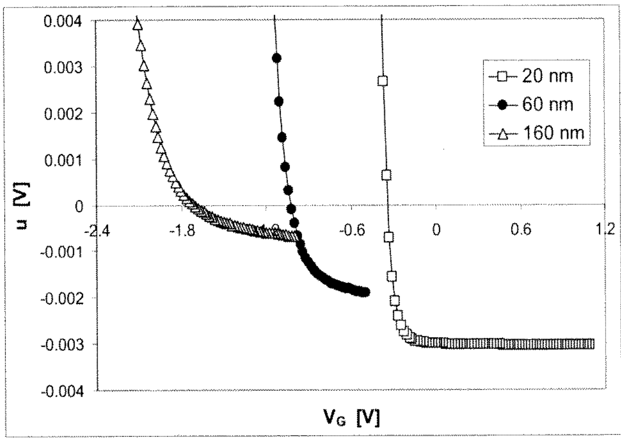

Fig. 10. Measured $u(V_G)$ characteristics for different dielectric thickness t_{OX} = 20, 60 and 160 nm.

The V_{FB} values obtained for all thicknesses of dielectric layer of the MOS structures by all methods described in Section II are shown in Table II.

TABLE II
V_{FB} VALUES OBTAINED BY A-E METHODS

t_{OX} [nm]	20	60	160
Method	V_{FB} [V]		
A	-0.346	-1.046	-1.624
B	-0.349	-1.054	-1.682
C	-0.375	-1.088	-1.744
D	-0.276	-1.021	-1.646
ave.	-0.337	-1.052	-1.674
st. dev.	0.037	0.024	0.045
E	**-0.341**	**-1.025**	**-1.710**

The average and standard deviation values were calculated for methods based on $C(V_G)$ characteristic measurements (A-D). The V_{FB} values obtained by LPT method (E) are in good agreement with average values of the A-D methods, although the st. dev. of V_{FB} values for all thicknesses t_{OX} is significant. These results confirmed that the accuracy of the methods based on electric $C(V_G)$ measurements is rarely better than ± 50 mV. The expected accuracy of the photoelectric LPT method is assumed to be better (± 10 mV), although the definition of the total accuracy of the photoelectric LPT method is still problematic.

V. CONCLUSION

The comparison of different measurement and calculation techniques of determination of the flat-band voltage V_{FB} in semiconductor of the MOS structure have been performed. The results obtained for methods based on electric $C(V_G)$ characteristic measurements show considerable differences of the V_{FB} values and total accuracy of these methods is not better than ± 50 mV. This accuracy depends on many factors, but the most important are: proper values of parameters used in calculations (e.g. doping concentration N_D, temperature T), high precision of $C(V_G)$ characteristic measurements (e.g. capacitance in inversion range C_{MIN}), and other factors as discussed in the text.

Results obtained by photoelectric LPT method in many cases are different from values obtained by electric methods. The average V_{FB} values obtained for MOS structures with different dielectric thicknesses t_{OX} by four different electric methods are quite similar to the LPT method results. Differences are not bigger than 40 mV and decrease with decreasing t_{OX}.

Despite many advantages of the LPT method, its good precision and reproducibility (± 5 mV), the absolute accuracy of this method can not be strictly defined. It is because of lack of another measurement technique with comparable or better accuracy than the precision and reproducibility of LPT method.

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