nMOS logic IC design

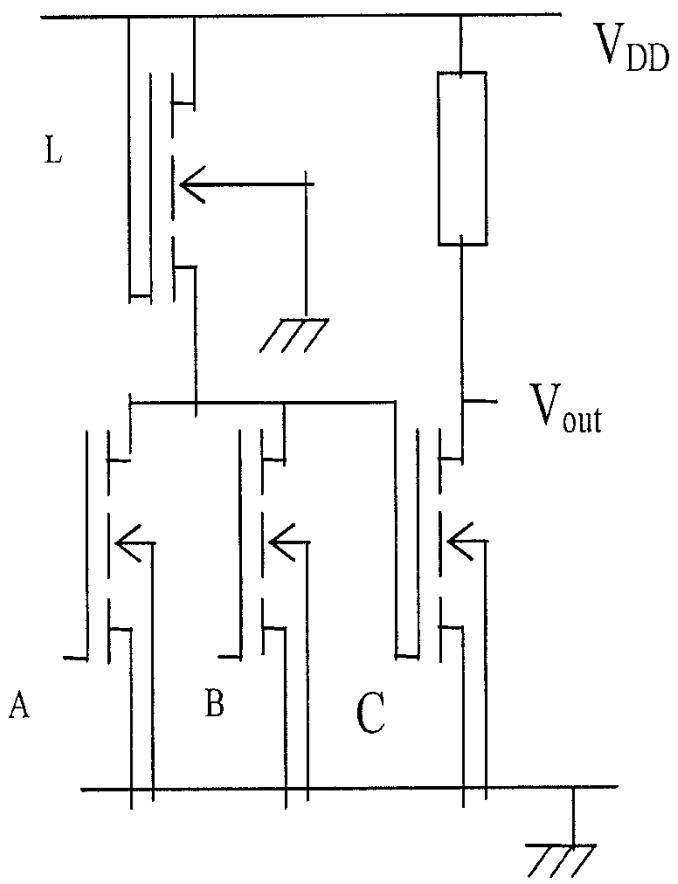
Material developed by Prof. C. Z. Zhao

OUTLINE

- **nMOS logic (examples)**
  - Truth table
  - Calculation
  - Layout
- **Design Exercise 2017 (15% marks)**

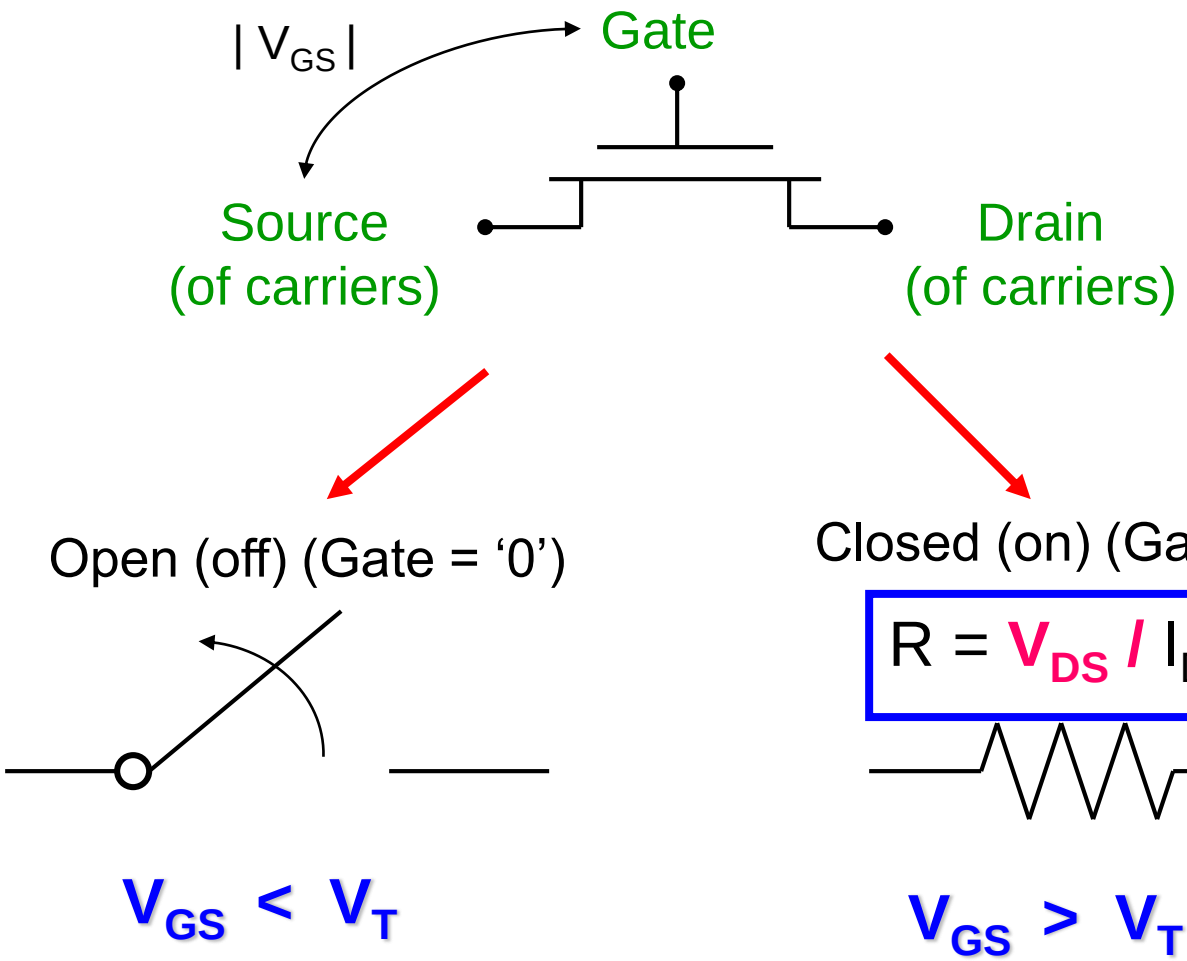
nMOS IC logic family

- Inverters
- NAND gate
- NOR gate
- General gate
  - Complicated gate
  - Example →



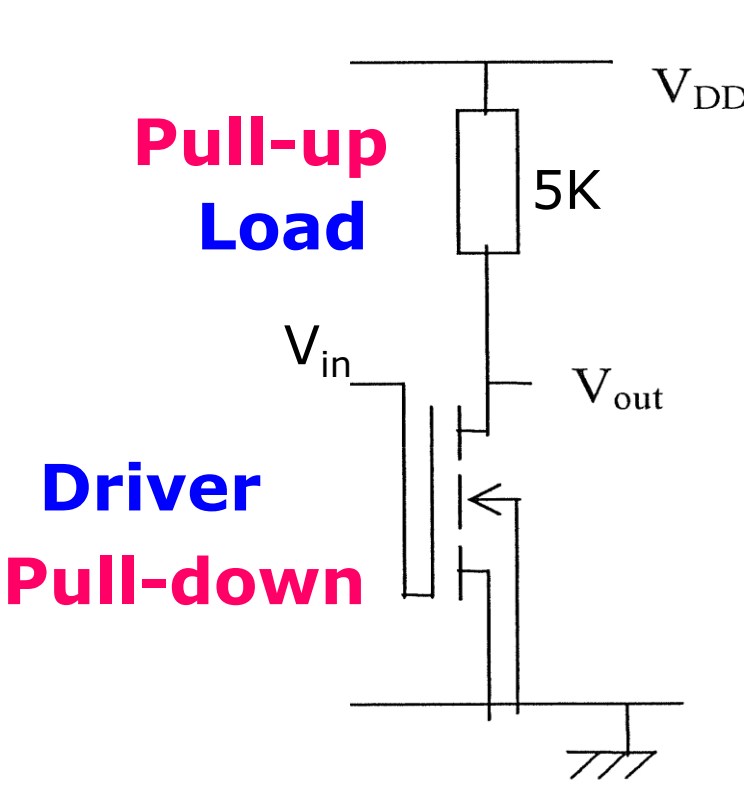
Switch Model of nMOS Transistor

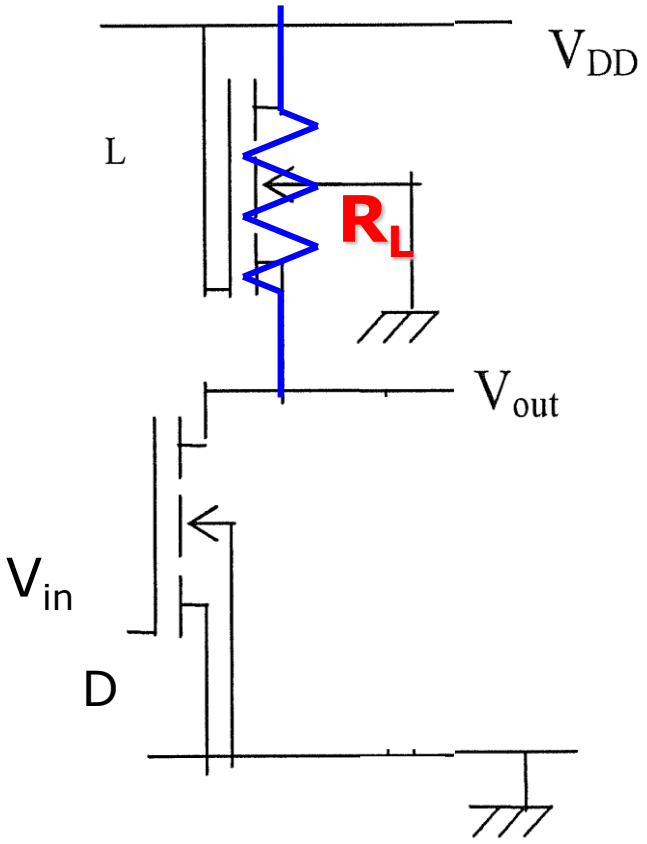
PL



If $V_{GS} = V_{DD}$, the nMOSFET is on.

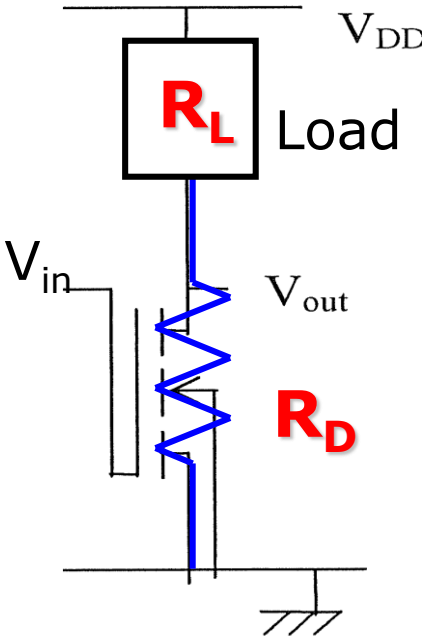
nMOS Logic (Inverters)





$V_{in} = V_{GS}$, $V_{out} = V_{DS}$

nMOS Logic (Inverter)



Vin	*Vout*
0 (0V)	1 (V_{DD})
1 (V_{DD})	**0 (0V)**

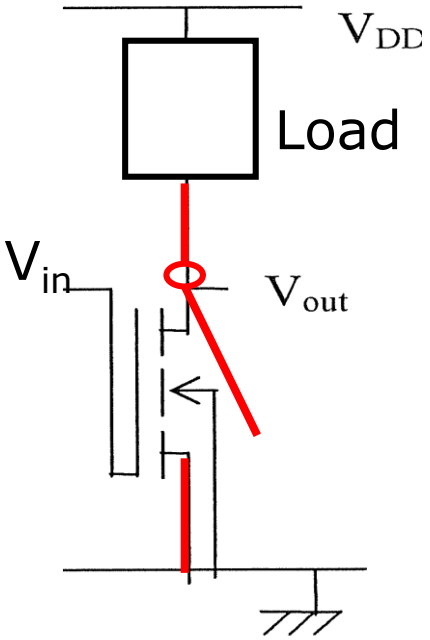
V_{in} = V_{DD} causes NMOS transistor to be on (in triode). Low effective resistance of transistor causes voltage divider with V_{out} **near** 0V.

If $R_L >> R_D$ (large R_L)

$$V_{out} = \frac{R_D}{R_L + R_D} V_{DD} \approx 0$$

$$V_{out} << V_T$$

nMOS Logic (Inverter)



Vin	*Vout*
0 (0V)	**1 (V_{DD})**
1 (V_{DD})	0 (0V)

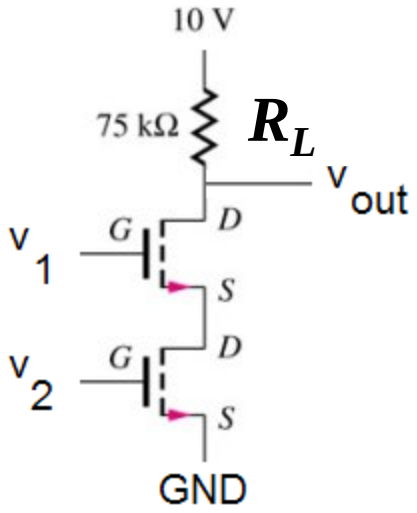
V_{in} = V_{DD} causes NMOS transistor to be on (in triode). Low effective resistance of transistor causes voltage divider with V_{out} **near** 0V.

$$V_{out} = \frac{R_D}{R_L + R_D} V_{DD} \approx 0$$

V_{in} = 0V causes NMOS transistor to be off (cutoff). High effective resistance of transistor causes voltage divider with V_{out} **near** V_{DD}.

$$V_{out} \approx V_{DD} \qquad \text{If } V_{in} << V_T$$

nMOS Logic (NAND)

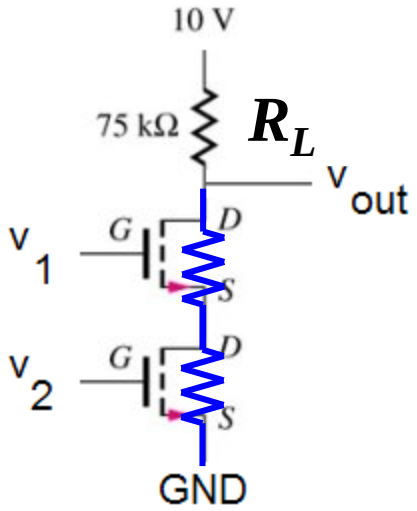


V_1	V_2	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

$V_1 = V_2 = 10$V causes both NMOS transistors to be on (in triode). Low effective resistance of transistors causes voltage divider with V_{out} **near** 0V.

$V_1 = 0$V or $V_2 = 0$V (or both) cause one or both NMOS transistors to be off (cutoff). High effective resistance of series transistors cause voltage divider with V_{out} near 10V.

nMOS Logic (NAND)

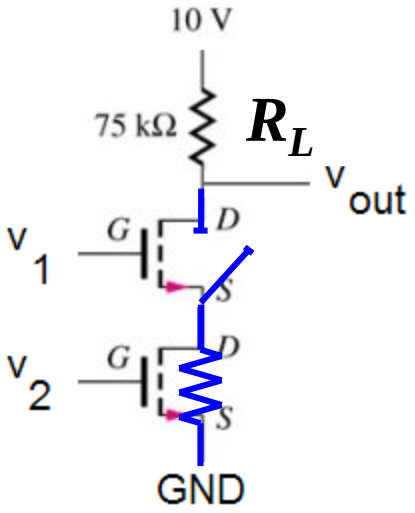


$V_1 = V_2 = 10$V causes both NMOS transistors to be on (in triode). Low effective resistance of transistors causes voltage divider with V_{out} **near** 0V.

$$V_{out} = \frac{R_1 + R_2}{R_L + R_1 + R_2} V_{DD} \approx 0 \quad (\text{Large } R_L)$$

V_1	V_2	V_{out}
0	0	1
0	1	1
1	0	1
1	**1**	**0**

nMOS Logic (NAND)



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0	**1**	**1**
1	0	1
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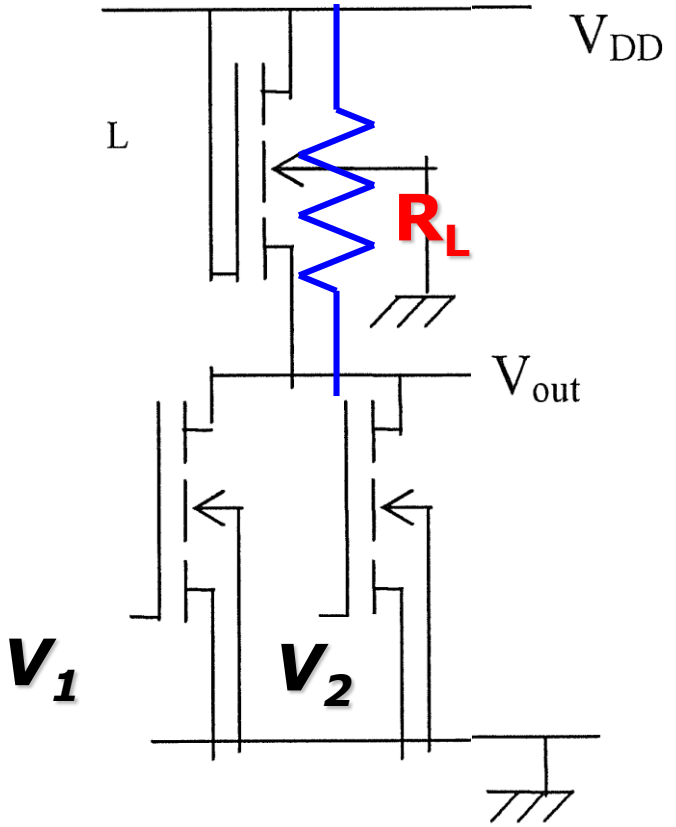
$$V_{out} \approx V_{DD}$$

nMOS Logic (NOR)

V_1	V_2	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0



nMOS Logic (NOR)

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V_1	V_2	V_{out}
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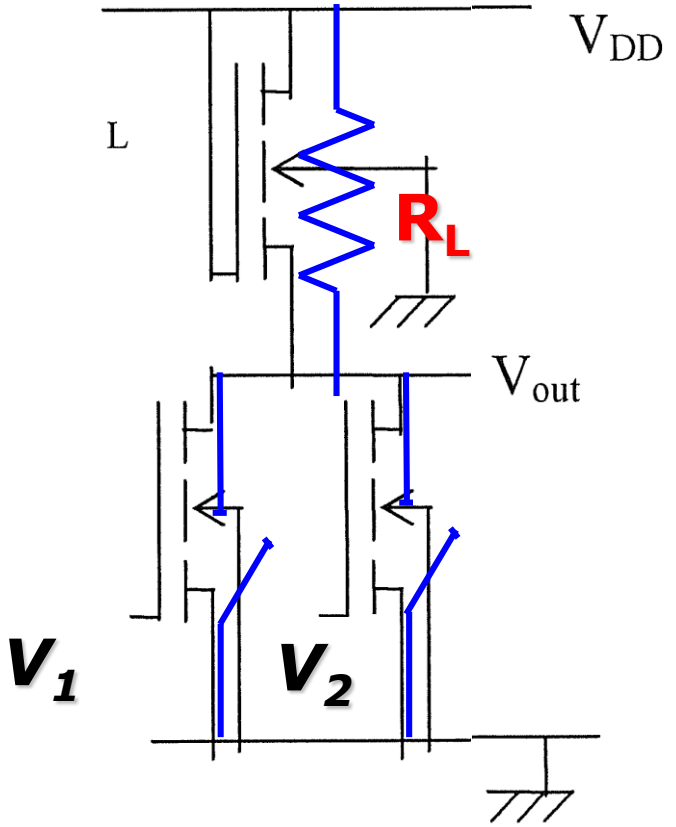
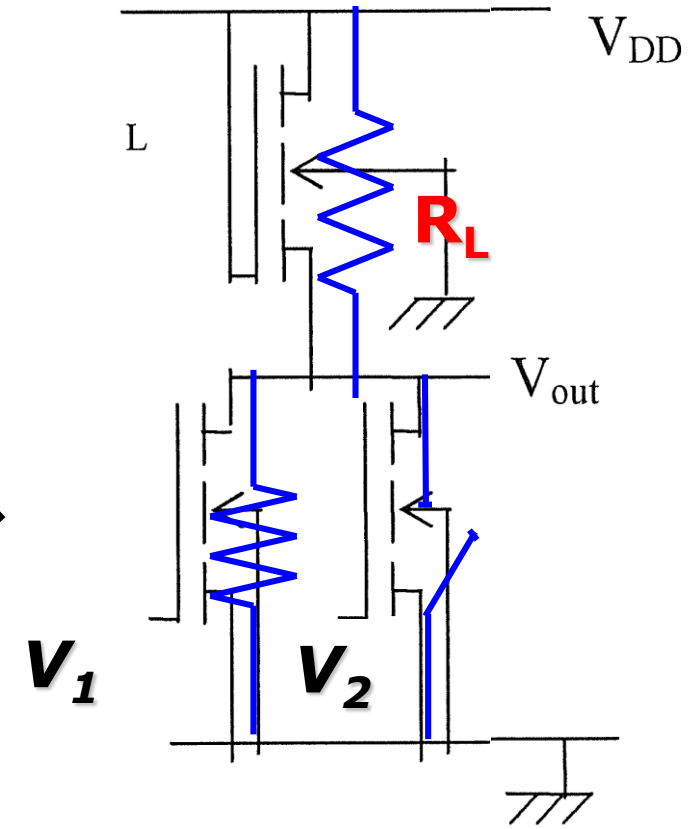
0	1	0
1	0	0
1	1	0



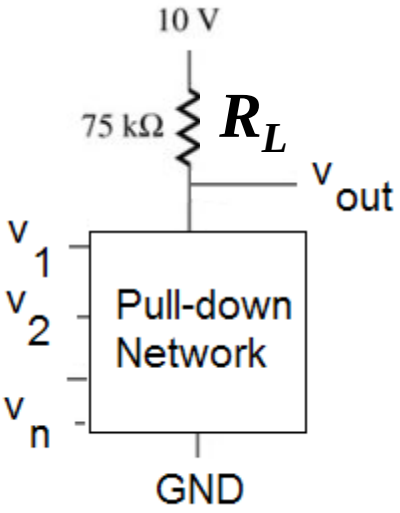
nMOS Logic (NOR)

$$V_{out} = \frac{R_1}{R_L + R_1} V_{DD} \approx 0 \ \ (\text{Large } R_L)$$

V_1	V_2	V_{out}
0	0	1
0	1	0
1	**0**	**0**
1	1	0



nMOS Logic (General)

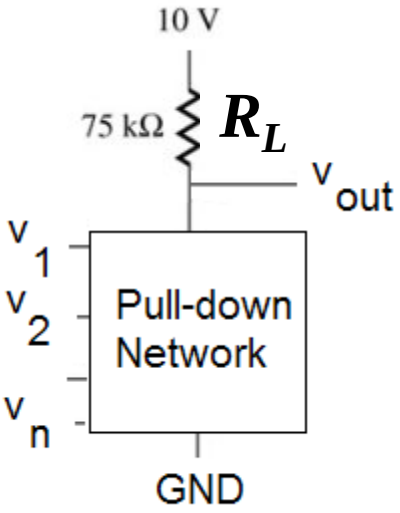


Any combination of inputs V_1 V_2 … V_n that should result in an output of 0 should produce a low-resistance path from V_{out} to ground in the pull-down network.

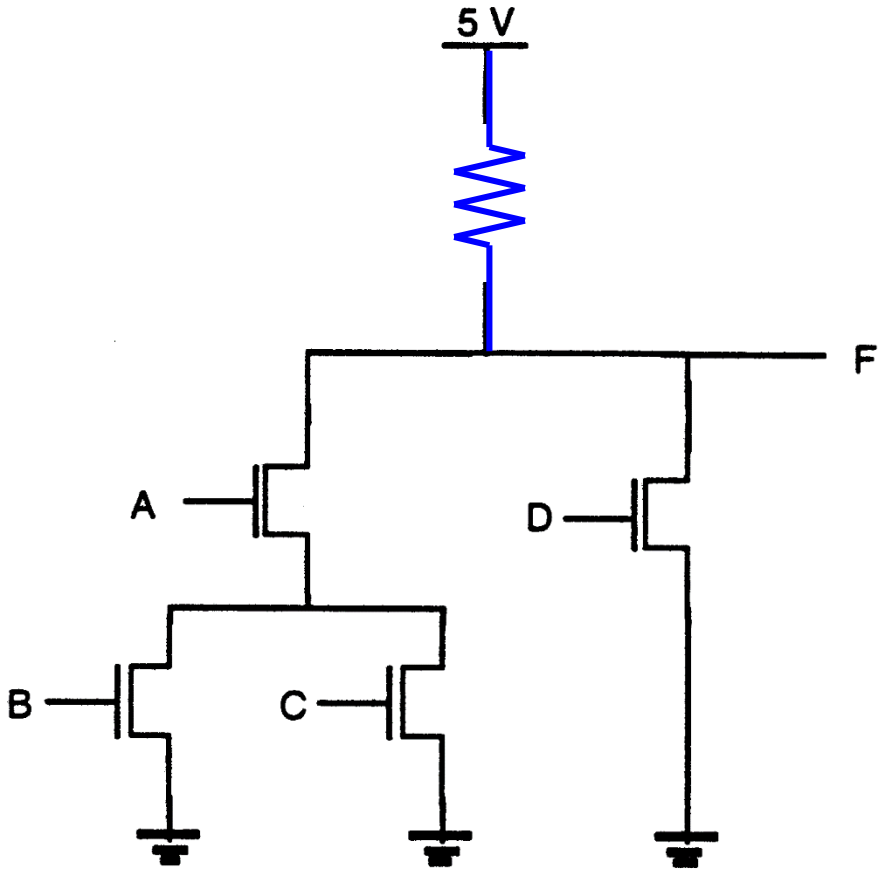
Any combination of inputs that does not pull the output V_{out} to ground through the network will result in the output pulled high through the pull-up resistor R_D.

NMOS logic draws current continuously when V_{out} is low.

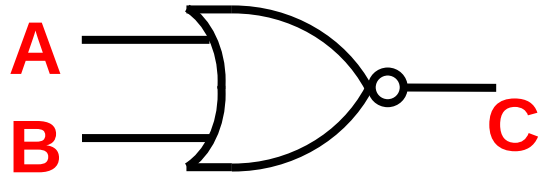
nMOS Logic (General)



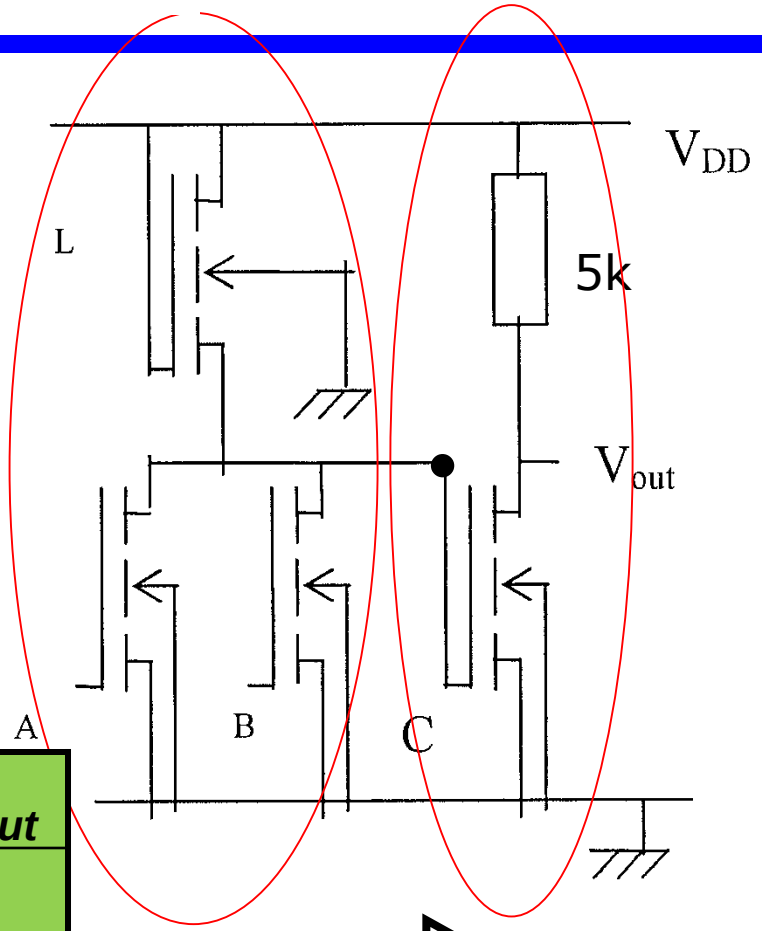
Example:



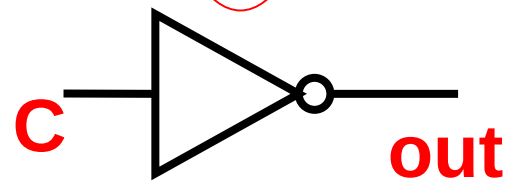
Example: Design Exercise 2016



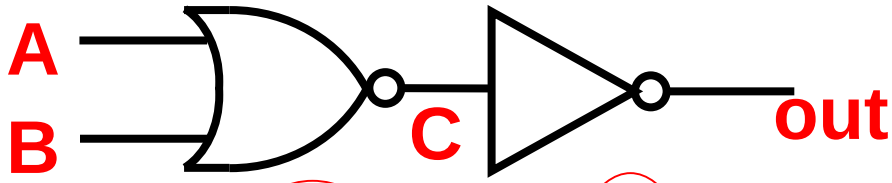
- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega$



V_A	V_B	V_C	V_C	V_{out}
0	0	1	1	0
0	1	0	0	1
1	0	0	0	1
1	1	0	0	1



Example 2016



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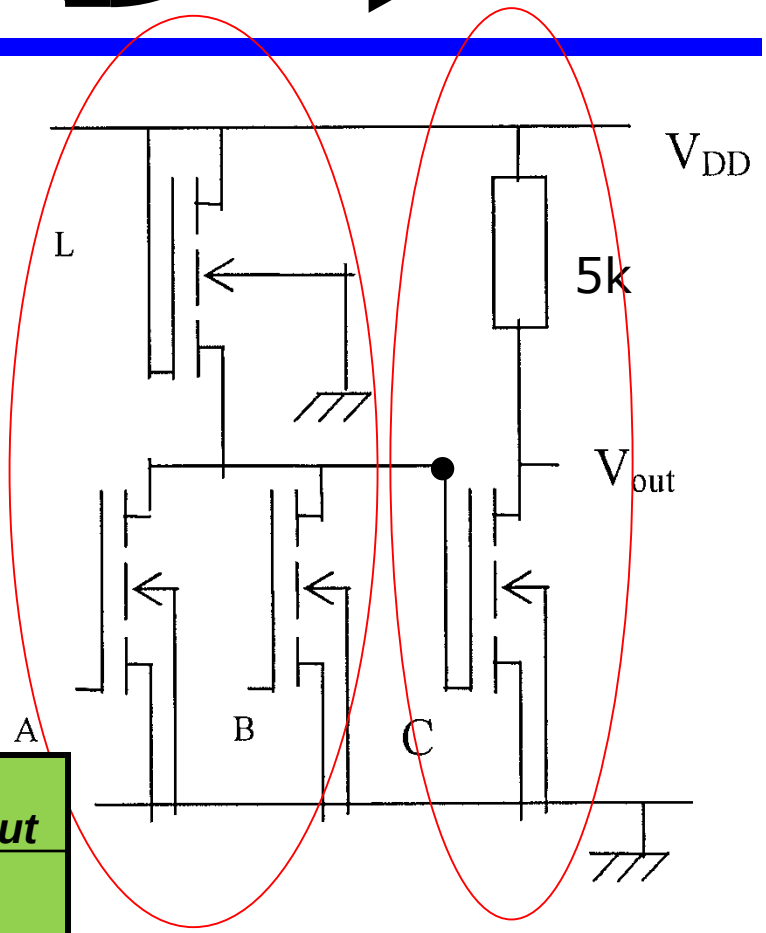
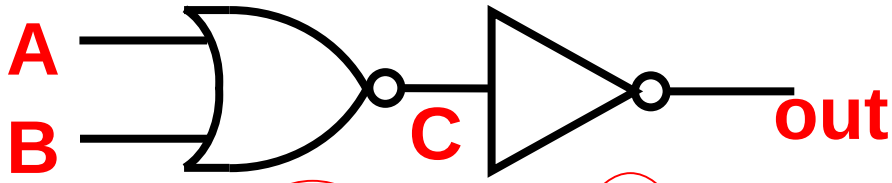


V_A	V_B	V_C	V_C	V_{out}
0	0	1	1	0
0	1	0	0	1
1	0	0	0	1
1	1	0	0	1

Example 2016



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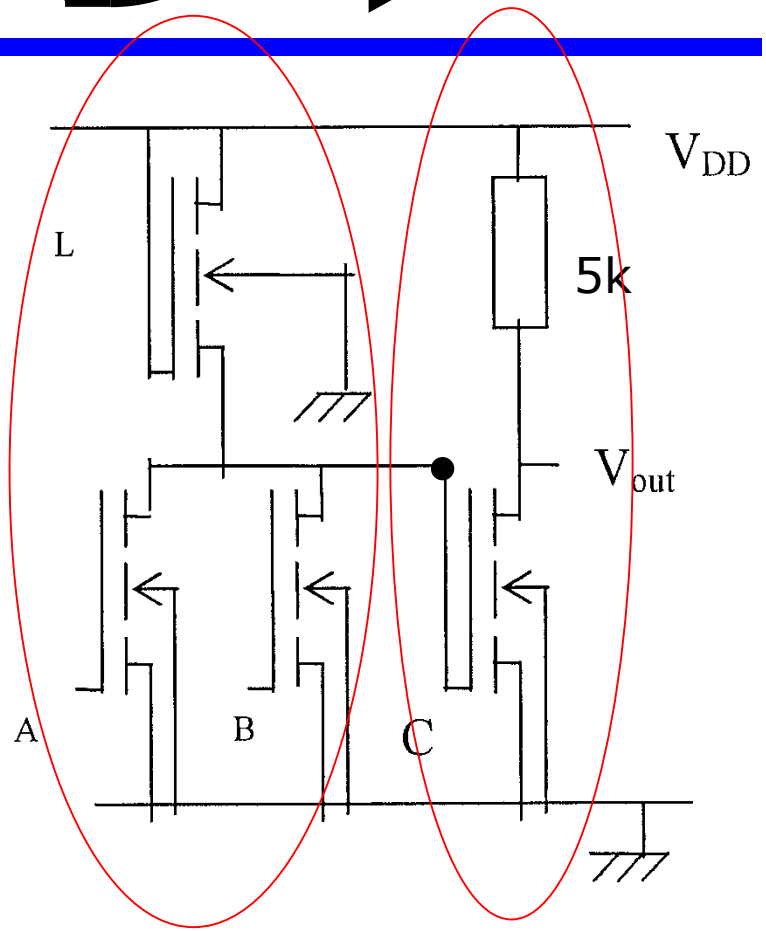
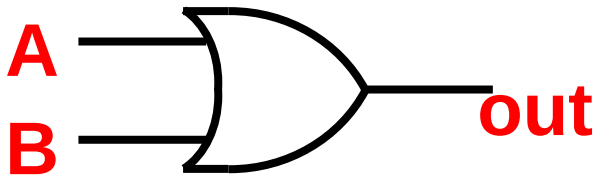
V_A	V_B	V_C	V_{out}
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1





OUTLINE

- **nMOS logic (examples)**
  - Truth table
  - **Calculation**
  - Layout
- Design Exercise 2017 (15% marks)

nMOS Logic (Inverter): example1

Calculate W/L with the following specification:
1) R_L=5k. 2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) V_T =0.3V. 4) V_{DD}=5V.

Solution: The output of the driver when it is switched on must be significantly less than V_T say 0.1V, that is, let V_{Out} = 0.1V:

$I_D = \beta[(V_G-V_T)V_D-V_D^2/2] \approx \beta[(V_G-V_T)V_D]$

or $I_D = \beta[(V_{DD}-V_T)V_{Out}]$.

The effective resistance of the driver (R_D) between source and drain is, therefore:

$R_D = V_{Out}/I_D = (\beta[(V_{DD}-V_T)])^{-1}$

it is obtained as a potential divider

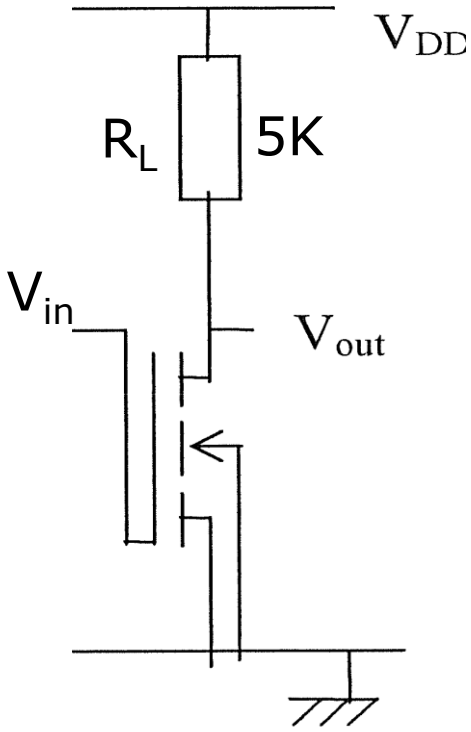
$[R_D/(R_D+R_L)]=V_{Out}/V_{DD}=0.1/5=0.02$ so $R_D<<R_L$

and $R_L/R_D = 1/0.02=50 \rightarrow$ **$R_D=100\Omega$**

$R_D=1/[\beta(V_G-V_T)]=1/[\beta(5-0.3)]=100\Omega$

$\rightarrow \beta \approx 20*10^{-4}$

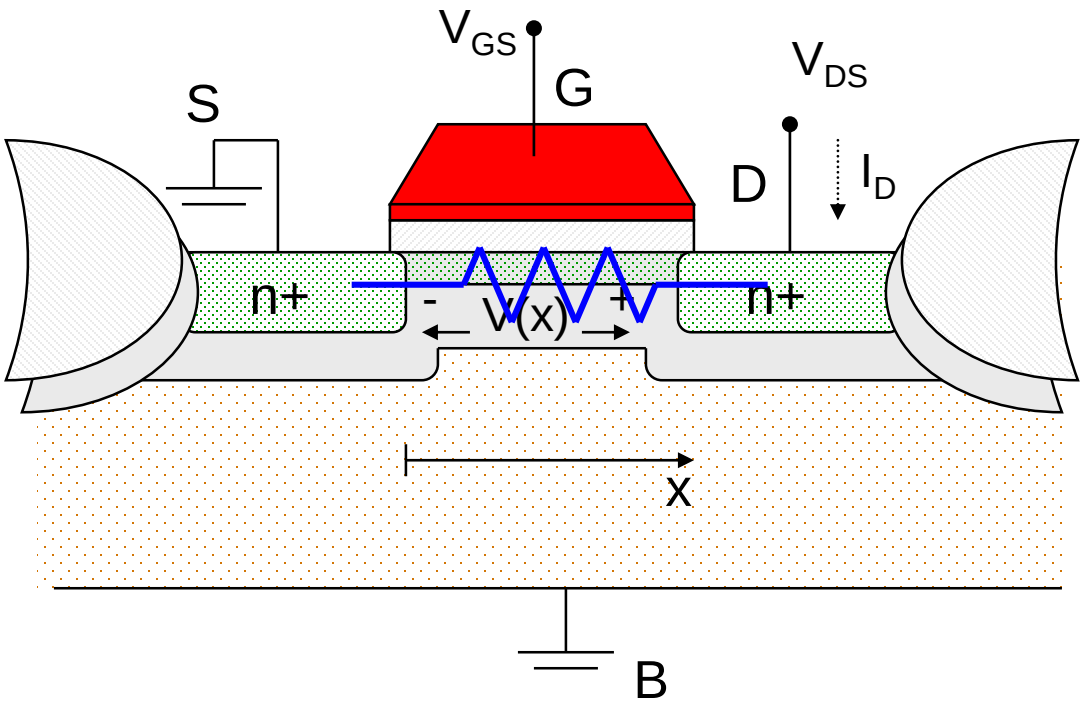
Therefore, the aspect ratio, W/L, is 12.

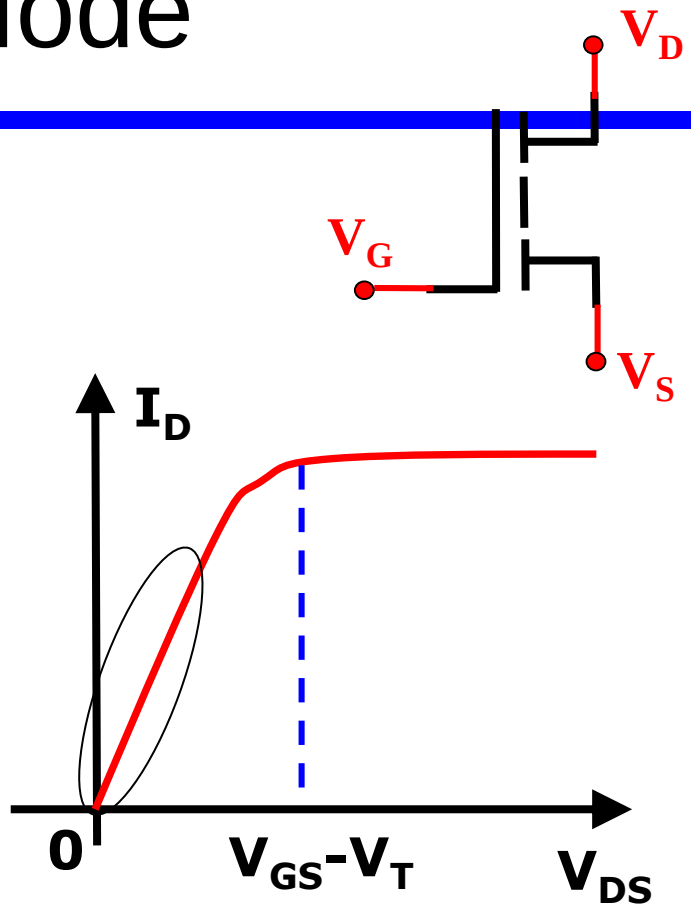


Transistor in Linear Mode

PL

Assuming $V_{GS} > V_T$





When $V_{DS} \leq V_{GS} - V_T$: $I_D = \beta_0 W/L [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$

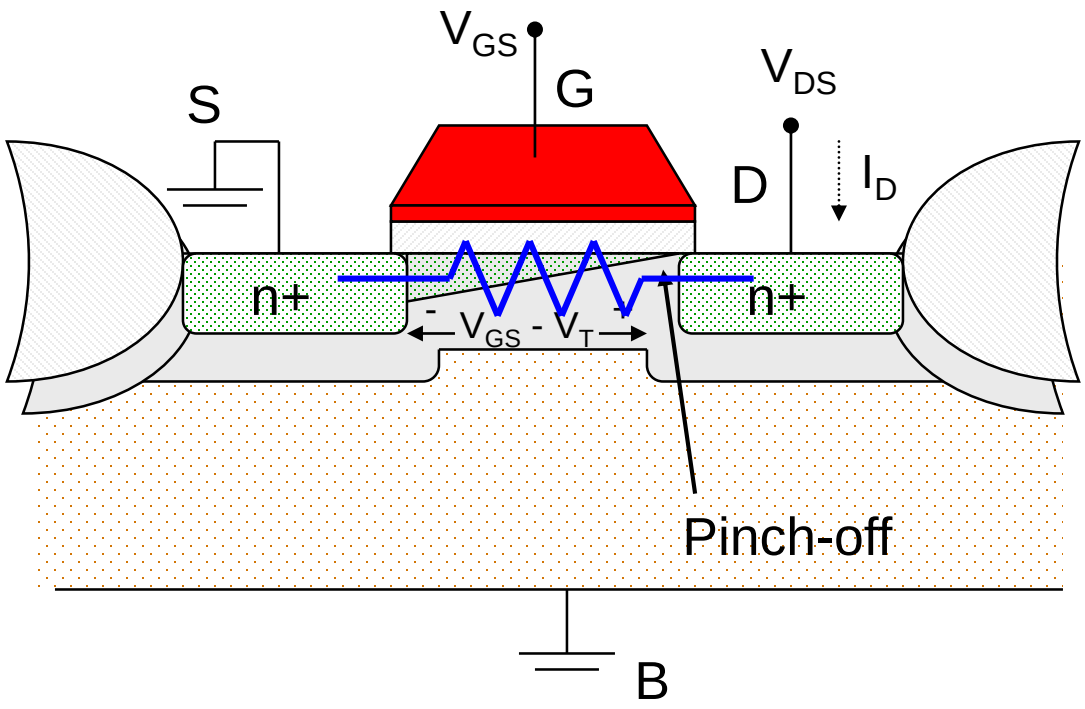
$\beta_0 = \mu_n C_{ox}$

$R = V_{DS} / I_D$

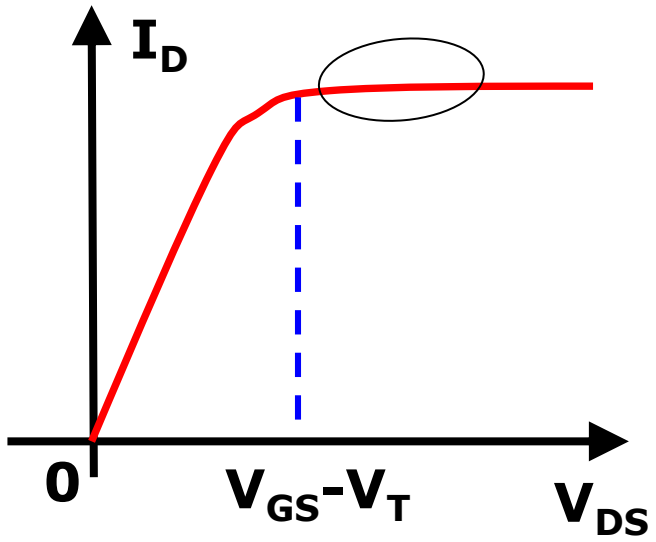
Transistor in Saturation Mode

PL

Assuming $V_{GS} > V_T$



$V_{DS} > V_{GS} - V_T$



When $V_{DS} \geq V_{GS} - V_T$: $I_D = (\beta_0/2)\, W/L\, [(V_{GS} - V_T)^2]$

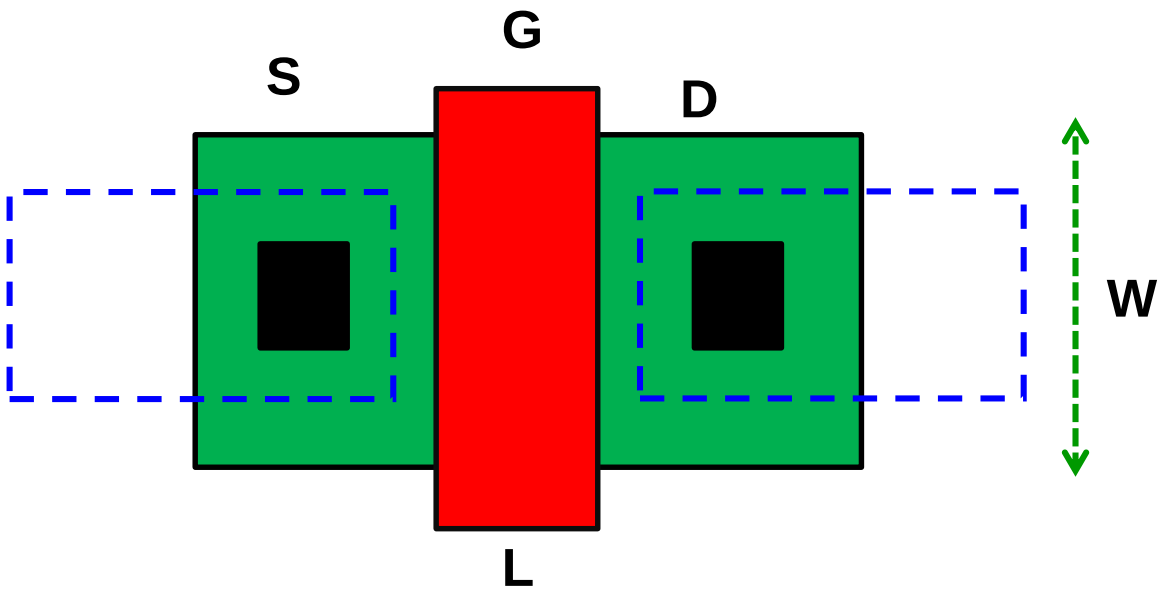
$R = V_{DS} / I_D$

nMOS Logic (Inverter): example1

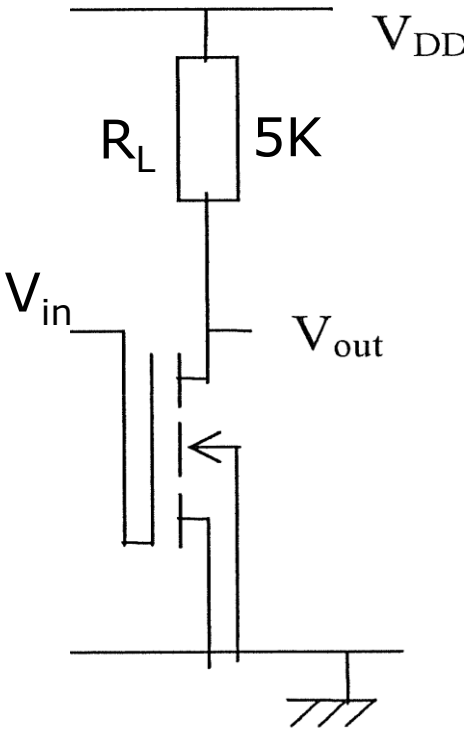
Calculate W/L with the following specification:
1) R_L=5k. 2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) V_T =0.3V. 4) V_{DD}=5V.

$\beta_0 = \mu C_{ox}$

The aspect ratio, W/L, is ??



Layout(版图)



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Solution:

If $V_{in} = V_{DD}$, **let V_{Out} = 0.1V << V_T**

Potential divider:

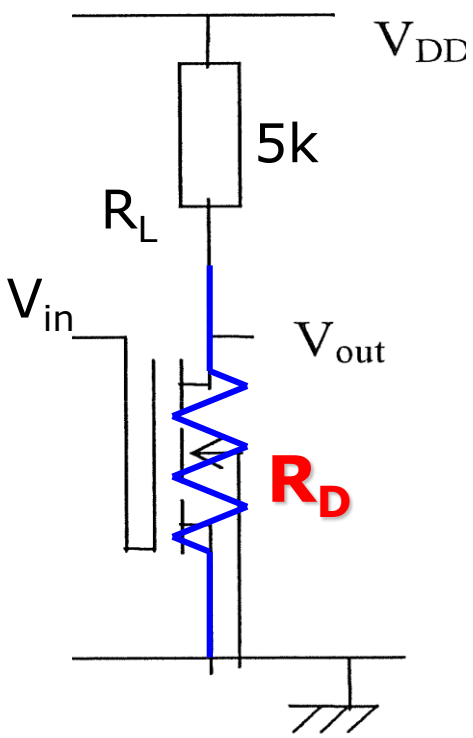
$R_D/(R_D+R_L)=V_{Out}/V_{DD}=0.1/5=0.02$

→ **$R_D \approx 100\Omega$**

$I_D = \beta[(V_G-V_T)V_D-V_D^2/2] \approx \beta[(V_G-V_T)V_D]$

$R_D = V_{Out}/I_D = \{\beta[(V_{DD}-V_T)]\}^{-1} = 1/[\beta(5-0.3)]=100\Omega$

→ **$\beta \approx 20*10^{-4}$. Therefore, the aspect ratio, W/L, is 12.**



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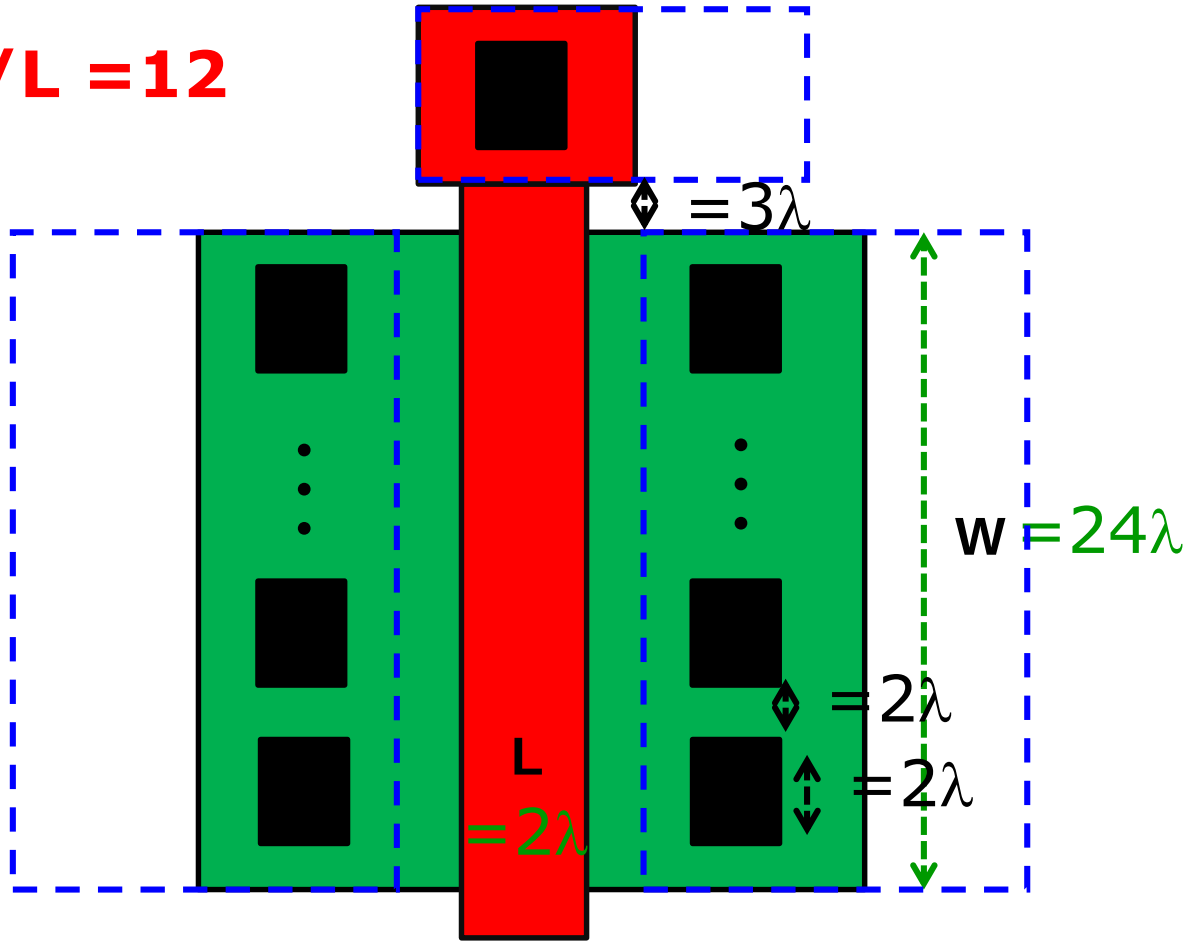
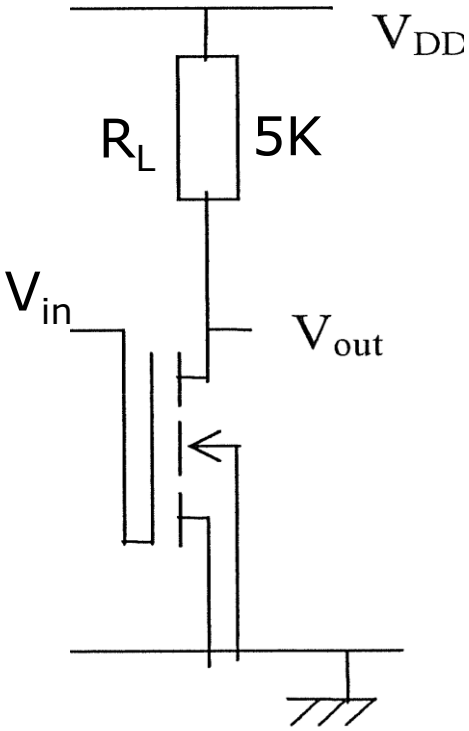
W/L =12





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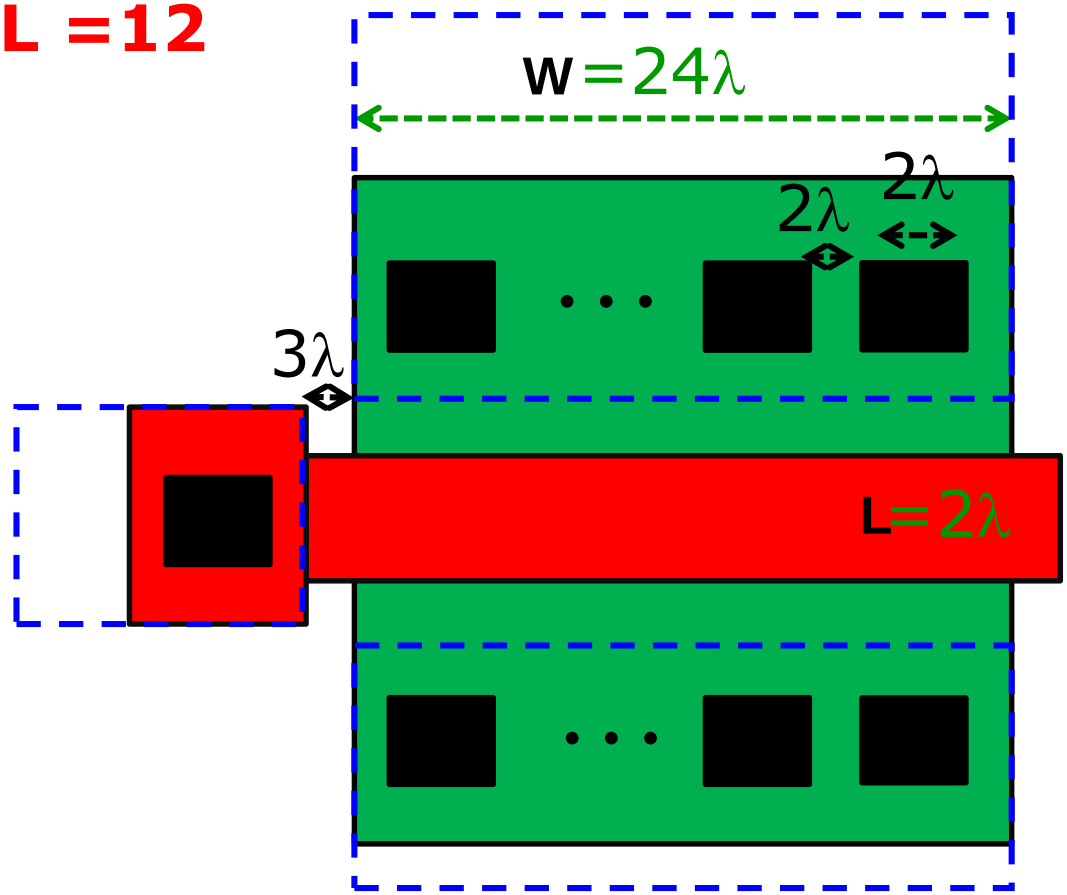
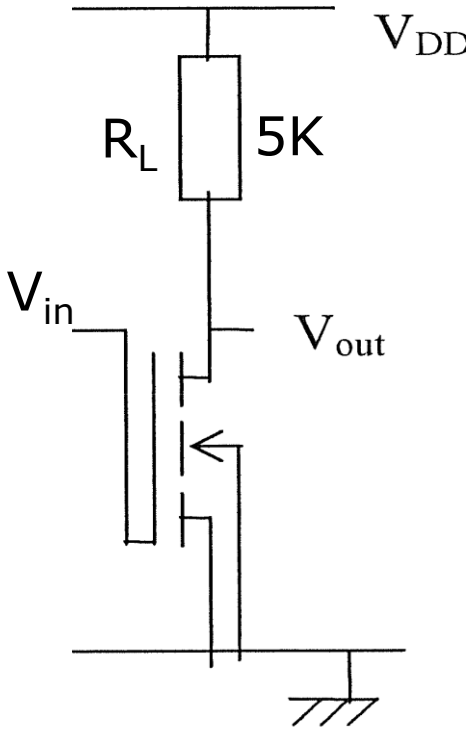
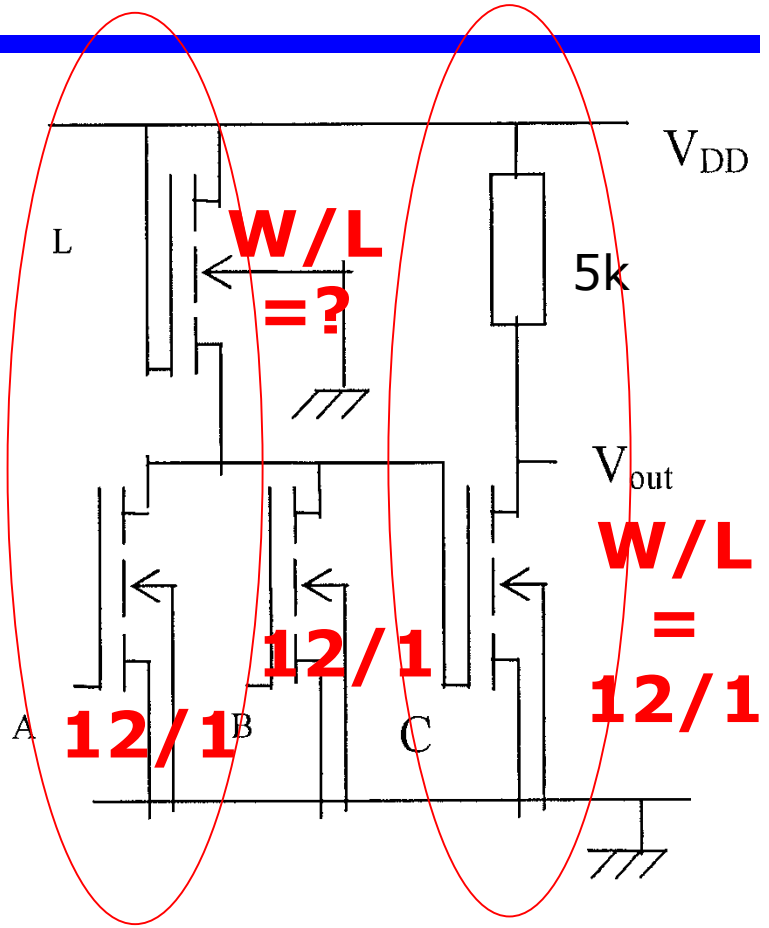




Example: Design Exercise 2016

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$
- HINTS: Liverpool notes.



nMOS Logic (Inverter): example2

Calculate W/L of Load with the following specification:

1) The aspect ratios of D is 12.

2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.

3) $V_T = 0.3V$. 4) $V_{DD}=5V$.

Solution: The output of the driver when it i switched on is $V_{Out} = 0.1V$:

$I_D = \beta[(V_{DD}-V_T)V_{Out}]$.

The effective resistance of the driver is,

$R_D = V_{Out}/I_D = (\beta_D[(V_{DD}-V_T)])^{-1} = 100\ \Omega$

R_L is obtained as a potential divider

$[R_D/(R_D+R_L)]=V_{Out}/V_{DD}=0.1/5=0.02$ so

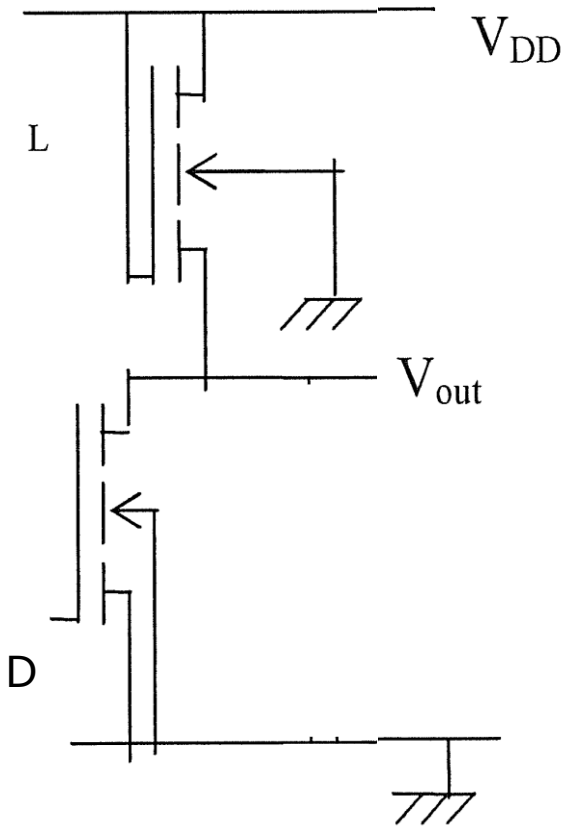
$R_D << R_L$ and $R_L/R_D = 1/0.02=50$

$\rightarrow$ **R_L=5kΩ** and the load current

- $I_D = \beta_L/2\ (V_{DD}-V_T)^2$

$R_L = (V_{DD}-V_{out})/I_D = 5*2/[\beta_L(5-0.3)^2] = 5k\Omega$

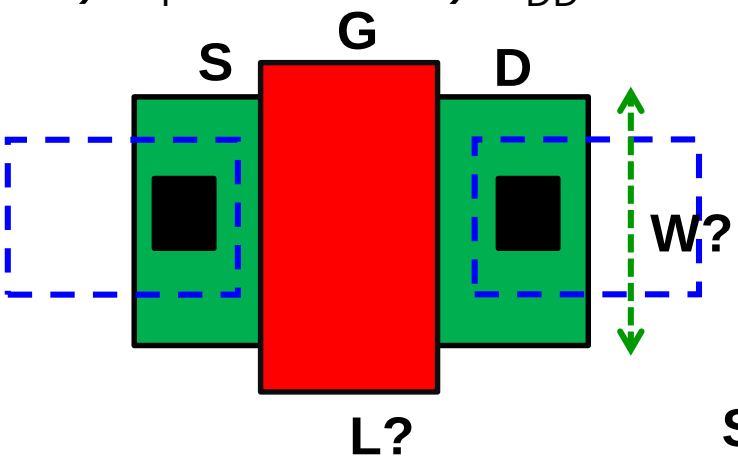
$\rightarrow \beta_L = 1*10^{-4} \rightarrow$ aspect ratio of Load=**0.5**

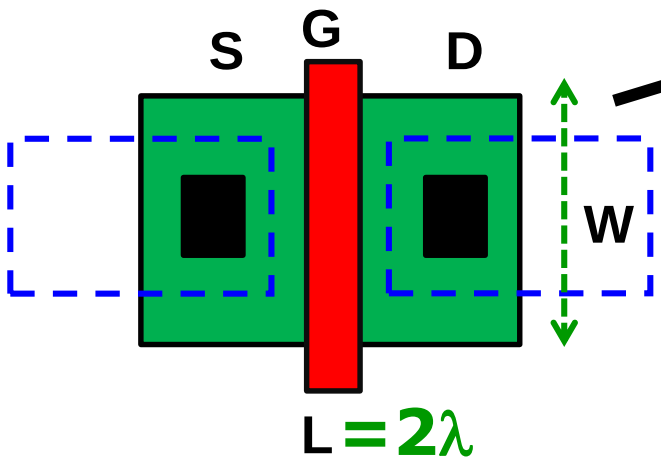


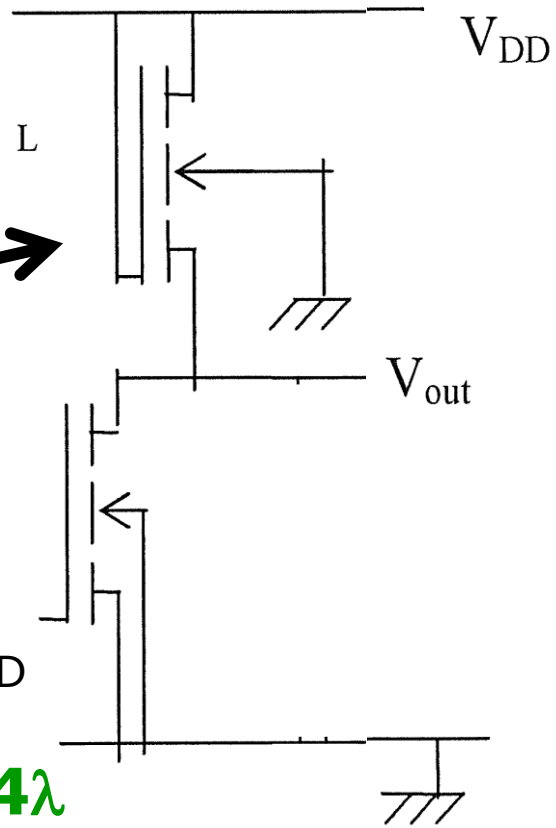
nMOS Logic (Inverter): example2

Calculate W/L of Load with the following specification:

1) **The aspect ratios of D is 12.**
2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) $V_T = 0.3V$. 4) $V_{DD}=5V$.







nMOS Logic (Inverter): example2

Calculate W/L of Load with the following specification:

1) **The aspect ratios of D is 12.**
2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) $V_T = 0.3V$. 4) $V_{DD}=5V$.

Solution:

If $V_{in} = V_{DD}$, let $V_{Out} = 0.1V$:

$$I_D = \beta_D[(V_{in}-V_T)V_{Out}-V_{Out}^2/2]$$

$$\mathbf{R_D = V_{Out}/I_D = (12\beta_0[(V_{DD}-V_T)])^{-1} = 100\ \Omega}$$

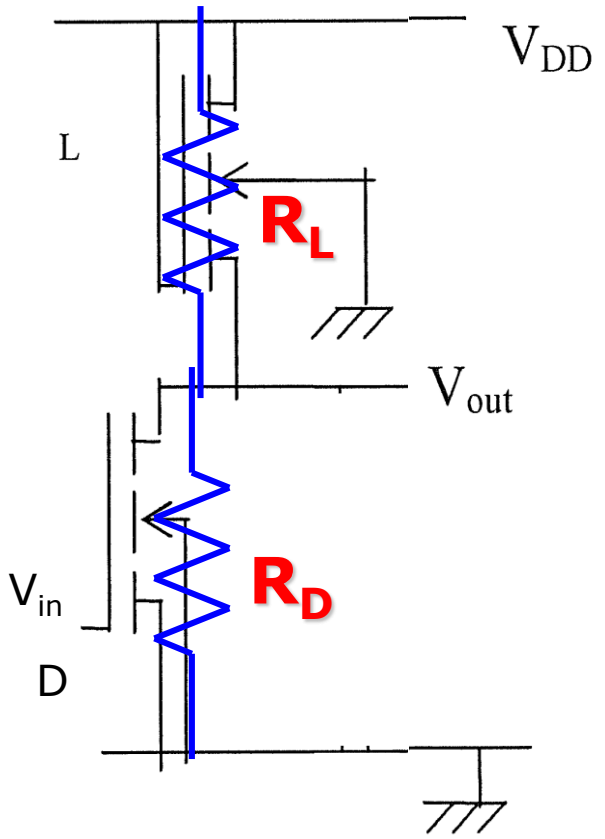
$$[R_D/(R_D+R_L)]=V_{Out}/V_{DD}=0.1/5=0.02$$

$$\rightarrow \mathbf{R_L \approx 5k\Omega}$$

$$\mathbf{I_D = \beta_L(V_{DD}-V_T)^2/2}$$

$$R_L = (V_{DD}-V_{out})/I_D = 4.9*2/[\beta_L(5-0.3)^2] = 5k\Omega$$

$$\rightarrow \beta_L = 8.9*10^{-5} \rightarrow \text{aspect ratio of load} = \underline{\mathbf{0.5}}$$



nMOS Logic (Inverter): example2

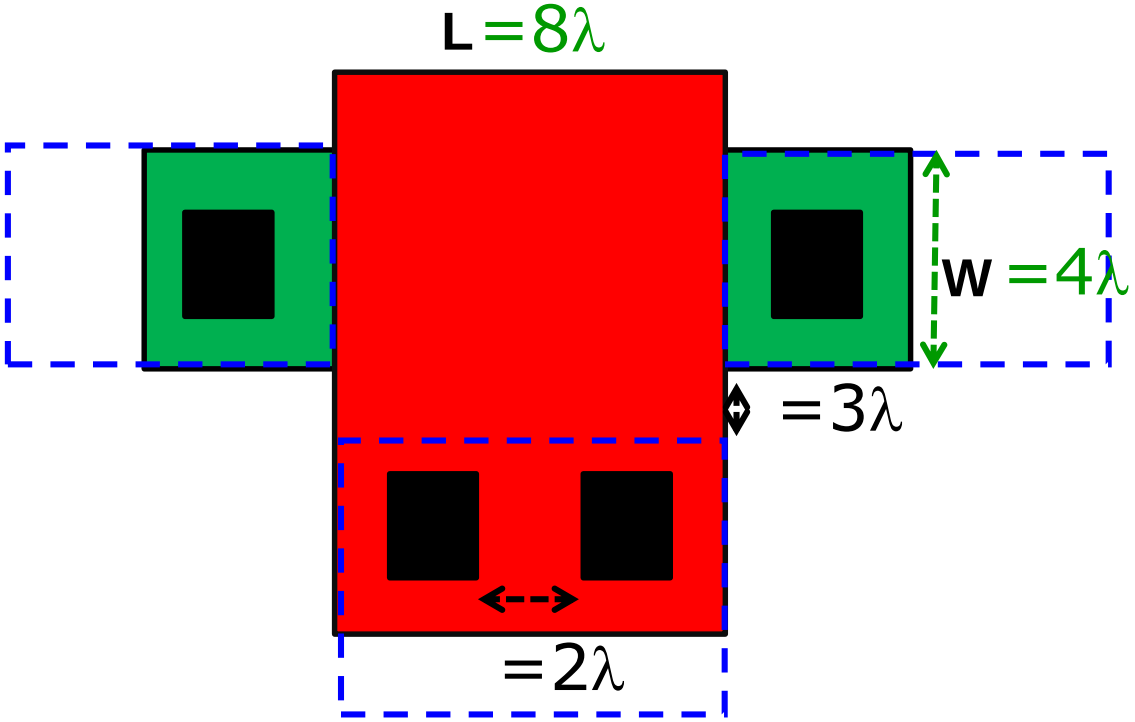
Calculate W/L of Load with the following specification:

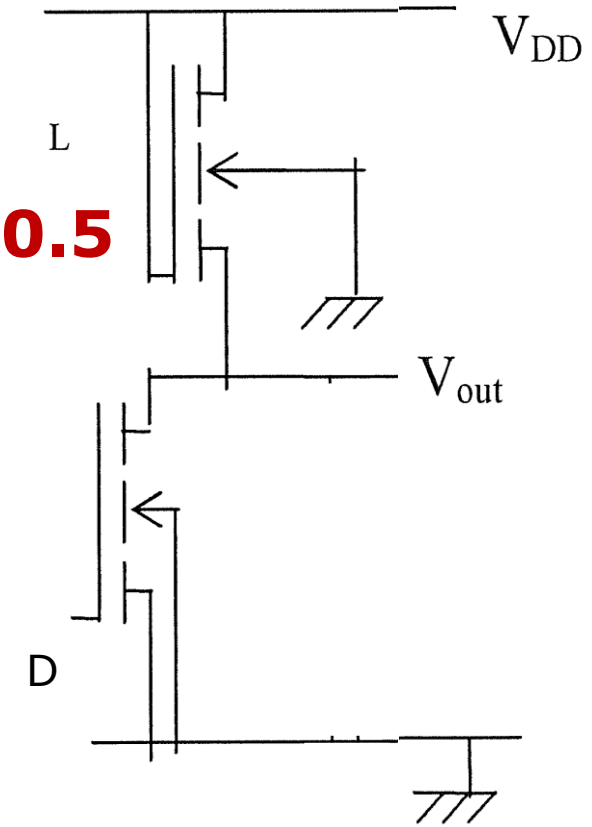
1) The aspect ratios of D is 12.

2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.

3) $V_T = 0.3V$. 4) $V_{DD}=5V$.

W/L of Load= 0.5

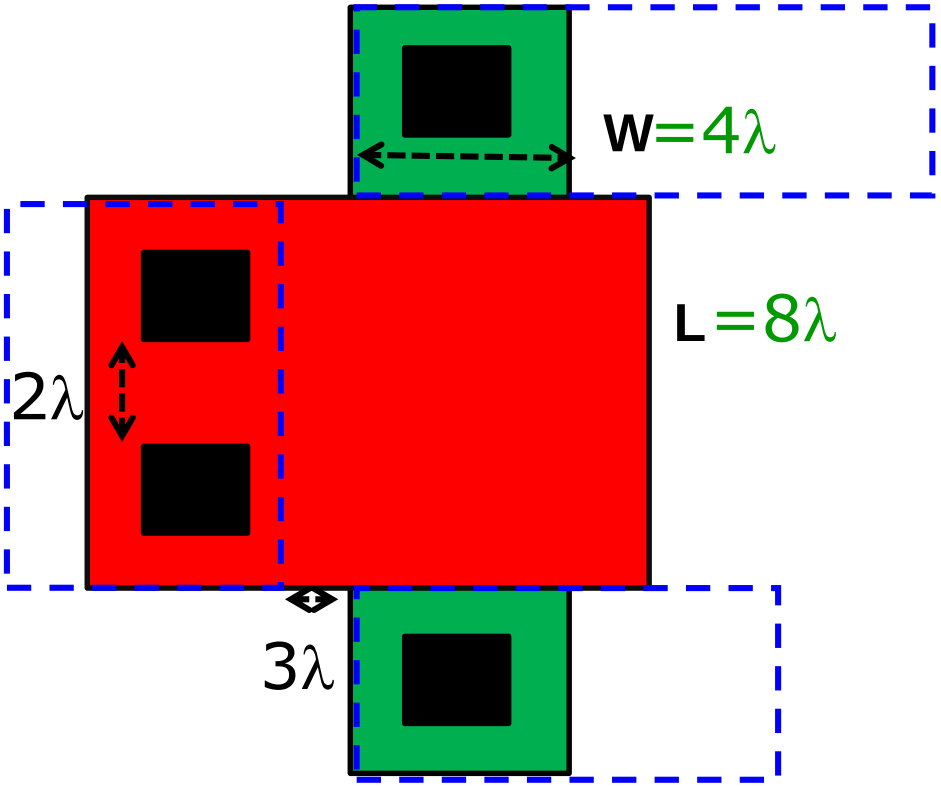




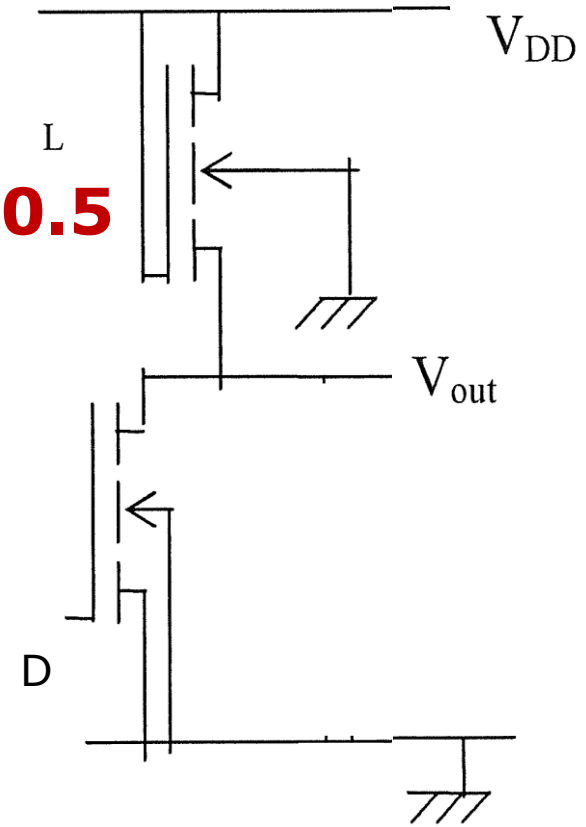
nMOS Logic (Inverter): example2

Calculate W/L of Load with the following specification:

1) **The aspect ratios of D is 12.**
2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) $V_T = 0.3V$. 4) $V_{DD}=5V$.



W/L = 0.5



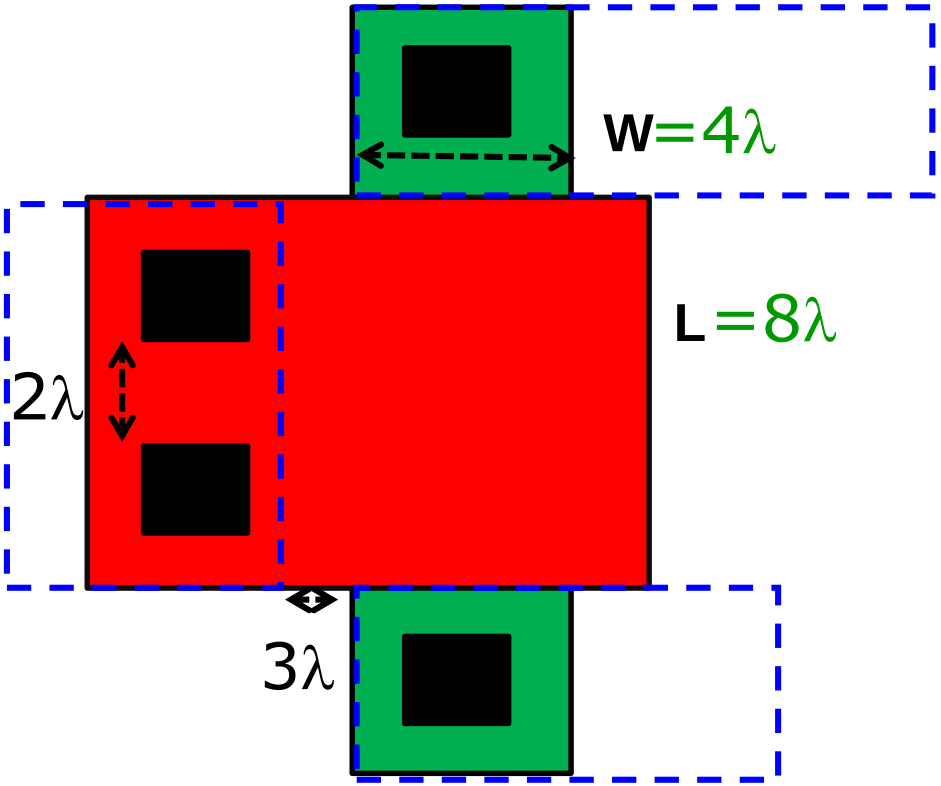
nMOS Logic (Inverter): example2

Calculate W/L of Load with the following specification:

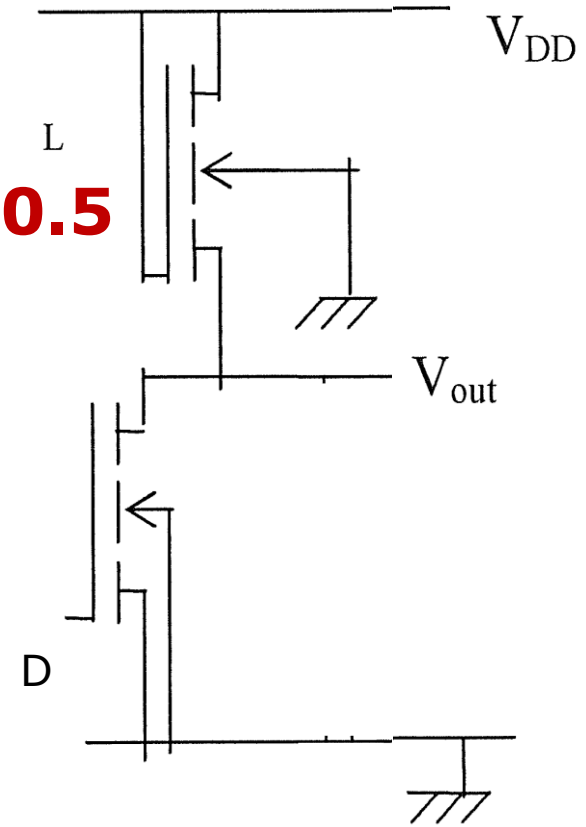
1) The aspect ratios of D is 12.

2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.

3) $V_T = 0.3V$. 4) $V_{DD}=5V$.



W/L = 0.5



nMOS Logic (NOR): example3

Calculate W/L of Load with the following specification:

1) The aspect ratios of D is 12.

2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.

3) $V_T = 0.3V$. 4) $V_{DD}=5V$.

Solution:

let $V_{Out} = 0.1V$:

$$I_D = \beta_D[(V_{inA}-V_T)V_{Out}-V_{Out}^2/2]$$

$$\mathbf{R_D = V_{Out}/I_D = (\beta_D[(V_{DD}-V_T)])^{-1} = 100\ \Omega}$$

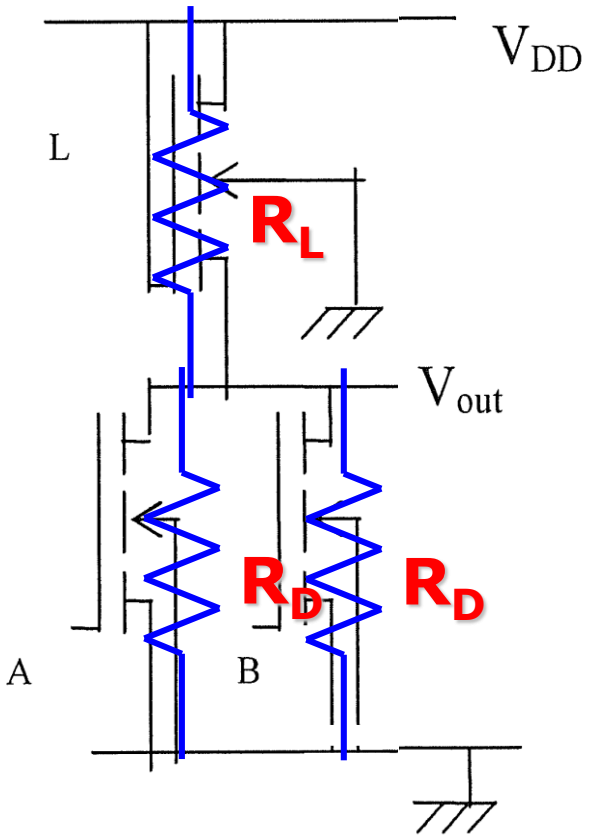
$$[\mathbf{0.5}R_D/(\mathbf{0.5}R_D+R_L)]=V_{Out}/V_{DD}=0.1/5=0.02$$

$$\rightarrow \mathbf{R_L = 2.5k\Omega}$$

$$\mathbf{I_D = \beta_L(V_{DD}-V_T)^2/2}$$

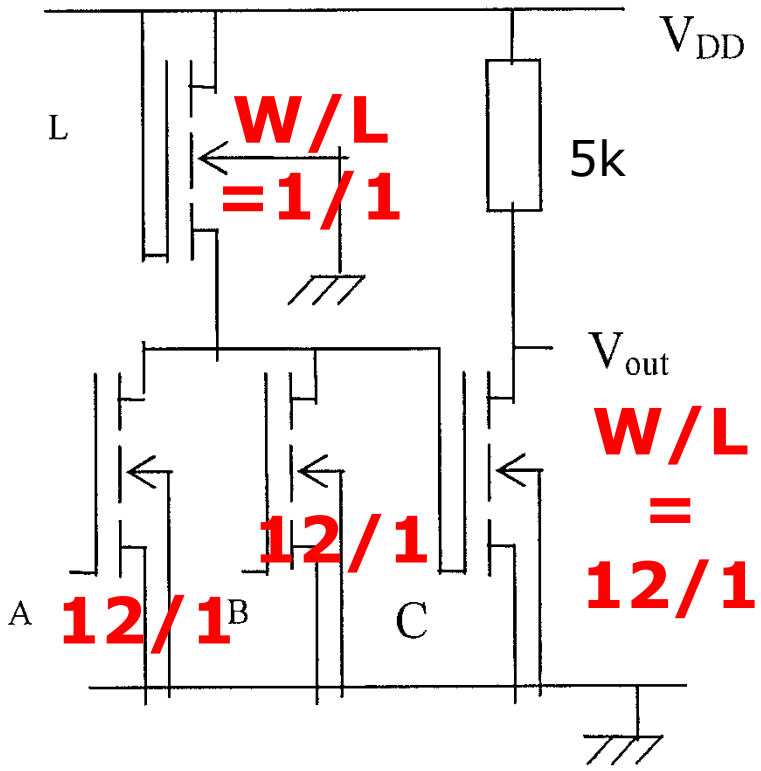
$$R_L = (V_{DD}-V_{out})/I_D = 4.9*2/[\beta_L(5-0.3)^2] = 2.5k\Omega$$

$$\rightarrow \beta_L = 1.8*10^{-4} \rightarrow \text{aspect ratio of Load} = 1.$$



Example: Design Exercise 2016

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$
- HINTS: Liverpool notes.



Design Exercise 2017

Layout design of the nMOS IC shown in Fig.1

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$

$$\mu C_{ox} = \beta_0$$

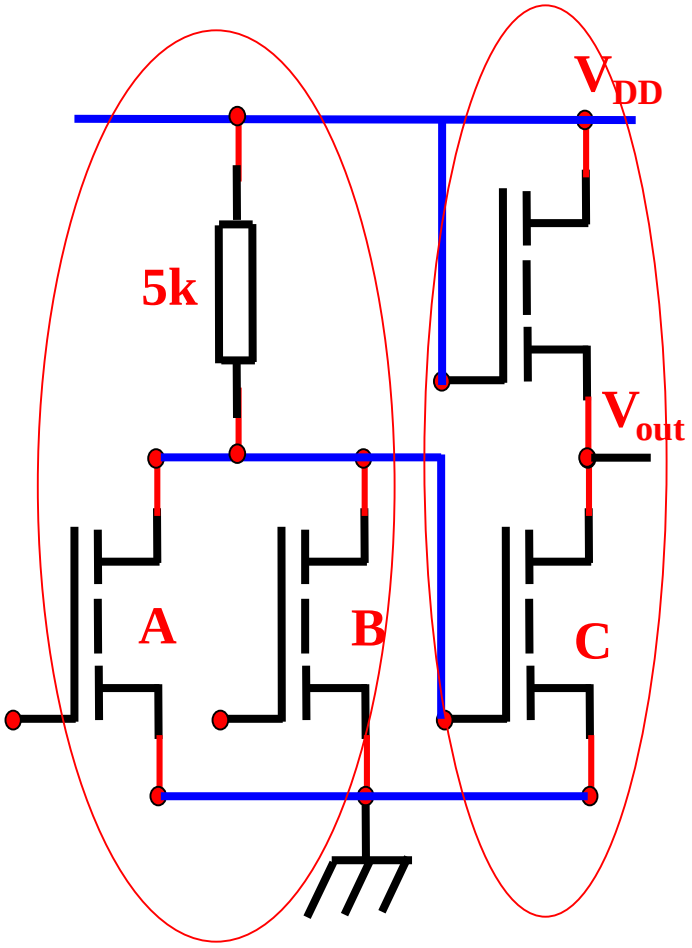


Fig.1

nMOS Logic (NOR): example4

Calculate W/L with the following specification:
1) R_L=5k. 2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) V_T =0.3V. 4) V_{DD}=5V.

Solution:

If $V_A=V_B=V_{DD}$, **let V_{Out} = 0.1V << V_T**

Potential divider:

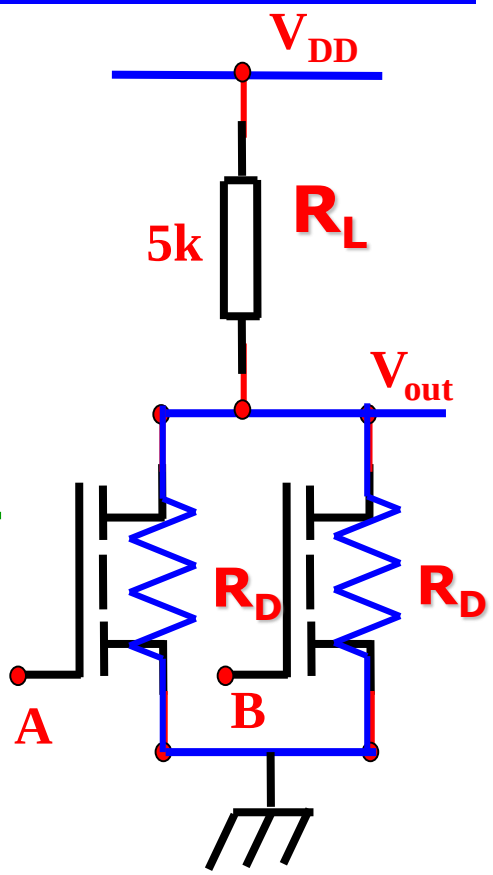
$0.5R_D/(0.5R_D+R_L)=V_{Out}/V_{DD}=0.1/5=0.02$

→ **$R_D \approx 200\Omega$**

$I_D= \beta[(V_G-V_T)V_D-V_D^2/2] \approx \beta[(V_G-V_T)V_D]$

$R_D=V_{Out}/I_D=\{\beta[(V_{DD}-V_T)]\}^{-1} =1/[\beta(5-0.3)]=200\Omega$

→ **$\beta \approx 10*10^{-4}$. Therefore, the aspect ratio, W/L, is 6.**



Design Exercise 2017

Layout design of the nMOS IC shown in Fig.1

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$

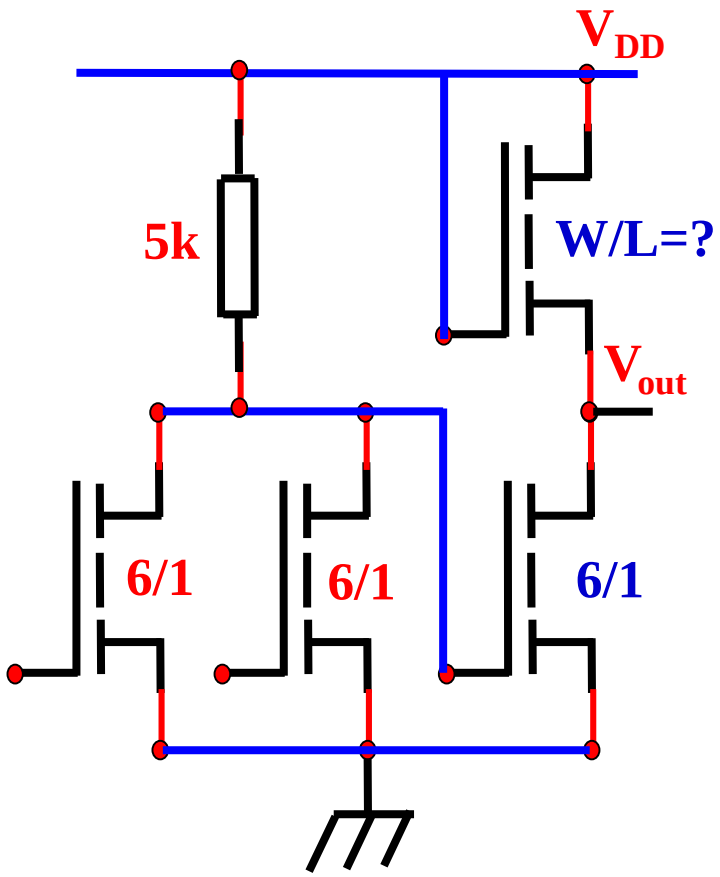


Fig.1

nMOS Logic (Inverter): example5

Calculate W/L of Load with the following specification:

1) The aspect ratios of D is **6**.
2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) $V_T = 0.3V$. 4) $V_{DD}=5V$.

Solution:

If $V_{in} = V_{DD}$, let $V_{Out} = 0.1V$:

$$I_D = \beta_D[(V_{in}-V_T)V_{Out}-V_{Out}^2/2]$$

$$\mathbf{R_D = V_{Out}/I_D = (6\beta_0[(V_{DD}-V_T)])^{-1} = 200\ \Omega}$$

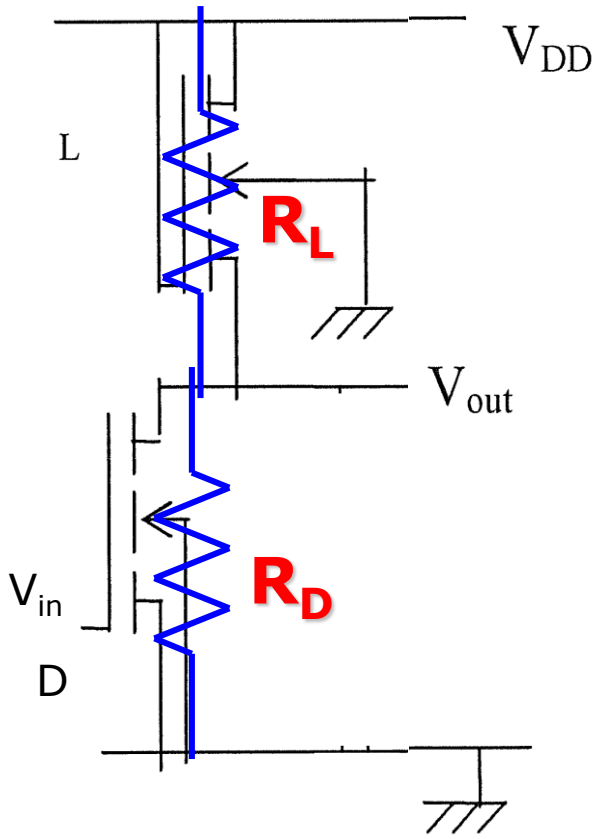
$$[R_D/(R_D+R_L)]=V_{Out}/V_{DD}=0.1/5=0.02$$

$$\rightarrow \mathbf{R_L \approx 10k\Omega}$$

$$\mathbf{I_D = \beta_L(V_{DD}-V_T)^2/2}$$

$$R_L = (V_{DD}-V_{out})/I_D = 4.9*2/[\beta_L(5-0.3)^2] = 10k\Omega$$

$$\rightarrow \beta_L = 4.4*10^{-5} \rightarrow \text{aspect ratio of load} = \underline{\mathbf{0.25}}$$



Design Exercise 2017

Layout design of the nMOS IC shown in Fig.1

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$

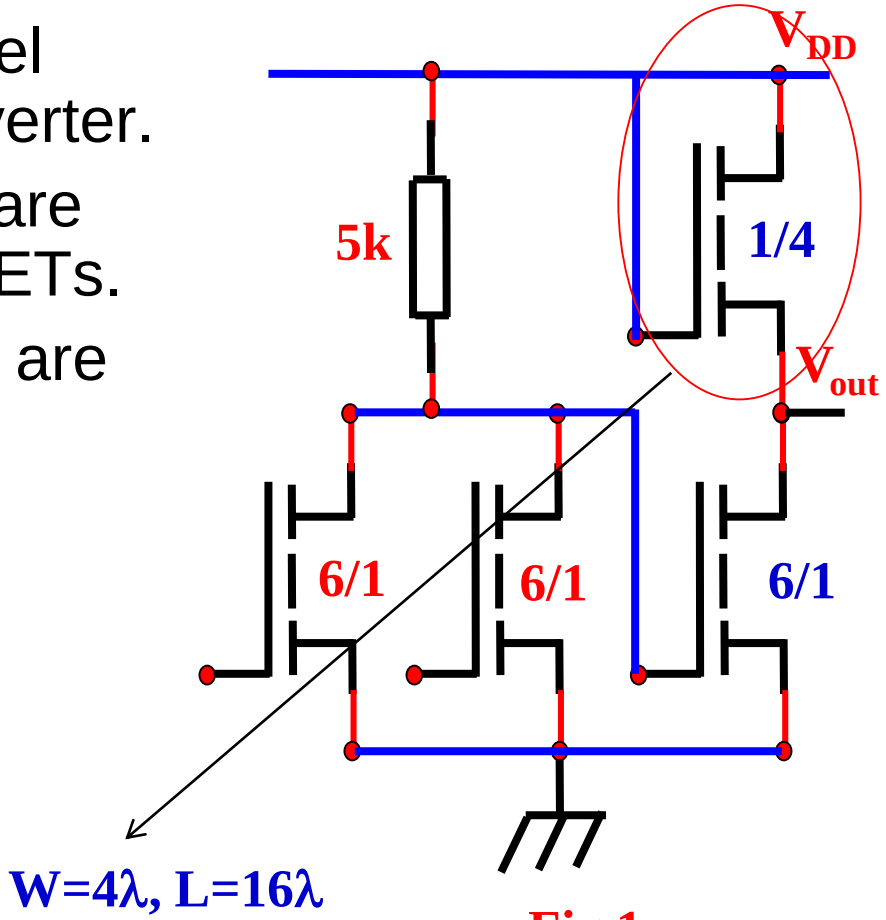


Fig.1

Design Exercise 2017

Layout design of the nMOS IC shown in Fig.1

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$

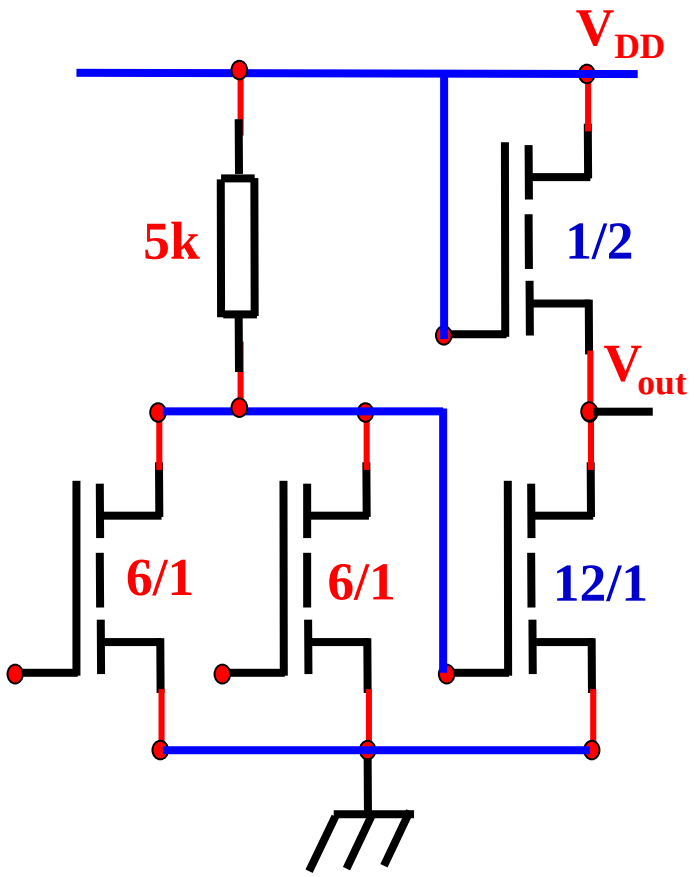
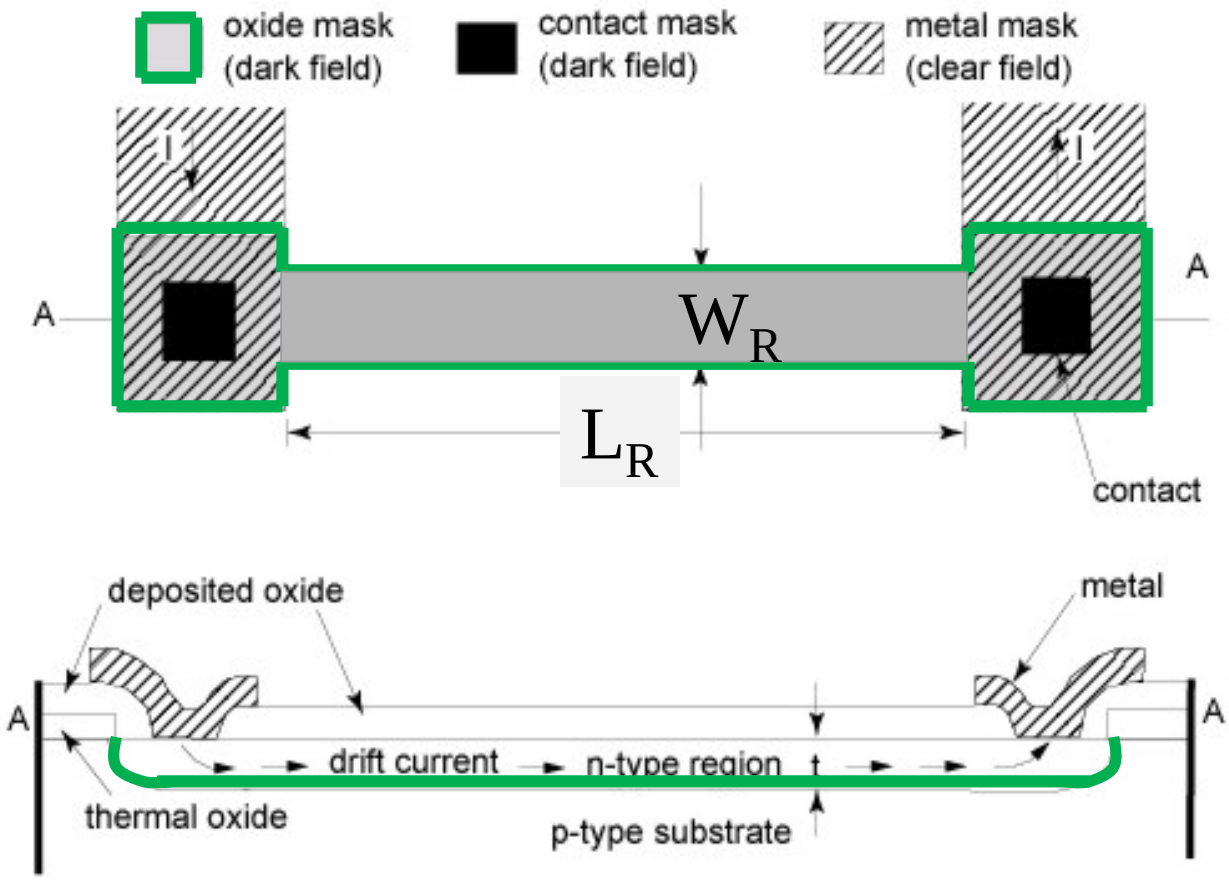


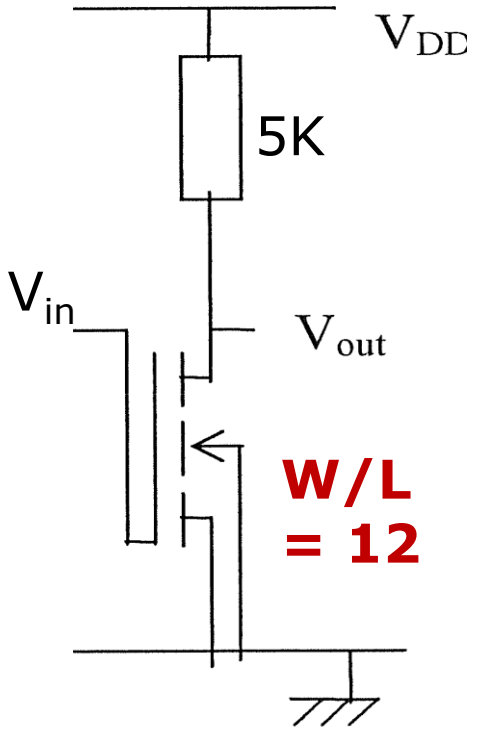
Fig.1

OUTLINE

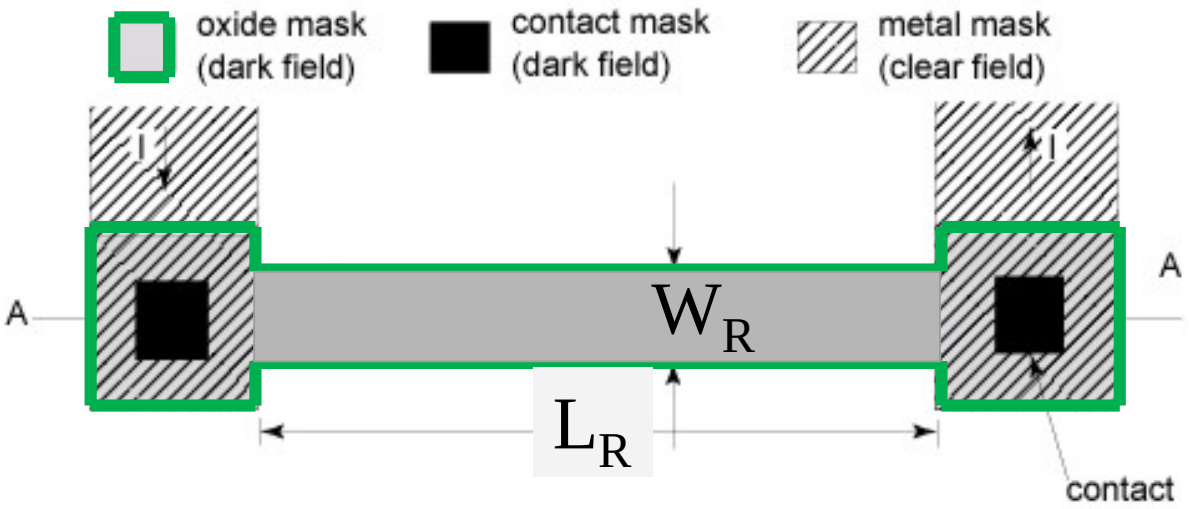
- **nMOS logic (examples)**
  - Truth table
  - Calculation
  - **Layout**
- Design Exercise 2017 (15% marks)

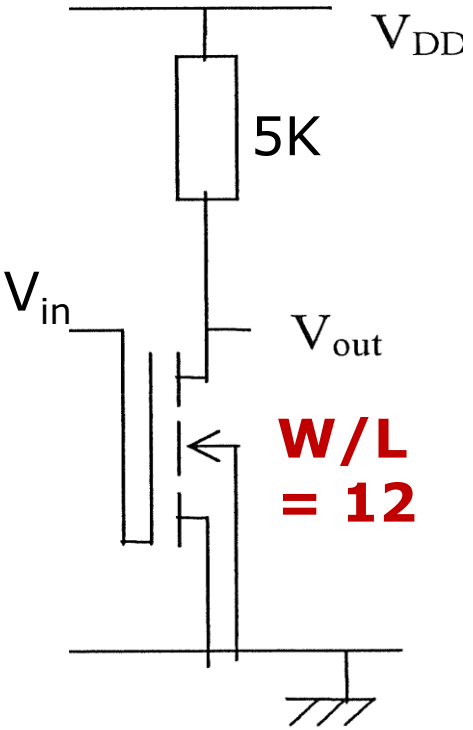
nMOS Logic (Inverter): example1



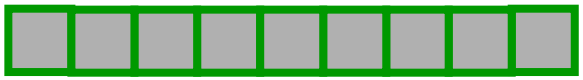


nMOS Logic (Inverter): example1

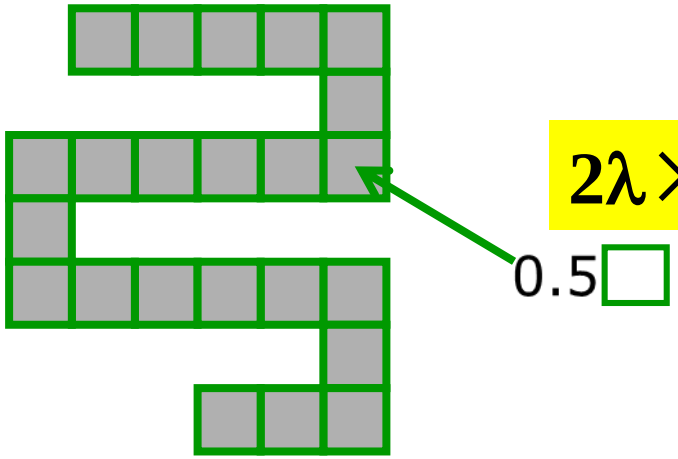




For small L_R/W_R:
(e.g. L_R/W_R=9)

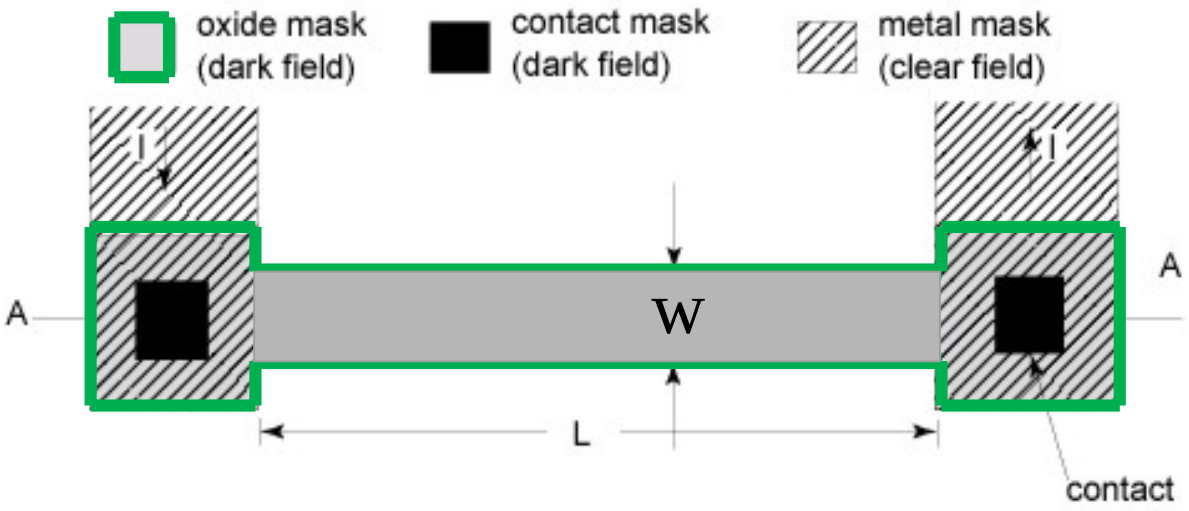


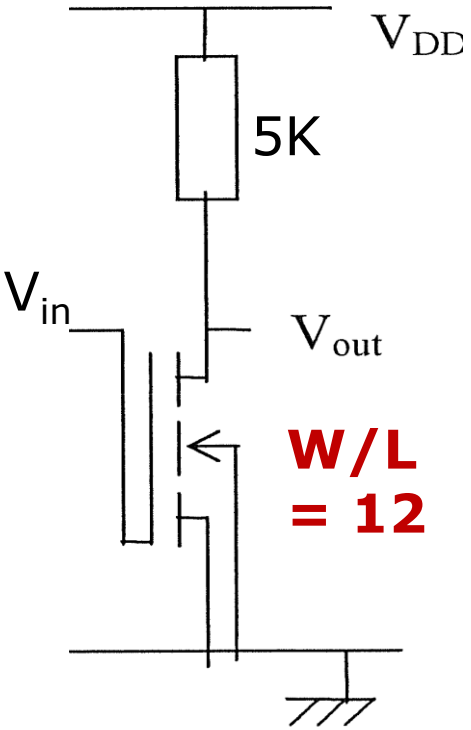
For large L_R/W_R:
(e.g. L_R/W_R=20)



Squares are used to calculate the length, L.

nMOS Logic (Inverter): example1



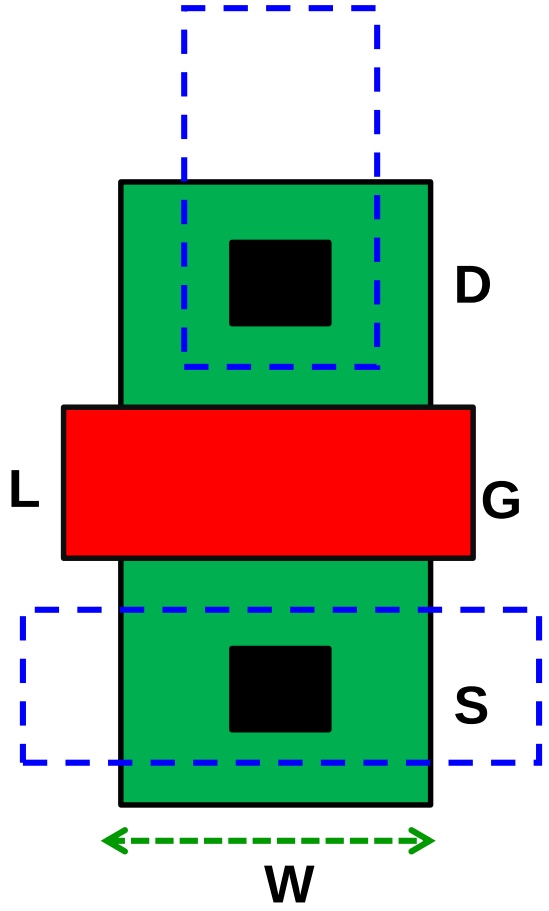


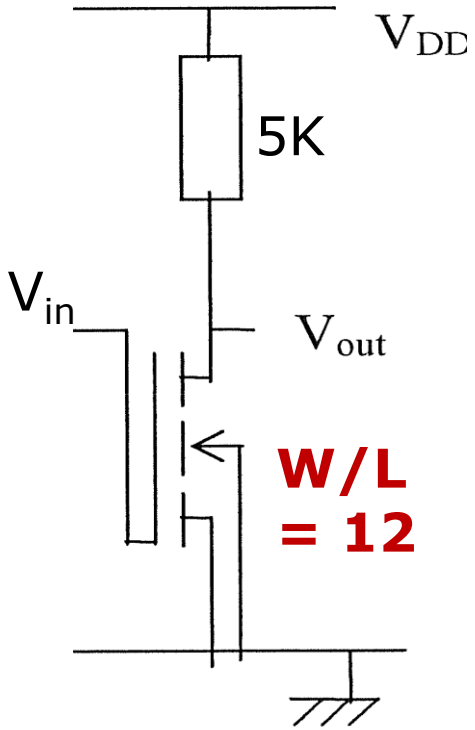
For small L_R/W_R:
(e.g. L_R/W_R=9)

For large L_R/W_R:
(e.g. L_R/W_R=20)

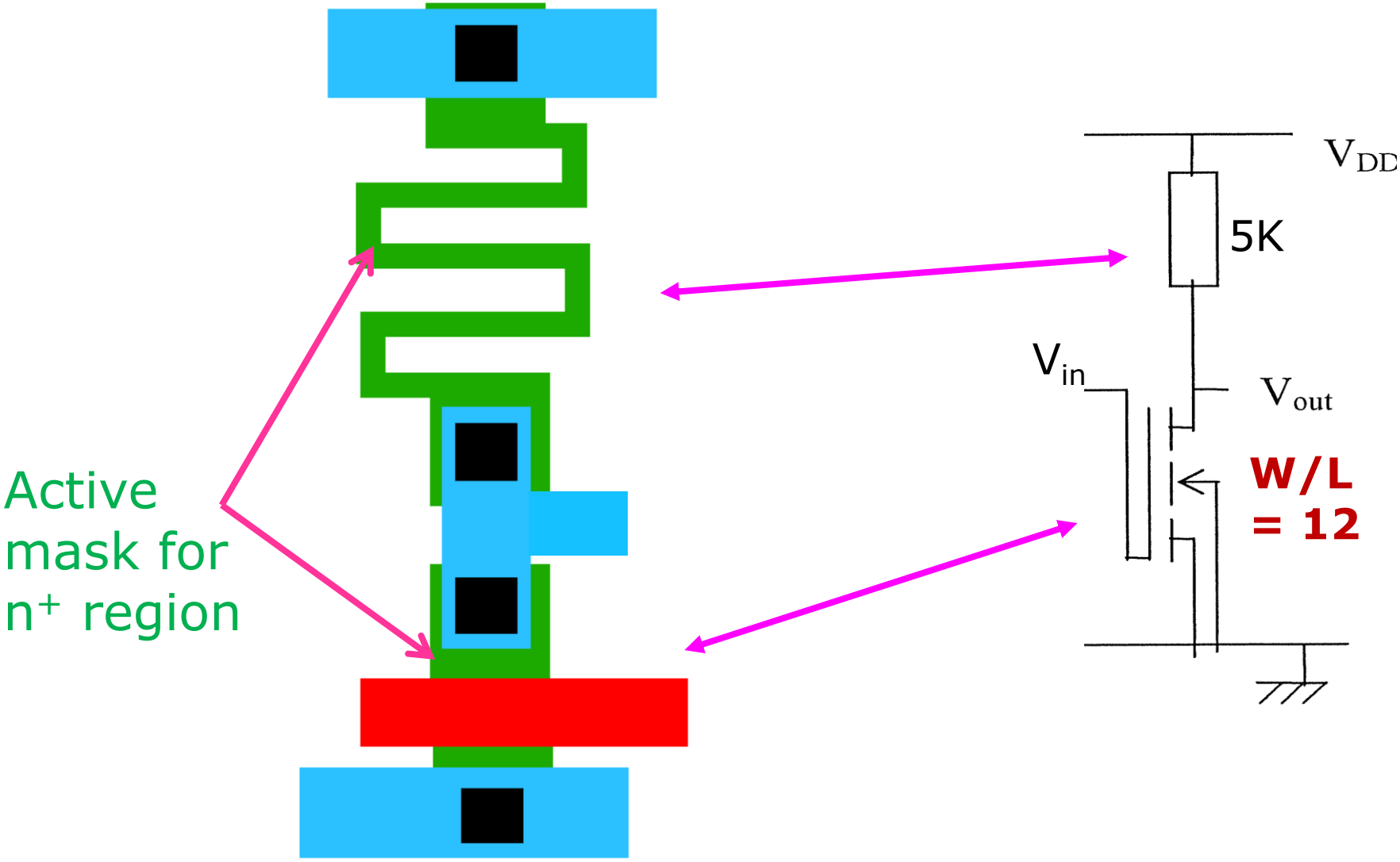
Every square must disappear when drawing your layout

nMOS Logic (Inverter): example1





nMOS Logic (Inverter): example1

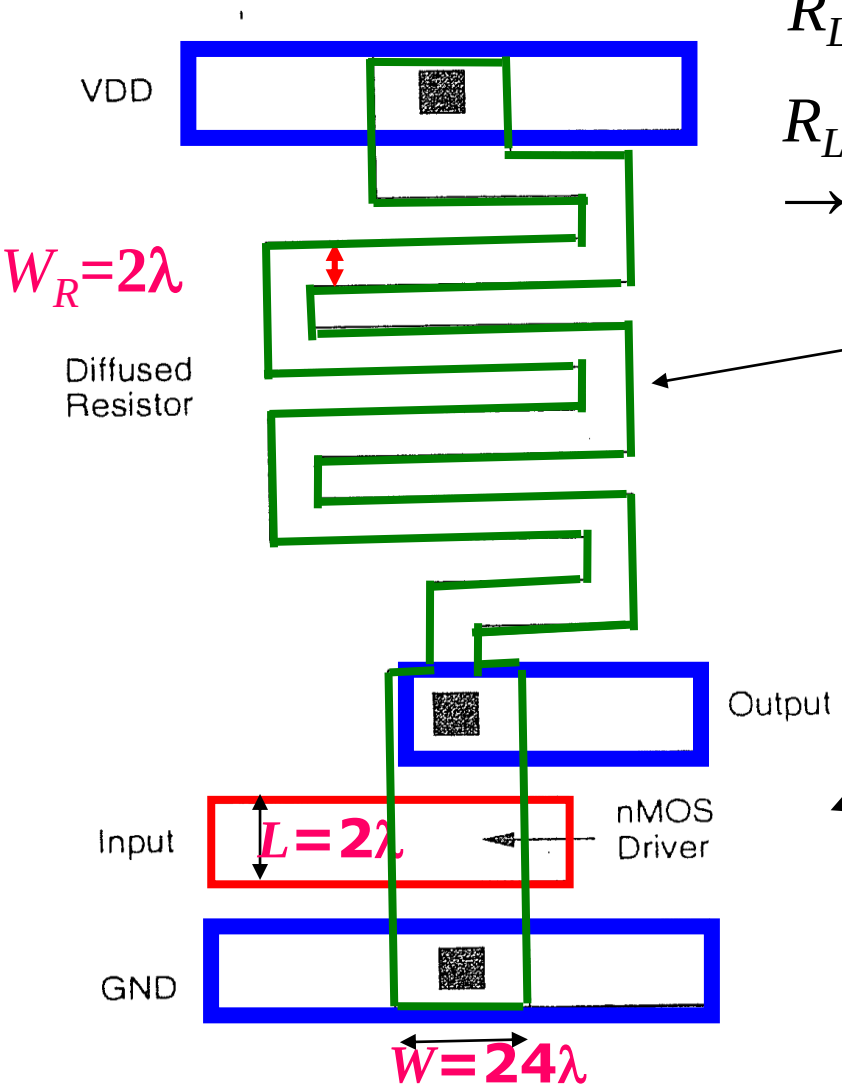


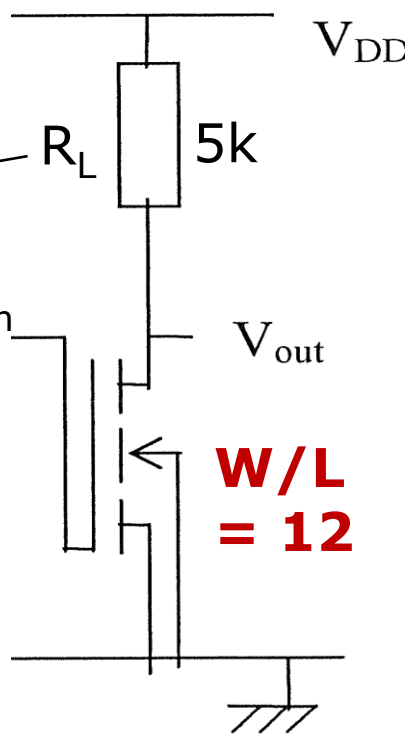
NMOS Logic (Inverter): example1

R_L=5k & R_s=100Ω/sq

$R_L=R_s(L_R/W_R)$

→ L_R/W_R=50



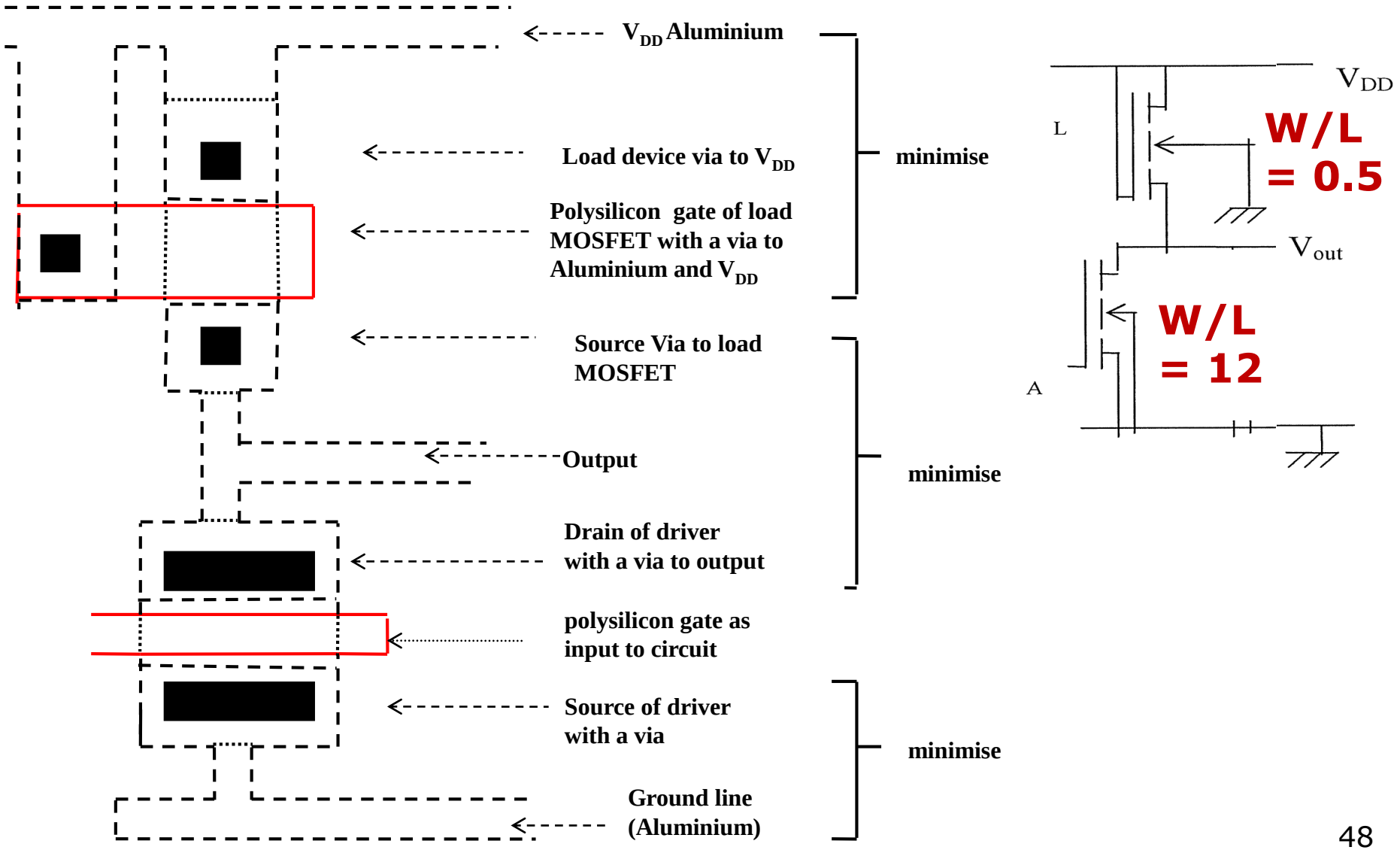


MOSFET

→ W/L=12

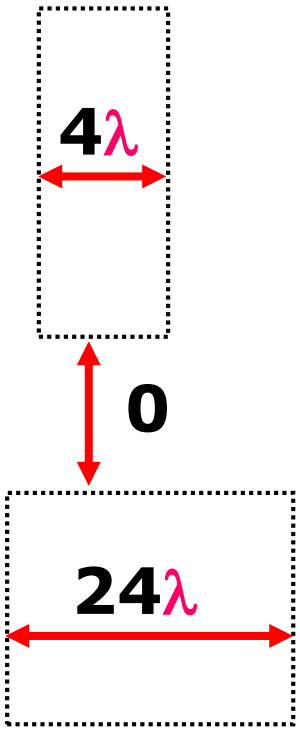
W/L = 12

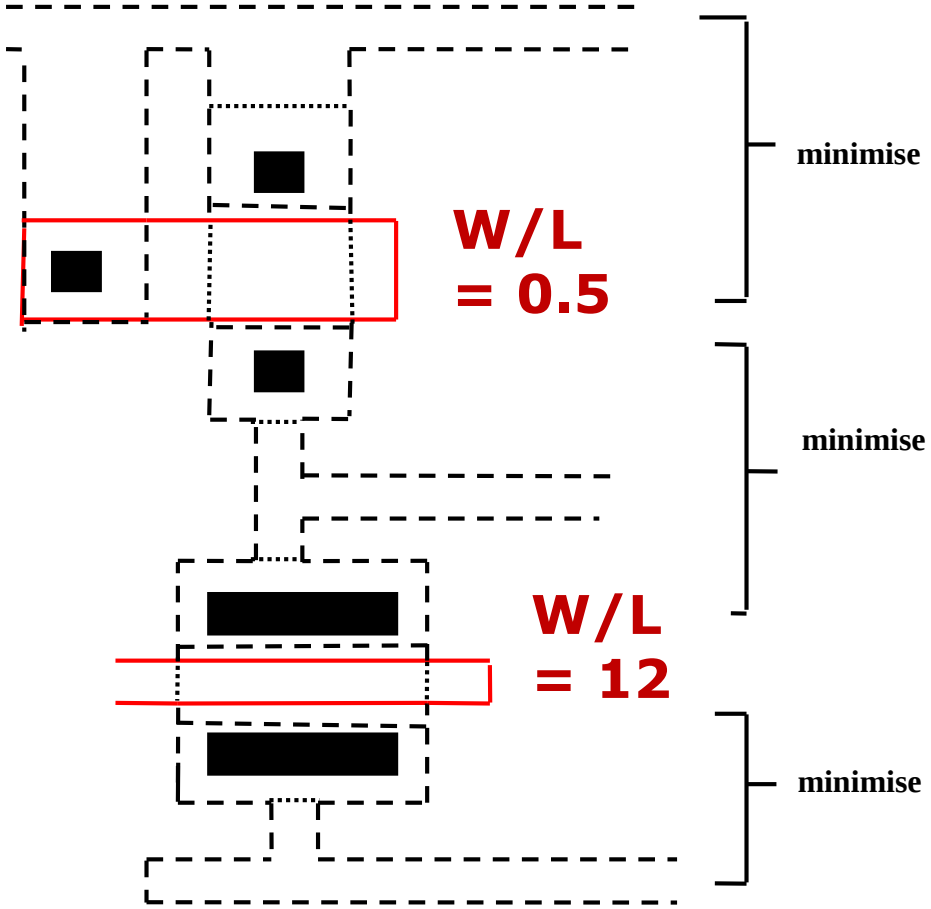
nMOS Logic (Inverter): example2



nMOS Logic (Inverter): example2

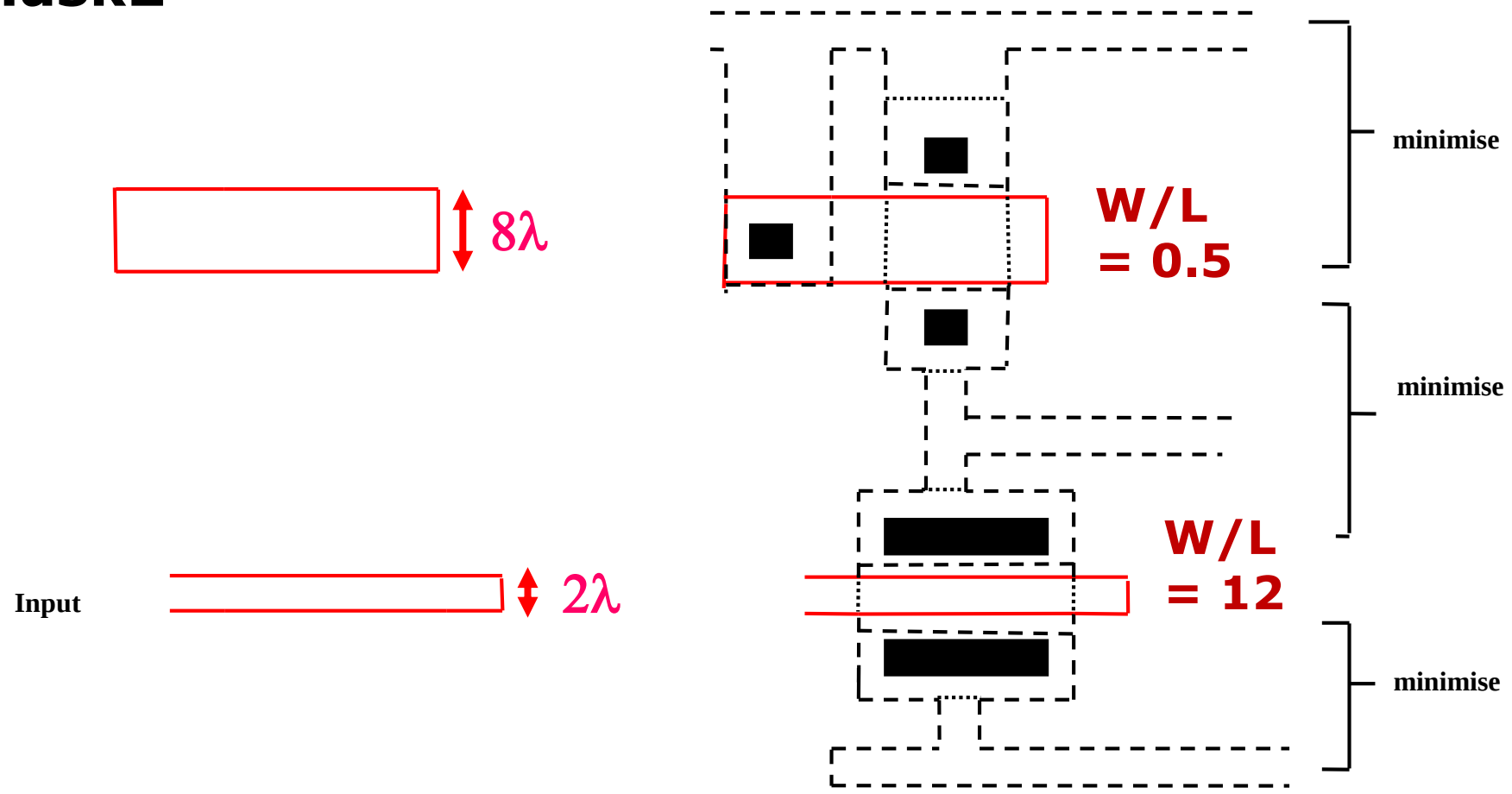
Mask1





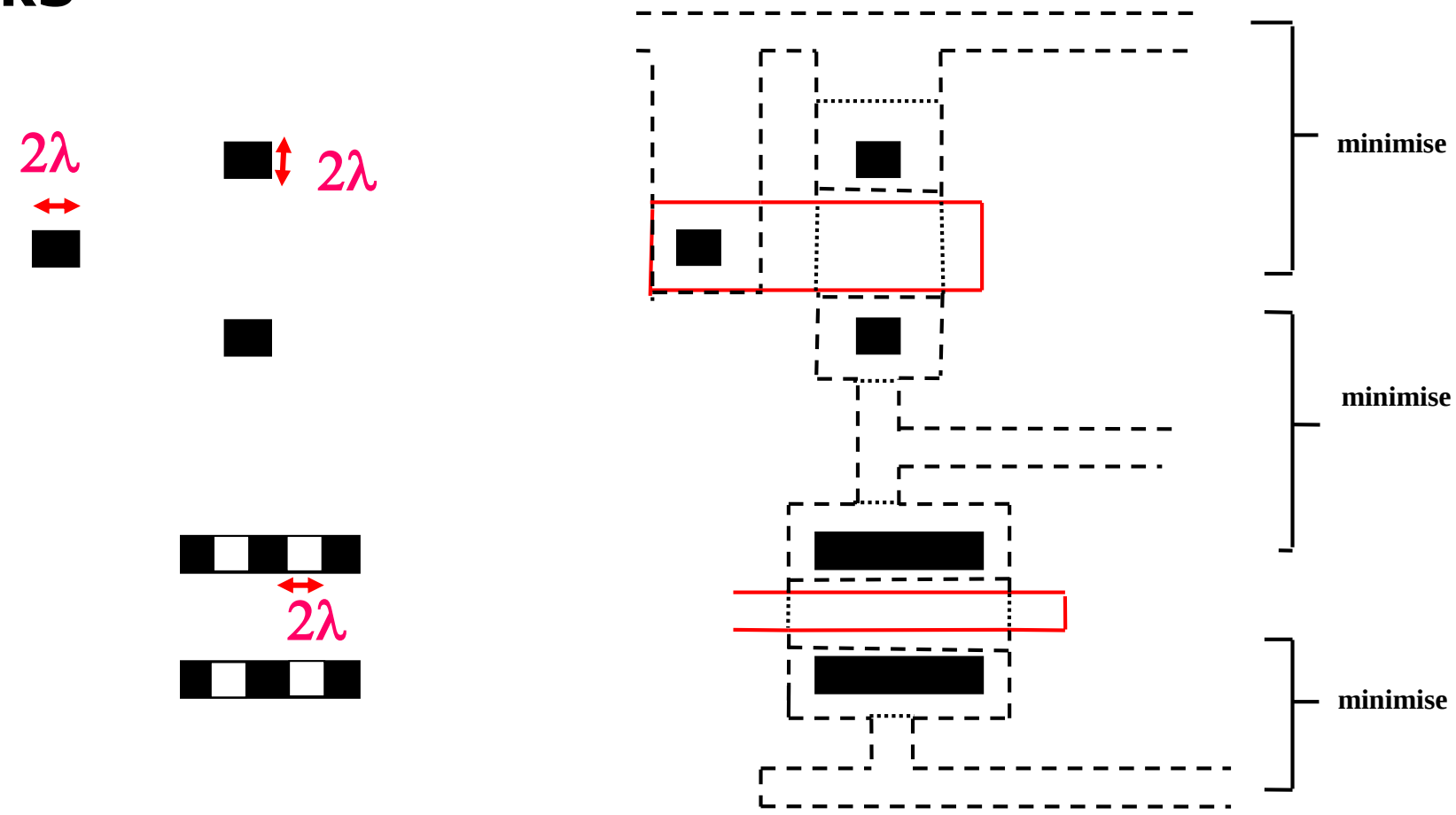
nMOS Logic (Inverter): example2

Mask2



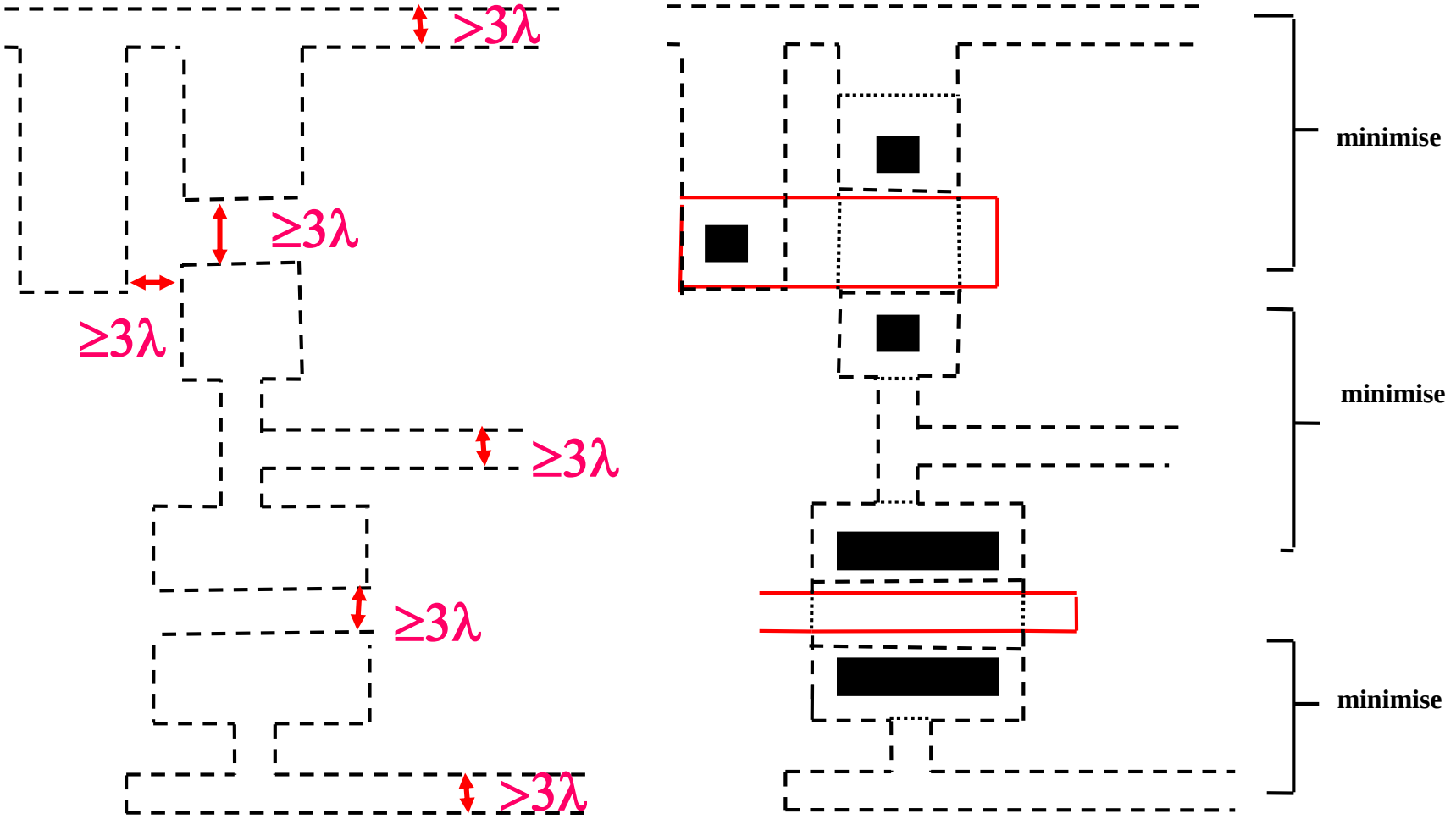
nMOS Logic (Inverter): example2

Mask3

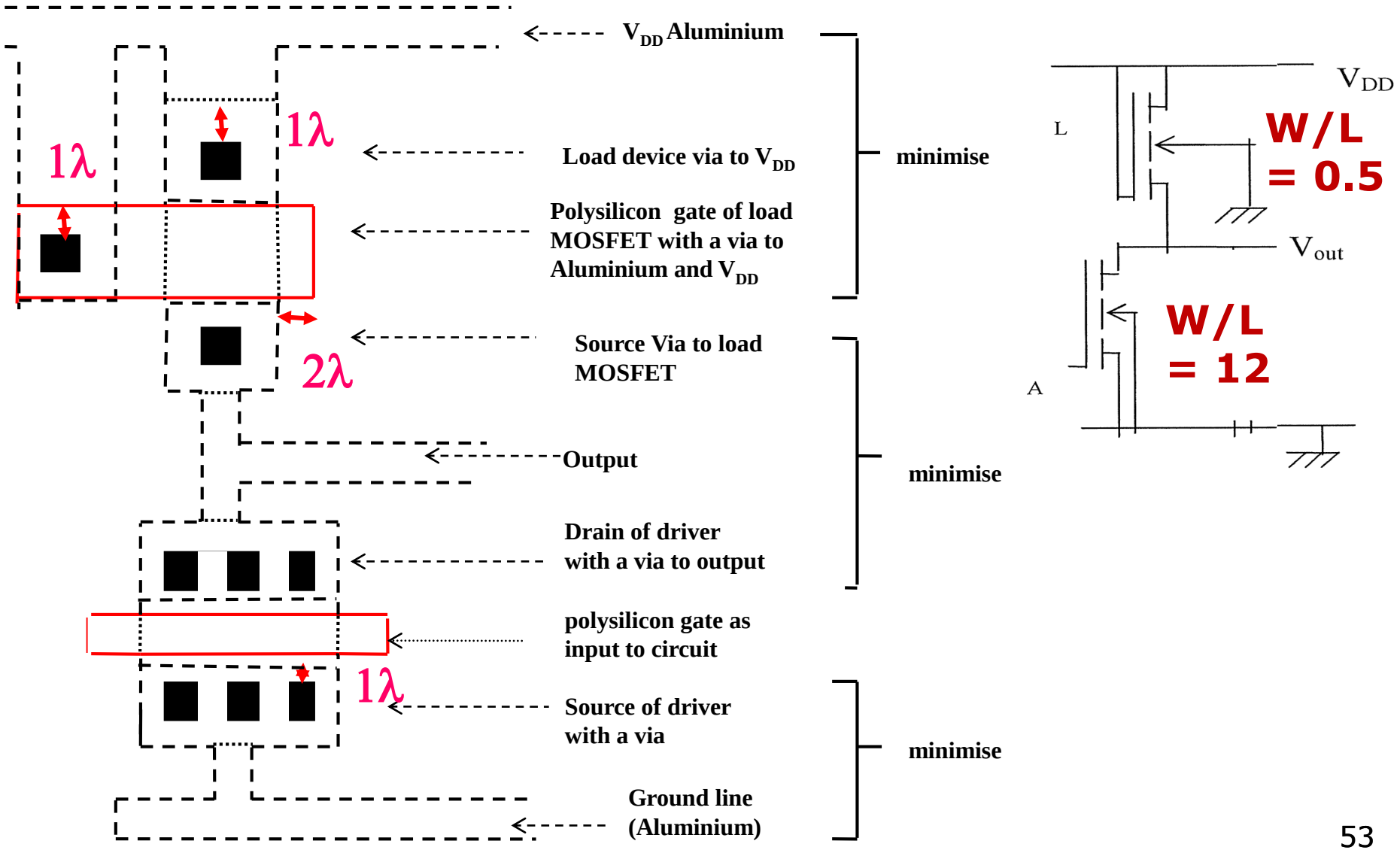


nMOS Logic (Inverter): example2

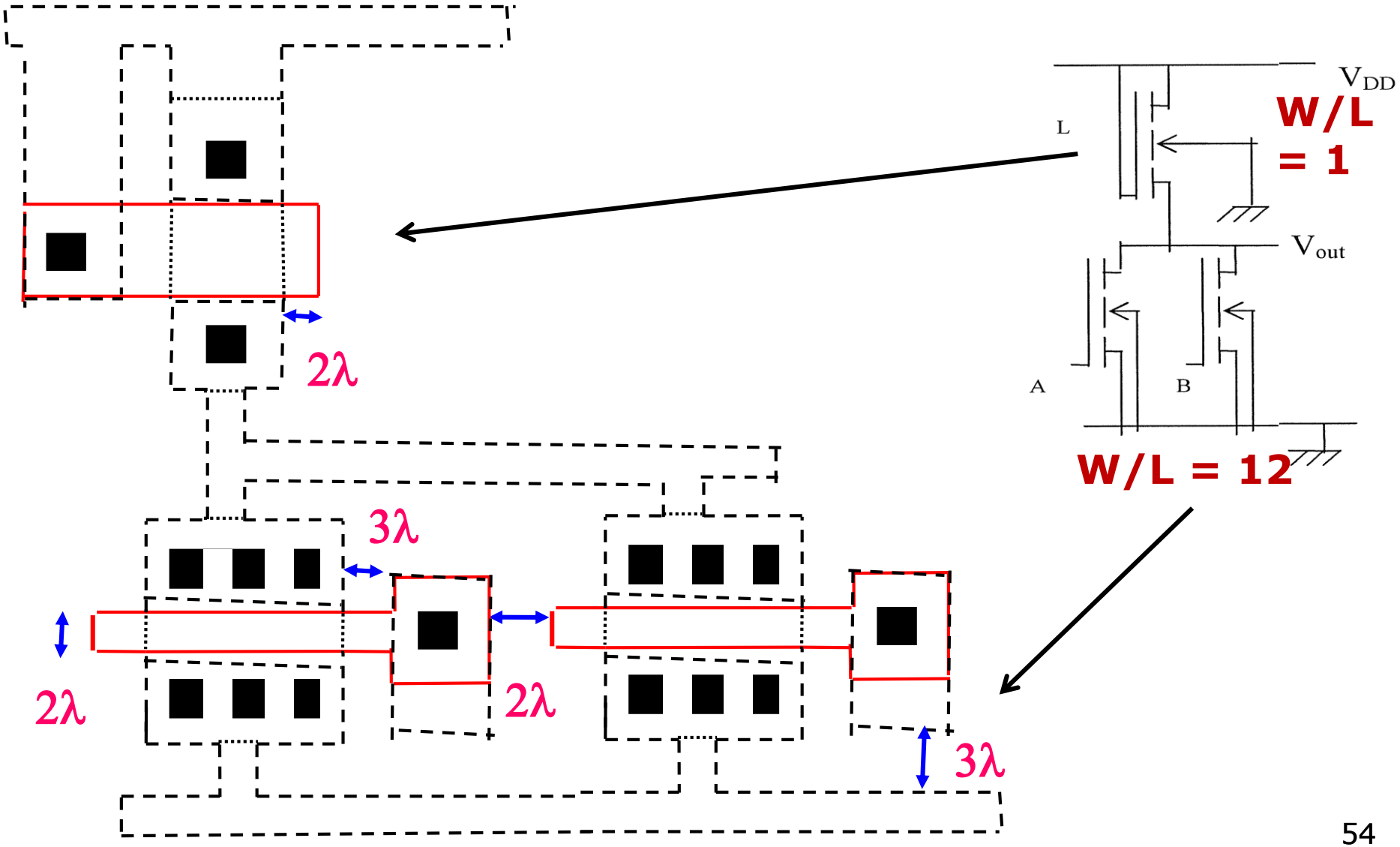
Mask4



nMOS Logic (Inverter): example2



nMOS NOR gate: example3



OUTLINE

- nMOS logic (examples)
  - Truth table
  - Calculation
  - Layout
- **Design Exercise 2017 (15% marks)**

Design Exercise 2017

Layout design of the nMOS IC shown in Fig.1

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$

$$\mu C_{ox} = \beta_0$$

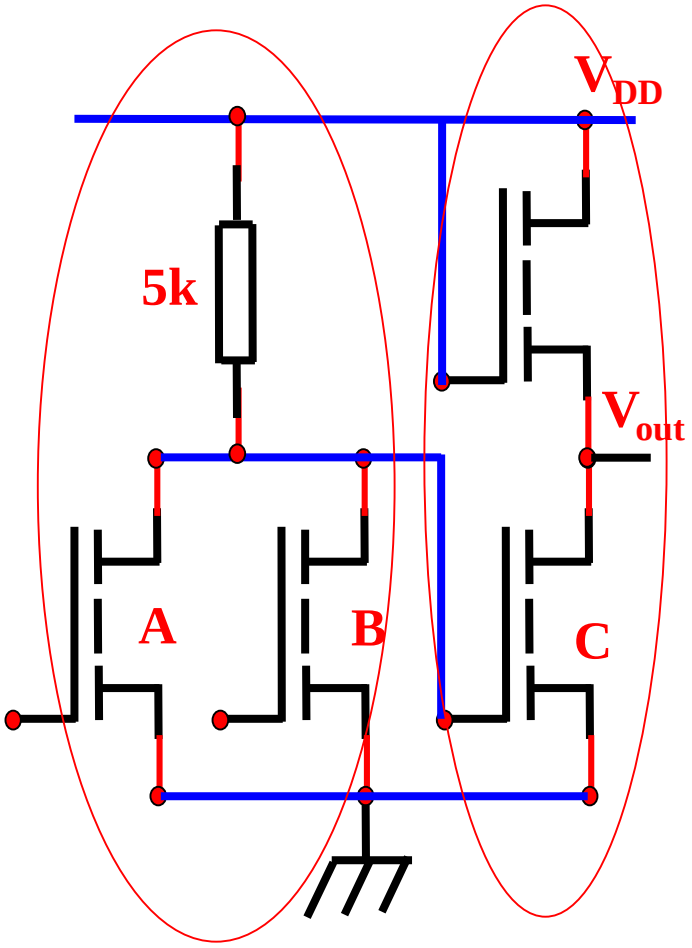
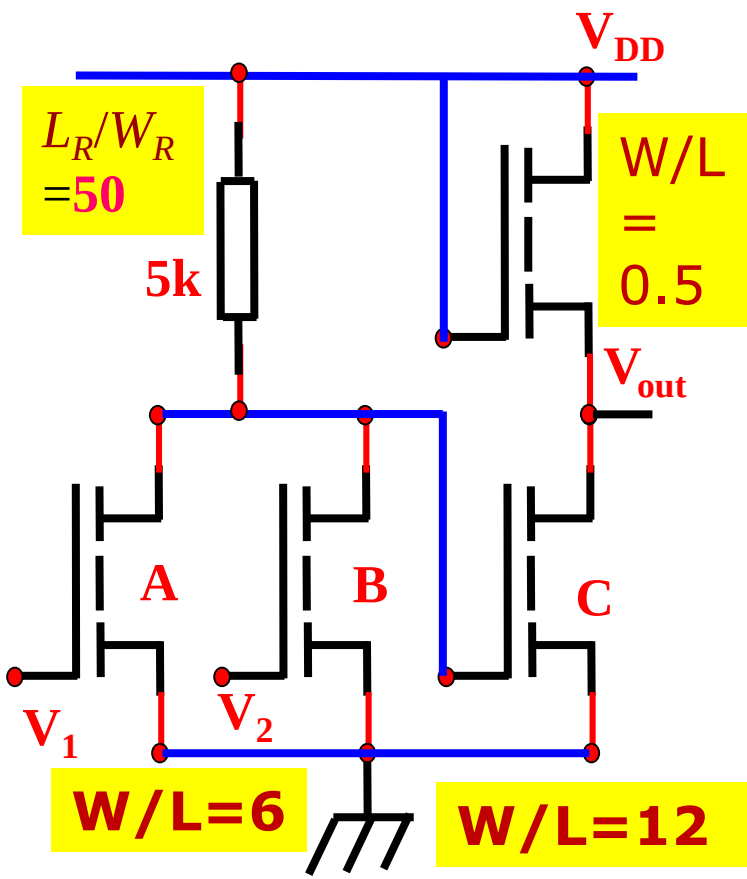


Fig.1

Design Exercise 2017

- Design rules:
- The driver transistors should have channel length L equal to the minimum feature size λ_m. The width of the drivers W, which must always be a whole number (n) of minimum feature sizes ($n\lambda_m$), and **the overall value of W must be chosen to give the required output voltage.** This must be significantly less than the threshold voltage of the third gate C if this transistor is to stay off.
- The layouts must take account of the alignment accuracy λ_a.
- $\lambda_m = 2\lambda_a$



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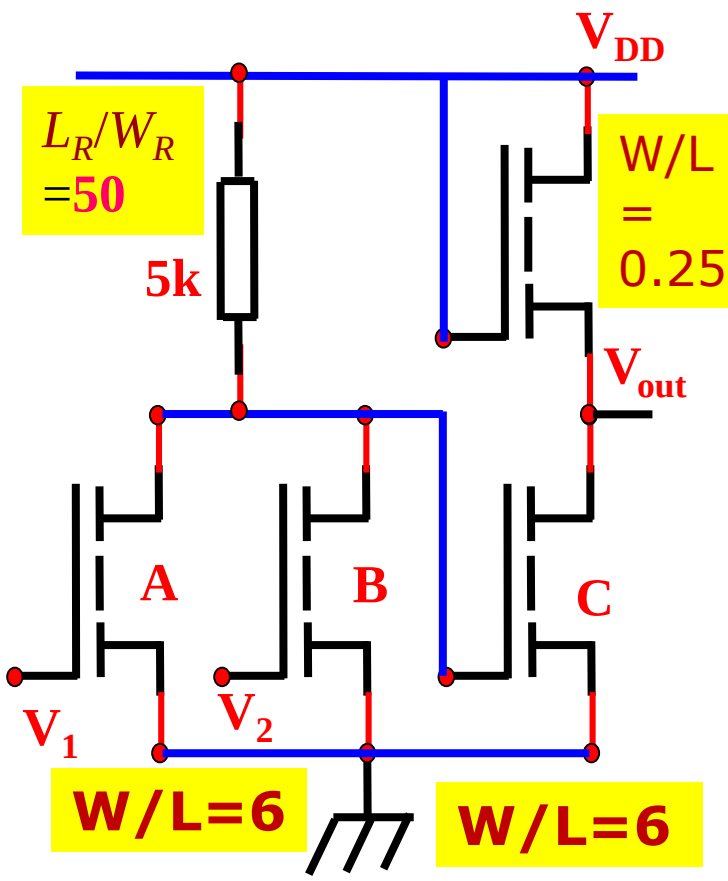


Design Exercise 2017

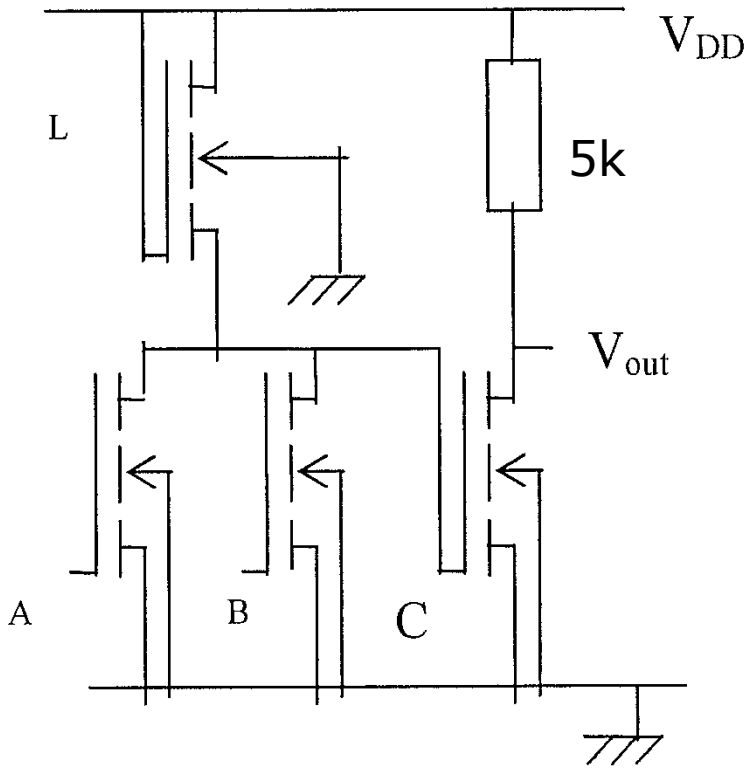
1) The Design involves producing the patterns corresponding to each of the stages of the process already discussed.
2) Each of the patterns should be drawn on graph paper with a stipulated scale. (e.g **1μm per cm**.)
3) The patterns would be transferred at a later stage to glass masks, as opaque regions. There are 4 masks :

M1. define the device area
M2. define the gate stripe
M3. define the contacts
M4. define the metal pattern

4) Your design paper should include 5 parts: ***4*** masks and ***1*** layout. Your report should include a brief explanation and calculations.

Example: Design Exercise 2016

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$
- HINTS: Liverpool notes.



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Design Exercise 2016

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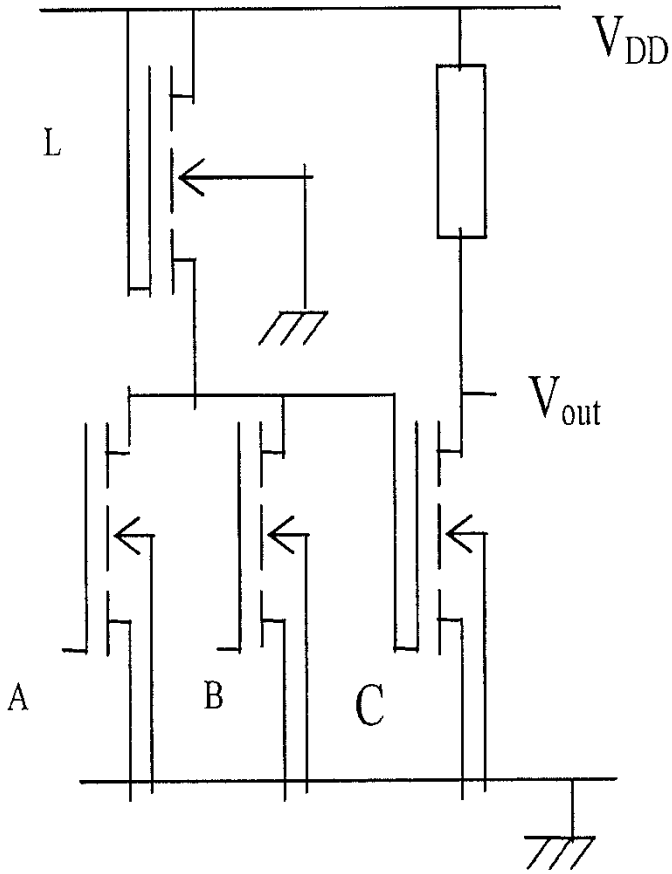
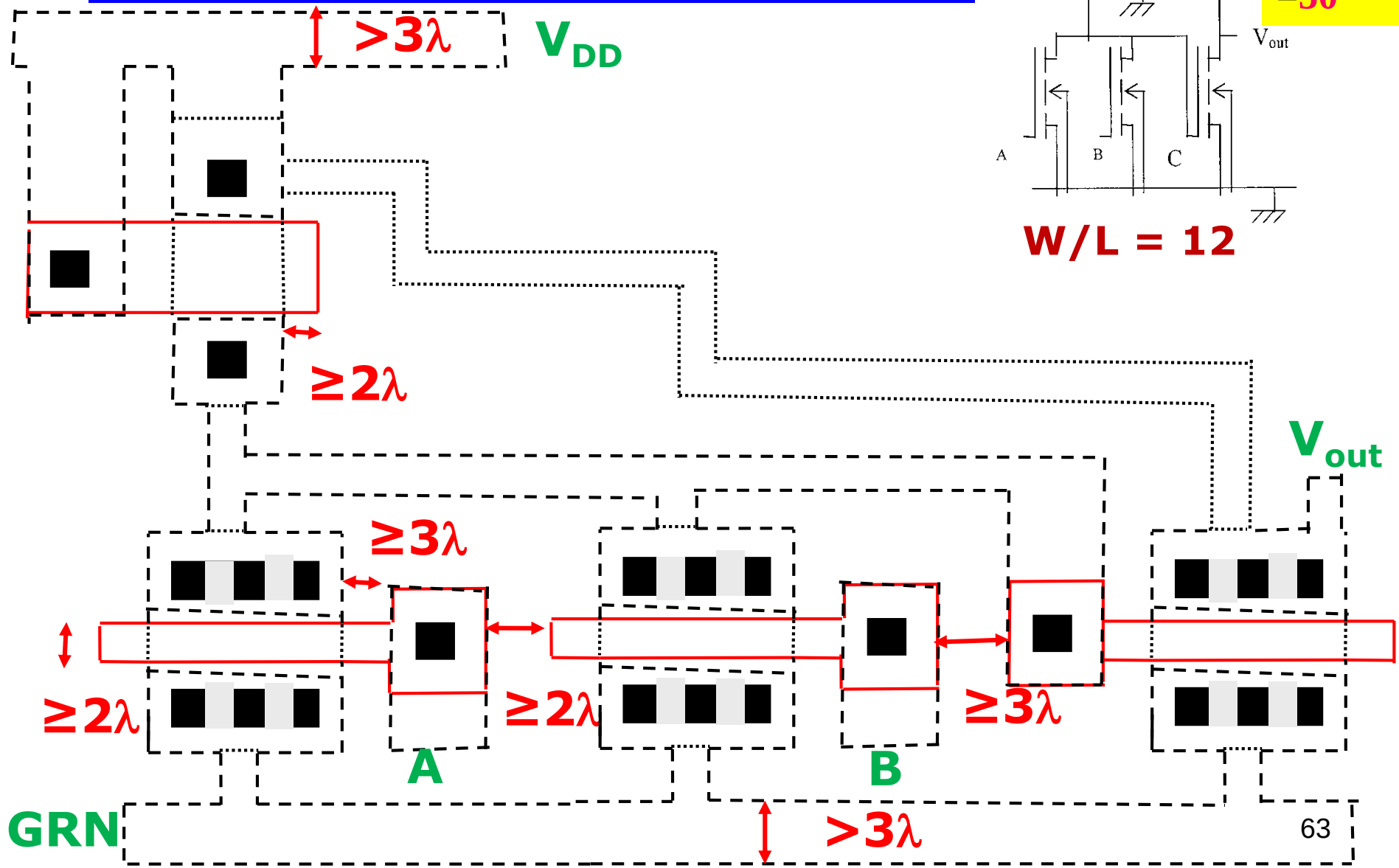
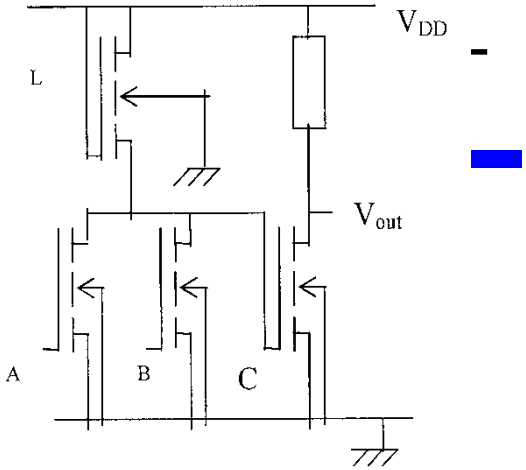
- The layouts must take account of the alignment accuracy λ_a.
- $\lambda_m = 2\lambda_a$ (correction needed)



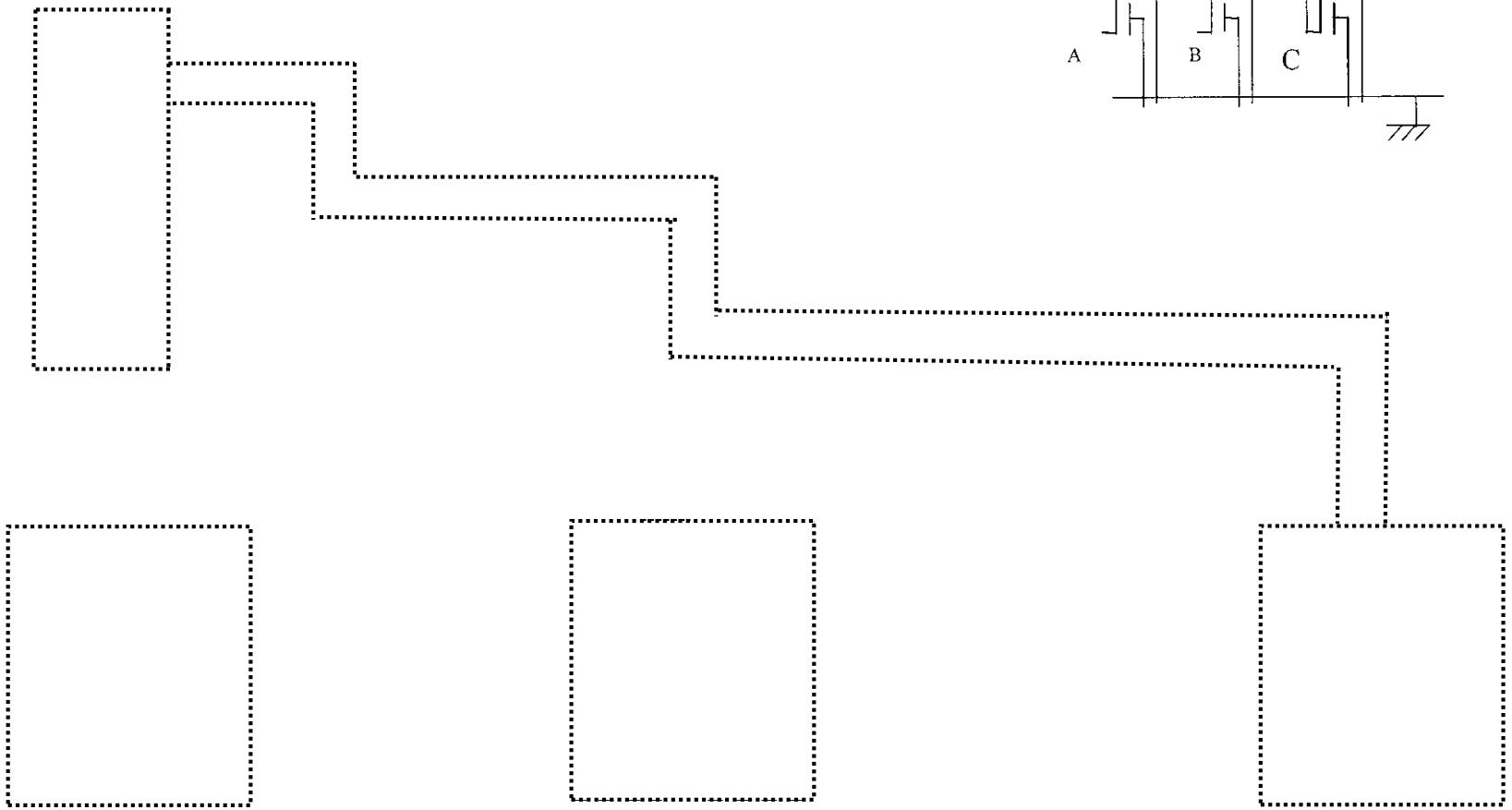
nMOS IC: example



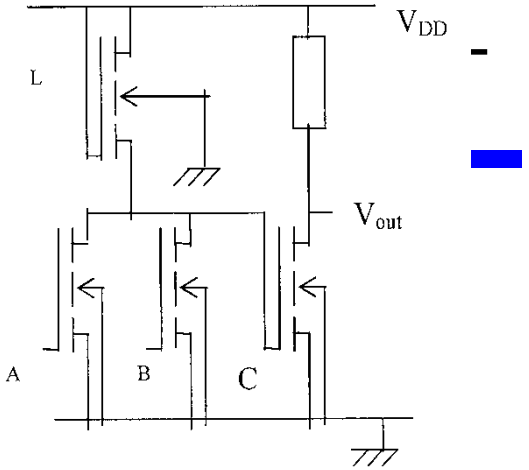
nMOS IC: example



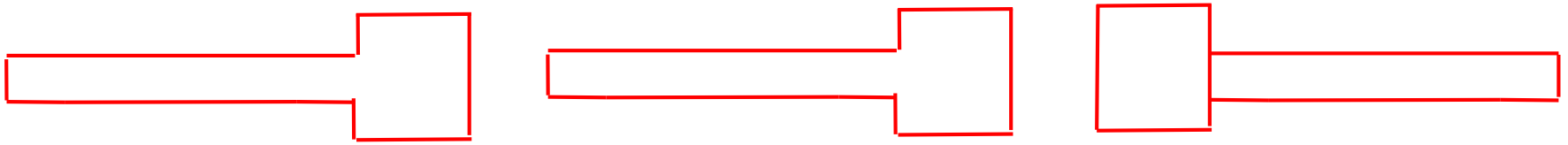
Mask1



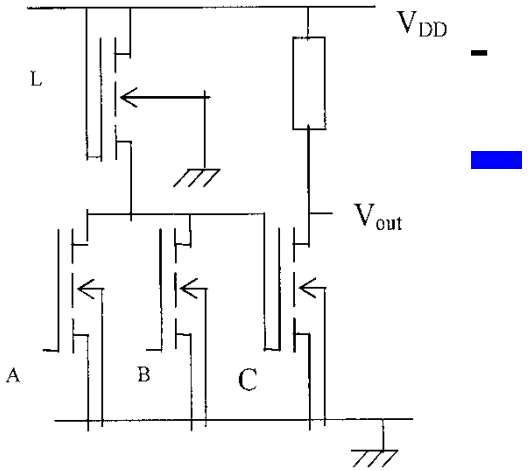
nMOS IC: example



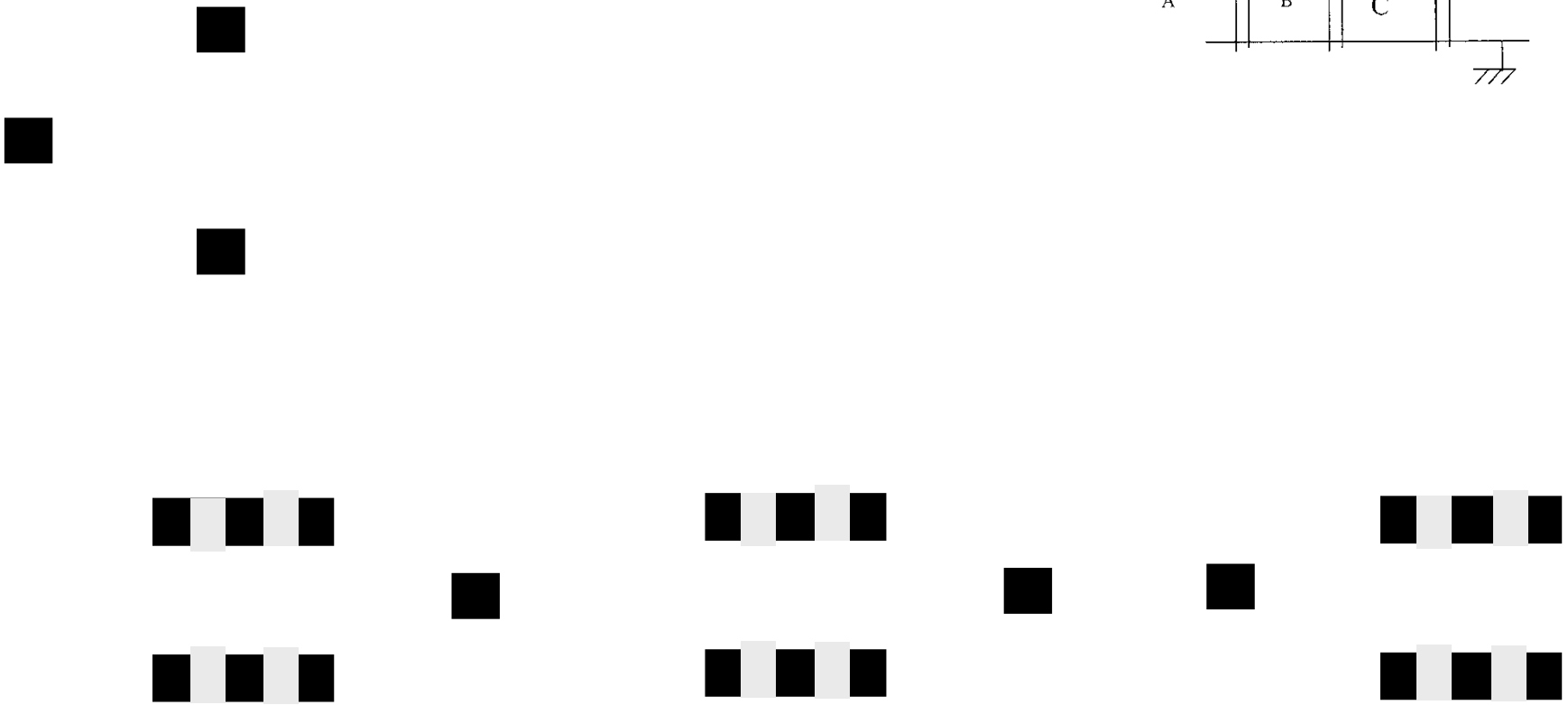
Mask2



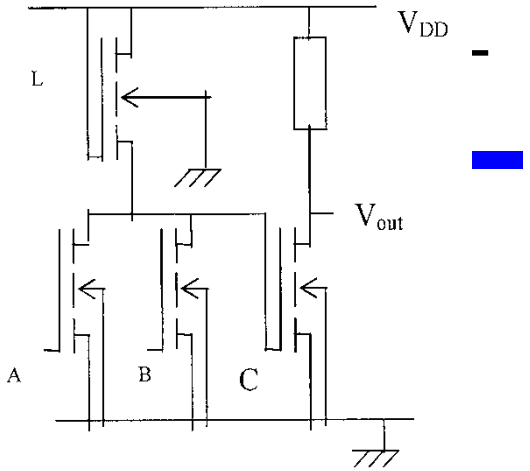
nMOS IC: example



Mask3

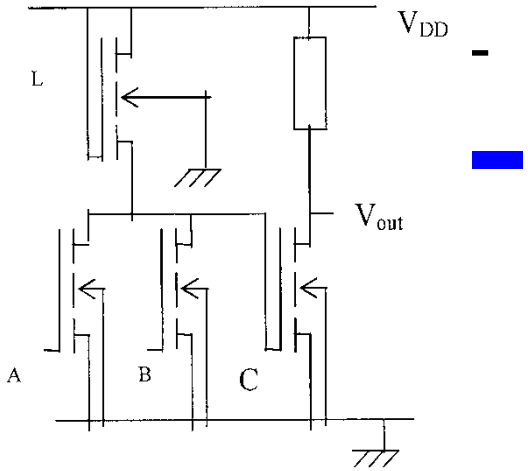


nMOS IC: example



Mask4

nMOS IC: example



Mask4