EEE104 – Digital Electronics (I)

Lecture 19

Dr. Ming Xu

Dept of Electrical & Electronic Engineering

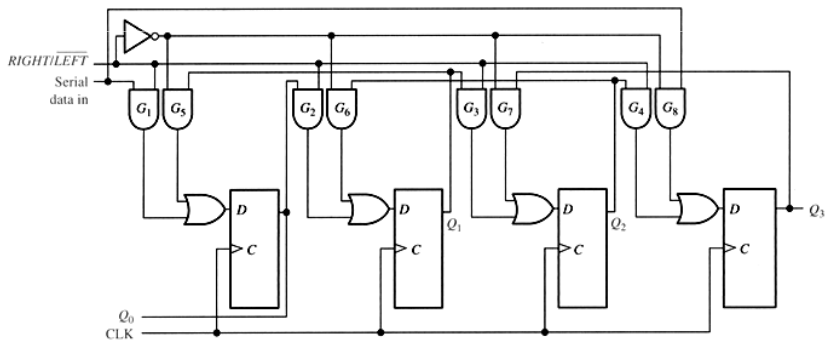
XJTLU

In This Session

- Shift Registers
  - Bidirectional Shift Registers
  - Shift Register Counters

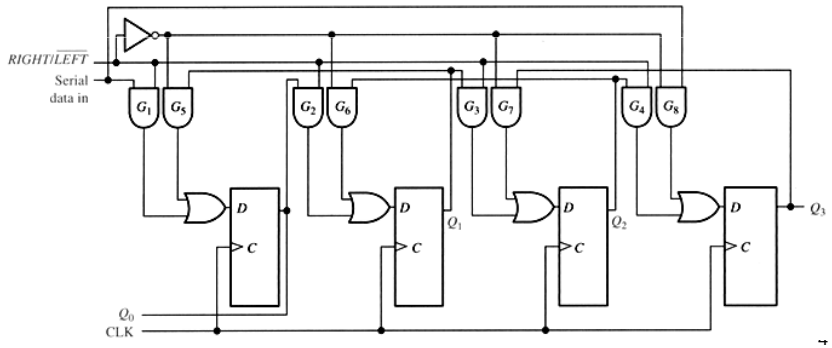
Bidirectional Shift Registers

- A HIGH on R/L will enable G_1 to G_4.
- The output of a stage is fed to the D input of the next stage.

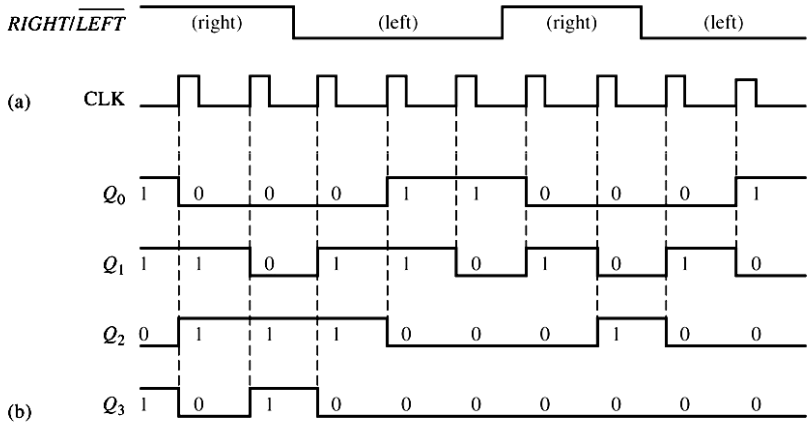


Bidirectional Shift Registers

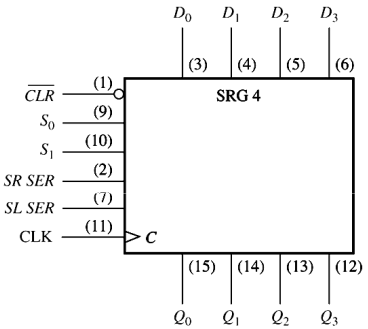
- A LOW on R/L will enable G_5 to G_8.
- The output of a stage is fed to the D input of the preceding stage.



Bidirectional Shift Registers



Bidirectional Shift Registers



74HC194: A 4-bit universal shift register

Mode selection

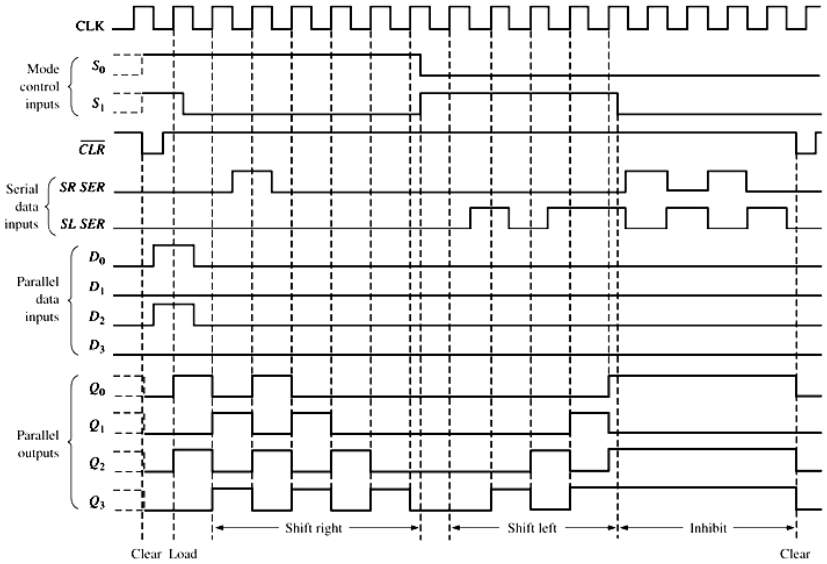
S_1	S_0	Mode
0	0	Inhibit
0	1	Shift right
1	0	Shift left
1	1	Load

SR SER: Shift-right serial data in

SL SER: Shift-left serial data in

CLR: asynchronous clear

Bidirectional Shift Registers



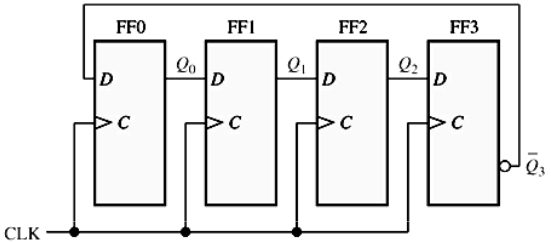
Shift Register Counters

- A **shift register counter** is a shift register with the serial output connected back to the serial input.
- It will produce a specified sequence of state **periodically**. Hence the name "counter".
- Two most common types are the Johnson counter and the ring counter.

The Johnson Counter

The **Johnson counter** – The *complemented* output of the last stage is connected back.

The counter will fill up with 1s first and then with 0s.

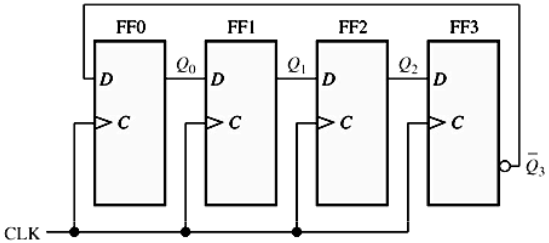


Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

The Johnson Counter

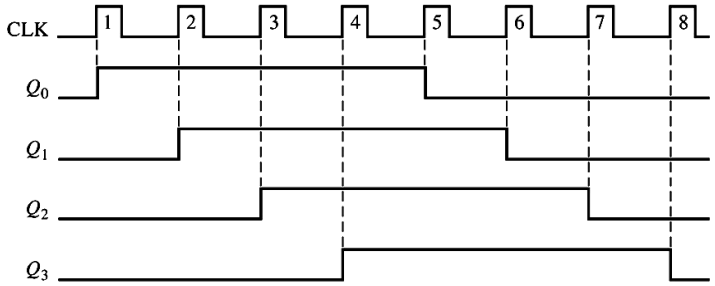
What will happen if the initial state are not one of the 8 states?

The counter will loop through the other 8 states.



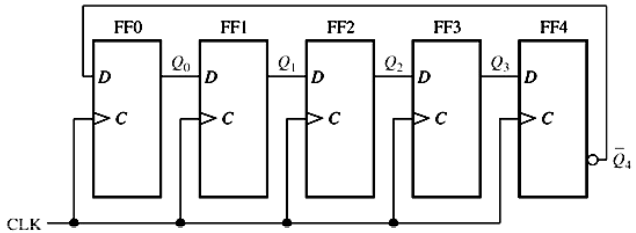
Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	1	0
1	1	0	0	1
2	0	1	0	0
3	1	0	1	0
4	1	1	0	1
5	0	1	1	0
6	1	0	1	1
7	0	1	0	1

The Johnson Counter



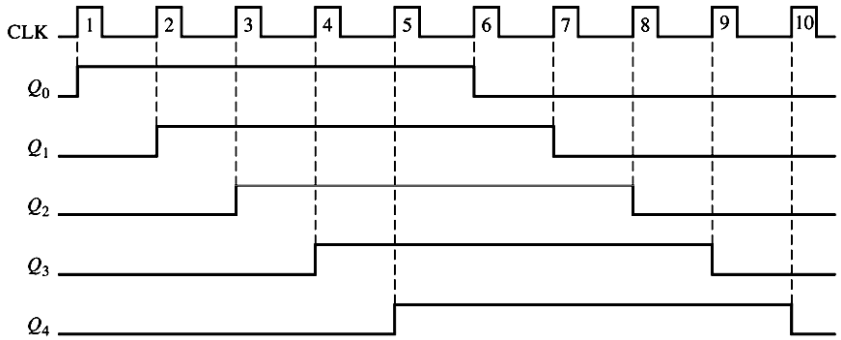
A 4-bit Johnson counter has 8 states.

The Johnson Counter



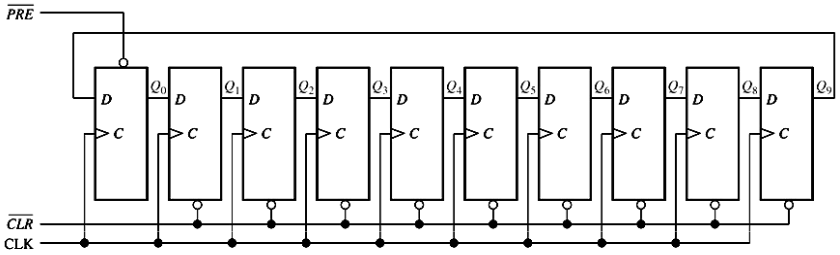
Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

The Johnson Counter



A 5-bit Johnson counter has 10 states. So an n-stage Johnson counter will have 2n states.

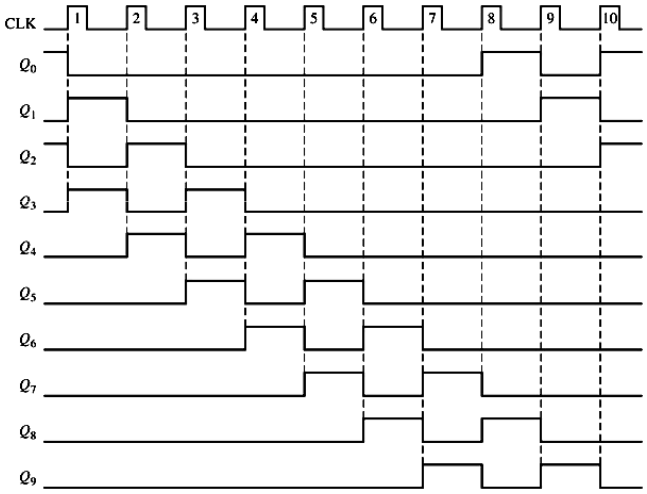
The Ring Counter



Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

The output of the last stage is connected back.

The Ring Counter



Shift Register Counters

- The disadvantage is that the maximum available states are not fully utilized.
- Beware that both the Ring and the Johnson counter must initially be forced into a valid state in the count sequence, because they operate on a subset of the available number of states. Otherwise, the ideal sequence will not be followed.
- The advantage over a binary counter is that no extra decoding circuit is needed.