EEE112 Integrated Electronics and Design
nMOS IC Design Project

Assessment Weighting

This assessment counts for **15%** of the module.

Aims

This project aims to provide students with an experience of designing a simple integrated circuit at the Silicon layout level, as well as offering an insight into the manufacturing process flow.

Learning Outcomes

On completion of this project you should be able to:

1. Understand the manufacturing processes involved in fabricating silicon based devices. In particular the nMOSFETs.
2. Understand the design process and constraints involved in developing IC's.
3. Produce layout and mask designs to scale of an nMOSFET logic circuit.
4. Produce an engineering style report.

Design Task

The objective of this assignment is to design and minimize the layout and masks for each layer required to manufacture the simple logic circuit shown in Figure 1, being formed at the component level as shown in Figure 2.

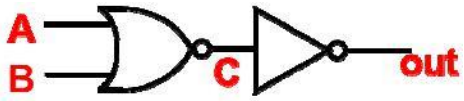

Fig. 1 Logic symbol

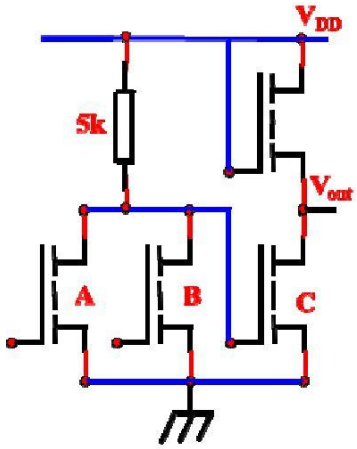

Fig.2 Logic circuit

The process parameters for the design are listed in Table 1. You should use these to calculate the aspect ratio or width/ length of each component and then determine a suitable layout to interconnect the components, while minimizing surface area.

Table 1: Process Parameters

Normalized Device Constant β_0	1.8×10^{-4} A/V^2
Threshold Voltage V_T	0.3 V
Supply Voltage V_{DD}	5 V
High Input Voltages (A and B) V_{IN}	V_{DD}
Low Input Voltages (A and B) V_{IN}	0 V
MOSFET Load Resistance R_L	5 kΩ
Sheet Resistance R_S	100 Ω/□

Once you have calculated the component sizes using the data in the table you should be able to produce a full circuit design layout to scale together with the necessary masks to form each layer, by considering the MOSIS design rules (see page 5), and your knowledge from the lectures.

You should attempt to minimize the surface area required for fabrication.

Assignment Output and Grading Information

Layout (50%)

On the sheet of squared graph paper provided (Yang Wang from Room EE205A) you should produce to a suitable scale (e.g. 1 cm = 2λ) the following designs (all with the same scale):

1. Active layer Mask
2. Poly-Si layer Mask
3. Contact layer Mask
4. Metal Mask
5. Layout of the design – Overlay of Masks

Use different line styles or fills to differentiate between layers and make sure there is a clear legend defining the styles for each layer and the scale of the design.

Your design will be graded on the following points (10% for each):

Layout (50%)

1. Layout Design: Application of design rules, clearly show each mask overlaid so that the spacing is clearly visible. (Use various line styles or fills to differentiate mask regions)
2. Active Mask, Contact Mask and Poly Mask: Application of design rules, (Ensure that all design requirements shown on page 5 are met e.g. min. poly spacing is 2λ or minimum contact size is 2λ)
3. Metal Mask: Application of design rules (such as interconnection width and spacing 3λ, VDD and ground >3λ, ensure all regions meet minimum size requirements).
4. Safety Margins: Application of design rules for protection against alignment error (such as all holes are covered by 4λ metal, min. gate extension of poly over active is 2λ)
5. All 4 masks must be drawn to the have the same size (outline areas should be equal). The spacing between each component should be minimized to minimize chip area.

Report (50%)

Write a short formal report to accompany the design. The report will be graded against the requirements are set out below (10% for each):

1. Report format: cover page, contents, abstract, introduction, main body, conclusion, references. Abstract: read and understood independently of the rest of the report. Introduction should include the design specification.
2. Main body 1: fabrication process flow of nMOS ICs and design rules' description.
3. Main body 2: design of the logic circuit (truth table and calculation of the aspect ratio of W/L)

4. Main body 3: results (design rules application on 4 masks) and discussion [chip area calculation, discuss how to reduce the chip area (for example, to share source and drain of transistor A & B, or to replace the resistor R using an active resistor), what is the worst case (discussions to make sure $V_{out} << V_T$ at logic low), and how changing the value of V_{out} (for example, 0.1V and 0.01V) affects the size of the drivers].
5. Conclusion should be consistent with earlier sections.

Academic Misconduct

Students should be aware that when submitting assessed work that the work is their own and that it fully acknowledges the work and opinions of others. For further clarification students should read the latest version of the XJTLU Code of Conduct. These can be found on the university web pages.

Assignment Submission and Deadline

Please submit your completed design assignment (drawing paper + report) directly to the **assignment box outside of EB314 (EB, not EE!)** no later than:

5pm June 1st 2018-Friday (Week 14)

Also, e-copy of your report submitted on ICE.

Late submission shall follow university policy available on the university website.

Note: Please make sure you attach the **University assignment cover sheet** to your **report** and make sure that **your name and student ID** are clearly written on your **layout sheet (drawing paper)**.

MOSIS Layout Design Rules

Active Area Rules

R1	Minimum Active area Width	3λ
R2	Minimum Active area Spacing	3λ

Poly-Silicon Rules

R3	Minimum Poly Width	2λ
R4	Minimum Poly Spacing	2λ
R5	Minimum Gate extension of Poly over Active	2λ
R6	Minimum Poly-Active Edge Spacing (Poly Outside of Active area)	λ
R7	Minimum Poly-Active Edge Spacing (Poly Inside of Active area)	3λ

Metal Rules

R8	Minimum Metal Width	3λ
R9	Minimum Metal Spacing	3λ

Contact Rules

R10	Poly Contact size	2λ
R11	Minimum Poly Contact Spacing	2λ
R12	Minimum Poly Contact to Poly Edge Spacing	λ
R13	Minimum Poly Contact to Metal Edge Spacing	λ
R14	Minimum Poly Contact to Active Edge Spacing	3λ
R15	Active Contact size	2λ
R16	Minimum Active Contact Spacing (On the same Active region)	2λ
R17	Minimum Active Contact to Active Edge Spacing	λ
R18	Minimum Active Contact to Metal Edge Spacing	λ
R19	Minimum Active Contact to Poly Edge Spacing	2λ
R20	Minimum Active Contact Spacing (On different Active regions)	6λ

Supply Rail Metal

R21	V_{DD}	>3λ
R22	Ground	>3λ

Resistor Rules

R23	Minimum resistor width	2λ