EEE104 – Digital Electronics (I)

Lecture 11

Dr. Ming Xu

Dept of Electrical & Electronic Engineering

XJTLU

In This Session

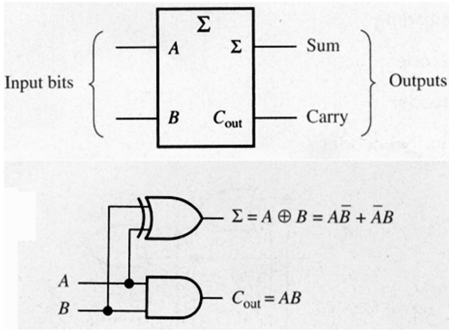
- Functions of Combinational Logic Gates
  - Adders
  - Comparators
  - Decoders

Basic Adders – The Half-Adder

The half-adder does not add an input carry.

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

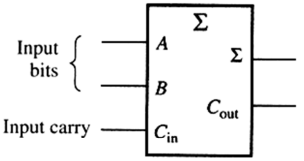
Σ = sum
C_{out} = output carry
A and B = input variables (operands)



- The sum is 1 only when the inputs are different — an XOR operation.
- The output carry is 1 only when both the inputs are 1 — an AND operation.

Basic Adders – The Full-Adder

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

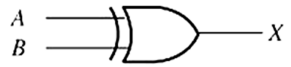


$$\Sigma = (A \oplus B) \oplus C_{in}$$

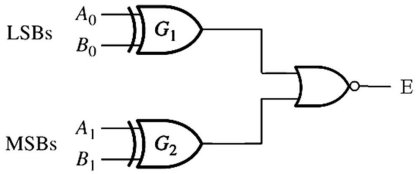
$$C_{out} = ABC_{in} + AB\bar{C}_{in} + A\bar{B}C_{in} + \bar{A}BC_{in}$$
$$= \left(ABC_{in} + AB\bar{C}_{in}\right) + \left(ABC_{in} + A\bar{B}C_{in}\right) + \left(ABC_{in} + \bar{A}BC_{in}\right)$$
$$= AB + AC_{in} + BC_{in}$$

Comparators — Equality Comparators

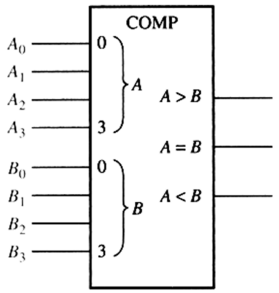
1. An XOR gate is a 1-bit comparator.



2. 2-bit comparators



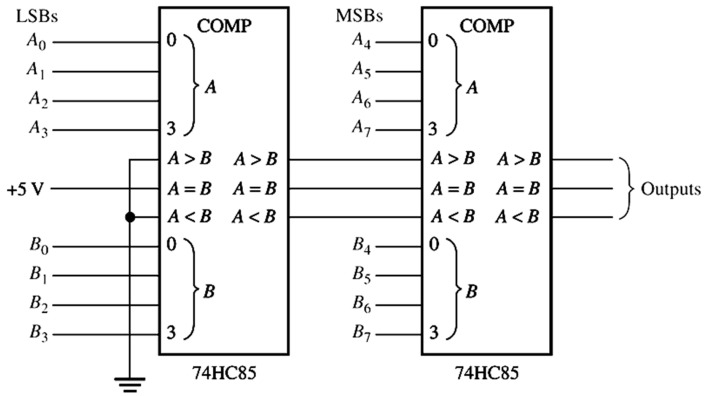
Comparators — Inequality Comparators



1. Check the highest–order bit first.
2. If $A_3 = 1$ and $B_3 = 0$, A > B.
3. If $A_3 = 0$ and $B_3 = 1$, A < B.
4. If $A_3 = B_3$, examine the next lower bit position.

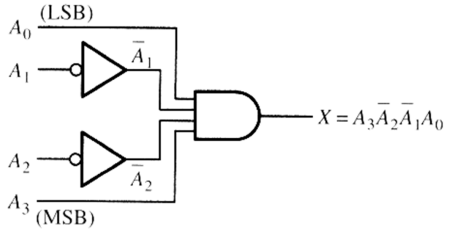
MSI magnitude comparator: 74HC85, which has three cascade inputs A < B, A = B, A > B.

Comparators — Inequality Comparators



Decoders

A decoder is used to detect a specified combination of input bits (code), e.g. to determine when the inputs are 1001.



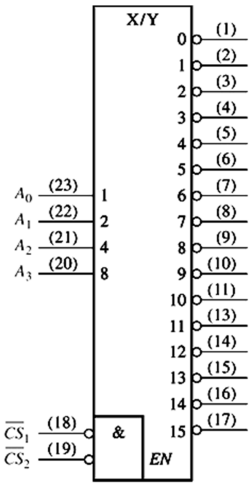
- The output is 1 only when $A_3A_2A_1A_0 = 1001$.
- Implemented with an AND (NAND) gate and inverters for an active-HIGH (LOW) output.

Decoders – The 4-Bit Decoder

The truth table (with active-LOW output)

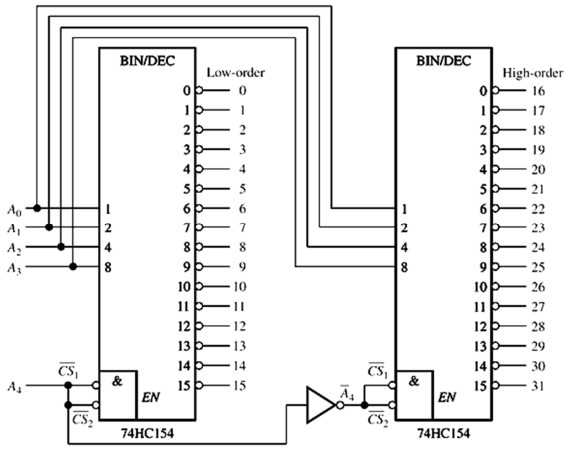
BINARY INPUTS				DECODING	OUTPUTS														
A_3	A_2	A_1	A_0	FUNCTION	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	$\overline{A}_3\overline{A}_2\overline{A}_1\overline{A}_0$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	$\overline{A}_3\overline{A}_2\overline{A}_1A_0$	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	$\overline{A}_3\overline{A}_2A_1\overline{A}_0$	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	$\overline{A}_3\overline{A}_2A_1A_0$	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	$\overline{A}_3A_2\overline{A}_1\overline{A}_0$	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	1	0	1	$\overline{A}_3A_2\overline{A}_1A_0$	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	1	0	$\overline{A}_3A_2A_1\overline{A}_0$	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	1	1	1	$\overline{A}_3A_2A_1A_0$	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	0	0	0	$A_3\overline{A}_2\overline{A}_1\overline{A}_0$	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	1	$A_3\overline{A}_2\overline{A}_1A_0$	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
1	0	1	0	$A_3\overline{A}_2A_1\overline{A}_0$	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
1	0	1	1	$A_3\overline{A}_2A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1	1	0	0	$A_3A_2\overline{A}_1\overline{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	0	1	$A_3A_2\overline{A}_1A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	1	1	0	$A_3A_2A_1\overline{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	$A_3A_2A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Decoders – The 4-Bit decoder



- The 4-bit decoder is usually called a *4-line-to-16-line decoder*.
- The 74HC154 is an MSI decoder.
- Both chip select inputs must be LOW to enable the device, otherwise all the outputs are HIGH.

Decoders – The 4-Bit decoder



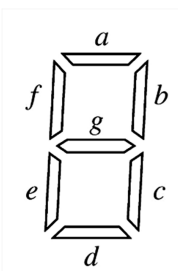
The chip select inputs may be used to expand the decoder to higher orders.

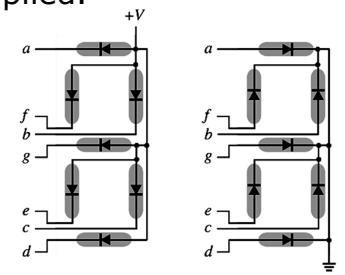
E.g. to decode a 5-bit number.

Decoders — BCD-to-7-Segment Decoders

LED Displays

- A 7-segment LED display consists of light-emitting diodes (LED).
- For common-cathode displays, the LED is turned on when a HIGH is applied.

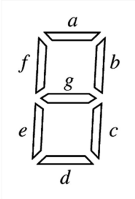




(a) Common-anode (b) Common-cathode

Decoders — BCD-to-7-Segment Decoders

LED Displays 



DECIMAL DIGIT	INPUTS D	C	B	A	SEGMENT OUTPUTS a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10	1	0	1	0	X	X	X	X	X	X	X
11	1	0	1	1	X	X	X	X	X	X	X
12	1	1	0	0	X	X	X	X	X	X	X
13	1	1	0	1	X	X	X	X	X	X	X
14	1	1	1	0	X	X	X	X	X	X	X
15	1	1	1	1	X	X	X	X	X	X	X

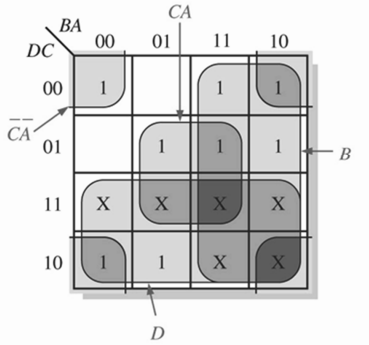
Decoders — BCD-to-7-Segment Decoders

Karnaugh map to simplify the segment-a logic.

INPUTS D	C	B	A	a
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

Standard SOP expression:

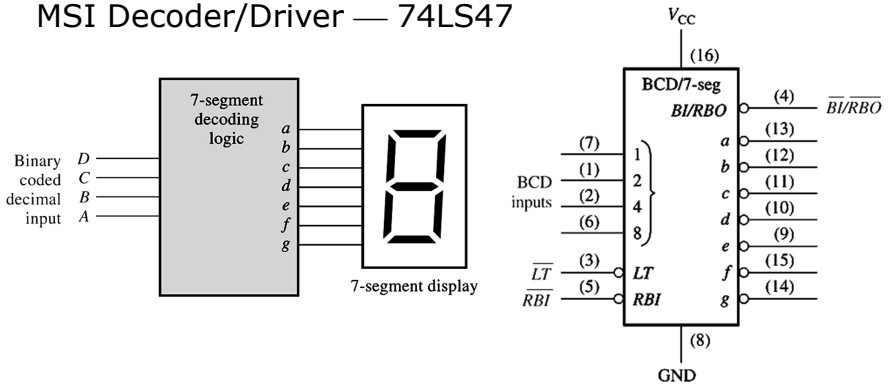
$\bar{D}\bar{C}\bar{B}\bar{A} + \bar{D}\bar{C}B\bar{A} + \bar{D}C\bar{B}\bar{A} + \bar{D}CB\bar{A} + \bar{D}CBA + D\bar{C}\bar{B}\bar{A} + D\bar{C}\bar{B}A$



Minimum SOP expression: $D + B + CA + \overline{C}\overline{A}$

Decoders — BCD-to-7-Segment Decoders

MSI Decoder/Driver — 74LS47



- LT is for lamp test.
- RBI and RBO are for zero suppression.