Lecture 6

of

EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Thursday, 25th October 2018

- **CMOS Fabrication**
  - connection between physical layout & structure
  - NMOS process & LOCOS
  - process steps in CMOS

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IC Fabrication & Layout Linkage

(why care about fabrication in layout design)

- In **integrated circuit** (**IC**) design, certain degree of knowledge about the **IC fabrication** will be helpful in creating the **physical layout**:
  - understand the **device structures** resulting from the **physical layout design** (i.e. knowing what will get, especially by visualising the 2-D or 3D structure)
  - understand better the **layout design rules** (from fabrication constraints)
  - avoid certain pitfalls in the circuits while designing the **physical layout**
  - obtain somewhat better device and circuit performance with optimised **IC layout**

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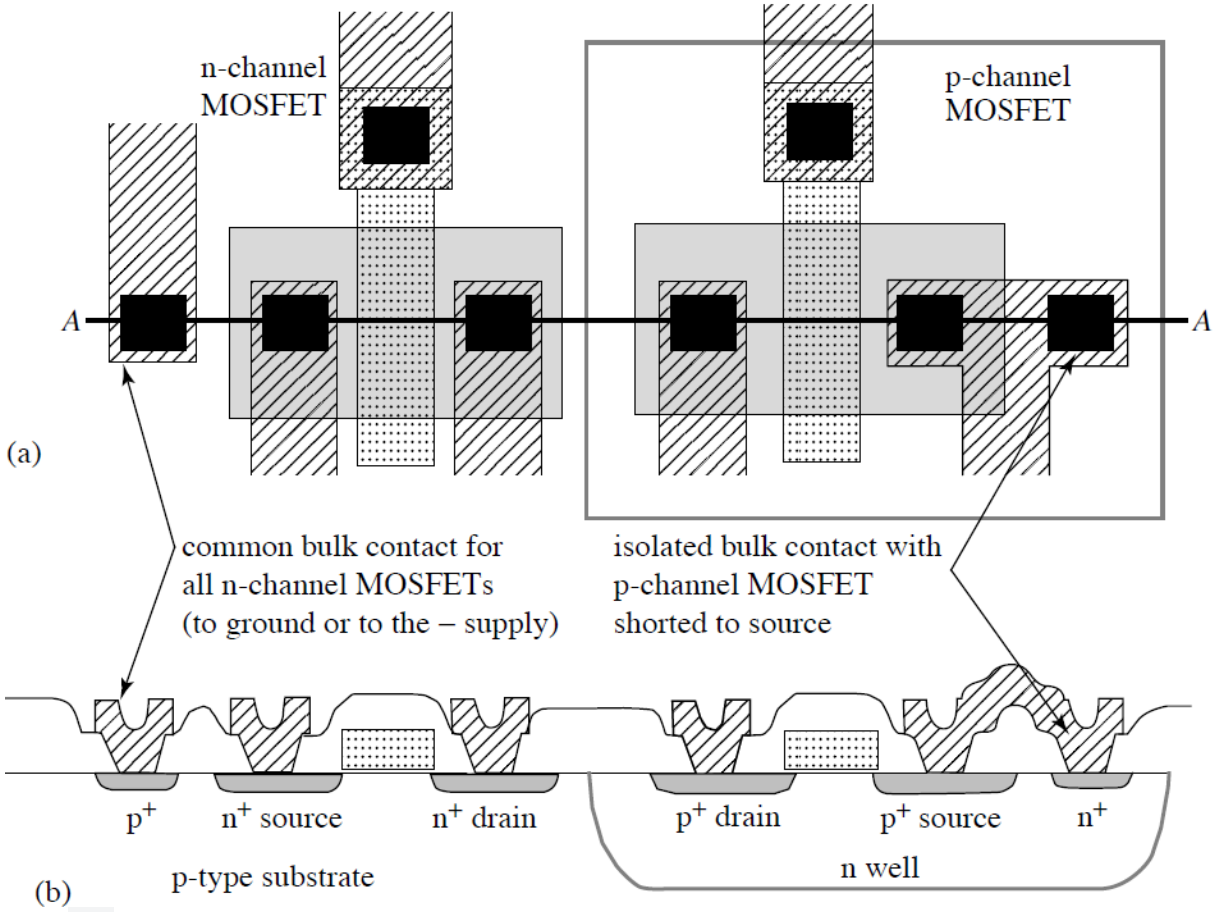
IC Fabrication & Layout Linkage

(CMOS transistors – nMOS & pMOS)



- In studying EEE201, you should be able to draw the **transistor schematic circuit** from the **IC layout** (a) & sketch the corresponding cross-sectional structure (b).

From: Roger T. Howe & Charles G. Sodini, *Microelectronics: An Integrated Approach*, © 1997 Prentice-Hall, USA.

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MOSFET

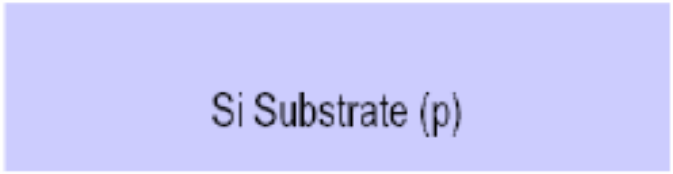
– fabrication & layout

(material originally developed by Professor Cezhou Zhao)

OUTLINE (fabrication & layout)

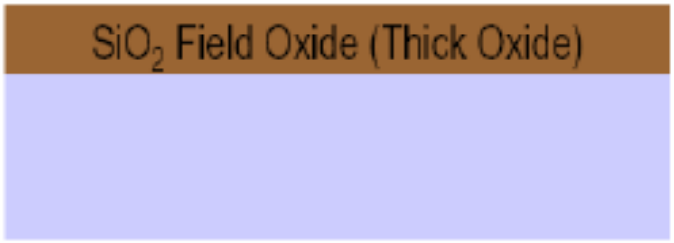
- Process Flow Example #1
  - Etched field oxide isolation
- Process Flow Example #2
  - LOCOS isolation
- Process Flow Example #3
  - CMOS n-Well process

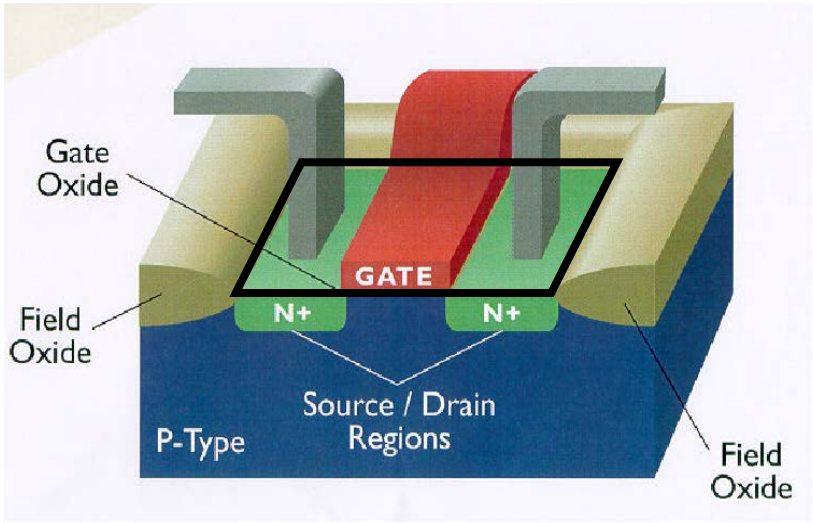
Process Flow Example #1



Oxidation (Lay

Oxide 1





Oxide etching (Patterning)

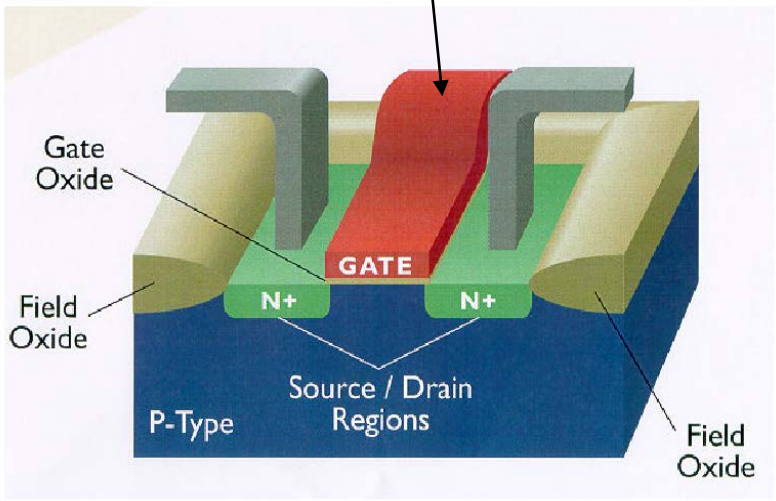
Mask 1

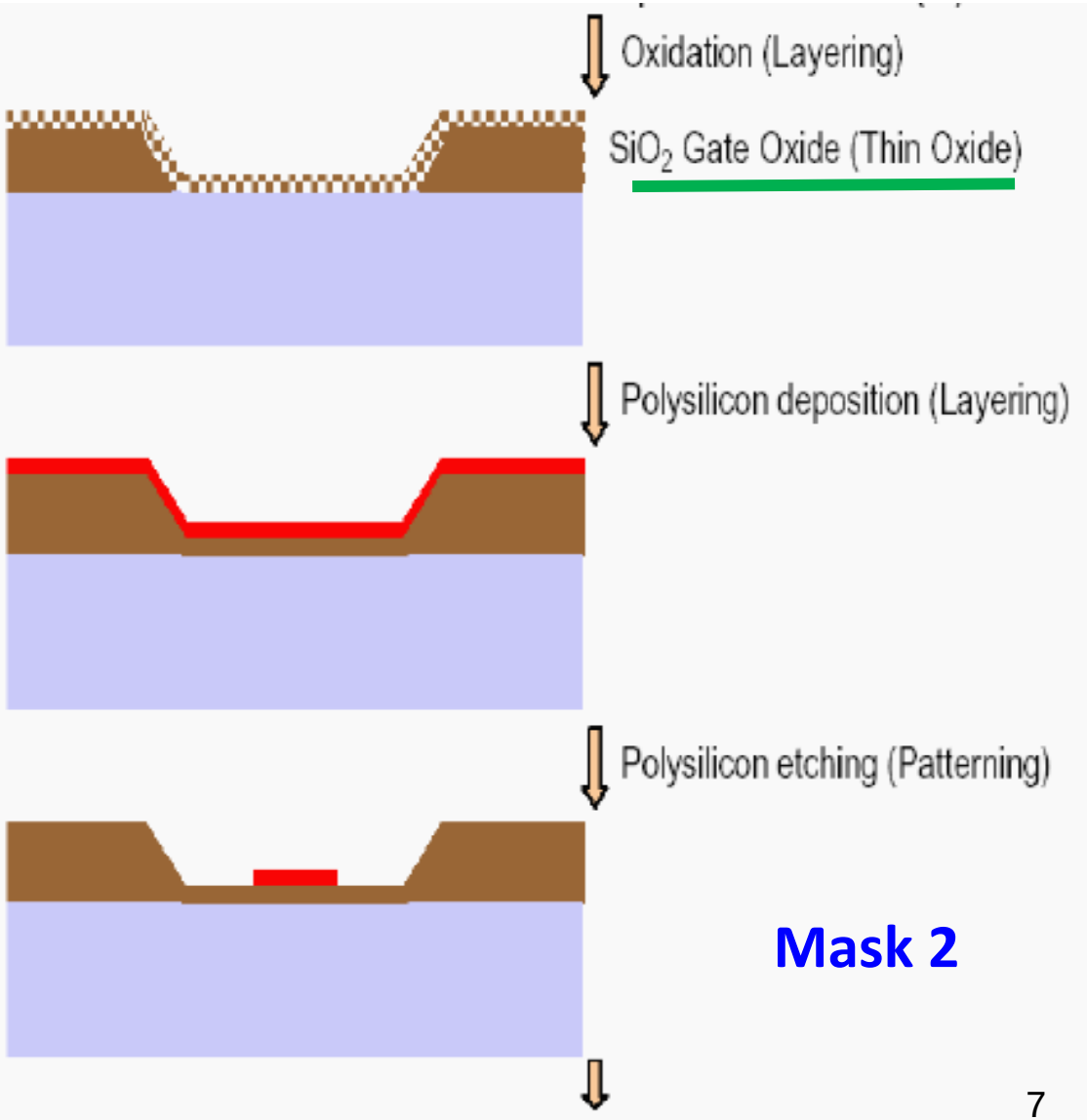
Mask 1: Active region

Etched field oxide isolation

Process Flow Example #1

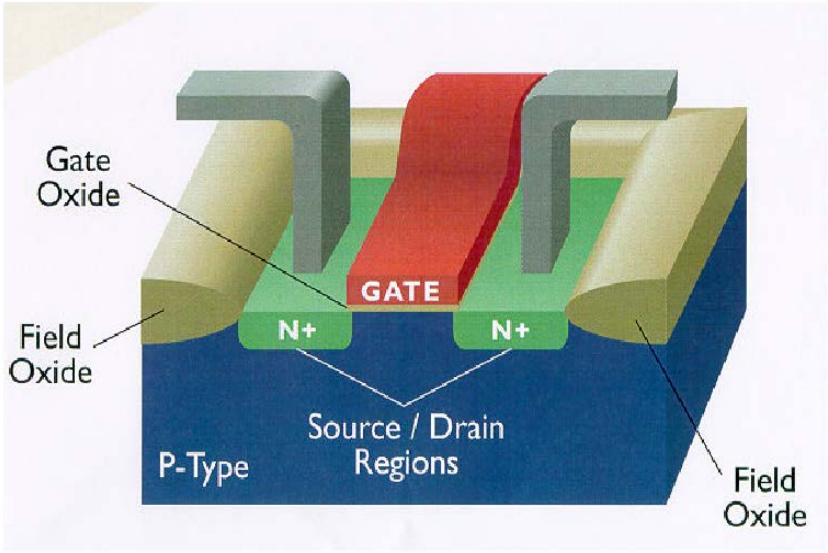
Mask 2: Gate

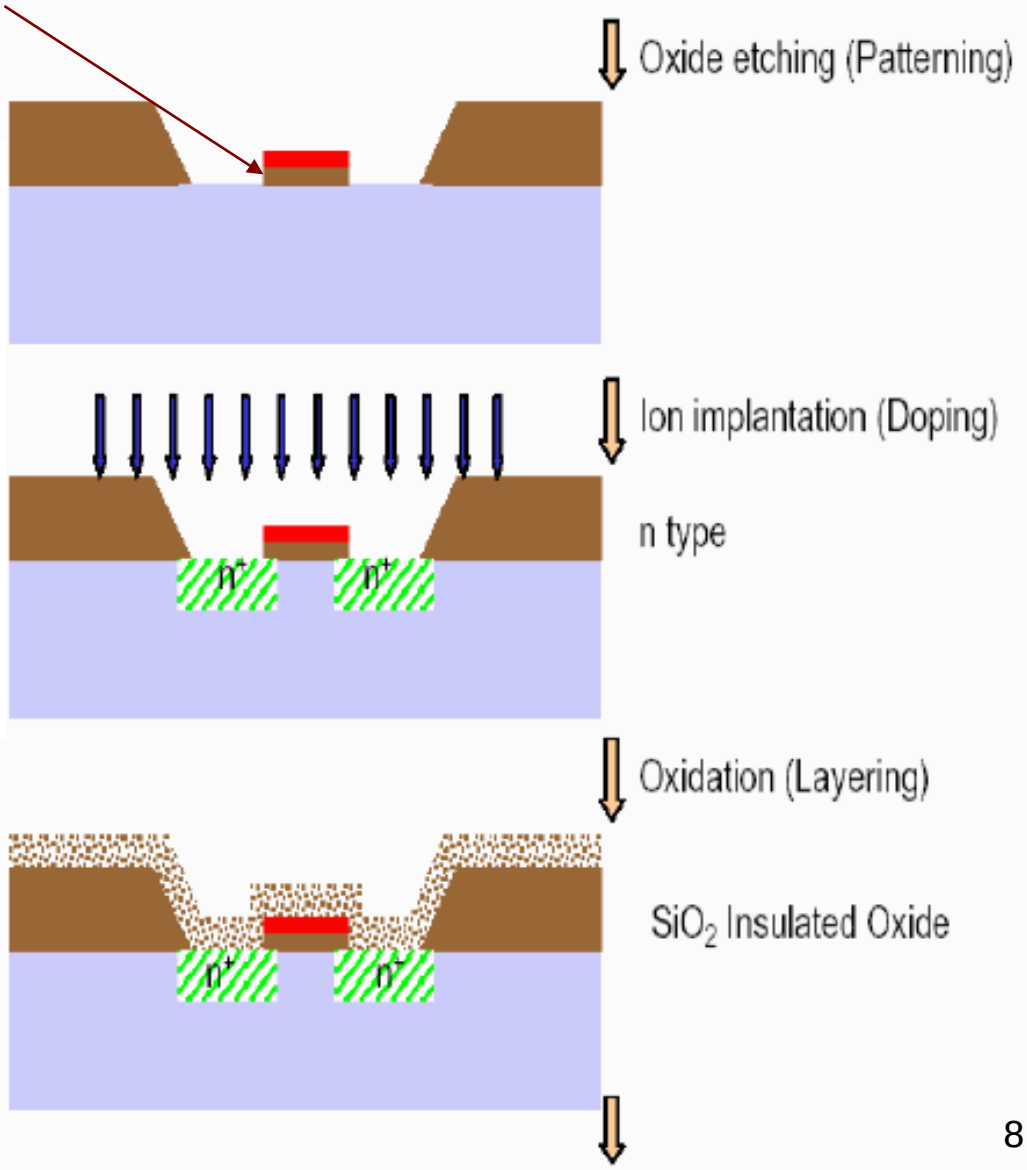




Process Flow Example #1

Keep gate oxide

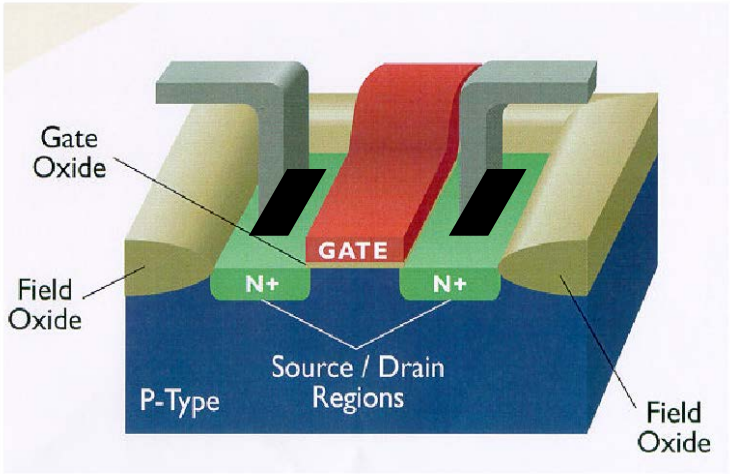




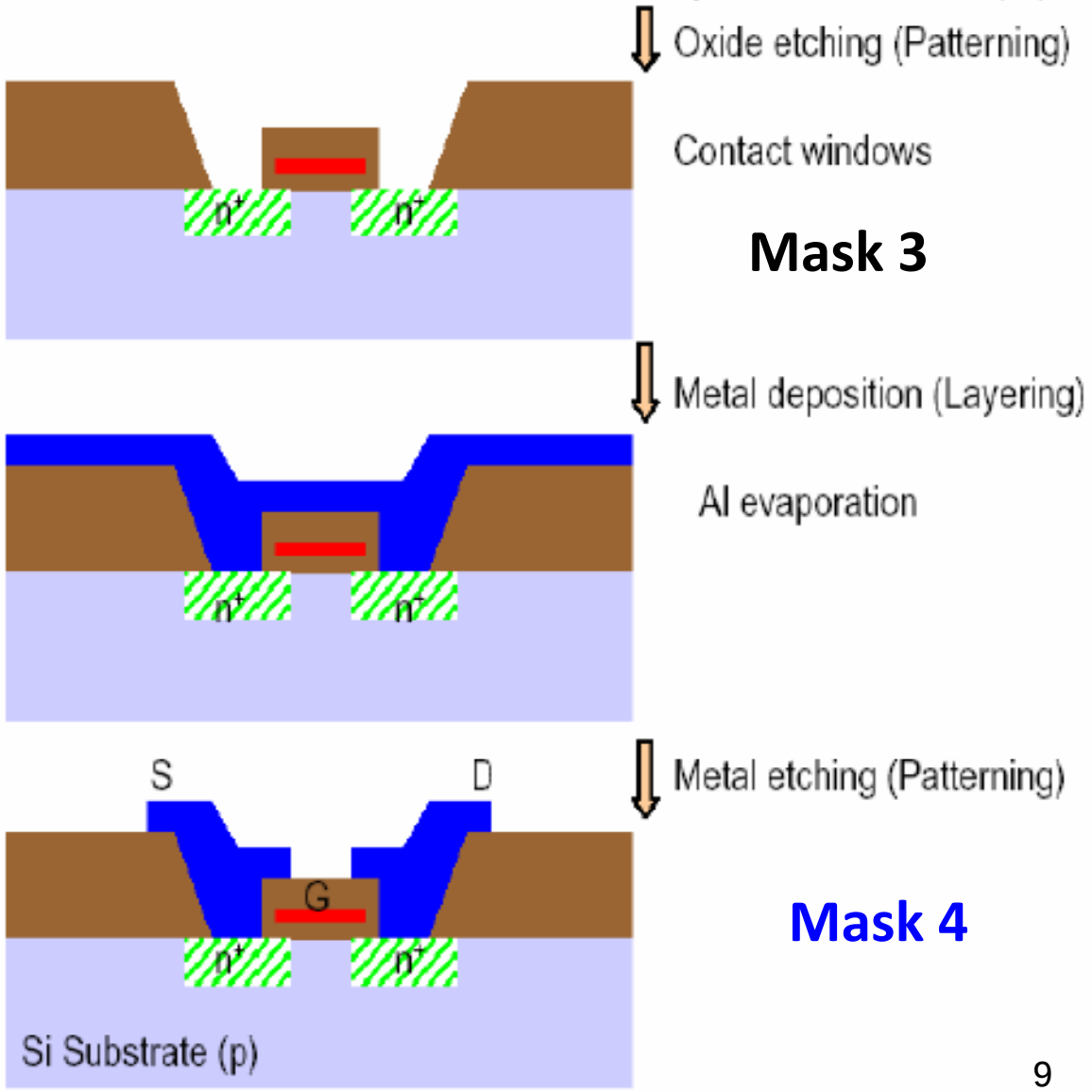
Gate becomes n+ type.

Process Flow Example #1

Mask 3: contacts

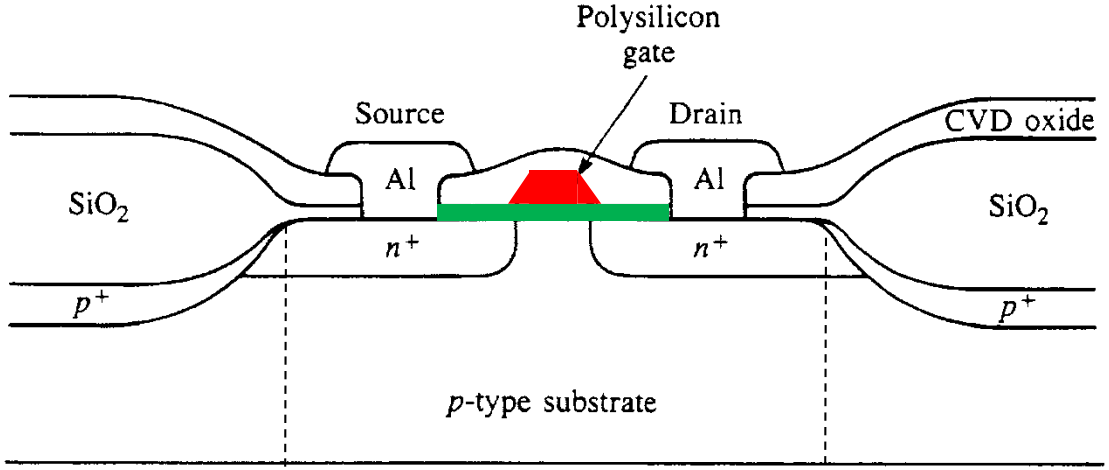


Mask 4: metal lines

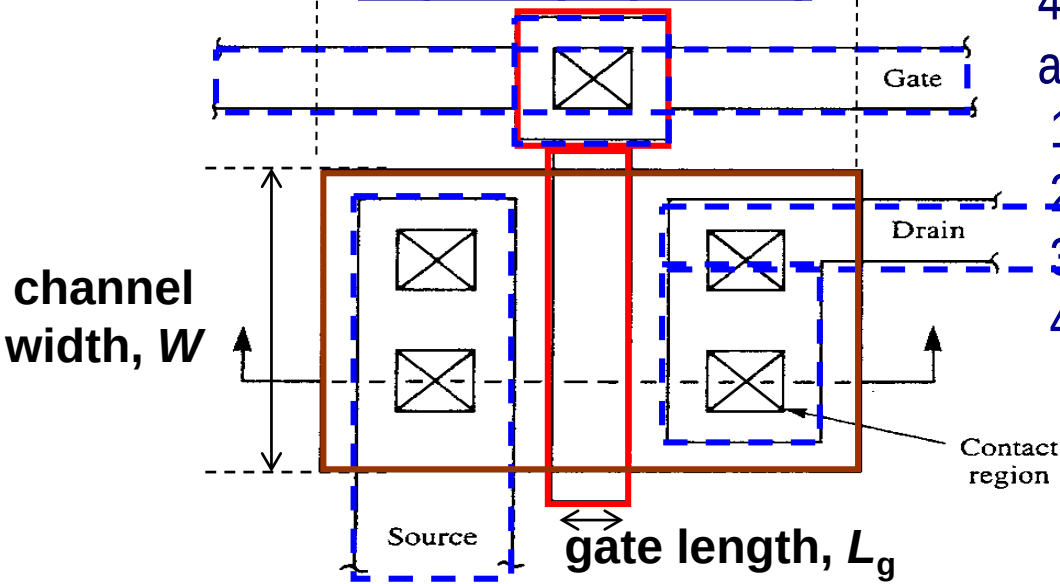


Process Flow Example #2: nMOSFET

Schematic Cross-Sectional View



Layout (Top View)



4 lithography steps are required:

1. active area
2. gate electrode
3. contacts
4. metal interconnects

Process Flow Example #2: nMOSFET

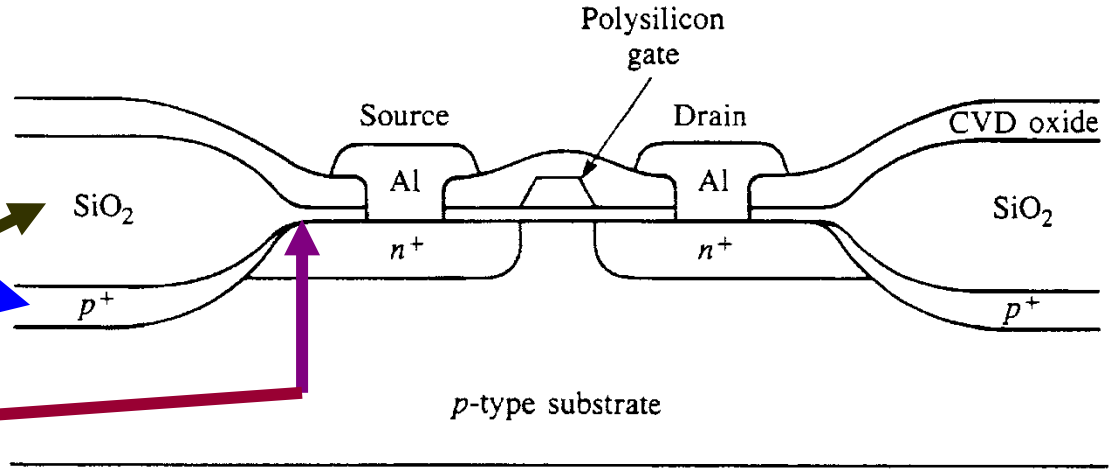
LOCOS ():

1. **Pad oxide**
2. **p+ doping**
3. **Field oxide**
4. **Bird's beak**

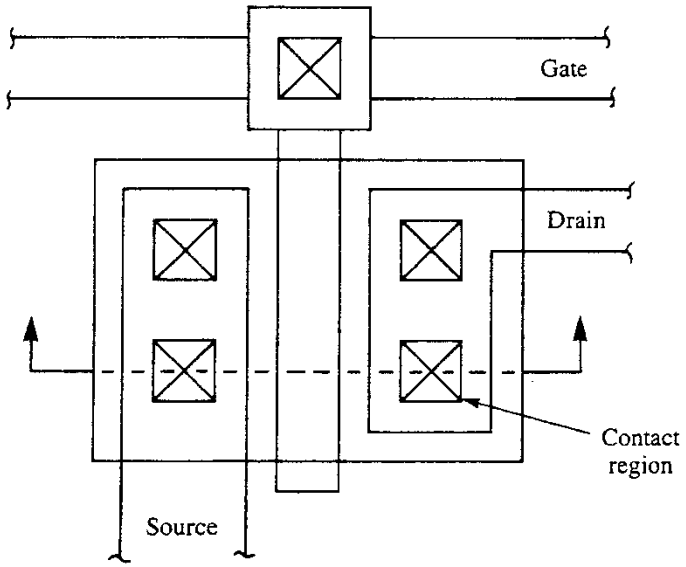
4 lithography steps are required:

1. active area
2. gate electrode
3. contacts
4. metal interconnects

Schematic Cross-Sectional View



Layout (Top View)



Local Oxidation of Silicon

Process Flow Example #2: nMOSFET

1) Thermal oxidation (~10 nm "pad oxide")

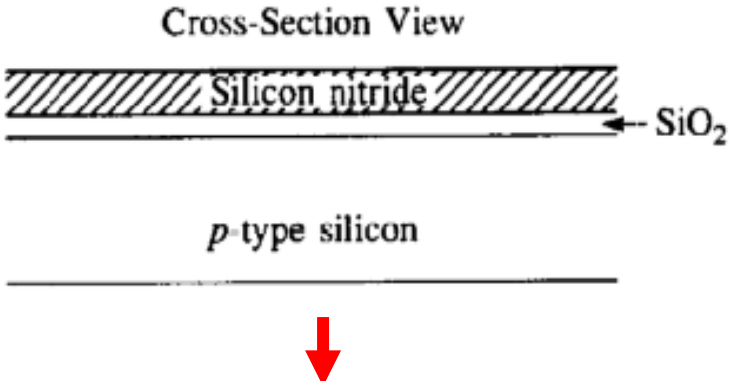
2) Silicon-nitride (Si_3N_4) deposition by CVD (~40nm)

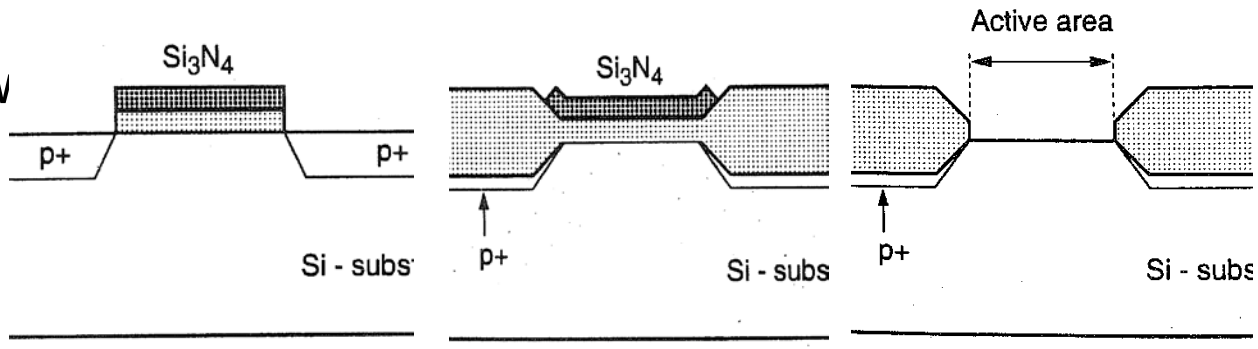
3) Active-area definition (lithography & etch)

4) Boron ion implantation ("channel stop" implan-,

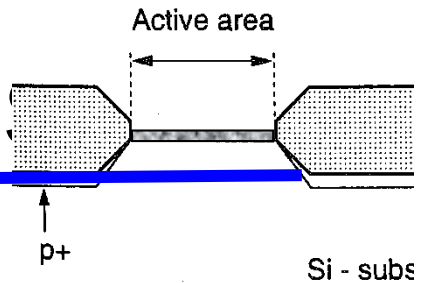
5) Thermal oxidation to grow oxide in "field regions"

6) Si_3N_4 & pad oxide removal

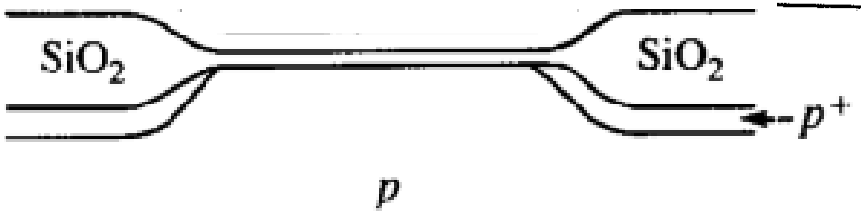




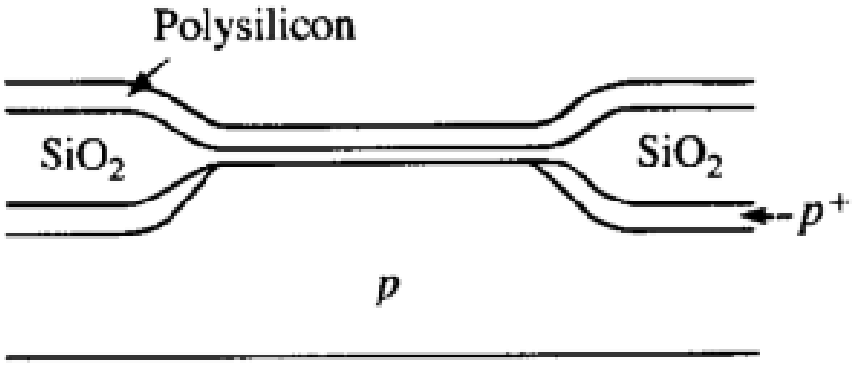
Process Flow Example #2: nMOS



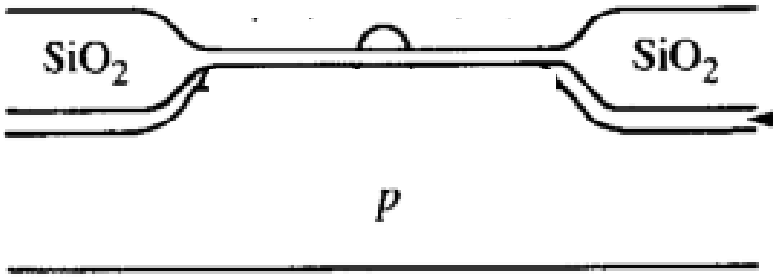
7) Thermal oxidation
("gate oxide")



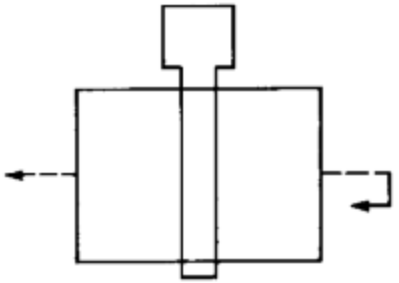
8) Poly-Si deposition by CVD



9) Poly-Si gate-electrode
patterning (litho. & etch)



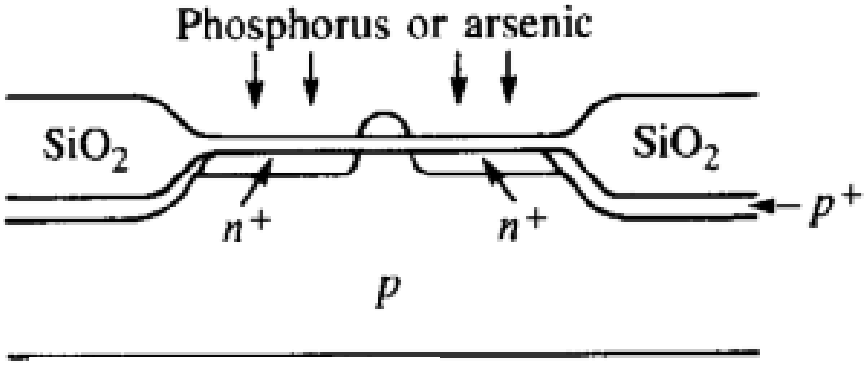
Top view of masks



mask2

Process Flow Example #2: nMOSFET

10) P or As ion implantation + annealing to form n+ source and n+ drain regions



Self-Aligned Technology: poly-Si gate

The poly-Si gate of a MOSFET is used as a mask for the doping of the source and drain regions.

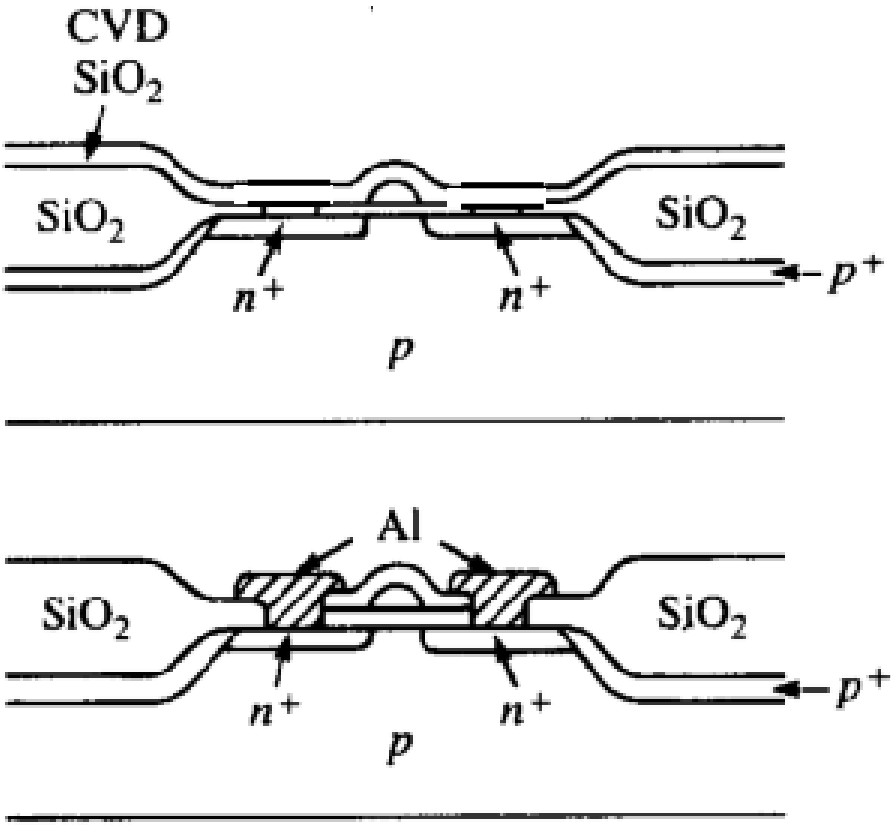
Process Flow Example #2: nMOSFET

11) SiO_2 CVD

12) Contact definition
(litho. & etch)

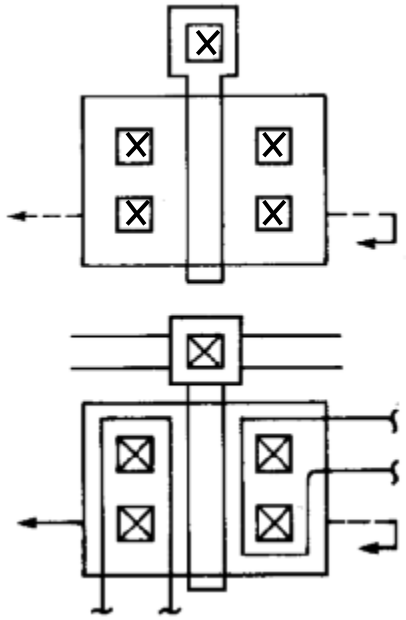
13) Al deposition
by sputtering

14) Al patterning
by litho. & etch
to form interconnects



Top view of masks

mask3



mask4

Complementary Metal Oxide Semiconductor

CMOS Process

CMOS n-Well process

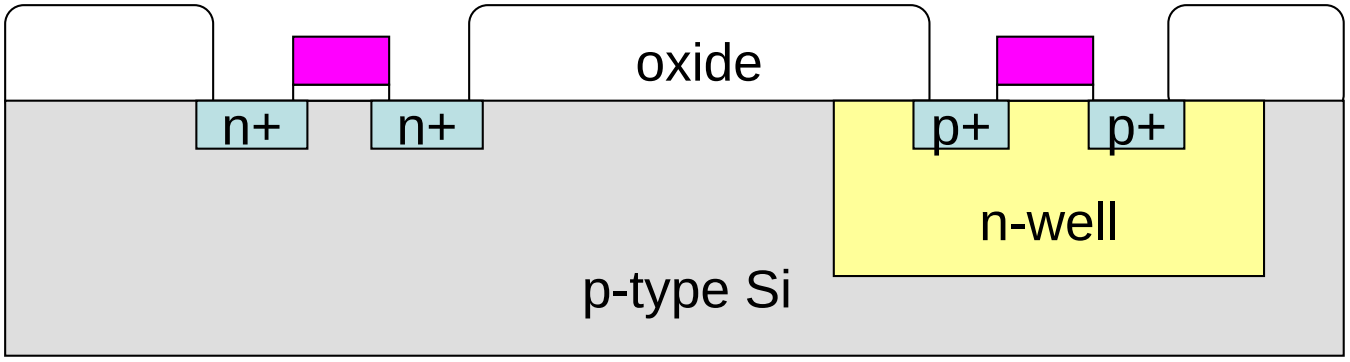
Additional Process Steps Required for CMOS

CMOS Technology

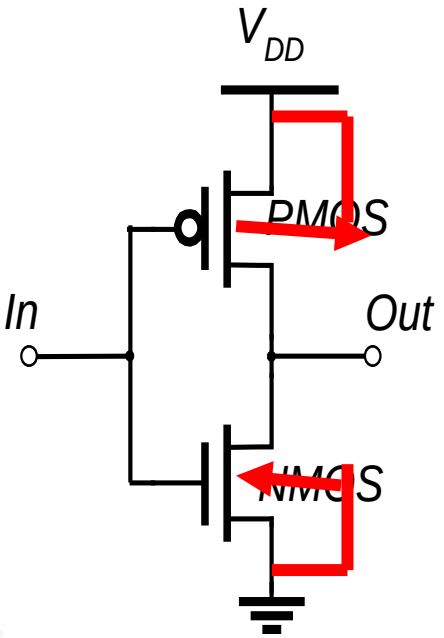
Challenge: Build both NMOS & PMOS transistors on a single silicon chip

- **NMOSFETs need a p-type substrate**
- **PMOSFETs need an n-type substrate**

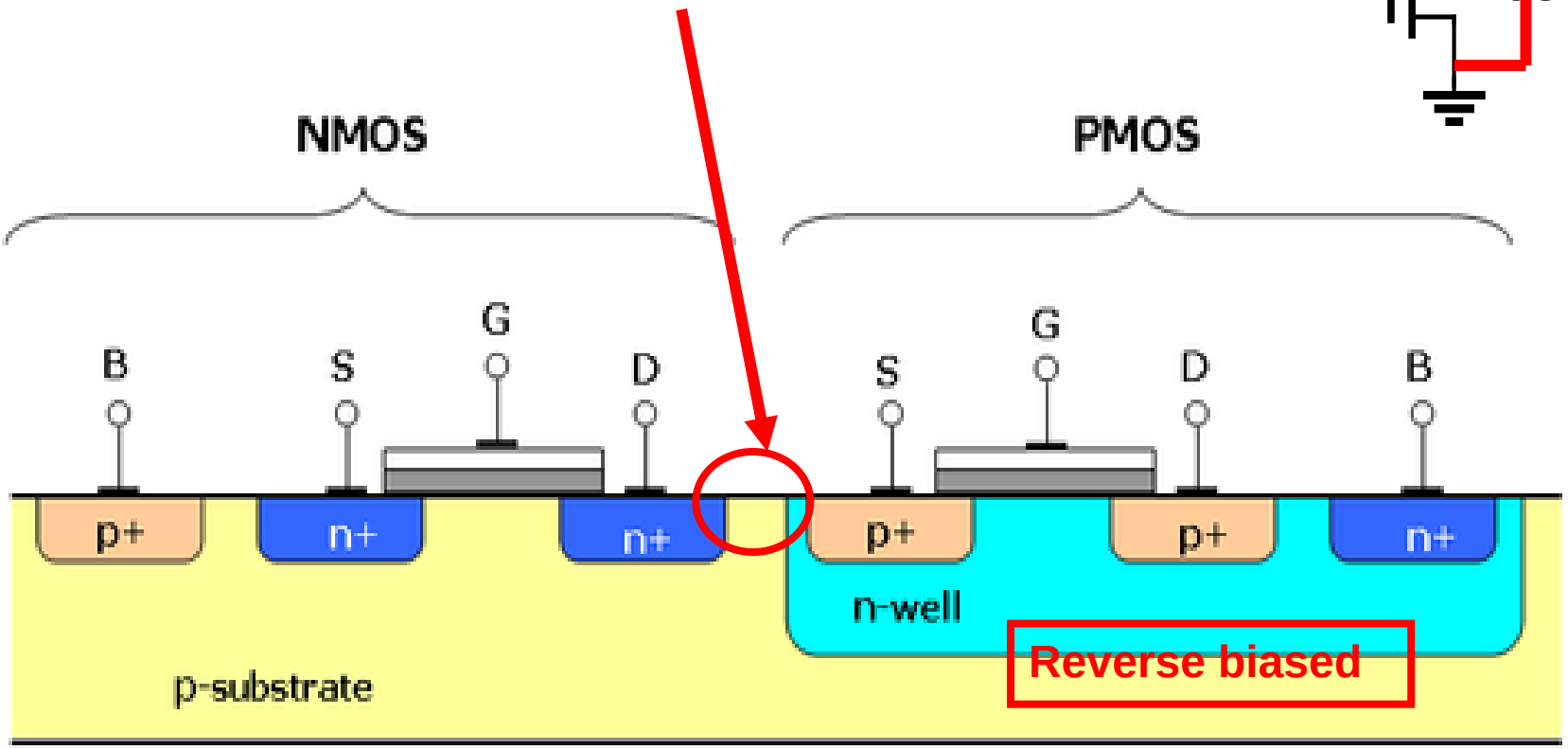
→ Requires extra process steps!



CMOS basic structure

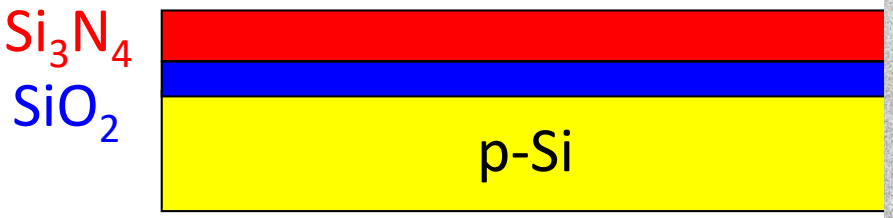


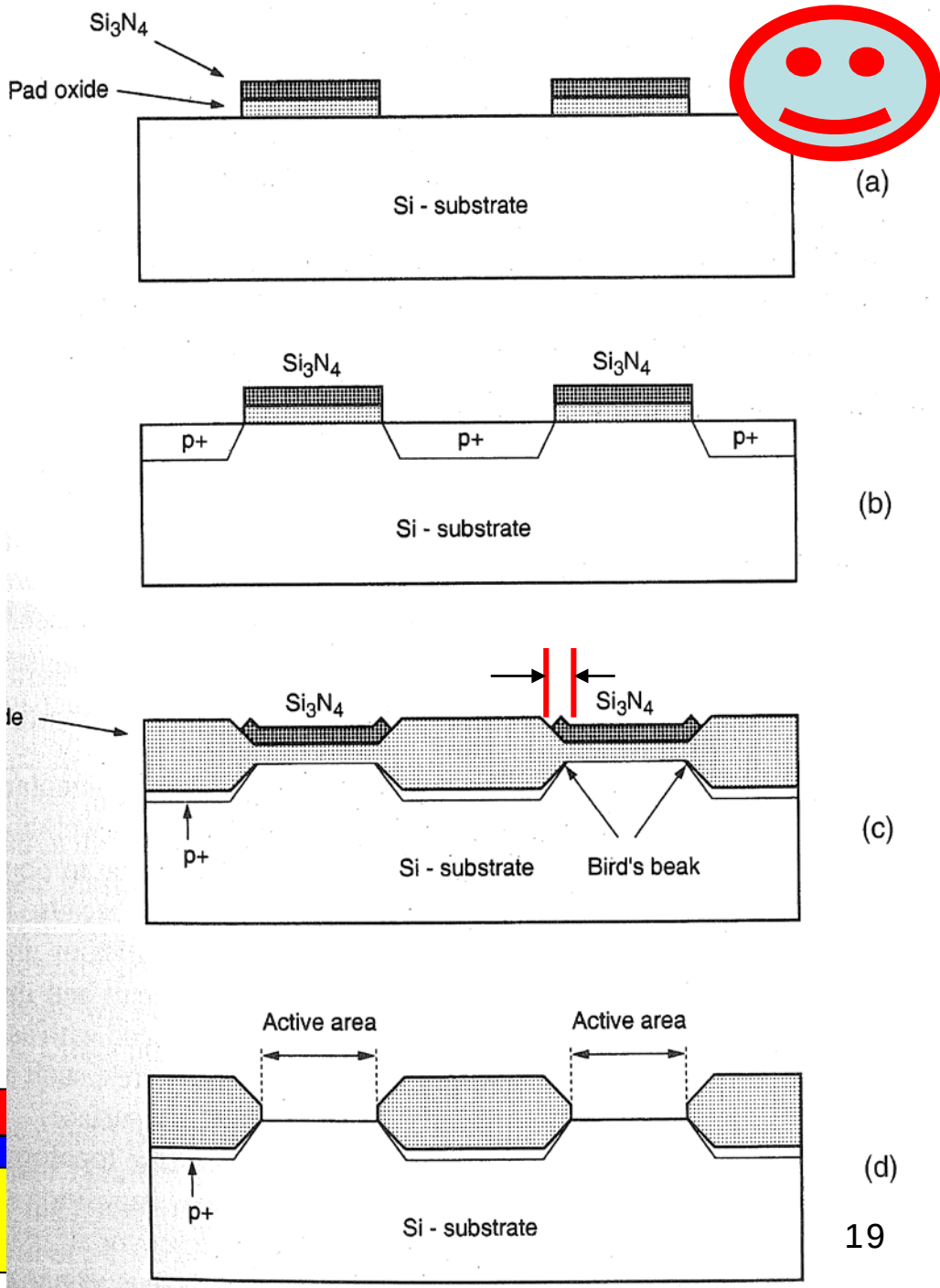
Field oxide (isolation): the lateral insulation between transistors.
($V_T\uparrow$ **to stop n^+/n-well channel**)



LOCOS

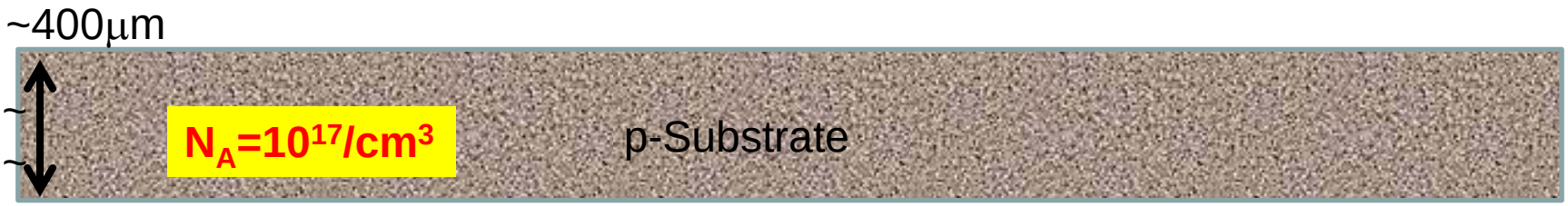
1. Pad SiO_2 is used to protect the Si surface from stress caused by Si_3N_4.
2. p+ doping: n channel-stop implants.
3. Field oxide (isolation): the lateral insulation between transistors.
4. Bird's beak region: a reduction of the active region.



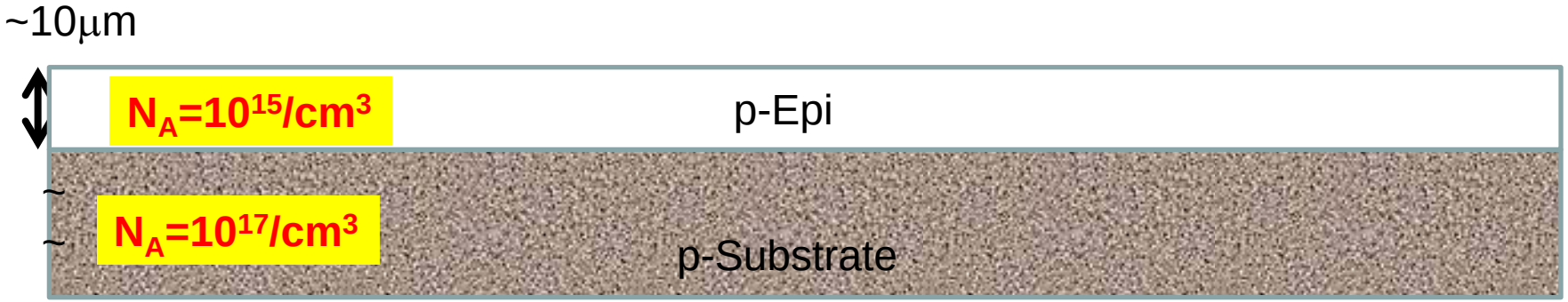


CMOS Fabrication

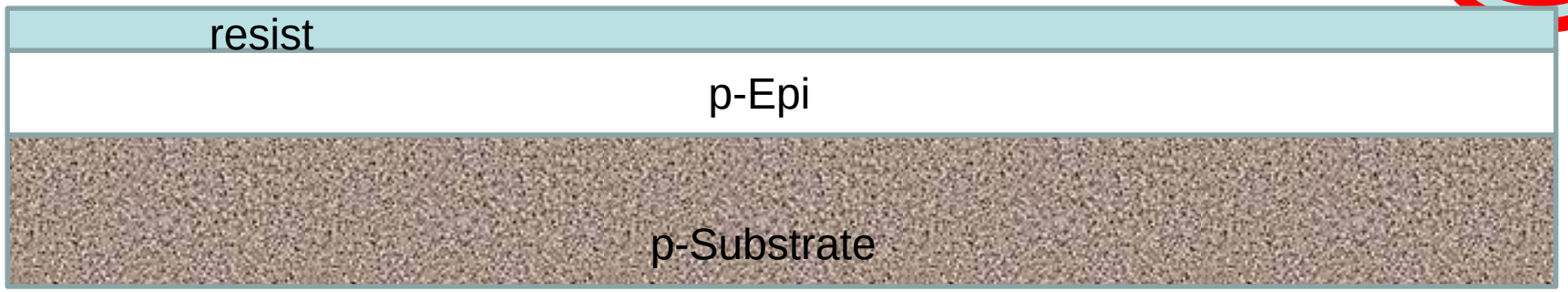
p-type start wafer



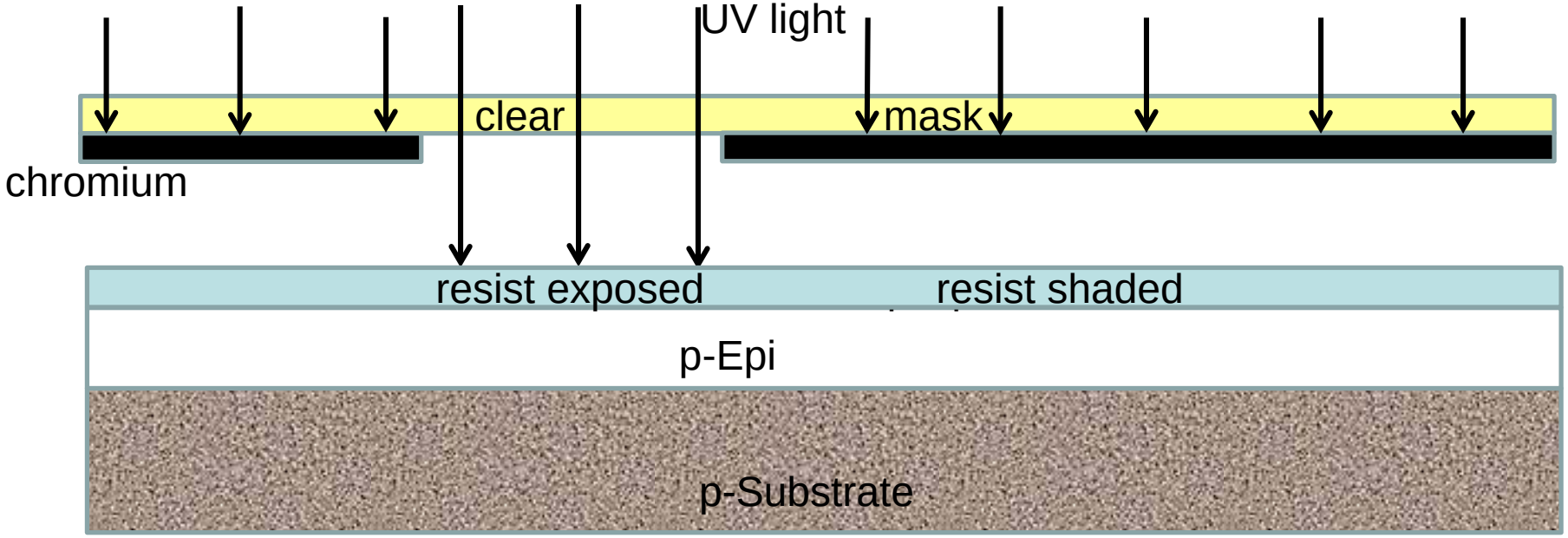
Grow p epitaxial layer



Spin Resist Coating

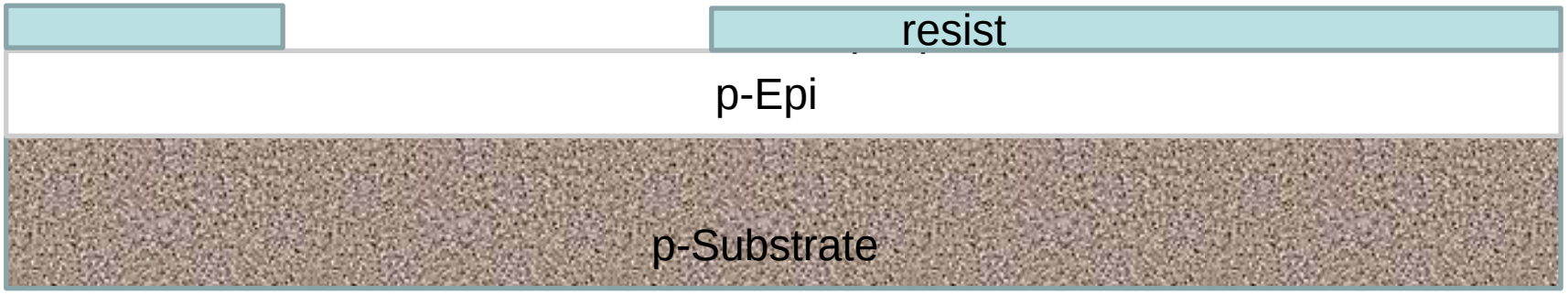


M1 Expose resist with n-well mask

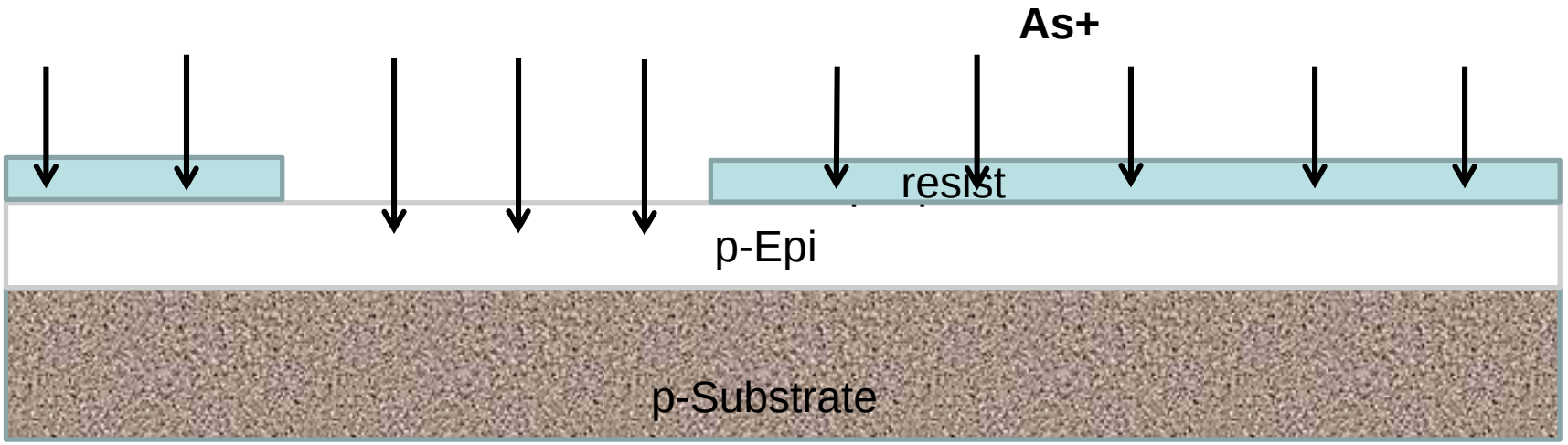


Mask1: n-Well

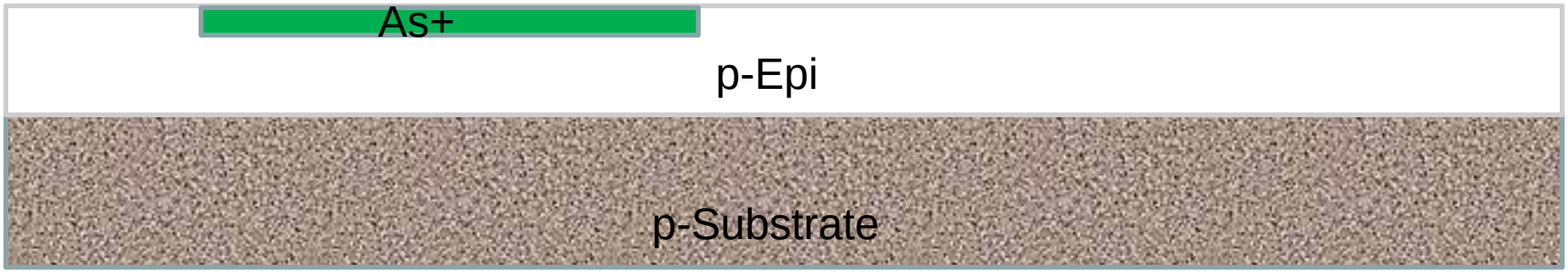
Develop resist



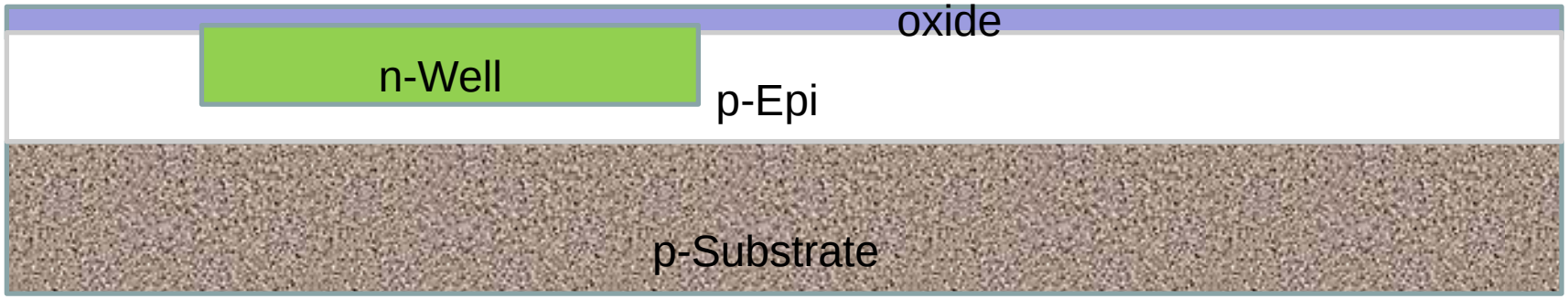
Implant n-type Well



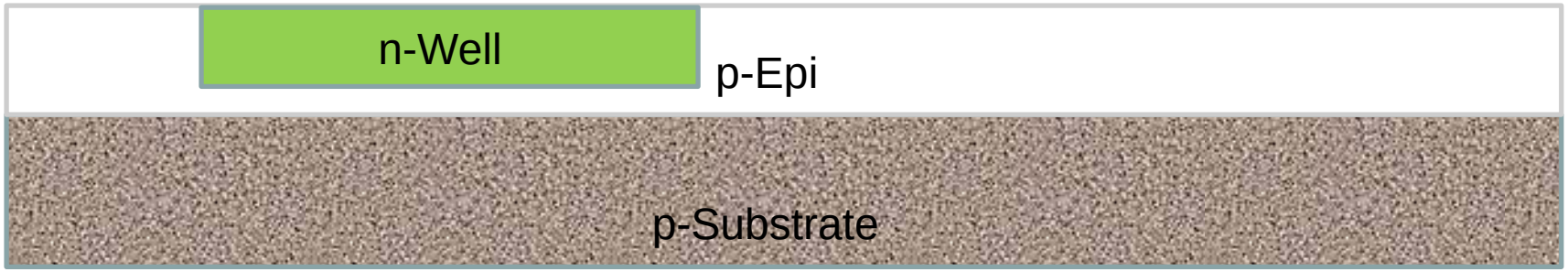
Remove resist



Anneal wafer – gives us new oxide layer and diffuses n-Well

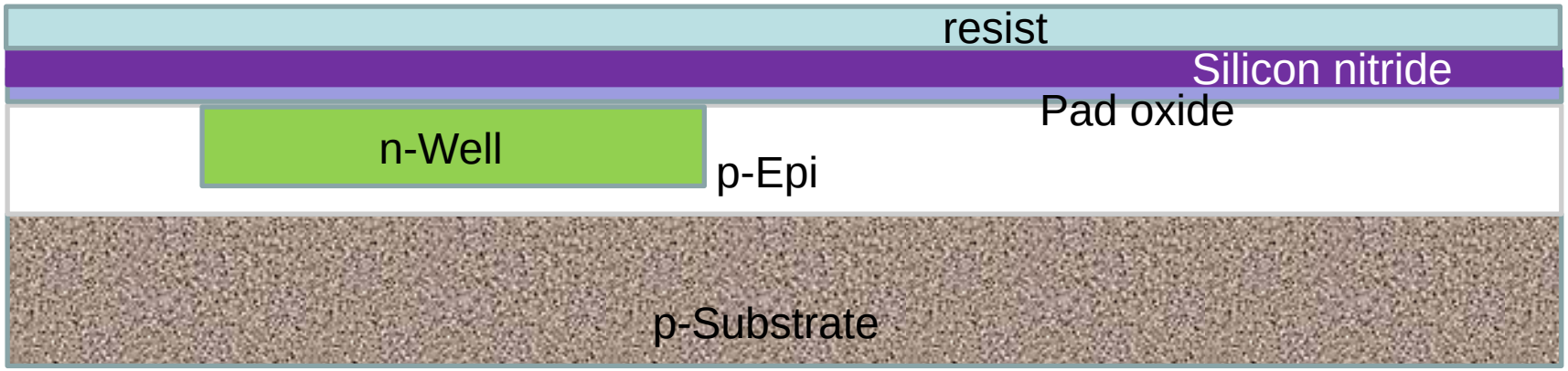


Remove oxide from anneal



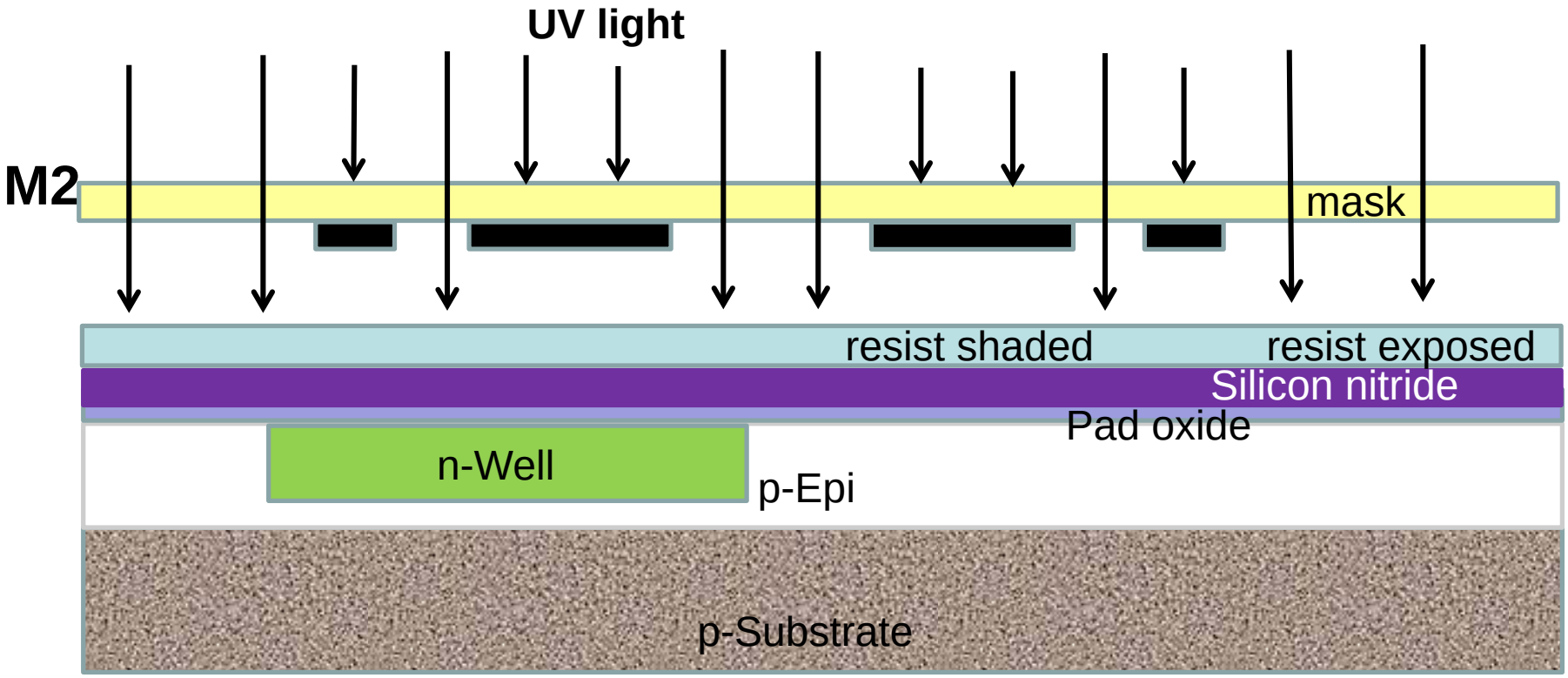
LOCOS: **Pad SiO_2 + Si_3N_4 + Resist, then M2 & p+ implantation**

Grow pad SiO_2, CVD Si_3N_4, and then Spin resist

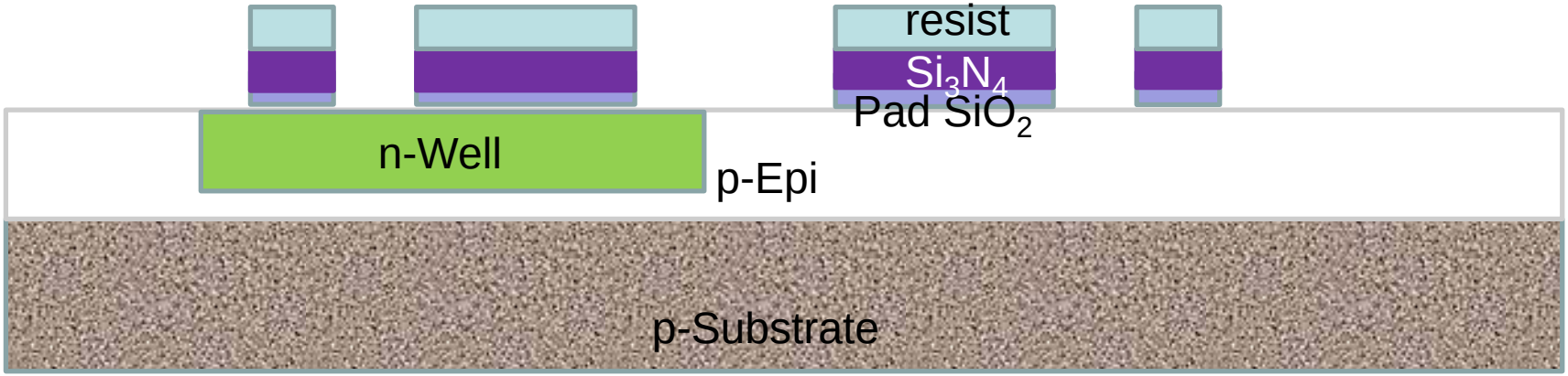


Mask2: active regions

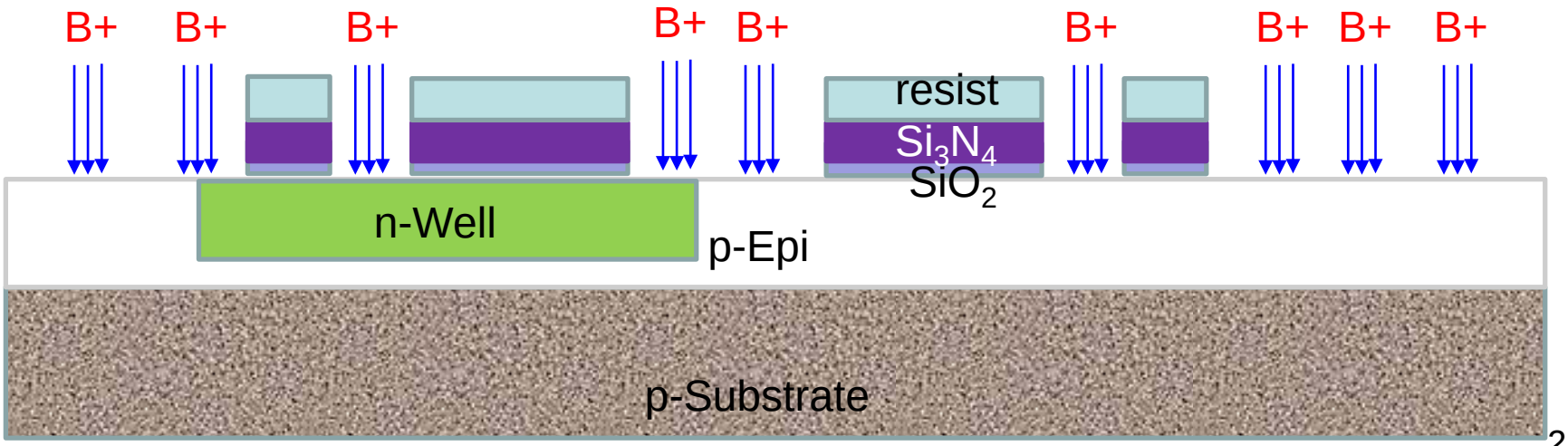
Expose resist with Active diffusion mask



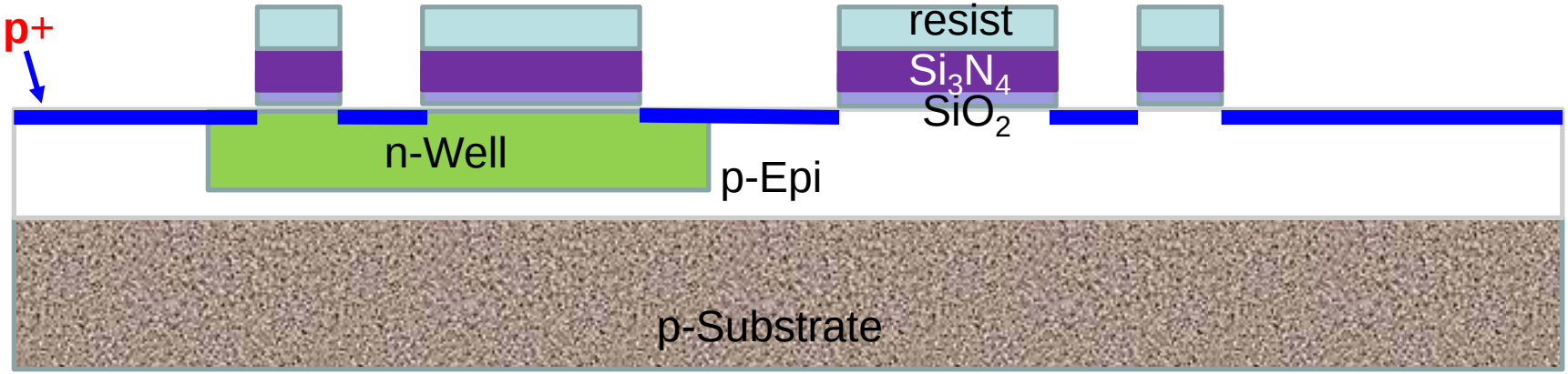
Develop resist and etch SiO_2 and Si_3N_4



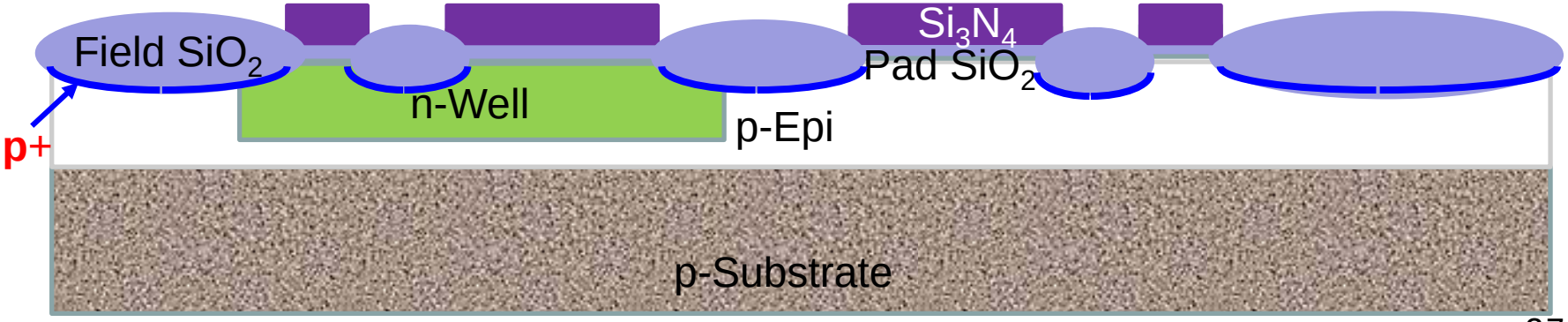
Channel stop implantation



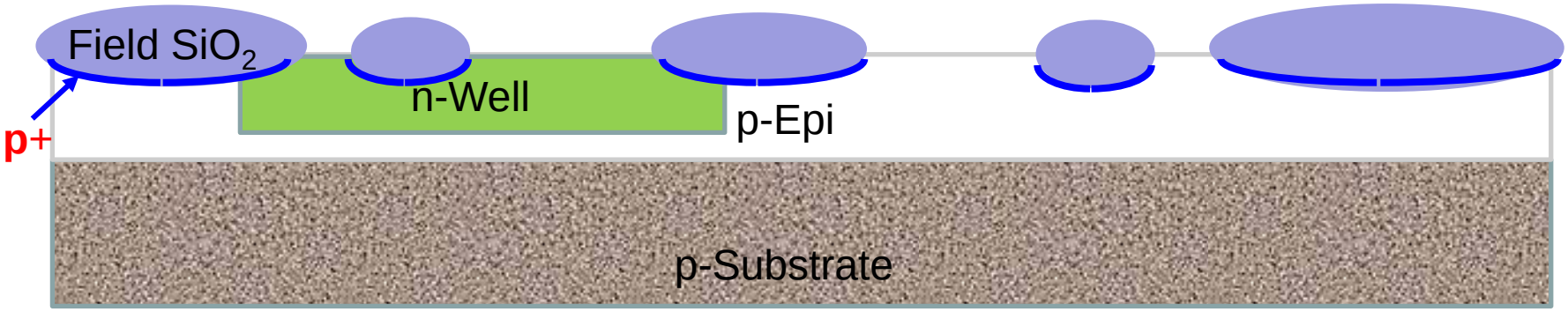
Channel stop implantation



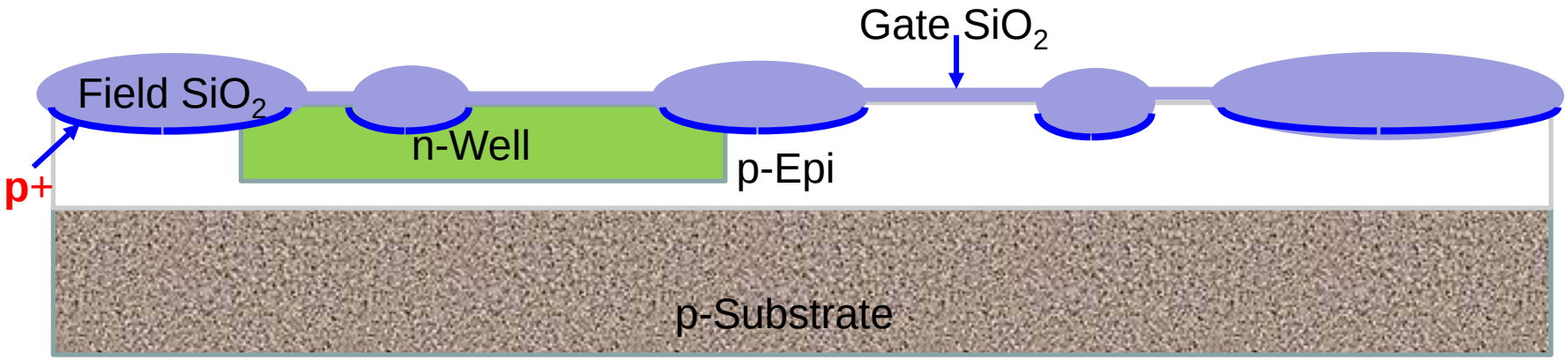
Resist is removed during growing field oxide on exposed surface



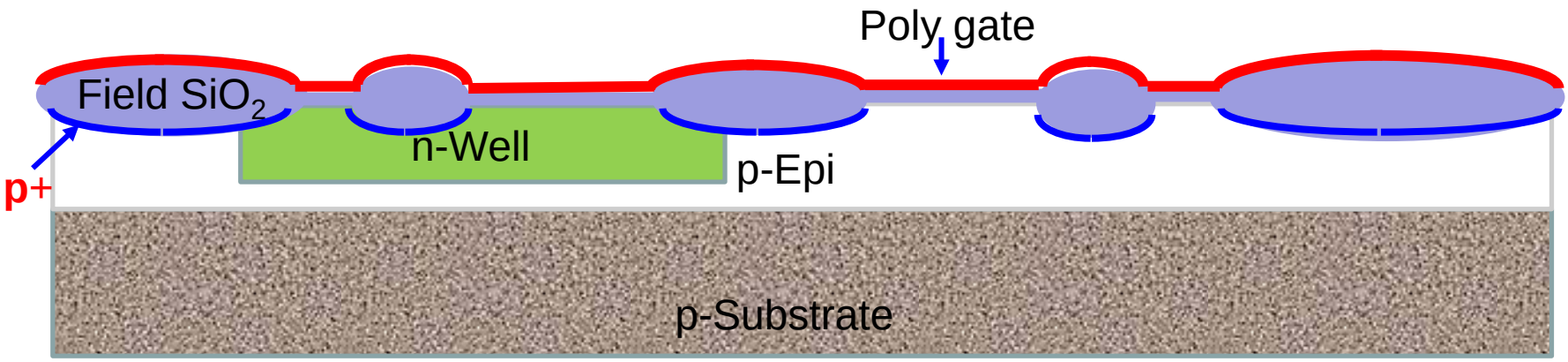
Remove pad SiO_2 and CVD Si_3N_4



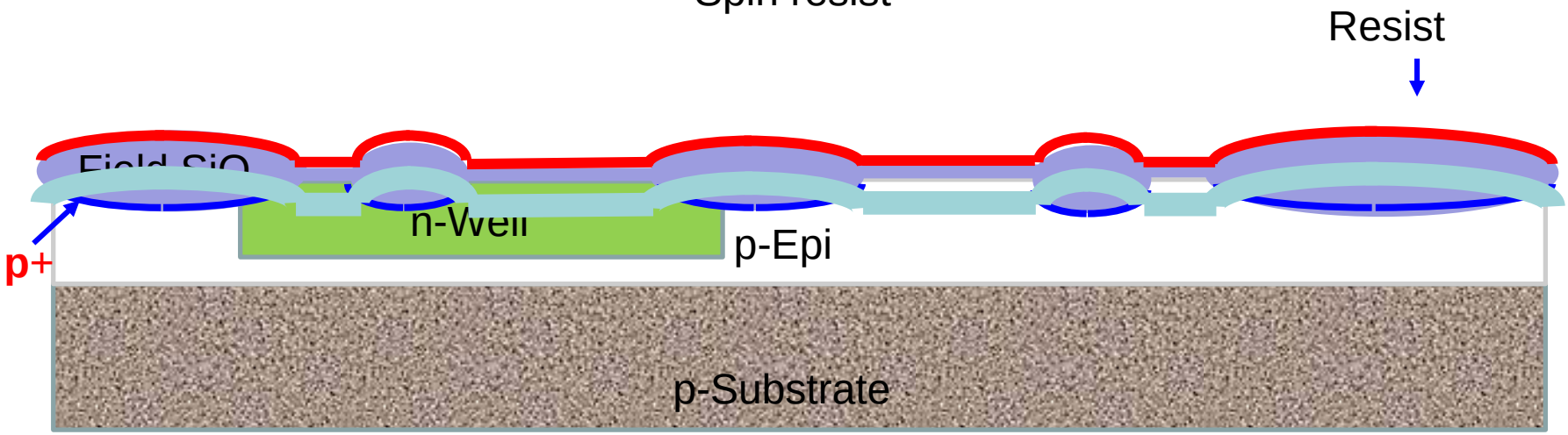
Grow thin gate oxide



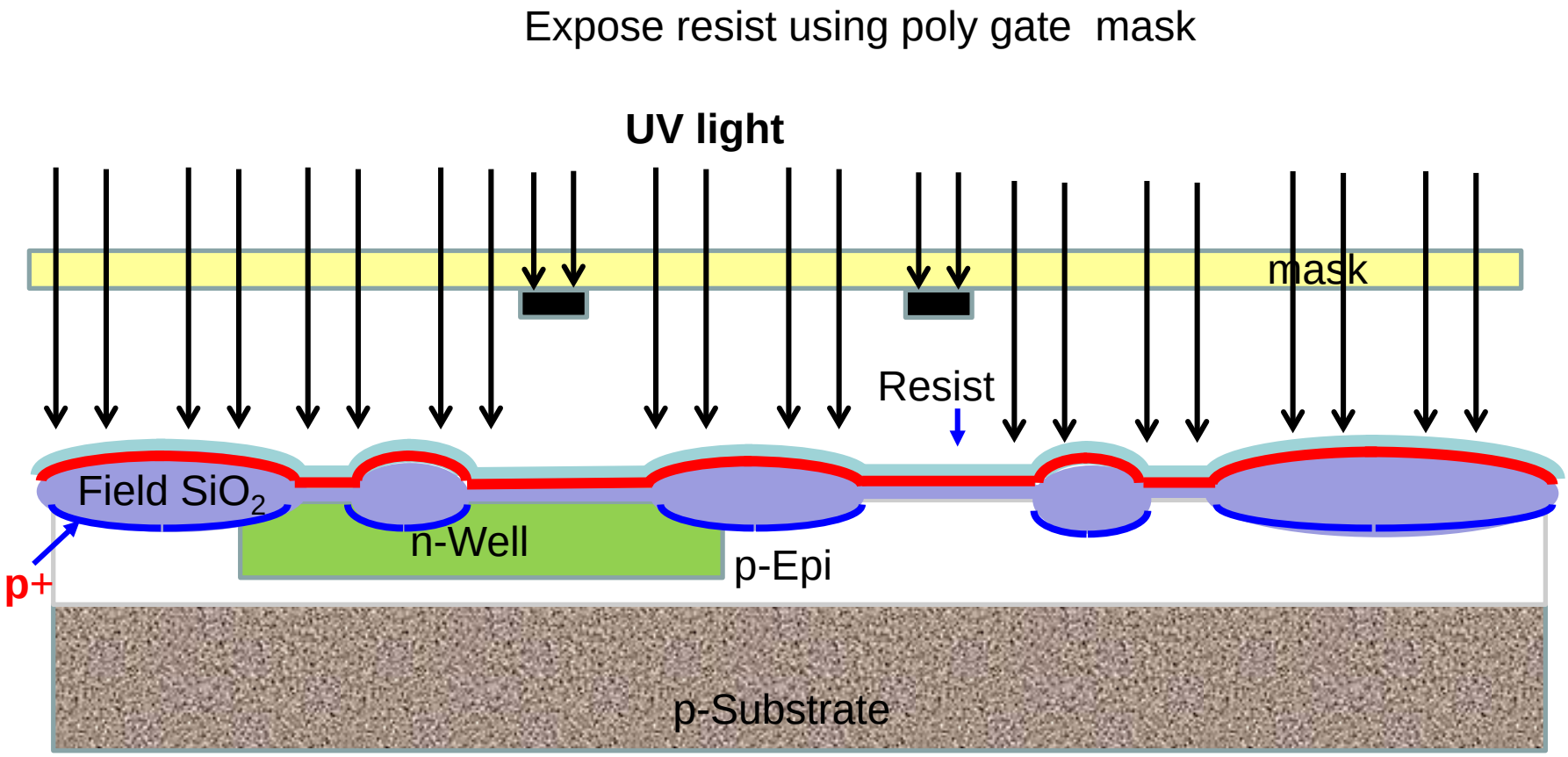
Deposit poly silicon using CVD over surface



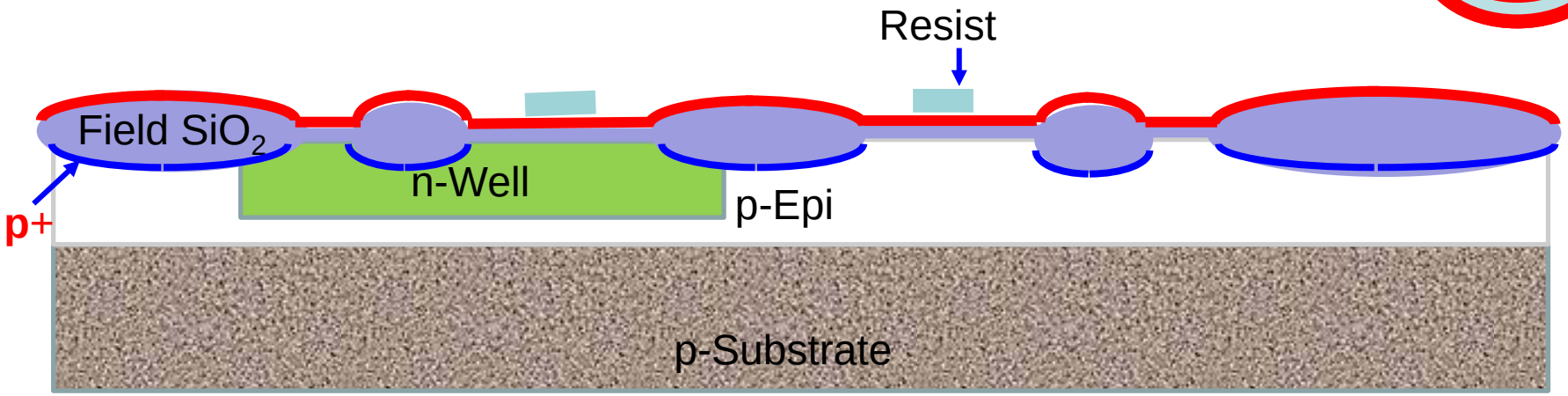
Spin resist



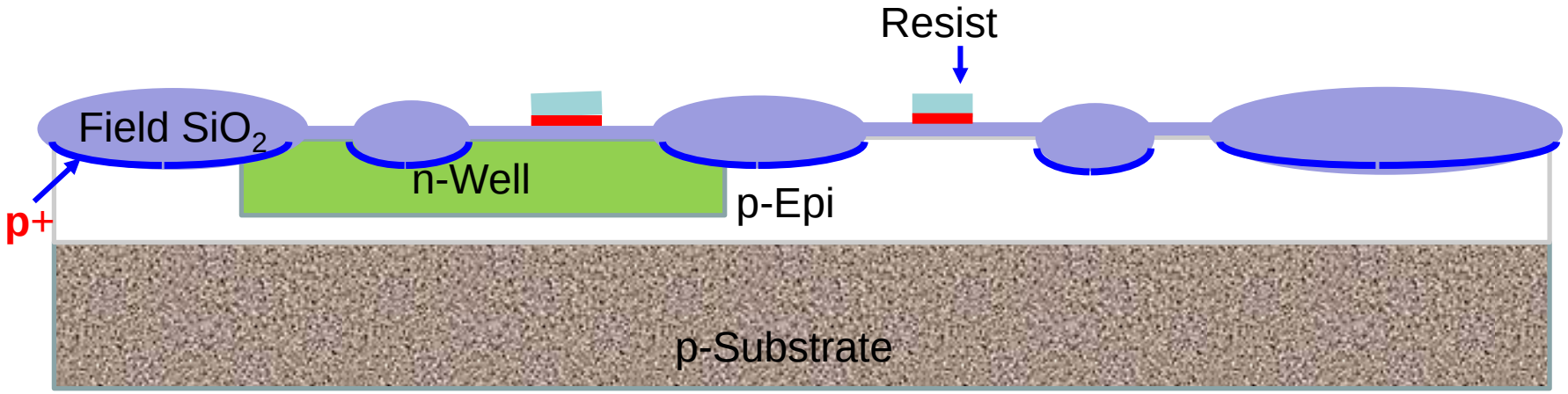
Mask3: poly gate



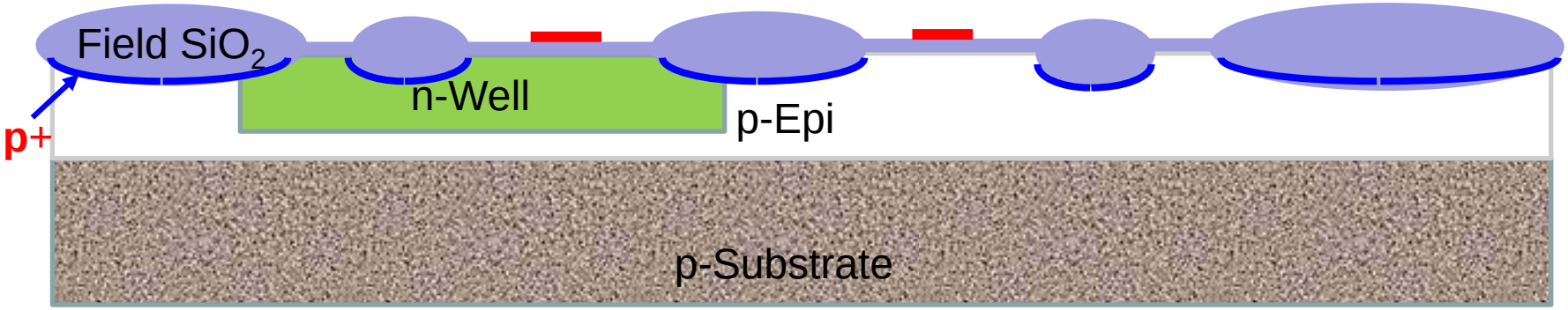
Develop resist



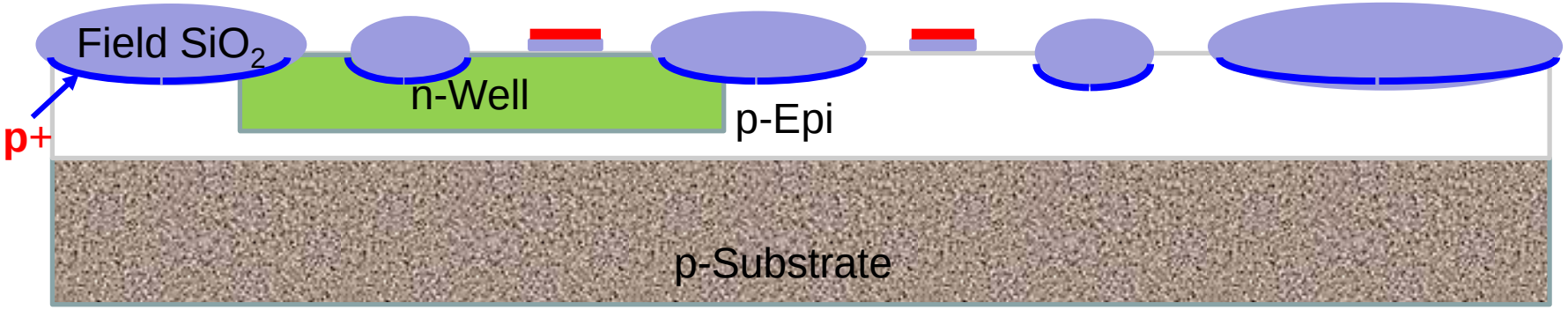
Etch poly silicon



Remove resist

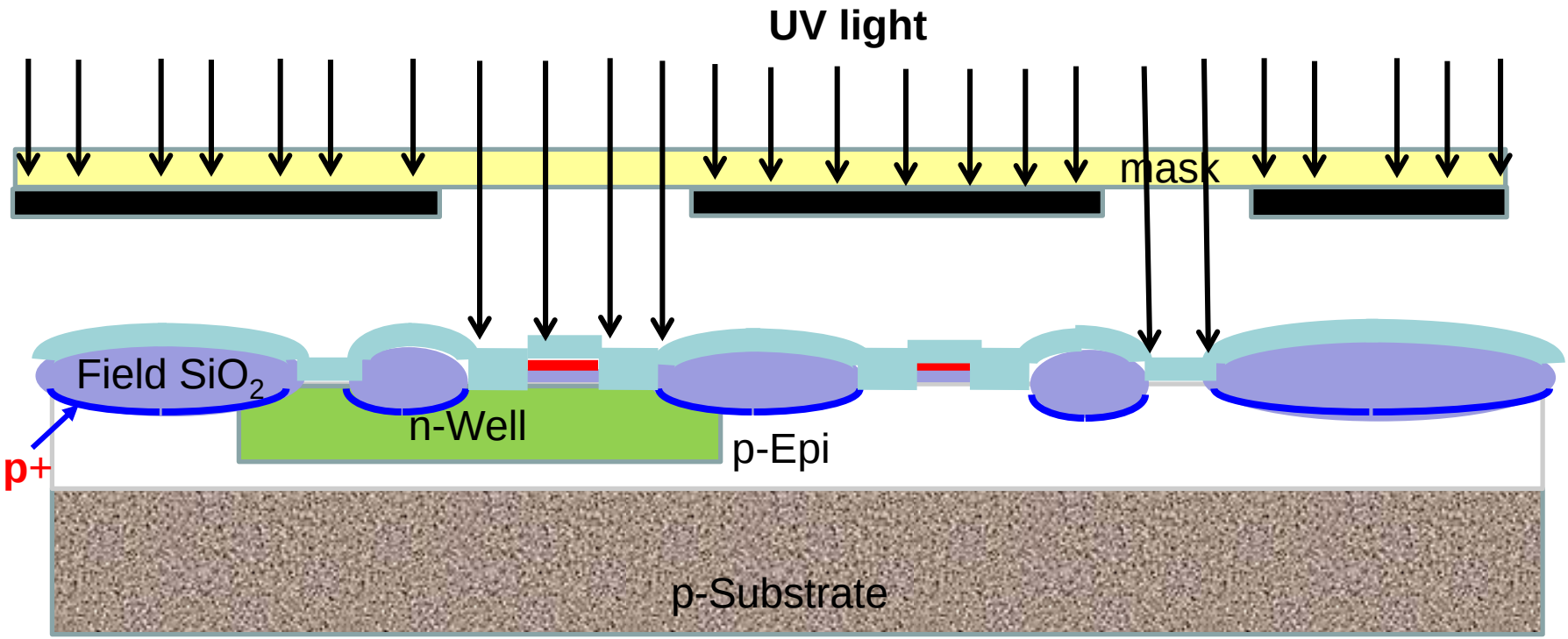


Remove thin gate oxide layer where exposed

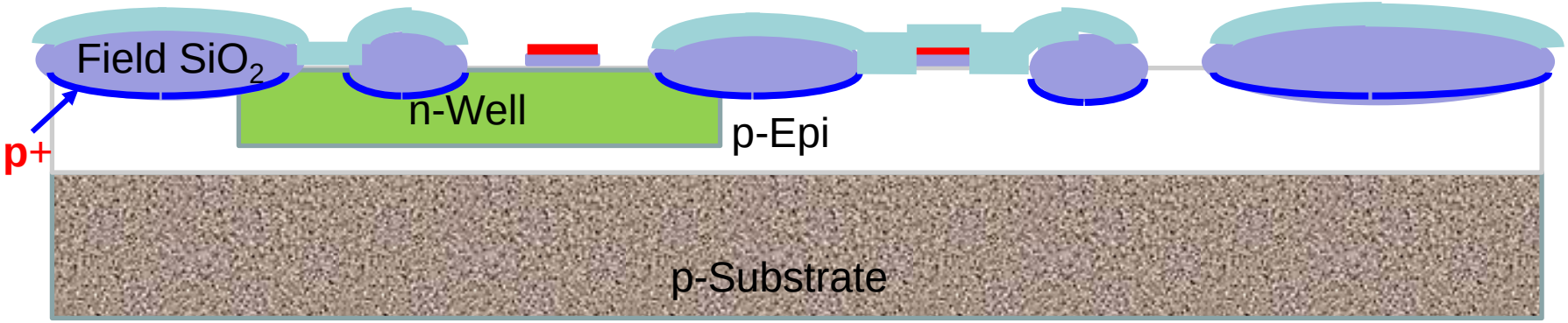


Mask4: p-select

Spin resist and Expose resist using p-select mask

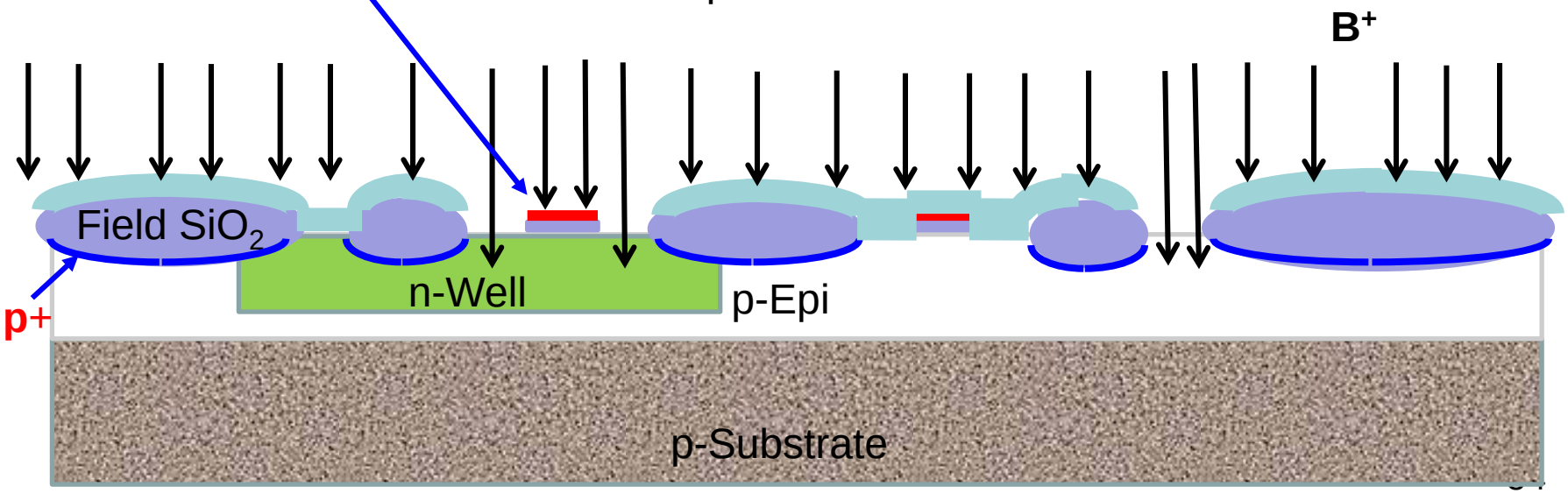


Develop resist

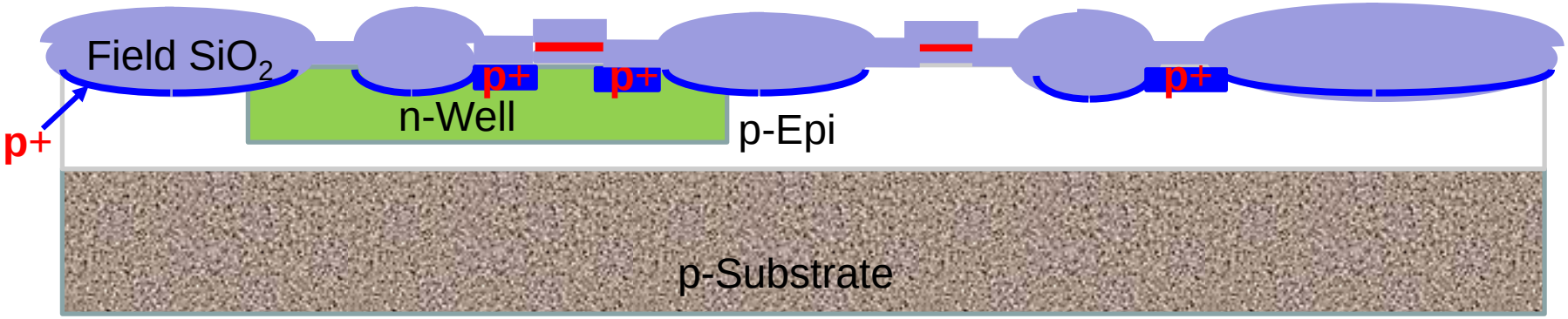


Self-alignment

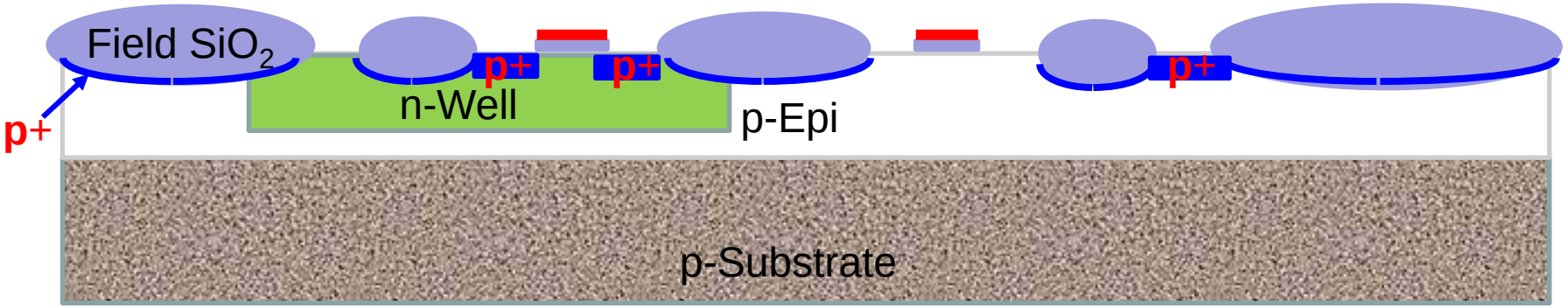
Implant with B^+



Resist is removed and oxide is formed during annealing for B^+ implantation

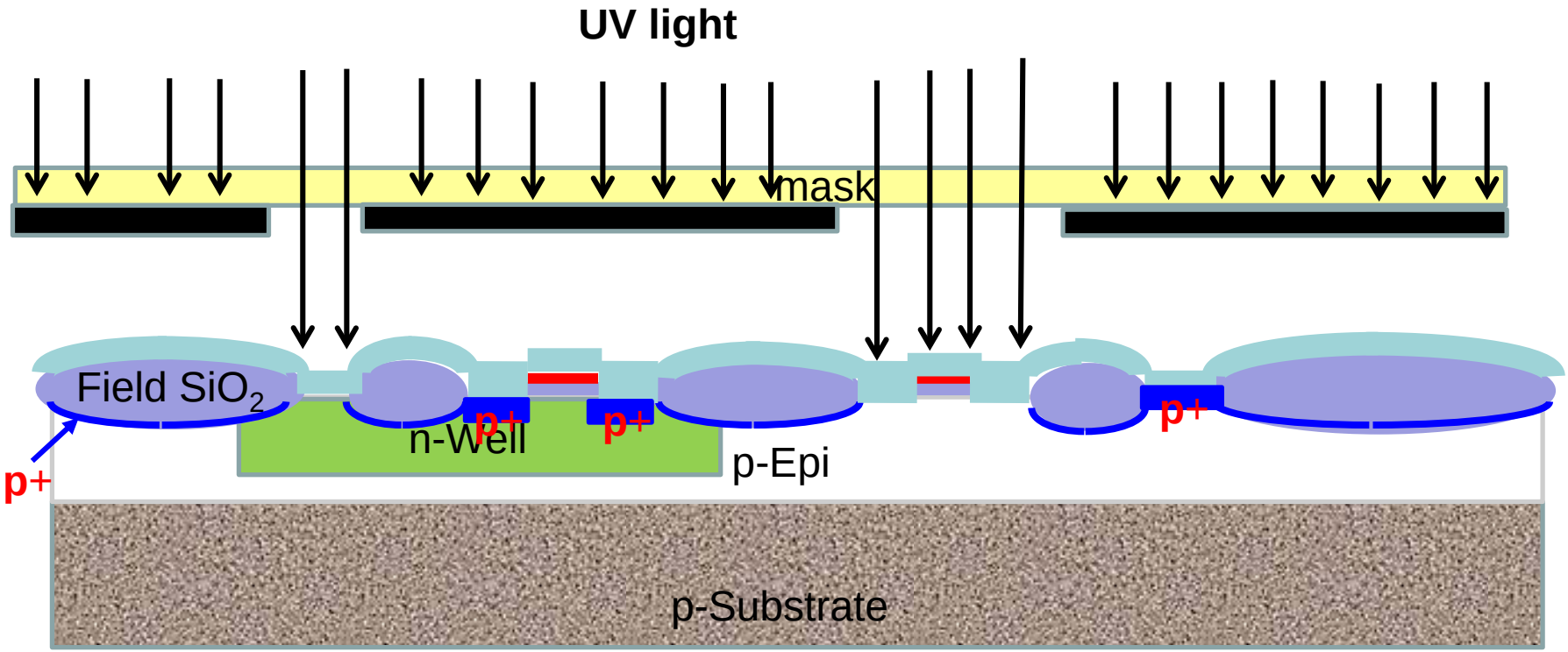


Etch oxide

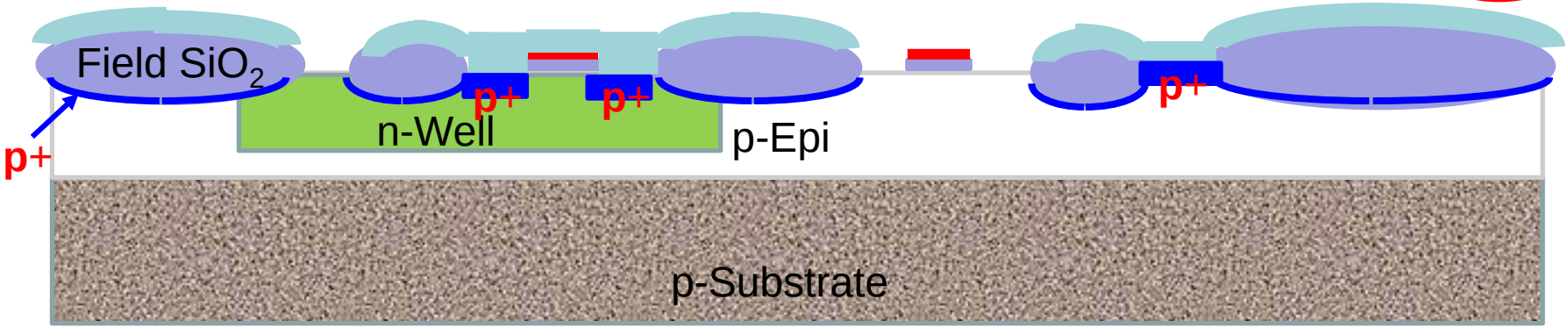


Mask5: n-select

Spin resist and Expose resist using n-select mask



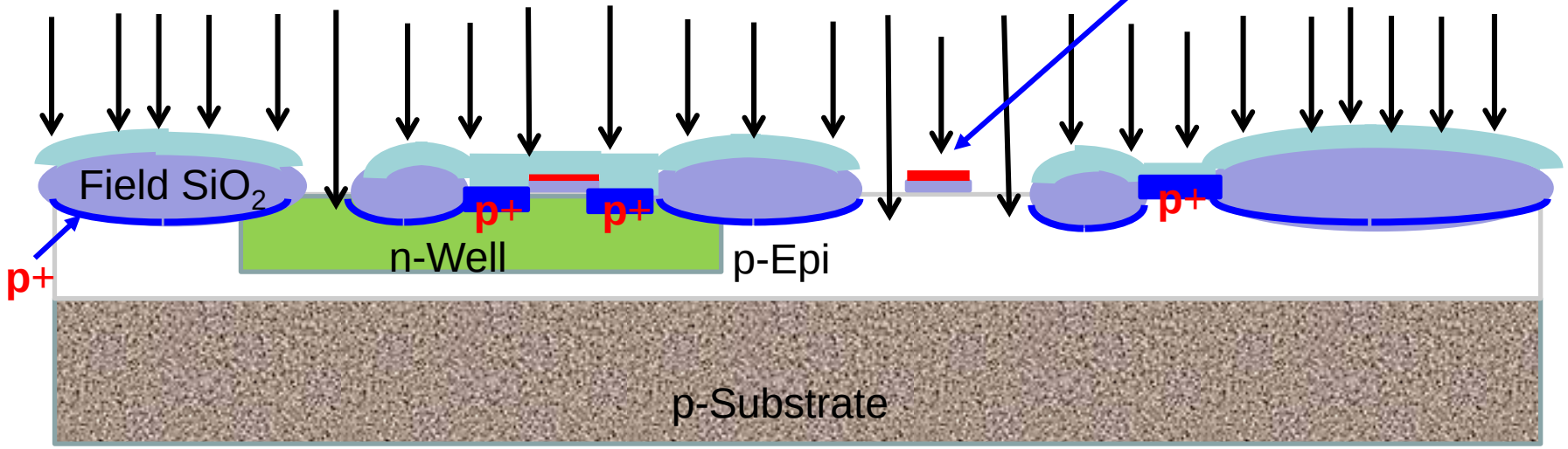
Develop resist



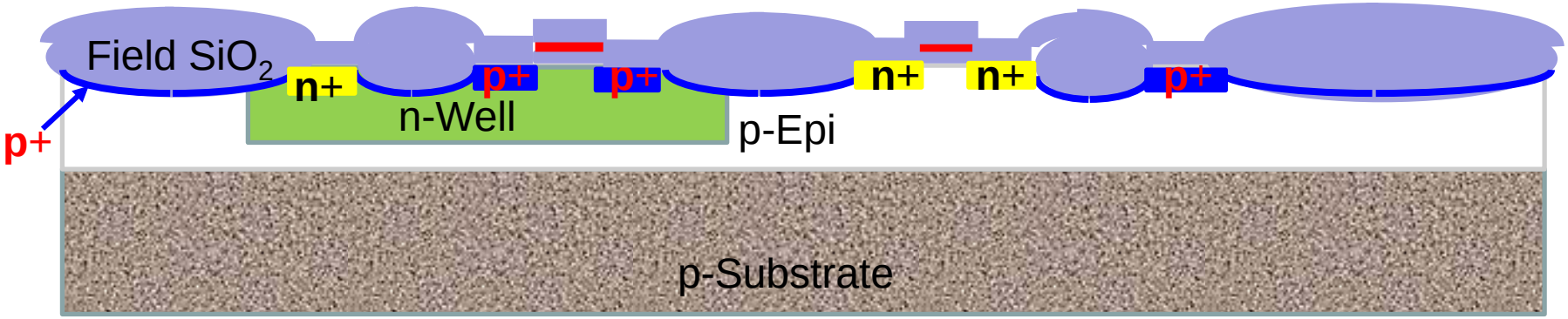
Implant with As^+

Self-alignment

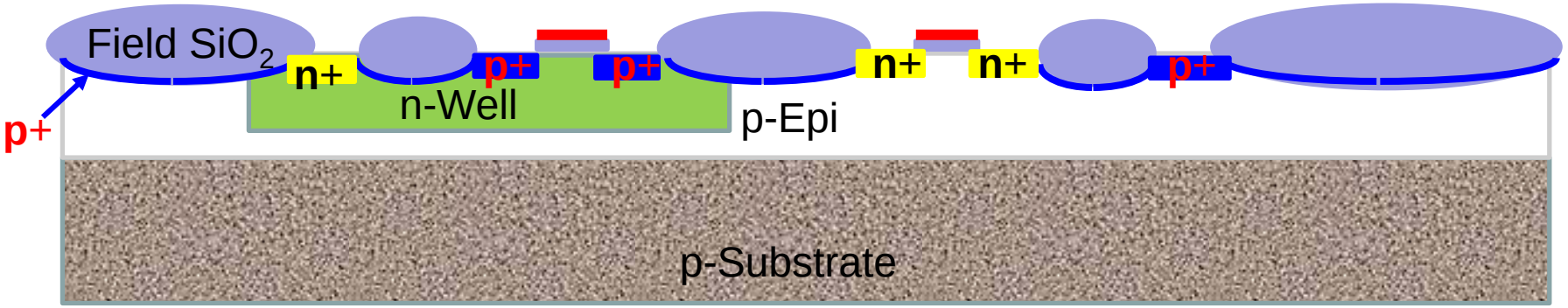
As^+



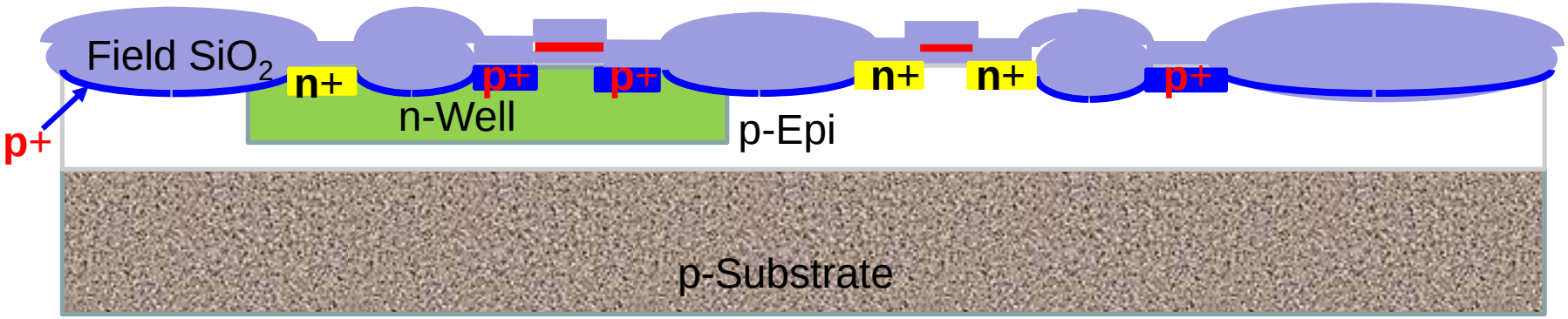
Resist is removed and oxide is formed during annealing for As^+ implantation



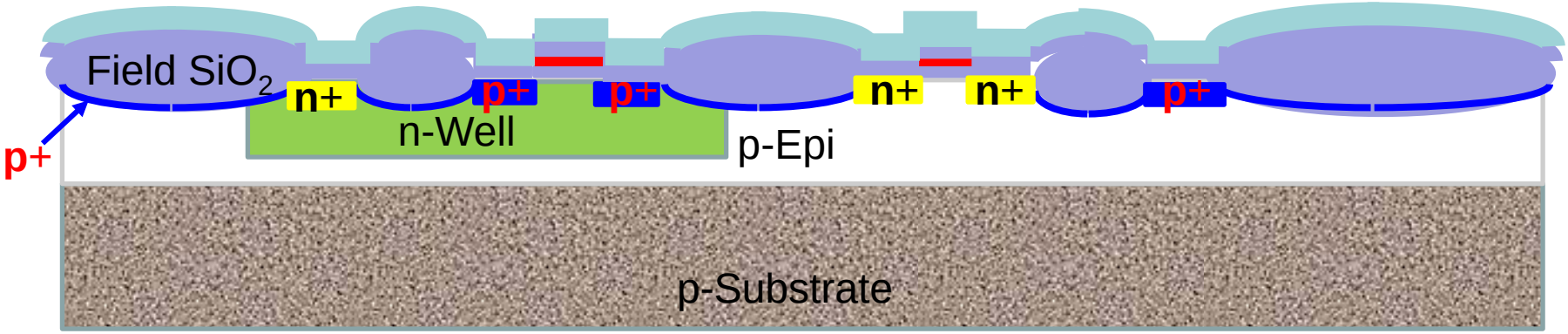
Etch oxide



Deposit oxide using CVD

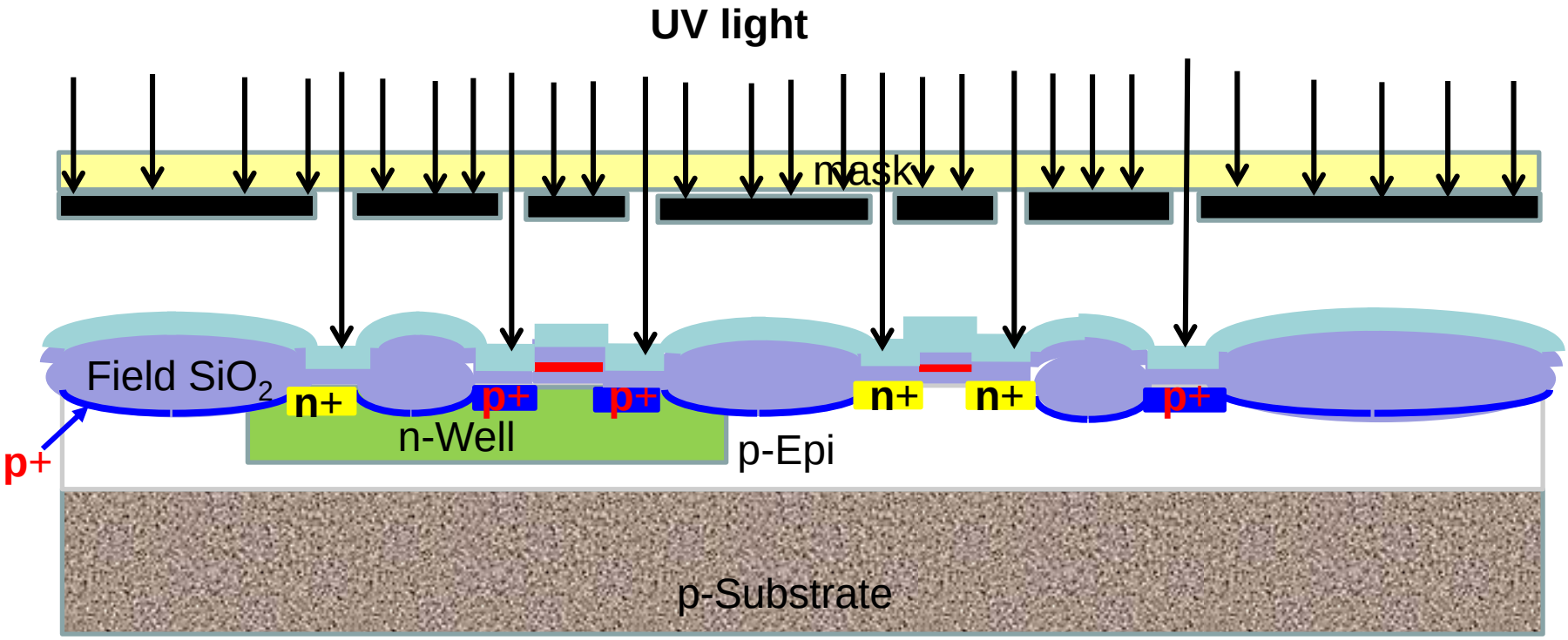


Spin resist

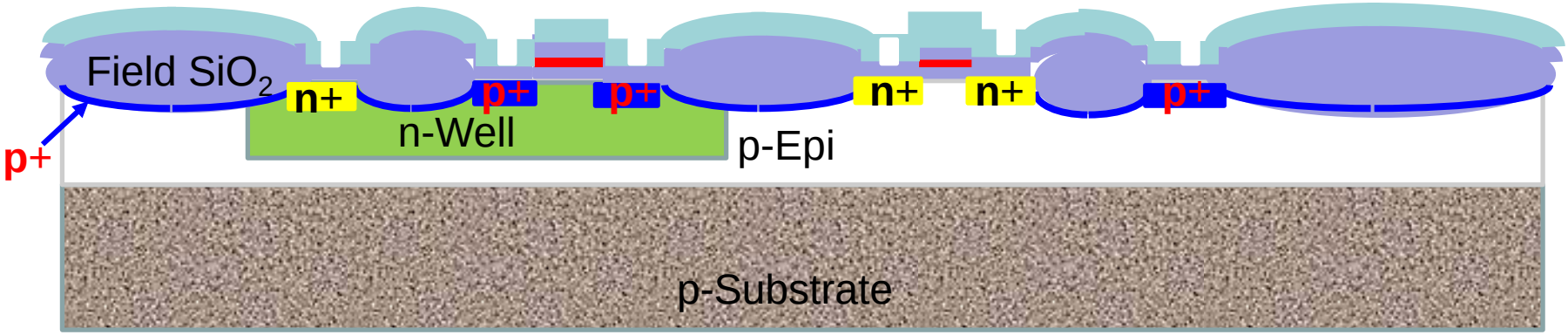


Mask6: ohmic contact

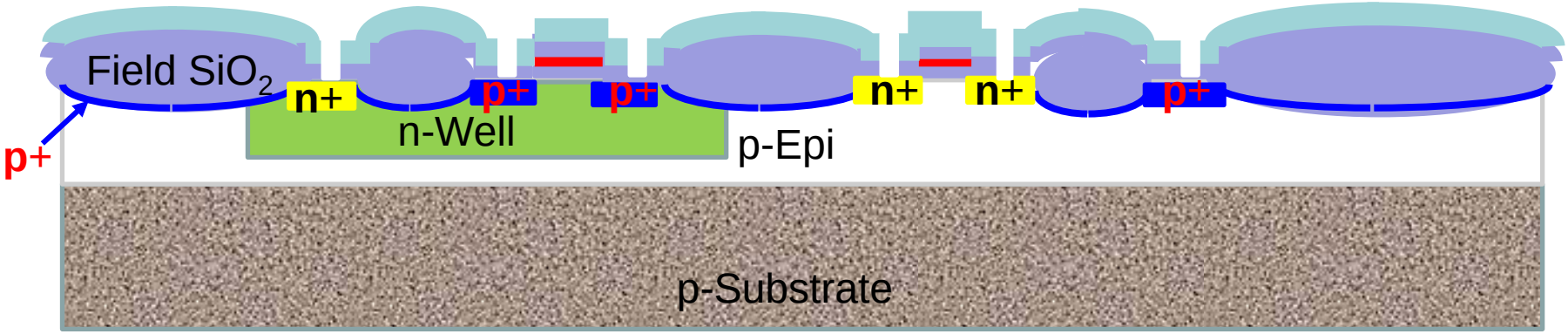
Expose resist using contact mask



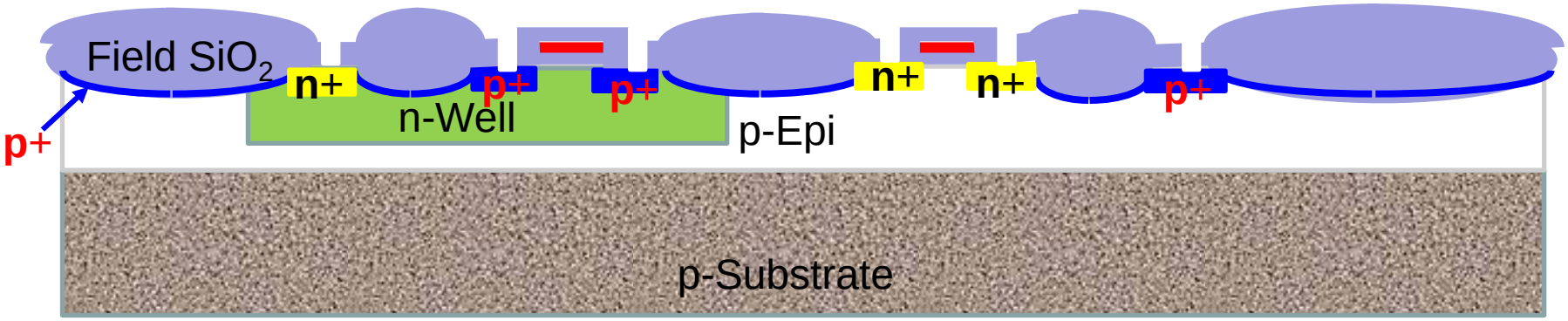
Develop resist



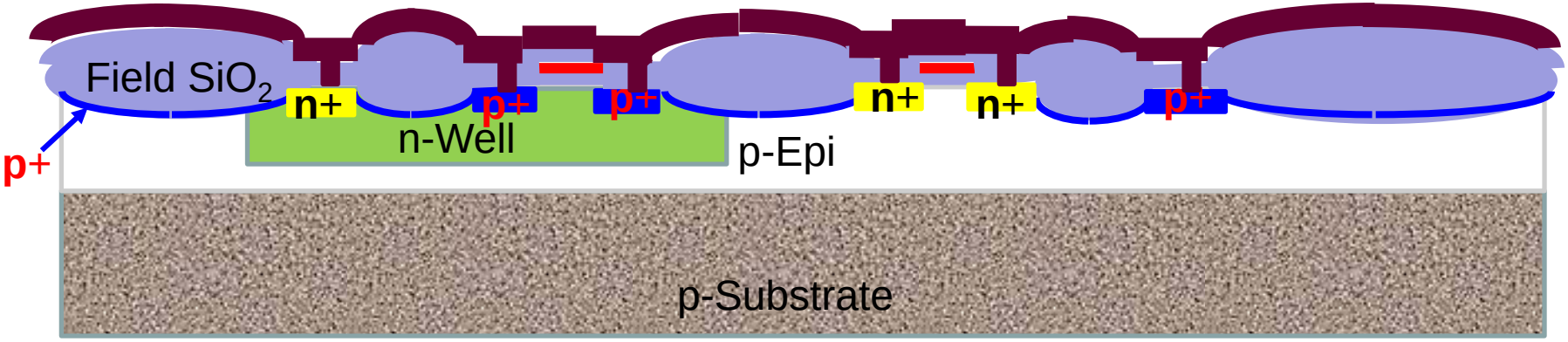
Etch contact holes



Remove resist

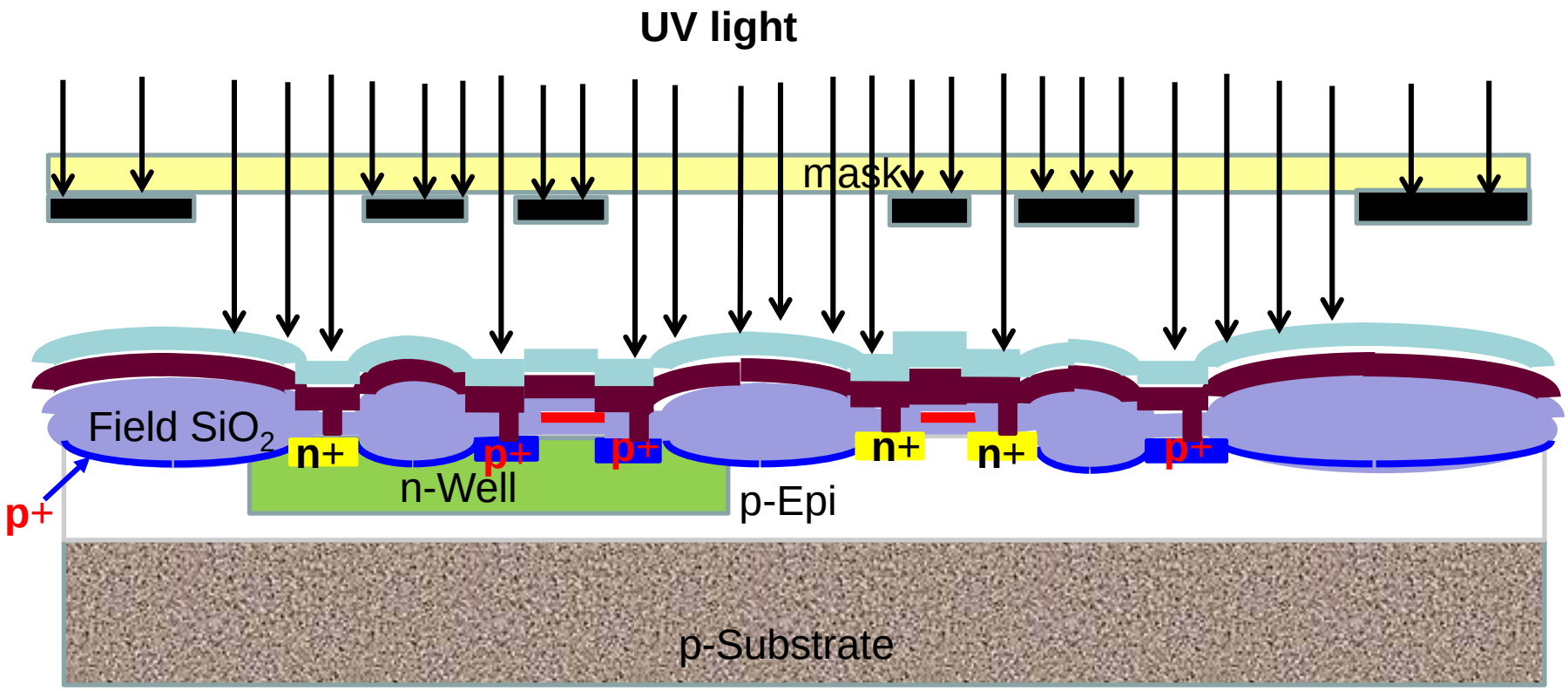


Deposit metal Al using PVD

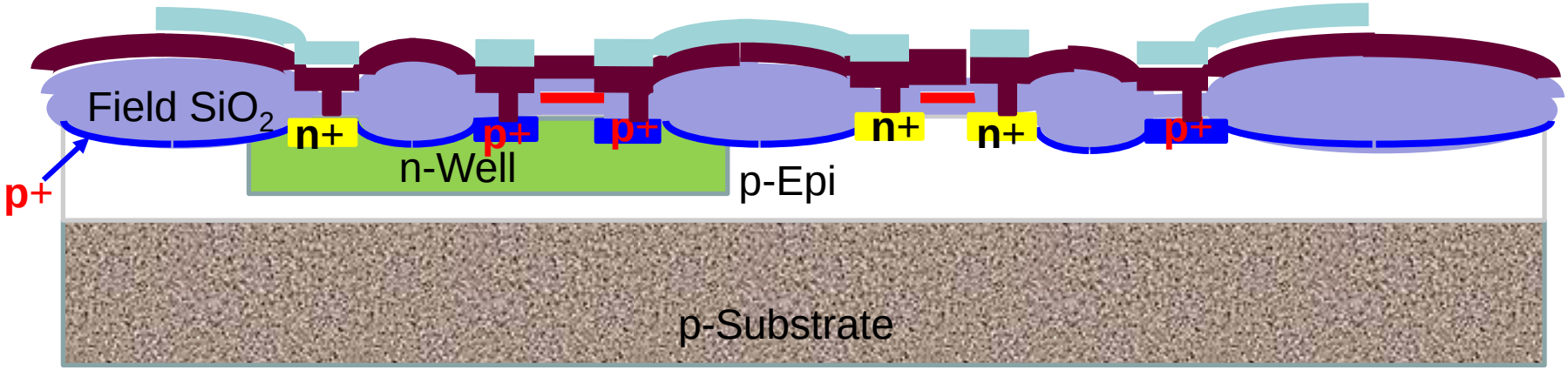


Mask 7: metal mask

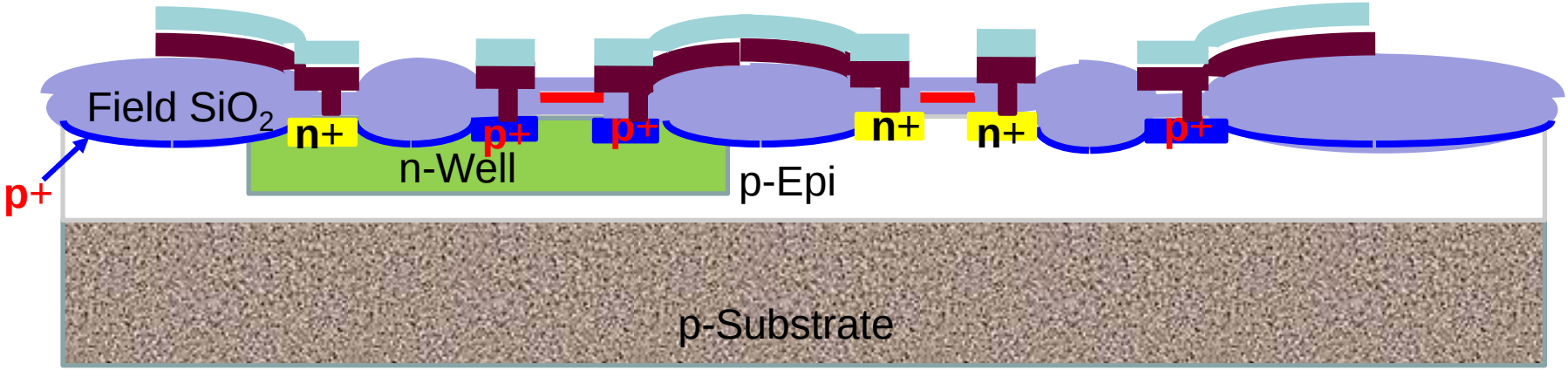
Spin resist and Expose resist using metal mask



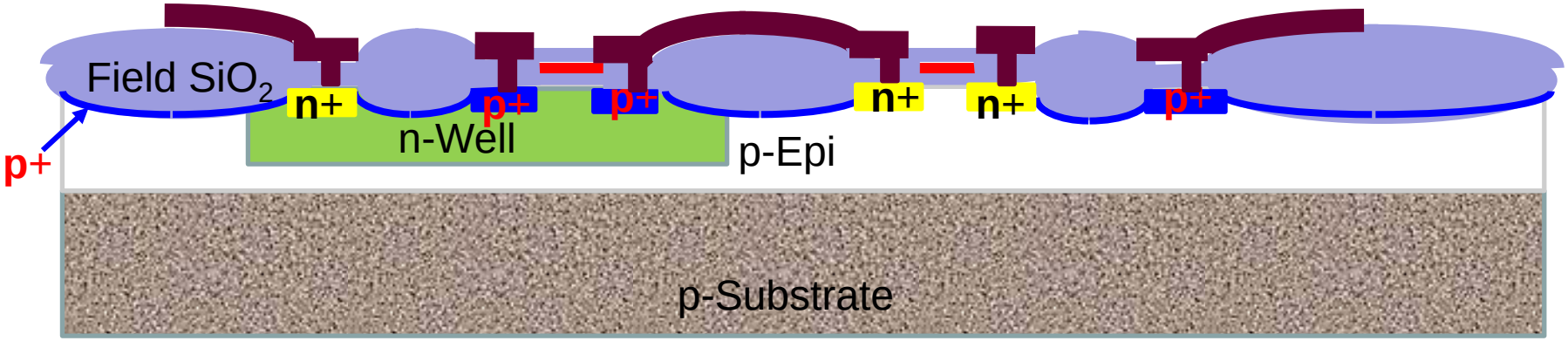
Develop resist



Etch metal



Remove resist



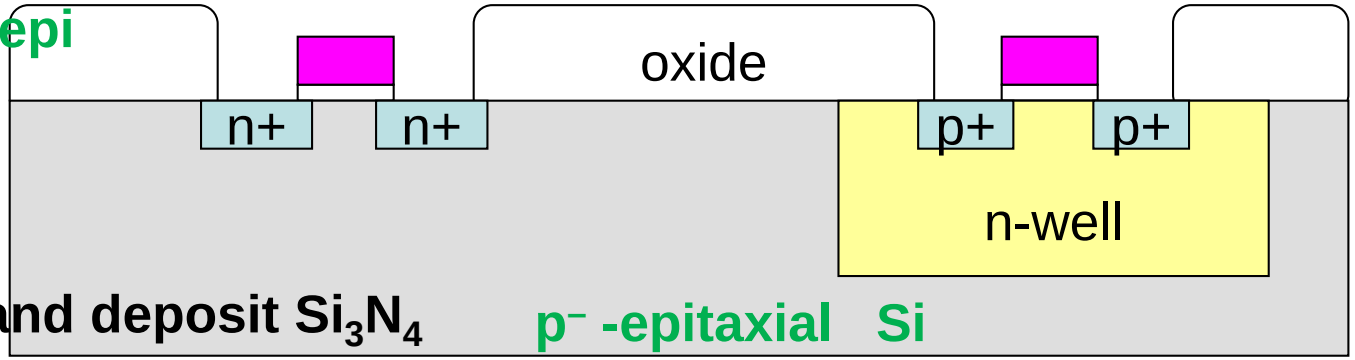
Passivation


Mask1
clear
mask
chromium
Mask2
mask
Mask3
mask
Mask4
mask
Mask5
mask
Mask6
mask
Mask7
mask

M2=M4, M2=M5

Conceptual CMOS Process Flow

1. p-type wafer, p^-- epi



2. Using M1 to Create "n-well"

3. Grow pad oxide and deposit Si_3N_4

Using M2 to define active region, channel stop implant, field oxidation

4. Remove pad oxide and Si_3N_4, grow gate oxide

5. Deposit & pattern poly-Si gate electrodes using M3

M4

6. Dope p-channel S/D & p-Sub contacts (need to protect NMOS areas)

7. Dope n-channel S/D & n-well contacts (need to protect PMOS areas)

M5

8. Deposit insulating layer (oxide)

Open contact holes using M6

→ At least 3 more masks, as compared to NMOS process

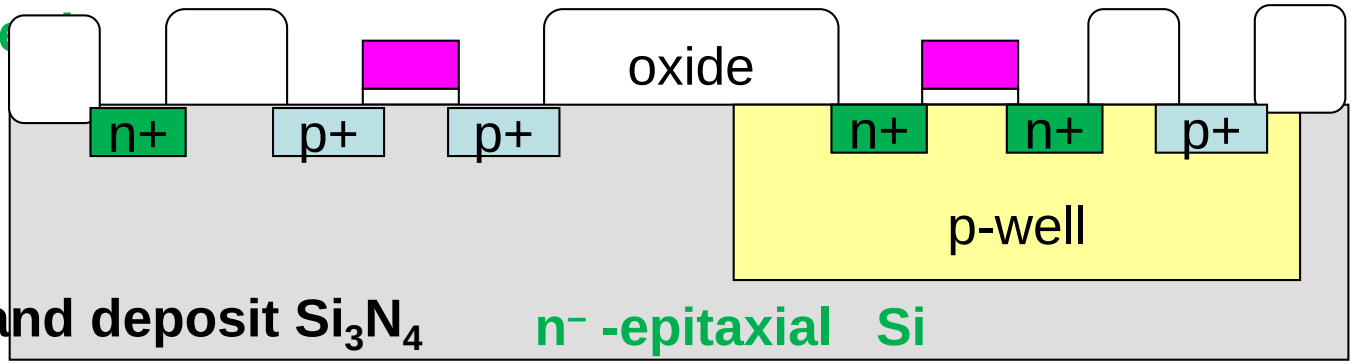
9. Deposit and pattern metal interconnects using M7

Conceptual CMOS Process Flow

1. n-type wafer, n^-- (

2. Using M1 to

   Create "p-well"



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   Using M2 to define active region, channel stop implant, field oxidation

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6. Dope n-channel S/D & n-Sub contacts (need to protect PMOS areas)

7. Dope p-channel S/D & p-well contacts (need to protect NMOS areas)

M5

8. Deposit insulating layer (oxide)

   Open contact holes using M6

→ At least 3 more masks, as compared to NMOS process

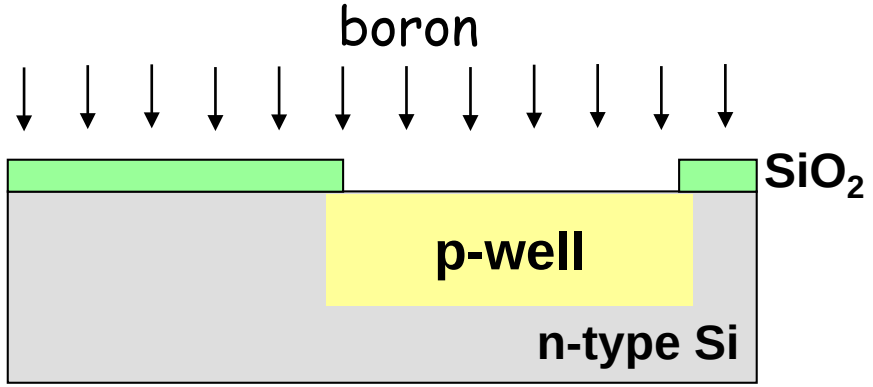
9. Deposit and pattern metal interconnects using M7

Additional Process Steps Required for CMOS

1. Well Formation

Top view of p-well mask
(dark field)

Cross-sectional view of wafer



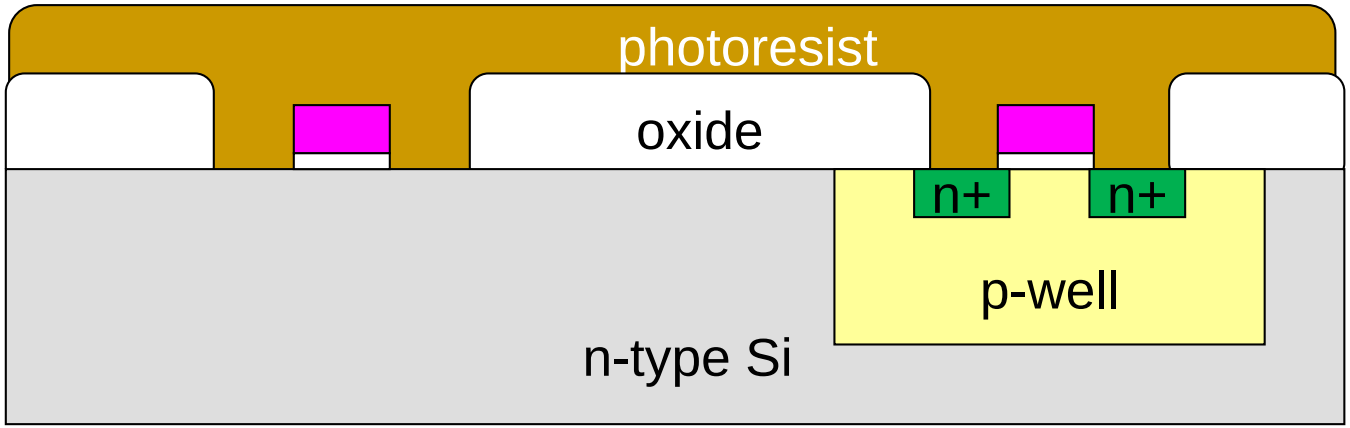
- **Before transistor fabrication, we must perform the following process steps:**
  a) grow oxide layer; pattern oxide using p-well mask
  b) implant phosphorus; anneal to form deep p-type regions

2. Masking the Source/Drain Implants

"Select p-channel" ⟶ We must protect the n-channel devices during the **boron** implantation step, and

"Select n-channel" ⟶ We must protect the p-channel devices during the **arsenic** implantation step

Example: Select p-channel

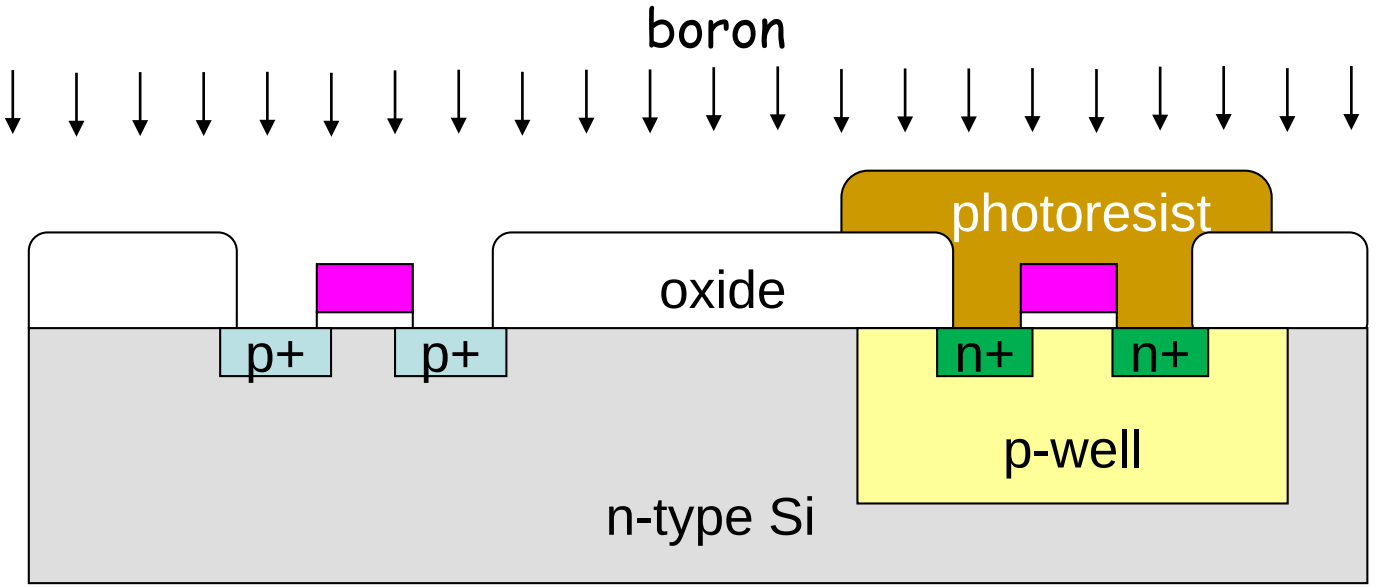


2. Masking the Source/Drain Implants

"Select p-channel" ⟶ We must protect the n-channel devices during the **boron** implantation step, and

"Select n-channel" ⟶ We must protect the p-channel devices during the **arsenic** implantation step

Example: Select p-channel

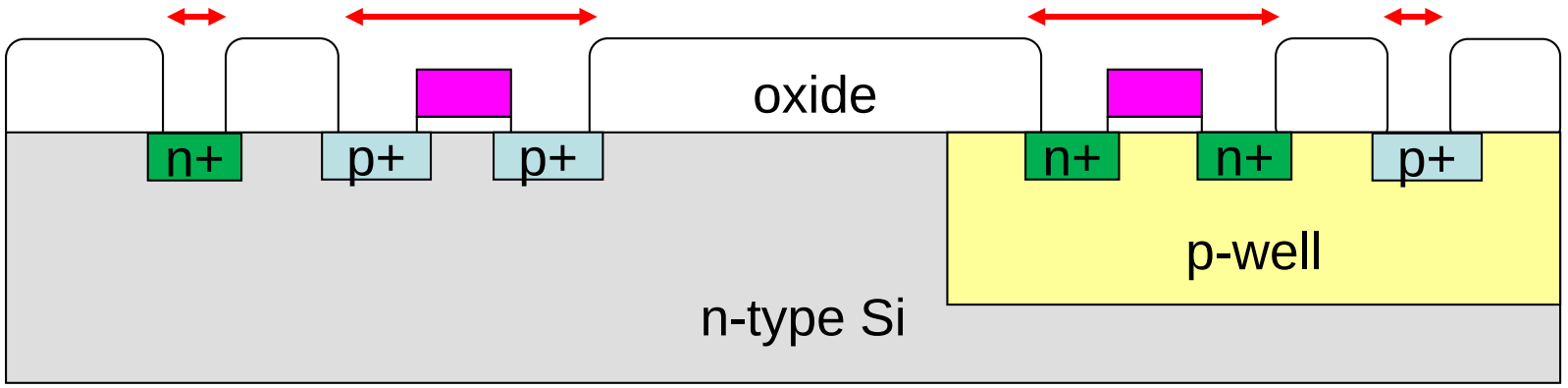


Forming Body Contacts

Modify oxide mask and “select” masks:

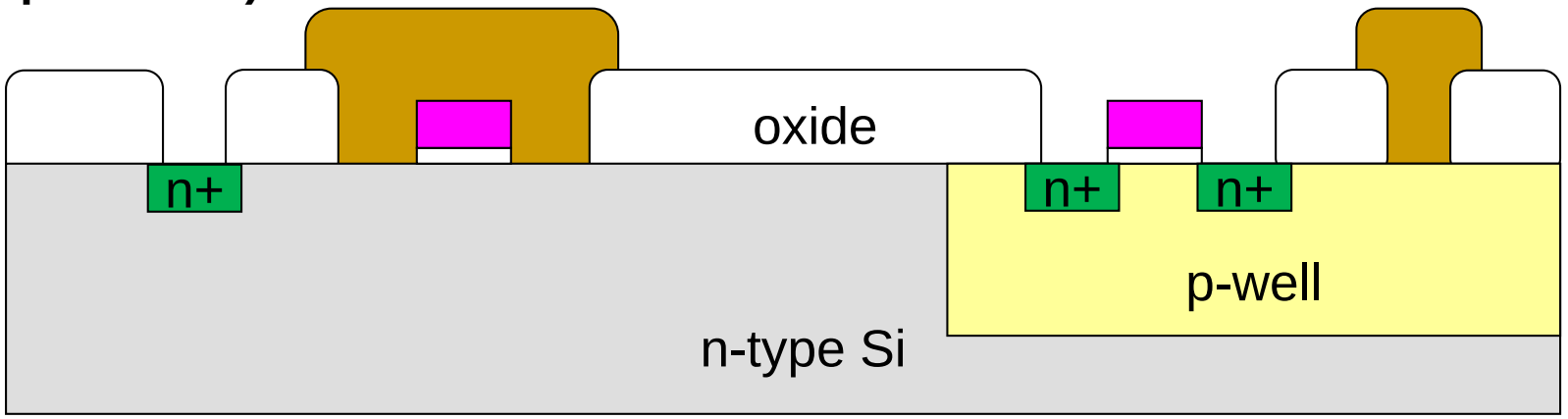
1. Open holes in original oxide layer, for body contacts
2. Include openings in select masks, to dope these regions

Active mask

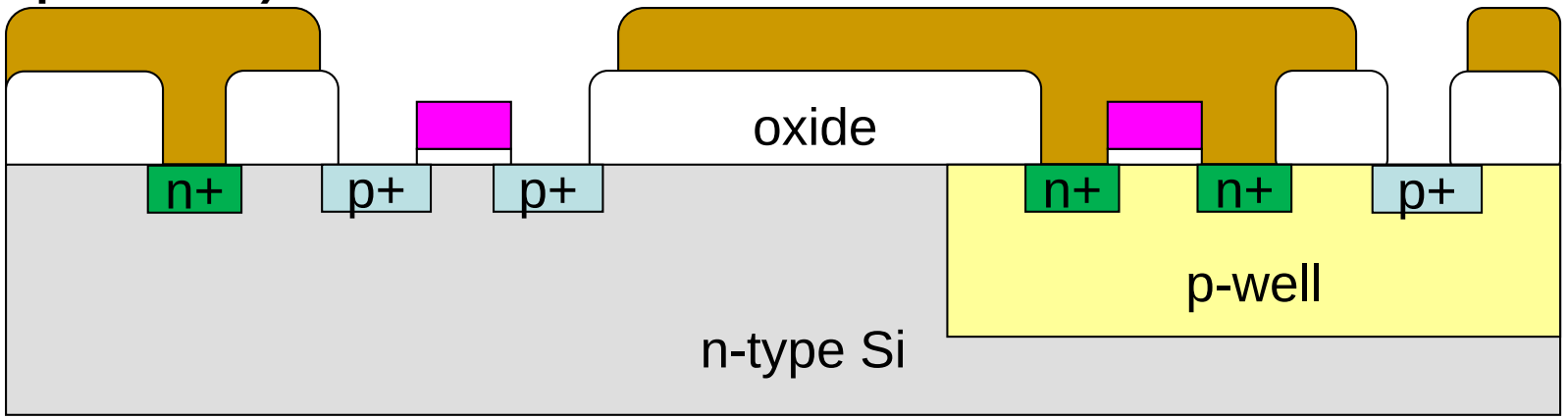


Select Masks

N-select: (As+ implantation)



P-select: (B+ implantation)



Simplified CMOS Inverter Process: Masks

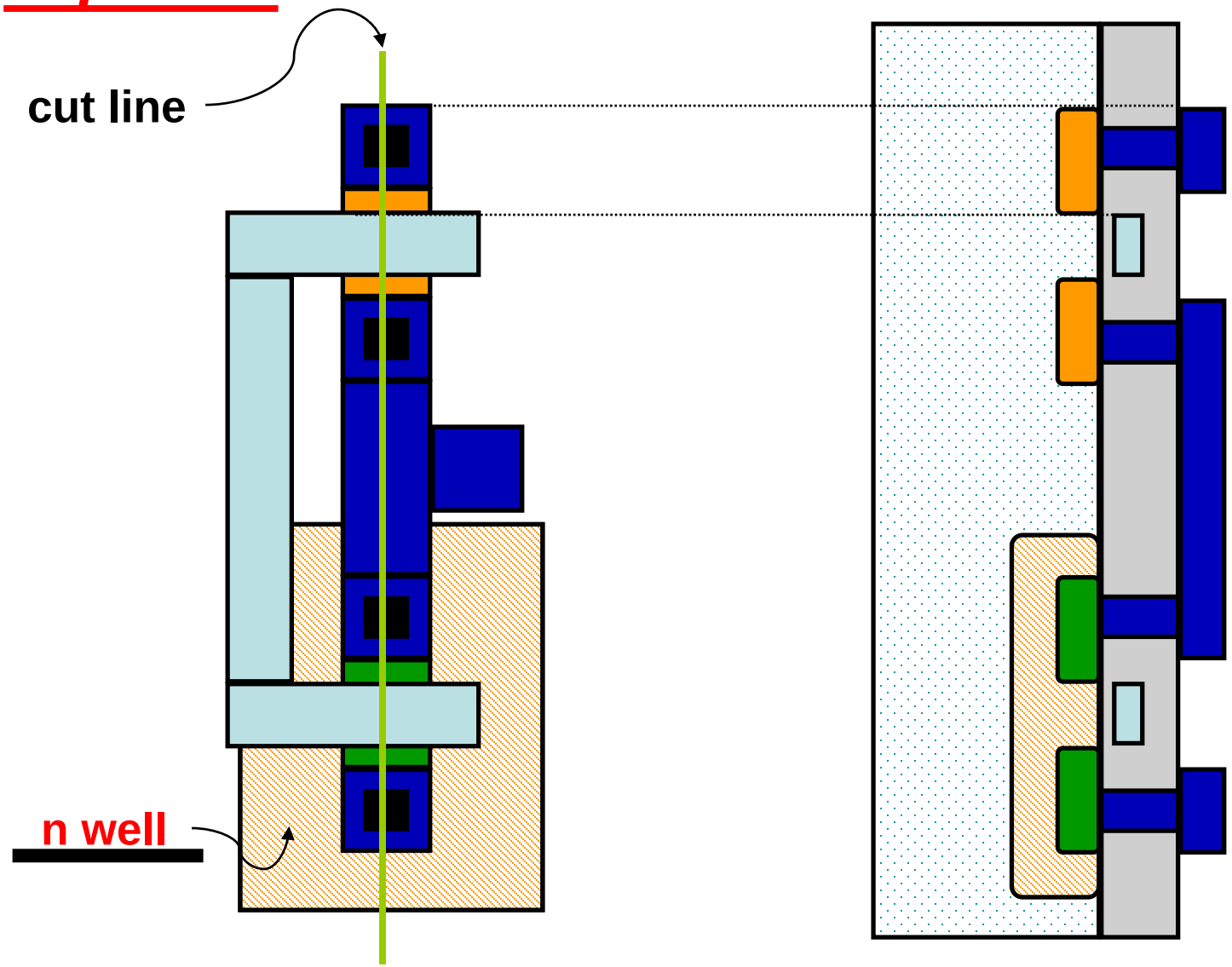
Thanks to Mary Jane Irwin
www.cse.psu.edu/~cg477

[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

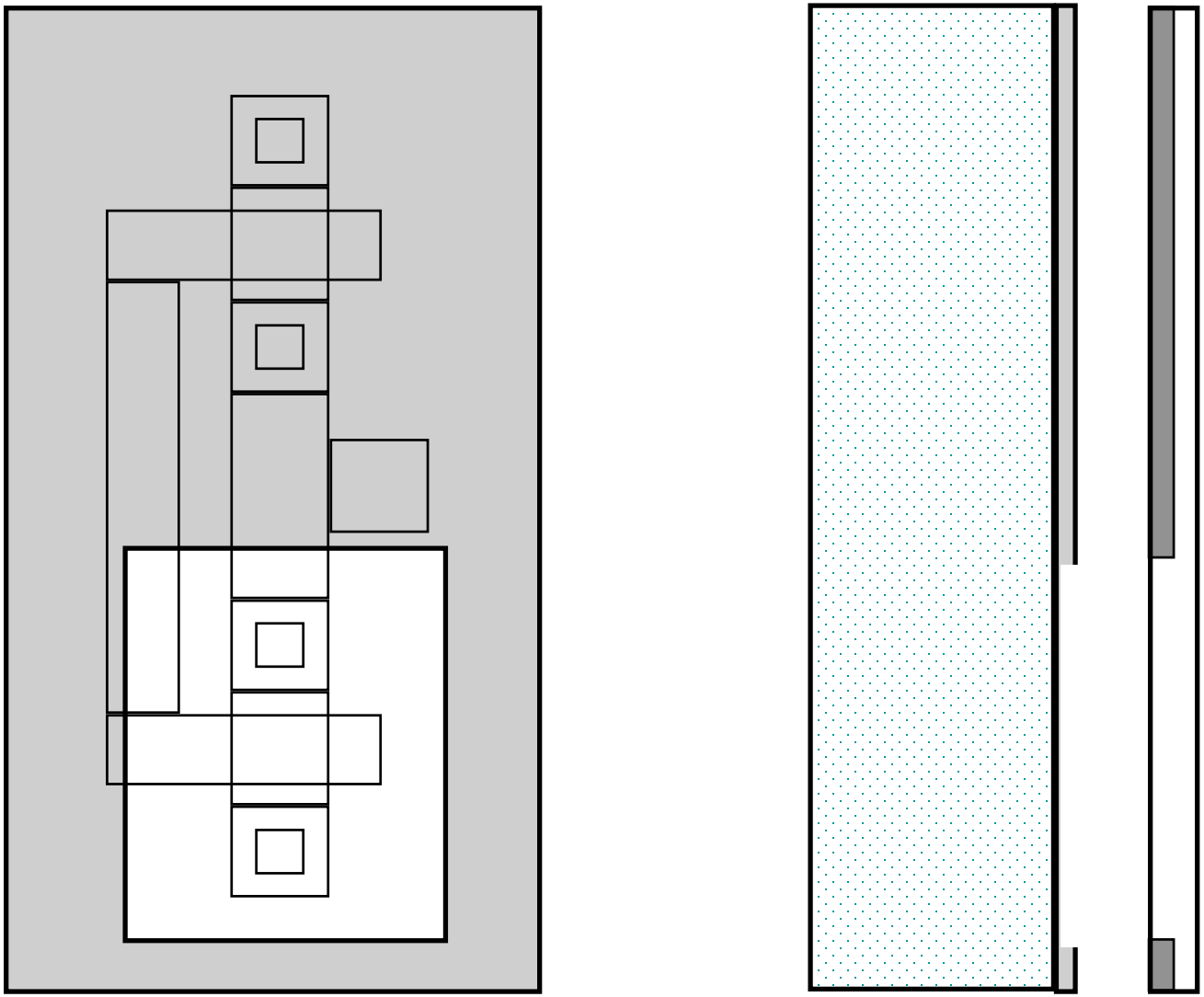
Simplified CMOS Inverter Process

Top View:

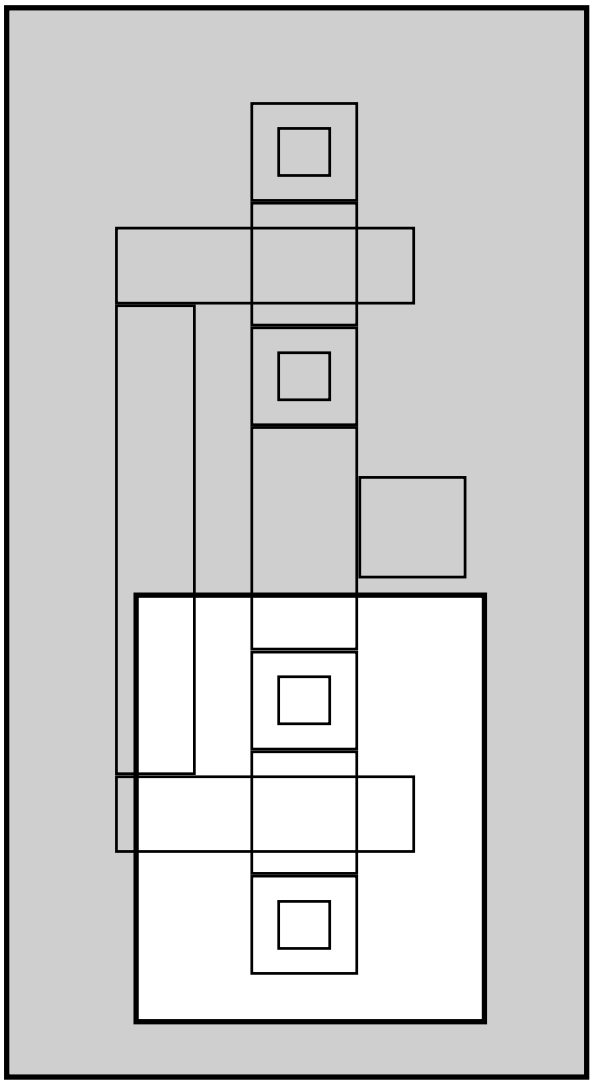
Cross-Sectional View:

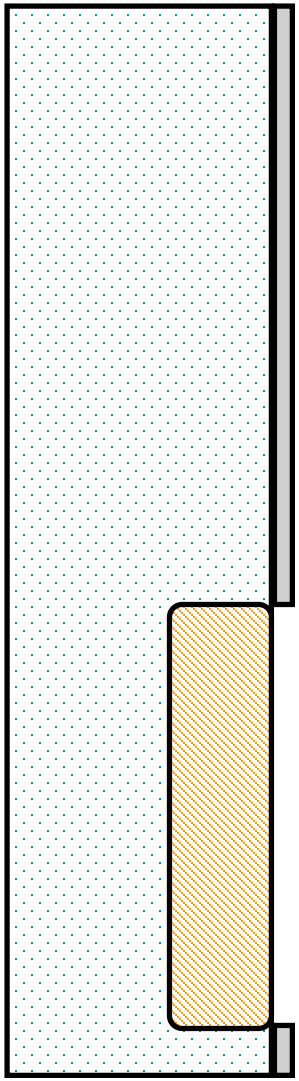


n-Well Mask (M1)

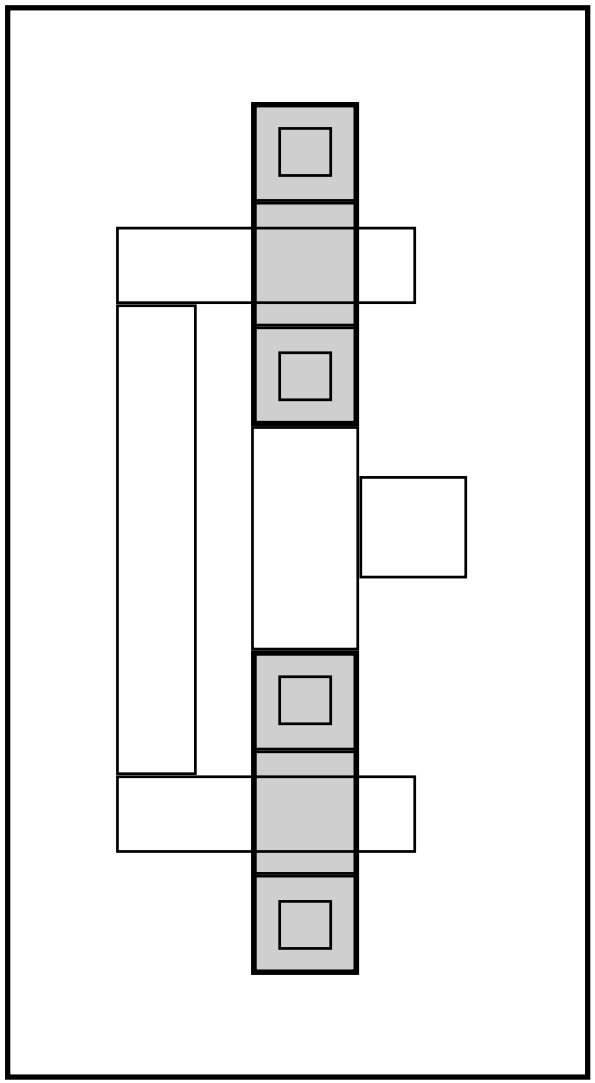


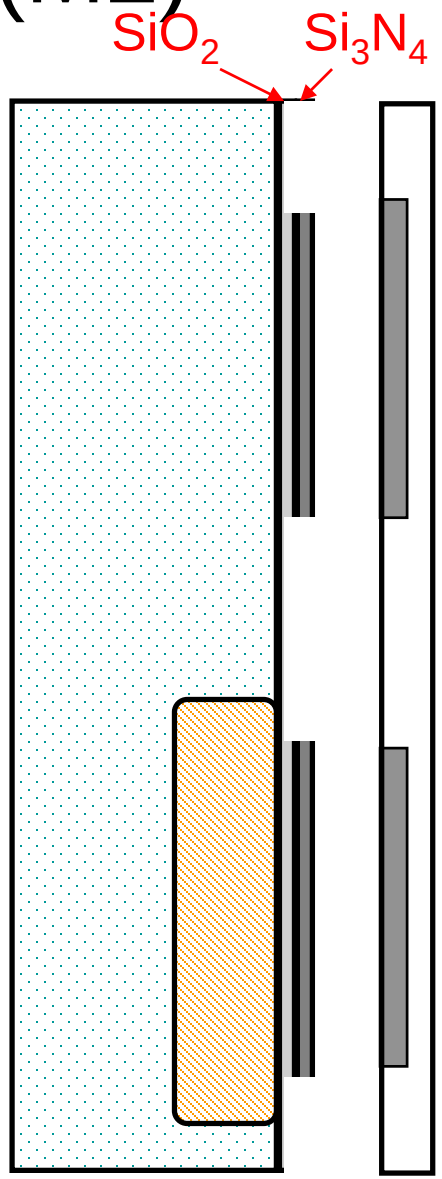
After n-well mask, As^+ implant + drive-in



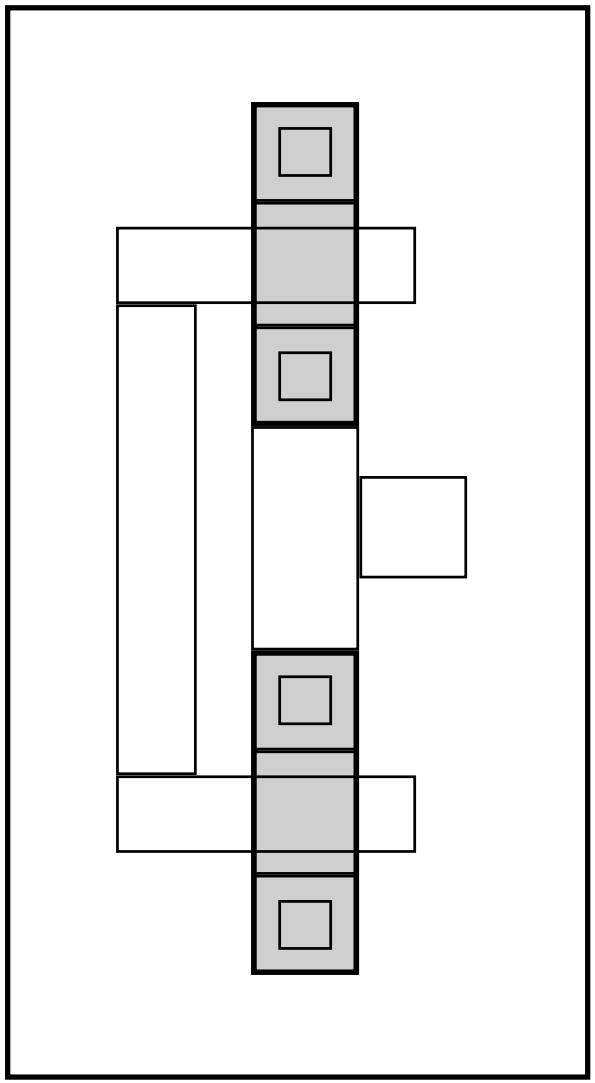


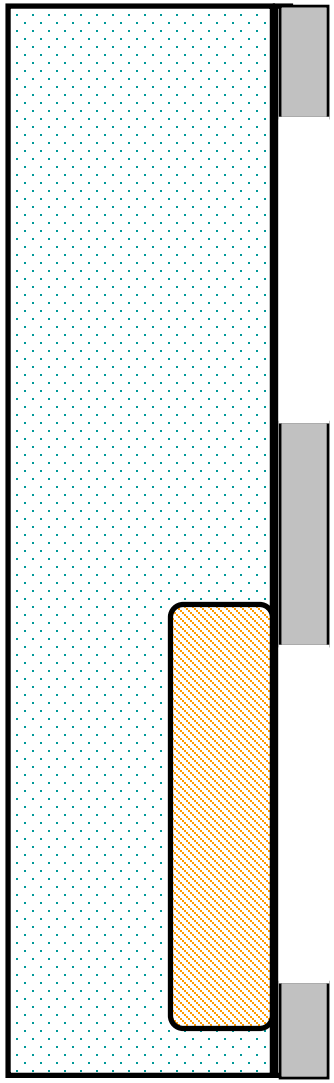
Active Mask (M2)



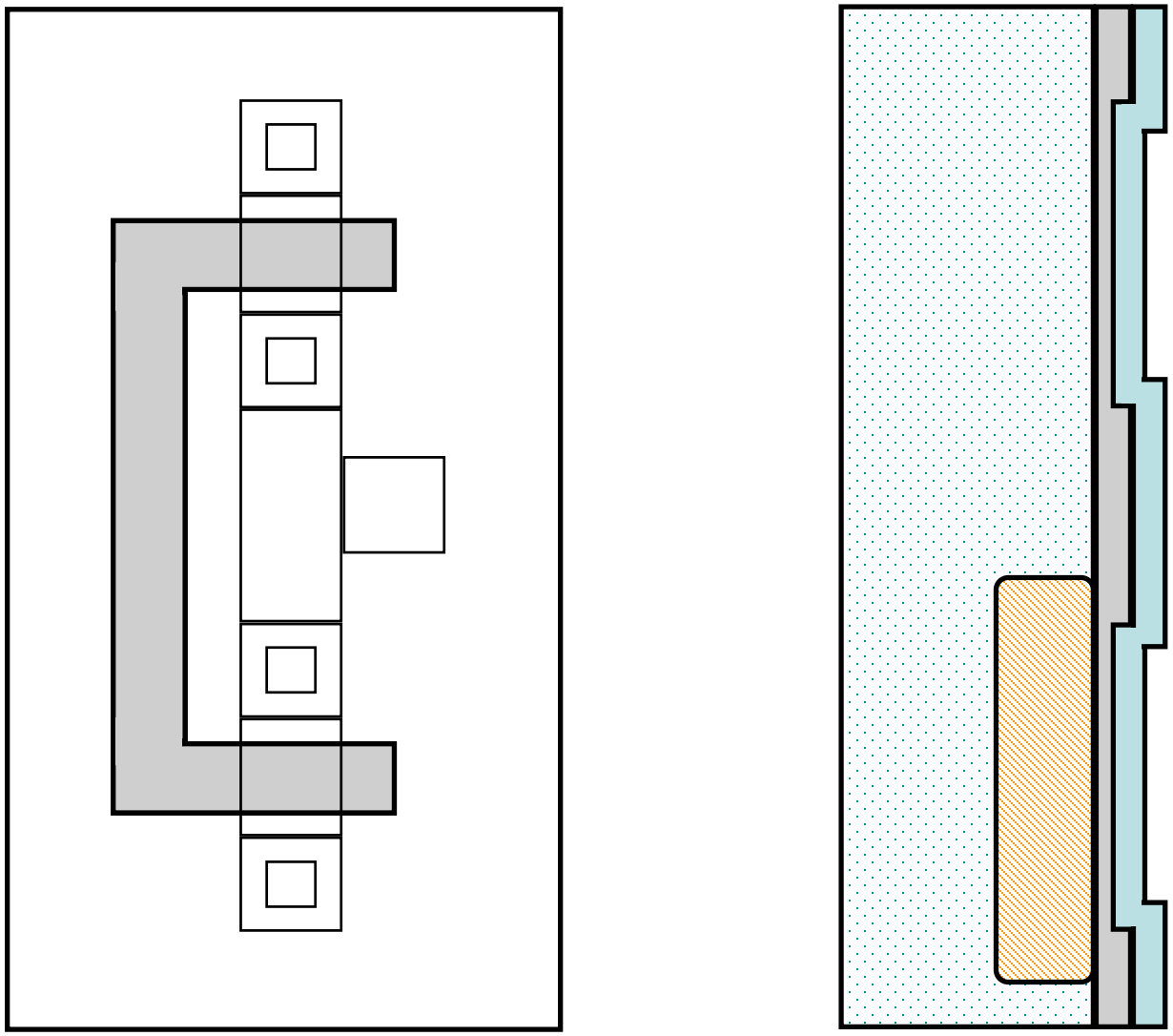


After M2, field oxide + gate oxide

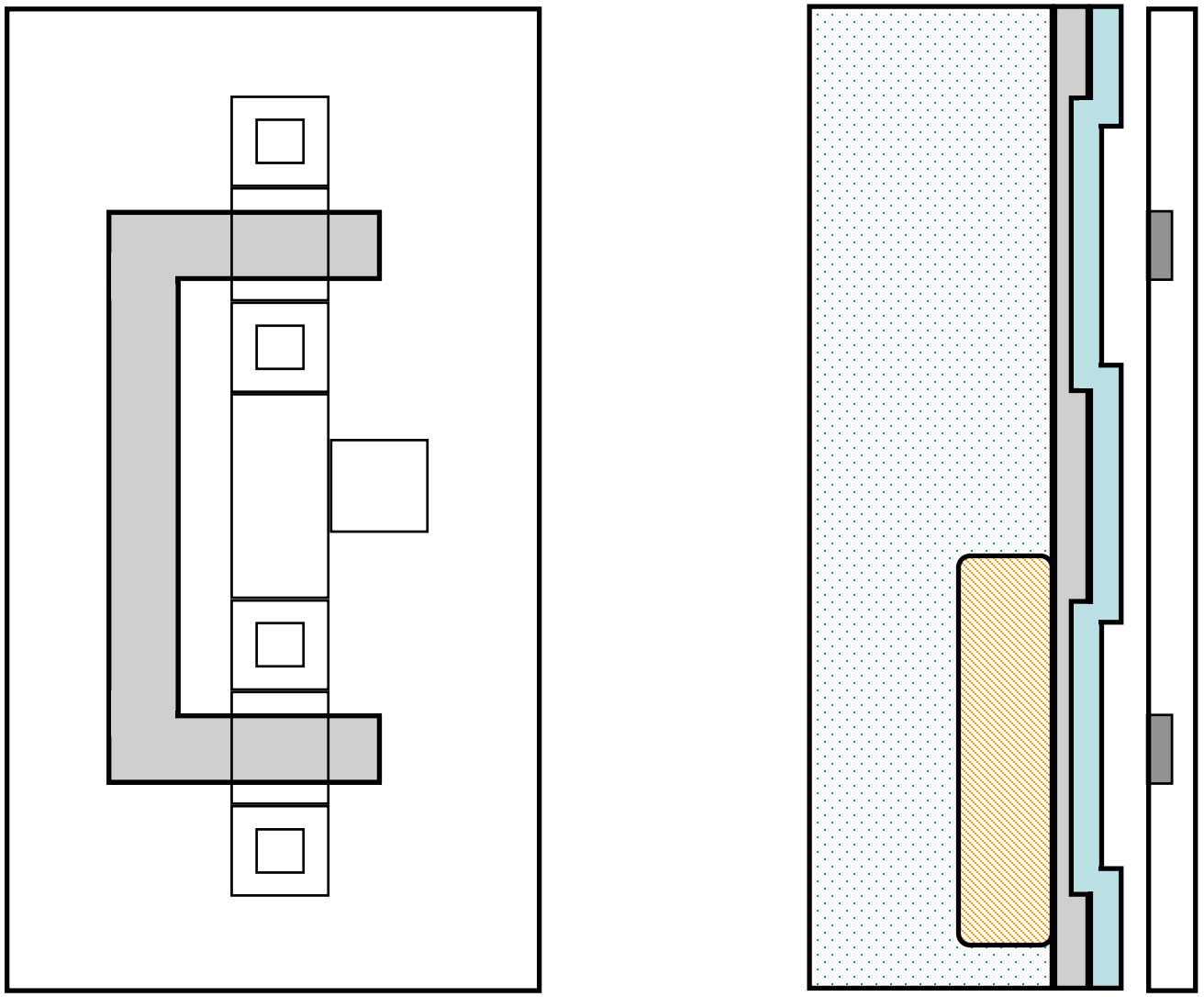




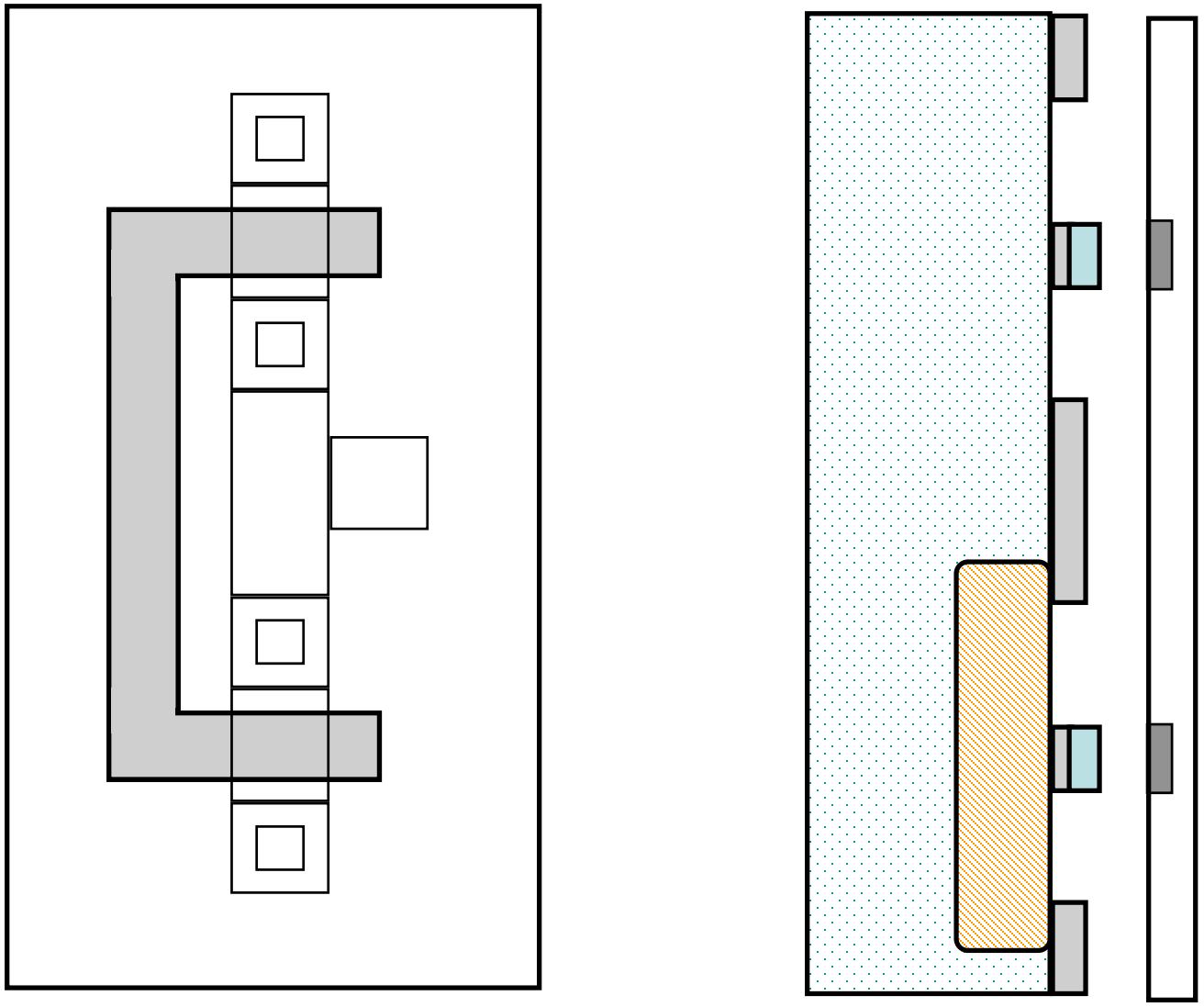
poly-Si deposition



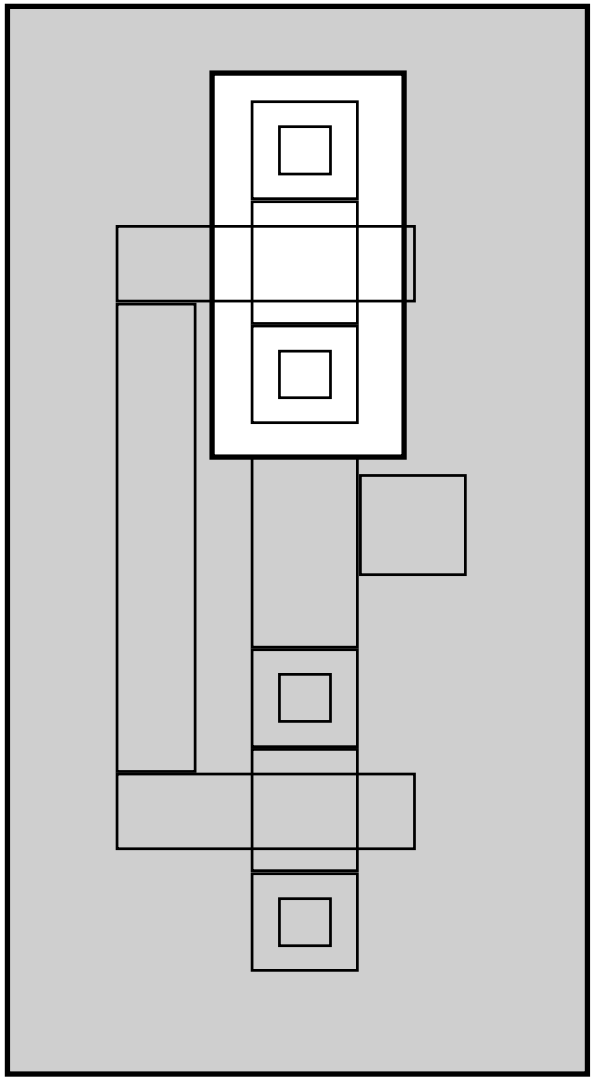
Poly Mask (M3)

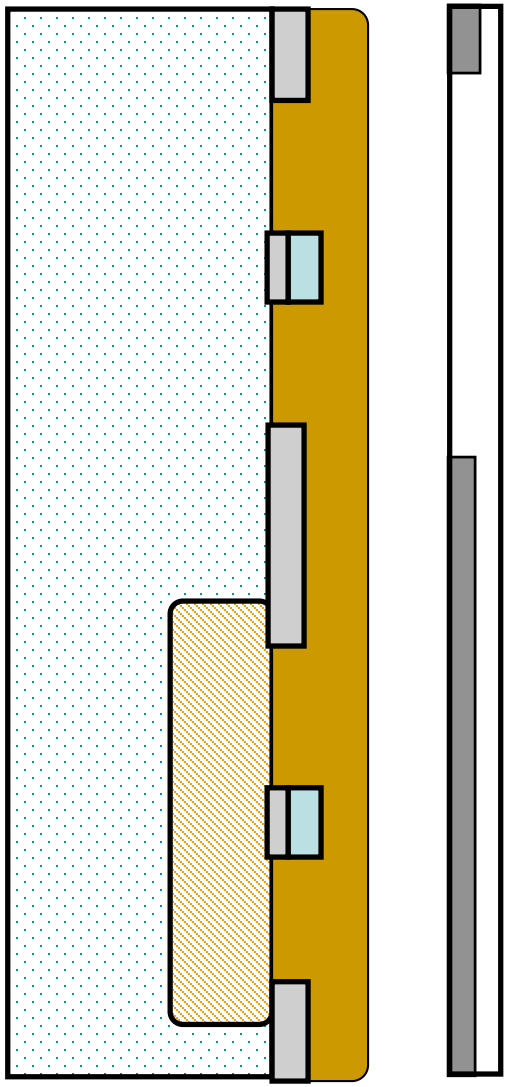


Poly Mask (M3)

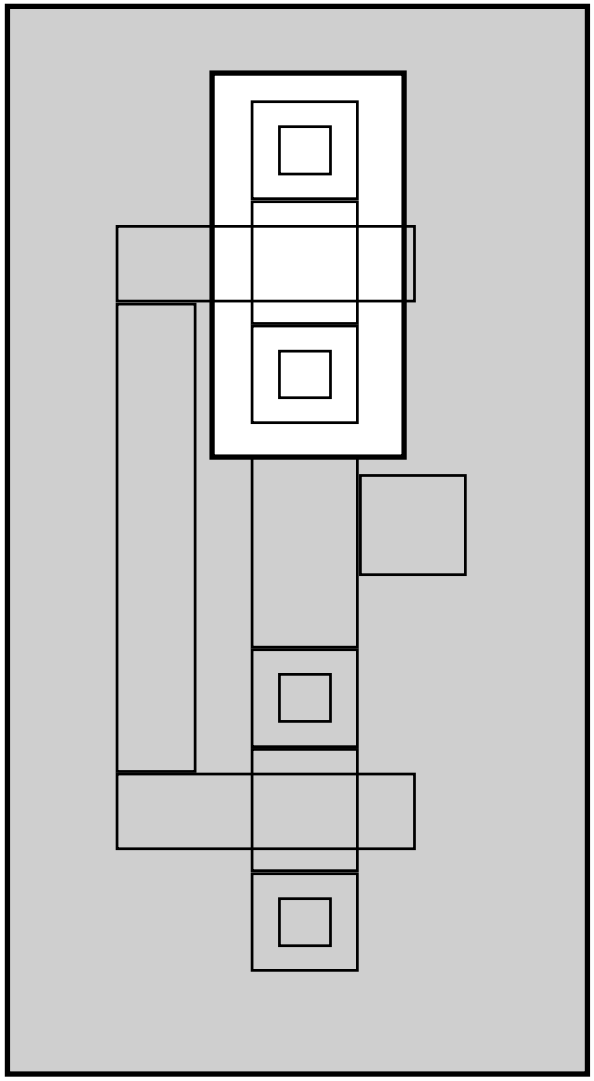


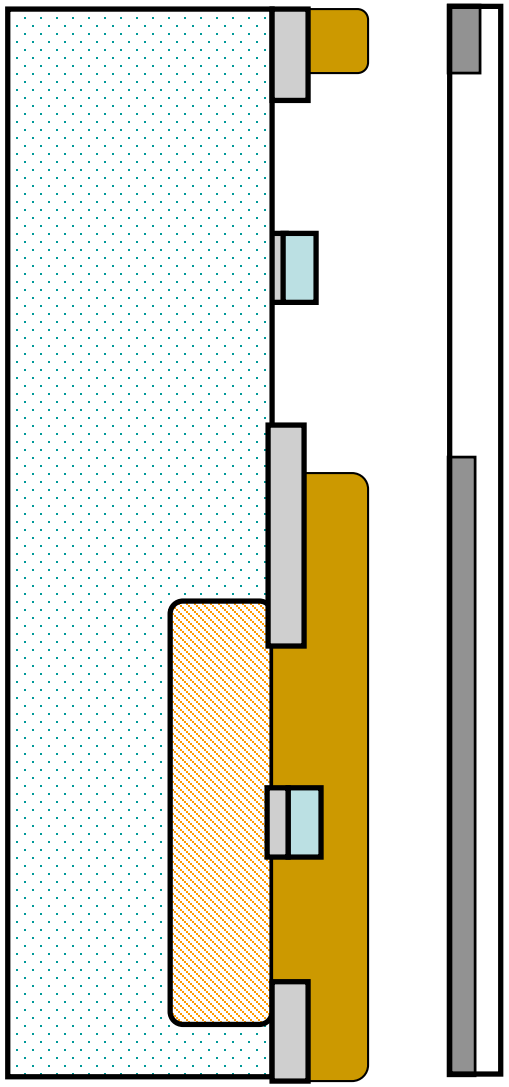
N-Select Mask (M4)



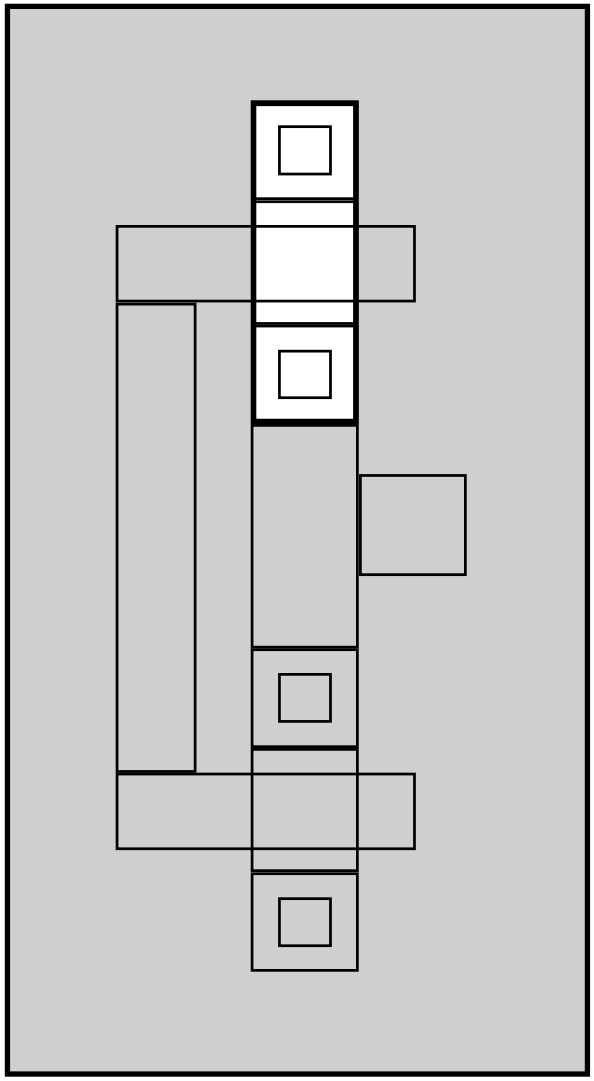


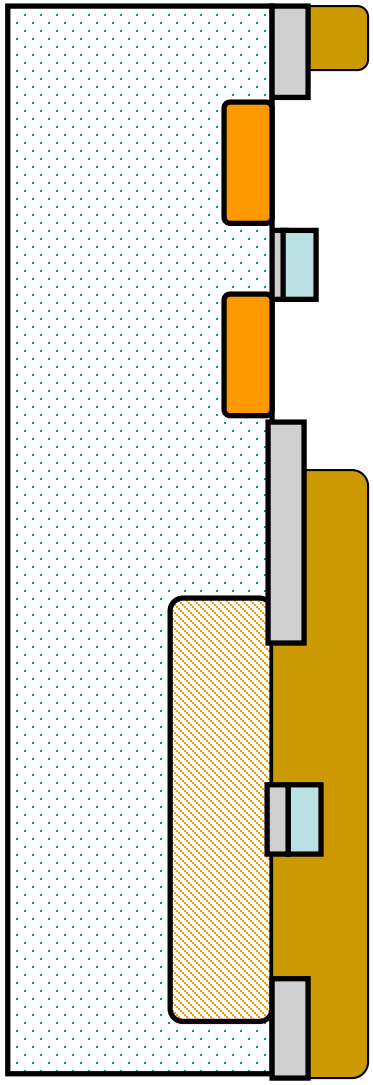
N Select Mask (M4)



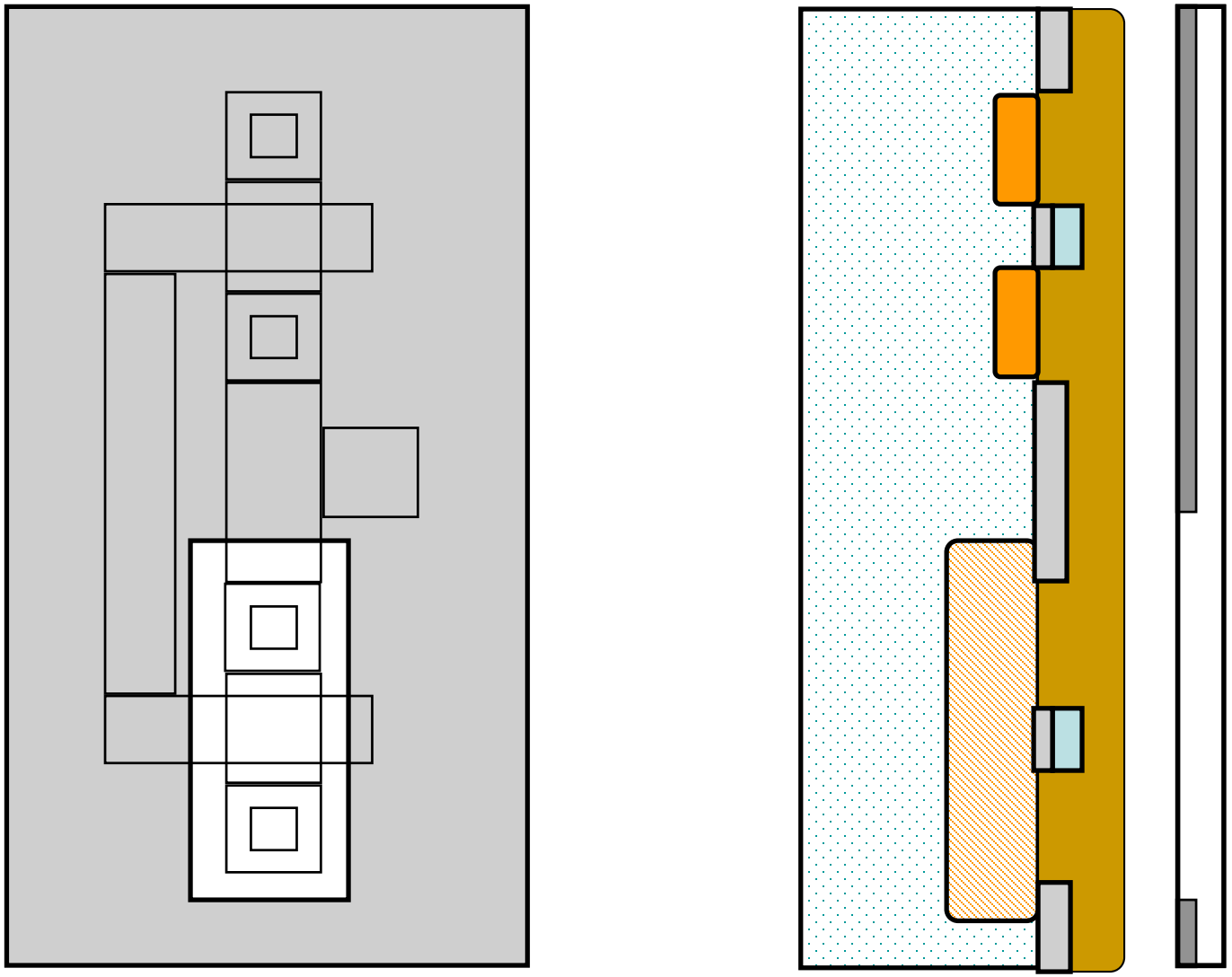


After M4, As^+ implant

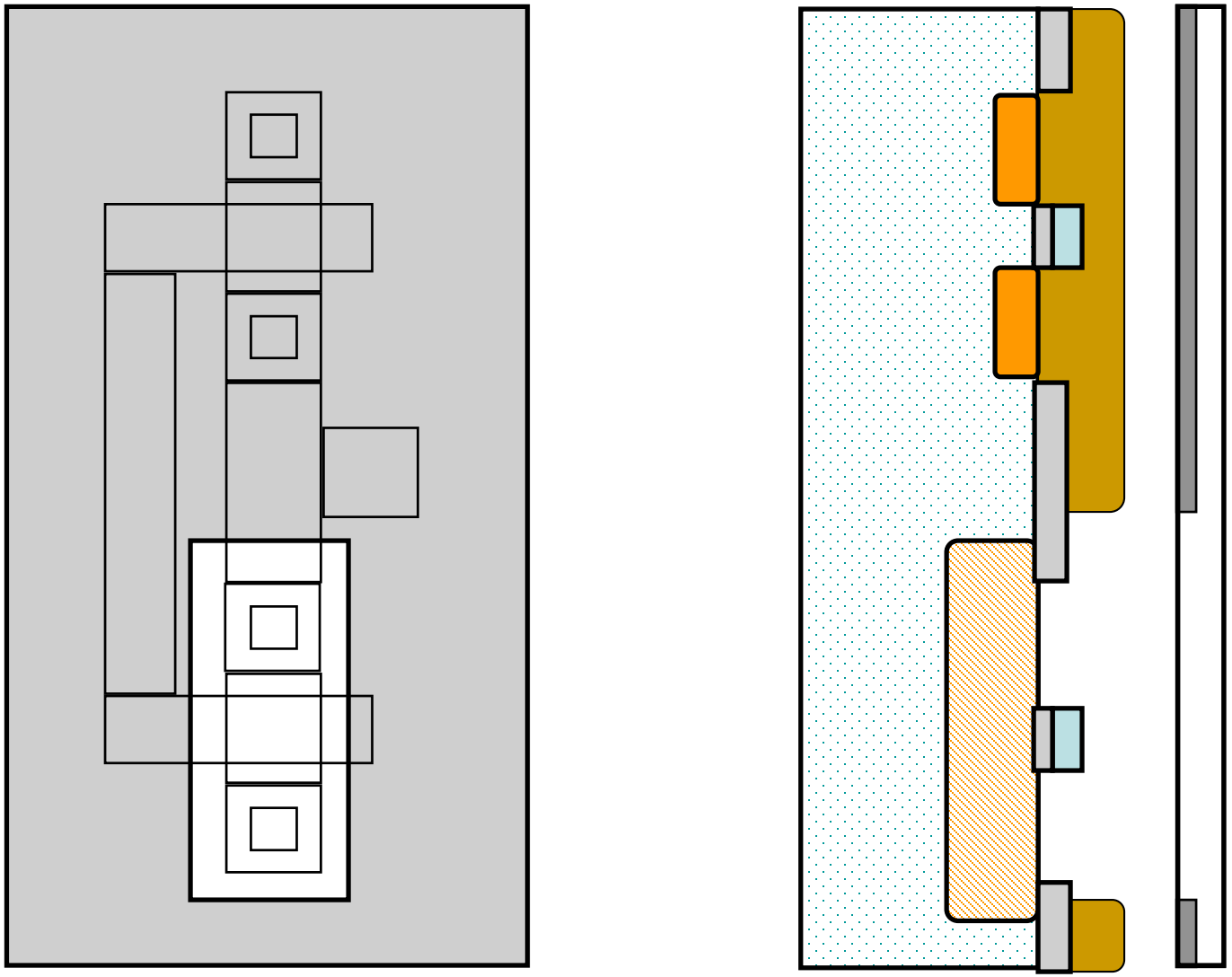




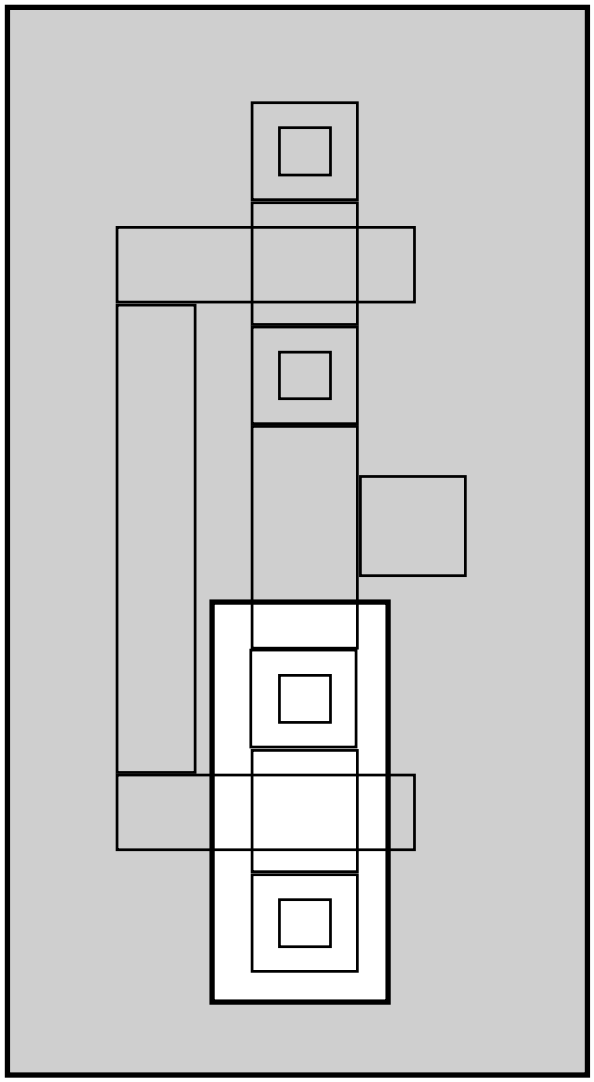
P-Select Mask (M5)

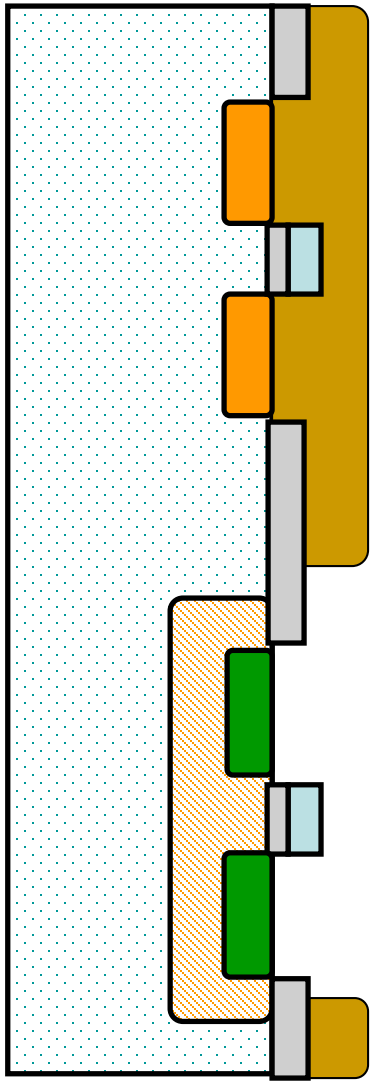


P-Select Mask (M5)

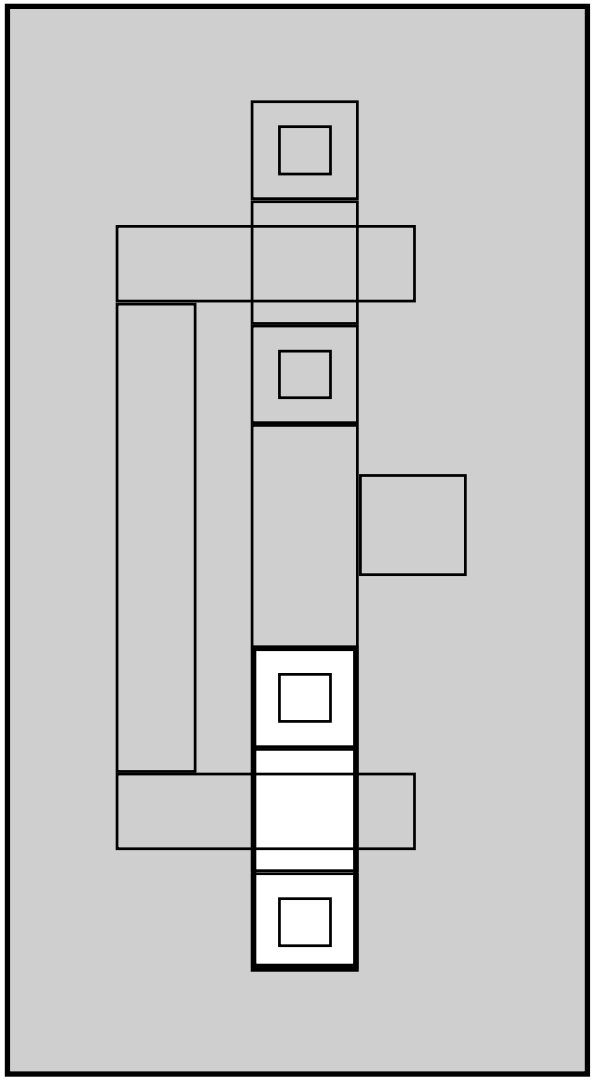


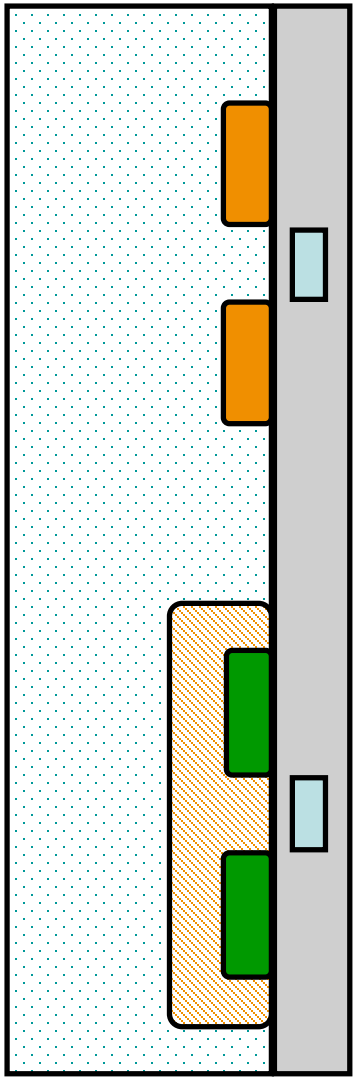
After M5, B^+ implant



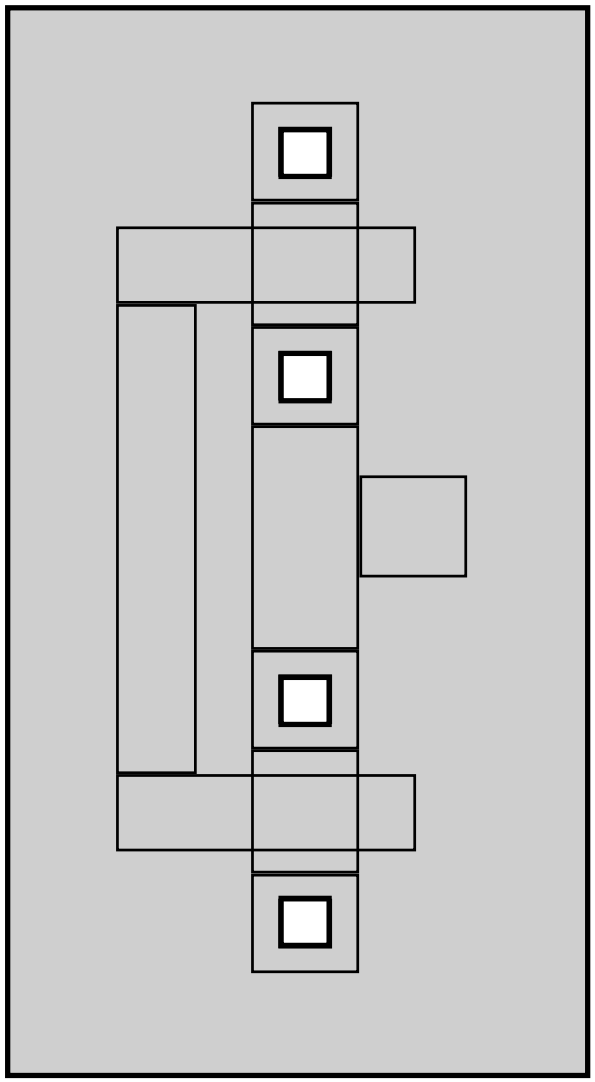


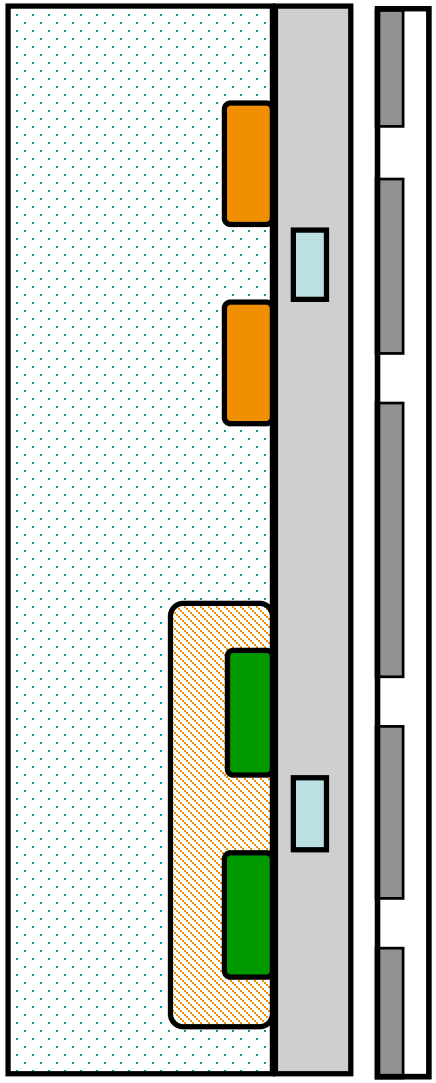
After M5, B^+ implant + drive-in



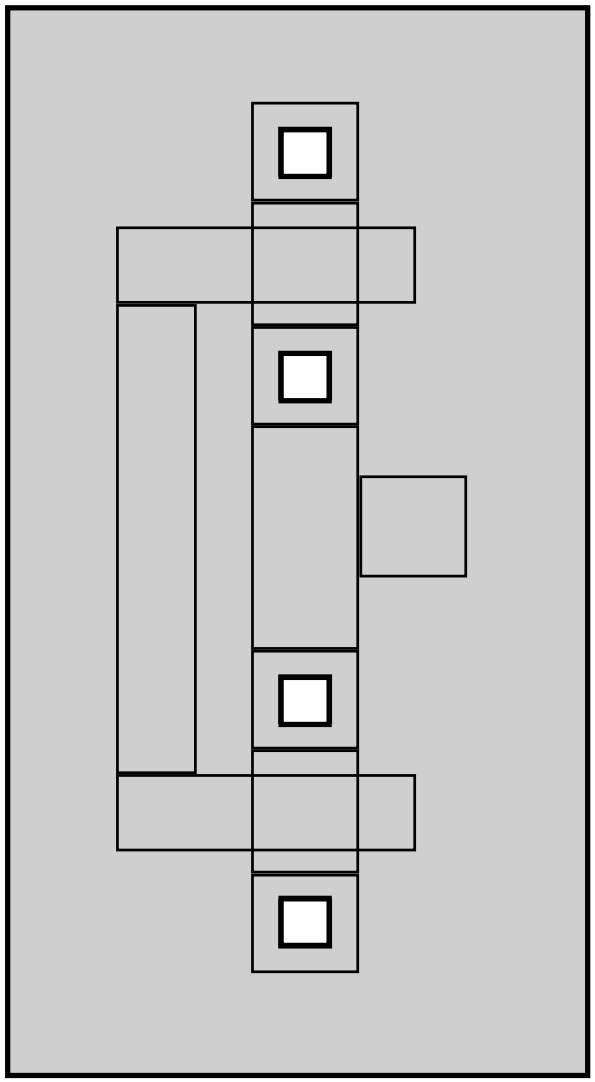


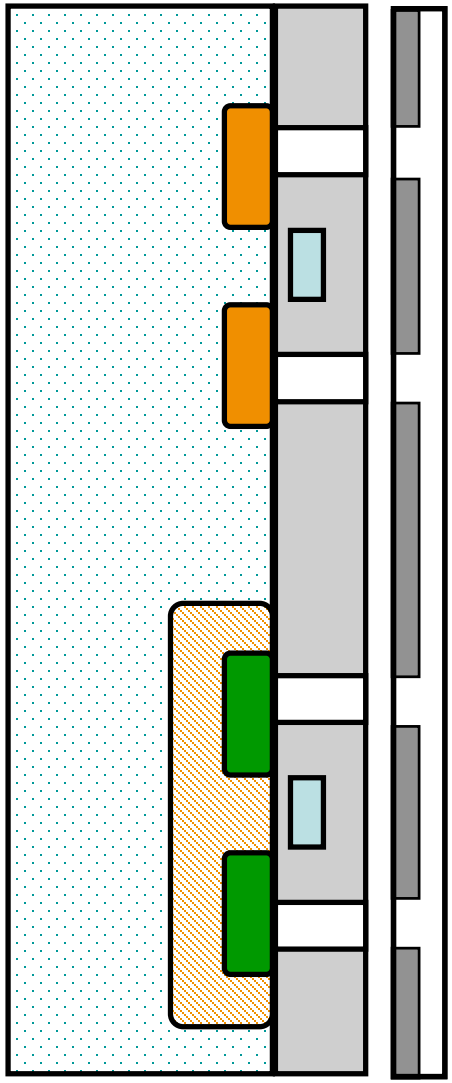
Contact Mask (M6)



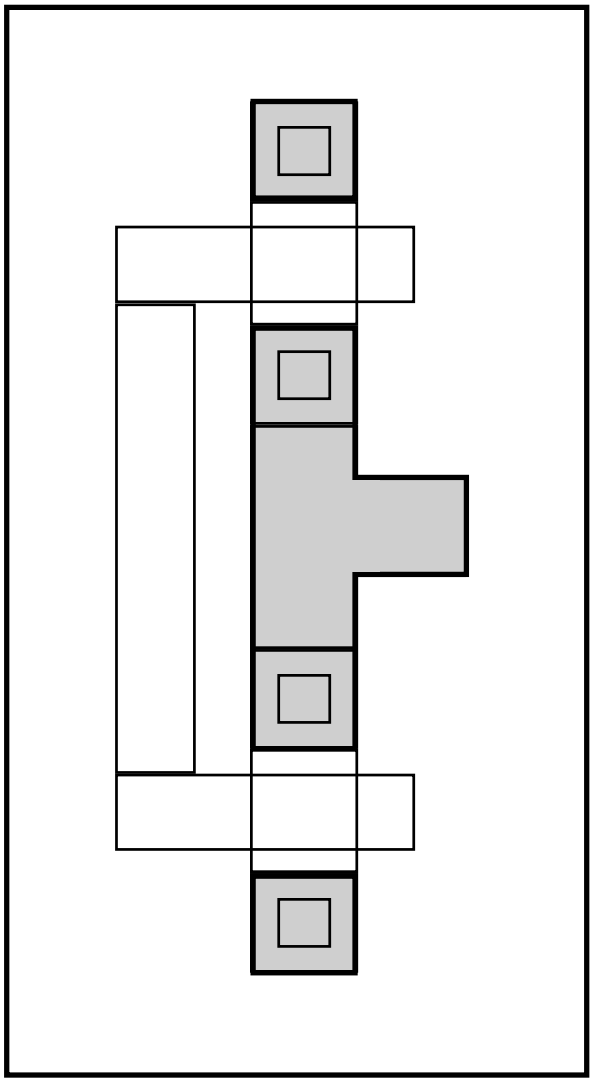


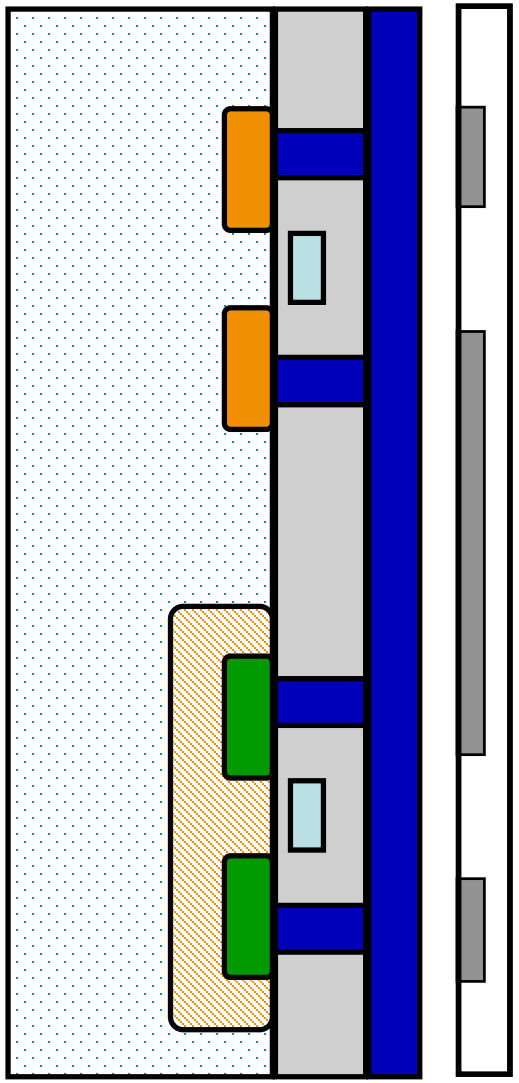
Contact Mask (M6)





Metal Deposit





Metal Mask (M7)