

MM54HC373/MM74HC373 TRI-STATE® Octal D-Type Latch

General Description

These high speed octal D-type latches utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are pres-

ent at the other inputs and the state of the storage elements.

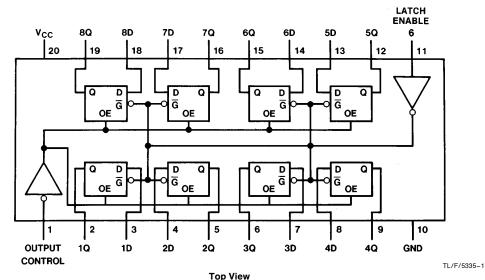
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{\rm CC}$ and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA maximum (74 Series)
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



Order Number MM54HC373 or MM74HC373

Truth Table

Output Control	Latch Enable	Data	373 Output
L	Н	Н	Н
L	Н	L	L
L	L	Х	Q_0
Н	Х	X	Z

H = high level, L = low level

Q₀ = level of output before steady-state input conditions were established.

Z = high impedance

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Absolute Maximum Ratings (Notes 1 & 2) If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) -0.5 to +7.0V DC Input Voltage (V_{IN}) -1.5 to $V_{CC} + 1.5V$ DC Output Voltage (V_{OUT}) -0.5 to $V_{CC} + 0.5V$ Clamp Diode Current (I_{IK}, I_{OK}) \pm 20 mA DC Output Current, per pin (I_{OUT}) $\pm\,35~\text{mA}$ DC V_{CC} or GND Current, per pin (I_{CC}) $\pm\,70~mA$ Storage Temperature Range (T_{STG}) -65°C to $+\,150^{\circ}\text{C}$

Power Dissipation (PD)

(Note 3) 600 mW 500 mW S.O. Package only 260°C

Lead Temp. (T_L) (Soldering 10 seconds)

Operating Conditi	Ulio		
	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage (V _{IN} ,V _{OUT})	0	V_{CC}	V
Operating Temp. Range (T _A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times			
(t_{r}, t_{f}) $V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

Operating Conditions

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC}	T _A =25°C		74HC T _A = -40 to 85°C	54HC T _A = -55 to 125°C	Units
				Тур		Guaranteed		
V_{IH}	Minimum High Level Input Voltage		2.0V 4.5V 6.0V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V V V
V _{IL}	Maximum Low Level Input Voltage**		2.0V 4.5V 6.0V		0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V V V
V _{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT} \le 20 \mu A$	2.0V 4.5V 6.0V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V V V
		$V_{IN} = V_{IH}$ or V_{IL} $\left I_{OUT}\right \le 6.0$ mA $\left I_{OUT}\right \le 7.8$ mA	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V V
V _{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \le 20 \mu A$	2.0V 4.5V 6.0V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V V V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \le 6.0$ mA $ I_{OUT} \le 7.8$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V
I _{IN}	Maximum Input Current	V _{IN} =V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μΑ
loz	Maximum TRI-STATE Output Leakage Current	$V_{IN} = V_{IH}$ or V_{IL} , $OC = V_{IH}$ $V_{OUT} = V_{CC}$ or GND	6.0V		±0.5	±5	±10	μΑ
lcc	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	μΑ

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

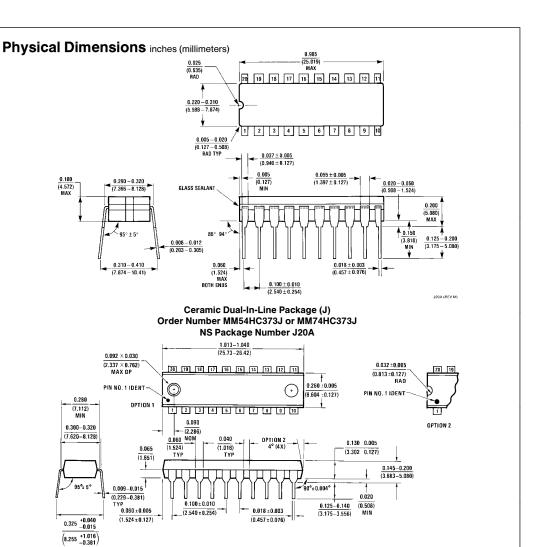
^{**}V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics V _{CC} =5V, T _A =25°C, t _r =t _f =6 ns								
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units			
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Data to Q	C _L =45 pF	18	25	ns			
t _{PHL} , t _{PLH}	Maximum Propagation Delay, LE to Q	C _L =45 pF	21	30	ns			
t _{PZH} , t _{PZL}	Maximum Output Enable Time	$R_L = 1 k\Omega$ $C_L = 45 pF$	20	28	ns			
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$ $C_L = 5 pF$	18	25	ns			
t _S	Minimum Set Up Time			5	ns			
t _H	Minimum Hold Time			10	ns			
t _W	Minimum Pulse Width		9	16	ns			

$\textbf{AC Electrical Characteristics} \ \ V_{CC} = 2.0 - 6.0 \ V, \ C_L = 50 \ pF, \ t_r = t_f = 6 \ ns \ (unless \ otherwise \ specified)$

Symbol	Parameter	Conditions	Vcc	T _A =25°C		74HC T _A = -40 to 85°C	54HC T _A = -55 to 125°C	Units
				Тур		Guaranteed		
t_{PHL} , t_{PLH}	t _{PHL} , t _{PLH} Maximum Propagation Delay, Data to Q		2.0V 2.0V	50 80	150 200	188 250	225 300	ns ns
		$C_L = 50 \text{ pF}$ $C_L = 150 \text{ pF}$	4.5V 4.5V	22 30	30 40	37 50	45 60	ns ns
		$C_L = 50 \text{ pF}$ $C_L = 150 \text{ pF}$	6.0V 6.0V	19 26	26 35	31 44	39 53	ns ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay, LE to Q	$C_L = 50 \text{ pF}$ $C_L = 150 \text{ pF}$	2.0V 2.0V	63 110	175 225	220 280	263 338	ns ns
		$C_L = 50 \text{ pF}$ $C_L = 150 \text{ pF}$	4.5V 4.5V	25 35	35 45	44 56	52 68	ns ns
		$C_L = 50 \text{ pF}$ $C_L = 150 \text{ pF}$	6.0V 6.0V	21 28	30 39	37 49	45 59	ns ns
t _{PZH} , t _{PZL}	Maximum Output Enable Time	$R_L = 1 k\Omega$ $C_L = 50 pF$ $C_L = 150 pF$	2.0V 2.0V	50 80	150 200	188 250	225 300	ns ns
		C _L = 50 pF C _L = 150 pF	4.5V 4.5V	21 30	30 40	37 50	45 60	ns ns
		$C_L = 50 \text{ pF}$ $C_L = 150 \text{ pF}$	6.0V 6.0V	19 26	26 35	31 44	39 53	ns ns
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$ $C_L = 50 pF$	2.0V 4.5V 6.0V	50 21 19	150 30 26	188 37 31	225 45 39	ns ns ns
ts	Minimum Set Up Time		2.0V 4.5V 6.0V		50 9 9	60 13 11	75 15 13	ns ns ns
t _H	Minimum Hold Time		2.0V 4.5V 6.0V		5 5 5	5 5 5	5 5 5	ns ns ns
t _W	Minimum Pulse Width		2.0V 4.5V 6.0V	30 10 9	80 16 14	100 20 18	120 24 20	ns ns ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time	C _L =50 pF	2.0V 4.5V 6.0V	25 7 6	60 12 10	75 15 13	90 18 15	ns ns ns
C _{PD}	Power Dissipation Capacitance (Note 5)	(per latch) OC=V _{CC} OC=GND		30 50				pF pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF
C _{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC} \ V_{CC}$, and $I_S = C_{PD} \ V_{CC} \ f + I_{CC} \ V_{CC} \ f + I_{CC}$



Molded Dual-In-Line Package (N) Order Number MM74HC373N NS Package Number N20A

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