Revision A4 may be identified by the date/revision brand yywwA4, where yy and ww are the year and workweek of manufacture, respectively. This errata sheet is valid only when used in conjunction with the most current version of the data sheet available from Dallas Semiconductor via the Internet.

This document contains the following types of information:

Errata: These are design errors which deviate from published specifications. Errata are intended to be fixed in subsequent revisions of the device.

Specification Modifications: These are changes to the published specifications and will be reflected in the next update of the documentation and apply to all subsequent revisions of the device.

Documentation Changes: This information includes typographical mistakes, errors, omissions or clarifications of device operation. Items listed in this section will be reflected in the next update of the documentation.

ERRATA

1. The Stop mode current with the band gap reference disabled is typically 1 μA or less over the entire temperature range. On a few devices, however, it may be as high as 25μA at 25 degrees C, 100μA at 70 degrees C or 150μA at 85C.

   The Stop mode current with the band gap reference enabled is typically 50μA or less over the entire temperature range. On a few devices, however, it may be as high as 95μA at 25 degrees C, 170μA a 70 degrees C or 195μA at 85C.

2. The PSEN\ pin toggles regardless of whether internal or external program memory is used. The function description of this pin indicates that it should be inactive during internal program execution.
   Work Around: None.

3. The broadcast address portion of either serial port's address mode does not function. All other aspects of this mode work properly.

   Work Around: Use the "Given Address" (SADDR masked by SADEN) to create a group that may be addressed separately or as a unit.

4. SPTA0 and SPRA0 bits may not show the correct state if a write to SCON0 is performed during reception or transmission of a character on serial port 0. Also, SPTA1 and SPRA1 bits may not show the correct state if a write to SCON1 is performed during reception or transmission of character on serial port 1.

   Work Around: Prior to writing to either SCON, verify that there is no activity on the serial port by reading the appropriate SPTA and SPRA bits.

5. At voltages below 4.25V, serial ports 0 and 1 operating in modes 1, 2, or 3 may not properly detect a false start bit, causing the device to erroneously detect the start of a serial reception.

Work Around: Operate the device V_{CC} as close as possible to 5.0V.

6. The serial port operating in mode 0 may violate the t_{QVXL} spec when the external crystal speed is above 25 MHz.

   Work Around: Use the rising edge only of the clock to latch output data if the external crystal speed is above 25 MHz.

7. The device may erroneously set one or more EPROM lock bits when exiting In-System Disable (ISD) mode. This could cause a device with an unlocked EPROM to become locked.

   Work Around: None.

8. In In-System Disable (ISD) mode, ALE and PSEN\ are pulled low. The functional description of these pins in this mode states they should be held weakly high.

   Work Around: None.

9. Modifying the Clock Control Register (CKCON; 8Eh) while the watchdog timer is enabled can advance the watchdog time count by a random amount. This could result in an inaccurate watchdog timer period. This will not occur if the current watchdog time-out period is already set to its maximum count (WD1:0=11; CKCON7:6).

   Work Around: If the watchdog timer is enabled, reset the watchdog timer via the RWT bit (WDCON.0) before accessing the CKCON register. This will prevent an unexpected early time-out of the watchdog timer.

10. SPTA0 does not correctly indicate serial port 0 transmit activity if a character is written to SBUF0 while TI_0 is high. Also, SPTA1 does not correctly indicate serial port 1 transmit activity if a character is written to SBUF1 while TI_1 is high.

    Work Around: When managing transmission by polling the SPTA bits, clear the appropriate TI bit before writing each character to the SBUF.

11. When any reset occurs during the execution of an extended MOVX data memory access, most instructions located at 0000h can fail to execute correctly. The exception is the LCALL instruction, mentioned below. In each case the failure causes the program to incorrectly execute the first several machine cycles of the affected instruction(s).

    Work Around: Use the instruction LCALL at location 0000h (the reset vector) to jump to the starting point of the main user code. This will use two bytes of the stack, which can be easily restored if necessary by resetting the stack pointer.

12. When a short reset stimulus occurs during the execution of an extended MOVX data memory access, the ALE signal may not be driven with the strong transition drivers (V_{OH2} test levels) on the first instruction fetch following reset. This reduced drive current may not allow the ALE signal to rise to a logic high level before the first instruction fetch at location 0000h, possibly latching an incorrect address. This situation will only occur during a watchdog timer reset (the timer generates a momentary pulse to the internal reset circuitry) or when an external reset pulse of less than 2 μs is asserted. This errata does not affect a power-on reset as the internal crystal warm-up period counter provides a reset pulse of greater than 2 μs.

    Work Around: If the watchdog timer reset function is employed, use the watchdog timer interrupt to ensure that the device will not be executing MOVX instructions when the watchdog timer reset occurs. If an external reset stimulus is used, be sure that it is at least 2 μs in duration.

SPECIFICATION MODIFICATIONS

1. NONE

DOCUMENTATION CHANGES

1. A typographical error in the data book states that an interrupt will be blocked if the current instruction is an access to IP, IE, EIP or EIE. The corrected version should state that interrupts will only be blocked if the current instruction writes to one of those registers.

    Work Around: None. This clarification does not represent a change in the functional characteristics of the device.