SGS-THOMSON MICROELECTRONICS

AN905
APPLICATION NOTE

SGS-THOMSON SOLUTION FOR ANALOG PORTS IN REMOTE APPLICATIONS BASED ON L3037 AND ST5088

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1. INTRODUCTION

With higher diffusion of digital and radio transmission the need to connect analog telephone with the ISDN network (TA applications) or radio access network (WLL application) is more and more evident.

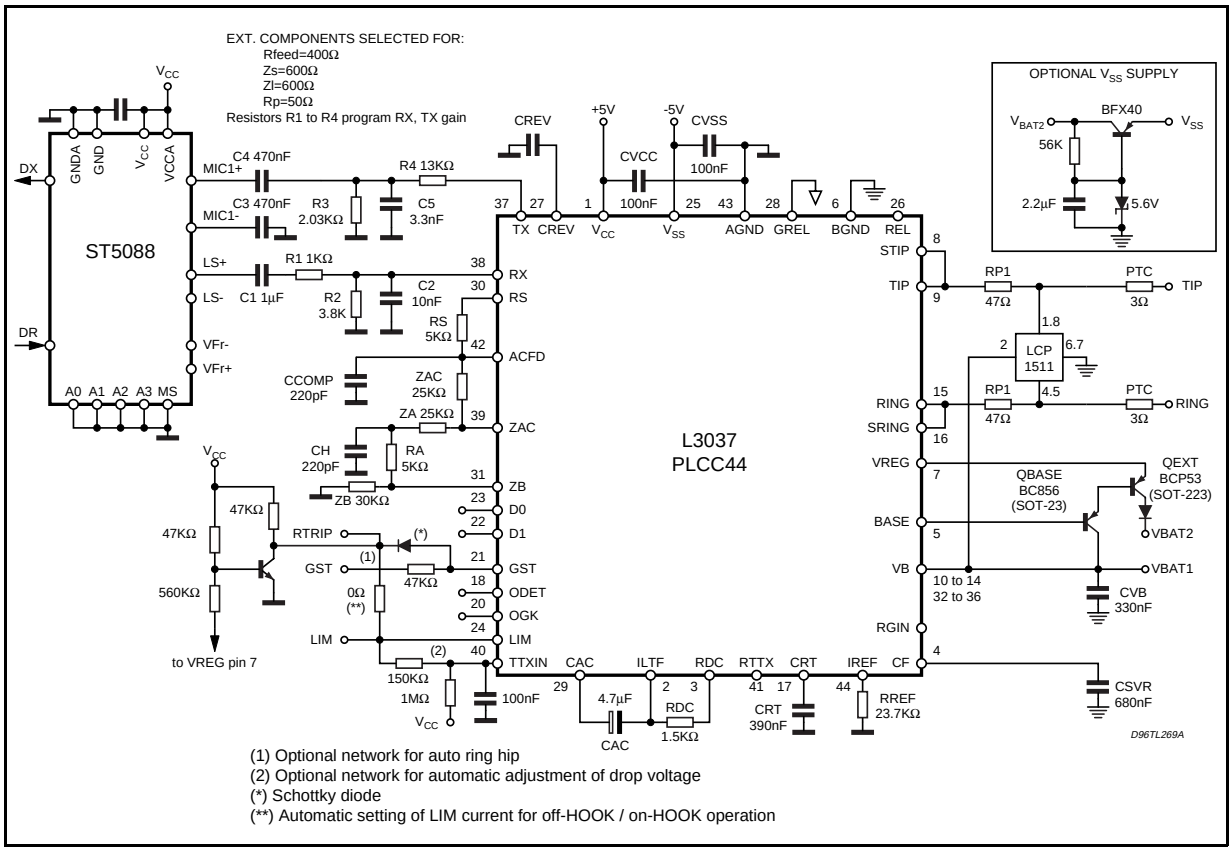
Using the SGS-Thomson ST5088 (Programmable ISDN Analog Front End), a few external components and the monochip slic L3037 in integrated ringing configuration it is possible to obtain a complete circuit optimised for this type of application.

One of the particular advantages in using the ST5088 instead of a standard codec/filter is the possibility to use the device built in tone generator to provide all the typical tones needed in the standard analog port signalling. Moreover, by proper programming , the ST5088 can be used also to perform the CLID (CAller IDentifier) function.

Another advantage of ST5088 is its flexibility, in fact it is possible to control the device both in GCI (IOM-2) mode or uW (serial control + PCM) mode.

2. INTERFACING ST5088 WITH L3037

Figure 1. ST5088 + L3037 typical application diagram



In this chapter is described a particular configuration that will guarantee a TX gain programmability in a 15dB range with 1dB step and a RX gain programmability in a 30dB range with 2dB step. Particular attention is dedicated to the interface between ST5088 and L3037. For more information on ST5088 see the device datasheet and the next chapters (4 and 5)

Concerning the other L3037 external components please refer to the L3037 datasheet and to the next paragraphs (6 and 7) describing the integrated ringing and dual battery applications.

Due to the fact that very often in this type of systems the -5V supply is not present fig.1 shows also a very simple circuit that allow to generate the -5V supply needed by the L3037 directly from the negative battery (this is possible thanks to the L3037 very low current consumption from Vss) .

2.1 TX coupling

Referring to fig.1 it is possible to see how the TX signal coming from L3037 is transferred to ST5088. In particular the TX signal is applied to the MIC1+ input of ST5088 via a C4 (470nF) decoupling capacitor. The other MIC1- input should be connected to GND with an equivalent decoupling capacitor C3 (470nF).

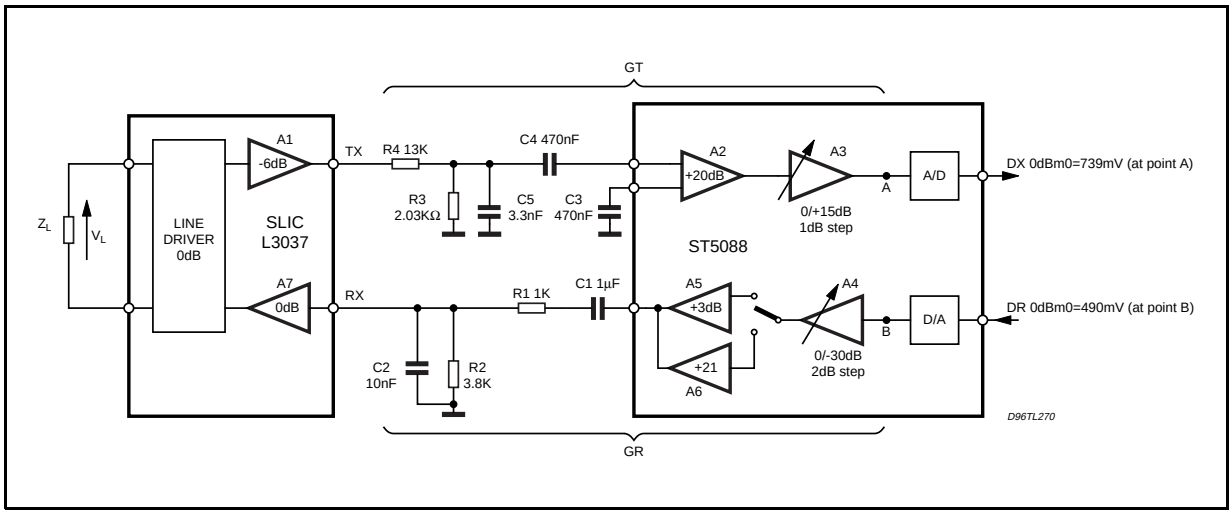
R3 and R4 resistors are used to properly adjust the L3037 TX output level to the ST5088 MIC1+ input dynamic range. In addition a C5 capacitor is used to implement a first order low pass filter to reduce possible pick up noise (f_T should be in the range of 30KHz).

2.2 RX coupling

The RX signal generated by the ST5088 is transferred to the L3037 RX input from the LS+ output. C1 (1µF) is used for decoupling, R1, R2 are used to adjust the signal level and C2 is implementing a first order low pass filter in order to reduce eventual out of band noise (f_T should be in the range of 20KHz).

3. ST5088 L3037 OVERALL GAIN SETTINGS

Figure 2. ST5088 + L3037 RX, TX gains path



3.1 TX gain setting

Fig.2 shows the signal path from the analog line VL to the transmit digital output DX.

The TX gain can be set choosing properly R3 and R4 and programming the A3 gain (for ST5088 programming see the device datasheet or par. 4). In order to achieve the best noise performances it is better to keep A3 in the low gain range (0 to 6dB).

Let's now see what are the different steps to be followed in order to set properly R3, R4 and A3:

1. Get the administration parameters: Zin (Slic 2wire input impedance or Return Loss reference impedance) and TX relative level expressed in dBr (that means the analog level applied at line terminals that should generate 0dBm0 level on the digital side).
2. Calculate the voltage level equivalent to 0dBm on the reference impedance Zin as:

   $Vo = \sqrt{(10^{-3} \cdot |Zin|_{@1KHz})}$
3. Define the voltage level required at line terminals converting properly the TX relative level from [dBr] to [V].
4. Define the voltage level at Slic TX output based on the Slic TX gain (-6dB in case of L3037)
5. Considering the A/D 0dBm0 reference (739mV) of the codec define GT as the analog gain between Slic TX output and codec A/D input (point A in fig.2). GT=20log(V(A)/V(TX)).
6. Select A3 to the minimum possible value considering eventual sw. gain adjustment possibility.
7. Based on A3 and A2 (fixed to +20dB) define the gain G(DIV) to be associated to the voltage divider R3, R4. G(DIV) = GT-A2-A3
8. Convert G(DIV) into linear $G(DIV)l_{lin}$ = 10(G(DIV)/20) and calculate R3 and R4:
   $R3 = (G(DIV)l_{lin}/(1-G(DIV)l_{lin}) \cdot R4$
9. Define C5 for f_T = 30KHz. $C5=1/(2 \cdot \pi \cdot f_T \cdot (R3//R4))$

Example:

1. Administration requirements: Zin=600ohm; TX rel. level = 0dBr
2. Vo = $\sqrt{(10^{-3} \cdot 600)} = 0.7746V$
3. VL = 0dBr = 0.7746V
4. V(TX) = 0.7746/2 = 0.3873
5. GT = 20log(0.739/0.3873) = 5.61dB
6. A3 = +3dB
7. G(DIV) = 5.61 - 20 - 3 = -17.39
8. $G(DIV)|_{lin} = 10^{-(17.39/20)} = 0.135$ R3 = (0.135/0.865) · R4; supposing R4=13K, R3=2.03K.
9. $C5 = 1/(2 \cdot \pi \cdot 30 \cdot 10^3 \cdot (1756)) = 3.02nF$ (C5 = 3.3nF)

3.2 RX gain setting

Fig.2 shows the signal path from the digital input DR and the analog line VL.

The RX gain can be set choosing properly R1 and R2, selecting A5 or A6 amplification path and programming the A4 gain (for ST5088 programming see the device datasheet or par. 4). In order to achieve the best noise performances it is better to use the A5 amplification path and program A4 in the high gain range (0 to -6dB).

Let's now see what are the different steps to be followed in order to set properly R1, R2 and A4:

1. Get the administration parameters: Zin (Slic 2wire input impedance or Return Loss reference impedance) and RX relative level expressed in dBr (that means the analog level that will appear at line terminals when a 0dBm0 level is applied on the digital side).
2. Calculate the voltage level equivalent to 0dBm on the reference impedance Zin as:
   $Vo = \sqrt{(10^{-3} \cdot |Zin|_{@1KHz})}$
3. Define the voltage level required at line terminals converting properly the RX relative level from [dBr] to [V].
4. Define the voltage level at Slic RX input based on the Slic RX gain (0dB in case of L3037).
5. Considering the D/A 0dBm0 reference (490mV) of the codec define GR as the analog gain between Slic RX input and codec D/A output (point B in fig.2).
   GR=20log(V(RX)/V(B)).
6. Choose A5 or A6 depending on the maximum required RX relative level (A5 should be preferred). Program A4 to the maximum possible value considering eventual sw. gain adjustment possibility. Based on A4, A5 (+3dB) or A6 (+21dB) define the gain G(DIV) to be associated to the voltage divider R1, R2. G(DIV) = GR-A4-A5 (if A5 is selected).
7. Convert G(DIV) into linear $G(DIV)|_{lin}$=10(G(DIV)/20) and calculate R1 and R2:
   $R2=(G(DIV)|_{lin}/(1-G(DIV)|_{lin})) \cdot R1$
8. Define C2 for f_T = 20KHz. $C2=1/(2 \cdot \pi \cdot f_T \cdot (R1//R2))$

Example:

1. Administration requirements: Zin=600ohm; RX rel. level = -3dBr
2. Vo = $\sqrt{(10^{-3} \cdot 600)} = 0.7746V$
3. V_L = 0dBr = $0.7746 \cdot 10^{(-3/20)} = 0.5484V$
4. V(RX) = 0.5484V
5. GR = 20log(0.5484/0.490) = 0.98dB
6. A5 = +3dB; A4 = 0dB
7. G(DIV) = 0.98 - 0 - 3 = -2.02dB
8. $G(DIV)|lin = 10^{-(2.02/20)} = 0.7925$ R2 = (0.7925/0.2075) · R1; supposing R1=1K, R2=3.82K
9. $C2 = 1/(2 \cdot \pi \cdot 20 \cdot 10^3 \cdot (791)) = 10nF$

4. ST5088 BASIC PROGRAMMING

ST5088 provides a choice of either of two types of Digital Interface for both control data and PCM:

- for compatibility with systems which use time slot oriented PCM busses with a separate microwire Control Interface, as used on COMBO I/II families of devices;
- for systems in which PCM and control data are multiplexed together using GCI interface scheme

ST5088 will automatically switch to one of these two types of interface by sensing the MS pin.

4.1MICROWIRE CONTROL INTERFACE

Control information or data is written into or read-back from ST5088 via the serial control port consisting of control clock CCLK, serial data input CI and output CO, and Chip Select input, CS. All control instructions require 2 bytes as listed in Table 1 of the ST5088 datasheet, with the exception of a single byte power-up/down command.

To shift control data into ST5088, CCLK must be pulsed high 8 times while $\overline{CS}$ is low. Data on CI input is shifted into the serial input register on the rising edge of each CCLK pulse. After all data is shifted in, the content of the input shift register is decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide CS pulse or may follow the first contiguously, i.e. it is not mandatory for CS to return high in between the first and second control bytes. At the end of the 2nd control byte, data is loaded into the appropriate programmable register. CS must return high at the end of the 2nd byte.

To read-back status information from ST5088, the first byte of the appropriate instruction is strobed in during the first CS pulse, as defined in Table 1. CS must be set low for a further 8 CCLK cycles, during which data is shifted out of the CO pin on the falling edges of CCLK.

When $\overline{CS}$ is high, CO pin is in the high impedance Tri-state, enabling CO pins of several devices to be multiplexed together. Thus, to summarise, 2 byte READ and WRITE instructions may use either two 8-bit wide CS pulses or a single 16 bit wide CS pulse.

4.2 GCI COMPATIBLE MODE

The frame is structured at the GCI interface into two 256 kbit/s channel:

a) GCI channel 0: It is structured in four sub-channels:

- B1 channel 8 bits per frame
- B2 channel 8 bits per frame
- M channel 8 bits per frame ignored by ST5088
- SC channel 8 bits per frame ignored by ST5088

Only B1 or B2 channel can be selected in ST5088 for PCM data transfer.

b) GCI channel 1: It is structured also in four subchannels:

- B1* channel 8 bits per frame
- B2* channel 8 bits per frame
- M* channel 8 bits per frame
- SC* which is structured as follows:
  - 6 bits ignored by ST5088
  - A* bit associated with M* channel
  - E* bit associated with M* channel.

B1* or B2* channel can be selected in ST5088 for PCM data transfer. M* channel and two associated bits E* and A* are used for ST5088 control.

Thus, to summarise, B1, B2, B1* or B2* channel can be selected to transmit PCM data and M* channel is used to read/write status/command peripheral device registers. Protocol for byte exchange on the M* channel uses E* and A* bits.

The interface is physically constituted with 4 wires:

Input Data wire: DR

Output Data wire: DX

Bit Clock: MCLK

Frame Synchronisation: FS

Data is synchronised by MCLK and FS clock inputs.

Protocol allows a bi-directional transfer of bytes between ST5088 and GCI controller with acknowledgement at each received byte. For ST5088, standard protocol is simplified to provide read or write register cycles almost identical to MICROWIRE serial interface.

During a Write cycle unit sends through the GCI controller the following bytes:

- First byte is the chip select byte. The first four bits indicate the device address: (A3,A2,A1,A0). The four last bits are ignored. ST5088 compare the validated byte received internally with the address defined by pins A3, A2, A1, A0. If comparison is true, byte is acknowledged, if not, ST5088 does not acknowledge the byte.
- Second byte is structured as defined in Table 1 of the ST5088 Datasheet.
- Third byte is the Data byte to write into the Register.

It is possible but optional to write to several different registers in a single message. In this case the Chip Select byte is sent only once at the beginning of the message, the device automatically toggles between address byte and data byte.

The full protocol for byte exchange on the M* channel using E* and A* bits is described in details in the ST5088 Datasheet.

5. CALLER ID IMPLEMENTATION WITH ST5088

One and Zero symbols of a Caller Identification (CLID) message are translated as listed below, following the ITU_T V.23 recommendation at 1200bps:

FX = 1300 Hz (symbol 1, mark)

FY = 2100 Hz (symbol 0, space)

Tolerance for FX and FY is +/- 10 Hz.

Two methods are available for toggling between two frequencies with ST5088:

- using one ST5088 tone generator and changing the desired frequency each time by writing an 8-bit value in either register CR8 or register CR9, depending on which of the two tone generators has been enabled;
- programming the two frequencies in the two tone generators only once and then enabling the desired generator and muting the other one as required. Switching between the two generators can be done either by writing 01 or 10 in bits 3:2 of register CR7 via software or by toggling the AT pin voltage between Vcc and GND, as described in the ST5088 Datasheet.

Unfortunately toggling between two different generators, as done in the latter method, does not preserve phase integrity at switching instants, which is necessary for correct detection of CLID tones. This excludes external control via the AT pin and demands the use of a microcontroller in order to program register CR8 (generator no. 1) or CR9 (generator no. 2) with the desired frequencies, as described in the former method.

The worst case in terms of CPU load is when it has to send at 1200 bps alternatively ...0101010101... bits. One bit is equal to 0.833 ms and it can be achieved only in microwire mode due to this timing constraint. In GCI mode in fact frame synchronisation constants prevent from attending the correct 0.833ms period, therefore caller ID can be implemented only adopting microwire control interface.

MICROWIRE CONTROL INTERFACE WITH ONE TONE GENERATOR

By adopting the microwire control interface and the one-tone generator method, two bytes (one for ADR and one for DAT) should be sent each time in order to program FX or FY in the selected tone generator. As no particular time constraints exist on the delay between each register write operation, the CPU can perfectly match the 0.833ms period constraint for 1200bps between two successive programmations.

The use of only one tone generator preserves phase integrity at switching instants, which is necessary for correct detection of CLID tones. This is the way the caller identification procedure has been implemented with ST5088.

Registers should be programmed as follows:

CR4 bit 3 = 1RTL switch closed

CR7 bits 3:2= 10Tone generator #1 enabled, #2 muted

CR8 bits 7:0= 53h 1296.875 Hz

= 87h 2109.375 Hz

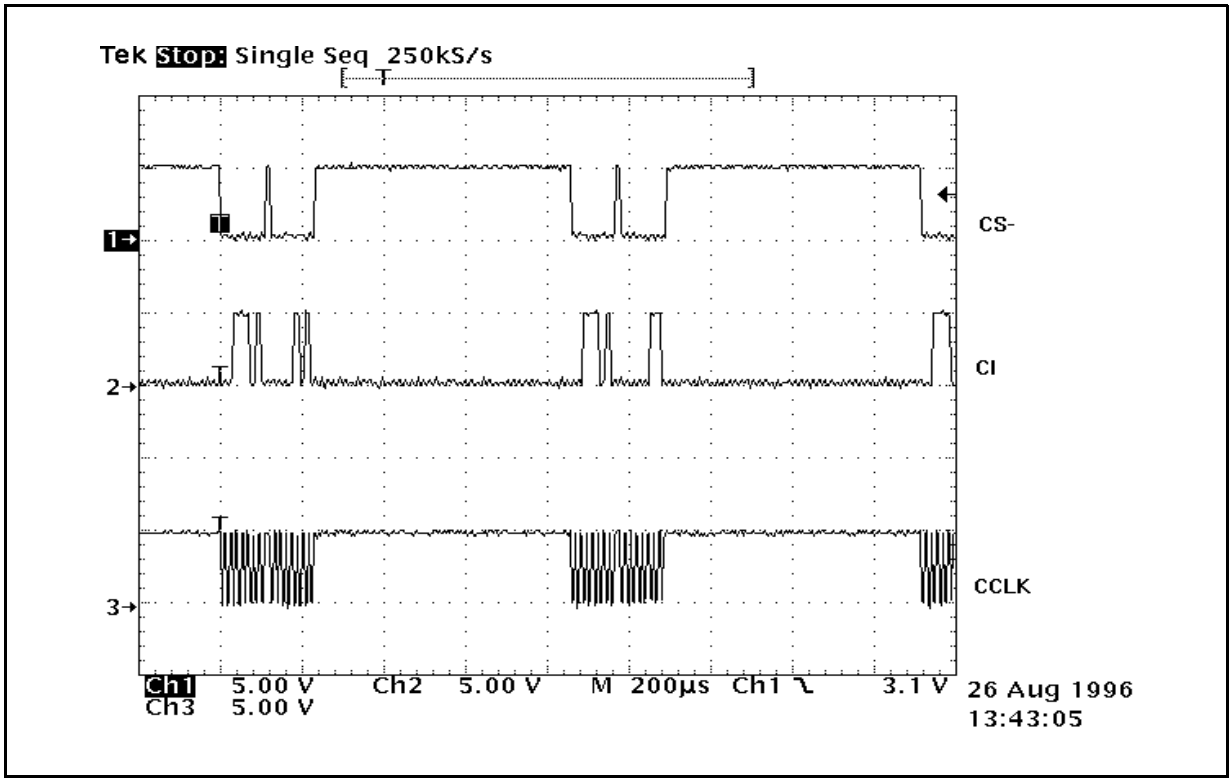
CR10 bits 1:0= 10Doubled range

By software every 0.833ms CR8 is programmed with 53h and 87h alternatively to produce the mark/space sequence. The 0.833ms timing can be achieved in several ways and depends only on the adopted CPU. With an ST9, for example, there is a wide choice of options, ranging from software NOP loops to timer or counter interrupt-driven routines.

Picture 1 shows the microwire interface signals used for programming register CR8.

Picture 2 shows the resulting waveform measured at LS+.

Picture 1. ST5088 microwire interface programmation signals



Picture 2. waveform at LS+

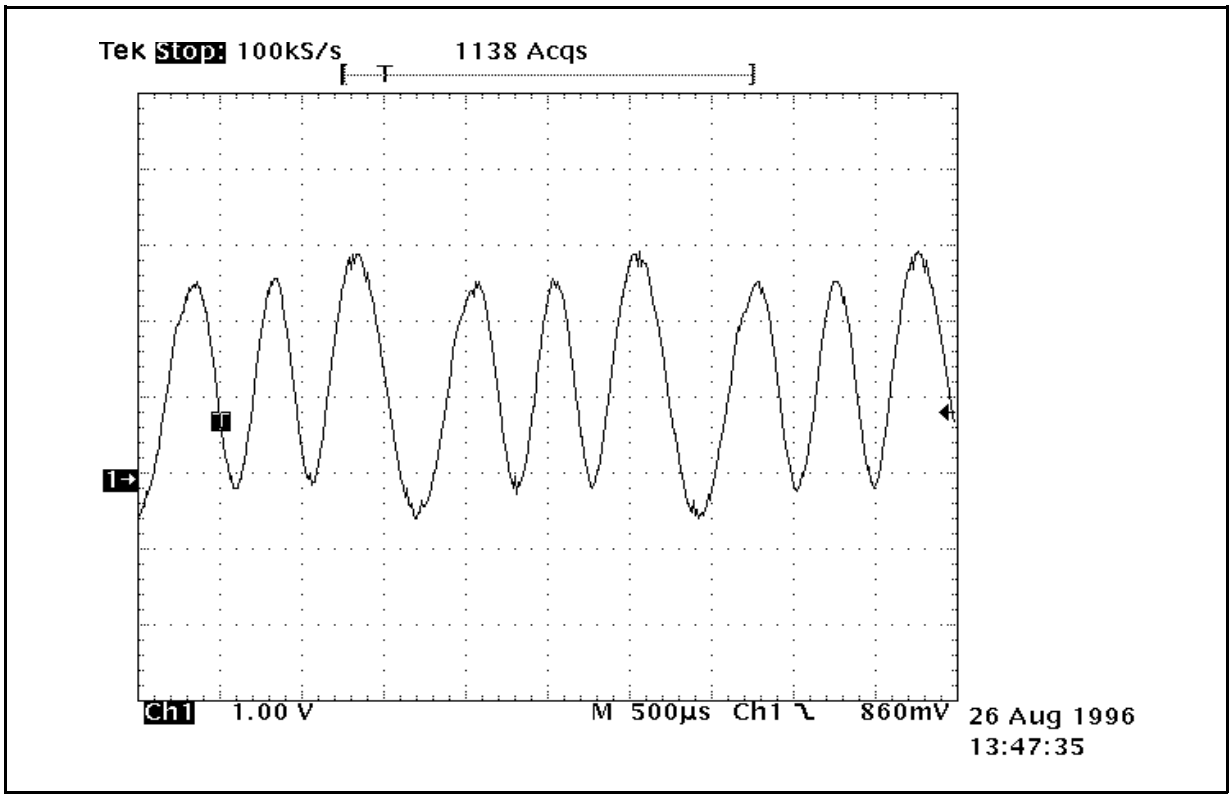
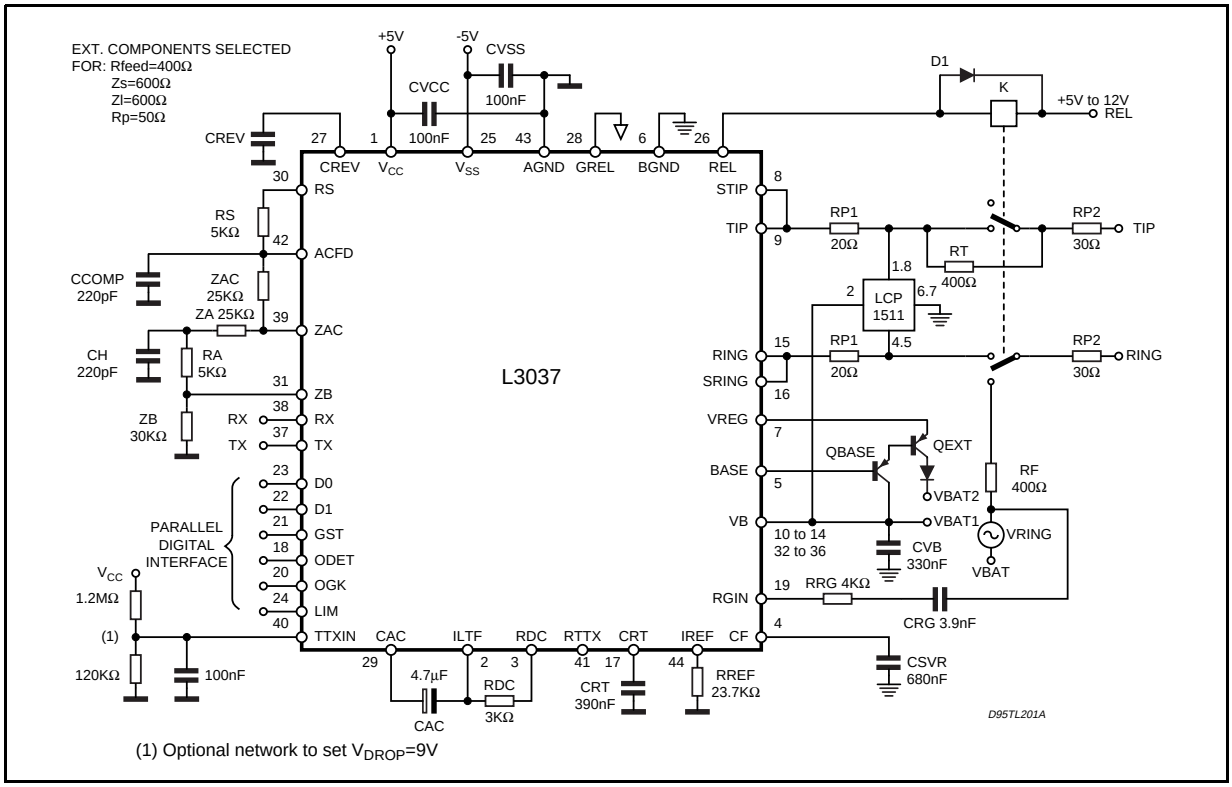


Figure 3. Typical Application Diagram for Dual Battery implementation.



6. DUAL BATTERY IMPLEMENTATION WITH L3037

In several application with short loop (FITL, Radio Access, Cable TV) it is necessary to show a proper On-Hook voltage (> 42.75V) and operate from a reduced battery in off-hook condition.

Main reason for this is to allow an overall limited power dissipation in all the operating modes.

When there is only one device per system the best way to achieve this function is to use a controlled DC/DC converter that generate the full battery voltage (on-hook) or a reduced battery voltage (off-hook) driven by the local microcontroller. It should be noted that the L3037 can operate properly with battery voltages down to -17V. In this case it is suggested to reduce the line voltage drop from the nominal 12V to 9V applying 645mV DC level to the TTXIN pin.

In case there is more than one device per system or it is not possible to guarantee that once in off-hook condition the loop resistance is always low enough to allow proper loop current also with the reduced battery it is necessary to implement a kind of automatic switching between two different battery voltages available in the system. The device will automatically select the full battery voltage in on-hook condition or in off-hook with long loops and the reduced battery when off-hook in presence of short loops.

Thanks to the internal architecture of the L3037 monochip SLIC this function can be easily implemented adding only one small signal transistor and one diode to the standard application diagram.

6.1 Functional description

When the line is in On-Hook condition, D1 is reverse biased and the loop current is provided by VBAT 1.

As soon as Off-Hook is detected the VREG voltage increase switching on the QEXT transistor and supplying the line from VBAT 2.

The switching from VBAT 1 to VBAT 2 is automatic and soft since the substrate supply voltage of the L3037 itself is never modified.

In particular supposing a current limit value set to 25 mA (LIM pin = 0) the loop current start to flow through VBAT 2 when the loop resistance decrease below Rth with:

$$R_{th} = \frac{V_{BAT2} - V_{drop}}{25mA} - 2Rp$$

Vdrop represents the difference between VBAT 1 and the open loop voltage.

When TTXIN=0, Vdrop =12V (see L3037 datasheet).

In this particular application in order to optimise the battery voltage value it is advisable to reduce the Vdrop to 9V (still allowing On-Hook transmission) applying a proper dc level to the TTXIN pin (645 mV)

When the line is On-Hook and no On-Hook transmission is needed, the L3037 should be set into Stand-by mode (Vdrop = 7V). For more information refer to L3037 datasheet.

Suggested external transistor types for SMD application are:

QBASE : BC 856 (SOT-23)

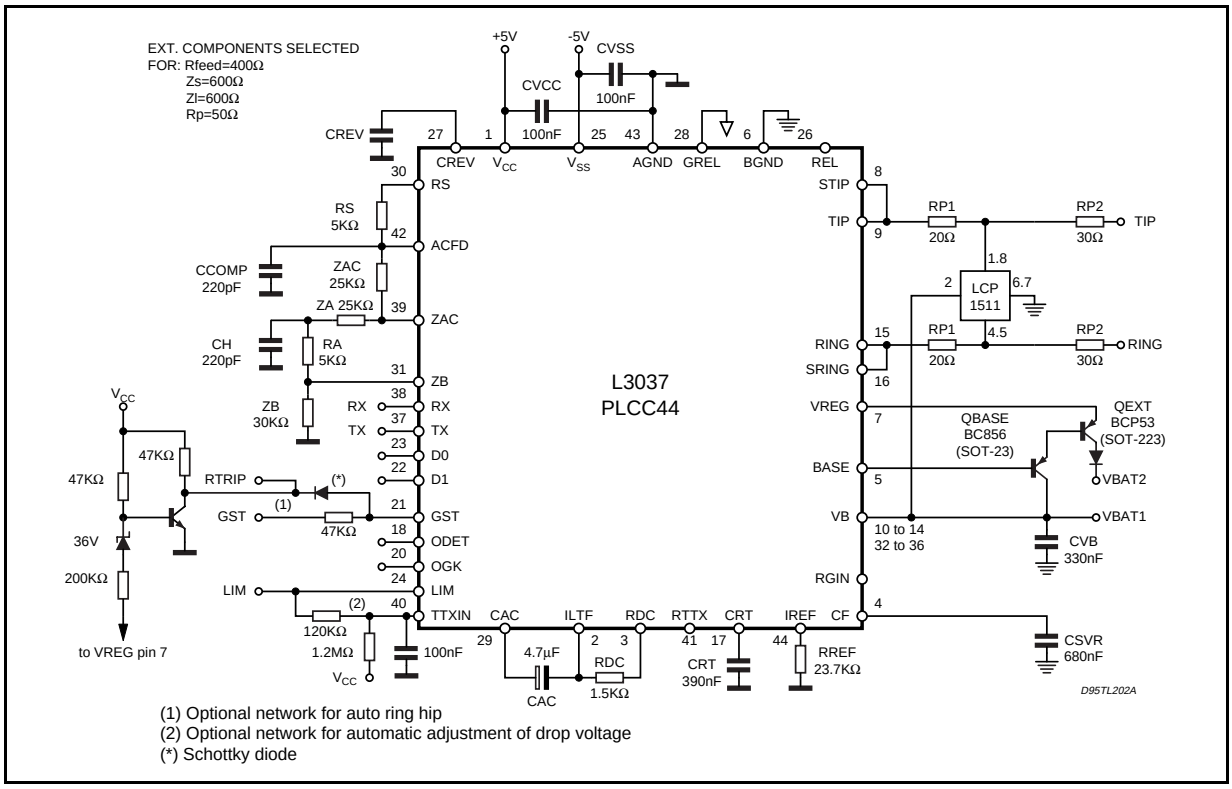
QEXT : BCP 53 (SOT-223)

Note: A BCP 53 transistor should be used for QBASE when RLOOP > Rth in order to allow proper power dissipation.

If the dual voltage supplies are not available a solution with a single transistor (standard application) can be used. In this case the power dissipation can be limited using a programmable V_{bat} supply that, when off-hook is detected, switches to a proper lower supply.

7. INTEGRATED RINGING IMPLEMENTATION WITH L3037

Figure 4. Typical Application Diagram for Ringing generation with L3037.



With the evolution of digital transmission the need to connect POTS to very short loop is increasing (Terminal Adapters, Radio Access, Cable TV, Extended NT applications).

This kind of applications normally require integrated ringing function.

SGS-Thomson is providing integrated Ringing SLIC solution since several years (L3000N/L3030 or L3000N/L3092), and now introducing L3000N/L3040.

Such solutions are fully compliant to public and private requirements in term of ringing amplitude and

distortion.

If amplitude and distortion requirements are not very severe a simpler integrated ringing solution can be provided with the L3037 monochip SLIC.

7.1 - Ringing injection with L3037

It is possible to generate a "trapezoidal" ringing signal just applying a proper 20Hz square wave (0 to 5V), duty cycle 50%, to the GST control pin of L3037.

In particular to set L3037 in integrated Ringing Mode the logic interface should be set as follow:

Ringing Mode - Logic interface

D0	D1	GST	LIM
1	0	20Hz square wave (0 to 5V)	1

The ringing frequency is the same of the one applied to the GST pin.

The ringing Crest Factor can be adjusted via CREV capacitor (see L3037 datasheet).

During ringing injection the ODET bit is not significative, the ring trip information is available at the RTRIP output (see Fig.4 - Typical Application Diagram for L3037 with integrated ringing).

This output, if properly connected to the GST input can be used to implement auto ring trip function, allowing automatic ring signal disconnection in presence of Off/Hook during ringing burst (typ. t RTRIP = 100 ms).

It should be noted that for proper Ring Trip detection RDC should be set to 1.5K ohm (typ.)

and RLOOP, including telephone set, should not exceed 500 ohm.

During ringing pause or after Ring Trip detection, the L3037 must be configured in Active Mode (25mA limitation current) that is:

Active Mode - Logic interface

D0	D1	GST	LIM
1	0	0	1

When the SLIC is set in active mode the off-hook information is carried out by the ODET pin.

Supposing that the metering pulse function is not needed (2Vrms TTX), the open loop voltage in both active and integrated ringing mode can be optimised applying a proper DC level to the TTX IN pin.

In particular a 645mV DC during active mode produces a 9V drop still allowing On-Hook

transmission.

During ringing the TTXIN pin voltage is further increased in order to provide the maximum dynamic to the ring signal.

In this case the voltage applied to the TTXIN pin is about 1.5V.

It should be noted that after Off-Hook, the L3037 switches automatically to a proper reduced battery voltage.

For more details on this function see paragraph 6 in this application note.

7.2 Typical measurements results

In the following table are shown the ringing level measured at Ringer terminal after 1000 feet loop (26AWG) with Vbat = -62V ; f = 20Hz for different REN numbers.

1 REN = 8µF + 6930 ohm.

CREV	CREST FACTOR	1 REN		3 REN		5 REN	
		Vpeak	Vrms	Vpeak	Vrms	Vpeak	Vrms
10nF	1.18	56.8V	48.0V	53.5V	46.0V	50.2V	44.0V
12nF	1.21	56.6V	46.5V	53.0V	45.0V	50.1V	43.0V
15nF	1.25	56.8V	45.5V	53.5V	44.0V	50.2V	42.0V
18nF	1.29	56.7V	44.0V	53.3V	42.5V	50.4V	41.0V
22nF	1.34	56.3V	42.0V	53.1V	40.0V	50.0V	38.2V

The following tables show the ringing and distortion level measured at Ringer terminal after 1000 feet loop for different ring frequency.

CREV	CREST FACTOR	1 REN		THD (f = 20Hz)
		Vpeak	Vrms	
10nF	1.18	56.8V	48.0V	28 %
12nF	1.21	56.6V	46.5V	26 %
15nF	1.25	56.8V	45.5V	20 %
18nF	1.29	56.7V	44.0V	15 %
22nF	1.34	56.3V	42.0V	9 %

CREV	CREST FACTOR	1 REN		THD (f = 25Hz)
		Vpeak	Vrms	
10nF	1.22	56.3V	46.0V	26 %
12nF	1.24	56.0V	45.0V	24 %
15nF	1.28	56.0V	43.5V	17 %
18nF	1.33	56.0V	42.0V	11 %
22nF	1.43	55.8V	39.0V	5 %