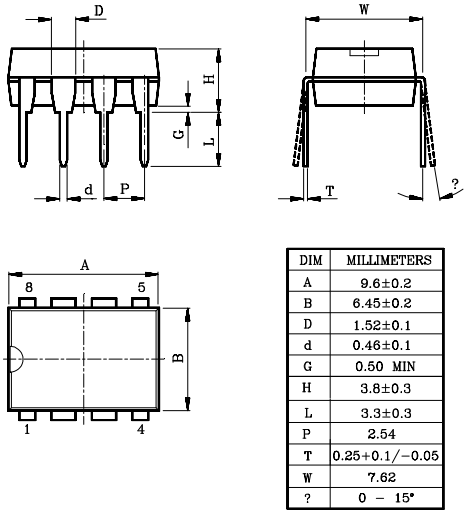
LOW POWER AUDIO AMPLIFIER

The KIA6419P/F is a low power audio amplifier integrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 volts minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80dB, and the closed loop gain is set with two external resistors. A chip disable pin permits powering down and/ or muting the input signal. The KIA6419 is available in a standard 8-pin DIP or a surface mount package.



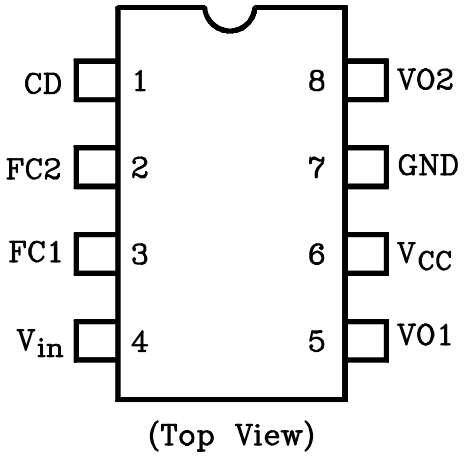

| DIM | MILLIMETERS |
|---|---|
| A | 9.6±0.2 |
| B | 6.45±0.2 |
| D | 1.52±0.1 |
| d | 0.46±0.1 |
| G | 0.50 MIN |
| H | 3.8±0.3 |
| L | 3.3±0.3 |
| P | 2.54 |
| T | 0.25+0.1/−0.05 |
| W | 7.62 |
| ? | 0 ~ 15° |

DIP-8

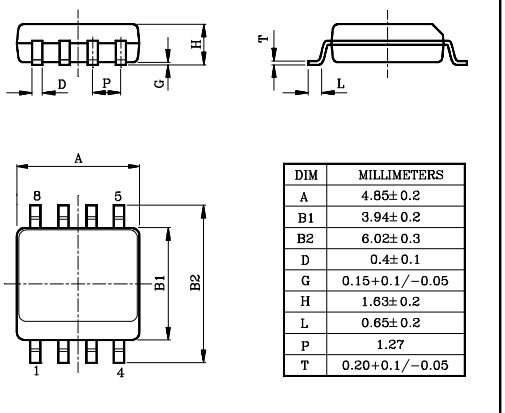
FEATURES

- Wide Operating Supply Voltage Range (2-16 volts)-Allows Telephone Line Powered Applications.
- Low Quiescent Supply Current 2.0mA Typical) for Battery Powered Applications.
- Chip Disable Input to Power Down the IC.
- Low Power-Down Quiescent Current (65μA Typical)
- Drives a Wide Range of Speaker Loads (8 Ohms and Up)
- Output Power Exceeds 250mW with 32 Ohm Speaker
- Low Total Harmonic Distortion (0.5% Typical)
- Gain Adjustable from <0 dB to> 46dB for Voice Band
- Requires Few External Components

PIN CONNECTION



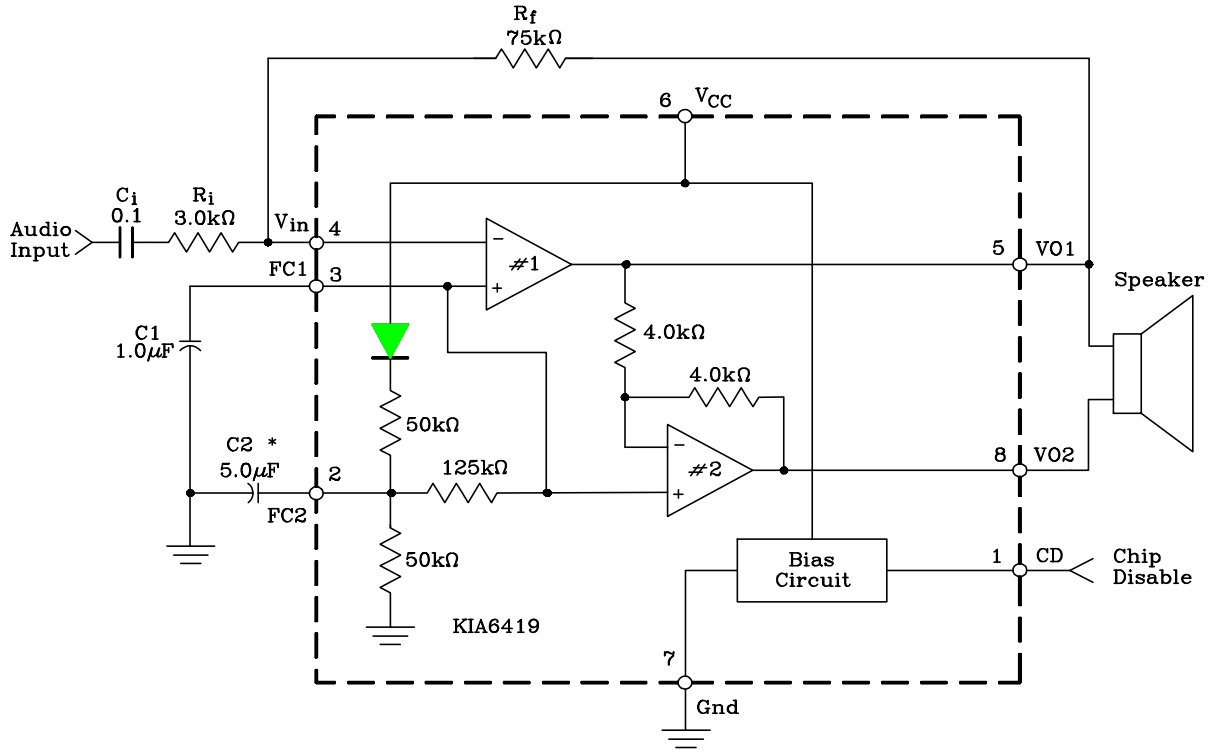

(Top View)




| DIM | MILLIMETERS |
|---|---|
| A | 4.85±0.2 |
| B1 | 3.94±0.2 |
| B2 | 6.02±0.3 |
| D | 0.4±0.1 |
| G | 0.15+0.1/−0.05 |
| H | 1.63±0.2 |
| L | 0.65±0.2 |
| P | 1.27 |
| T | 0.20+0.1/−0.05 |

FLP-8

BLOCK DIAGRAM AND TYPICAL APPLICATION CIRCUIT




* =Optional
Differential Gain = $2\times\frac{R_f}{R_i}$

MAXIMUM RATINGS (Ta=25℃)

| PARAMETER | VALUE | UNITS |
|---|---|---|
| Supply Voltage | -1.0 to 18 | Vdc |
| Maximum Output Current at VO1, VO2 | ±250 | mA |
| Maximum Voltage @Vin, FC1, FC2, CD | -1.0 $V_{CC}$+1.0 | Vdc |
| Applied Output Voltage to VO1, VO2 when disabled | -1.0 $V_{CC}$+1.0 | Vdc |
| Operating Temperature | -20~70 | ℃ |
| Junction Temperature | -55~140 | ℃ |

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | +2.0 | - | +16 | Vdc |
| Load Impedance | $R_L$ | 8.0 | - | 100 | Ω |
| Peak Load Current | $I_L$ | - | - | ±200 | mA |
| Differential Gain (5.0kHz bandwidth) | AVD | 0 | - | 46 | dB |
| Voltage @ CD (Pin 1) | VCD | 0 | - | $V_{CC}$ | Vdc |
| Ambient Temperature | $T_A$ | -20 | - | +70 | ℃ |

ELECTRICAL CHARACTERISTICS (Ta=25℃)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **AMPLIFIERS (AC CHARACTERISTCIS)** | | | | | |
| AC Input Resistance (@$V_{IN}$) | $r_i$ | - | >30 | - | MΩ |
| Open Loop Gain (Amplifier #1, f<100Hz) | $A_{VOL1}$ | 80 | - | - | dB |
| Closed Loop Gain (Amplifier #2) ($V_{CC}$=6.0V, f=1.0kHz, $R_L$=32Ω) | $A_{V2}$ | -0.35 | 0 | +0.35 | dB |
| Gain Bandwidth Product | GBW | - | 1.5 | - | MHz |
| Output Power, $V_{CC}$=3.0V, $R_L$=16Ω, THD≤10%<br>$V_{CC}$=6.0V, $R_L$=32Ω, THD≤10%<br>$V_{CC}$=12V, $R_L$=100Ω, THD≤10% | Pout3<br>Pout6<br>Pout12 | 55<br>250<br>400 | -<br>-<br>- | -<br>-<br>- | mW |
| Total Harmonic Distortion (f=1.0kHz)<br>($V_{CC}$=6.0V, $R_L$=32Ω, Pout=125mW)<br>($V_{CC}$≥3.0V, $R_L$=8.0Ω, Pout=20mW)<br>($V_{CC}$≥12V, $R_L$=32Ω, Pout=200mW) | THD | -<br>-<br>- | 0.5<br>0.5<br>0.6 | 1.0<br>-<br>- | % |
| Power Supply Rejection ($V_{CC}$=6.0V, $\Delta V_{CC}$=3.0V)<br>(C1=∞, C2=0.01μF)<br>(C1=0.1μF, C2=0, f=1.0kHz)<br>(C1=1.0μF, C2=5.0μF, f=1.0kHz) | PSRR | 50<br>-<br>- | -<br>12<br>52 | -<br>-<br>- | dB |
| Muting ($V_{CC}$=6.0V, 1.0kHz≤f≤20kHz, CD=2.0V) | GMT | - | >70 | - | dB |
| **AMPLIFIERS (DC CHARACTERISTCIS)** | | | | | |
| Output DC Level @VO1, VO2, $V_{CC}$=3.0V, $R_L$=16Ω<br>(Rf=75k) $V_{CC}$=6.0V<br>$V_{CC}$=12V | VO(3)<br>VO(6)<br>VO(12) | 1.0<br>-<br>- | 1.15<br>2.65<br>5.65 | 1.25<br>-<br>- | Vdc |
| Output High Level ($I_{OUT}$=-75mA, 2.0V≤$V_{CC}$≤16V) | $V_{OH}$ | - | $V_{CC}$-1.0 | - | Vdc |
| Output Low Level ($I_{OUT}$=75mA, 2.0V≤$V_{CC}$≤16V) | $V_{OL}$ | - | 0.16 | - | Vdc |
| Output DC Offset Voltage (VO1-VO2)<br>($V_{CC}$=6.0V, Rf=75kΩ, $R_L$=32Ω) | $\Delta V_O$ | -30 | 0 | +30 | mV |
| Input Bias Current @$V_{IN}$ ($V_{CC}$=6.0V) | $I_{IB}$ | - | -100 | -200 | nA |
| Equivalent Resistance @FC1 ($V_{CC}$=6.0V) | $R_{FC1}$ | 100 | 150 | 220 | kΩ |
| Equivalent Resistance @FC2 ($V_{CC}$=6.0V) | $R_{FC2}$ | 18 | 25 | 40 | kΩ |
| **CHIP DISABEL (Pin 1)** | | | | | |
| Input Voltage-Low | $V_{IL}$ | - | - | 0.8 | Vdc |
| Input Voltage-High | $V_{IH}$ | 2.0 | - | - | Vdc |
| Input Resistance ($V_{CC}$=$V_{CD}$=16V) | $R_{CD}$ | 50 | 90 | 175 | kΩ |
| Power Supply | | | | | |
| Power Supply Current<br>($V_{CC}$=3.0V, $R_L$=∞, CD=0.8V)<br>($V_{CC}$=16V, $R_L$=∞, CD=0.8V)<br>($V_{CC}$=3.0V, $R_L$=∞, CD=2.0V) | $I_{CC3}$<br>$I_{CC16}$<br>$I_{CCD}$ | -<br>-<br>- | 2.0<br>3.0<br>65 | 3.0<br>4.0<br>100 | mA<br><br>μA |

Note : Currents into a pin are positive, currents out of a pin are negative.

PIN DESCRIPTION

| SYMBOL | PIN. | DESCRIPTION |
|---|---|---|
| CD | 1 | Chip Disable-Digital Input. A logic "0"(<0.8V) sets normal operation. A Logic "1" (≥2.0V) sets the power down mode. Input impedance is nominally 90kΩ. |
| FC2 | 2 | A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at FC1 is sufficient. |
| FC1 | 3 | Analog Ground for the amplifiers. A 1.0μF capacitor at this pin (with a 5.0μF capacitor at Pin 2) provides (typically) 52dB of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input. |
| $V_{IN}$ | 4 | Amplifier Input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and VO1. |
| VO1 | 5 | Amplifier Output #1. The dc level is ≈ ($V_{CC}$-0.7V)/2. |
| $V_{CC}$ | 6 | DC supply voltage (+2.0 to +16volts) is applied to this pin. |
| GND | 7 | Ground pin for the entire circuit. |
| VO2 | 8 | Amplifier Output #2. This signal is equal in amplitude, but 180° out of phase with that at VO1. The dc level is ≈ ($V_{CC}$-0.7V)/2. |

TYPICAL TEMPERATURE PERFORMANCE (-20° <$T_A$<+70℃)

| SYMBOL | Typical Change | Units |
|---|---|---|
| Input Bias Current (@$V_{IN}$) | ±40 | pA/℃ |
| Total Harmonic Distortion ($V_{CC}$=6.0V, $R_L$=32Ω, Pout=125mW, f=1.0kHz) | +0.003 | %/℃ |
| Power Supply Current ($V_{CC}$=3.0V, $R_L$=∞, CD=0V) ($V_{CC}$=3.0V, $R_L$=∞, CD=2.0V) | -2.5 -0.03 | μA/℃ |

DESIGN GUIDELINES

**GENERAL**

The KIA6451P is a low power audio amplifier capable of low voltage operation ($V_{CC}$=2.0V minimum) such as that encountered in line-powered speakerphones. The circuit provides a differential output (VO1=VO2) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs tothe amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

**AMPLIFIERS**

Referring to the block diagram. The internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open loop gain of ≥ 80 dB (at f≤100Hz), and the closed loop gain is set by external resistors Rf and Ri. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5MHz. In order to adequately cover the telephone voice band (300-3400Hz). a maximum closed leep gain of 46dB is recommended. Amplifier #2 is internally set to a gain of -1.0 (0dB). The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200mA. The outputs can typically swing to within≈0.4 volts above ground and to within ≈1.3 volts below $V_{CC}$. at the maximum current. See Figures 18 and 19 for $V_{OH}$ and $V_{OL}$ curves. The output dc offset voltage (VO1-VO2) is primarily a function of the feedback resistor(Rf), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular Ic, and therefore nearly cancel each other at the outputs.

Amplifier #1's bias current, however, flows out of $V_{IN}$ (Pin4) and through Rf, forcing VO1 to shift negative by an amount equal to ($R_f \times 1_{IB}$). VO2 is shifted positive an equal amount. The output offset voltage specified in the Electrical characteristics is measured with the feedback resistor shown in the typical application circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to $V_{CC}$.