DATA SHEET

BFG97
NPN 5 GHz wideband transistor

Product specification
File under Discrete Semiconductors, SC14

September 1995

Philips Semiconductors

PHILIPS

NPN 5 GHz wideband transistor | BFG97

DESCRIPTION

NPN planar epitaxial transistor mounted in a plastic SOT223 envelope.
It features excellent output voltage capabilities, and is primarily intended for use in MATV applications.

PNP complement is the BFG31.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	emitter
4	collector

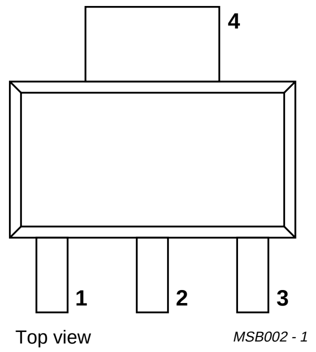


Fig.1 SOT223.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–	20	V
V_{CEO}	collector-emitter voltage	open base	–	–	15	V
I_C	DC collector current		–	–	100	mA
P_{tot}	total power dissipation	up to T_s = 125 °C (note 1)	–	–	1	W
h_{FE}	DC current gain	I_C = 70 mA; V_{CE} = 10 V; T_j = 25 °C	25	80	–	
f_T	transition frequency	I_C = 70 mA; V_{CE} = 10 V; f = 500 MHz; T_{amb} = 25 °C	–	5.5	–	GHz
G_{UM}	maximum unilateral power gain	I_C = 70 mA; V_{CE} = 10 V; f = 500 MHz; T_{amb} = 25 °C	–	16	–	dB
		I_C = 70 mA; V_{CE} = 10 V; f = 800 MHz; T_{amb} = 25 °C	–	12	–	dB
V_o	output voltage	I_C = 70 mA; V_{CE} = 10 V; d_{im} = –60 dB; R_L = 75 Ω; $f_{(p+q-r)}$ = 793.25 MHz; T_{amb} = 25 °C	–	700	–	mV

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	20	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	DC collector current		–	100	mA
P_{tot}	total power dissipation	up to T_s = 125 °C (note 1)	–	1	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	175	°C

Note

1. T_s is the temperature at the soldering point of the collector tab.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	up to T_s = 125 °C (note 1)	50 K/W

Note

1. T_s is the temperature at the soldering point of the collector tab.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = 10 V	–	–	100	nA
h_{FE}	DC current gain	I_C = 70 mA; V_{CE} = 10 V	25	80	–	
f_T	transition frequency	I_C = 70 mA; V_{CE} = 10 V; f = 500 MHz; T_{amb} = 25 °C	–	5.5	–	GHz
C_c	collector capacitance	$I_E = i_e$ = 0; V_{CB} = 10 V; f = 1 MHz	–	1.5	–	pF
C_e	emitter capacitance	$I_C = i_c$ = 0; V_{EB} = 0.5 V; f = 1 MHz	–	6.5	–	pF
C_{re}	feedback capacitance	I_C = 0; V_{CE} = 10 V; f = 1 MHz	–	1	–	pF
G_{UM}	maximum unilateral power gain (note 1)	I_C = 70 mA; V_{CE} = 10 V; f = 500 MHz; T_{amb} = 25 °C	–	16	–	dB
		I_C = 70 mA; V_{CE} = 10 V; f = 800 MHz; T_{amb} = 25 °C	–	12	–	dB
V_o	output voltage	note 2	–	750	–	mV
		note 3	–	700	–	mV
d_2	second order intermodulation distortion	note 4	–	–56	–	dB
		note 5	–	–53	–	dB

Notes

1. G_{UM} is the maximum unilateral power gain, assuming S_{12} is zero and

$$G_{UM} = 10\log\frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)}\ \text{dB.}$$

2. d_{im} = –60 dB (DIN 45004B); I_C = 70 mA; V_{CE} = 10 V; R_L = 75 Ω; T_{amb} = 25 °C
   $V_p = V_o$ at d_{im} = –60 dB;
   $V_q = V_o$ –6 dB; f_p = 445.25 MHz;
   $V_r = V_o$ –6 dB; f_q = 453.25 MHz; f_r = 455.25 MHz;
   measured at $f_{(p+q-r)}$ = 443.25 MHz.
3. d_{im} = –60 dB (DIN 45004B); I_C = 70 mA; V_{CE} = 10 V; R_L = 75 Ω; T_{amb} = 25 °C
   $V_p = V_o$ at d_{im} = –60 dB;
   $V_q = V_o$ –6 dB; f_p = 795.25 MHz;
   $V_r = V_o$ –6 dB; f_q = 803.25 MHz; f_r = 805.25 MHz;
   measured at $f_{(p+q-r)}$ = 793.25 MHz.
4. I_C = 70 mA; V_{CE} = 10 V; R_L = 75 Ω; T_{amb} = 25 °C;
   $V_p = V_q = V_o$ = 50 dBmV; $f_{(p+q)}$ = 450 MHz; f_p = 50 MHz; f_q = 400 MHz.
5. I_C = 70 mA; V_{CE} = 10 V; R_L = 75 Ω; T_{amb} = 25 °C;
   $V_p = V_q = V_o$ = 50 dBmV; $f_{(p+q)}$ = 810 MHz; f_p = 250 MHz; f_q = 560 MHz.

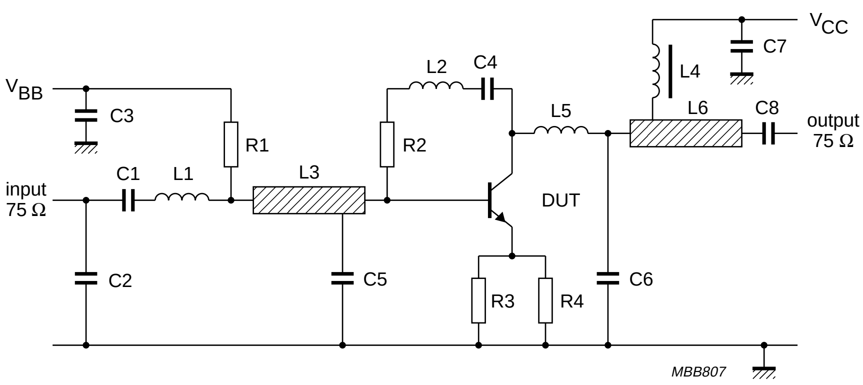


Fig.2 Intermodulation distortion and second order intermodulation distortion test circuit.

List of components (see test circuit)

DESIGNATION	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C2, C3, C7, C8	multilayer ceramic capacitor	10 nF		2222 590 08627
C1, C4, C6	multilayer ceramic capacitor	1.2 pF		2222 851 12128
C5 (note 1)	miniature ceramic plate capacitor	10 nF		2222 629 08103
L1 (note 1)	0.5 turns 0.4 mm copper wire		int. dia. 3 mm	
L2	microstripline	75 Ω	length 14 mm; width 2.5 mm	
L3	microstripline	75 Ω	length 8 mm; width 2.5 mm	
L4, L5 (note 1)	1.5 turns 0.4 mm copper wire		int. dia. 3 mm; winding pitch 1 mm	
L6	microstripline	75 Ω	length 19 mm; width 2.5 mm	
L7	Ferroxcube choke	5 μH		3122 108 20153
R1	metal film resistor	10 kΩ		2322 180 73103
R2 (note 1)	metal film resistor	220 Ω		2322 180 73221
R3, R4	metal film resistor	30 Ω		2322 180 73309

Notes

The circuit has been built on a double copper-clad printed circuit board with PTFE dielectric (ε_r = 2.2); thickness $^1\!/_{16}$ inch; thickness of copper sheet 2 × 35 μm.

1. Components C5, L1, L4, L5, and R2 are mounted on the underside of the PCB.

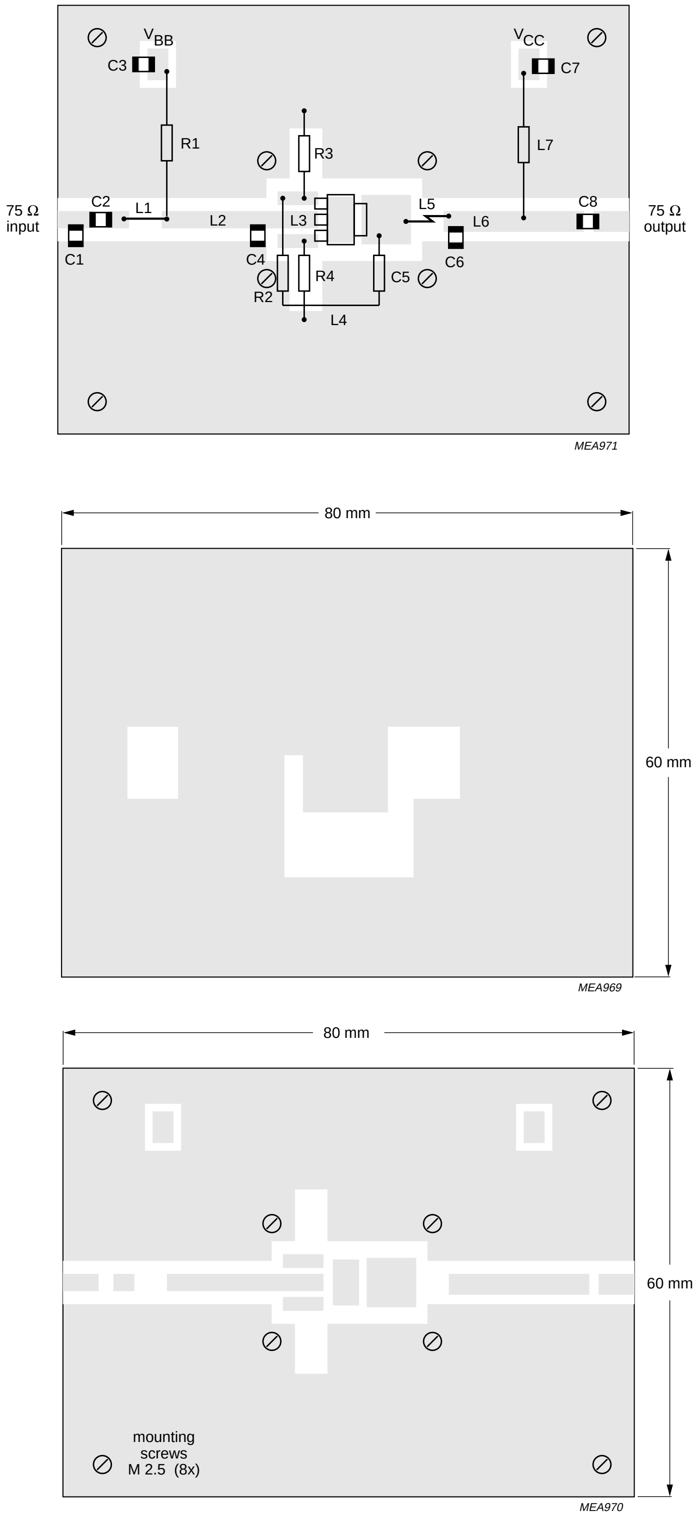


Fig.3 Intermodulation distortion and second order intermodulation distortion printed circuit board.

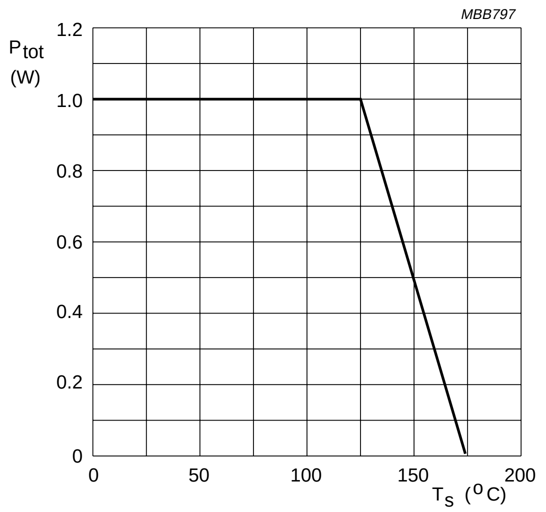
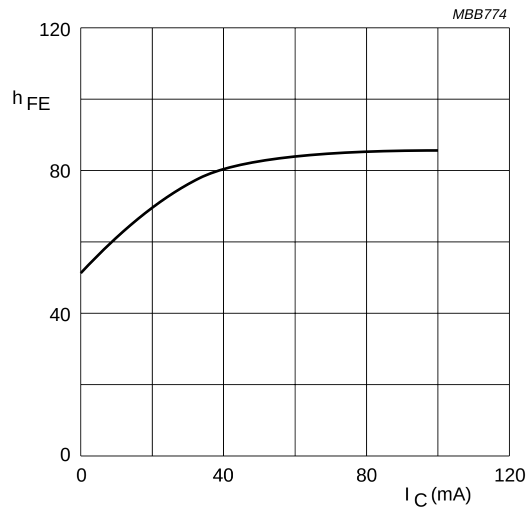
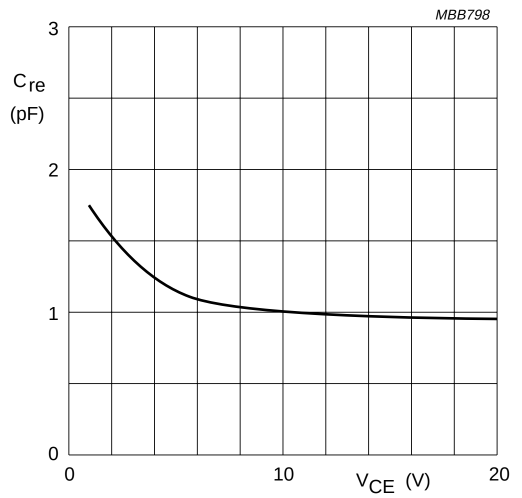


Fig.4 Power derating curve.



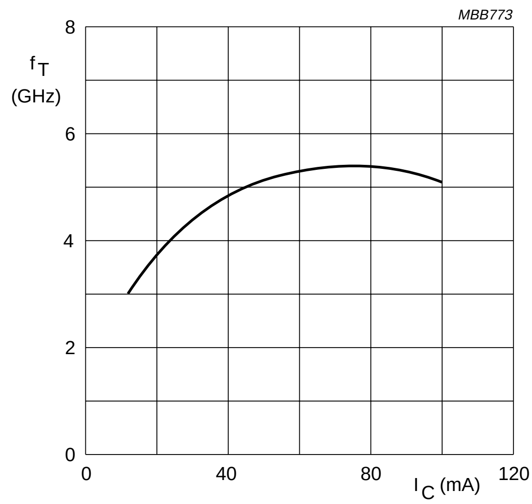
V_{CE} = 10 V; T_j = 25 °C.

Fig.5 DC current gain as a function of collector current.



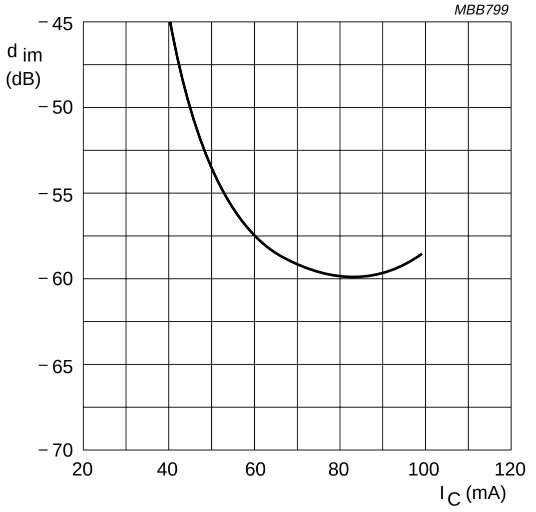
I_E = 0; f = 1 MHz; T_j = 25 °C.

Fig.6 Feedback capacitance as a function of collector-emitter voltage.



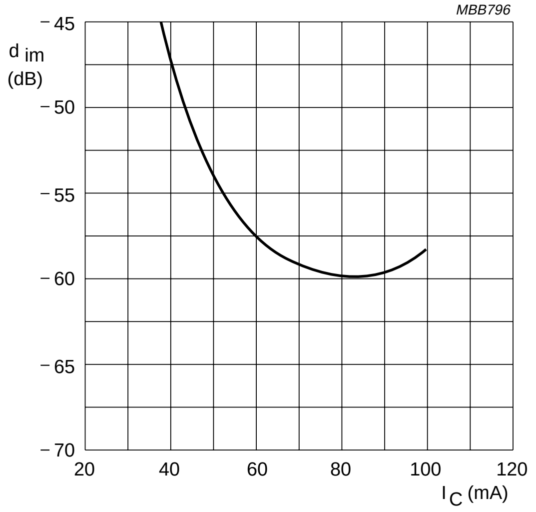
V_{CE} = 10 V; f = 500 MHz; T_j = 25 °C.

Fig.7 Transition frequency as a function of collector current.



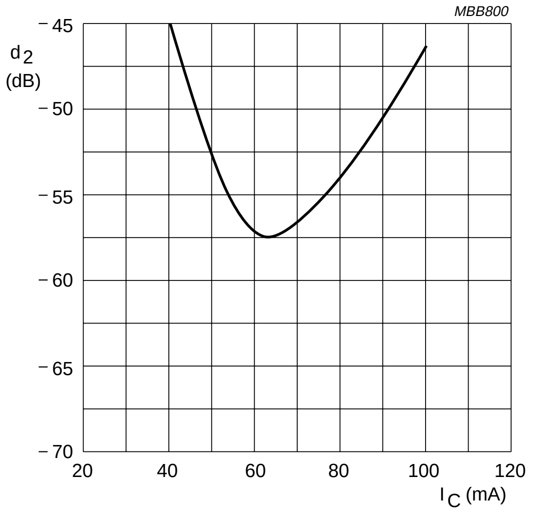
V_{CE} = 10 V; V_o = 750 mV; $f_{(p+q-r)}$ = 443.25 MHz;
T_{amb} = 25 °C.

Fig.8 Intermodulation distortion as a function of collector current.



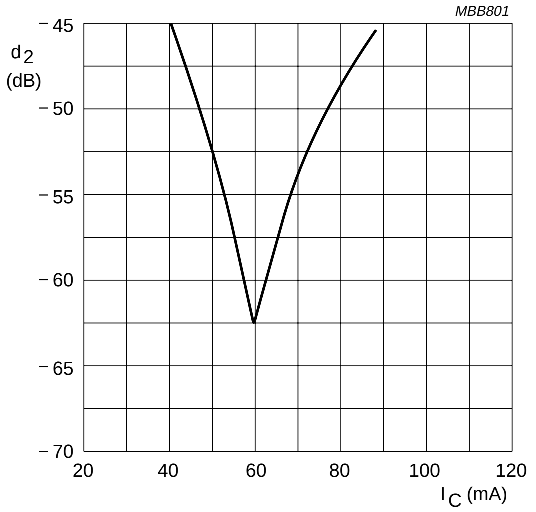
V_{CE} = 10 V; V_o = 700 mV; $f_{(p+q-r)}$ = 793.25 MHz;
T_{amb} = 25 °C.

Fig.9 Intermodulation distortion as a function of collector current.



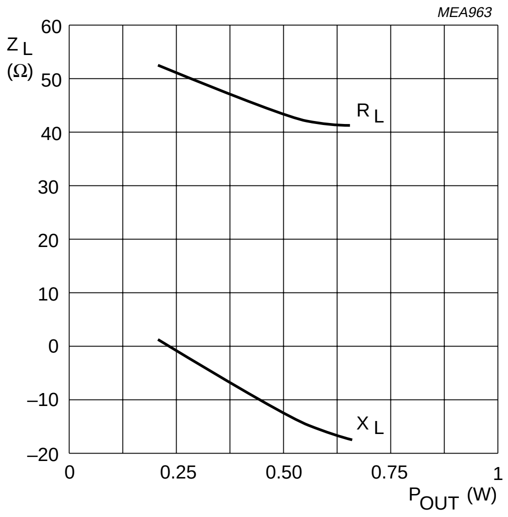
V_{CE} = 10 V; V_o = 50 dBmV; $f_{(p+q)}$ = 450 MHz;
T_{amb} = 25 °C.

Fig.10 Second order intermodulation distortion as a function of collector current.



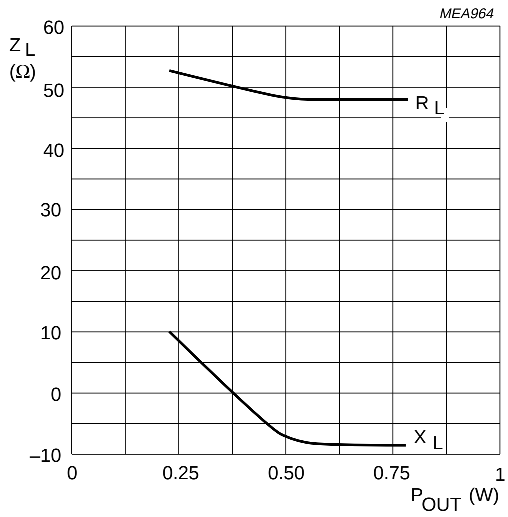
V_{CE} = 10 V; V_o = 50 dBmV; $f_{(p+q)}$ = 810 MHz;
T_{amb} = 25 °C.

Fig.11 Second order intermodulation distortion as a function of collector current.



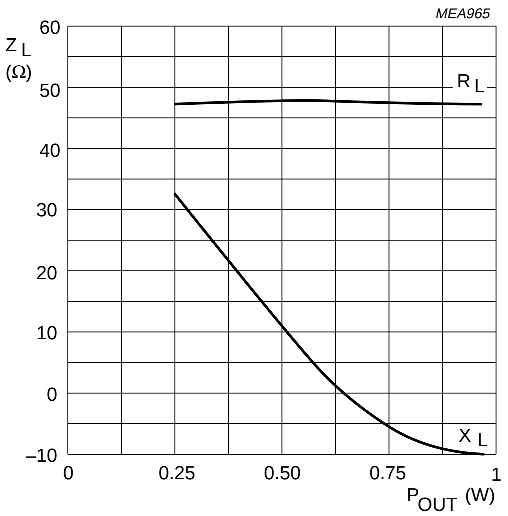
V_{CE} = 6 V; f = 900 MHz.

Fig.12 Load impedance as a function of output power.



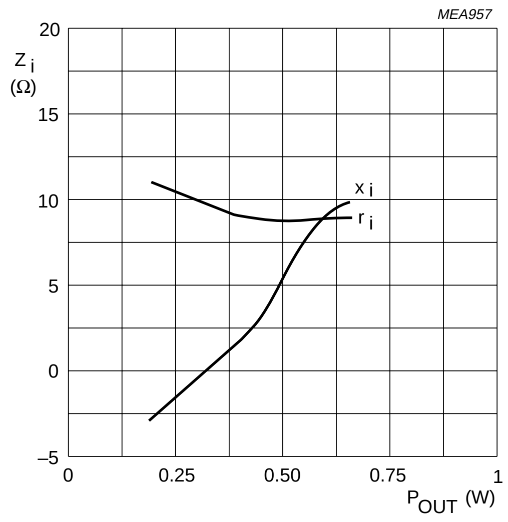
V_{CE} = 7.5 V; f = 900 MHz.

Fig.13 Load impedance as a function of output power.



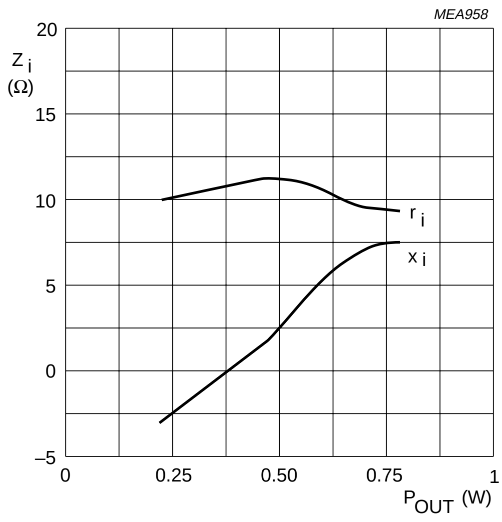
V_{CE} = 10 V; f = 900 MHz.

Fig.14 Load impedance as a function of output power.



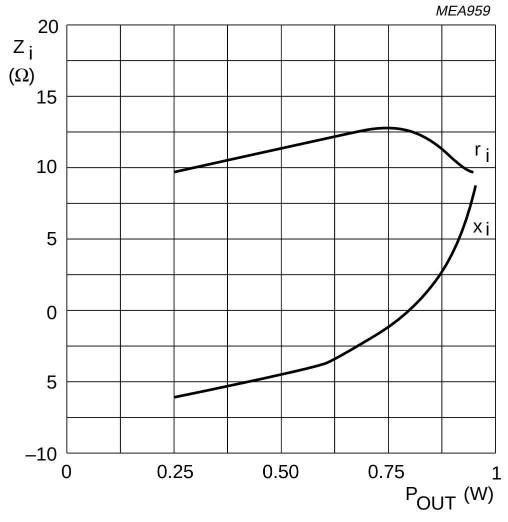
V_{CE} = 6 V; f = 900 MHz.

Fig.15 Input impedance as a function of output power.



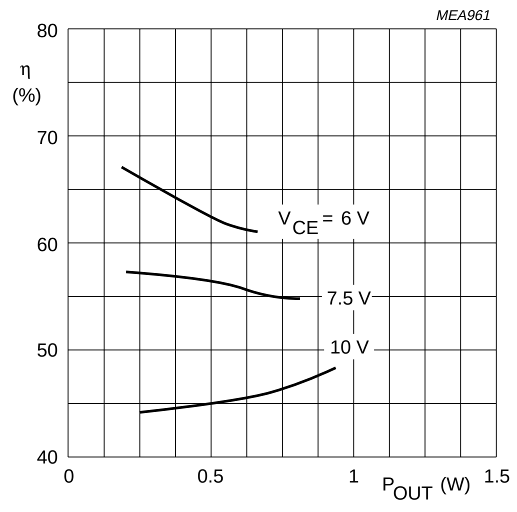
V_{CE} = 7.5 V; f = 900 MHz.

Fig.16 Input impedance as a function of output power.



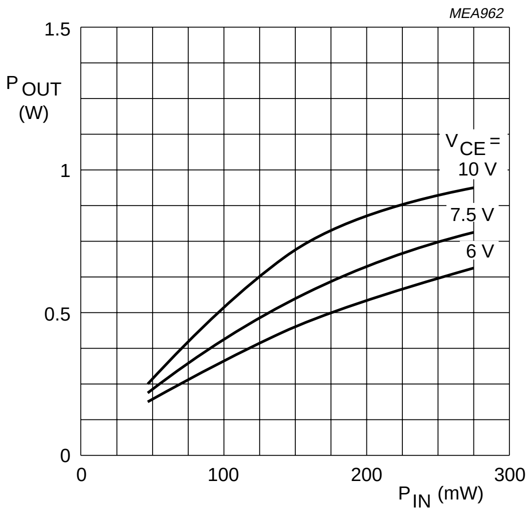
V_{CE} = 10 V; f = 900 MHz.

Fig.17 Input impedance as a function of output power.



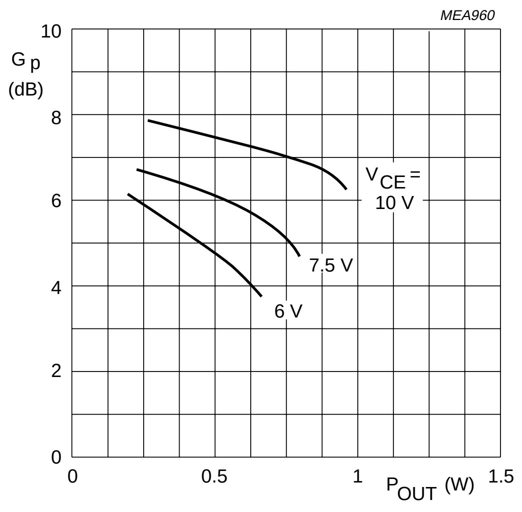
f = 900 MHz.

Fig.18 Efficiency as a function of output power.



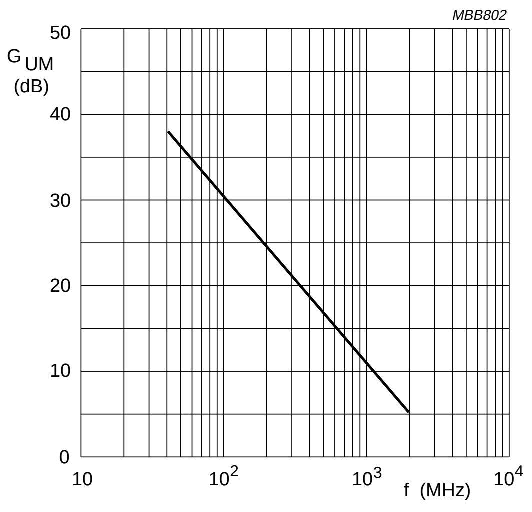
f = 900 MHz.

Fig.19 Output power as a function of input power.



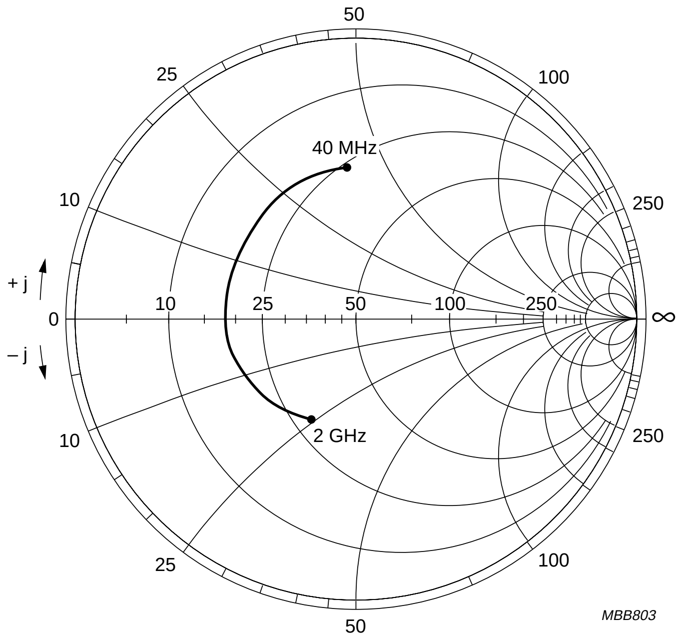
f = 900 MHz.

Fig.20 Power gain as a function of output power.



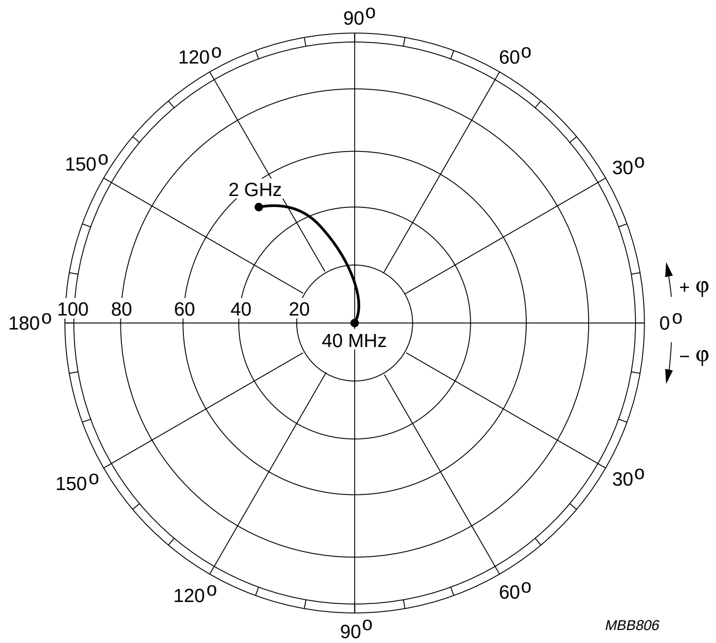
I_C = 70 mA; V_{CE} = 10 V; T_{amb} = 25 °C.

Fig.21 Maximum unilateral power gain as a function of frequency.



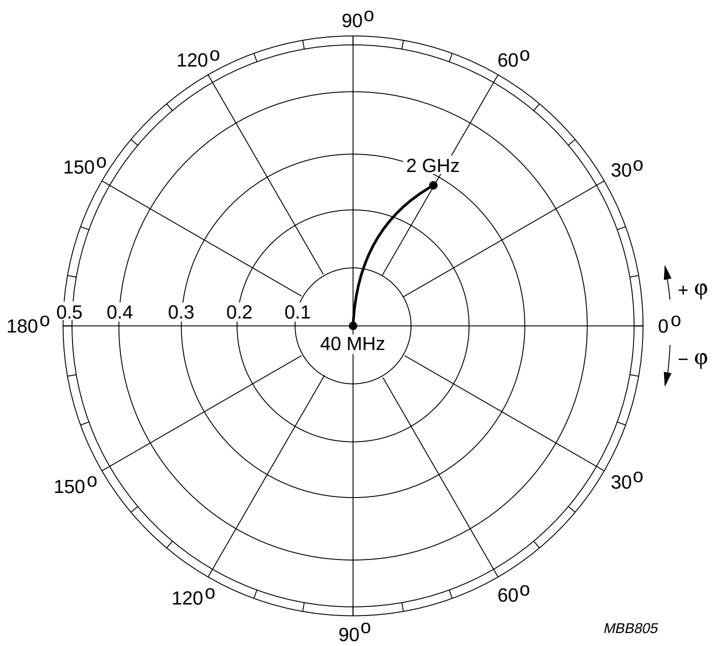
I_C = 70 mA; V_{CE} = 10 V; T_{amb} = 25 °C.
Z_o = 50 Ω.

Fig.22 Common emitter input reflection coefficient (S_{11}).



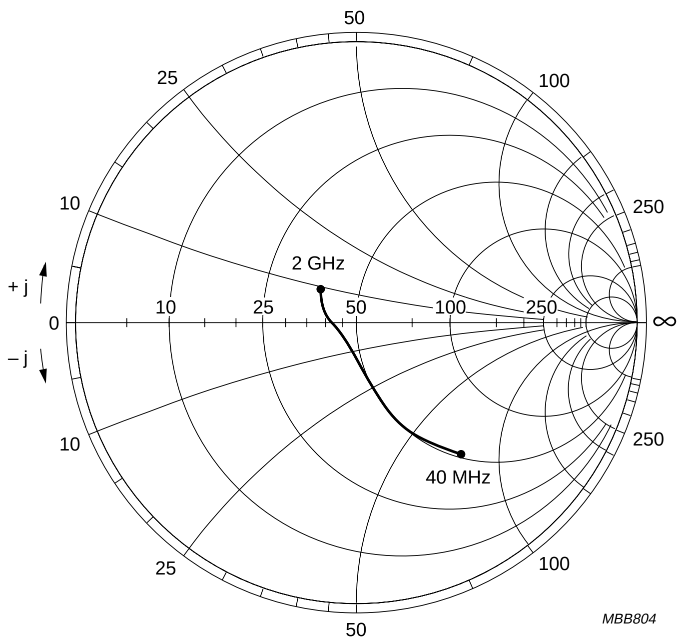
I_C = 70 mA; V_{CE} = 10 V; T_{amb} = 25 °C.

Fig.23 Common emitter forward transmission coefficient (S_{21}).

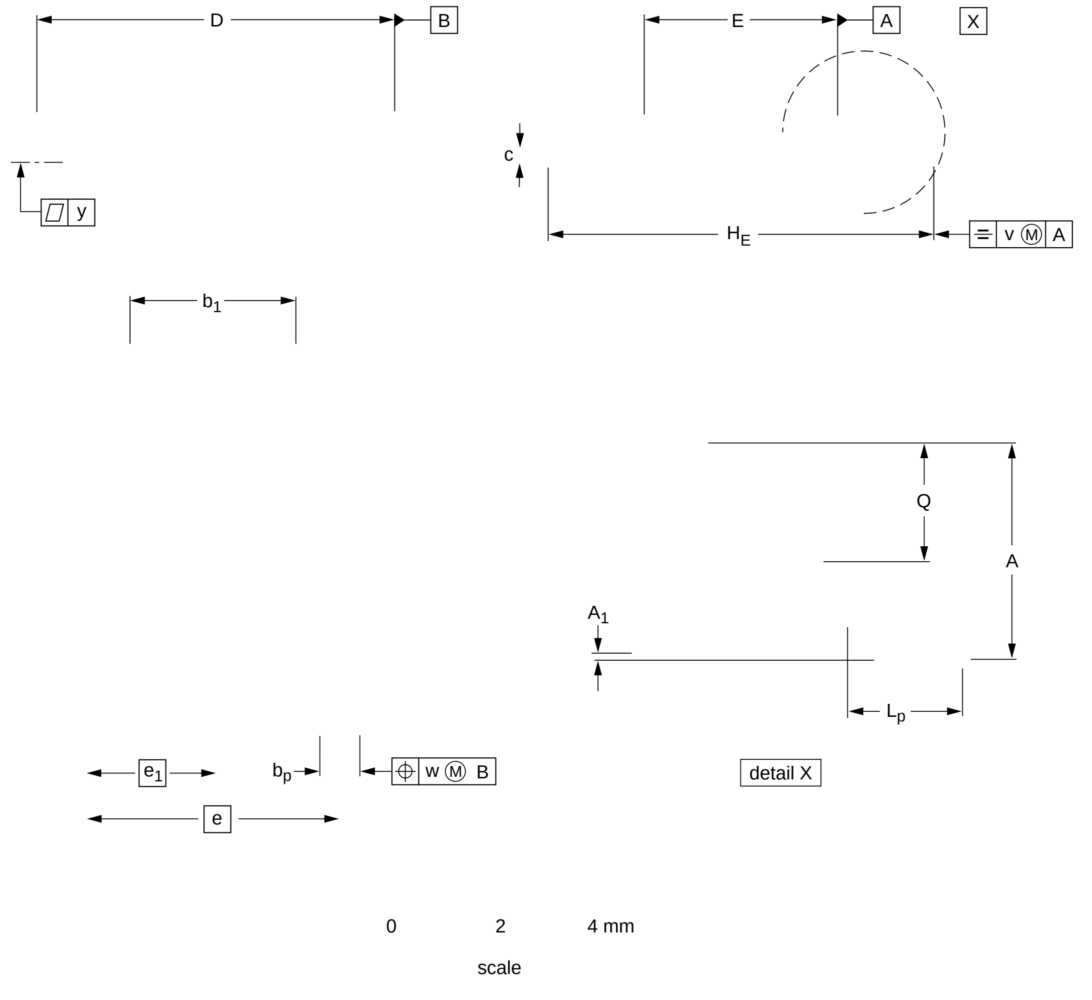


I_C = 70 mA; V_{CE} = 10 V; T_{amb} = 25 °C.

Fig.24 Common emitter reverse transmission coefficient (S_{12}).



PACKAGE OUTLINE



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						96-11-11 97-02-28

NPN 5 GHz wideband transistor BFG97

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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