



# TS4890

## RAIL TO RAIL OUTPUT 1W AUDIO POWER AMPLIFIER WITH STANDBY MODE

- OPERATING FROM  $V_{CC} = 2.2V$  to  $5.5V$
- **1W** RAIL TO RAIL OUTPUT POWER @  $V_{CC}=5V$ , THD=1%,  $f=1kHz$ , with  $8\Omega$  Load
- ULTRA LOW CONSUMPTION IN STANDBY MODE (**10nA**)
- **75dB** PSRR @ 217Hz from 5 to 2.2V
- POP & CLICK REDUCTION CIRCUITRY
- ULTRA LOW DISTORTION (**0.1%**)
- UNITY GAIN STABLE
- AVAILABLE IN **MiniSO8 & SO8**

### DESCRIPTION

The TS4890 (MiniSO8 & SO8) is an Audio Power Amplifier capable of delivering 1W of continuous RMS. output power into  $8\Omega$  load @ 5V.

This Audio Amplifier is exhibiting 0.1% distortion level (THD) from a 5V supply for a  $P_{out} = 250mW$  RMS. An external standby mode control reduces the supply current to less than 10nA. An internal thermal shutdown protection is also provided.

The TS4890 have been designed for high quality audio applications such as mobile phones and to minimize the number of external components.

The unity-gain stable amplifier can be configured by external gain setting resistors.

### APPLICATIONS

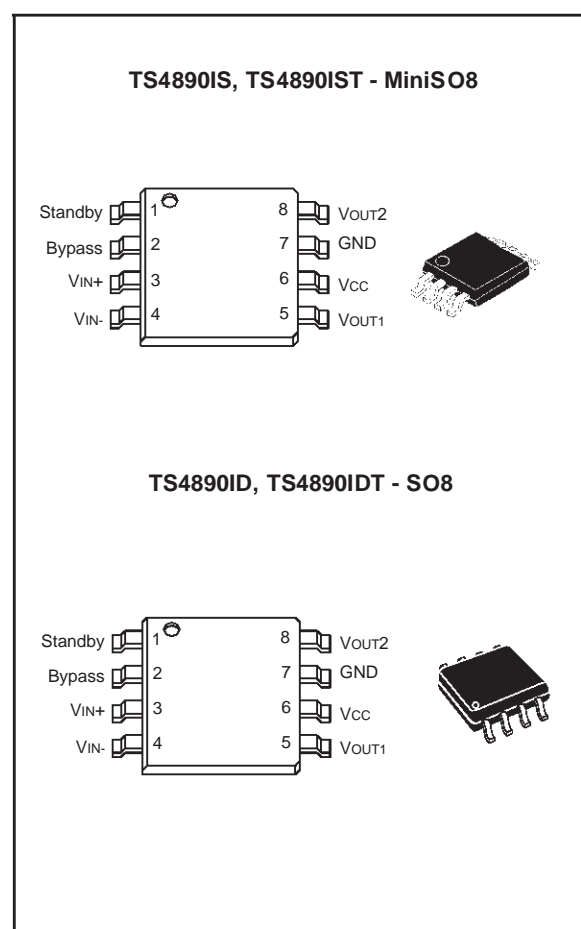
- Mobile Phones (Cellular / Cordless)
- Laptop / Notebook Computers
- PDAs
- Portable Audio Devices

### ORDER CODE

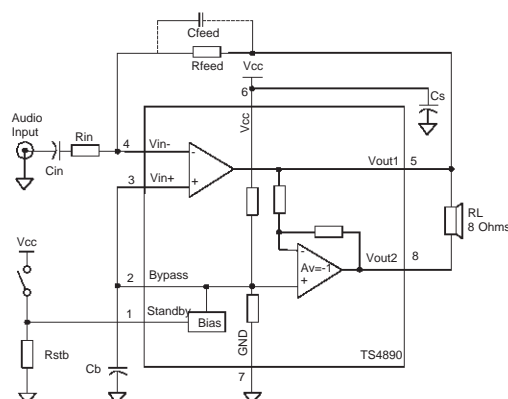
Part Number	Temperature Range	Package	
		S	D
TS4890IST	-40, +85°C	•	
TS4890IDT			•

S = MiniSO Package (MiniSO) - also available in Tape & Reel (ST)  
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

### PIN CONNECTIONS (Top View)



### TYPICAL APPLICATION SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>1)</sup>	6	V
$V_i$	Input Voltage <sup>2)</sup>	$G_{ND}$ to $V_{CC}$	V
$T_{oper}$	Operating Free Air Temperature Range	-40 to + 85	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_j$	Maximum Junction Temperature	150	°C
$R_{thja}$	Thermal Resistance Junction to Ambient <sup>3)</sup> SO8 MiniSO8	175 215	°C/W
$P_d$	Power Dissipation <sup>4)</sup>	See Power Derating Curves Fig. 24	W
ESD	Human Body Model	2	kV
ESD	Machine Model	200	V
	Latch-up Immunity	Class A	
	Lead Temperature (soldering, 10sec)	260	°C

1. All voltages values are measured with respect to the ground pin.

2. The magnitude of input signal must never exceed  $V_{CC} + 0.3V$  /  $G_{ND} - 0.3V$

3. Device is protected in case of over temperature by a thermal shutdown active @ 150°C.

4. Exceeding the power derating curves during a long period may involve abnormal working of the device.

## OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	2.2 to 5.5	V
$V_{ICM}$	Common Mode Input Voltage Range	$G_{ND} + 1V$ to $V_{CC}$	V
$V_{STB}$	Standby Voltage Input : Device ON Device OFF	$1.5 \leq V_{STB} \leq V_{CC}$ $G_{ND} \leq V_{STB} \leq 0.5$	V
$R_L$	Load Resistor	4 - 32	$\Omega$
$R_{thja}$	Thermal Resistance Junction to Ambient <sup>1)</sup> SO8 MiniSO8	150 190	°C/W

1. This thermal resistance can be reduced with a suitable PCB layout (see Power Derating Curves Fig. 24)

**ELECTRICAL CHARACTERISTICS**

$V_{CC} = +5V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current No input signal, no load		6	8	mA
$I_{STANDBY}$	Standby Current <sup>1)</sup> No input signal, $V_{stdby} = G_{ND}$ , $R_L = 8\Omega$		10	1000	nA
$V_{OO}$	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	20	mV
$P_o$	Output Power THD = 1% Max, $f = 1kHz$ , $R_L = 8\Omega$		1		W
THD + N	Total Harmonic Distortion + Noise $P_o = 250mW$ rms, $G_v = 2$ , $20Hz < f < 20kHz$ , $R_L = 8\Omega$		0.15		%
PSRR	Power Supply Rejection Ratio <sup>2)</sup> $f = 217Hz$ , $R_L = 8\Omega$ , $R_{Feed} = 22K\Omega$ , $V_{ripple} = 200mV$ rms		77		dB
$\Phi_M$	Phase Margin at Unity Gain $R_L = 8\Omega$ , $C_L = 500pF$		70		Degrees
GM	Gain Margin $R_L = 8\Omega$ , $C_L = 500pF$		20		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz

1. Standby mode is activated when  $V_{stdby}$  is tied to  $GND$

2. Dynamic measurements -  $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$ . Vripple is the surimposed sinus signal to  $V_{CC}$  @  $f = 217Hz$

$V_{CC} = +3.3V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current <sup>1)</sup> No input signal, $V_{stdby} = G_{ND}$ , $R_L = 8\Omega$		10	1000	nA
$V_{OO}$	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	20	mV
$P_o$	Output Power THD = 1% Max, $f = 1kHz$ , $R_L = 8\Omega$		450		mW
THD + N	Total Harmonic Distortion + Noise $P_o = 250mW$ rms, $G_v = 2$ , $20Hz < f < 20kHz$ , $R_L = 8\Omega$		0.15		%
PSRR	Power Supply Rejection Ratio <sup>2)</sup> $f = 217Hz$ , $R_L = 8\Omega$ , $R_{Feed} = 22K\Omega$ , $V_{ripple} = 200mV$ rms		77		dB
$\Phi_M$	Phase Margin at Unity Gain $R_L = 8\Omega$ , $C_L = 500pF$		70		Degrees
GM	Gain Margin $R_L = 8\Omega$ , $C_L = 500pF$		20		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz

1. Standby mode is activated when  $V_{stdby}$  is tied to  $GND$

2. Dynamic measurements -  $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$ . Vripple is the surimposed sinus signal to  $V_{CC}$  @  $f = 217Hz$

**TS4890**

$V_{CC} = 2.6V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current No input signal, no load		5	8	mA
$I_{STANDBY}$	Standby Current <sup>1)</sup> No input signal, $V_{stdby} = G_{ND}$ , $R_L = 8\Omega$		10	1000	nA
$V_{OO}$	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	20	mV
$P_o$	Output Power THD = 1% Max, $f = 1kHz$ , $R_L = 8\Omega$		260		mW
THD + N	Total Harmonic Distortion + Noise $P_o = 200mW$ rms, $G_v = 2$ , $20Hz < f < 20kHz$ , $R_L = 8\Omega$		0.15		%
PSRR	Power Supply Rejection Ratio <sup>2)</sup> $f = 217Hz$ , $R_L = 8\Omega$ , $R_{Feed} = 22K\Omega$ , $V_{ripple} = 200mV$ rms		77		dB
$\Phi_M$	Phase Margin at Unity Gain $R_L = 8\Omega$ , $C_L = 500pF$		70		Degrees
GM	Gain Margin $R_L = 8\Omega$ , $C_L = 500pF$		20		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz

1. Standby mode is activated when  $V_{stdby}$  is tied to GND

2. Dynamic measurements -  $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$ . Vripple is the surimposed sinus signal to  $V_{CC}$  @  $f = 217Hz$

$V_{CC} = 2.2V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current No input signal, no load		5	8	mA
$I_{STANDBY}$	Standby Current <sup>1)</sup> No input signal, $V_{stdby} = G_{ND}$ , $R_L = 8\Omega$		10	1000	nA
$V_{OO}$	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	20	mV
$P_o$	Output Power THD = 1% Max, $f = 1kHz$ , $R_L = 8\Omega$		180		mW
THD + N	Total Harmonic Distortion + Noise $P_o = 200mW$ rms, $G_v = 2$ , $20Hz < f < 20kHz$ , $R_L = 8\Omega$		0.15		%
PSRR	Power Supply Rejection Ratio <sup>2)</sup> $f = 217Hz$ , $R_L = 8\Omega$ , $R_{Feed} = 22K\Omega$ , $V_{ripple} = 100mV$ rms		77		dB
$\Phi_M$	Phase Margin at Unity Gain $R_L = 8\Omega$ , $C_L = 500pF$		70		Degrees
GM	Gain Margin $R_L = 8\Omega$ , $C_L = 500pF$		20		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz

1. Standby mode is activated when  $V_{stdby}$  is tied to GND

2. Dynamic measurements -  $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$ . Vripple is the surimposed sinus signal to  $V_{CC}$  @  $f = 217Hz$

Components	Functional Description
Rin	Inverting input resistor which sets the closed loop gain in conjunction with Rfeed. This resistor also forms a high pass filter with Cin ( $f_c = 1 / (2 \times \pi \times R_{in} \times C_{in})$ )
Cin	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal
Rfeed	Feed back resistor which sets the closed loop gain in conjunction with Rin
Cs	Supply Bypass capacitor which provides power supply filtering
Cb	Bypass pin capacitor which provides half supply filtering
Cfeed	Low pass filter capacitor allowing to cut the high frequency (low pass filter cut-off frequency $1 / (2 \times \pi \times R_{feed} \times C_{feed})$ )
Rstb	Pull-down resistor which fixes the right supply level on the standby pin
Gv	Closed loop gain in BTL configuration = $2 \times (R_{feed} / R_{in})$

## REMARKS

1. All measurements, except PSRR measurements, are made with a supply bypass capacitor  $C_s = 100\mu F$ .
1. External resistors are not needed for having better stability when supply @  $V_{cc}$  down to 3V. The quiescent current still remains the same.
2. The standby response time is about  $1\mu s$ .

## APPLICATION INFORMATION

Fig. 101 : Demoboard Schematic

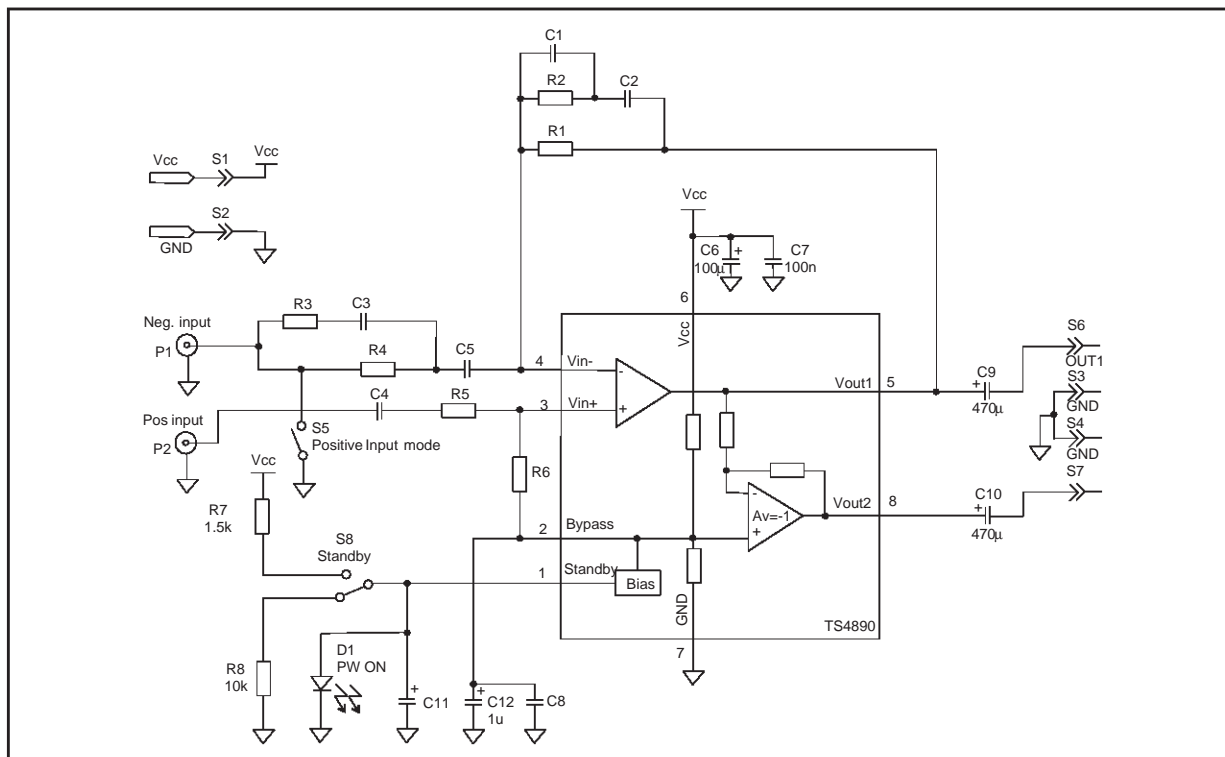
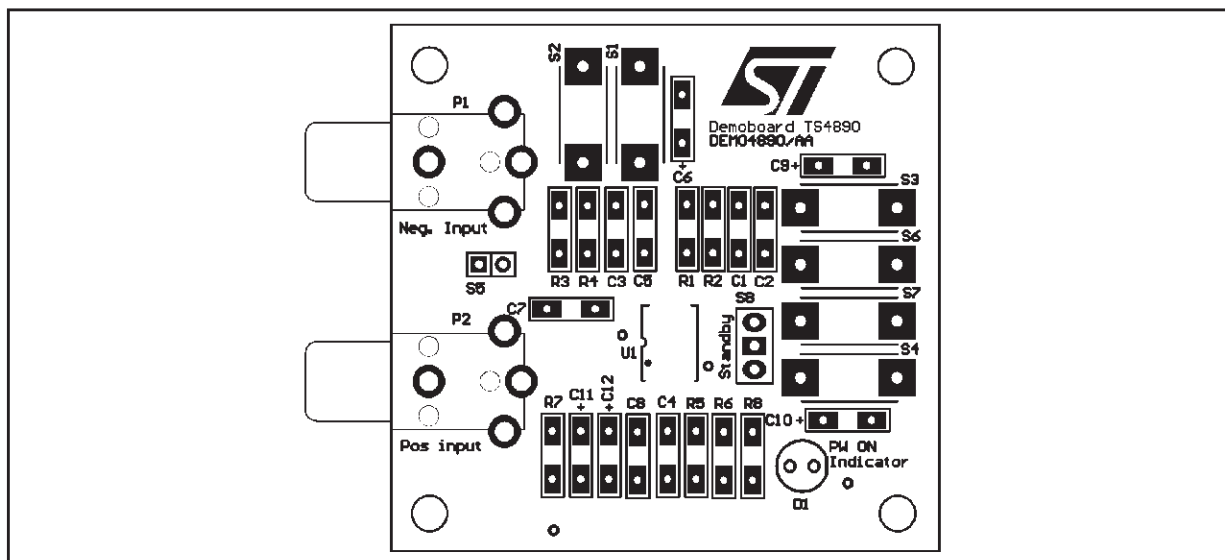
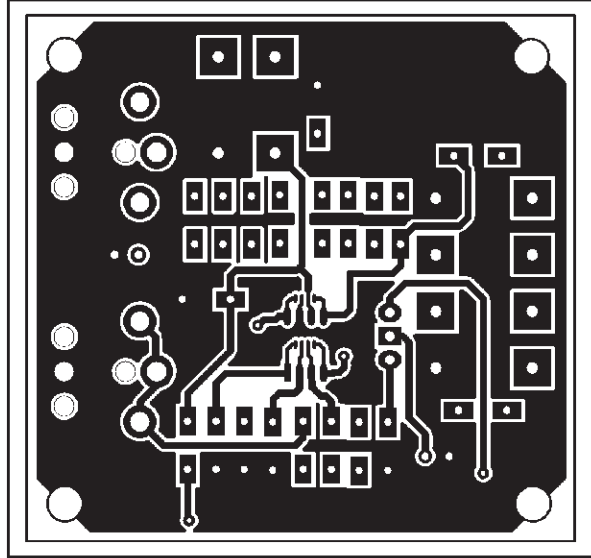


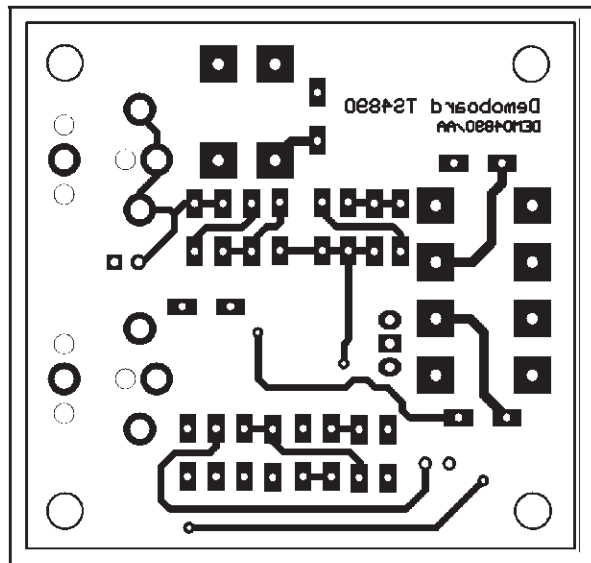
Fig. 102 : SO8 &amp; MiniSO8 Demoboard Components Side



**Fig. 103 : SO8 & MiniSO8 Demoboard Top Solder Layer**



**Fig. 104 : SO8 & MiniSO8 Demoboard Bottom Solder Layer**



#### ■ BTL Configuration Principle

The TS4890 is a monolithic power amplifier with a BTL output type. BTL (Bridge Tied Load) means that each end of the load are connected to two single ended output amplifiers. Thus, we have :

Single ended output 1 =  $V_{out1} = V_{out}$  (V)  
Single ended output 2 =  $V_{out2} = -V_{out}$  (V)

And  $V_{out1} - V_{out2} = 2V_{out}$  (V)

The output power is :

$$P_{out} = \frac{(2 V_{out_{RMS}})^2}{R_L} (W)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

#### ■ Gain In Typical Application Schematic (cf. page 1)

In flat region (no effect of  $C_{in}$ ), the output voltage of the first stage is :

$$V_{out1} = -V_{in} \frac{R_{feed}}{R_{in}} (V)$$

For the second stage :  $V_{out2} = -V_{out1}$  (V)

The differential output voltage is

$$V_{out2} - V_{out1} = 2 V_{in} \frac{R_{feed}}{R_{in}} (V)$$

The differential gain named gain ( $G_v$ ) for more convenient usage is :

$$G_v = \frac{V_{out2} - V_{out1}}{V_{in}} = 2 \frac{R_{feed}}{R_{in}}$$

Remark :  $V_{out2}$  is in phase with  $V_{in}$  and  $V_{out1}$  is 180 phased with  $V_{in}$ . It means that the positive terminal of the loudspeaker should be connected to  $V_{out2}$  and the negative to  $V_{out1}$ .

#### ■ Low and high frequency response

In low frequency region, the effect of  $C_{in}$  starts.  $C_{in}$  with  $R_{in}$  forms a high pass filter with a -3dB cut off frequency .

$$F_{CL} = \frac{1}{2\pi R_{in} C_{in}} (Hz)$$

In high frequency region, you can limit the bandwidth by adding a capacitor ( $C_{feed}$ ) in parallel on  $R_{feed}$ . Its form a low pass filter with a -3dB cut off frequency .

$$F_{CH} = \frac{1}{2\pi R_{feed} C_{feed}} (Hz)$$