SIMM Data Sheet

4, 8 MEG x 32 DRAM SIMMs (OBSOLETE)

DRAM MODULE

MT8D432(X)
MT16D832(X)

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, single in-line memory module (SIMM)
- 16MB (4 Meg x 32) and 32MB (8 Meg x 32)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE (FPM) access or Extended Data-Out (EDO) PAGE MODE access

OPTIONS

OPTIONS	MARKING
Timing	
50ns access	-5*
60ns access	-6
Packages	
72-pin SIMM	M
72-pin SIMM (Gold)	G
Operating Modes	
FAST PAGE MODE	None
EDO PAGE MODE	X
*EDO version only	

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	PLATING
MT8D432G- x X	4 Meg x 32	Gold
MT8D432M- x X	4 Meg x 32	Tin/Lead
MT16D832G-x X	8 Meg x 32	Gold
MT16D832M-x X	8 Meg x 32	Tin/Lead

x = speed

FPM Operating Mode

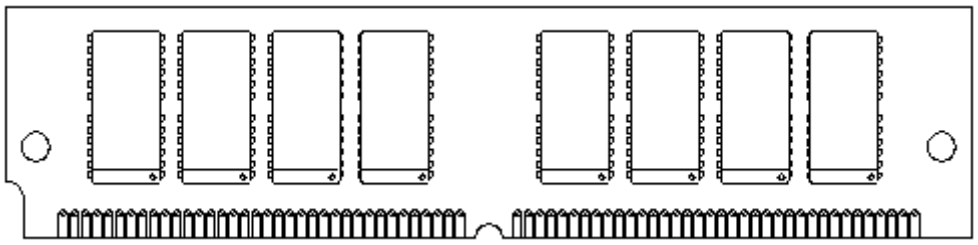
PART NUMBER	CONFIGURATION	PLATING
MT8D432G-x	4 Meg x 32	Gold
MT8D432M-x	4 Meg x 32	Tin/Lead
MT16D832G-x	8 Meg x 32	Gold
MT16D832M-x	8 Meg x 32	Tin/Lead

x = speed

PIN ASSIGNMENT (Front View)

72-Pin SIMM

4 Meg x 32
8 Meg x 32



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0#	58	DQ29
5	DQ18	23	DQ22	41	CAS2#	59	Vdd
6	DQ3	24	DQ7	42	CAS3#	60	DQ30
7	DQ19	25	DQ23	43	CAS1#	61	DQ14
8	DQ4	26	DQ8	44	RAS0#	62	DQ31
9	DQ20	27	DQ24	45	NC/RAS1#*	63	DQ15
10	VDD	28	A7	46	NC	64	DQ32
11	NC	29	NC (A11)	47	WE#	65	DQ16
12	A0	30	VDD	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC/RAS3#*	51	DQ10	69	PRD3
16	A4	34	RAS2#	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

*32MB version only

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	tRC	tRAC	tPC	tAA	tCAC	tCAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

FPM Operating Mode

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns

GENERAL DESCRIPTION

The MT8D432(X) and MT16D832(X) are randomly ac cessed, 16MB and 32MB solid-state memories organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through 22 address bits that are entered 11 bits (A0-A10) at a time. RAS# is used to latch the first 11 bits and CAS# the latter 11 bits. READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS#. Since WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle.

FAST PAGE MODE

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address- defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (tCP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates like FAST-PAGE-MODE READs, ex- cept data will be held valid or become valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW. (Refer to the MT4C4M4E8 DRAM data sheet for additional information on EDO functionality.)

REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#- ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS# addresses are executed at least every 32ms, regard- less of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS# addressing. terminates the FAST-PAGE-MODE operation.

x16 CONFIGURATION

For x16 applications, the corresponding DQ and CAS# pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0# to CAS2# and CAS1# to CAS3#). Each RAS# is then a bank select for the x16 memory organization.

JEDEC-DEFINED
PRESENCE-DETECT
MT8D432(X) (16MB)

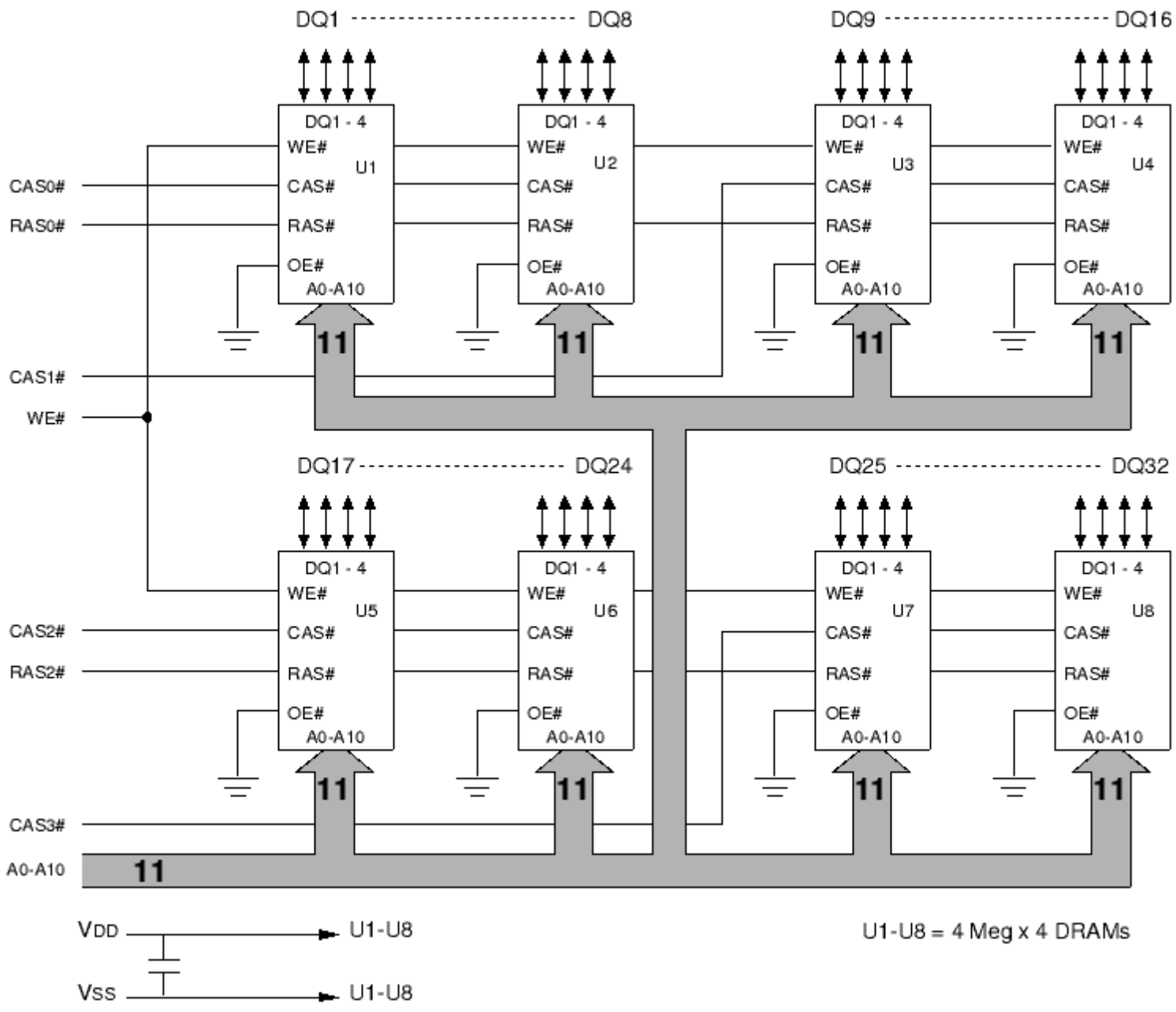
SYMBOL	PIN	-5*	-6
PRD1	67	VSS	VSS
PRD2	68	NC	NC
PRD3	69	VSS	NC
PRD4	70	VSS	NC

JEDEC-DEFINED
PRESENCE-DETECT
MT16D832(X) (32MB)

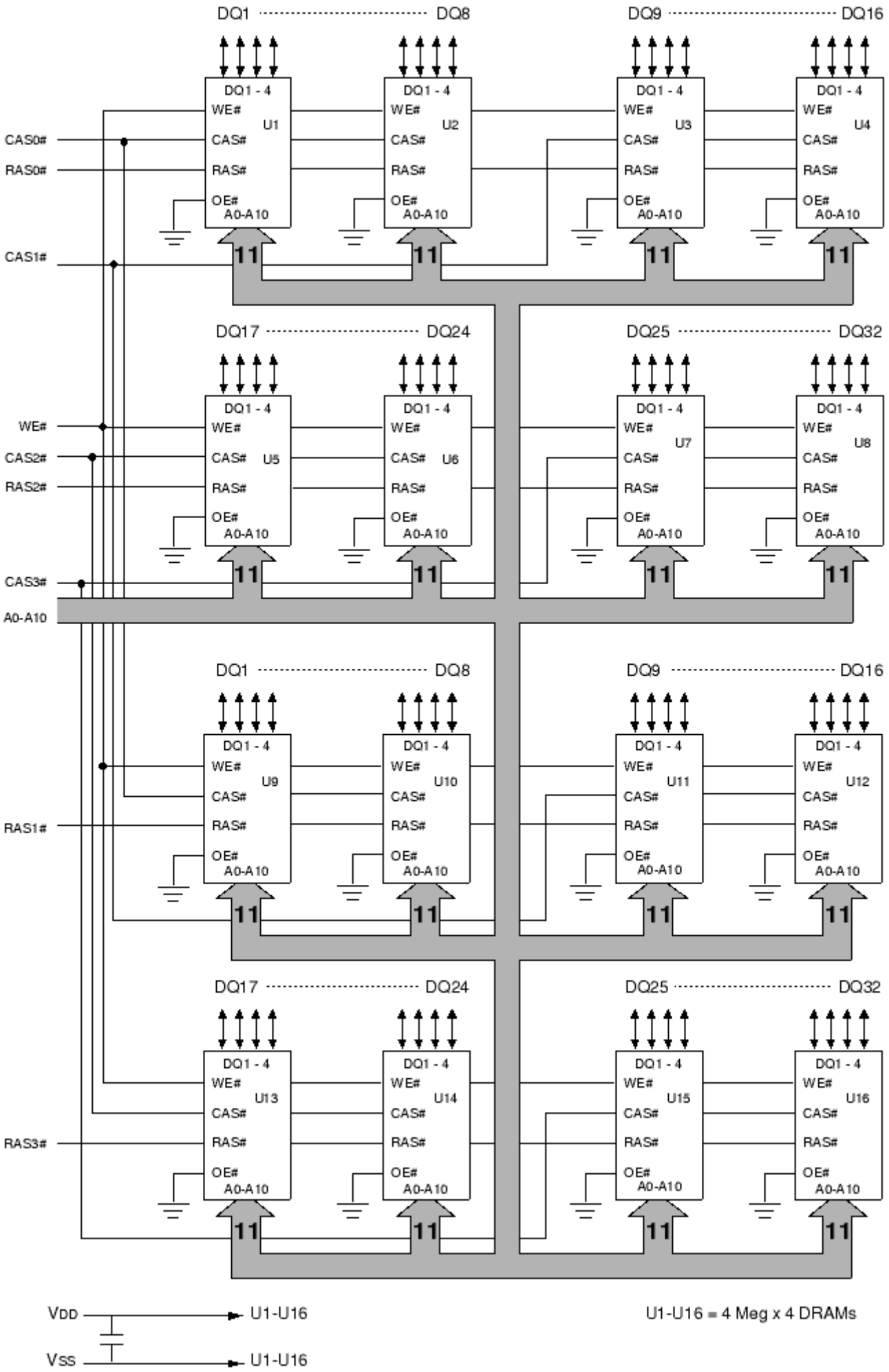
SYMBOL	PIN	-5*	-6
PRD1	67	NC	NC
PRD2	68	VSS	VSS
PRD3	69	VSS	NC
PRD4	70	VSS	NC

*EDO version only

FUNCTIONAL BLOCK DIAGRAM, MT8D432(X) (16MB)



FUNCTIONAL BLOCK DIAGRAM, MT16D832(X) (32MB)



ABSOLUTE MAXIMUM RATINGS*

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Voltage on Any Pin Relative to VSS ..................  -1V to +7V
Operating Temperature, TA (ambient) ..............  0°C to +70°C
Storage Temperature (plastic)...................  -55°C to +125°C
Power Dissipation ..........................................  8W
Short Circuit Output Current ..............................  50mA
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*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) (VDD = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	VDD	4.5	5.5	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	VIH	2.4	VDD + 1	V	

INPUT LOW VOLTAGE: Logic 0; All inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT:	RAS0# -RAS3#	II1	-8	8	µA	
Any input 0V VIN 5.5V	A0 -A10, WE#	II2	-32	32	µA	23
(All other pins not under test = 0V)	CAS0# -CAS3#	II3	-8	8	µA	23
OUTPUT LEAKAGE CURRENT:	DQ1 -DQ32	IOZ	-10	10	µA	23
(DQ is disabled; 0V VOUT 5.5V)						
OUTPUT LEVELS:		VOH	2.4		V	
Output High Voltage (IOUT = -5mA)						
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

ICC SPECIFICATIONS AND CONDITIONS

(Notes: 1, 5, 6) (VDD = +5V ±10%)

			MAX			
PARAMETER/CONDITION	SYMBOL	SIZE	-5*	-6	UNITS	NOTI
STANDBY CURRENT: FAST PAGE MODE (TTL)	ICC1	16MB		16	mA	
(RAS# = CAS# = VIH)		32MB		32		
STANDBY CURRENT: EDO PAGE MODE (TTL)	ICC2	16MB	8	8	mA	
(RAS# = CAS# = VIH)		32MB	16	16		
STANDBY CURRENT: (CMOS)	ICC3	16MB	4	4	mA	
(RAS# = CAS# = other inputs = VDD - 0.2V)		32MB	8	8		
OPERATING CURRENT: Random READ/WRITE		16MB	1120	1040	mA	3, 2
Average power supply current	ICC4					
(RAS#, CAS#, address cycling: tRC = tRC [MIN])		32MB	1128	1048		
OPERATING CURRENT: FAST PAGE MODE		16MB		800	mA	3, 2
Average power supply current	ICC5					
(RAS# = VIL, CAS#, address cycling: tPC = tPC [MIN]		32MB		816		
OPERATING CURRENT: EDO PAGE MODE	ICC6	16MB	880	800	mA	3, 2
Average power supply current	(X only)					
(RAS# = VIL, CAS#, address cycling: tPC = tPC [MIN])		32MB	888	808		
REFRESH CURRENT: RAS#-ONLY		16MB	1120	1040		
Average power supply current	ICC7				mA	3, 2
(RAS# cycling, CAS# = VIH: tRC = tRC [MIN])		32MB	1128	1048		
REFRESH CURRENT: CBR		16MB	1120	1040		
Average power supply current	ICC8				mA	3, 4
(RAS#, CAS#, address cycling: tRC = tRC [MIN])		32MB	1128	1048		

*EDO version only

CAPACITANCE

		MAX			
PARAMETER	SYMBOL	16MB	32MB	UNITS	NOTES
Input Capacitance: A0-A10	CI1	48	95	pF	2
Input Capacitance: WE#	CI2	64	127	pF	2
Input Capacitance: RAS0#-RAS3#	CI3	32	32	pF	2
Input Capacitance: CAS0#-CAS3#	CI4	16	32	pF	2
Input/Output Capacitance: DQ1-DQ32	CIO	10	16	pF	2

AC ELECTRICAL CHARACTERISTICS, FAST PAGE MODE

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (VDD = +5V ±10%)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		
PARAMETER	SYMBOL	MIN	MAX	UN
Access time from column address	tAA		30	
Column-address hold time (referenced to RAS#)	tAR	45		
Column-address setup time	tASC	0		
Row-address setup time	tASR	0		
Access time from CAS#	tCAC		15	
Column-address hold time	tCAH	10		
CAS# pulse width	tCAS	15	10,000	
CAS# hold time (CBR Refresh)	tCHR	10		
CAS# to output in Low-Z	tCLZ	3		
CAS# precharge time	tCP	10		
Access time from CAS# precharge	tCPA		35	
CAS# to RAS# precharge time	tCRP	5		
CAS# hold time	tCSH	60		
CAS# setup time (CBR Refresh)	tCSR	5		
WRITE command to CAS# lead time	tCWL	15		
Data-in hold time	tDH	10		
Data-in setup time	tDS	0		
Output buffer turn-off delay	tOFF	3	15	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		
Access time from RAS#	tRAC		60	
RAS# to column-address delay time	tRAD	15		
Row-address hold time	tRAH	10		
RAS# pulse width	tRAS	60	10,000	
RAS# pulse width (FAST PAGE MODE)	tRASP	60	125,000	
Random READ or WRITE cycle time	tRC	110		
RAS# to CAS# delay time	tRCD	20		
READ command hold time (referenced to CAS#)	tRCH	0		
READ command setup time	tRCS	0		
Refresh period (2,048 cycles)	tREF		32	
RAS# precharge time	tRP	40		
RAS# to CAS# precharge time	tRPC	0		
READ command hold time (referenced to RAS#)	tRRH	0		
RAS# hold time	tRSH	15		
WRITE command to RAS# lead time	tRWL	15		
Transition time (rise or fall)	tT	2	50	
WRITE command hold time	tWCH	10		
WRITE command hold time (referenced to RAS#)	tWCR	45		

WE# command setup time	tWCS	0
WRITE command pulse width	tWP	10
WE# hold time (CBR Refresh)	tWRH	10
WE# setup time (CBR Refresh)	tWRP	10

AC ELECTRICAL CHARACTERISTICS, EDO PAGE MODE

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (VDD = +5V ±10%)

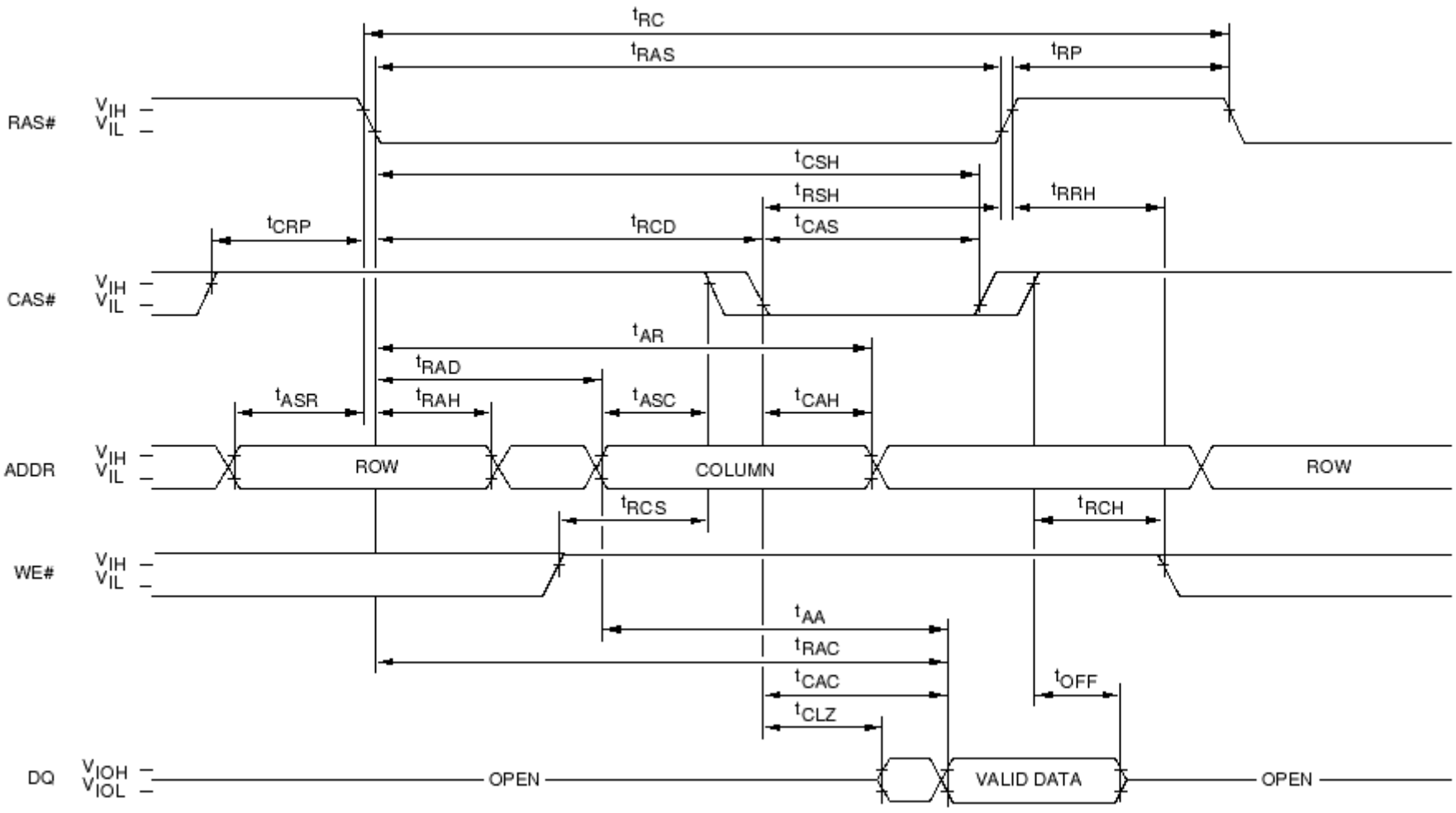
AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6	
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX
Access time from column address	tAA		25		30
Column-address set-up to CAS# precharge	tACH	12		15	
Column-address hold time (referenced to RAS#)	tAR	38		45	
Column-address setup time	tASC	0		0	
Row-address setup time	tASR	0		0	
Access time from CAS#	tCAC		13		15
Column-address hold time	tCAH	8		10	
CAS# pulse width	tCAS	8	10,000	10	10,00
CAS# hold time (CBR Refresh)	tCHR	8		10	
CAS# to output in Low-Z	tCLZ	0		0	
Data output hold after next CAS# LOW	tCOH	3		3	
CAS# precharge time	tCP	8		10	
Access time from CAS# precharge	tCPA		28		35
CAS# to RAS# precharge time	tCRP	5		5	
CAS# hold time	tCSH	38		45	
CAS# setup time (CBR Refresh)	tCSR	5		5	
WRITE command to CAS# lead time	tCWL	8		10	
Data-in hold time	tDH	8		10	
Data-in setup time	tDS	0		0	
Output buffer turn-off delay	tOFF	0	12	0	15
EDO-PAGE-MODE READ or WRITE cycle time	tPC	20		25	
Access time from RAS#	tRAC		50		60
RAS# to column-address delay time	tRAD	9		12	
Row-address hold time	tRAH	9		10	
RAS# pulse width	tRAS	50	10,000	60	10,00
RAS# pulse width (EDO PAGE MODE)	tRASP	50	125,000	60	125,0
Random READ or WRITE cycle time	tRC	84		104	
RAS# to CAS# delay time	tRCD	11		14	
READ command hold time (referenced to CAS#)	tRCH	0		0	
READ command setup time	tRCS	0		0	
Refresh period (2,048 cycles)	tREF		32		32
RAS# precharge time	tRP	30		40	
RAS# to CAS# precharge time	tRPC	5		5	
READ command hold time (referenced to RAS#)	tRRH	0		0	
RAS# hold time	tRSH	13		15	
WRITE command to RAS# lead time	tRWL	13		15	
Transition time (rise or fall)	tT	2	50	2	50
WRITE command hold time	tWCH	8		10	
WRITE command hold time (referenced to RAS#)	tWCR	38		45	
WE# command setup time	tWCS	0		0	
Output disable delay from WE#	tWHZ	0	12	0	15
WRITE command pulse width	tWP	5		5	
WE# pulse to disable at CAS# HIGH	tWPZ	10		10	
WE# hold time (CBR Refresh)	tWRH	8		10	
WE# setup time (CBR Refresh)	tWRP	8		10	

NOTES

1. All voltages referenced to VSS.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, VDD = 4.5V, DC bias = 2.4V at 15mV RMS).
3. ICC is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded.
7. AC characteristics assume tT = 5ns for FPM and tT = 2.5ns for EDO.
8. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
9. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
10. If CAS# = VIH, data output is High-Z.
11. If CAS# = VIL, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF, VOL = 0.8V and VOH = 2V.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for tCP.
14. The tRCD (MAX) limit is no longer specified. tRCD (MAX) was specified as a reference point only. If tRCD was greater than the specified tRCD (MAX) limit, then access time was controlled exclusively by tCAC (tRAC [MIN] no longer applied). With or without the tRCD (MAX) limit, tAA and tCAC must always be met.
15. The tRAD (MAX) limit is no longer specified. tRAD (MAX) was specified as a reference point only. If tRAD was greater than the specified tRAD (MAX) limit, then access time was controlled exclusively by tAA (tRAC and tCAC no longer applied). With or without the tRAD (MAX) limit, tAA, tRAC and tCAC must always be met.
16. Either tRCH or tRRH must be satisfied for a READ cycle.
17. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
18. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles.
19. OE# is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.

21. The 3ns minimum is a parameter guaranteed by design.
22. Column address changed once each cycle.
23. 16MB module values will be half of those shown.
24. For the FPM option, tOFF is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, tOFF on an EDO option is determined by the latter of the RAS# and CAS# signals to transition HIGH.
25. Applies to both EDO and FPM modules.

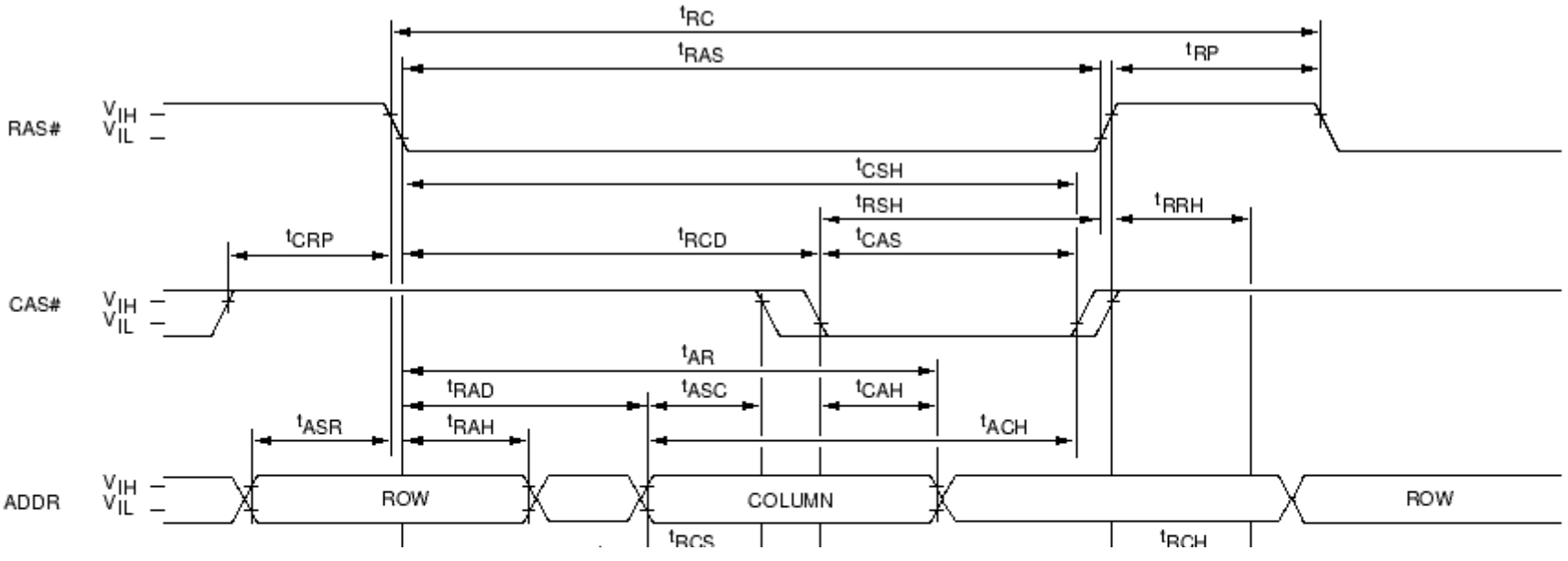
READ CYCLE (FAST PAGE MODE Module)

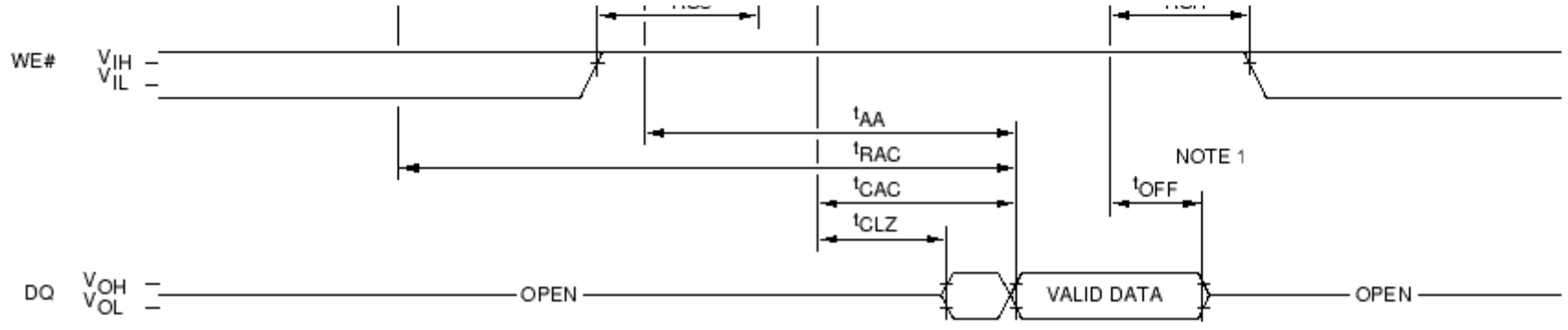


FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	MAX	UNITS	SYMBOL
tAA		30	ns	tRAC
tAR	45		ns	tRAD
tASC	0		ns	tRAH
tASR	0		ns	tRAS
tCAC		15	ns	tRC
tCAH	10		ns	tRCD
tCAS	15	10,000	ns	tRCH
tCLZ	3		ns	tRCS
tCRP	5		ns	tRP
tCSH	60		ns	tRRH
tOFF	3	15	ns	tRSH

READ CYCLE (EDO PAGE MODE Module)



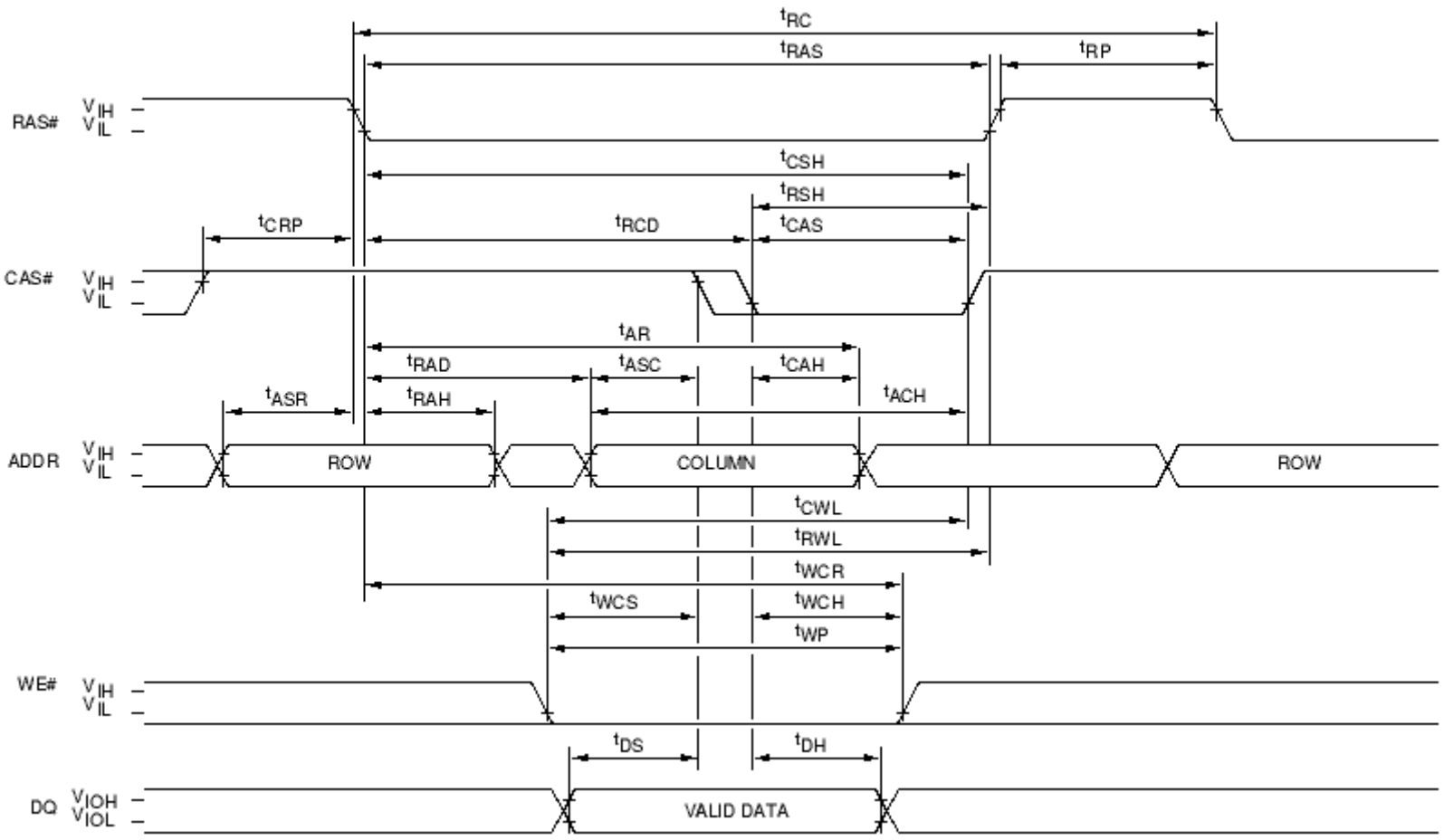


EDO PAGE MODE TIMING PARAMETERS

	-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tOFF	0	12	0	15	ns

NOTE: 1. tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

EARLY WRITE CYCLE[25]



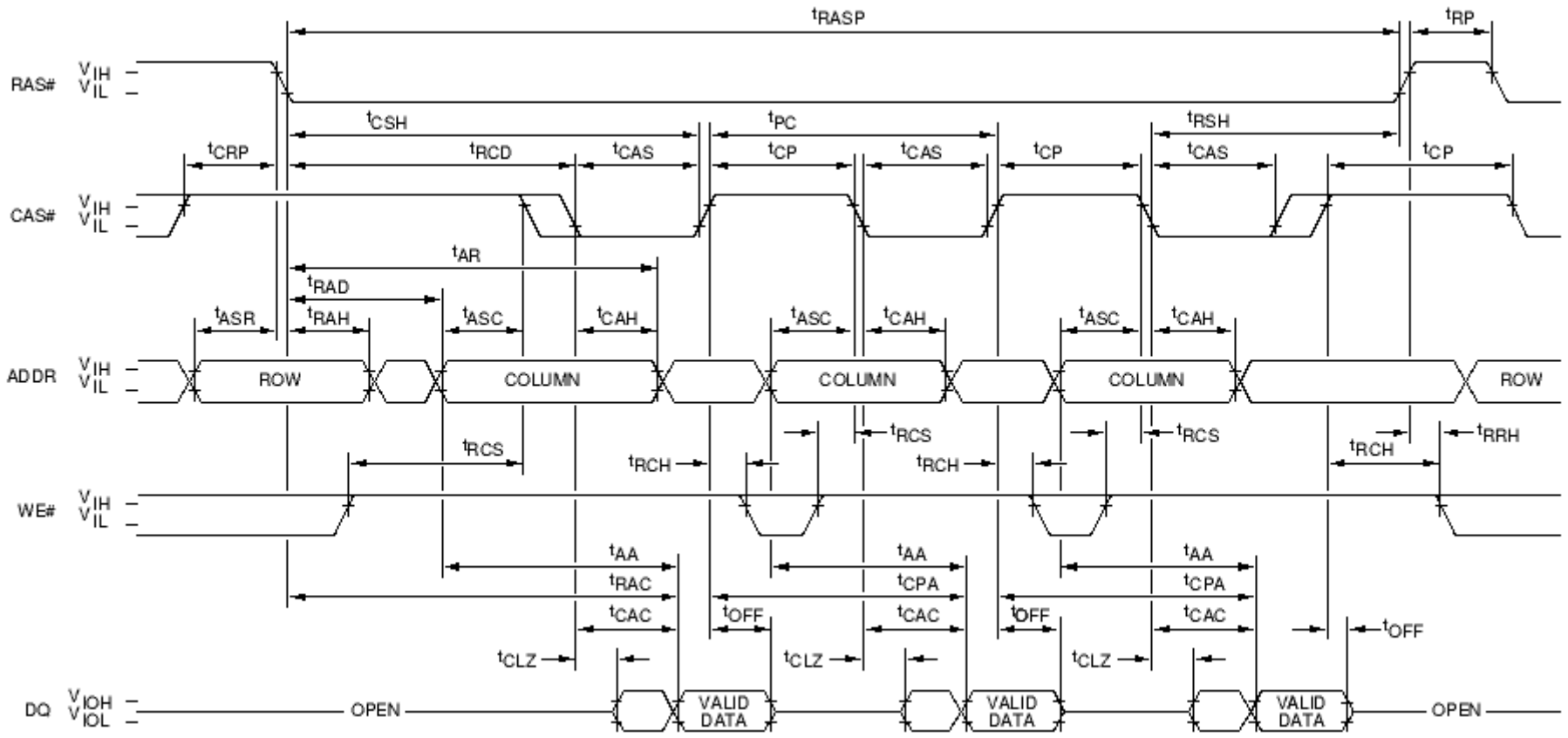
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tACH (EDO)	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS (FPM)			15	10,000	ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCRP	5		5		ns
tCSH (FPM)			60		ns
tCSH (EDO)	38		45		ns
tCWL (FPM)			15		ns

CWL (EDO)	8	10	ns
t DH	8	10	ns
t DS	0	0	ns
t RAD (FPM)		15	ns

*EDO version only

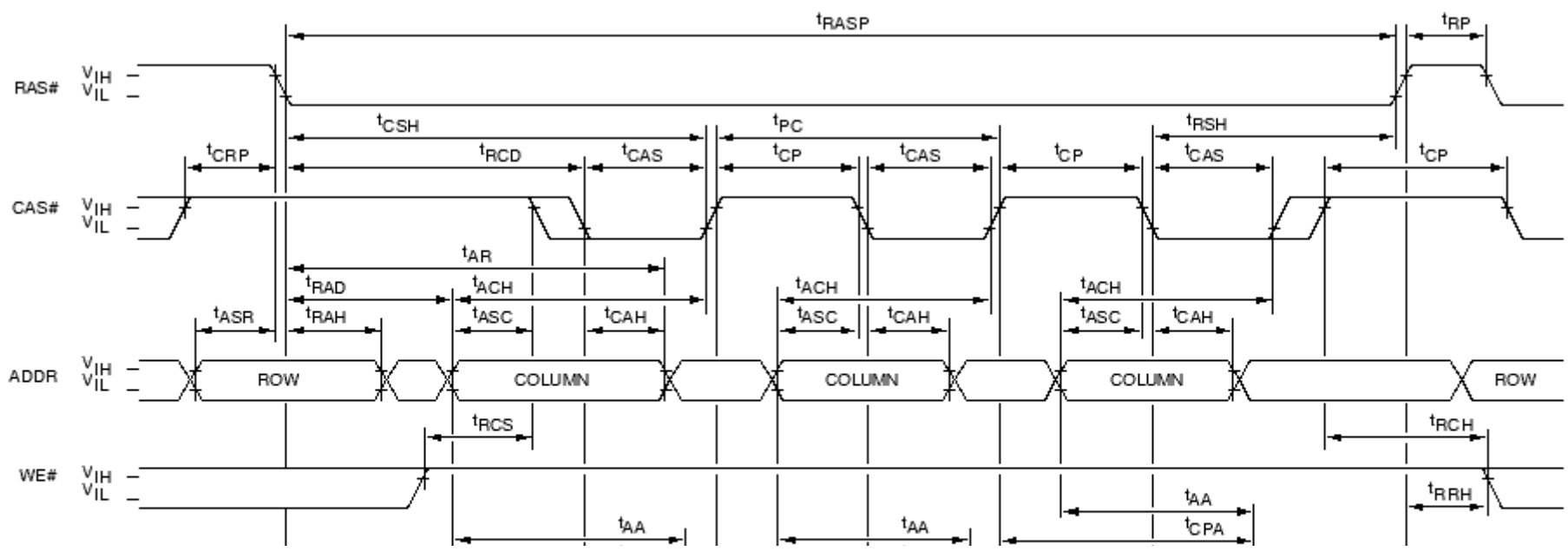
FAST-PAGE-MODE READ CYCLE

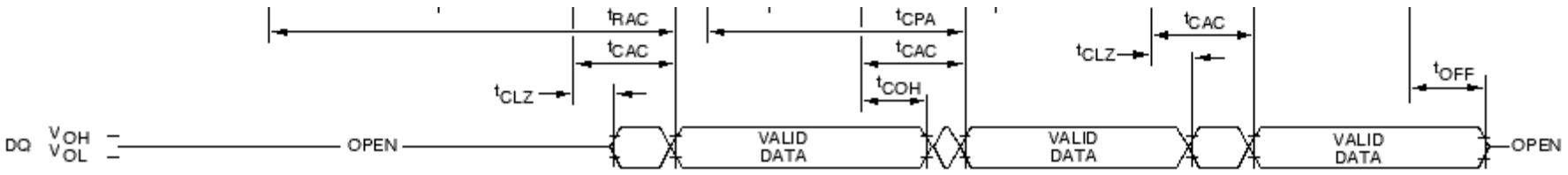


FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	MAX
t AA		30
t AR	45	
t ASC	0	
t ASR	0	
t CAC		15
t CAH	10	
t CAS	15	10,000
t CLZ	3	
t CP	10	
t CPA		35
t CRP	5	
t CSH	60	

EDO-PAGE-MODE READ CYCLE

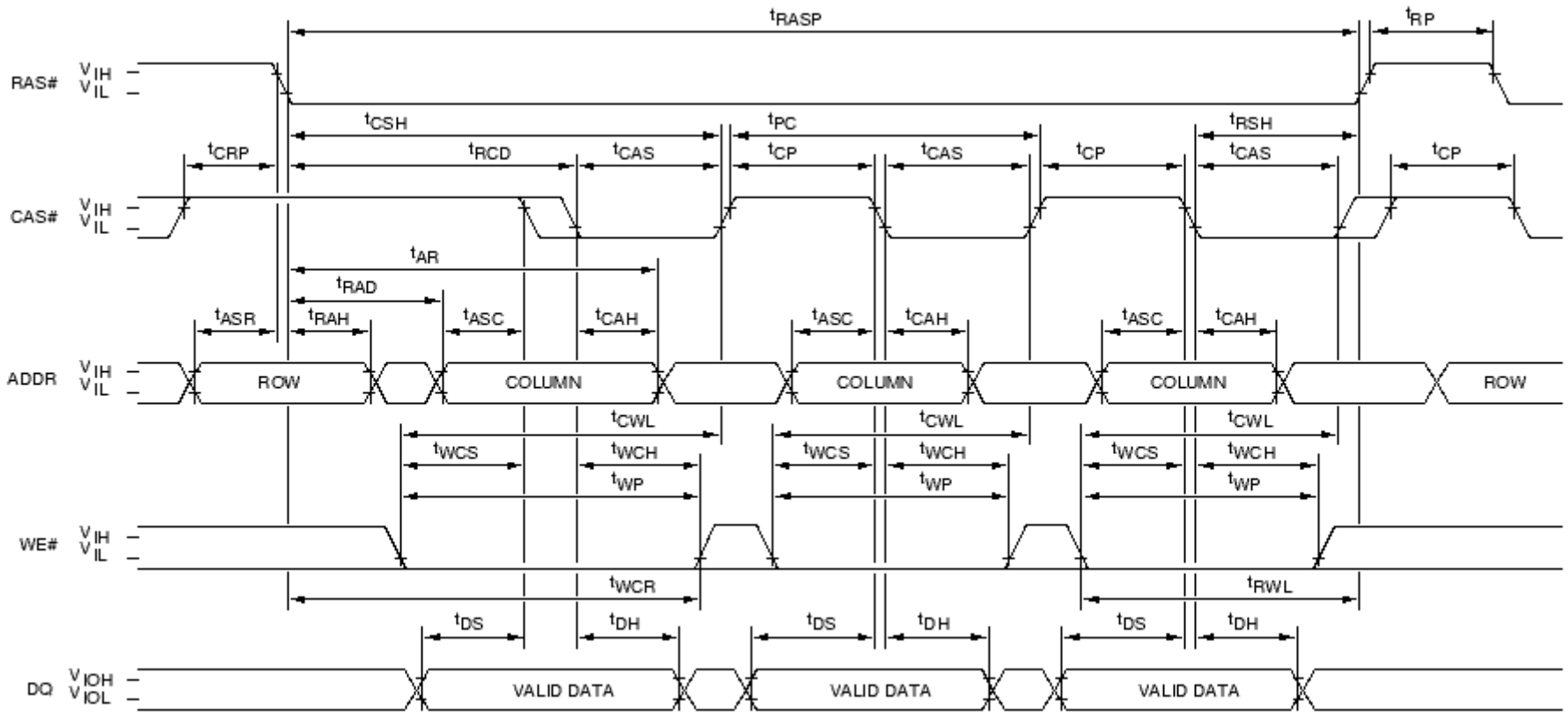




EDO PAGE MODE TIMING PARAMETERS

	-5		-6	
SYMBOL	MIN	MAX	MIN	MAX
tAA		25		30
tACH	12		15	
tAR	38		45	
tASC	0		0	
tASR	0		0	
tCAC		13		15
tCAH	8		10	
tCAS	8	10,000	10	10,000
tCLZ	0		0	
tCOH	3		3	
tCP	8		10	
tCPA		28		35
tCRP	5		5	

FAST-PAGE-MODE EARLY-WRITE CYCLE

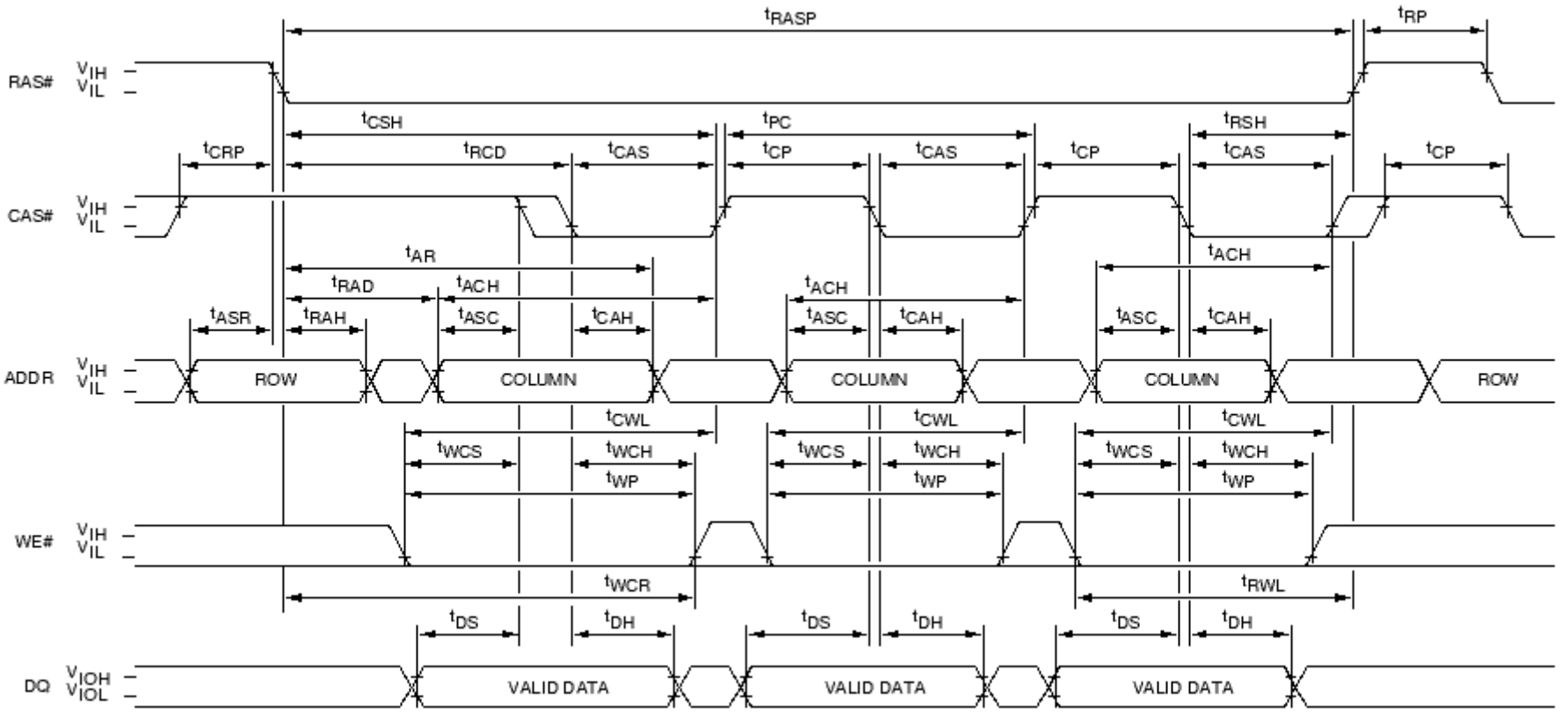


FAST PAGE MODE TIMING PARAMETERS

	-6	
SYMBOL	MIN	MAX
tAR	45	
tASC	0	
tASR	0	
tCAH	10	
tCAS	15	10,000
tCP	10	
tCRP	5	
tCSH	60	
tCWL	15	
tDH	10	

DS	0
tPC	35

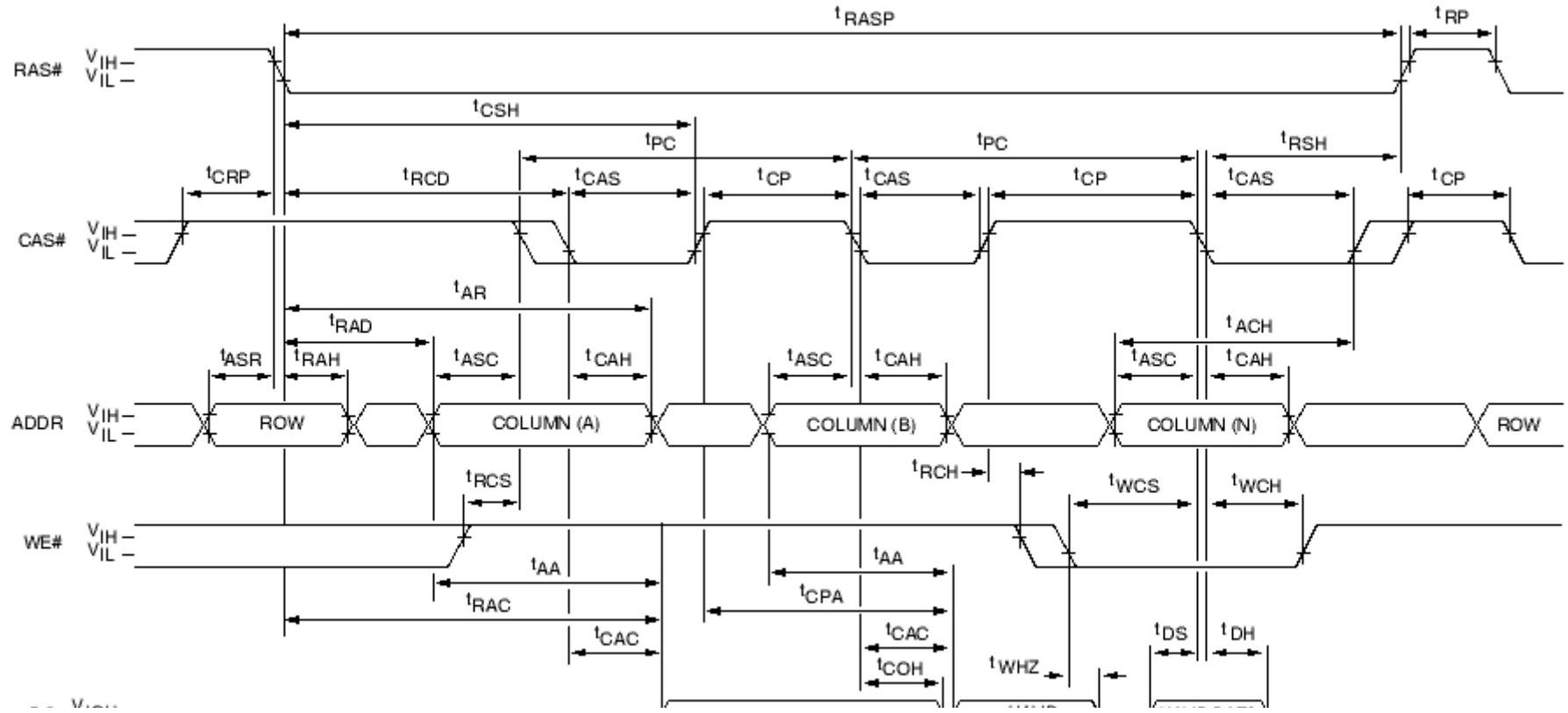
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO PAGE MODE TIMING PARAMETERS

	-5		-6	
SYMBOL	MIN	MAX	MIN	MAX
tACH	12		15	
tAR	38		45	
tASC	0		0	
tASR	0		0	
tCAH	8		10	
tCAS	8	10,000	10	10,000
tCP	8		10	
tCRP	5		5	
tCSH	38		45	
tCWL	8		10	
tDH	8		10	
tDS	0		0	

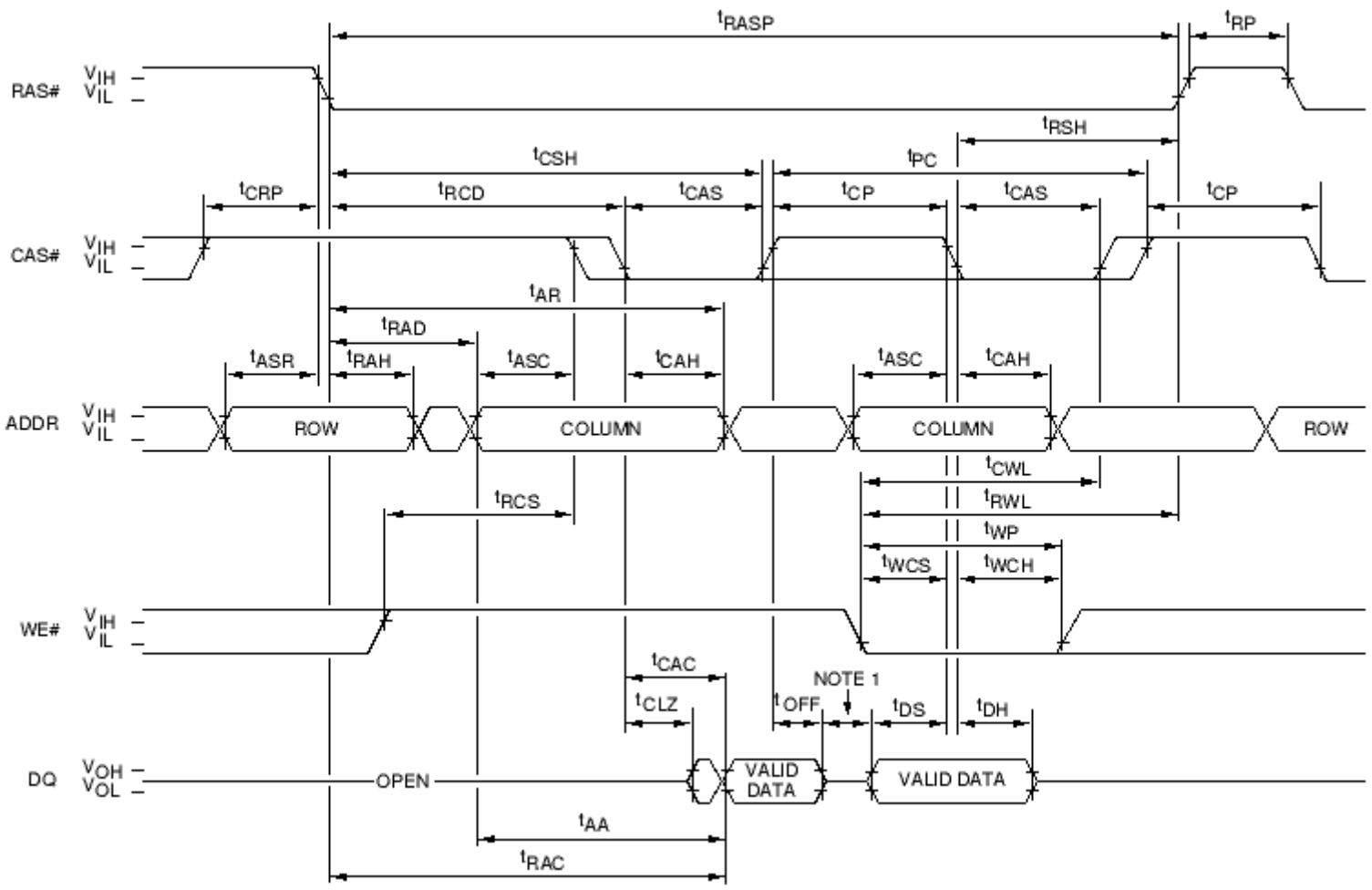
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY-WRITE)



EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	n
tACH	12		15		n
tAR	38		45		n
tASC	0		0		n
tASR	0		0		n
tCAC		13		15	n
tCAH	8		10		n
tCAS	8	10,000	10	10,000	n
tCOH	3		3		n
tCP	8		10		n
tCPA		28		35	n
tCRP	5		5		n
tCSH	38		45		n
tDH	8		10		n

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY-WRITE)

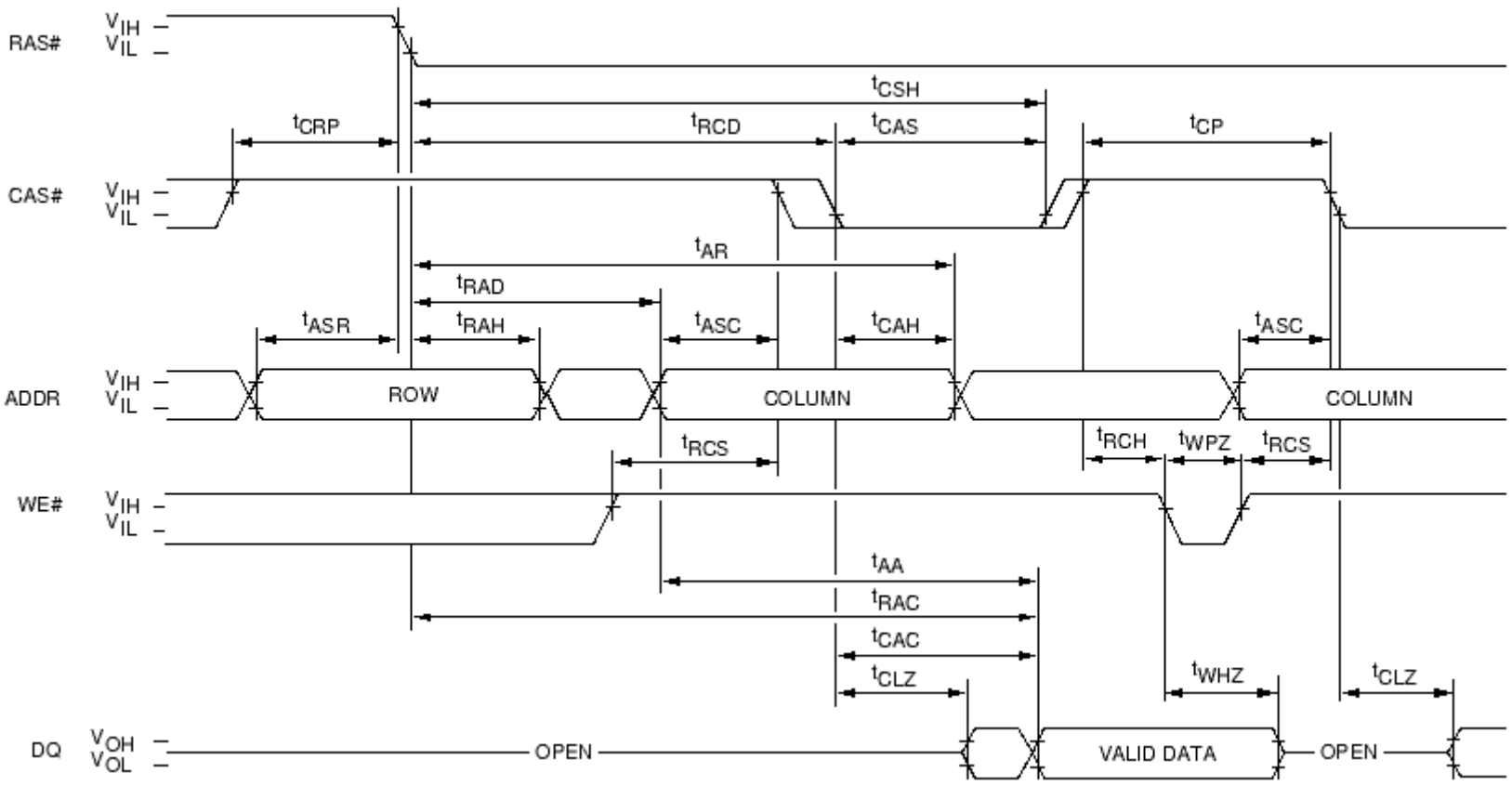


FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCP	10		ns

t_{CRP}	5	ns
t_{CSH}	60	ns
t_{CWL}	15	ns
t_{DH}	10	ns
t_{DS}	0	ns

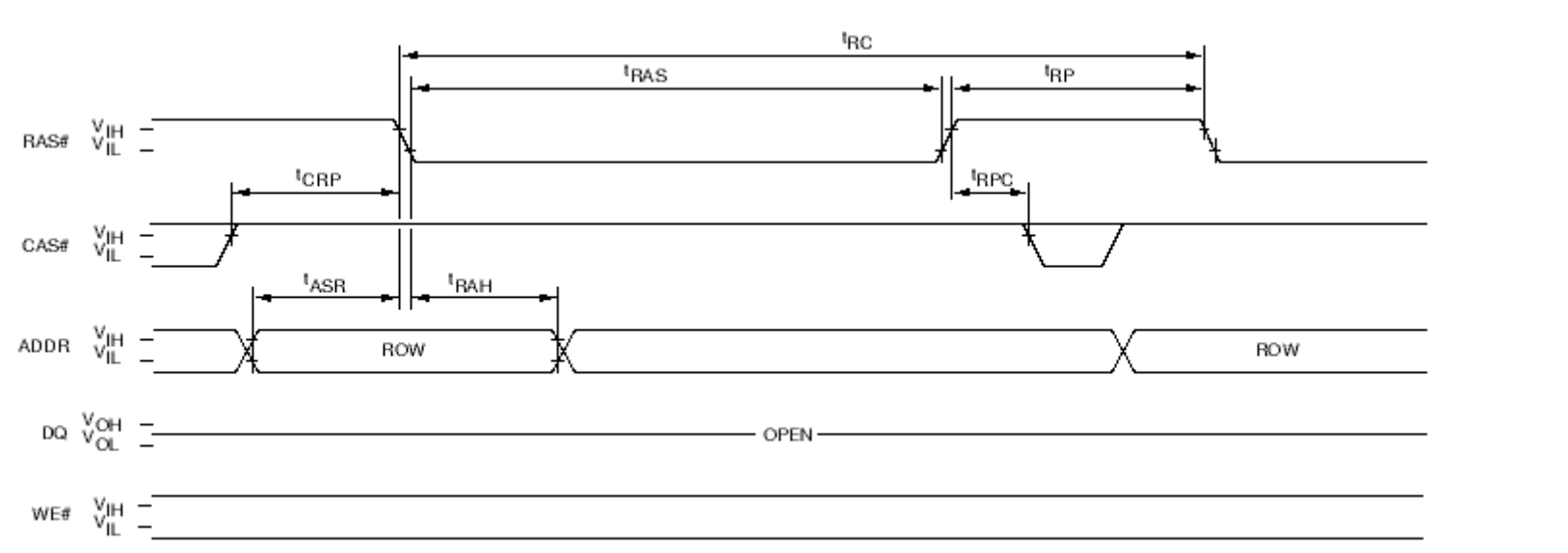
EDO READ CYCLE (with WE#-controlled disable)



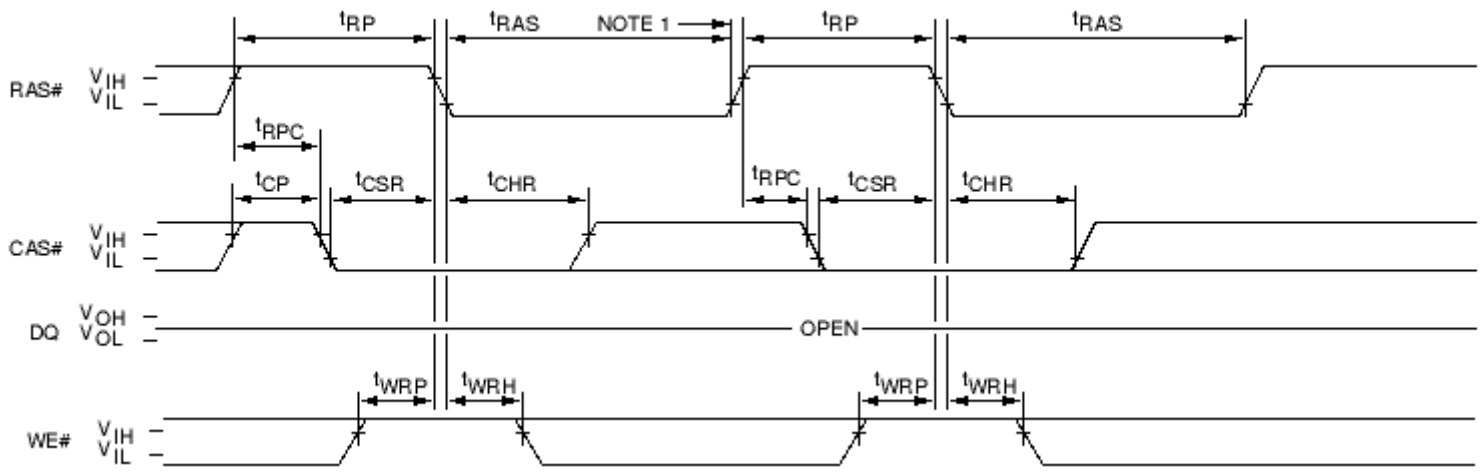
EDO PAGE MODE TIMING PARAMETERS

	-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCRP	5		5		ns

RAS#-ONLY REFRESH CYCLE 25



CBR REFRESH CYCLE 25 (Addresses = DON'T CARE)

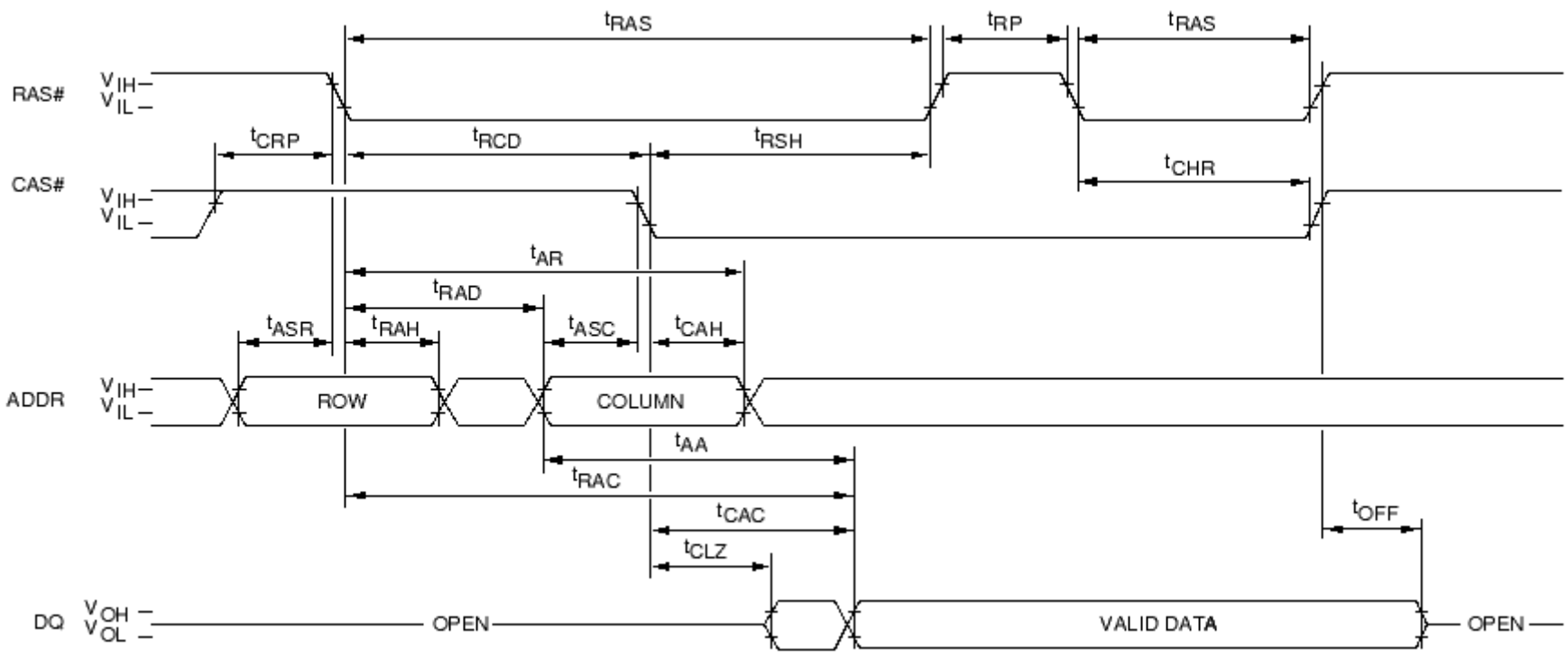


FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tASR	0		0		ns
tCHR (FPM)			10		ns
tCHR (EDO)	8		10		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSR	5		5		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns

*EDO version only

HIDDEN REFRESH CYCLE 20, 25 (WE# = HIGH)



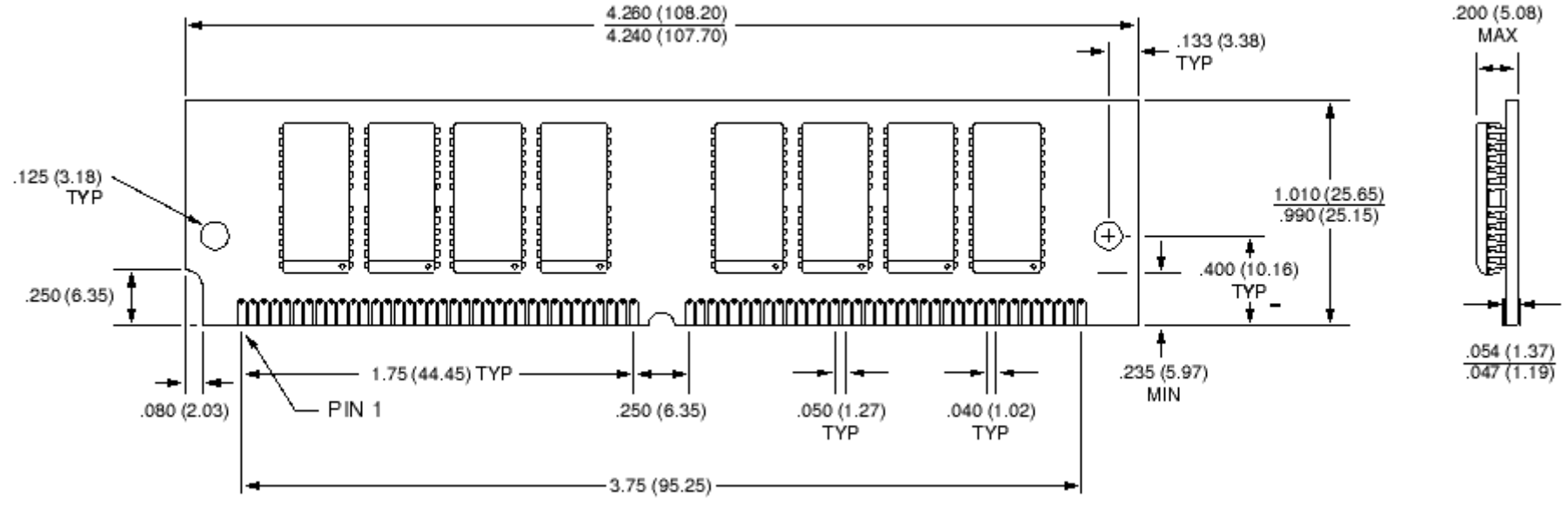
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCHR	8		10		ns
tCLZ (FPM)			3		ns
tCLZ (EDO)	0		0		ns

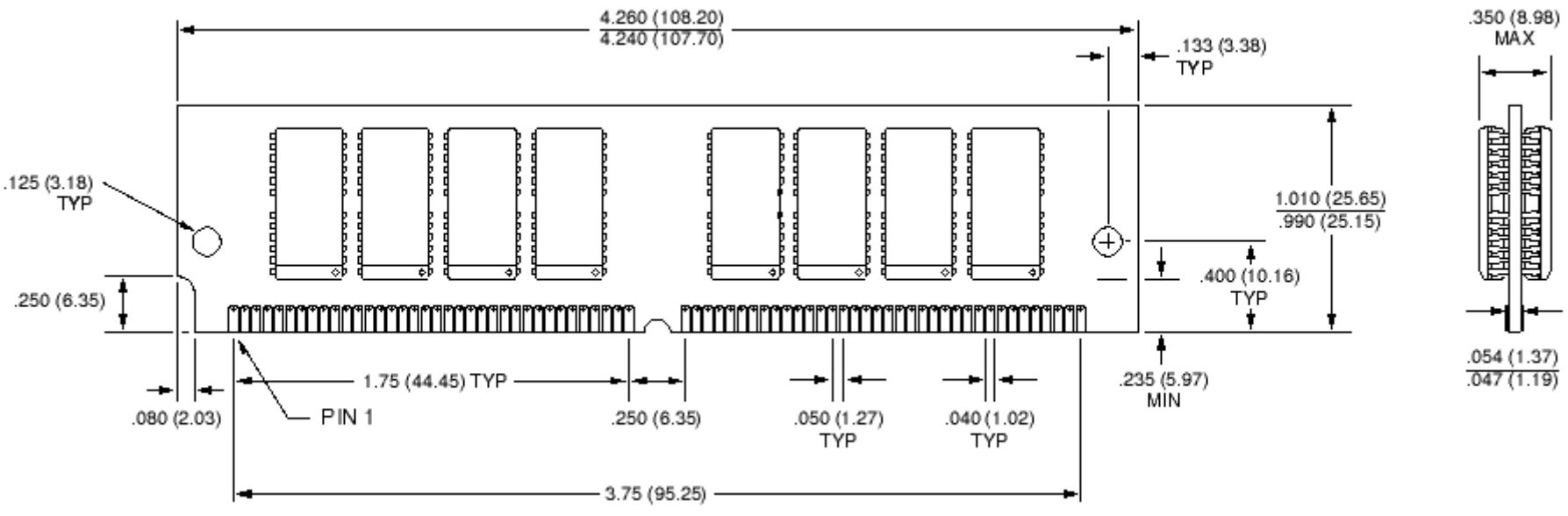
CRP	5	5	ns
tOFF (FPM)		3 15	ns

*EDO version only

72-Pin SIMM (16MB)



72-Pin SIMM (32MB)



NOTE: 1. All dimensions in inches (millimeters) MAX or typical where noted.

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