National Semiconductor

October 2000

LM4865 Boomer® Audio Power Amplifier Series
750 mW Audio Power Amplifier with DC Volume Control and Headphone Switch

General Description

The LM4865 is a mono bridged audio power amplifier with DC voltage volume control. The LM4865 is capable of delivering 750mW of continuous average power into an 8Ω load with less than 1% THD when powered by a 5V power supply. Switching between bridged speaker mode and headphone (single ended) mode is accomplished using the headphone sense pin. To conserve power in portable applications, the LM4865's micropower shutdown mode (I_Q = 0.7µA, typ) is activated when less than 300mV is applied to the DC Vol/$\overline{SD}$ pin.

Boomer audio power amplifiers are designed specifically to provide high power audio output while maintaining high fidelity. They require few external components and operate on low supply voltages.

Applications

- GSM phones and accessories, DECT, office phones
- Hand held radio
- Other portable audio devices

Key Specifications

- P_O at 1.0% THD+N into 8Ω SO, micro SMD — 750mW (typ)
- P_O at 10% THD+N into 8Ω SO, micro SMD — 1W (typ)
- Shutdown current — 0.7µA(typ)
- Supply voltage range — 2.7V to 5.5V

Features

- DC voltage volume control
- Headphone amplifier mode
- "Click and pop" suppression
- Shutdown control when volume control pin is low
- Thermal shutdown protection

Typical Application

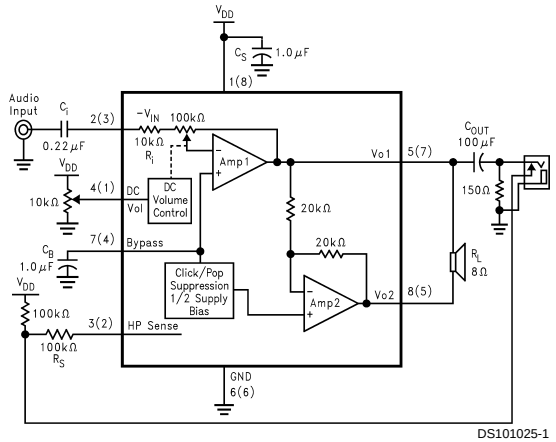

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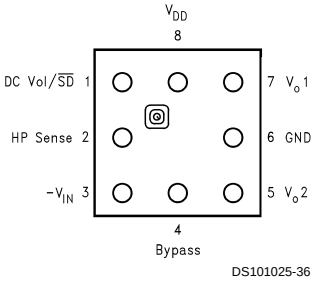
FIGURE 1. Typical Audio Amplifier Application Circuit
(Numbers in ( ) are specific to the micro SMD package)

Connection Diagram

micro SMD Package



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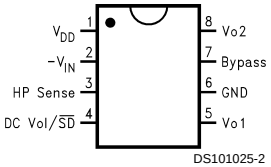
Top View
Order Number LM4865IBP
See NS Package Number BPA08CFB

Small Outline Package (SO)
Mini Small Outline Package (MSOP)



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Top View
Order Number LM4865M, LM4865MM
See NS Package Number M08A, MUA08A

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Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150˚C
Soldering Information	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C
Thermal Resistanc	
θ_{JC} (SOP)	35˚C/W
θ_{JA} (SOP)	150˚C/W
θ_{JC} (MSOP)	56˚C/W
θ_{JA} (MSOP)	190˚C/W
θ_{JA} (micro SMD)	150˚C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40˚C \le T_A \le +85˚C$
Supply Voltage	$2.7V \le V_{DD} \le 5.5V$

See AN-450 “Surface Mounting and their Effects on Product Reliability” for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

The following specifications apply for V_{DD} = 5V, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4865			
			Min (Note 7)	Typical (Note 6)	Max (Note 7)	Units
V_{DD}	Supply Voltage		2.7		5.5	V
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, HP Sense = 0V		4	7	mA
		V_{IN} = 0V, I_O - 0A, HP Sense = 5V		3.5	6	mA
I_{SD}	Shutdown Current	$V_{PIN4} \le 0.3V$		0.7		µA
V_{OS}	Output Offset Voltage	V_{IN} = 0V		5	50	mV
P_O	Output Power	THD = 1% (max), HP Sense < 0.8V, f = 1kHz, R_L = 8Ω	500	750		mW
		THD = 10% (max), HP Sense < 0.8V, f = 1kHz, R_L = 8Ω		1.0		W
		THD + N = 1%, HP Sense > 4V, f = 1kHz, R_L = 32Ω		80		mW
		THD = 10%, HP Sense > 4V, f = 1kHz, R_L = 32Ω		110		mW
THD+N	Total Harmonic Distortion + Noise	P_O = 300 mWrms, f = 20Hz–20kHz, R_L = 8Ω		0.6		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVrms, R_L = 8Ω, C_B = 1.0 µF, f = 1kHz		50		dB
$Gain_{RANGE}$	Single-Ended Gain Range	Gain with $V_{PIN4} \ge 4.0V$, (80% of V_{DD})	18.8	20		dB
		Gain with $V_{PIN4} \le 0.9V$, (18% of V_{DD})	−70	−72		dB
V_{IH}	HP Sense High Input Voltage		4			V
V_{IL}	HP Sense Low Input Voltage				0.8	V

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *“Absolute Maximum Ratings”* indicate limits beyond which damage to the device may occur. *“Operating Ratings”* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *“Electrical Characteristics”* state DC and AC electrical specifications under particular test conditions that guarantee specific performance limits. This assumes that the device operates within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given. The typical value, however, is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4865M, T_{JMAX} = 150˚C.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF–240pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

Note 7: Limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

Note 8: The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.

Application Information (Continued)

outputs track the voltage applied to the bypass pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the bypass pin is stable, the device becomes fully operational and the gain is set by the external voltage applied to the DC Vol/$\overline{SD}$ pin.

Although the bypass pin current cannot be modified, changing the size of C_B alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of C_B reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_B increases, the turn-on time increases. There is a linear relationship between the size of CB and the turn-on time. Shown below are some typical turn-on times for various values of C_B:

C_B	T_{ON}
0.01µF	20ms
0.1µF	200ms
0.22µF	420ms
0.47µF	840ms
1.0µF	2sec

In order eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause "clicks and pops". In a single-ended configuration, the output coupling capacitor, C_{OUT}, is of particular concern. This capacitor discharges through an internal 20kΩ resistor. Depending on the size of C_{OUT}, the time constant can be relatively large. To reduce transients in single-ended mode, an external 1kΩ - 5kΩ resistor can be placed in parallel with the internal 20kΩ resistor. The tradeoff for using this resistor is increased quiescent current.

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figure 4 through *Figure 6* show the recommended two-layer PC board layout that is optimized for the SO-8 packaged LM4865 and associated external components. *Figure 7* through *Figure 11* show the recommended four-layer PC board layout for the micro SMD packaged LM4865. A four-layer board is recommended when using the micro SMD packaged LM4865: the two inner layers, one connected to the GND pin, the other to the V_{DD} pin, provide heatsinking. Both layouts are designed for use with an external 5V supply, 8Ω speakers, and 32Ω headphones. The schematic for both recommended PC board layouts is *Figure 1*.

Both circuit boards are easy to use. Apply a 5V supply voltage and ground to the board's V_{DD} and GND pads, respectively. Connect a speaker with an 8Ω minimum impedance between the board's -OUT and +OUT pads. For headphone use, the layout has provisions for a headphone jack, J1. When a jack is connected as shown, inserting a headphone plug automatically switches off the external speaker.

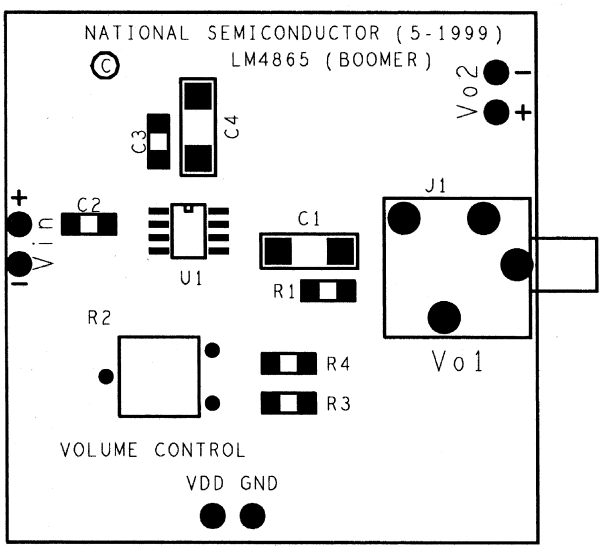

FIGURE 4. Recommended SO PC board layout: component side silkscreen

Application Information (Continued)

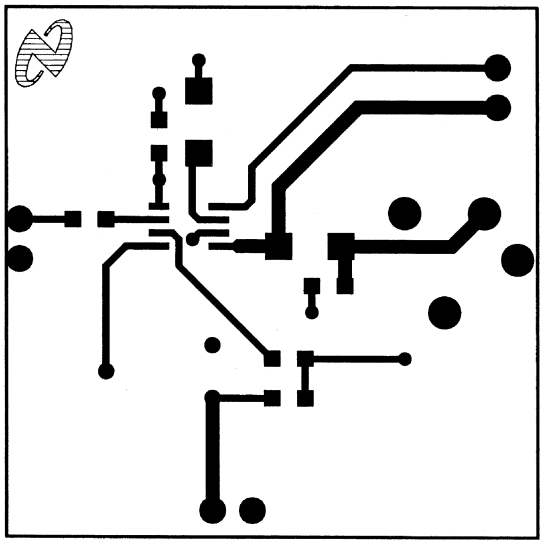

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FIGURE 5. Recommended SO PC board layout: component side layout

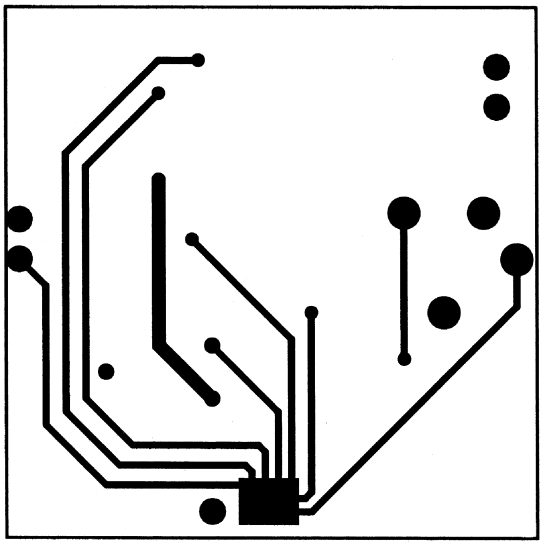

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FIGURE 6. Recommended SO PC board layout: bottom side layout

Application Information (Continued)

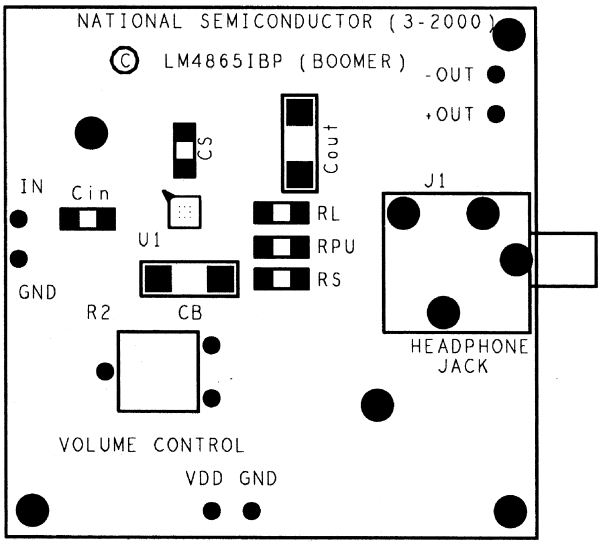

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FIGURE 7. Recommended micro SMD PC board layout: component side silkscreen

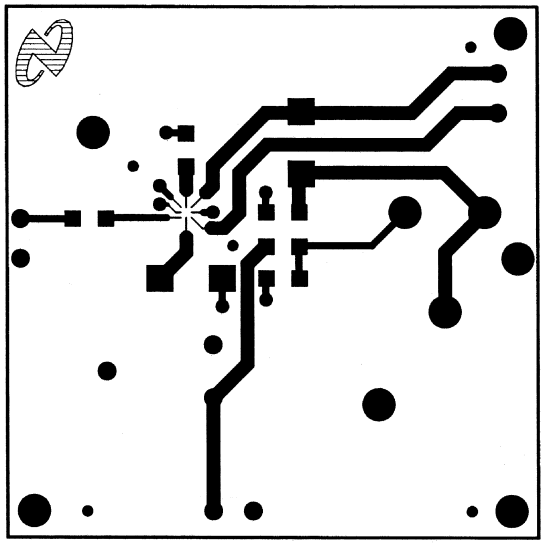

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FIGURE 8. Recommended micro SMD PC board layout: component side layout

Application Information (Continued)

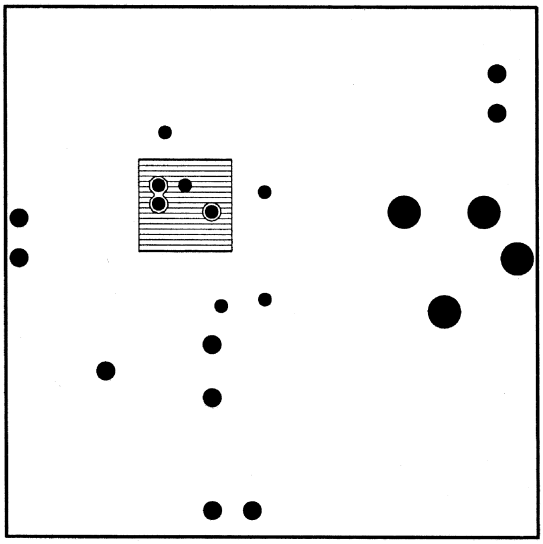

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FIGURE 9. Recommended micro SMD PC board layout: Inner layer V_{CC} layout

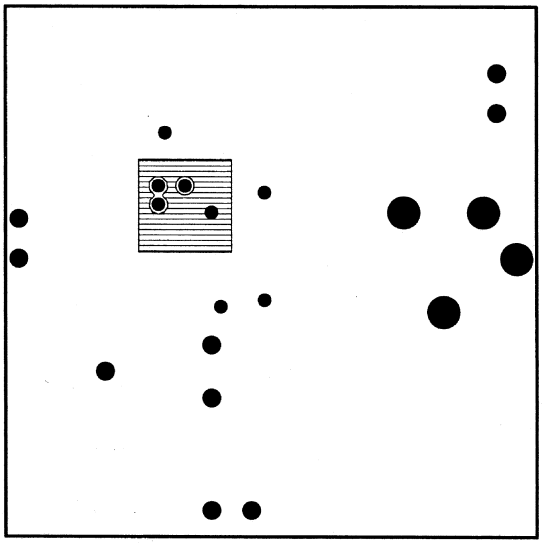

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FIGURE 10. Recommended micro SMD PC board layout: Inner layer ground layout

Application Information (Continued)

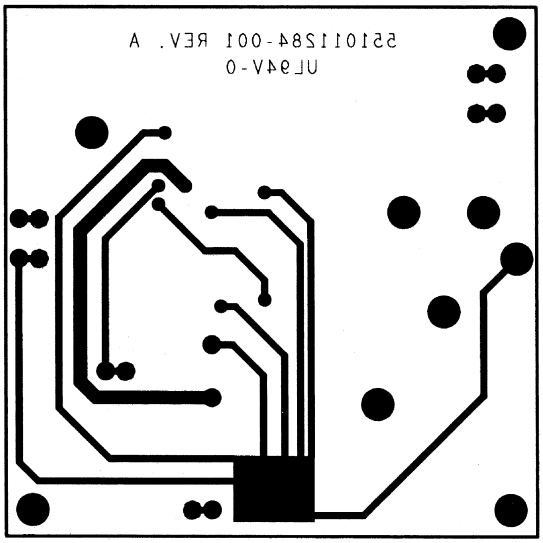

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FIGURE 11. Recommended micro SMD PC board layout: bottom side layout