STLC7546

MODEM (V.34bis) ANALOG FRONT END

- GENERAL-PURPOSE SIGNAL PROCESSING ANALOG FRONT END (AFE)
- TARGETED FOR V.34bis MODEM AND BUSINESS AUDIO APPLICATIONS
- 16-BIT OVERSAMPLING ΣΔ A/D AND D/A CONVERTERS
- 89dB SIGNAL-TO-(NOISE+DISTORTION) RATIO FOR SAMPLING FREQUENCY (FS) UP TO 16kHz @5V
- 94dB DYNAMIC RANGE @5V
- MAX SAMPLING FREQUENCY : 45kHz
- PROGRAMMABLE ADC AND DAC OVERSAMPLING FREQUENCIES. OVERSAMPLING FREQUENCY = N x 32 x FS, N = 2, 3, 4, 5, 6. THE OVERSAMPLING FREQUENCY CAN BE FROM 0.5MHz TO 2.88MHz
- MAX. SAMPLING FREQUENCY : 22.5kHz
- FILTER BANDWIDTHS : 0.425 x THE SAMPLING FREQUENCY
- ON-CHIP REFERENCE VOLTAGE
- DIFFERENTIAL OUTPUT WITH PROGRAMMABLE ATTENUATION : 0dB, 6dB OR INFINITE
- TWO SETS OF DIFFERENTIAL INPUTS WITH PROGRAMMABLE GAINS OF 0dB AND 6dB
- 16-BIT SYNCHRONOUS SERIAL INTERFACE WHOSE OPERATION IS EITHER HARDWARE OR SOFTWARE CONTROLLABLE
- SINGLE POWER SUPPLY RANGE : 5V ±5% OR DOUBLE POWER SUPPLY : +3.3 TO 5V ±5% DIGITAL PART ; 5.0V ±5% ANALOG PART
- LOW POWER CONSUMPTION : 100mW OPERATING POWER AT THE NOMINAL FREQUENCY OF 1.536MHz AND 5.0V SINGLE SUPPLY (70mW @ 3.3V). LESS THAN 50µW IN THE LOW POWER MODE WHEN THE MCLK NOT RUNNING
- 0.8µm CMOS PROCESS
- TQFP44 AND PLCC28 PACKAGES

DESCRIPTION

The STLC7546 is a high-resolution analog-to-digital and digital-to-analog converter targeted for V.34bis modem and consumer audio applications.

This device has a 16-bit oversampling ADC and DAC, filters and control logic for the serial interface. The oversampling frequencies for the ADC and DAC are user programmable.

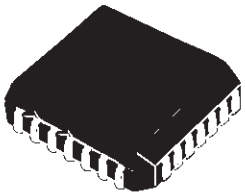
The device operation is controlled by reading the 16-bit information control register.

The major functions of the STLC7546 are :

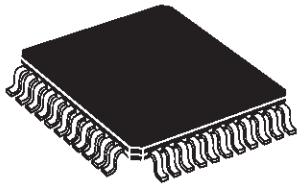
- To convert the audio-signal to 16-bit 2's complement data format through the ADC channel.
- To communicate with an external digital signal processor via serial interface logic.
- To convert 16-bit 2's complement data from a digital signal processor to an audio signal through the DAC channel.

The STLC7546 consists of two signal-processing channels, an ADC channel and a DAC channel, and the associated digital control. The two channels operate synchronously so that the transmitted data to the DAC channel and received data from the ADC channel occur during the same time interval. The data transfer is in 2s complement format.

To save power, e.g. in lap-top modem applications, the low-power reset mode can be used to reduce the power consumption to less than 1mW.



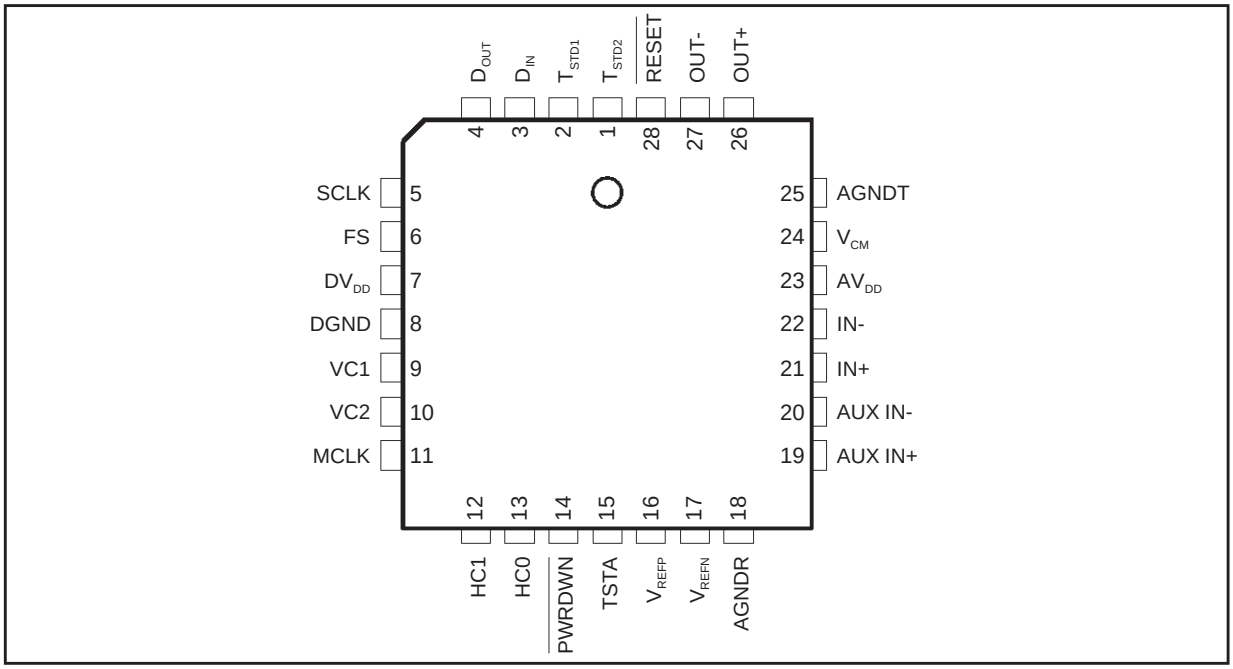
PLCC28
(Plastic Leaded Chip Carrier Package)
ORDER CODE : STLC7546CFN



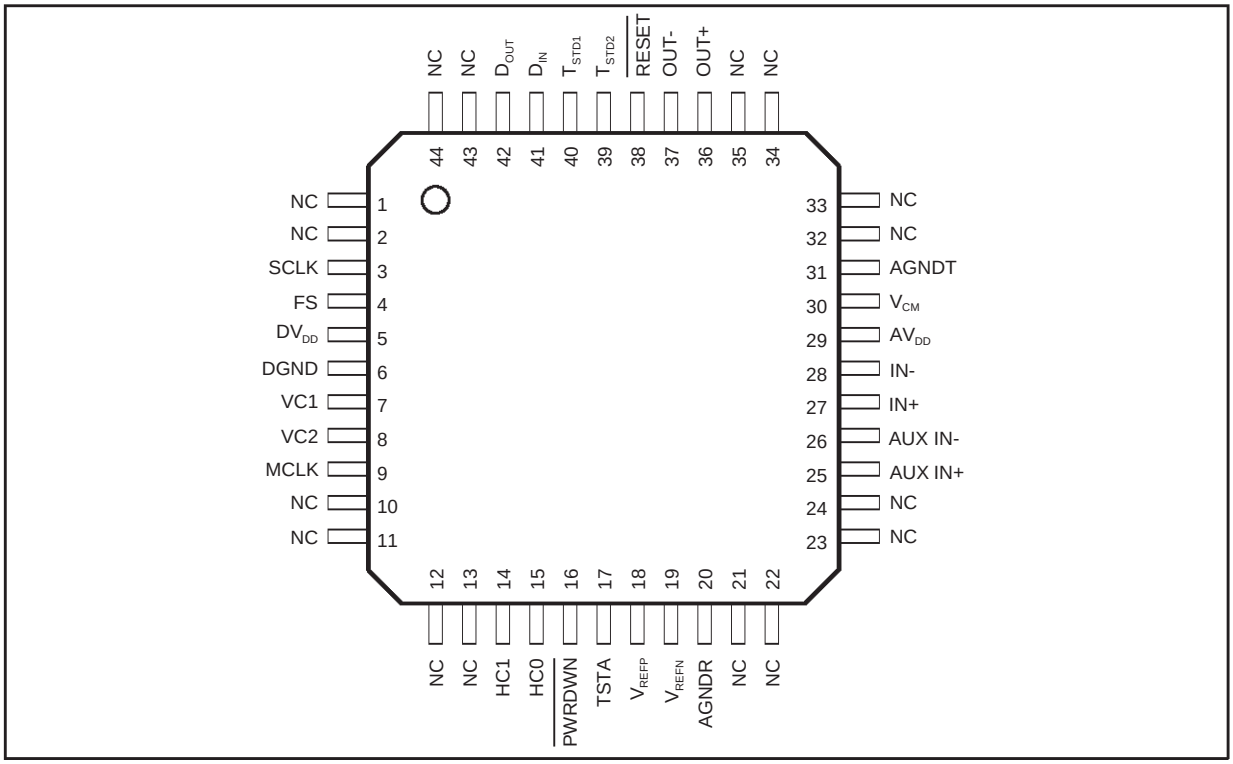
TQFP44 (10 x 10 x 1.4mm)
(Thin Plastic Quad Flat Package)
ORDER CODE : STLC7546TQFP4Y

PIN CONNECTIONS

STLC7546 Top View (PLCC28)



STLC7546 Top View (TQFP44)



PIN LIST

Name	Pin Number		Type	Description
	PLCC28	TQFP44		
SCLK	5	3	O	Shift Clock Output
FS	6	4	O	Frame Synchronization Output
DV_{DD}	7	5	I	Positive Digital Power Supply (+3.15V to 5.25V)
DGND	8	6	I	Digital Ground (0V)
VC1	9	7	O	Voltage Control (should be tied to ground)
VC2	10	8	O	Voltage Control (should be tied to ground)
MCLK	11	9	I	Master Clock Input (equal to the ADC and DAC oversampling frequency)
HC1	12	14	I	Hardware Control Input
HC0	13	15	I	Hardware Control Input
$\overline{PWRDWN}$	14	16	I	Power-down Input
TSTA	15	17	O	Analog Output Reserved for Test
V_{REFP}	16	18	O	16-bit DAC and ADC Positive Reference Voltage
V_{REFN}	17	19	O	16-bit DAC and ADC Negative Reference Voltage
AGNDR	18	20	I	Analog Ground (0V)
AUX IN+	19	25	I	NonInverting Input to Auxiliary Analog Input
AUX IN-	20	26	I	Inverting Input to Auxiliary Analog Input
IN+	21	27	I	NonInverting Input to Analog Input Amplifier
IN-	22	28	I	Inverting Input to Analog Input Amplifier
AV_{DD}	23	29	I	Positive Analog Power Supply (5V ±5%)
V_{CM}	24	30	O	Common Mode Voltage Output (AV_{DD}/2 ±5%)
AGNDT	25	31	I	Analog Ground (0V)
OUT+	26	36	O	Noninverting Smoothing Filter Output
OUT-	27	37	O	Inverting Smoothing Filter Output
$\overline{RESET}$	28	38	I	Reset Function to Initialize the Internal Counters
T_{STD2}	1	39	I	Digital Input Reserved for Test
T_{STD1}	2	40	O	Digital Output Reserved for Test
D_{IN}	3	41	I	Serial Data Input
D_{OUT}	4	42	O	Serial Data Output

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PIN DESCRIPTION

1 - POWER SUPPLY (5 pins)

1.1 - Analog V_{DD} Supply (AV_{DD})

This pin is the positive analog power supply voltage (4.75V to 5.25V) for the DAC and the ADC section. It is not internally connected to digital V_{DD} supply (DV_{DD}).

In any case the voltage on this pin must be higher or equal to the voltage of the Digital power supply (DV_{DD}).

1.2 - Digital V_{DD} Supply (DV_{DD})

This pin is the positive digital power supply for DAC and ADC digital internal circuitry.

1.3 - Analog Ground (AGNDT, AGNDR)

These pins are the ground return of the analog DAC (ADC) section.

1.4 - Digital Ground (DGND)

This pin is the ground for DAC and ADC internal digital circuitry.

Notes : 1. To obtain published performance, the analog V_{DD} and Digital V_{DD} should be decoupled with respect to Analog Ground and Digital Ground, respectively. The decoupling is intended to isolate digital noise from the analog section ; decoupling capacitors should be as close as possible to the respective analog and digital supply pins.

2. All the ground pins must be tied together. In the following section, the ground and supply pins are referred to as GND and V_{DD}, respectively.

2 - HOST INTERFACE (8 pins)

2.1 - Data In (D_{IN})

In Data Mode, the data word is the input of the DAC channel. In Control Mode, the data word is followed by the control register word.

2.2 - Data Out (D_{OUT})

In Data Mode, the data word is the ADC conversion result. In Control Mode, the data word is followed by the register read.

2.3 - Frame Synchronization (FS)

The frame synchronization signal is used to indicate that the device is ready to send and receive data. The data transfer begins on the falling edge of the frame-sync signal. The frame-sync is generated internally and goes low on the rising edge of SCLK.

2.4 - Serial Bit Clock (SCLK)

Clocks the digital data into D_{IN} and out of D_{OUT} during the frame synchronization interval. The Serial bit clock is generated internally and equal to the Master clock signal frequency.

2.5 - Reset Function ($\overline{\text{RESET}}$)

The reset function is to initialize the internal counters and control register. A minimum low pulse of 100ns is required to reset the chip. This reset function initiates the serial data communications. The reset function will initialize all the registers to their default value and will put the device in a pre-programmed state. After a low-going pulse on $\overline{\text{RESET}}$, the device registers will be initialized to provide an over-sampling ratio equal to 160, the serial interface will be in data mode, the DAC attenuation will be set to infinite, the ADC gain will be set to 0dB, the Differential input mode on the ADC converter will be selected, and the multiplexor will be set on the main inputs IN+ and IN-. After a reset condition, the first frame synchronization corresponds to the primary channel.

2.6 - Power Down ($\overline{\text{PWRDWN}}$)

The Power-Down input powers down the entire chip (<50µW). When $\overline{\text{PWRDWN}}$ pin is taken low, the device powers down such that the existing internally programmed state is maintained. When $\overline{\text{PWRDWN}}$ is driven high, full operation resumes after 1ms.

If the $\overline{\text{PWRDWN}}$ input is not used, it should be tied to V_{DD}.

2.7 - Hardware Control (HC0, HC1)

These two pins are used for Hardware/Software Control of the device. The data on HC0 and HC1 will be latched on to the device on the rising edge of the Frame Synchronization Pulse. If these two pins are low, Software Control Mode is selected. When in Software Control Mode, the LSB of the 16-bit word will select the Data Mode (LSB = 0) or the Control Mode (LSB = 1). Other combinations of HC0/HC1 are for Hardware Control. These inputs should be tied low if not used.

3 - CLOCK SIGNALS (3 pins)

3.1 - Master Clock (MCLK)

Master clock input. This signal is the oversampling clock of the D/A and A/D convertor. It also provides all the clocks of the serial interface. This input may be driven by a CMOS signal with a frequency from 0.5MHz up to 2.88MHz (maximum).

3.2 - Voltage Control (VC1, VC2)

The voltage control output from the internal PLL.

If DV_{DD} = 3.3V, VC2 should be tied to ground through a capacitor and VC1 must be tied to ground through a resistor.

If DV_{DD} = 5V, VC1 and VC2 can be tied to ground.

PIN DESCRIPTION (continued)

4 - ANALOG INTERFACE (9 pins)

4.1 - DAC and ADC Positive Reference Voltage Output (V_{REFP})

This pin provides the Positive Reference Voltage used by the 16-bit converters. The reference voltage, V_{REF}, is the voltage difference between the V_{REFP} and V_{REFN} outputs, and its nominal value is 2.5V. V_{REFP} should be externally decoupled with respect to V_{CM}.

4.2 - DAC and ADC Negative Reference Voltage Output (V_{REFN})

This pin provides the Negative Reference Voltage used by the 16-bit converters, and should be externally decoupled with respect to V_{CM}.

4.3 - Common Mode Voltage Output (V_{CM})

This output pin is the common mode voltage (AV_{DD} - AGND)/2. This output must be decoupled with respect to GND.

4.4 - Non-inverting Smoothing Filter Output (OUT+)

This pin is the non-inverting output of the fully differential analog smoothing filter.

4.5 - Inverting Smoothing Filter Output (OUT-)

This pin is the inverting output of the fully differential analog smoothing filter. Outputs OUT+ and OUT- provide analog signals with maximum peak to peak amplitude 2 x V_{REF}, and must be followed by an external two pole smoothing filter. The external filter follows the internal single pole switch capacitor filter. The cutoff frequency of the external filter must be greater than two times the sampling frequency (FS), so that the combined frequency response of both the internal and external filters is flat in the passband . The attenuator of the last output stage can be programmed to 0dB, 6dB or infinite.

4.6 - Non-inverting Analog Input (IN+)

This pin is the differential non-inverting ADC input.

4.7 - Inverting Analog Input (IN-)

This pin is the differential inverting ADC input. These analog inputs (IN+, IN-) are presented to the Sigma-Delta modulator via a multiplexer. The analog input peak to peak differential signal range must be less than 2 x V_{REF}, and must be preceded by an external single pole anti-aliasing filter. The cut-off frequency of the filter must be lower than one half the over-sampling frequency (MCLK). These filters should be set as close as possible to the IN+ and IN- pins. The gain of the first stage is 0dB and can be programmed to 6dB in differential hardware configuration.

4.8 - Non-inverting Auxiliary Analog Input (AUX IN+)

This pin is the differential non-inverting auxiliary ADC input. The characteristics are same as the IN+ input.

4.9 - Inverting Auxiliary Analog Input (AUX IN-)

This pin is the differential inverting auxiliary ADC input. The characteristics are same as the IN- input. The input pair (IN+/IN- or AUX IN+/AUX IN-) are software selectable.

5 - TEST (3 pins)

5.1 - Test Outputs (TSTD1)

Digital output reserved for test. Can be left open.

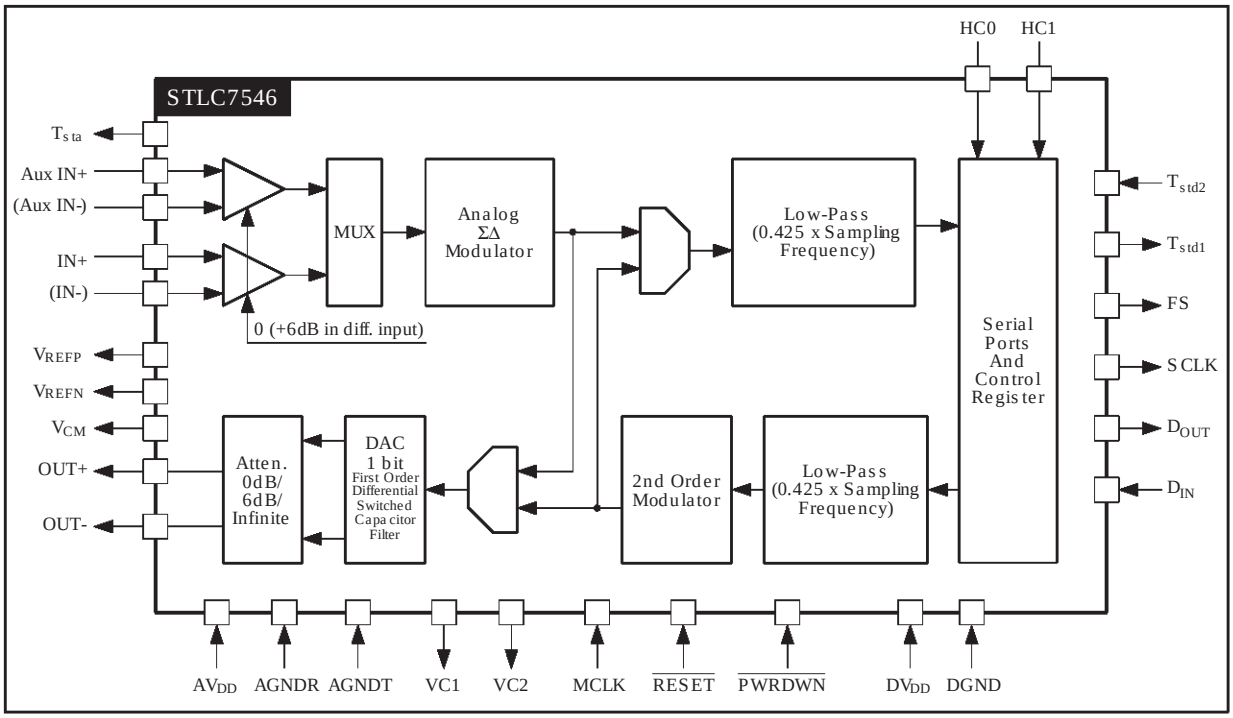
5.2 - Test Input (TSTD2)

Digital input reserved for test. Should be connected to GND.

5.3 - Analog Test Output (TSTA)

Analog output reserved for test. Can be left open.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1 - TRANSMIT D/A SECTION

The functions included in the Tx D/A section are detailed hereafter.

16-bit 2's complement data format is used in the DAC channel.

1.1 - Transmit Low Pass Filters

The transmit low pass filter is basically an interpolating filter. It is a combination of Finite Impulse Response filter (FIR) and an Infinite Impulse Response filter (IIR).

The digital signal from the serial interface gets interpolated by 2, 3, 4, 5 or 6 x Sampling Frequency (FS) through the IIR filter. The signal is further interpolated by 32 x FS x n (with n equal to 2, 3, 4, 5, 6) through the IIR and FIR filter. The low pass filter is followed by the DAC. The DAC is oversampled at 64, 96, 128, 160, 192 x FS. The oversampling ratio is user selectable.

1.2 - D/A Converter

The oversampled D/A converter includes a second order digital noise shaper, a one bit D/A converter and a single pole analog low-pass filter.

The gain of the last output stage can be programmed to 0dB, -6dB or infinite attenuation. The cut-off frequency of the single pole switch-capacitor low-pass filter is :

$$fc_{-3dB} = \frac{MCLK}{2 \cdot \pi \cdot 10}$$

with MCLK = Master Clock frequency.

Continuous-time filtering of the analog differential output is necessary using an off-chip amplifier and a few external passive components.

At least 86dB signal to noise plus distortion ratio can be obtained in the frequency band of 0.425 x 9.6kHz (with an oversampling ratio equal to 160).

2 - RECEIVE A/D SECTION

The different functions included in the ADC channel section are described below. 16-bit 2's complement data format is used in the ADC.

2.1 - A/D Converter

The oversampled A/D converter is based on a second order sigma-delta modulator. To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data. Single-ended mode can also be used. The ADC is oversampled at 64, 96, 128, 160 or 192 x FS. The oversampling ratio is user selectable. At least -86dB SNDR can be expected in the 0.425 x 9.6kHz bandwidth with a -6dBr differential input signal and an oversampling ratio equal to 160.

FUNCTIONAL DESCRIPTION (continued)

2.2 - Receive Low Pass Filter

It is a decimation filter. The decimation is performed by two decimation digital filters : one decimation FIR filter and one decimation IIR filter.

The purpose of the FIR filter is to decimate 32 times the digital signal coming from the ADC modulator.

The IIR is a cascade of 5 biquads. It provides the low-pass filtering needed to remove the noise remaining above half the sampling frequency. The output of the IIR will be processed by the DSP.

3 - Clock Generator

The master clock, MCLK is provided by the user. The ADC and DAC are oversampled at the MCLK frequency. MCLK is equal to the shift clock used in the serial interface. The MCLK frequency should be :
MCLK = Oversampling ratio x Sampling frequency

The clock generator provides, via an internal PLL, the clocks needed for the computation in the digital section. The MCLK clock is used by the PLL for the clock reference.

4 - Host Interface

The Host interface consist of the shift clock, the frame synchronization signal, the ADC-channel data output, and the DAC-channel data input.

The STLC7546 internally generates the shift clock and frame-sync signal for the serial communication. These signals are derived from the input master clock (MCLK). Two modes of serial transfer are available. The first is the software mode for 15-bit transmit data transfer and 16-bit receive data transfer, and the second is the hardware mode for 16-bit data transfer. Both modes are selected by the Hardware Control pins (HC0, HC1).

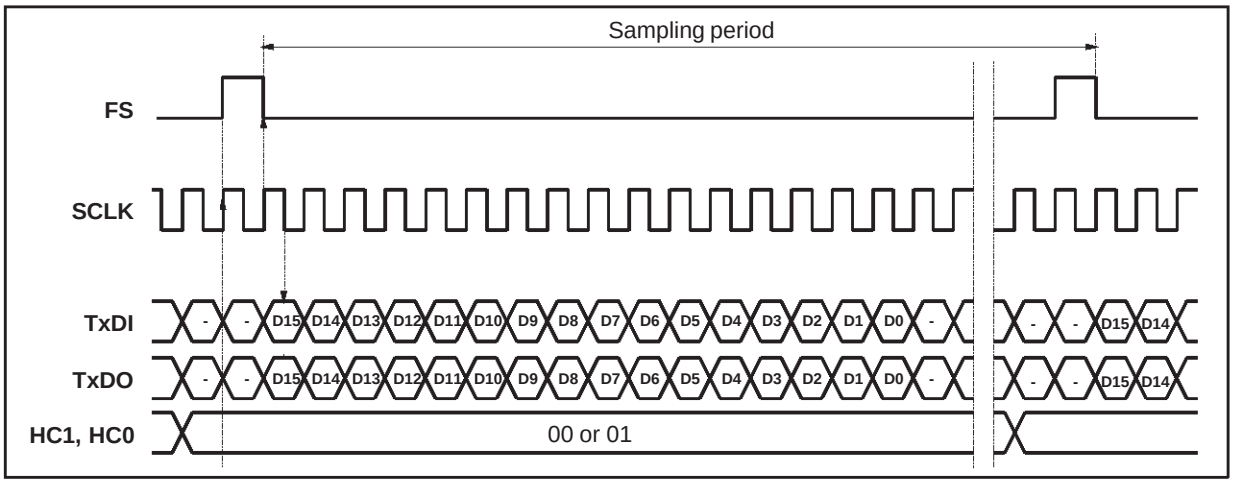
The data to the device, input/output are MSB-first in 2's complement format (see Table 1).

Table 1 : Mode Selection

HC1	HC0	Selected mode
0	0	Software mode Data/control through the LSB of the 16-bit word. LSB = 0 for data and LSB = 1 for control. At the end of the Secondary Frame Synchronization the device automatically returns to data mode.
0	1	Hardware mode for data transfer only. The 16-bit data word is input to the DAC. The 16-bit data word output is the ADC conversion result (operation equivalent to the software mode with LSB = 0).
1	X	Hardware mode for device programming and control register read. Operation equivalent to the Software mode with LSB = 1. 16-bit data is written to or read from the device during Primary Frame Synchronization. During the Secondary Frame Synchronization, the 16-bit control information is input to the device and the 16-bit data word output is the Register read data.

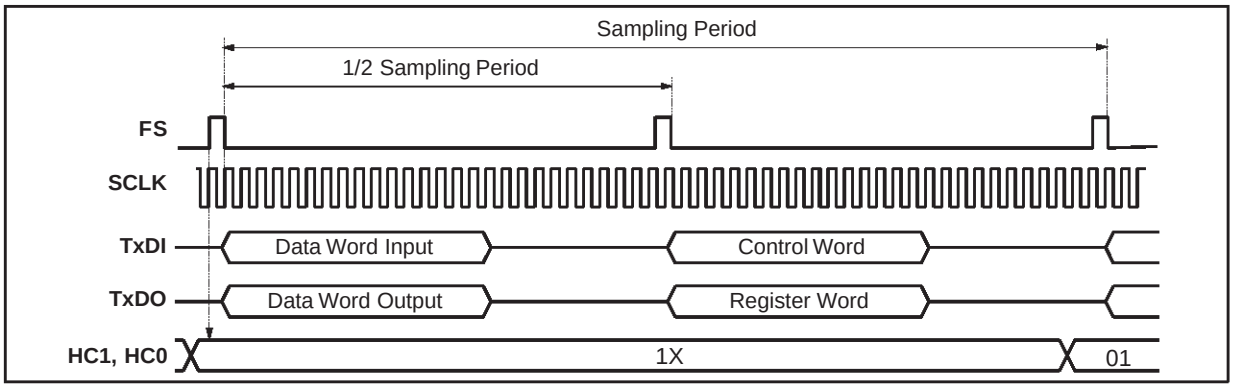
When Control Mode is selected, the device will internally generate an additional Frame Synchronization Pulse (Secondary Frame Synchronization Pulse) at the midpoint of the original Frame Period. The Original Frame Synchronization Pulse will also be referred to as the Primary Frame Synchronization Pulse.

Figure 1 : Data Mode



FUNCTIONAL DESCRIPTION (continued)

Figure 2 : Mixed Mode



5 - Control Register

This section defines the control and device status information. The register programming occurs only during Secondary Frame Synchronization. After a reset condition, the device is always in data mode.

Table 2

Bits	Symbol	Function
0	-	-
1	AUX/MAIN	Auxiliary / Main receive input
2	SING/DIFF	Single-ended /Differential Receive input
3	0VS0	Oversampling bit 0
4	0VS1	Oversampling bit 1
5	0VS2	Oversampling bit 2
6	AT0	Attenuator transmit bit 0
7	AT1	Attenuator transmit bit10
8	-	-
9	RL/RH	Voltage (reference low/reference high)
10	NC1	Not used
11	NC2	Not used
12	TEST0	Test mode bit 0
13	TEST1	Test mode bit 1
14	TEST2	Test mode bit 2
15	TEST3	Test mode bit 3

Table 3 : Auxiliary/Main Input (AUX/MAIN)

D1	Function
0	Main receive input
1	Auxiliary receive input

Table 4 : Single-ended/Differential Inputs (SING/DIFF)

D2	Function
0	Differential input : +0dBr gain
1	Single-ended input : 0dBr gain Differential input : +6dBr gain

Note : 0dBr = 2 x V_{REF} peak-to-peak signal.

Table 5 : Oversampling Ratio

D5	D4	D3	Function
0	0	0	160
0	0	1	192
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	64
1	1	0	96
1	1	1	128

Table 6 : Transmit Attenuator

D7	D6	Function
0	0	Infinite
0	1	Reserved
1	0	-6dB
1	1	0dB

Table 7 : Reserved Mode

D15	D14	D13	D12	D11	D10	D9	Function
0	0	0	0	0	0	0	Reserved

ELECTRICAL SPECIFICATIONS

Unless otherwise noted, Electrical Characteristics are specified over the operating range.
Typical values are given for V_{DD} = +5V, T_{amb} = 25°C and for nominal Master clock frequency MCLK = 1.536MHz and oversampling ratio = 160.

ABSOLUTE MAXIMUM RATINGS (referenced to GND)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3, 7.0	V
V_I,V_{IN}	Digital or Analog Input Voltage	-0.3, V_{DD}+0.3	V
I_I,I_{IN}	Digital or Analog Input Current	±1	mA
I_O	Digital Output Current	±20	mA
I_{OUT}	Analog Output Current	±10	mA
T_{oper}	Operating Temperature	0, 70	°C
T_{stg}	Storage Temperature	-40, 125	°C
P_{DMAX}	Maximum Power Dissipation	200	mW
ESD	Electrostatic Discharge Pins V_{REFP}, V_{REFN} All other Pins	1500 2000	V V

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DC CHARACTERISTICS (V_{DD} = 5.0V ± 5%, GND = 0V, T_A = 0 to 70°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
POWER SUPPLY AND COMMON MODE VOLTAGE					
SINGLE POWER SUPPLY (DV_{DD} = AV_{DD})					
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DDA}	Analog Supply Current		8.5		mA
I_{DDD}	Digital Supply Current		11.5		mA
I_{DD}-LP	Supply Current in Low Power Mode MCLK Stopped MCLK Running		10 800		µA µA
V_{CM}	Output Common Mode Voltage V_{CM} Output Voltage Load Current (see Note 1)	V_{DD}/2-5%	V_{DD}/2	V_{DD}/2+5%	V
DOUBLE POWER SUPPLY (DV_{DD} # AV_{DD})					
DV_{DD}	Digital Supply Voltage	3.15	3.3	3.45	V
AV_{DD}	Analog Supply Voltage	4.75	5	5,25	V
I_{DDA}	Analog Supply Current		8		mA
I_{DDD}	Digital Supply Current		6		mA
V_{CM}	Output Common Mode Voltage (see Note 1)	V_{DD}/2-5%	V_{DD}/2	V_{DD}/2+5%	V
DIGITAL INTERFACE					
(T_A = 25°C, DV_{DD} = +5V)					
V_{IL}	Low Level Input Voltage			0.8	V
V_{IH}	High Level Input Voltage	DV_{DD}-0.5			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	±1	10	µA
V_{OH}	High Level Output Voltage (I_{LOAD} = -1mA)	DV_{DD}-0.5			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = 1mA)			0.4	V
C_{IN}	Input Capacitance		5		pF
(T_A = 25°C, DV_{DD} = +3.3V)					
V_{IL}	Low Level Input Voltage	-0.3		0.5	V
V_{IH}	High Level Input Voltage	DV_{DD}-0.5			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	±1	10	µA
V_{OH}	High Level Output Voltage (I_{LOAD} = -600µA)	DV_{DD}-0.5			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = 800µA)			0.3	V

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Note : 1. Device is very sensitive to noise on V_{CM} Pin. V_{CM} output voltage load current must be DC (<10µA). in order to drive dynamic load, V_{CM} must be buffered. AC variation in V_{CM} current magnitude decrease A/D and D/A performance.

ELECTRICAL SPECIFICATIONS (continued)

DC CHARACTERISTICS

(V_{DD} = 5.0V ± 5%, GND = 0V, T_A = 0 to 70°C unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
ANALOG INTERFACE					
V_{REF} with AV_{DD} = +5V	Differential Reference Voltage Output $V_{REF} = (V_{REFP} - V_{REFN})$	2.4	2.5	2.6	V
Tempco (V_{REF})	V_{REF} Temperature Coefficient		200		ppm/°C
$V_{CMO\ IN}$	Input Common Mode Offset Voltage = [(IN+)+(IN-)]/2 -V_{CM} or [(AUX IN+)+(AUX IN-)]/2 -V_{CM}	-300		300	mV
$V_{DIF\ IN}$	Differential Input Voltage : [(IN+)-(IN-)] ≤ 2 x V_{REF} or [(IN+)-(IN-)] ≤ 2 x V_{REF}		2 x V_{REF}		Vpp
$V_{SIG\ IN}$	Single Ended Input Voltage : IN+ or IN- ≤ V_{REF}		V_{REF}		Vpp
$V_{OFF\ IN}$	Differential Input DC Offset Voltage : IN+ = IN- = V_{CM} (id. AUX IN)	-100		100	mV
$V_{CMO\ OUT}$	Output Common Mode Voltage Offset : (OUT+ + OUT-)/2 - V_{CM} (see Note 2)	-200		200	mV
$V_{DIF\ OUT}$	Differential Output Voltage : OUT+ - OUT- ≤ 2 x V_{REF}		2 x V_{REF}		V
$V_{OFF\ OUT}$	Differential Output DC Offset Voltage : (OUT+ - OUT-)	-100		100	mV
R_{IN}	Input Resistance IN+, IN- (id. AUX IN)	100			kΩ
R_{OUT}	Output Resistance (OUT+, OUT-)		50		Ω
R_L	Load Resistance (OUT+, OUT-)	10			kΩ
C_L	Load Capacitance (OUT+, OUT-)			20	pF
$V_{ADO\ OUT}$	Output A/D Modulator Voltage Offset		10		mV

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Note : 2. Device is very sensitive to noise on V_{CM} Pin. V_{CM} output voltage load current must be DC (<10µA). in order to drive dynamic load, V_{CM} must be buffered. AC variation in V_{CM} current magnitude decrease A/D and D/A performance.

AC ELECTRICAL CHARACTERISTICS

(Reference level V_{IL} = 0.8V, V_{IH} = DV_{DD} - 0.5V, V_{OL} = 0.4V, V_{OH} = DV_{DD} - 0.5V, DV_{DD} = 5V, Output load = 50pF unless otherwise)

Symbol	N°	Parameter	Min.	Typ.	Max.	Unit
SERIAL CHANNEL TIMING (see Figure 3 for Parameter numbers)						
	1	SCLK Period	300			ns
	2	SCLK Width Low	150			ns
	3	SCLK Width High	150			ns
	4	SCLK Rise Time			10	ns
	5	SCLK Fall Time			10	ns
	6	FS Setup	100			ns
	7	FS Hold	100			ns
	8	DIN Setup	50			ns
	9	DIN Hold	0			ns
	10	DOUT Valid			20	ns
	11	HC0,HC1 Set-up	20			ns
MASTER CLOCK INTERFACE (MCLK) (DV_{DD} = +5V or +3.3V)						
MCLK	-	Master Clock Input	0.92	1.54	2.8	MHz
tpw		Master Clock Duty Cycle Pulse Width	360	650		%
tph/tpw		Pulse Width High	45		55	%
tpl/tpw		Pulse Width Low	45		55	%

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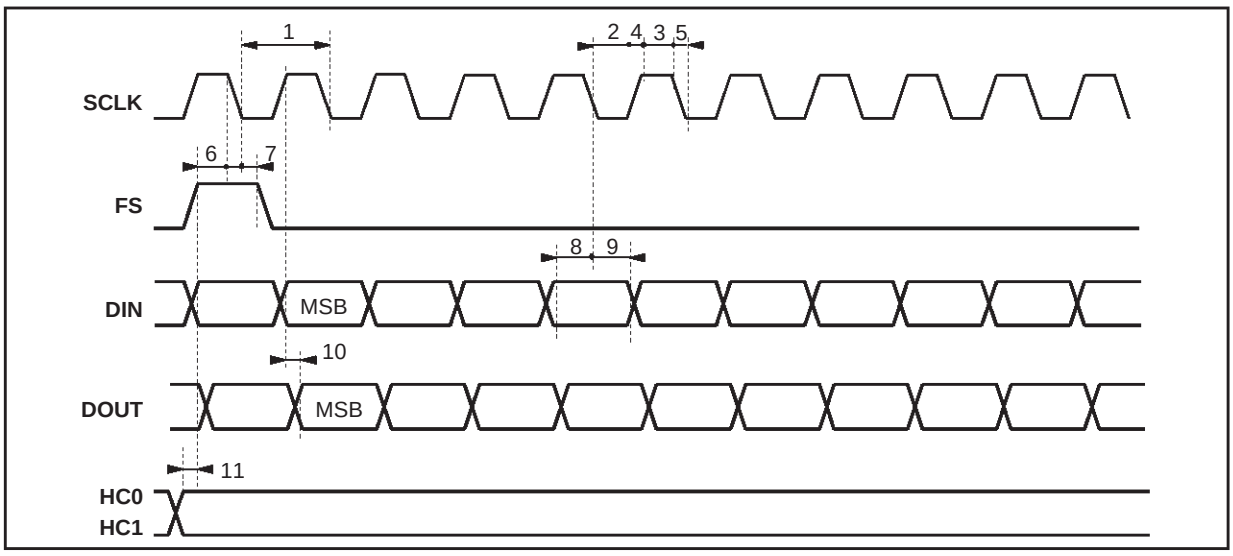
ELECTRICAL SPECIFICATIONS (continued)

Figure 3 : Serial Interface Timing Diagram



TRANSMIT CHARACTERISTICS

Performance of the Tx Channel

Typical values are given for AV_{DD} = +5V, T_{amb} = 25°C and for nominal master clock MCLK = 1.536MHz, differential mode and oversampling ratio = 160. Measurement band = DC to 0.425 x Sampling frequency.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Gabs	Absolute Gain at 1kHz	-0.5	0	0.5	dB
Ripple	Ripple in Band : 0 to 0.425 x FS (the sinX/X distortion must be corrected in the DSP)		±0.2		dB
THD	Total Harmonic Distortion (differential Tx signal : V_{OUT} = 2.5V_{PP}, f = 1kHz)		-89		dB
DR	Dynamic Range (f = 1kHz) (measured over the full 0 to FS/2 with a -20dBr output signal and extrapolated to full scale) (see Note 3)		94		dB
PSRR	Power Supply Rejection Ratio (f = 1kHz, V_{AC} = 200mV_{PP})		50		dB
CRxTx	Crosstalk (transmit channel to receive channel)		90		dB

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Smoothing Filter Transfer Characteristics

The cut-off frequency of the single pole switch-capacitor low-pass filter following the DAC is :

$$fc_{-3dB} = \frac{n \cdot 32 \cdot FS}{2 \cdot \pi \cdot 10} \quad \text{with } n = 2, 3, 4, 5, 6.$$

RECEIVE CHARACTERISTICS

Performance of the Rx Channel

Typical values are given for AV_{DD} = +5V, T_{amb} = 25°C and for nominal master clock MCLK = 1.536MHz, differential mode and oversampling ratio = 160. Measurement band = DC to 0.425 x Sampling Frequency.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Gabs	Absolute Gain at 1kHz	-0.5	0	0.5	dB
Ripple	Ripple in Band : 0 to 0.425 x FS		±0.2		dB
THD	Total Harmonic Distortion (differential Rx signal : V_{IN} = 2.5V_{PP}, f = 1kHz)		-89		dB
DR	Dynamic Range (f = 1kHz) (measured over the full 0 to FS/2 with a -20dBr input and extrapolated to full scale) (see Note 3)		94		dB
PSRR	Power Supply Rejection Ratio (f = 1kHz, V_{AC} = 200mV_{PP})		50		dB
CTxRx	Crosstalk (transmit channel to receive channel)		90		dB

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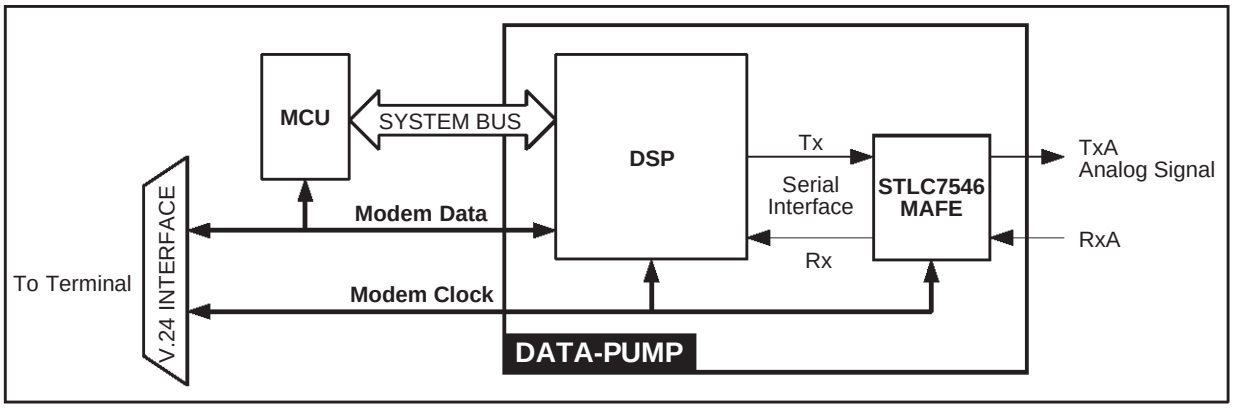
Note : 3. The dynamic range can be measured in bit with : $N_{bit} = \frac{DR - 1.76}{6.02}$ with DR in dB.

TYPICAL APPLICATIONS

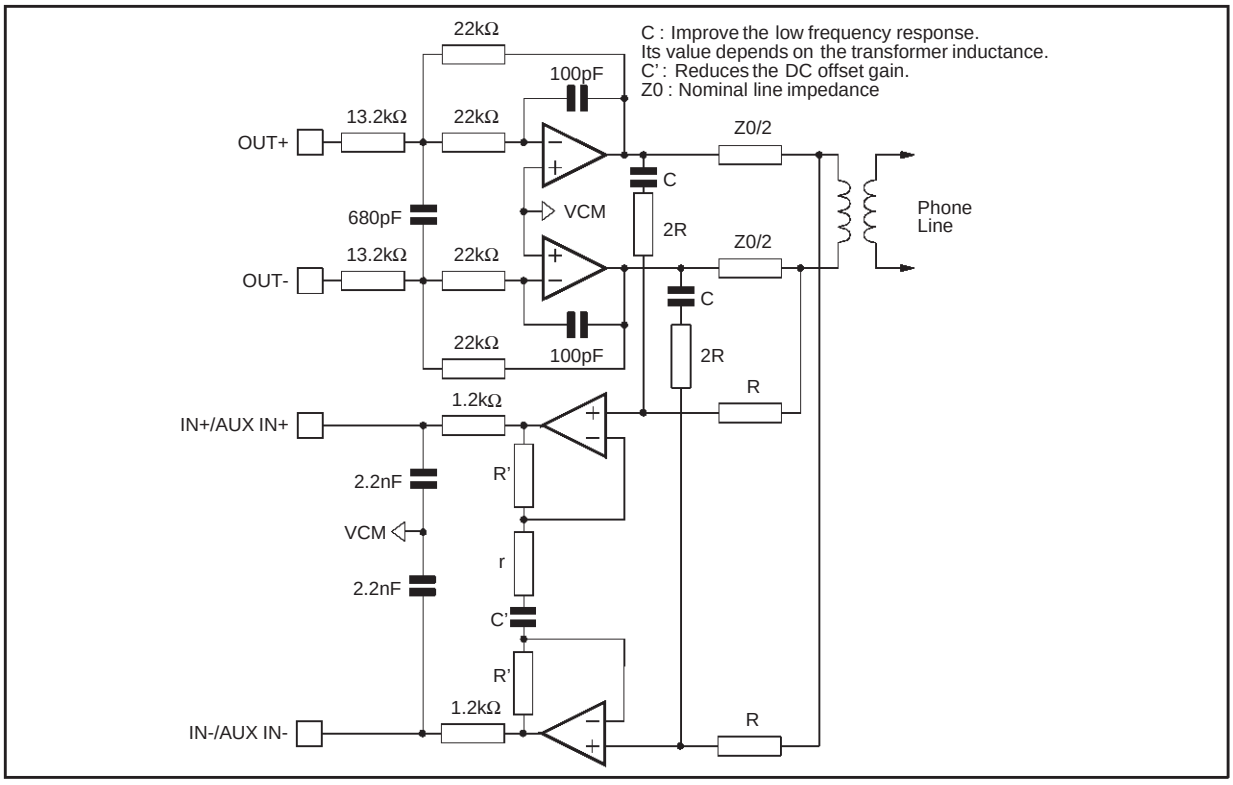
Multi-Standard Modem with Echo Cancelling

Figure 4



Line Interface - Differential Duplexor

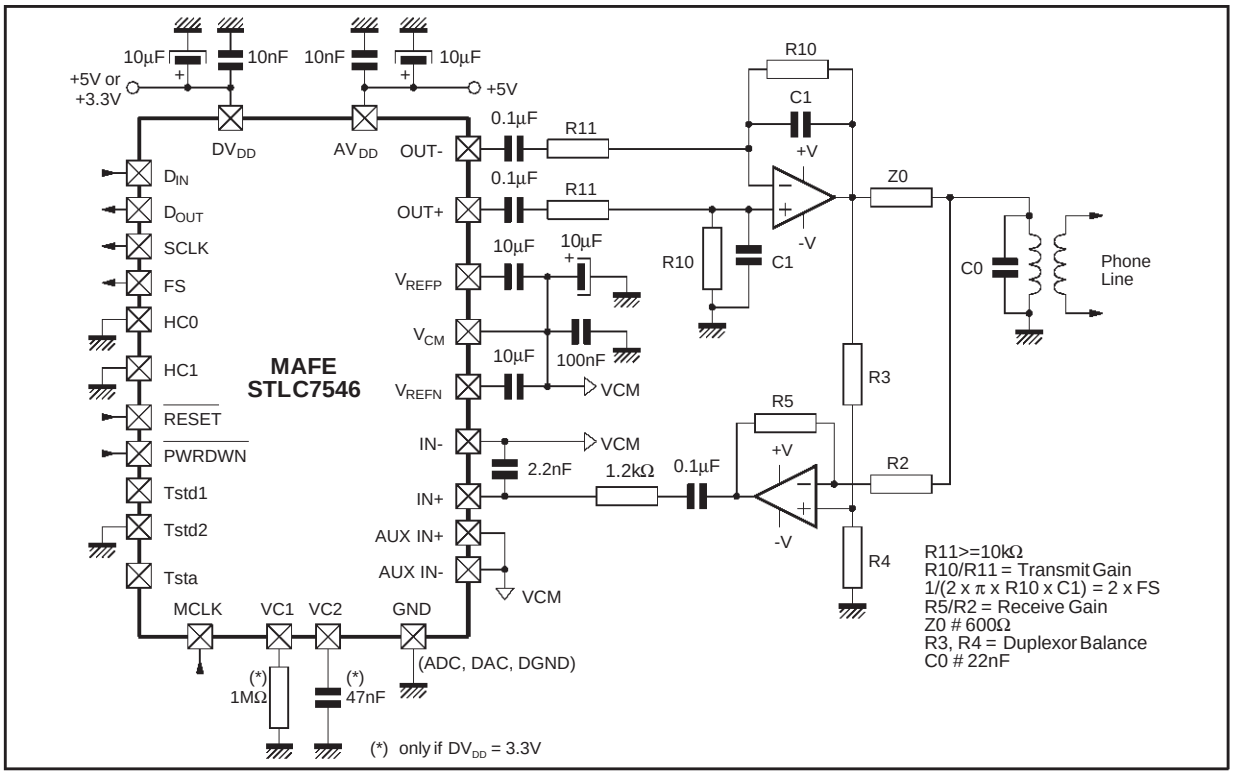
Figure 5



TYPICAL APPLICATIONS (continued)

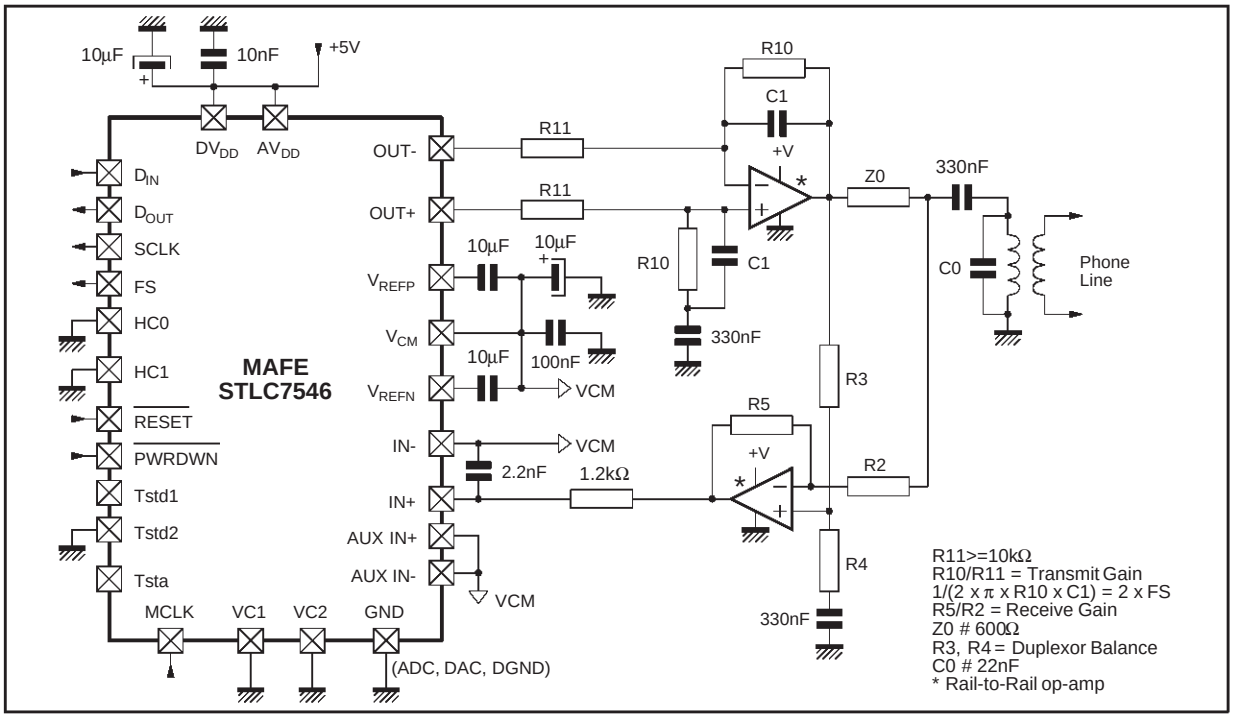
Line Interface - Low-Cost Duplexor

Figure 6



Line Interface - Low-Cost Duplexor Mono Supply

Figure 7

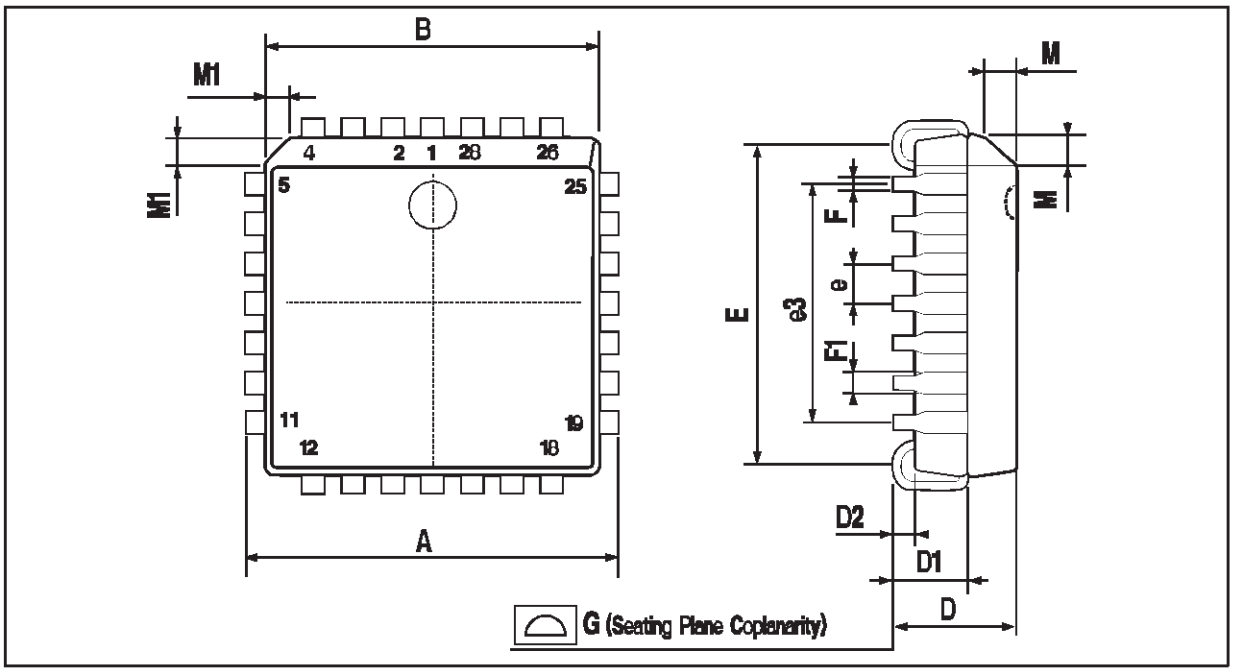


DEFINITION AND TERMINOLOGY

Data Transfer Interval	The time during which data is transfered from D_{OUT} and to D_{IN}. This interval is 16 shift clocks provides by the chip.
Signal Data	This refers to the input signal and all the converted representations through the ADC channel and the DAC channel.
Data Mode	This refers to the data transfer. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Control Mode	This refers to the digital control data transfer into DIN and the register read data from D_{OUT}. The control mode interval occurs when requested by hardware or software.
Frame Sync.	Frame sync refers only to the falling edge of the signal which initiates the data transfer interval. The primary frame sync starts the Data Mode and the secondary frame sync starts the Control Mode.
Frame Sync and Sampling Period	The time between falling edges of successive primary frame sync signals.
ADC Channel	This term refers to all signal processing circuits between the analog input and the digital conversion result at D_{OUT}.
DAC Channel	This term refers to all signal processing circuits between the digital data word applied to D_{IN} and the differential output analog signal available at OUT+ and OUT- pins.
OverSampling Ratio	This term refer to the ratio between the master clock MCLK corresponding to the oversampling frequency and the sampling frequency FS.
Resolution	The number of bits in the input words to the DAC, and the output words in the ADC.
Dynamic Range	The S/(N+D) with a 1kHz, -20dBr input signal and extrapolated to full scale. Use of a small input signal reduces the harmonic distortion components of the noise to insignificance. Units in dB or in N_{bit} as explained before.
Signal-to-(Noise+Distortion)	S/(THD+N) is the ratio of the rms of the input signal to the rms of all other spectral components within the measurement bandwidth (0.425 x Sampling Frequency). Units in dB.
Crosstalk	The amount of 1kHz signal present on the output of the grounded input channel with 1kHz 0dB signal present on the other channel. Units in dB.
Powersupply Rejection Ratio	PSSR. The amount of 1kHz signal present on the output of the grounded input channel with 1kHz 200mV_{PP} signal present on the power supply.

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC LEADED CHIP CARRIER (PLCC)

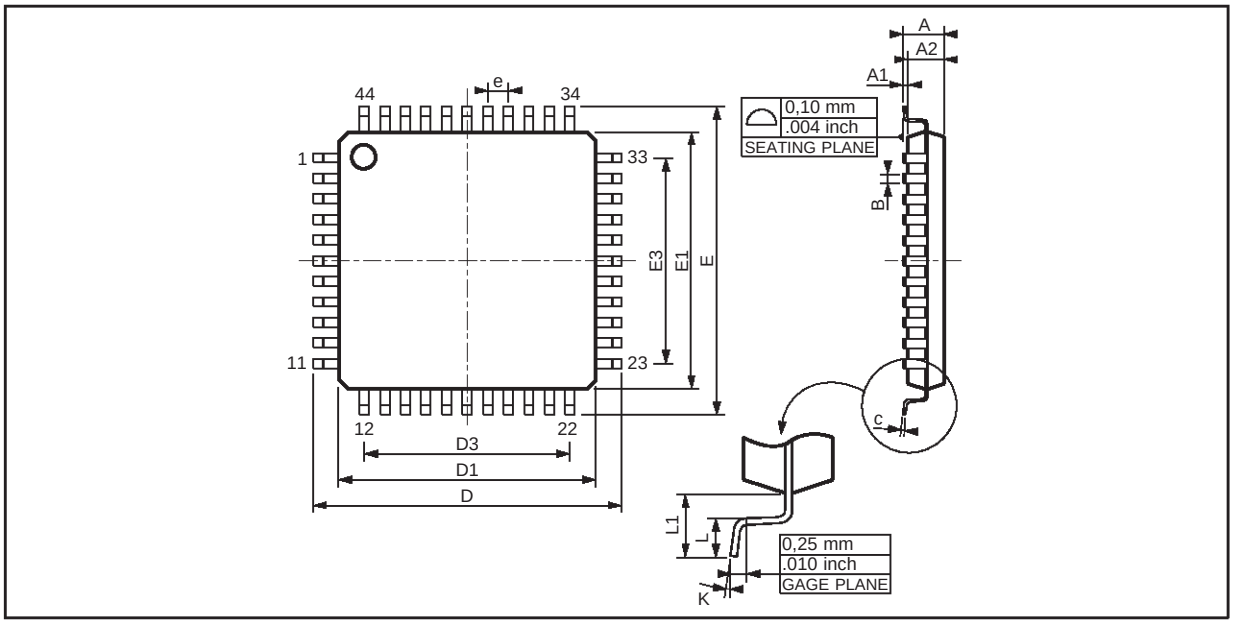


PMPLCC28.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

PLCC28.TBL

PACKAGE MECHANICAL DATA (continued)
44 PINS - PLASTIC QUAD FLAT PACK (THIN) (TQFP)



PMTQFP44.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.40	0.012	0.015	0.016
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					

4Y.TBL