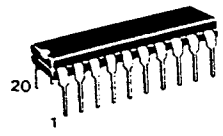
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC14489

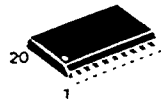
Advance Information

Multi-Character LED Display/Lamp Driver

CMOS



P SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC14489P	Plastic DIP
MC14489DW	SOIC Package

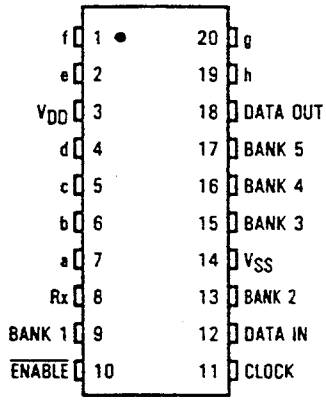
The MC14489 is a flexible light-emitting-diode driver which directly interfaces to individual lamps, 7-segment displays, or various combinations of both. LEDs wired with common cathodes are driven in a muliplexed-by-5 fashion. Communication with an MCU/MPU is established through a synchronous serial port. The MC14489 features data retention plus decode and scan circuitry, thus relieving processor overhead. A single, current-setting resistor is the only ancillary component required.

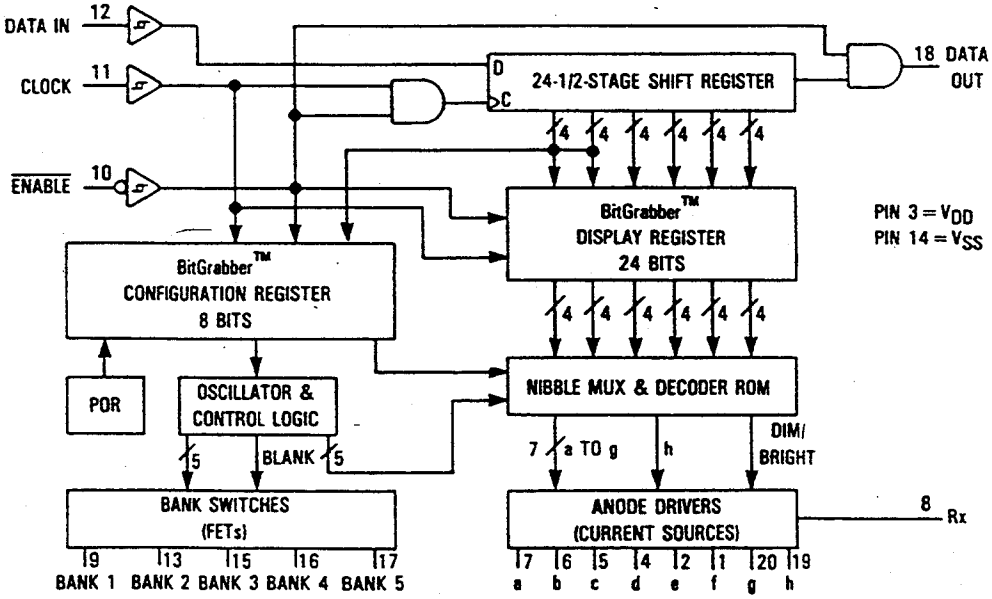
A single device can drive any one of the following: a 5-digit display plus decimals, a 4 1/2-digit display plus decimals and sign, or 25 lamps. A configuration register allows the drive capability to be partitioned off to suit many additional applications. The on-chip decoder outputs 7-segment-format numerals 0 to 9, hexadecimal characters A to F, plus 15 additional letters and symbols.

The MC14489 is compatible with the Motorola/RCA SPI and National MICROWIRE serial data ports. The chip's new BitGrabber registers augment the serial interface by allowing random access without steering or address bits. A 24-bit transfer updates the display register. Changing the configuration register requires an 8-bit transfer.

- Operating Voltage Range of Drive Circuitry: 4.5 to 6 V
- Operating Junction Temperature Range: −40° to 130°C
- Current Sources Controlled by Single Resistor Provide Anode Drive
- Low-Resistance FET Switches Provide Direct Common Cathode Interface
- Low-Power Mode and Brightness Controlled Via Serial Port
- Special Circuitry Minimizes EMI
- POR Blanks the Display on Power-Up
- May Be Used with the New Double-Heterojunction LEDs for Optimum Efficiency
- Chip Complexity: 4300 Elements (FETs, Resistors, Capacitors, etc.)

PIN ASSIGNMENT





BitGrabber is a trademark of Motorola Inc. Patent pending on BitGrabber registers. MICROWIRE is a trademark of National Semiconductor Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

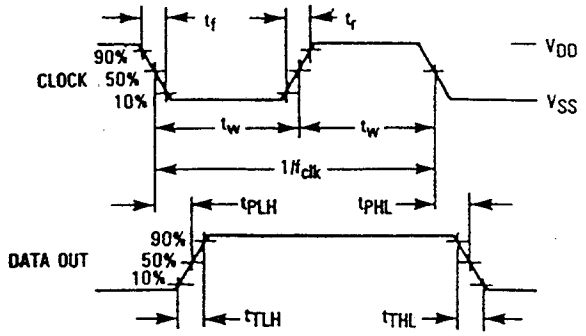


Figure 1

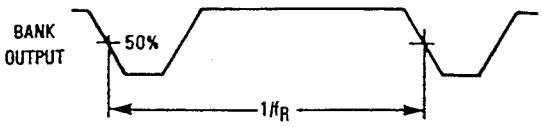


Figure 2

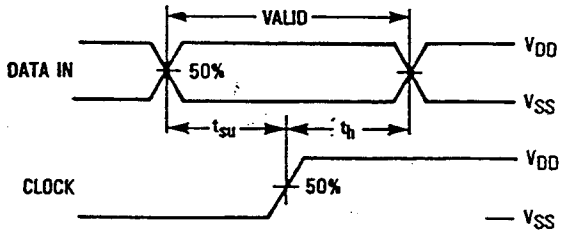


Figure 3

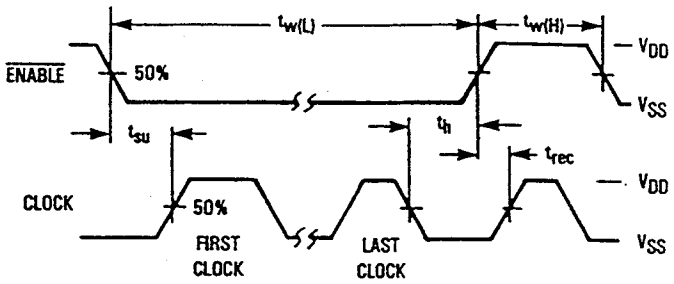
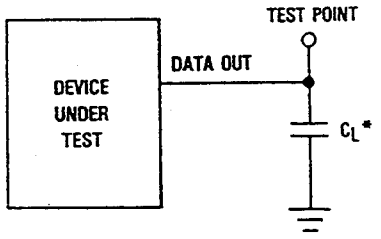
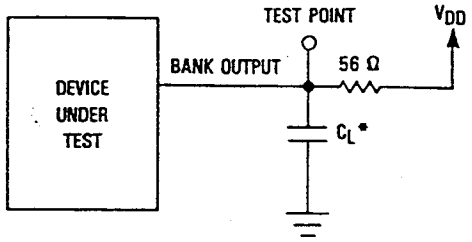


Figure 4



*Includes all probe and jig capacitance.

Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE

Data In (Pin 12)

Serial Data Input. The bit stream begins with the MSB and is shifted in on the low-to-high transition of Clock. When the device is not cascaded, the bit pattern is either 1 byte (8 bits) long to change the configuration register or 3 bytes (24 bits) long to update the display register. For two chips cascaded, the pattern is either 4 or 6 bytes, respectively. The display does not flicker during shifting.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the two registers. The format is shown in Figures 7 and 8. Information on the segment decoder is given in Table 1.

Data In typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. These features combine to maximize noise immunity for use in harsh environments and bus applications. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC14504B, MC74HCT04A) or pullup resistor of 1 kΩ to 10 kΩ must be used. Parameters to be considered when sizing the resistor are the worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Clock (Pin 11)

Serial Data Clock Input. Low-to-high transitions on Clock shift bits available at Data In, while high-to-low transitions shift bits from Data Out. The chip's 24-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or

intermittent mode. The Clock input does not need to be synchronous with the on-chip clock oscillator which drives the multiplexing circuit.

Eight clock cycles are required to access the configuration register, while 24 are needed for the display register when the MC14489 is not cascaded. See Figures 7 and 10.

As shown in Figure 11, two devices may be cascaded. In this case, 32 clock cycles access the configuration register and 48 access the display register, as depicted in Figure 8.

Cascading of 3 and 4 devices is shown in Figures 12 and 13, respectively.

Clock typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow Clock rise and fall times are tolerated. See the last paragraph of **Data In** for more information.

$\overline{\text{Enable}}$ (Pin 10)

Active-Low Enable Input. This pin allows the MC14489 to be used on a serial bus, sharing Data In and Clock with other peripherals. When $\overline{\text{Enable}}$ is in an inactive high state, Data Out is forced to a known (low) state and shifting is inhibited. To transfer data to the device, $\overline{\text{Enable}}$ is taken low, a serial transfer is made via Data In and Clock, and $\overline{\text{Enable}}$ is taken high. The low-to-high transition on $\overline{\text{Enable}}$ transfers data to either the configuration or display register, depending on the data stream length.

CAUTION

Transitions on $\overline{\text{Enable}}$ must not be attempted while Clock is high.

This input is also Schmitt-triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data in the registers. See the last paragraph of **Data In** for more information.

Data Out (Pin 18)

Serial Data Output. Data is transferred out of the shift register through Data Out on the high-to-low transition of Clock. This output is a no connect, unless used in one of the manners discussed below.

When cascading MC14489s, Data Out feeds Data In of the next device per Figures 11, 12, and 13.

Data Out could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, pc board traces, solder joints, etc.

The pin could be monitored at an in-line Q.A. test during board manufacturing.

Finally, Data Out facilitates troubleshooting a system.

DISPLAY INTERFACE

Rx (Pin 8)

External Current-Setting Resistor. A resistor tied between this pin and ground (V_{SS}) determines the peak segment drive current delivered at pins a through h. Pin 8's resistor ties into a current mirror with an approximate current gain of 10 when bit D23 = high (brighten). With D23 = low, the peak current is reduced about 50%. Values for Rx range from 700 Ω to infinity. When Rx = ∞ (open circuit), the display is extinguished. For proper current control, resistors having ± 1% tolerance should be used. See Figure 9.

CAUTION

Small Rx values may cause the chip to overheat if precautions are not observed. See **THERMAL CONSIDERATIONS**.

a through h (Pins 1, 2, 4-7, 19, 20)

Anode-Driver Current Sources. These outputs are closely-matched current sources which directly tie to the anodes of external discrete LEDs (lamps) or display segment LEDs.

When used with lamps, outputs a, b, c, and d are used to independently control up to 20 lamps. Output h is used to control up to 5 lamps dependently. (See Figure 15.) For lamps, the *No Decode* mode is selected via the configuration register, forcing e, f, and g inactive (low).

When used with segmented displays, outputs a through g drive segments a through g, respectively. Output h is used to drive the decimals. If unused, h must be left open. Refer to Figure 10.

Bank 1 through Bank 5 (Pins 9, 13, 15, 16, 17)

Diode-Bank FET Switches. These outputs are low-resistance switches to ground (V_{SS}) capable of handling currents of up to 320 mA. These pins directly tie to the common cathodes of segmented displays or the cathodes of lamps (wired with cathodes common).

The display is refreshed at a nominal 1 kHz rate to achieve optimum brightness from the LEDs. A 20% duty cycle is utilized.

Special design techniques are used on-chip to accommodate the high currents with low EMI (electromagnetic interference) and minimal spiking on the power lines.

POWER SUPPLY

V_{SS} (Pin 14)

Most-negative supply potential. This pin is usually ground.

Resistor Rx is externally tied to ground (V_{SS}). Therefore, the chip's V_{SS} pin does not contain the Rx current component.

V_{DD} (Pin 3)

Most-positive supply potential.

To guarantee data integrity in the registers and to ensure the serial interface is functional, this voltage may range from 3 to 6 volts with respect to V_{SS}. For example, within this voltage range, the chip could be placed in and out of the low-power mode.

To adequately drive the LEDs, this voltage must be 4.5 to 6 volts with respect to V_{SS}.

The V_{DD} pin contains the Rx current component plus the chip's current drain. In the low-power mode, the current mirror and clock oscillator are turned off, thus significantly reducing the V_{DD} current, I_{DD}.

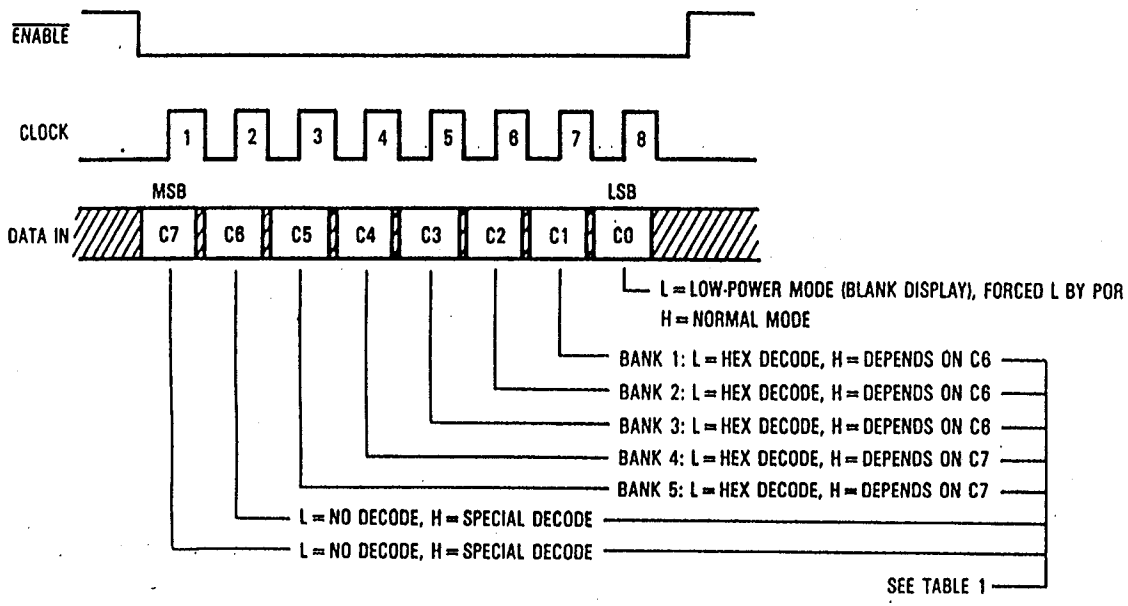


Figure 7a. Configuration Register Format (1 Byte)

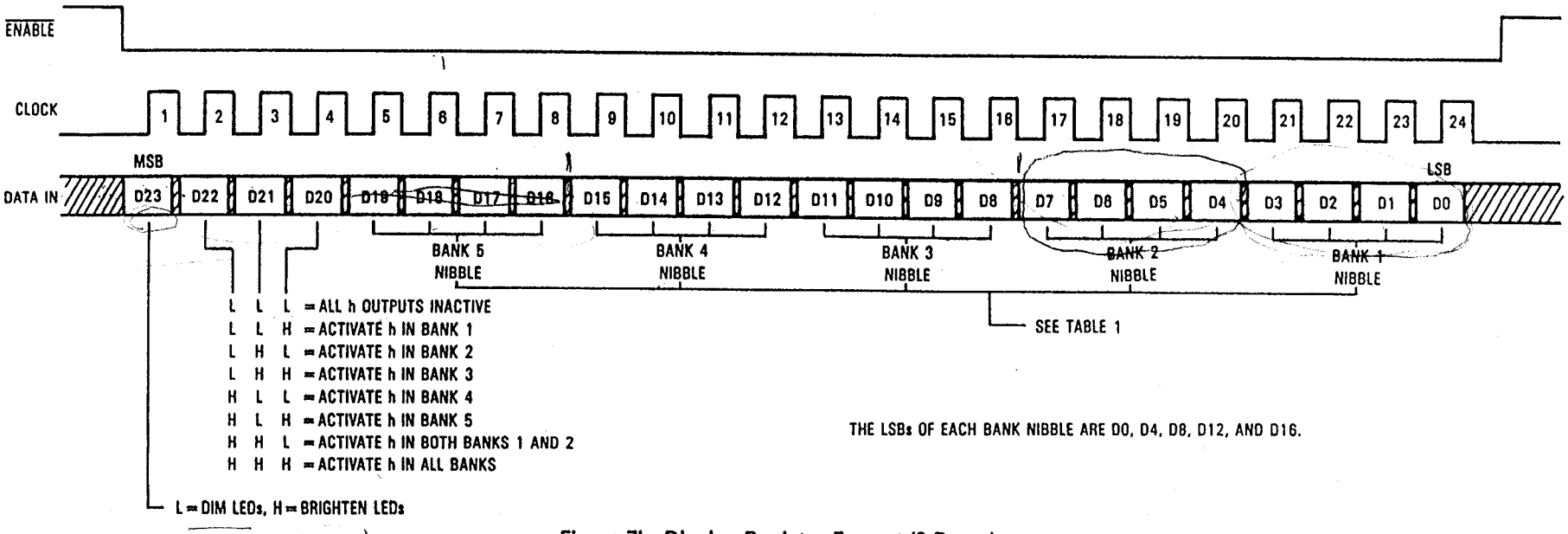


Figure 7b. Display Register Format (3 Bytes)

NOTE: L = Low Voltage Level (Logic 0), H = High Voltage Level (Logic 1)

Figure 7. Timing Diagrams for Non-Cascaded Devices

Table 1. Triple-Mode Segment Decoder Function Table

Bank Nibble Value		7-Segment Display Characters		Lamp Conditions			
				No Decode (1) (Invoked via Bits C1 to C7)			
Hexadecimal	Binary MSB LSB	Hex Decode (Invoked via Bits C1 to C5)	Special Decode (Invoked via Bits C1 to C7)	d	c	b	a
$0	L L L L	0					
$1	L L L H	1	c				on
$2	L L H L	2	H			on	
$3	L L H H	3	h			on	on
$4	L H L L	4	J		on		
$5	L H L H	5 (2)	L		on		on
$6	L H H L	6	n		on	on	
$7	L H H H	7	o		on	on	on
$8	H L L L	8 (3)	P	on			
$9	H L L H	9 (4)	r	on			on
$A	H L H L	A	U	on		on	
$B	H L H H	b	u	on		on	on
$C	H H L L	C	y	on	on		
$D	H H L H	d	-	on	on		on
$E	H H H L	E	=	on	on	on	
$F	H H H H	F	o	on	on	on	on

(1) In the *No Decode* mode, outputs e, f, and g are unused and are all forced inactive (low). Output h's decoding is unaffected, i.e., unchanged from the other modes. The *No Decode* mode is used for three purposes:

1. Individually controlling lamps.
2. Controlling a half digit with sign.
3. Controlling annunciators—examples: AM, PM, UHF, kV, mm Hg.

(2) Can be used as "cap S".

(3) Can be used as "cap B".

(4) Can be used as "small g".

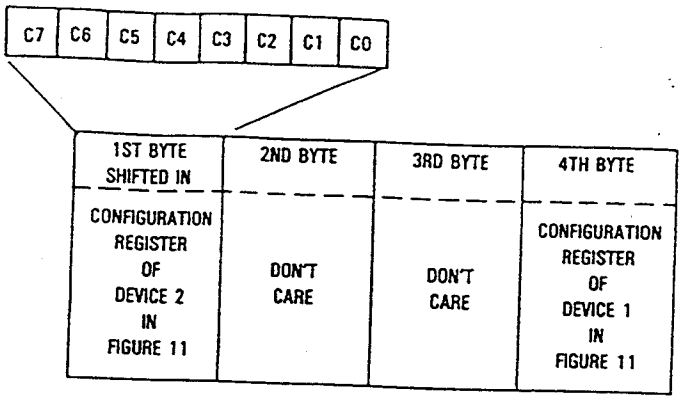


Figure 8a. Configuration Registers

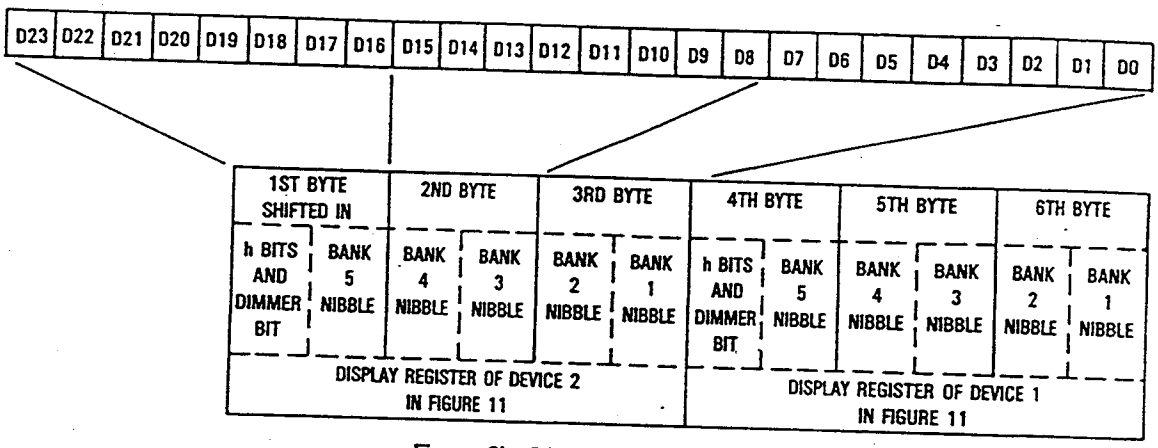


Figure 8b. Display Registers

NOTE: $\overline{\text{ENABLE}}$ is kept active-low during the entire 4-byte configuration transfer or 6-byte display transfer. When $\overline{\text{ENABLE}}$ is brought high, either a 4- or 6-byte transfer occurs in the cascaded devices.

Figure 8. Bit Stream Formats for Two Devices Cascaded

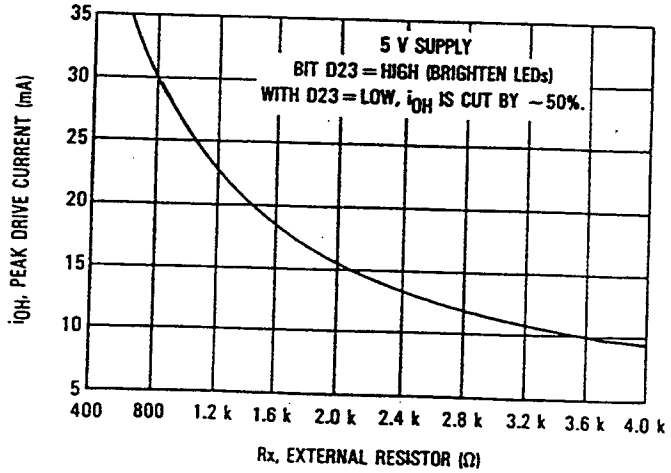


Figure 9. a through h Current versus Rx

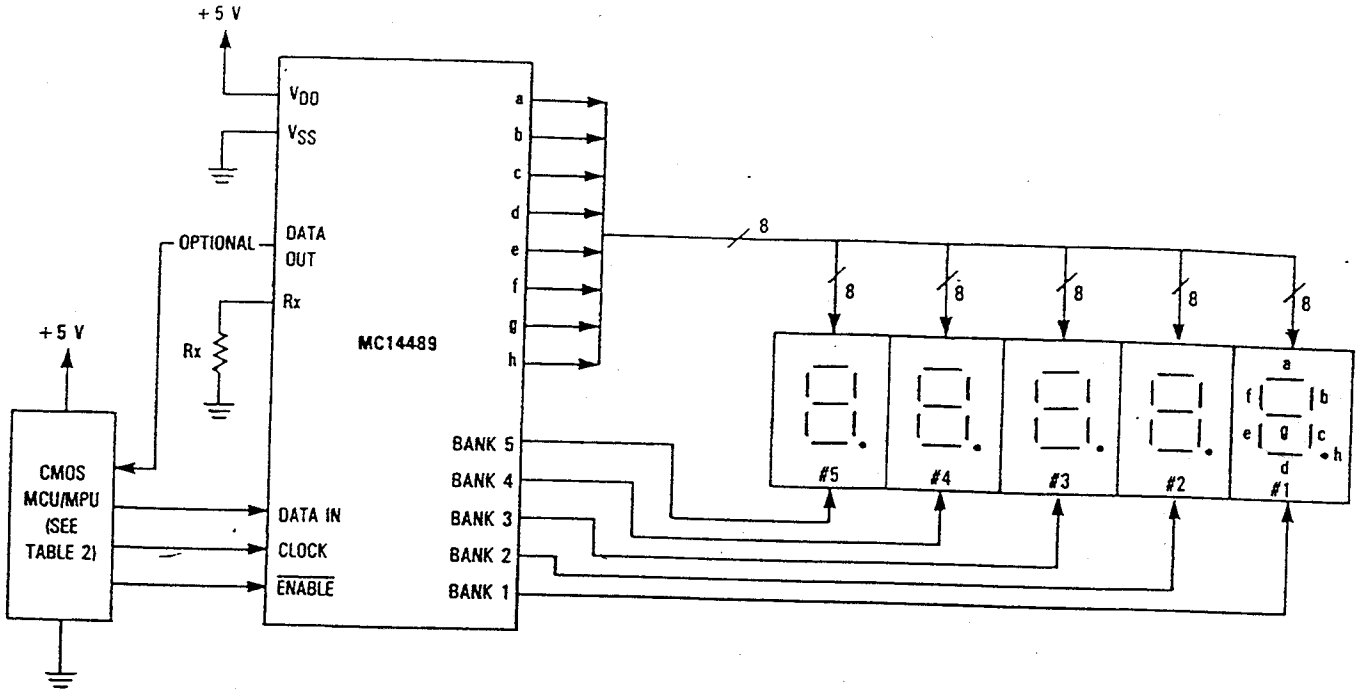


Figure 10. Non-Cascaded Application Example: 5 Character Common Cathode LED Display with Two Intensities as Controlled via Serial Port

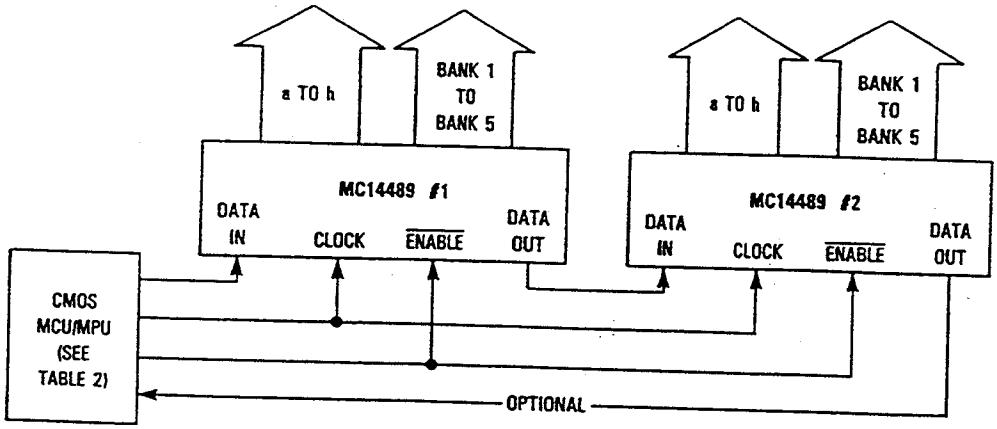


Figure 11. Cascading Two Devices

CLOCK & FREQUENCY LED DISPLAYS

DIGIT SIZE	BRIGHT RED		GREEN		DESCRIPTION			
	PART NUMBER	TYP. Iv/SEG. @10mA	PART NUMBER	TYP. Iv/SEG. @10mA	DRIVE MODE		DISPLAY MODE (HOUR)	DISPLAY FONT
→	LTC-5881A1P		LTC-5881A1G		MULTIPLEX	C.C.	FF	8888
	LTC-5881P		LTC-5881G		MULTIPLEX	C.C.	FF	8888

Notes: C.C.:COMMON CATHODE C.A.:COMMON ANODE FF:FULL FEATURE NC: NO CONNECTION

PIN CONNECTION																	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
+A	NC	+D	−1	NC	NC	−2	+C	NC	−3	+B	+F	+E	−4	+DP	+G	−	−
+A	NC	+D	−1	NC	NC	−2	+C	NC	−3	+B	+F	+E	−4	+DP	+G	−	−

DP:DECIMAL POINT UC:UPPER COLON LC:LOWER COLON NC:NO CONNECTION

5-16 LTC-5881A1x/5882A1x Series