Rail-to-Rail Output Audio Amplifiers

SSM2275/SSM2475*

FEATURES
Single or Dual-Supply Operation
Excellent Sonic Characteristics
Low Noise: 7 nV/√Hz
Low THD: 0.0006%
Rail-to-Rail Output
High Output Current: ±50 mA
Low Supply Current: 1.7 mA/Amplifier
Wide Bandwidth: 8 MHz
High Slew Rate: 12 V/μs
No Phase Reversal
Unity Gain Stable
Stable Parameters Over Temperature

APPLICATIONS
Multimedia Audio
Professional Audio Systems
High Performance Consumer Audio
Microphone Preamplifier
MIDI Instruments

GENERAL DESCRIPTION

The SSM2275 and SSM2475 use the Butler Amplifier front end, which combines both bipolar and FET transistors to offer the accuracy and low noise performance of bipolar transistors and the slew rates and sound quality of FETs. This product family includes dual and quad rail-to-rail output audio amplifiers that achieve lower production costs than the industry standard OP275 (the first Butler Amplifier offered by Analog Devices). This lower cost amplifier also offers operation from a single 5 V supply, in addition to conventional ±15 V supplies. The ac performance meets the needs of the most demanding audio applications, with 8 MHz bandwidth, 12 V/μs slew rate and extremely low distortion.

The SSM2275 and SSM2475 are ideal for application in high performance audio amplifiers, recording equipment, synthesizers, MIDI instruments and computer sound cards. Where cascaded stages demand low noise and predictable performance, SSM2275 and SSM2475 are a cost effective solution. Both are stable even when driving capacitive loads.

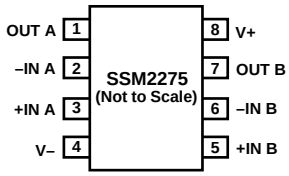
The ability to swing rail-to-rail at the outputs (see Applications section) and operate from low supply voltages enables designers to attain high quality audio performance, even in single supply systems. The SSM2275 and SSM2475 are specified over the extended industrial (–40°C to +85°C) temperature range. The SSM2275 is available in 8-lead plastic DIPs, SOICs, and microSOIC surface-mount packages. The SSM2475 is available in narrow body SOICs and thin shrink small outline (TSSOP) surface-mount packages.

*Protected by U.S. Patent No. 5,101,126.

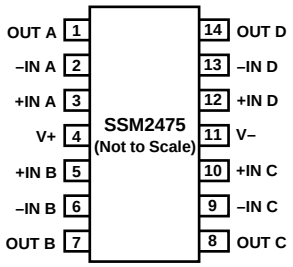
REV. A

PIN CONFIGURATIONS

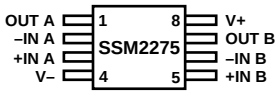
8-Lead Narrow Body SOIC (SO-8)



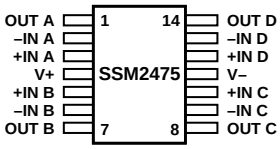
14-Lead Narrow Body SOIC (R-14)



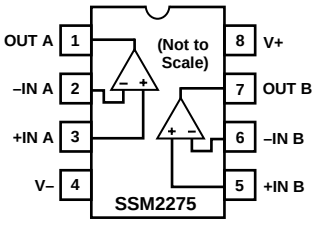
8-Lead microSOIC (RM-8)



14-Lead TSSOP (RU-14)



8-Lead Plastic DIP (N-8)



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Fax: 781/326-8703

SSM2275/SSM2475–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = +25°C, V_{CM} = 0 V unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	4	mV
		–40°C ≤ T_A ≤ +85°C		1	6	mV
Input Bias Current	I_B			250	400	nA
		–40°C ≤ T_A ≤ +85°C		300	500	nA
Input Offset Current	I_{OS}			5	75	nA
		–40°C ≤ T_A ≤ +85°C		15	125	nA
Input Voltage Range	V_{IN}	V_S = ±15 V	–14		+14	V
Common-Mode Rejection Ratio	CMRR	–12.5 V ≤ V_{CM} ≤ +12.5 V	80	100		dB
		–40°C ≤ T_A ≤ +85°C,				
		–12.5 V ≤ V_{CM} ≤ +12.5 V	80	100		V/mV
A_{VO}		R_L = 2 kΩ, –12 V ≤ V_O ≤ +12 V	100	240		V/mV
		–40°C ≤ T_A ≤ +85°C	80	120		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage, High	V_{OH}	I_L ≤ 20 mA	14	14.5		V
		–40°C ≤ T_A ≤ +85°C	14.5	14.7		V
Output Voltage, Low	V_{OL}	I_L = 20 mA		–14	–13.5	V
		I_L = 10 mA		–14.6	–14.4	V
		I_L = 10 mA, –40°C ≤ T_A ≤ +85°C		–14.3	–13.9	V
Output Short Circuit Current Limit	I_{SC}		±25	±50	±75	mA
		–40°C ≤ T_A ≤ +85°C	±17	±40	±80	mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±2.5 V ≤ V_S ≤ ±18 V	85	110		dB
		–40°C ≤ T_A ≤ +85°C	80	105		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		1.7	2.9	mA
		–40°C ≤ T_A ≤ +85°C		1.75	3.0	mA
DYNAMIC PERFORMANCE						
Total Harmonic Distortion	THD	R_L = 10 kΩ, f = 1 kHz, V_O = 1 V rms		0.0006		%
Slew Rate	SR	R_L = 2 kΩ‖50 pF	9	12		V/µs
Gain Bandwidth Product	GBW			8		MHz
Channel Separation	CS	R_L = 2 kΩ, f =1 kHz		128		dB
NOISE PERFORMANCE						
Voltage Noise Spectral Density	e_n	f > 1 kHz		8		nV/√Hz
Current Noise Spectral Density	i_n	f > 1 kHz		< 1		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = +5 V, T_A = +25°C, V_{CM} = 2.5 V unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	4	mV
		$-40°C \le T_A \le +85°C$		1	6	mV
Input Bias Current	I_B			250	400	nA
		$-40°C \le T_A \le +85°C$		300	500	nA
Input Offset Current	I_{OS}			5	75	nA
		$-40°C \le T_A \le +85°C$		15	125	nA
Input Voltage Range	V_{IN}		0.3		4.7	V
Common-Mode Rejection Ratio	CMRR	$+0.8\ V \le V_{CM} \le +2\ V$		85		dB
		$-40°C \le T_A \le +85°C$		80		dB
A_{VO}		R_L = 2 kΩ, $-0.5\ V \le V_O \le +4.5\ V$	25	60		V/mV
		$-40°C \le T_A \le +85°C$	20	50		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage, High	V_{OH}	$I_L \le -15$ mA	4.2	4.5		V
		$I_L \le -10$ mA, $-40°C \le T_A \le +85°C$	4.5	4.8		V
Output Voltage, Low	V_{OL}	$I_L \le -15$ mA		0.6	1.0	V
		$I_L \le -10$ mA		0.3	0.5	V
		$I_L \le -10$ mA, $-40°C \le T_A \le +85°C$		0.7	1.1	V
Output Short Circuit Current Limit	I_{SC}	$-40°C \le T_A \le +85°C$		40		mA
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}	V_O = 0 V		1.7	2.9	mA
		$-40°C \le T_A \le +85°C$		1.75	3.0	mA
DYNAMIC PERFORMANCE						
Total Harmonic Distortion	THD	R_L = 10 kΩ, f = 1 kHz, V_O = 1 V rms		0.0006		%
Slew Rate	SR	R_L = 2 kΩ‖50 pF		12		V/µs
Gain Bandwidth Product	GBW	R_L = 2 kΩ‖10 pF		6		MHz
Channel Separation	CS	R_L = 2 kΩ, f =1 kHz		128		dB
NOISE PERFORMANCE						
Voltage Noise Spectral Density	e_n	f > 1 kHz		8		$nV/\sqrt{Hz}$
Current Noise Spectral Density	i_n	f > 1 kHz		< 1		$pA/\sqrt{Hz}$

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage (V_S) . . . . . ±18 V
Input Voltage (V_{IN}) . . . . . ±15 V
Differential Input Voltage[2] . . . . . ±15 V
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . −40°C to +85°C
Junction Temperature Range . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C
ESD Susceptibility . . . . . 2,000 V

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supplies less than ±15 V, the input voltage and differential input voltage must be less than ±15 V.

Package Type	θ_{JA}*	θ_{JC}	Units
8-Lead Plastic DIP	103	43	°C/W
8-Lead SOIC	158	43	°C/W
8-Lead microSOIC	206	43	°C/W
14-Lead SOIC	120	36	°C/W
14-Lead TSSOP	180	35	°C/W

*θ_{JA} is specified for the worst case conditions, i.e., for device in socket for DIP packages and soldered onto a circuit board for surface mount packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
SSM2275P	–40°C to +85°C	8-Lead PDIP	N-8
SSM2275S	–40°C to +85°C	8-Lead SOIC	SO-8
SSM2275RM	–40°C to +85°C	8-Lead microSOIC	RM-8
SSM2475S	–40°C to +85°C	14-Lead SOIC	R-14
SSM2475RU	–40°C to +85°C	14-Lead TSSOP	RU-14

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2275/SSM2475 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

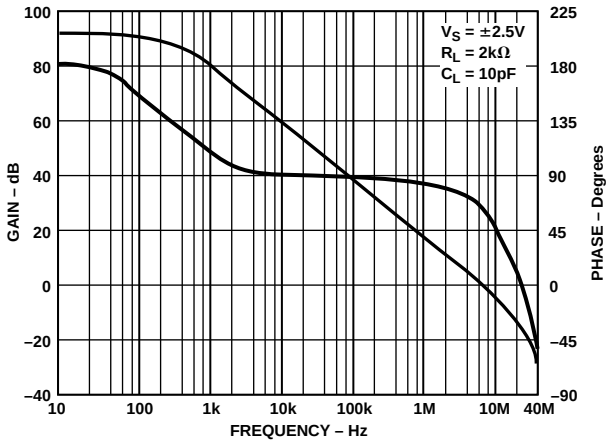

Figure 1. Phase/Gain vs. Frequency

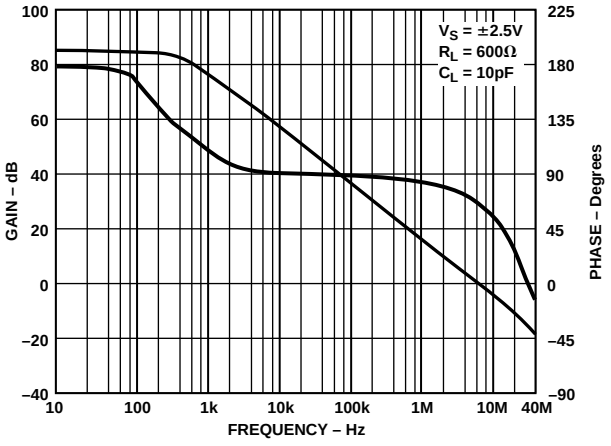

Figure 2. Phase/Gain vs. Frequency

SPICE Macro-model

The SPICE macro-model for the SSM2275 is shown in Listing 1 on the following page. This model is based on typical values for the device and can be downloaded from Analog Devices' Internet site at **www.analog.com**. The model uses a common emitter output stage to provide rail-to-rail performance. A resistor and dc voltage source, in series with the collector, accurately portray output dropout voltage versus output current. The VCMH and VCML sources set the upper and lower limits of the input common mode voltage range. Both are set up as a function of the supply voltage to mimic the varying common mode range with supply voltage. The EOS voltage source establishes the offset voltage and is also used to create the common-mode rejection and power supply rejection characteristics for the model.

A secondary pole section is also set up to vary the gain bandwidth product and phase margin of the model based on the supply voltage. The H1 and VR1 sources set up an equivalent resistor that is linearly varied with supply voltage. This equivalent resistance, in parallel with C2, creates the secondary pole. G2 is also linearly varied to increase the GBW at higher supply voltages. With a supply voltage of 5 V, the gain bandwidth product is 6.3 MHz with a 47 degree phase margin. At a 30 V supply voltage, the GBW product moves out to 7.5 MHz with 48° phase margin.

The broadband input referred voltage noise for the model is 6.8 nV/$\sqrt{\text{Hz}}$. Flicker noise characteristics are also accurately modeled with the 1/f corner frequency set through the KF and AF terms in the input stage transistors. Finally, a voltage-controlled current source, GSY, is used to model the amplifier's supply current versus supply voltage characteristics.

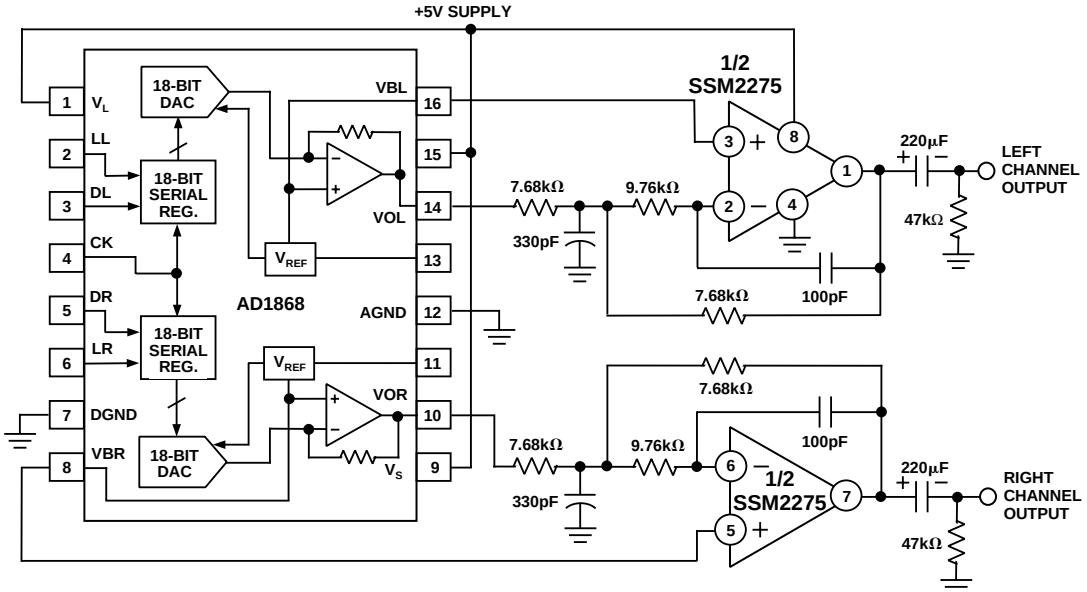

Figure 42. A Smoothing Filter for an 18-Bit Stereo DAC