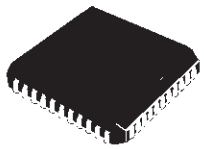
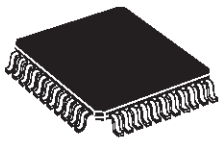
STLC7545

ENHANCED V.34 BIS ANALOG FRONT-END

- FULL ECHO CANCELLING CAPABILITY
- FULLY COMPATIBLE WITH THE ST7544
- 16-BIT OVERSAMPLING A/D AND D/A CONVERTERS
  - Programmable down-sampling frequency from 7200 to 22kHz.
  - Sampling frequency can be 3, 4, 6, 8, 12, 16 x symbol rate.
  - Programmable Oversampling frequency (128, 160 or 192 x sampling frequency).
  - The STLC7545 can work with external oversampling clocks.
  - Programmable symbol rate (600, 1200, 1600, 2400, 2560, 2743, 2800, 2954, 3000, 3200, 3429 and 3491).
  - Bit rates of 300bps, 600bps, 1200 and all multiples of 2400bps up to 38400bps can be generated.
  - Dynamic range : 92dB with a sampling frequency 9600Hz, oversampling ratio 160.
  - Total harmonic distortion : -89dB.
- ON CHIP REFERENCE VOLTAGE
- THREE PROGRAMMABLE DIGITAL FILTERS SECTIONS (up to 14th order each, coefficients loaded into RAM) :
  - Tx interpolation filter
  - Rx decimation filter
  - Rx reconstruction filter
- ANCILLARY CONVERTERS FOR EYE-DIAGRAM MONITORING
- CLOCK SYSTEM BASED ON DIGITAL PHASE LOCKED LOOPS
  - Separate Tx DPLL and Rx DPLL
  - Terminal clock input for Tx synchronization on all multiples of 2400Hz (VFast synchronization mode) or on sub-multiple of baud rate (7544 synchronization mode)
  - Bit, Baud, sampling and highest synchronous clock outputs
  - Maximum master clock frequency is 38MHz
- SINGLE OR DUAL SYNCHRONOUS SERIAL INTERFACE TO DSP
- ANALOG POWER SUPPLY VOLTAGE : +5V
- DIGITAL POWER SUPPLY FROM 3.3V TO 5V
- LOW POWER CONSUMPTION :
  - 100mW operating power at the nominal crystal frequency of 36.864MHz (digital supply at 3.3V)
  - Less than 5mW in the Low-Power Reset Mode
- 0.7µm CMOS PROCESS
- PLCC44 OR TQFP44 (1.4mm body thickness)



PLCC44 (Plastic Leaded Chip Carrier)
ORDER CODE : STLC7545CFN



TQFP44 (10 x 10 x 1.4mm)
(Thin Full Plastic Quad Flat Pack)
ORDER CODE : STLC7545TQFP4Y

DESCRIPTION

The STLC7545 is a single chip Analog Front-End (AFE) designed to implement high speed voice-grade Modems up to 384kbps with echo cancelling capability.
Associated with one or several Digital Signal Processors (DSP), it provides a powerful solution for the implementation of multi-mode Modems meeting CCITT (V.17, V.21, V.22, V.22 bis, V.23, V.26, V.27, V.29, V.32, V.32bis, V.33, V.34 and V.34bis) and BELL (103, 202, 212A...) recommendations. It is fully compatible with the ST7544 and is also well suited emerging applications involving bit rates up to 38400bps (in the VFast synchronization mode).
The transmit section includes a 16-bit over-sampling D/A converter with a programmable interpolating filter. The receive section includes a 16-bit oversampling A/D converter with two programmable filters (one for decimation and the other for reconstruction). Oversampling ratio is selectable to either 128, 160 or 192. Two additional 8-bit D/A converters allow eyediagram monitoring on a scope for modem performance adjustment.
Two independant clock generator systems are provided, one synchronized on the Tx rate and the other on the Rx rate.
In External Clock Mode, external oversampling clocks can be provided to the chip.
Two independant synchronous serial interfaces (SSI) allow several versatile ways of communicating with standard DSPs.
To save power, e.g. in lap-top modem applications, the lowpower reset mode can be used to reduce the power consumption to less than 5mW.

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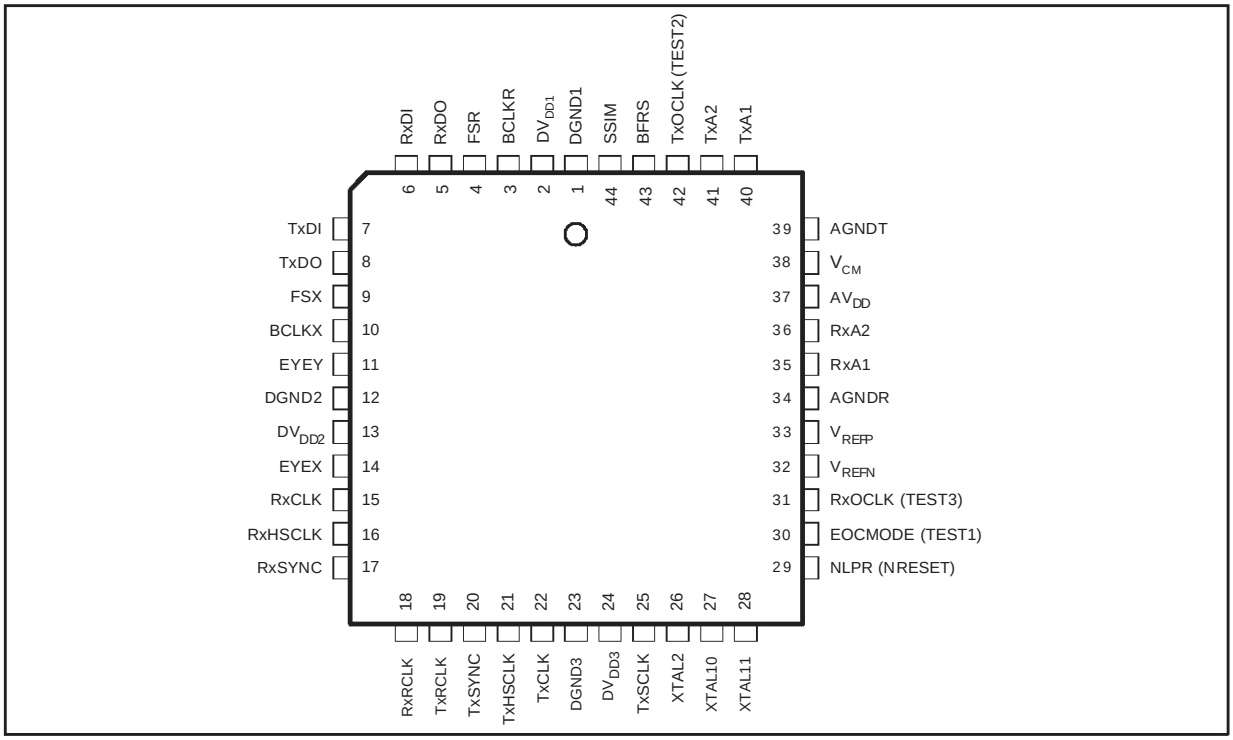
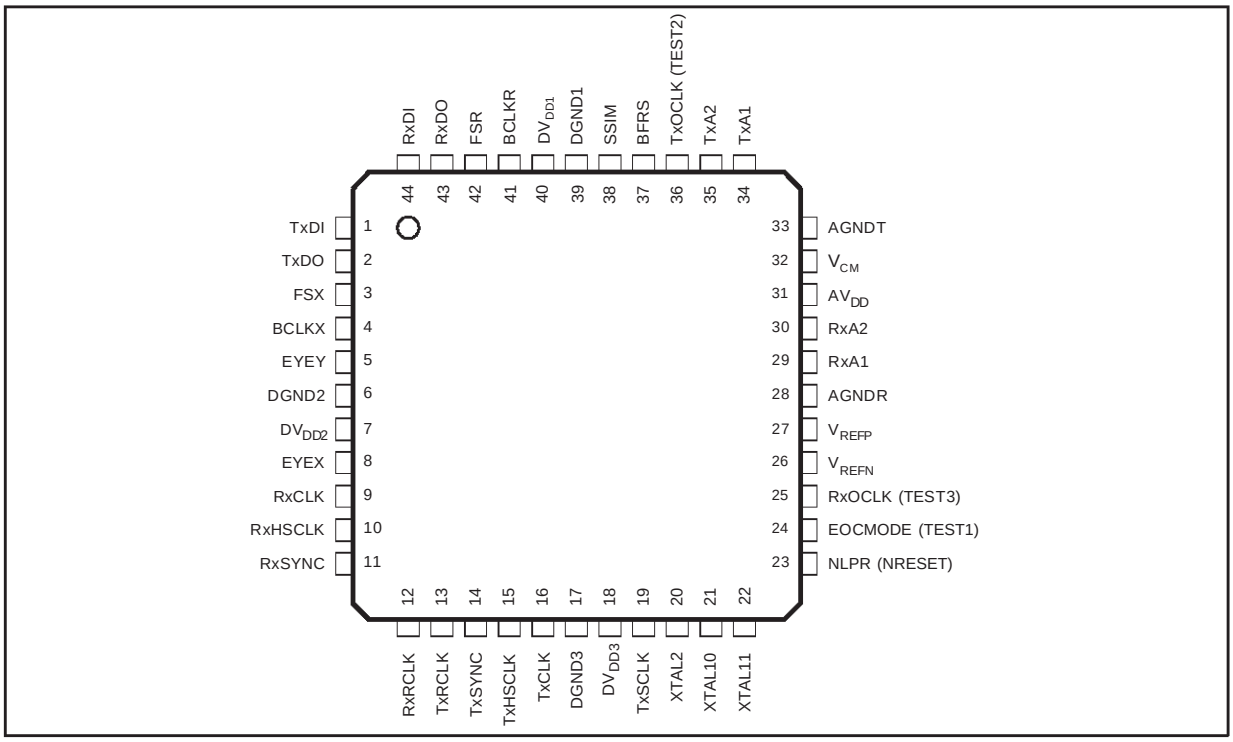
I - PIN DESCRIPTION

I.1 - PIN CONNECTIONS (Top View)

PLCC44



TQFP44



Note : The pin names in the parenthesis are the corresponding for the ST7544.

I - PIN DESCRIPTION (continued)

I.2 - PIN LIST

PQFP	PLCC	NAME	DESCRIPTION
39	1	DGND1	Digital Ground (0V)
40	2	DV_{DD1}	Positive Digital Power Supply (3.15V to 5.25V)
41	3	BCLKR	Receive bit Clock Output
42	4	FSR	Receive Frame Synchronization Output
43	5	RxDO	Receive Serial Data Output
44	6	RxDI	Receive Serial Data Input
1	7	TxDI	Transmit Serial Data Input
2	8	TxDO	Transmit Serial Data Output
3	9	FSX	Transmit Frame Synchronization Output
4	10	BCLKX	Transmit Bit Clock Output
5	11	EYEY	8 bit Y D/AC Output for Eye Pattern display
6	12	DGND2	Digital Ground (0V)
7	13	DV_{DD2}	Positive Digital Power Supply (3.15V to 5.25V)
8	14	EYEX	8bit X D/AC Output for Eye Pattern display
9	15	RxCLK	Receive Bit Rate Clock Output
10	16	RxHSCLK	Receive Highest Clock Output
11	17	RxSYNC	Receive Synchronization Pulse Output
12	18	RxRCLK	Receive Baud Rate Clock Output
13	19	TxRCLK	Transmit Baud Rate Clock Output
14	20	TxSYNC	Transmit Synchronous Pulse Output
15	21	TxHSCLK	Transmit Highest Clock Output
16	22	TxCLK	Transmit Bit Rate Clock Output
17	23	DGND3	Digital Ground (0V)
18	24	DV_{DD3}	Positive Digital Power Supply (3.15V to 5.25V)
19	25	TxSCLK	Transmit Synchronization Clock Input
20	26	XTAL2	Crystal Output
21	27	XTAL10	External Clock/Crystal Input 1
22	28	XTAL11	External Clock/Crystal Input 2
23	29	NLPR	Low Power Reset Input
24	30	EOCMODE (TEST1)	External Oversampling Clock Mode Input. Must be tied to DGND in either the STLC7545 normal mode or the 7544 mode.
25	31	RxOCLK (TEST3)	Receive Oversampling Clock Input. Output high-impedance in normal mode.
26	32	V_{REFN}	16 bit D/AC and A/DC Negative Reference Voltage
27	33	V_{REFP}	16 bit D/AC and A/DC Positive Reference Voltage
28	34	AGNDR	Analog Ground (0V)
29	35	RxA1	Receive Positive Analog Input
30	36	RxA2	Receive Negative Analog Input
31	37	AV_{DD}	Positive Analog Power Supply (+5V±5%)
32	38	V_{CM}	Common Mode Voltage Output (2.5V ±10%)
33	39	AGNDT	Analog ground (0V)
34	40	TxA1	Smoothing filter positive Output
35	41	TxA2	Smoothing filter negative Output
36	42	TxOCLK (TEST2)	Transmit Oversampling Clock Input. Output high-impedance in normal mode.
37	43	BFRS	Bit Frame Rate Select Input
38	44	SSIM	Serial Synchronous Interface Mode Input

Note : The pin names in brackets are the corresponding names for the ST7544.

I - PIN DESCRIPTION (continued)

I.3 - PIN FUNCTION

I.3.1 - Power Supply (9 Pins)

Analog V_{DD} Supply (AV_{DD})
This pin is the positive analog power supply (+5V±5%) for the Transmit and the Receive sections. It is not internally connected to digital V_{DD} supply (DV_{DD1-3}).

Digital V_{DD} Supply (DV_{DD1},DV_{DD2},DV_{DD3})
These pins are the positive digital power supply (3.5V to 5.25V) for Transmit and Receive digital internal circuitry.

Analog Ground (AGNDT,AGNDR)
These pins are the analog ground return of the analog Transmit (Receive) section.

Digital Ground (DGND1,DGND2,DGND3)
These pins are the ground connections for Transmit and Receive internal digital circuitry.

Note 1 : To obtain published performance, the analog V_{DD} and Digital V_{DD} should be decoupled with respect to AGND and DGND, respectively. The decoupling is intended to isolate digital noise from the analog section; decoupling capacitors should be as close as possible to the respective analog and digital supply pins.

Note 2 : All the ground pins must be tied together. In the following section, the ground and supply pins are refered to as GND and V_{DD}, respectively.

I.3.2 - Clock and Control Signals (16 Pins)

External Clock/Crystal Inputs (XTAL10,XTAL11)
XTAL10 and XTAL11 inputs must be tied to external crystal(s) or external clock(s). These inputs are selected from the TxCtrl register. The maximum clock rate is 38MHz. XTAL10 is the default External Clock/Crystal input. It is mandatory to shortcircuit XTAL10 and XTAL11 when a single external crystal or clock generator is used. The nominal master clock frequency is 36.864MHz (this frequency and the frequency 25.8048MHz are well suited for the V.34 application) but the onchip amplifier is designed for a parrallel crystal oscillator with a frequency equal to 18.432MHz. The other master clocks frequencies (18.432MHz, 25.8048MHz and 29.4912MHz) are well suited for the well known CCITT recommendations (V.21 through V.32bis).

Crystal Outputs (XTAL2)
This output is to be tied to one or two external crystals (see Figure 1). If an external clock is used, XTAL2 should be left open circuit.

Low power and Reset Input (NLPR)
This pin , when low, synchronizes the STLC7545 clock system and puts it in low power mode. NLPR pin must be tied to V_{DD} during normal operation. Access to the chip is disabled during power-on reset until the clock oscillator starts. The reset time duration can be increased by connecting the NLPR input to an external RC network (see Figure 9). The Low-Power Reset Mode is activated when this pin is tied to GND (Operation of all clocks and the analog section is stopped).

Transmit Synchronization Clock Input (TxSCLK)
This pin can be connected to an external terminal clock to phase-lock the internal transmit clocks. It can be disabled under software control to allow the Tx DPLL to free run or phase lock on the Rx clock system. To phase lock the TxDPLL there must be transition on TxSCLK input within FCOMP period when programming TxCR2 register.

Transmit Bit Rate Clock Output (TxCLK)
This pin outputs the synchronous transmit bit clock selected for the MODEM.

Transmit Baud Rate Clock Output (TxRCLK)
This pin, when the bit D4 within receive register RxCR3 is set to 0, outputs the synchronous transmit baud rate clock (initial state). When bit D4 is set to 1 this pin outputs the frequency comparison signal FCOMP (used by the TxDPLL in both 7544 mode and V.Fast synchronization) when bit 0 of RxCR1 is set to 0 this output is disabled.

Transmit Synchronization Pulse Output (TxSYNC)
This pin outputs the synchronization transmit reset pulse when a soft reset is applied to the STLC7545. Combined with TxHSCLK clock it can be used to externally provide any synchronous transmit clock.

Transmit Highest Clock Output (TxHSCLK)
This pin outputs the highest synchronous transmit clock to provide any external or multiplexing clock when bit 0 of RxCR1 is set to 0 this output is disabled.

Transmit Oversampling Clock input (TxOCLK)
This input can be connected to an external clock to provide the chip with the over-sampling clock, depending on the External Over sampling Mode input (EOCMODE). In normal mode this pin should be static (tied to GND or V_{DD}).

Receive Bit Rate Clock Output (RxCLK)
This pin outputs the synchronous receive bit clock selected for the MODEM.

Receive Baud Rate Clock Output (RxRCLK)
This pin outputs the synchronous Receive baud rate clock when bit 0 of RxCR1 is set to 0 this output is disabled.

I - PIN DESCRIPTION (continued)

Receive Synchronization Pulse Output (RxSYNC)
This pin outputs the synchronization receive reset pulse when a soft reset is applied to the STLC7545. Combined with RxHSCLK clock it can be used to externally provide any synchronous receive clock.

Receive Highest Clock Output (RxHSCLK)
This pin outputs the highest synchronous receive clock to give any external or multiplexing clock when bit 0 of RxCR1 is set to 0 this output is disabled.

Receive Oversampling Clock input (RxOCLK)
This input can be connected to an external clock to provide the chip with the oversampling clock, depending on the External Over sampling Mode input Pin (EOCMODE). In normal mode this pin should be static (tied to GND or V_{DD}).

External Oversampling Clock Mode (EOCMODE)
This pin is used for selecting one of the two possible oversampling modes. When EOCMODE is tied to GND, all the clock are provided internally (mode compatible with the ST7544). When EOCMODE is tied to V_{DD}, the oversampling clocks must be input on TxOCLK and RxOCLK pins. The TxHSCLK (RxHSCLK) and TxSync (RxSync) signals along with external fractional divider can be used to provide the oversampling clocks to the STLC7545.

I.3.3 - Synchronous Serial Interfaces (SSIA,SSIB) (10 pins)

Serial Synchronous Interface Mode input (SSIM)
This input activates one or both serial interfaces. When SSIM is tied to V_{DD}, both A and B ports are functional : port A (SSIA) is dedicated to the Transmit channel and port B (SSIB) is dedicated to the Receive channel.
When SSIM is tied to GND only port A (SSIA) is selected. In this case SSIA carries both Tx and Rx Signals and EYE pattern.

Bit Frame Rate Select input (BFRS)
This input selects one of the two possible bit frequencies for the BCLKX and BCLKR clocks. When BFRS is tied to V_{DD} the BCLKX (BCLKR) frequencies are equals to the oversampling ratio (divider V Table 40) times the FSX (FSR) frequencies. When BFRS is tied to GND, BCLKX (BCLKR) frequencies are equal to V/2 times the FSX (FSR) frequencies.

Frame Synchronization Transmit output (FSX)
This output clock is the Transmit Frame synchronization pulse signal of the SSIA port which has nominal frequency equal to the transmit sampling frequency. This pulse indicates the beginning of the 16-bit serial words on the serial data input/output port A.

Bit Clock Transmit output (BCLKX)
This output pin provides the serial bit clock for the SSI port A. The BCLKX frequency equals V or V/2 times the Transmit sampling frequency, depending on the Bit Frame Select Input (BFRS).

Serial Data Transmit input (TxDI)
This input receives word-oriented serial data. Data is loaded from TxDI into the Transmit Shift Register (TSRIN) on the falling edge of BCLKX and transfered to the Transmit Buffer Register (TBRIN) when a complete 16 bit word has been received. Data is assumed to be received MSB first.

Serial Data Transmit output (TxDO)
This output sends word-oriented serial data. The 16 bit Data Word loaded in the Transmit Buffer Register (TBROUT) is transfered to the Transmit Shift Register (TSROUT) and clocked out of TSROUT on the rising edge of BCLKX. Serial words are transmitted MSB first.

Receive Frame Synchronization output (FSR)
This output clock is the Receive Frame synchronization pulse signal of SSI port B which has frequency equal to the receive sampling frequency. This pulse is used to indicate the beginning of serial words on the serial data input/output port B.

Receive Bit Clock output (BCLKR)
This output pin provides the serial bit clock for the SSI port B. The BCLKR frequency is V times or (V/2) times, selected by BFRS) the receive sampling frequency.

Receive Serial Data input (RxDI)
This input receives word-oriented serial data. Data is clocked from RxDI into the Receive Shift Register (RSRIN) on the falling edge of BCLKR and transfered to the Receive Buffer Register (RBRIN) when a complete 16-bit word has been received. Data is assumed to be received MSB first.

Receive Serial Data output (RxDO)
This output sends word-oriented serial data. The 16-bit Data Word loaded in the Receive Buffer Register (RBROUT) is transfered to the Receive Shift Register (RSROUT) and clocked out of RSROUT on the rising edge of BCLKR. Serial words are transmitted MSB first.

I - PIN DESCRIPTION (continued)

I.3.4 - Analog Interface (9 pins)

D/AC and A/DC Positive Reference Voltage output (V_{REFP})
This pin provides the Positive Reference Voltage used by the 16-bit converters. The reference voltage, V_{REF}, is the voltage difference between the V_{REFP} and V_{REFN} outputs, and its nominal value is 2.5V. V_{REFP} should be externally decoupled with respect to V_{CM} (see Figure 17).

D/AC and A/DC Negative Reference Voltage (V_{REFN})
This pin provides the Negative Reference Voltage used by the 16 bit converters, and should be externally decoupled with respect to V_{CM}.

Common Mode Voltage Output (V_{CM})
This output pin is the common mode Voltage (AV_{DD}-AGND)/2 internally generated. This output must be decoupled with respect to AGND. This output pin could be forced externally (compatible with ST7544 application).

Smoothing filter positive Output (TxA1)
This pin is the positive output of the fully differential analog smoothing filter.

Smoothing filter negative Output (TxA2)
This pin is the negative output of the fully differential analog smoothing single pole switch capacitor filter. Outputs TxA1 and TxA2 provide analog signals with maximum peak to peak amplitude 2 x V_{REF}, and must be followed by an external continuous time two pole smoothing filter (see Figure 16). The smoothing filter order depends of the acceptable transmit signal spectrum on the line. The cut-off frequency of the external filter must be greater than two times the transmit sampling frequency (Fsx), so that the combined frequency response of both the internal and external filters is flat in the pass band.

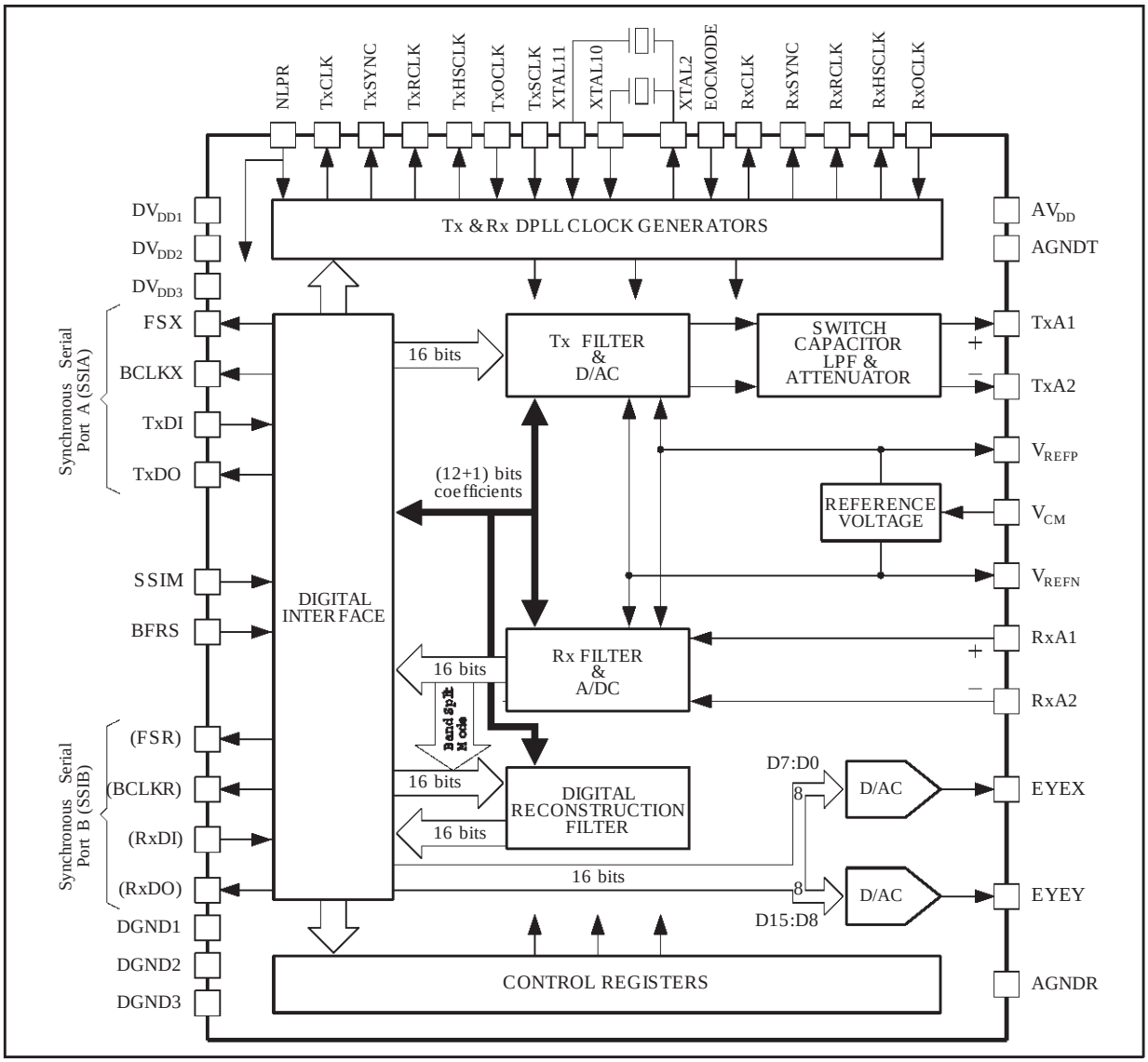
Receive Positive Analog Input (RxA1)
This pin is the differential positive A/DC Input.

Receive Negative Analog Input (RxA2)
This pin is the differential negative A/DC Input.
These analog inputs (RxA1,RxA2) are presented to the SigmaDelta modulator, the analog input peak to peak signal range must be less than 2 x V_{REF}, and must be preceeded by an external continuous-time single pole anti-aliasing filter (see Figure 16). The cut-off frequency of the filter must be lower than one half the transmit over-sampling frequency (TxOSCK). These filters should be set as close as possible to the RxA1 (RxA2) pins.

D/AC output for Eye Pattern (EYEX,EYEY)
These pins are the outputs of two 8-bit digital to analog converters used to monitor, on a CRT, the X and Y quadrature signals of the eye pattern of the demodulated signal.

II - BLOCK DIAGRAM

Figure 1 : General Block Diagram

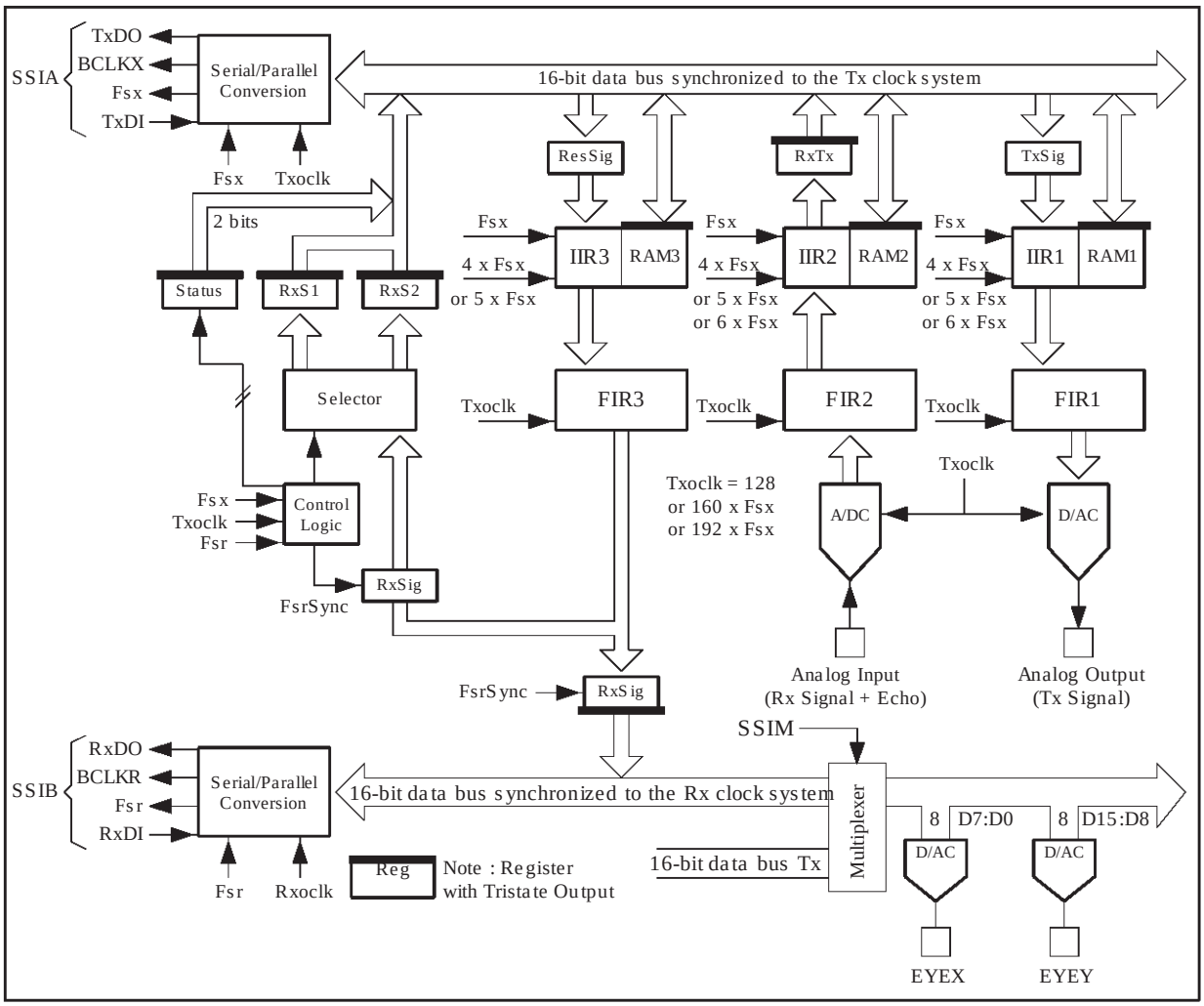


III - FUNCTIONAL DESCRIPTION

III.1 - SIGNAL TRANSFER BLOCK DIAGRAM

The STLC7545 Block Diagram illustrates three paths as follows : The Transmit D/A Section, the Receive A/D section and the Receive Reconstruction section.

Figure 2 : Signal Transfer Block Diagram



III - FUNCTIONAL DESCRIPTION (continued)

III.2 - TRANSMIT D/A SECTION

The functions included in the Tx D/A section are detailed hereafter.

III.2.1 - Interpolation Filters

The oversampling is performed by two cascaded digital interpolating filters : IIR1 and FIR1. The IIR1 and FIR1 filters are sampled at 4 x Fsx and 128 x Fsx (5 x Fsx and 160 x Fsx) (6 Fsx and 192 x Fsx), respectively.

III.2.1.1 - Programmable Interpolation Filter (IIR1)

IIR1 is an infinite impulse response interpolating filter.

The purpose of this digital filter is to interpolate 4-times (5 times, 6 times) the digital signal coming from the DSP. This filter is sampled at the basic sampling frequency, (e.g. 9600 x 4 Hz), and must exhibit, as a minimum, a low-pass section which is mandatory to remove replicas above half the sampling frequency (e.g. 4800Hz) (see Figure 13).

The digital samples are encoded in 16-bit two's complement format.

The IIR1 filter is a cascade of seven biquads (see Figure A1). The filter coefficients are loaded into the associated RAM (38 x 13). Each coefficient is coded into 12bits and can be doubled by virtue of an extra bit. All 38 coefficients have to be loaded to implement an IIR transfer function (see Annexe A).

This filter has been made programmable to offer each user the possibility to add filtering characteristics, e.g. high-pass section or equalization, matched to a particular application.

III.2.1.2 - FIR Filter (FIR1)

FIR1 is a finite impulse response interpolating filter. Its input sampling frequency is 4 x Fsx (or 5 x Fsx) (or 6 x Fsx) and its interpolation ratio is 32. The Z transfer function of this FIR is :

$$H(z) = \left(\frac{1 - z^{-32}}{32\,(1 - z^{-1})} \right)^3$$

with Z = exp (j2πF/Txoclk)
and Txoclk = 128 (160, 192) x Fsx

III.2.2 - D/A Converter

The 128-times (160 times, 192 times) oversampled D/A converter includes a second order digital noise shaper, a one bit D/A converter and a single pole analog low-pass filter. The gain of the last output stage can be programmed to 0dB,-6dB or infinite attenuation. The cut-off frequency of the single pole switch-capacitor low-pass filter is :

$$fc\text{-}3dB = Txoclk / (2 \times \pi \times 10)$$

where Txoclk = 128 (160, 192) x Fsx

Continuous-time filtering of the analog differential output is necessary using an off-chip amplifier and a few external passive components (see Figure 16).

At least 86dB signal to noise plus distortion ratio can be obtained in the frequency band 300-3400Hz, with a -6dBr output signal.

III.3 - RECEIVE A/D SECTION

The different functions included in the Rx A/D section are detailed hereafter. The format used at the digital interfaces of the Rx channel is two's complement encoded 16-bit.

III.3.1 - A/D Converter

The 128 (160, 192) oversampled A/D converter is based on a second order sigma-delta modulator. The signal to noise plus distortion ratio obtained for a signal spectrum limited to the 300-3400Hz telephone band, is typically 86dB with a -6dBr input signal.

III.3.2 - Decimation Filters

The 128 (160, 192) decimation is performed by two interpolating digital filters : FIR2 and IIR2, which are sampled at 128 x Fsx and 4 x Fsx (160 x Fsx and 5 x Fsx) (192 x Fsx and 6 x Fsx), respectively .

III.3.2.1 - FIR Filter (FIR2)

FIR2 is a finite impulse response decimating filter. Its sampling frequency is 128 x Fsx (or 160 x Fsx or 192 x Fsx) and its decimation ratio is 32. The Z transfer function of this FIR is :

$$H(z) = \left(\frac{1 - z^{-32}}{32\,(1 - z^{-1})} \right)^3$$

with Z = exp (j2πF/Txoclk)
and Txoclk = 128 (160, 192) x Fsx

III - FUNCTIONAL DESCRIPTION (continued)

III.3.2.2 - Programmable Decimation Filter (IIR2)

IIR2 is an infinite impulse response filter. It provides the low-pass filtering needed to remove the noise remaining above half the sampling frequency (e.g. 4800Hz) (see Figure 14). The output of the IIR2, RxTx, will be processed by the DSP. In "band split" mode (see Table 21), RxTx becomes the input signal to IIR3. The RxTx will always be available on serial interface (SSIA in Figure 2).

The IIR2 filter is a cascade of seven biquads. The filter coefficients are loaded into the associated RAM (38 x 13).

The filter transfer function has been made programmable in order to meet specific requirements. The sampling frequency is 4-times (5-times, 6-times) the down-sampling frequency selected for the Tx section (e.g. 9600 x 4Hz).

To support echo cancelling applications the clocks used for the A/D converter and the decimation filters are synchronized on the Tx system clock, i.e. on the Tx rate. It must be pointed out that using a single clock system in A/D and D/A conversions is important for reducing induced noise.

The 12+1 bit filter coefficients are loaded into the internal RAM2 and must be loaded from the serial bus. All 38 coefficients have to be loaded to implement an IIR transfer function.

III.3.3 - Eye-diagram Display

Two 8-bit digital to analog converters are provided to monitor, on a CRT, the X and Y quadrature signals of the eye pattern related to the demodulated signal. The format of the data input is MSB first, 8-bit two's complement, and most significant byte for EYEY sample and least significant byte for the EYEX sample. The reference voltage of these two converters is the power supply voltage V_{DD}. The EYE pattern can be monitored on one or two Synchronous Serial Interface mode.

III.4 - RECEIVE RECONSTRUCTION SECTION

As the Rx channel sampling is synchronized to the Tx system clock, it is necessary to reconstruct the Rx signal in order to get samples synchronized to the Rx symbol rate recovered in the demodulator.

The function of the reconstruction filter (IIR3 and FIR3) is to oversample by 128 x Fsx (160 x Fsx, 192 x Fsx) the receive signal (ResSig) comming from the DSP after echo cancellation. The oversampled signal is then down-sampled at Fsr rate to make it available to the DSP as RxSig at SSIB or RxS1/RxS2 at SSIA (see section IV.1 and IV.2). The down sampling process does not introduce significant error.

The transfer function of the first section of the reconstruction filter is programmable in the same way as the Tx and Rx IIR filters previously described.

III.4.1 - Programmable Interpolation Filter (IIR3)

IIR3 is an infinite impulse response interpolating filter.

The purpose of this digital filter is to interpolate 4-times (5-times, 6-times) the digital signal from the DSP. This filter is sampled at 4-times (5-times, 6-times) the basic sampling frequency, (e.g. 9600 x 4 Hz).

The digital samples are encoded in 16-bit two's complement format.

The IIR3 filter is a cascade of seven biquads. The filter coefficients are loaded into the associated RAM (38 x 13). Each coefficient is coded into 12 bits and can be doubled by virtue of an extra bit. All 38 coefficients have to be loaded to implement an IIR transfer function.

This filter has been made programmable to offer each user the possibility to add filtering characteristics, e.g. highpass section or equalization, matched to a particular application.

For example, in a band-split MODEM application, the first section can be a wide channel band-pass filter (allowing the DSP to supervise boundary audio tones) and the second section can be dedicated to high band and low band splitting.

III.4.2 - FIR Filter (FIR3)

FIR3 is a finite impulse response interpolating filter. Its input sampling frequency is 4 x Fsx (5 x Fsx), (6x Fsx) and the interpolation ratio is 32. The Z transfer function of this FIR is :

$$H(z) = \left(\frac{1 - z^{-32}}{32\ (\ 1 - z^{-1}\ )} \right)^3$$

with Z = exp (j2πF/Txoclk)
and Txoclk = 128 (160, 192) x Fsx

III - FUNCTIONAL DESCRIPTION (continued)

III.5 - CLOCK GENERATION

Master clock is obtained from either a crystal tied between pins XTAL10 (or XTAL11) and XTAL2 or from an external signal connected to the XTAL10 (or XTAL11) pin, in the latter case, the XTAL2 pin should be left open circuit.

Two external crystals (or two external master clock signals), software selectable one at a time, can be used to cope with complex applications. It is mandatory to shortcircuit XTAL10 and XTAL11 when a single external crystal or clock generator is used.

The crystal selection is done by bit D13 (QS) in TxCTRL word of the serial interface A.
Setting QS to 0 select the XTAL11 input and TxCLK = FQ / (N x R x S x T x CS) with CS = 8.
Setting QS to 1 select the XTAL10 Input and TxCLK = FQ / (N x R x S x T x CS) with CS = 16.

To insure the start-up of the STLC7545, the XTAL10 input must always be tied to a crystal or an external clock signal, as that pin is automatically selected when powering-on the device.

The different transmit (Tx) and Receive (Rx) clocks are obtained by master clock frequency division in several programmable counters. The Tx and Rx clocks can be synchronized on external signals by performing phase shifts in the frequency division process (equivalent to adding or suppressing master clock transitions at the counter inputs). Two independant digital phase locked loops (DPLL) are implemented using this principle , one for Tx and one for Rx.

Two clock modes are available, selected by the External Oversampling Clock Mode input pin (EOCMODE). When the EOCMODE pin is tied to the GND the internal clock mode is selected. In this mode all the clock are generated internally. When the EOCMODE pin is tied to V_{DD}, the External Oversampling Clock Mode is selected.

In external oversampling clock mode, the user must provide the chip with the oversampling frequency knowing the interpolation and the decimation ratios selected in the TxCR3 and RxCR3 register. It can be provided from the highest synchronous clock (TxHSCLK and RxHSCLK) using an external divider. In any case, the user will have to comply with the relation : Crystal frequency FQ must be greater than 470 x 4 x Fsx with an oversampling ratio of 128 or than 470 x 5 x Fsx with an oversampling ratio of 160 or than 470 x 6 x Fsx with an oversampling ratio of 192.

Several values can be chosen for the master clock frequency. The four frequencies given in table 1 are of particular interest, as they are compatible with standard Modem frequencies.

Note : In the remainder of the datasheet, unless otherwise indicated, 36.864MHz will be considered as the nominal master clock frequency. The maximum master clock frequency is 38MHz.

Table 1 : List of usual frequency available

Crystal Frequency	Symbol Rate Frequency	Bit Rate (bps)	Sampling (bps)
FQ (MHz)	Fbaud (baud)		Fsx, Fsr (Hz) (1)
18.432 (2)	600, 1200, 1600, 2400	All up to 19200	3,4,5,6,8,12 or 16 times Fbaud
25.8048	600, 1200, 1600, 2400, 2800	All up to 28800	3,4,5,6,8,12 or 16 times Fbaud
29.4912 (2)	600, 1200, 1600, 2400	All up to 19200	3,4,5,6,8,12 or 16 times Fbaud
36.864 (3)	600, 1200, 1600, 2400, 2560, 2743, 2954, 3000, 3200, 3429, 3491	All up to 38400	3,4,5,6,8,12 or 16 times Fbaud

Notes : 1. Depending on the symbol rate frequency
2. 7544 like
3. This crystal frequency provides all the symbol rates satisfying the relation :
Symbol rate = (2400 x 16)/K with K = (16, 15, 14, 13, 12, 11)
Symbol rate = (2400 x 8)/K with K = (8, 7, 6)
Symbol rate = (2400 x 10)/K with K = (8, 7)

III - FUNCTIONAL DESCRIPTION (continued)

III.5.1 - Transmit DPLL

Frequency control of the Tx clock system (Figure 10) is obtained by performing additional up or down counting steps in the three input dividers M, N and P.

These elementary phase shifts of one master clock period are repeated at either the rate of the Fsx clock, or half that rate, depending on the required capture and tracking ranges (see Table 15 and 26).

The average updated frequency then varies between the following limits :

$$FQ - FSHIFT \leq Faverage \leq FQ + FSHIFT$$

Where FQ is the master clock frequency and FSHIFT equals Fsx or Fsx/2 (see table 26).

The TxDPLL phase comparison which determines lead or lag decisions, is simply obtained by sampling the synchronization clock, TxSCLK or RxCLK, on the falling edges of an internal clock taken from the division chain, FCOMP (see table 25). FCOMP frequency must be an integer submultiple of the synchronization clock. This frequency determines the Tx jitter magnitude. In V.34 synchronization mode FCOMP is equal to 2400Hz, and in 7544 mode the synchronization clock FCOMP can be chosen to be equal to the baud rate frequency. Only phase shifts of the same sense (lead or lag) are performed during each FCOMP period. The actual phase shifts during FCOMP period are given by the ratio

$$FSHIFT/FCOMP$$

These phase shifts are performed at the inputs of the M,N, and P dividers to lock the DPLL to the synchronisation signal (see Table 22).

If there is no transition on TxSCLK Pin, the Tx DPLL is free running.

To phase lock the TxDPLL there must be transistion on TxSCLK input within FCOMP period when programming TxCR2 register.

The Tx clock system may also run freely without any phase shift. In this case, the TxSCLK input is no longer active.

The DPLL capture and tracking range equals ±FSHIFT/FQ. They have to be greater than ± 200ppm to comply with CCITT recommendations. FSHIFT = Fsx/2 minimizes the jitter. Because of this, there is a trade-off between higher capture and tracking ranges and lower jitter.

Ex : FQ = 36.864MHz and FSHIFT = 9600Hz.
Capture and tracking range = ± FSHIFT/FQ
= ± 9600Hz/36.864MHz = ± 260ppm

III.5.2. Transmit Clocks

III.5.2.1 - Internal Mode

The internal clock mode is selected when the pin EOCMODE is tied to GND. In this mode the STLC7545 provides three Tx programmable synchronous modem clocks :

- a transmit bit rate clock TxCLK
- a transmit baud rate clock TxRCLK
- a transmit highest synchronous clock TxHSCLK, associated with the TxSYNC synchronization pulse, useful to generate additional clocks (e.g. extra divisors) if needed.

The outputs of the TxRCLK and TxHSCLK clocks, can be disabled when not used, but in 7544 synchronisation mode a correct baud rate frequency must be programmed as the FCOMP clock frequency depends on it.

The Tx clock system provides the sampling and oversampling clocks as well as the bit and synchro clocks (BCLKX and FSX) used by the serial interface A (SSI-A) described in section IV.

The counters of the Tx clock system (Figure 10) are automatically reset when powering-on the STLC7545 and when the NLPR input level is low. They can also be reset, under software control, during the following conditions :

(1) on the next falling edge of the TxSCLK terminal clock or of the RxCLK receive bit rate clock (SST bit Table 22).
(2) on the next falling edge of the TxRCLK transmit baud rate clock (baud chain clock reset) and in the next falling edge of FCOMP (bit chain clocks) when TxCR0, TxCR2 or TxCR3 register is accessed.

The case (1) gives the capability to speed-up the Tx DPLL synchronization; the case (2) is useful to fix the phase of the bit rate clock with respect to the baud rate clock, in particular after each modification of the bit or baud rate value.

The internally generated pulse resetting the Tx counters is output at the TxSYNC pin in order to synchronize external functions using the TxHSCLK clock.

III.5.2.2 - External Mode

The external clock mode is selected when the pin EOCMODE is tied to the V_{DD}. In this mode the user must provide the STLC7545 with the transmit oversampling clock. The internal DPLL can be used if the external transmit oversampling clock is generated by a divider synchronized by both the TxHSCLK and TxSync signals.

III - FUNCTIONAL DESCRIPTION (continued)

III.5.3 - Receive DPLL

The synchronization of the Rx counters delivering the Rx clocks (Figure 11) is performed by addition or suppression of master clock periods under DSP control. In this case, the phase comparison function of the RxDPLL is implemented in the associated DSP recovering the received symbols.
Two types of phase shift control are provided in the STLC7545 :

- a coarse phase lag of programmable magnitude, obtained from the suppression of 64 to 4096 successive master clock transitions. This control is to be used to reduce the RxDPLL locking time.
- a fine phase lead or lag of programmable magnitude (i.e. 8 to 32 master clock periods or one Tx oversampling clock period) continuously used to implement the phase control loop. (see Table 38). Each elementary phase shift, corresponding to an addition or a subtraction of one master clock transition, is synchronized on an internal clock with frequency equal to the Rxoclk (128, 160 or 192 times the Rx sampling frequency Fsr). A phase shift is ,therefore, always completed in less than one Fsr period.

III.5.4 - Receive Clocks

III.5.4.1- Internal Mode

The internal clock mode is selected when the pin EOCMODE is tied to GND. In this mode the STLC7545 provides three Rx synchronous programmable modem clocks :

- receive bit rate clock RxCLK
- receive baud-rate clock RxRCLK
- receive highest synchronous clock, RxHSCLK associated with the RxSYNC synchronization pulse useful to generate additional clocks

The RxRCLK and RxHSCLK outputs can be disabled when not used. The bit rate clock frequency of the Rx modem can be chosen to be different from its Tx counterpart, provided Rx to Tx loopback is not required. The Rx clock system also provides the Rx sampling clock as well as the bit and synchro clocks (BCLKR and FSR) used by the serial interface B (SSI-B) described in section IV. The digital reconstruction filter implemented in the STLC7545 makes possible the choice of a receive nominal sampling frequency different from the transmit nominal sampling frequency. The counters of the Rx clock system (Figure 11) are reset when powering on the STLC7545 and when the NLPR input level is low. They can also be reset, under software control, on the next falling edge of the RxRCLK receive baud rate clock when the RxCR0, RxCR1 or RxCR3 register are accessed : this feature is used to fix the phase of the bit rate clock with respect to the baud rate clock, e.g. after each modification of the bit or baud rate value. The internally generated pulse resetting the Rx counters is output at the RxSYNC pin in order to be used with the RxHSCLK clock.

III.5.4.2 - External Mode

The external clock mode is selected when the pin EOCMODE is tied the V_{DD}. In this mode the user must provide the STLC7545 with the receive oversampling clock. The internal DPLL can be used if the external receive oversampling clock is generated by a divider synchronized by both the RxHSCLK and RxSync signals.

III.6 - SERIAL INPUT/OUTPUT SYNCHRONOUS INTERFACES

The STLC7545 has two Synchronous Serial Interfaces ports, SSIA and SSIB. They allow independent transmit and receive paths. Through the two serial ports, the STLC7545 can talk to various digital signal processors. The various serial interface signals and internal registers are given below :

SSI PORT A (SSIA)

- Transmit Frame Synchronization output (FSX)
- Transmit Bit clock output (BCLKX)
- Transmit Serial Data input (TxDI)
- Transmit input Shift Register (TSRIN)
- Transmit input Buffer Register (TBRIN)
- Transmit output Shift Register (TSROUT)
- Transmit Serial Data output (TxDO)

SSI PORT B (SSIB)

- Receive Frame Synchronization output (FSR)
- Receive Bit clock output (BCLKR)
- Receive Serial Data input (RxDI)
- Receive input Shift Register (RSRIN)
- Receive input Buffer Register (RBRIN)
- Receive output Shift Register (RSROUT)
- Receive Serial Data output (RxDO)

INPUT MODES

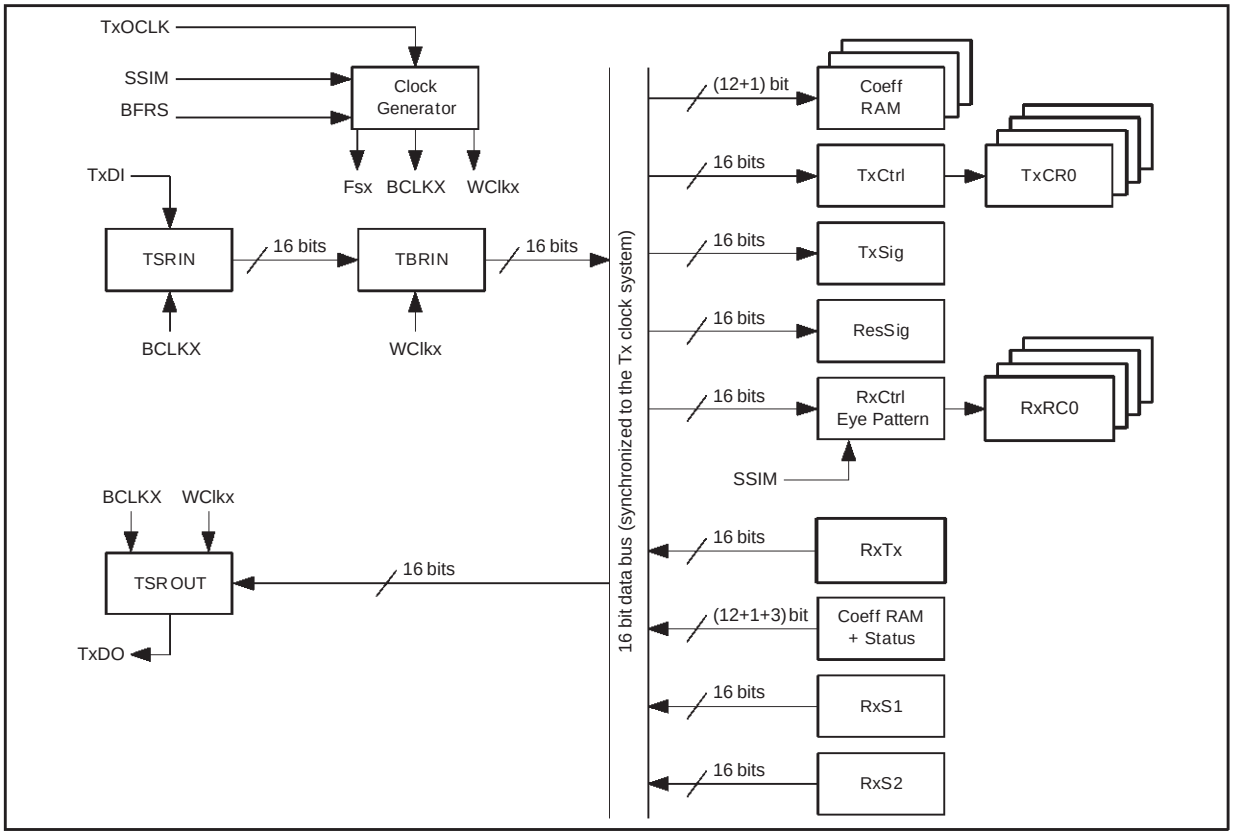
- Synchronous Serial Interface Mode (SSIM)
- Bit Frame Rate Select (BFRS)

With SSIM input, the user can choose either single interface mode or dual interface mode. In single interface mode (section IV.2), only port SSIA is operational. Where as in dual interface mode (section IV.1), both SSIA and SSIB ports are operational. These two ports carry data inside a synchronous frame consisting of four/five or eight/ten sixteen bit time slots (only the four first time slots are used for transporting information. SSIA port is synchronous to the Tx system clock and SSIB port is synchronous to Rx system clock. The format of the signal samples carried on these port is two's complement with MSB sent or received first. As explained hereafter it is also possible to use the port A only to transfer the data between the STLC7545 and the associated DSP.

III - FUNCTIONAL DESCRIPTION (continued)

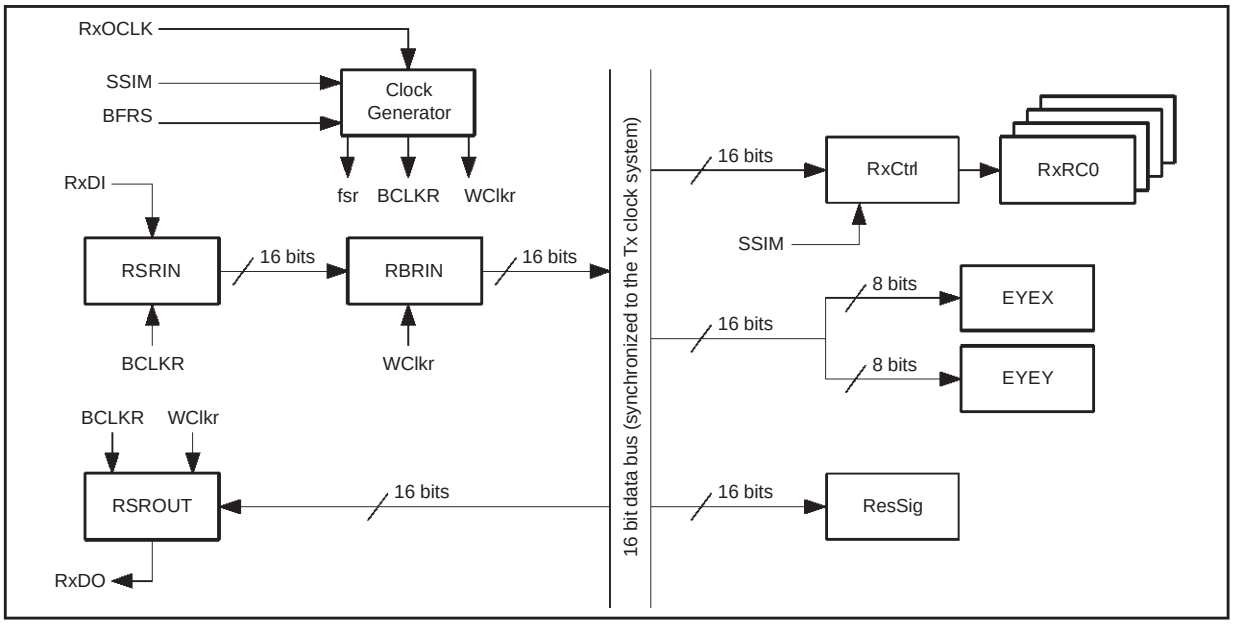
III.6.1 - Tx Clock Related Registers

Figure 3 : Tx Clocks Related Registers



III.6.2 - Rx Clock Related Registers

Figure 4 : Rx Clocks Related Registers



IV - SERIAL INTERFACE OPERATION

Serial data transmission (reception) is initiated by a frame synchro signal FSX (FSR). The Data is clocked from TxDI (RxDI) into TSRIN (RSRIN) on the falling edge of BCLKX (BCLKR) and transfered to the TBRIN (RBRIN) register when a complete 16 bit word has been received. Data is assumed to be received MSB first.

Serial data transmission (reception) output is initiated by a frame synchro signal FSX (FSR). The 16-bit Data word is loaded into TSROUT (RSROUT) and serially clocked out of TSROUT (RSROUT) to TxDO (RxDO) on the rising edge of BCLKX (BCLKR).

BCLKX (BCLKR) frequency can be programmed to be either 64 or 128 (80 or 160) (90 or 192) times Fsx (Fsr) using the Bit Frame Select (BFRS) input pin. This mean that the frame contains four, five, six, eight, ten or twelve time slots of 16 bits. The time slots used for circuit operation are indicated in the next paragraph.

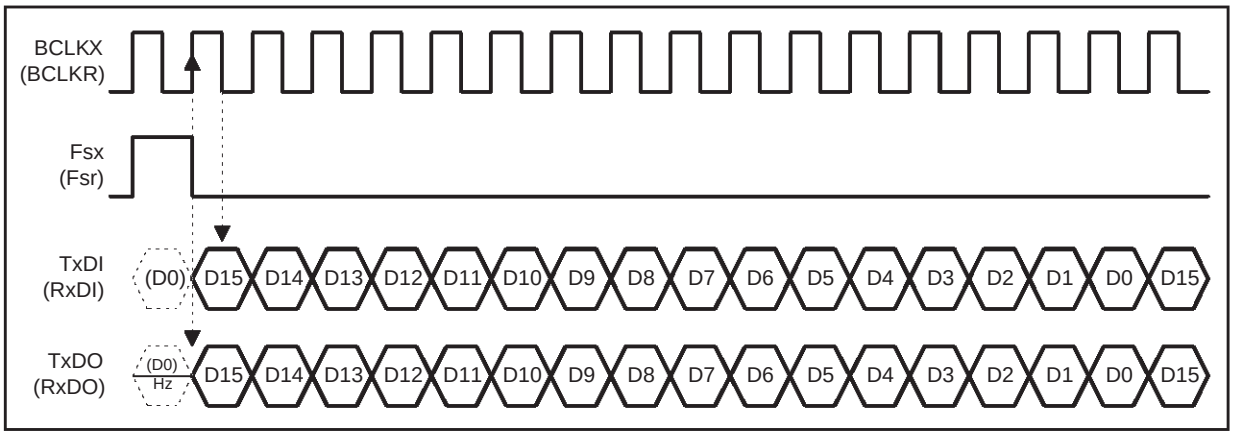
IV.1 - DUAL SERIAL INTERFACE MODE (SSIA, SSIB)

When SSIM is tied to V_{DD}, both A and B ports are functional : port A (SSIA) is dedicated to the Tx channel and port B (SSIB) to the Rx channel. The timing diagram showing the data format is given in Figures 5 and 6.

The time-slot TXO1 is dedicated to RAM coefficient reading. The RAM coefficient is selected by the address bits RA0 to RA1 in the TxCtrl word (see Table 4). Reading is initiated by the rising edge of Start bit Stb (bit D14 in Table 3) in the TxCtrl word.

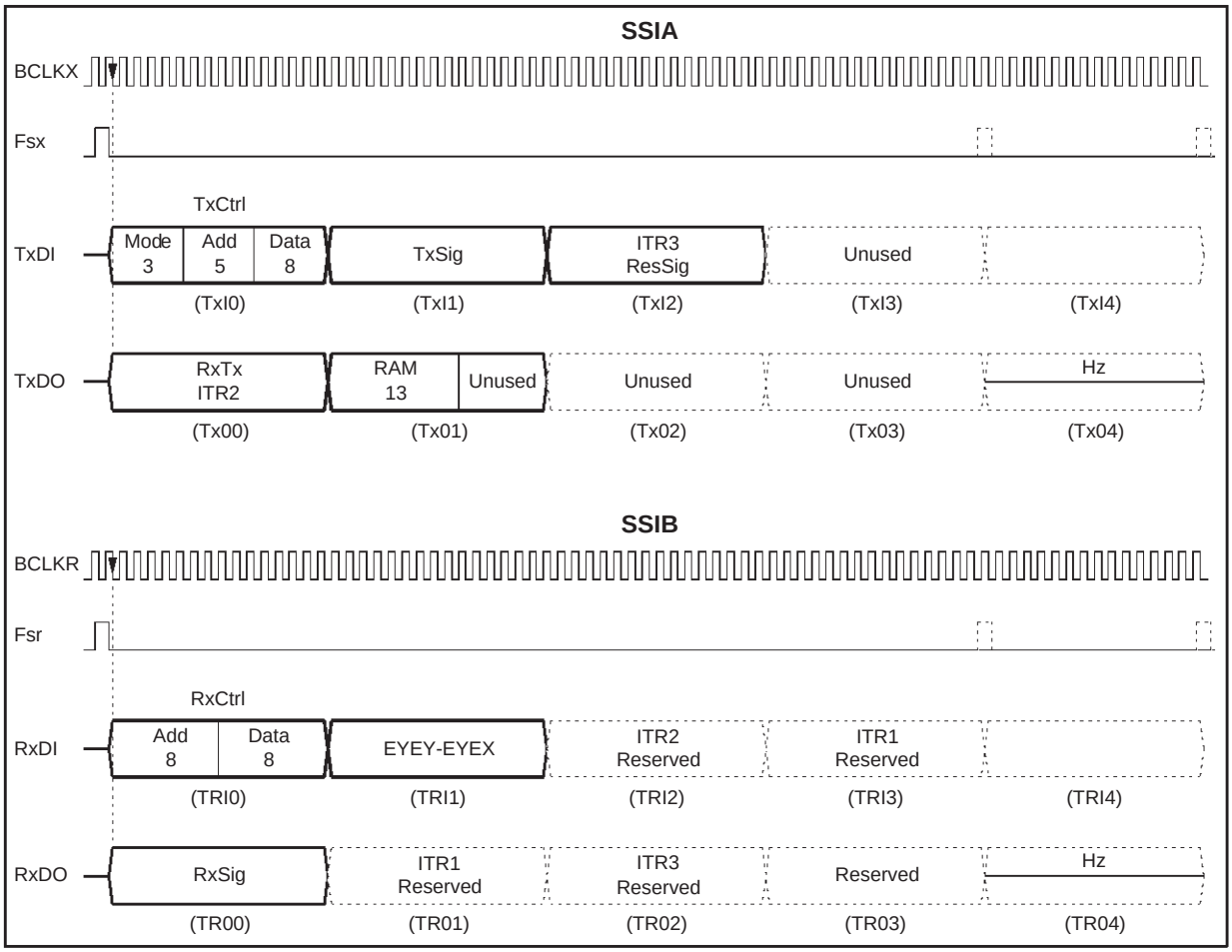
Note : RxSig is also available in two time slot RxS1 and RxS2 on the time slot TxO2 and TxO3 on SSIA (see section IV.2)

Figure 5 : Serial Channel Timing



IV - SERIAL INTERFACE OPERATION (continued)

Figure 6 : Serial Channel Timing. Dual Port Mode



IV.2 - SINGLE SERIAL INTERFACE MODE

When SSIM is tied to GND, only port A (SSIA) is selected. In this case, port A carries both Tx and Rx signal samples and control words at Tx sampling rate (Fsx).
The RxDI input should be tied to V_{DD}. Since port B is not functional in this mode, the RxSig (synchronized to Fsr) will be available in the two time slots, RxS1 and RxS2, synchronized to Fsx.
The reason for the two time slots is that the Fsr could be different in magnitude and phase from the Fsx.
The status bit St0 and St1 are used to indicate which of the RxS1 and RxS2 are valid. Please see the table following. For example, if Fsx = 9600Hz and Fsr = 14400Hz both RxS1 and RxS2 could carry valid data. Figure 7 shows the timing diagram.

The time-slot TXO1 is dedicated to RAM coefficient reading. The RAM coefficient is selected by address bits (RA0 to RA1) in the TxCtrl word (see Table 4). Reading is initiated by the rising edge of a Start bit Stb (bit D14 in Table 3) in the TxCtrl word. The time-slot TxI3 is dedicated to the RxCtrl word or the EYE-PATTERN, selected in the TxCtrl (see Table 5).

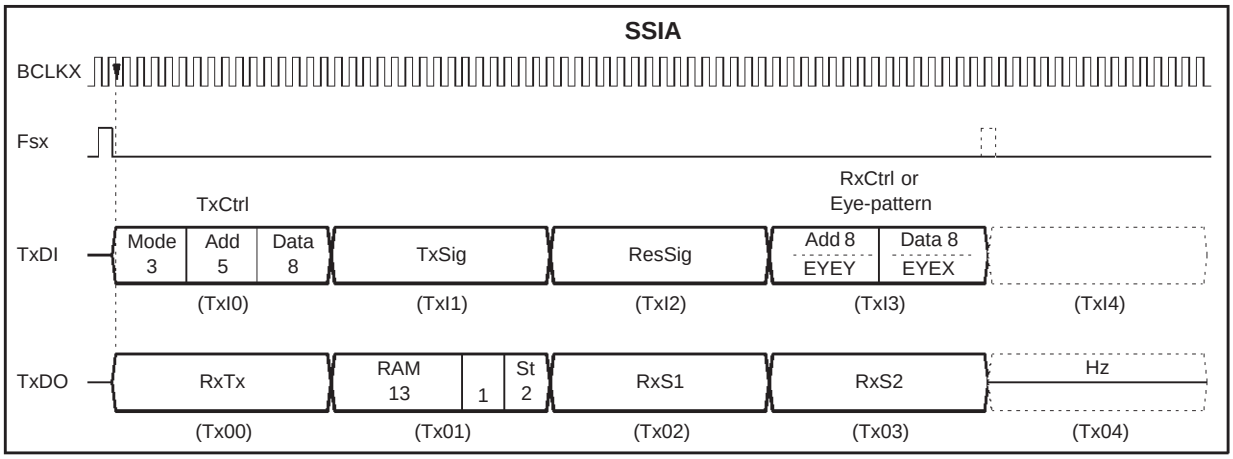
Table 2

STATUS WORD IN TxO1 TIME SLOT		
D1	D0	Valid Data
St1	St0	
0	0	None
0	1	None
1	0	RxS2
1	1	RxS1 and RxS2 (1)

Note 1 : The RxS1 sample precedes the RxS2 sample.

IV - SERIAL INTERFACE OPERATION (continued)

Figure 7 : Serial Channel Timing. Single Port Mode



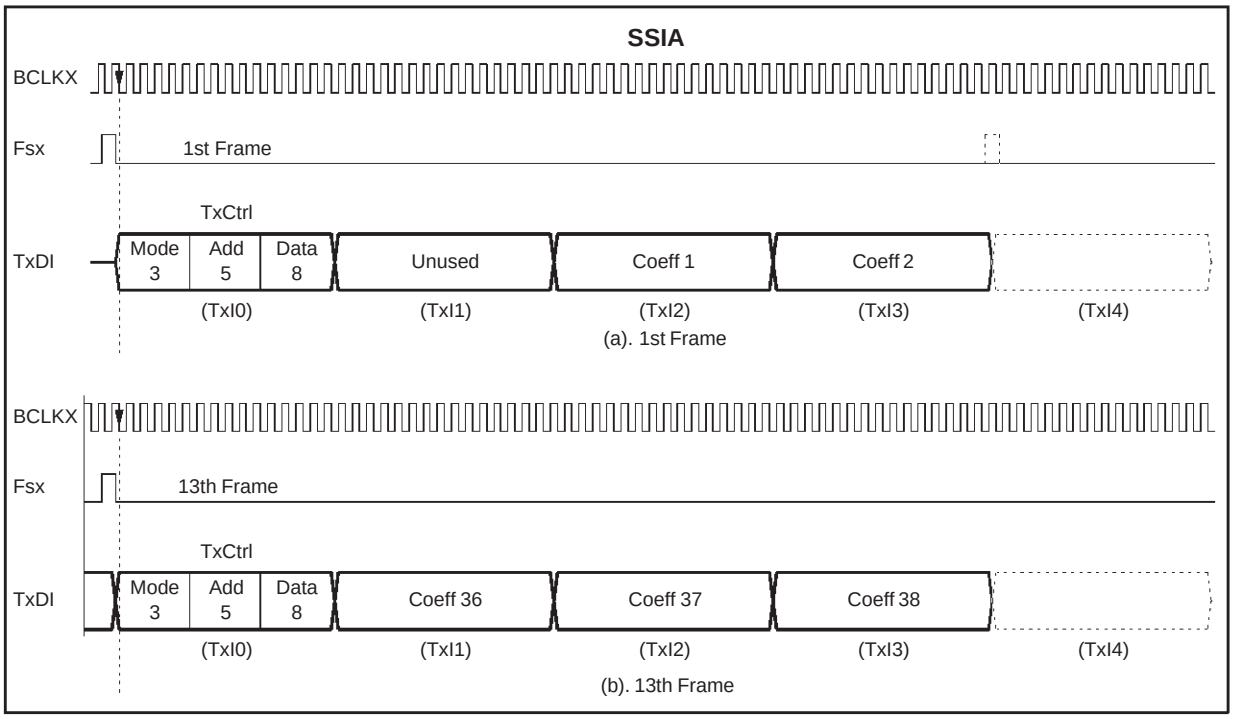
IV.3 - COEFFICIENT LOADING MODE

The Coefficient Loading Mode is selected by the Mode Select bit (MS) in the TxCtrl Word (Table 3). When the MS bit is a logic "1" the loading mode is selected. The IIR RAMS (RAM1 to RAM3) are selected in the TxCtrl word by two address bits (RA0 to RA1). Each coefficient RAM stores 38 coefficients of 13 bits. Therefore the size of the coefficient RAM is 38 x 16 bits. The first frame transfers 2 coefficients and the 12 following frames each transfer 3 coefficients into the selected RAM, as shown in Figure 8. The transfer is initiated by the rising edge of the Start bit coefficient Stb which is loaded into the TxCtrl word. When the coefficient loading mode is selected all data path are fixed to zero.

Notes : 1. Coefficient loading is the same for both dual and single interface modes.

2. In coefficient loading mode , the EYE-PATTERN (time slot TxI3) (and the RxCtrl in a single serial interface) cannot be accessed

Figure 8 : Coefficient Loading Mode



IV - SERIAL INTERFACE OPERATION (continued)

IV.4 - COEFFICIENT READING

Coefficient reading is selected in DATA mode only, i.e. when the Mode Select bit (MS) in the TxCtrl word is tied to logical 0. The IIR RAMS (RAM1 to RAM3) are selected in the TxCtrl word by two address bits (RA0 to RA1). The 38 coefficients of 13 bits are available, one per frame, in the timeslot TxO1 on the output Tx port A (see Figures 6, 7). The reading is available on the rising edge of the Start bit Stb loaded into the TxCtrl word. The first coefficient is output with one frame of delay on TxO1.

IV.5 - CRYSTAL SELECTION (XTAL10, XTAL11)

For application needing different or higher symbol rates, the user can software select different master clock frequencies for the STLC7545. Two XTAL inputs are provided for this purpose. The active XTAL input is selected in the time slot TxI1 with the Quartz Select bit (QS). It is mandatory to shortcircuit the XTAL10 and XTAL11 inputs when a single external crystal or clock generator is used.

IV.6 - FRAME FREQUENCY PROGRAMMING

When using the nominal master clock frequency, the frame frequency can be from 7200Hz to 16000Hz (see Tables 15 and 32). Whenever the frame frequency Fsx (Fsr) is modified, the data to the STLC7545 during that frame should be high in the time slots TxI1 (RxI1), TxI2 (RxI2) and TxI3 (RxI3). This is because the BCLKX (BCLKR) during that frame may not be correct. Therefore, whenever the Fsx (Fsr) is changed the user has to send information to the STLC7545 after one frame delay.

IV.7 - INITIALIZATION AND LOW-POWER RESET MODE

Internal power-on circuitry automatically resets the DPLL, the clock generator counters, and initializes the internal control registers. The clocks affected are the symbol clock, the bit clock and the sampling clock. The initial status of these registers is given in the PROGRAMMABLE FUNCTIONS section. The transmit attenuator is initialized to an infinite attenuation mode (see Table 24) to avoid the transmission of undesirable signals on the phone line.

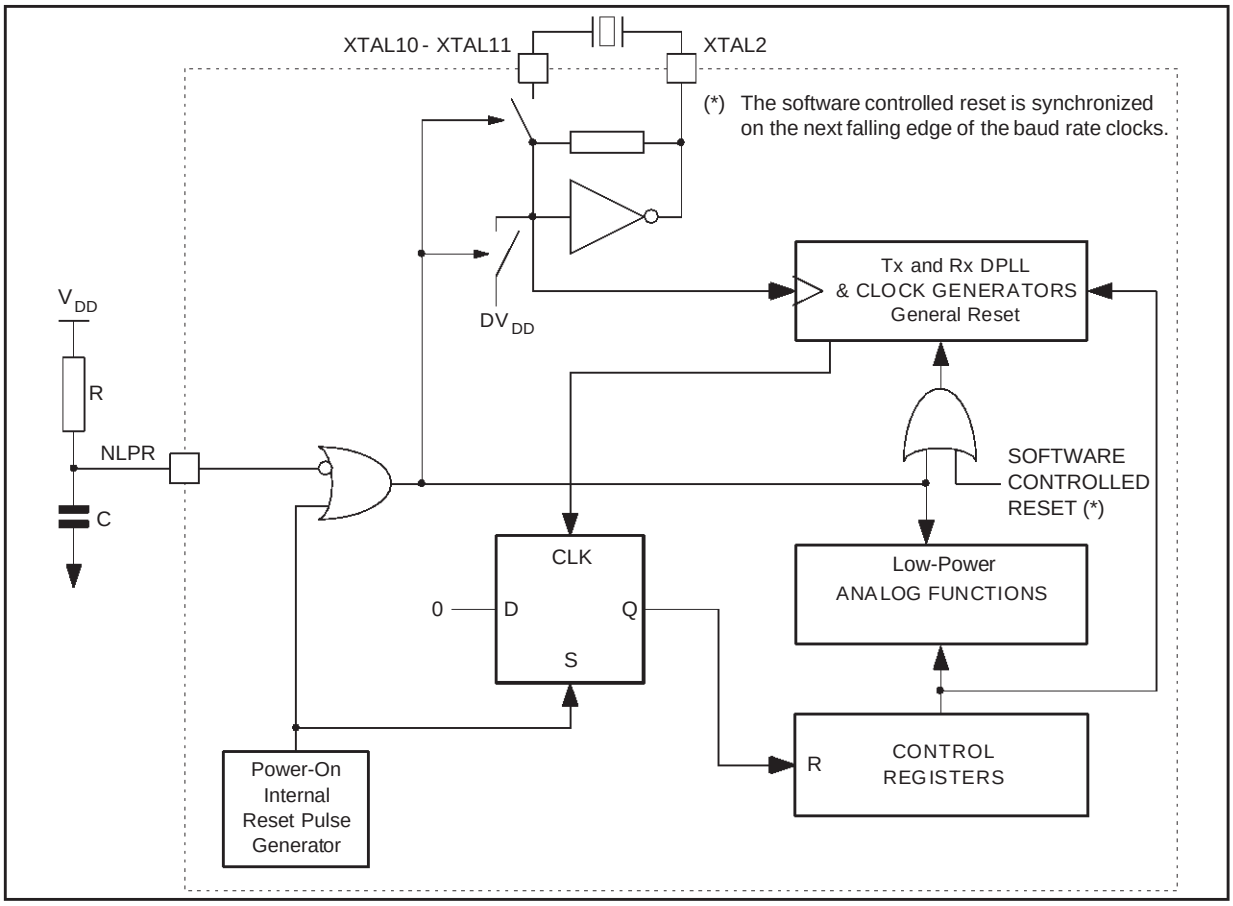
During hardware low power reset (NLPR pin is tied to GND), the input of the inverter (across the crystal) will be high (DV_{DD}), the DPLLs and the clock generator counters are initialized, all the analog circuitry is placed in low-power mode and the XTAL oscillator is stopped.

Access to the circuit is disabled during reset until the clock oscillator starts. The duration of the reset time can be increased by connecting the NLPR input to an external RC timeconstant as indicated in Figure 9.

In normal operation the NLPR input is used to control the LowPower mode. When NLPR is not used, it must be tied to V_{DD}.

IV - SERIAL INTERFACE OPERATION (continued)

Figure 9 : Power-on Initialization Circuitry



V - CIRCUIT PROGRAMMING

This section defines the control and status words required to program the STLC7545.

The circuit configuration is managed by the control words TxCtrl and RxCtrl and the SSIM, BFRS inputs. The control words contain three fields :

- **Mode Field** 3 bits (D15-D13) mode control bit
- **Address Field** 5 bits (D12-D8) 2 bits for Coeff Ram address
  3 bits for Control Registers address
- **Data Field** 8 bits (D7-D0) Control Registers content

V.1 - MODE FIELD

Table 3 : Mode Field

TxCtrl Word			
D15	D14	D13	Select mode
MS	Stb	QS	
0	-	-	Data Mode and Control Register access mode
1	-	-	Coefficient Loading Mode and Filter Data Memory Reset (INI)
-	↑	-	Start bit for Coefficient Loading or Reading. The loading is initiated by a rising edge, i.e. a logical one programmed after a logical zero.
-	-	1	XTAL10 Selected (INI) (CS equals 16 in bit chain clock)
-	-	0	XTAL11 Selected (CS equals 8 in bit chain clock)

INI : initial value

V.2 - ADDRESS FIELD

V.2.1 - RAM Address Field

Table 4 : RAM Address Field

TxCtrl Word								
D15	D14	D13	D12	D11	D10	D9	D8	RAM Address
MS	Stb	QS	RA0	RA1	AD2	AD1	AD0	
-	↑	-	0	0	-	-	-	RAM 1 (INI)
-	↑	-	0	1	-	-	-	RAM 2
-	↑	-	1	0	-	-	-	RAM 3
-	-	-	1	1	-	-	-	Not RAM access

INI : initial value

V.2.2 - Transmit Control Register Address Field

Table 5 : Transmit Control Register Address Field

Register Name	TxCtrl Word (2)							
	D15	D14	D13	D12	D11	D10	D9	D8
	MS	Stb	QS	RA0	RA1	AD2	AD1	AD0
TxCR0 (1)	-	-	-	-	-	0	0	0
TxCR1 (1)	-	-	-	-	-	0	0	1
TxCR2	-	-	-	-	-	0	1	0
TxCR3 (1)	-	-	-	-	-	0	1	1
None	-					1	1	1
EYE Pattern on TxI3						1	1	0 (3)

Notes : 1. A reset is generated when programming these registers (see III.5.2.1).
2. No register access for the non-specified code
3. In single interface mode only

V - CIRCUIT PROGRAMMING (continued)

V.2.3 - Receive Control Register Address Field

Table 6 : Receive Control Register Address Field

Register Name	RxCtrl Word (2, 3)							
	D15	D14	D13	D12	D11	D10	D9	D8
	-	-	-	-	-	AD2	AD1	AD0
RxCR0 (Note 1)	-	-	-	-	-	0	0	0
RxCR1 (Note 1)	-	-	-	-	-	0	0	1
RxCR2	-	-	-	-	-	0	1	0
RxCR3 (Note 1)	-	-	-	-	-	0	1	1
None	-	-	-	-	-	1	1	1

Notes : 1. A reset is generated when programming the RxCR0, RxCR1 and RxCR3 registers, this reset is synchronous with the falling edge of the Rx symbol clock.
2. In single interface mode, the RxCtrl registers cannot be programmed during the coefficient loading mode (see Figures 7 and 8).
3. No register access for the non-specified code

V.3 - CONTROL REGISTER DATA FIELD

V.3.1 - Transmit Control Register Programming

Table 7 : Transmit Control Register Programming

Register	Data								Programmed Function
	D7	D6	D5	D4	D3	D2	D1	D0	
TxCR0	N0	R1	R0	S1	S0	T2	T1	T0	Tx Bit rate clock generator
TxCR1	M0	Q1	Q0	U2	U1	U0	P0	BS	Tx Sampling, Baud and HS clock generators; Band Split configuration.
TxCR2	AT1	AT0	LTX	LC	SST	R3	VF	R2	Tx Attenuator, TxClock Synchronization, V.Fast Synchronization mode, Divider by 12/11 Bit clock
TxCR3	V2	V1	V0	W	HQ1	HQ0	Ts0	DL	Tx Sampling (used with TxCR1), FCOMP and FSHIFT frequency programming HALF-INTEGER Q DIVIDER (used with TxCR1), Test configuration

V.3.2 - Receive Control Register Programming

Table 8 : Receive Control Register Programming

Register	Data								Programmed Function
	D7	D6	D5	D4	D3	D2	D1	D0	
RxCR0	N0	R1	R0	S1	S0	T2	T1	T0	Rx Bit rate clock generator
RxCR1	M0	Q1	Q0	U2	U1	U0	P0	ECK	Rx Sampling, Baud and HS clock generators, Baud and HS clock Enable
RxCR2	LL	PS3	PS2	PS1	PS0	AP2	AP1	AP0	Rx Fine and Coarse Phase, Shift Control
RxCR3	V2	V1	V0	EMX	R2	R3	HQ1	HQ0	Rx Sampling (used with RxCr1), FCOMP or TxRCLK output enable HALF-INTEGER Q DIVIDER (used with RxCR1), Divider by 12/11 and 15/13 Bit clock, Test configuration

V - CIRCUIT PROGRAMMING (continued)

V.3.3 - Control Bit Function Summary

V.3.3.1 - TxCTRL WORD

Table 9 : TxCTRL Word, Programmed Function

Table	Bit	Programmed Function
11,12,13,14	N0	N Divisor rank : 3, 4
"	R3,R2,R1,R0	R Divisor rank : 15/13, 12/11, 10/9, 8/7, 6/5, 4/3, 1 (1)
"	S1,S0	S Divisor rank : 1, 3, 5, 7
"	T2,T1,T0	T Divisor rank : 4, 8, 16, 32, 64, 128, 256, 512
14,15,16,17,18	M0	M Divisor rank : 3, 4
"	Q1,Q0	Q Divisor rank : 5, 6, 7, 8
19	U2,U1,U0	U Divisor rank : 3, 4, 5, 6 ,7, 8, 12, 16
20	P0	P Divisor rank : 3, 4
21	BS	Band Split or Echo cancelling mode. (In band split mode the IIR2 Filter output is internally tied to IIR3 Filter Input)
22	LTX	Synchronization signal : TxSCLK or RxCLK
22	LC	Synchronization enabling : Lock or Free DPLL.
22	SST	TxDPLL reset on the next falling edge of the synchronization signal. SST is automatically reset after its action is completed.
23	VF	7544 and V.34 synchronization mode
23	R2, R3	R Divisor rank
24	AT1,AT0	Tx Attenuation : 0dB, 6dB or infinite
25	V2,V1,V0	V Divisor rank : 128 , 160, 192
25	F	F Divisor rank
24	W	FSHIFT frequency : Fsx or Fsx / 2 (Related to frequency capture range of the TxDPLL as FQ-FSHIFT < FAVERAGE < FQ + FSHIFT)
27	Ts0,HQ1, HQ0	HALF-INTEGER Q DIVIDER (used with TxCR1 Q bit). Test Functions. Must be set to logical 0 for normal operation
27	DL	Test Loop

Note 1 : The R2 and R3 bits are found in the TxCR2 register Table 23

V.3.3.2 - RxCTRL WORD

Table 10 : RxCTRL Word, Programmed Function

Table	Bit	Programmed Function
28,29,30,31	N0	N Divisor rank : 3, 4
"	R3,R2, R1,R0	R Divisor rank : 15/13, 12/11, 10/9, 8/7, 6/5, 4/3, 1 (1)
"	S1,S0	S Divisor rank : 1, 3, 5, 7
"	T2,T1,T0	T Divisor rank : 4, 8, 16, 32, 64, 128, 256, 512
32,33,34,35	M0	M Divisor rank : 3, 4
"	Q1,Q0	Q Divisor rank : 5, 6, 7, 8
36	U2,U1,U0	U Divisor rank : 3, 4, 5, 6 ,7, 8, 12, 16
37	P0	P Divisor rank : 3, 4
37	ECK	Tx/RxRCLK and Tx/RxHSCLK output enabling
38	LL	Rx DPLL Lead/Lag control
38	PS1,PS0	Rx DPLL Phase Shift magnitude : 0, 8, 12, 16, 20, 24, 28, PS2
38	PS3	Rx DPLL Phase Shift magnitude : One 128*Fsx period. This bit is reset after phase shift completion.
39	AP2,AP1	Rx DPLL Coarse Phase Lag : 0, 64, 128, 256 512, 1024, AP0
40	V2,V1,V0	V Divisor rank
41	EMX	FCOMP or TxRCLK output enable (used in V.Fast synchronization mode to multiplex the transmit bit Frame)
41	HQ0,HQ1	Half-integer Q divider (used with RxCR1 Q bit)
41	R3, R2	R Divisor rank

Note 1 : The R2 and R3 bits are found in the RxCR3 register Table 41

VI - PROGRAMMABLE FUNCTIONS

VI.1 - TRANSMIT SECTION

The different transmit (Tx) clocks are obtained by frequency division in several counters (see Figure 10).

Note 1 : TxPCLK is an internal Processing Clock used by the three IIR filters

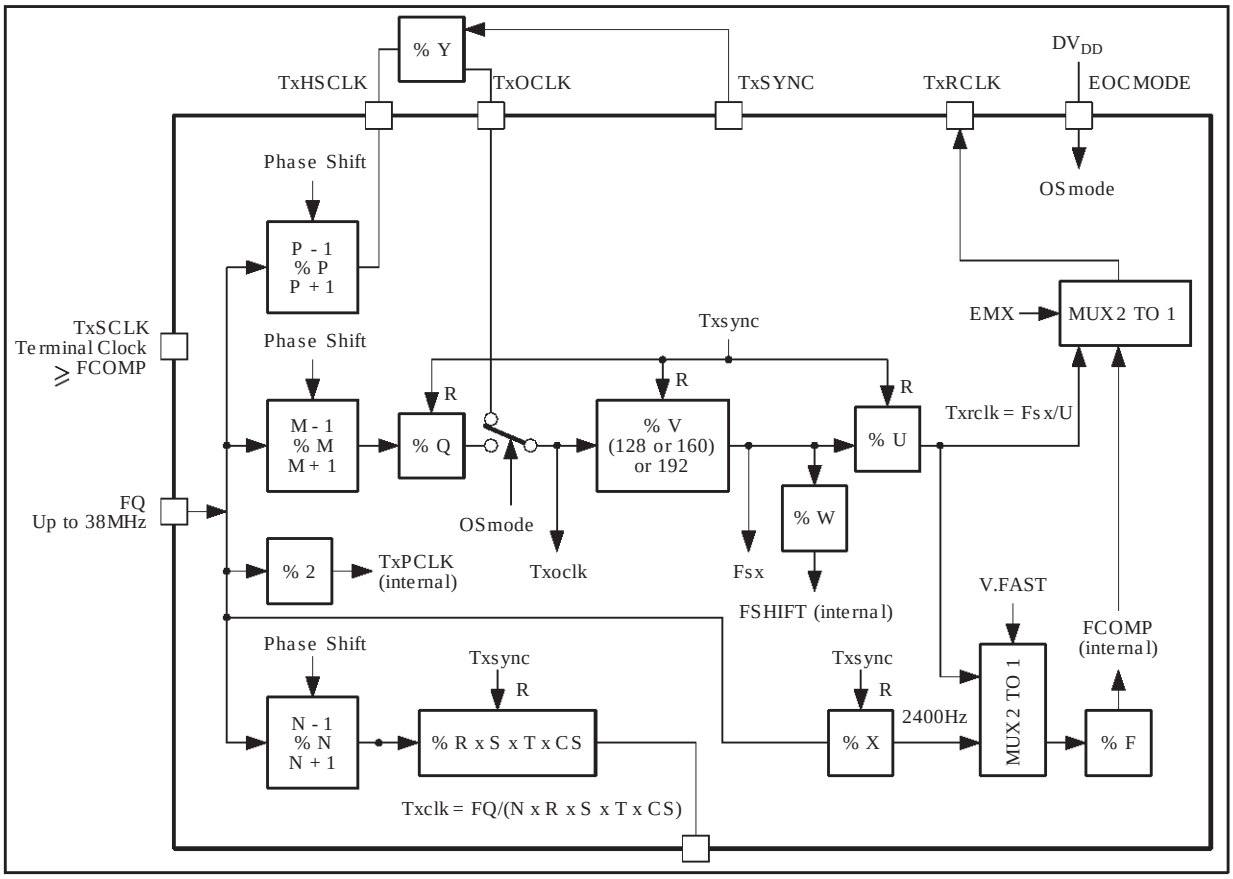
Note 2 : The phase of internal clock FCOMP will be compared to the synchronization signal (Table 22) in order to control TxDPLL (see Tables 22, 25 and 26). In V.34 synchronization mode FCOMP is automatically set to 2400/F Hz if the crystal frequency is equal to 36.864MHz (with QS = 1) or 25.8048MHz (with QS = 0) and if the bit rate clock is multiple of 2400Hz chosen from the Table. In 7544 mode V divisor must be chosen such that the FCOMP frequency is an integral sub-multiple of the synchronization frequency. In the 7544 mode the most typical frequency for FCOMP is the baud rate frequency.
During each period of FCOMP the average input frequency of the transmit clock generator can be :

FQ , FQ + FSHIFT or FQ - FSHIFT
with FSHIFT = Fsx or Fsx/2

Note 3 : In 7544 mode the bit rate frequency must always be an integer multiple of the baud rate frequency for the transmit DPLL to lock onto the synchronization signal.

Note 4 : The X divisor is programed automatically with respect to QS bit.

Figure 10 : Transmit Clock Generator



VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.1 - Transmit Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Table 11 : Transmit Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

TxCRO Register											Bit Rate Clock Frequency(Hz)
TxCR2 D2	TxCR2 D0	D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(FQ = 36.864MHz) Txclk = FQ/(N*R*S*T*CS) (1)
R3	R2	N0	R1	R0	S1	S0	T2	T1	T0		
0	0	0	1	1	1	0	0	0	0	960	38400
0	0	1	1	1	0	0	0	1	0	1024	36000
0	0	0	0	0	1	0	0	0	0	960x8/7	33600
0	0	0	1	1	0	1	0	0	1	1152	32000
1	1	1	0	0	0	0	0	1	0	1024x15/13	31200
0	0	1	1	1	1	0	0	0	0	1280	28800
0	1	1	0	0	1	0	0	0	0	1280x12/11	26400
0	0	1	1	1	0	1	0	0	1	1536	24000
0	0	1	1	0	1	0	0	0	0	1280x4/3	21600
0	0	0	1	1	1	0	0	0	1	1920	19200 (INI)
0	0	0	0	0	1	0	0	0	1	1920x8/7	16800
0	0	0	1	1	0	1	0	1	0	2304	16000
0	0	1	1	1	1	0	0	0	1	2560	14400
0	0	1	1	1	0	1	0	1	0	3072	12000
0	0	0	1	1	1	0	0	1	0	3840	9600
0	0	0	1	1	0	1	0	1	1	4608	8000
0	0	1	1	1	1	0	0	1	0	5120	7200
0	0	0	1	1	1	0	0	1	1	7680	4800
0	0	0	1	1	1	0	1	0	0	15360	2400
0	0	0	1	1	1	0	1	0	1	30720	1200
0	0	0	1	1	1	0	1	1	0	61440	600
0	0	0	1	1	1	0	1	1	1	122880	300

Note : 1. The QS bit in TxCTRL word (bit D3) must be set to 1 to have CS = 16.

VI.1.2 - Transmit Bit Rate Clock Frequency Programming with Master clock Frequency FQ=25.8048MHz

Table 12 : Transmit Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

TxCRO Register										Bit Rate Clock Frequency (Hz)
TxCR2 D0	D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(FQ = 25.8048MHz) Txclk = FQ/(N*R*S*T*CS) (2)
R2	N0	R1	R0	S1	S0	T2	T1	T0		
0	1	1	1	1	1	0	0	0	896	28800
1	1	0	0	1	1	0	0	0	896x12/11	26400
0	1	0	1	1	1	0	0	0	896x6/5	24000
0	1	1	0	1	1	0	0	0	896x4/3	21600
0	0	1	1	1	1	0	0	1	1344	19200
0	0	0	0	1	1	0	0	1	1344x8/7	16800
0	0	0	1	1	1	0	0	1	1344x6/5	16000
0	1	1	1	1	1	0	0	1	1792	14400
0	1	0	1	1	1	0	0	1	1792x6/5	12000
0	0	1	1	1	1	0	1	0	2688	9600
0	0	0	1	1	1	0	1	0	2688x6/5	8000
0	1	1	1	1	1	0	1	0	3584	7200
0	0	1	1	1	1	0	1	1	5376	4800
0	0	1	1	1	1	1	0	0	10752	2400
0	0	1	1	1	1	1	0	1	21504	1200
0	0	1	1	1	1	1	1	0	43008	600
0	0	1	1	1	1	1	1	1	86016	300

Note : 2. The QS bit in TxCTRL word (bit D3) must be set to 0 to have CS = 8.

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.3 - Transmit Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Table 13 : Transmit Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

TxCRO Register									Bit Rate Clock Frequency (Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	Txclk= FQ/(N*R*S*T*CS) (1)
N0	R1	R0	S1	S0	T2	T1	T0		
0	1	1	0	1	0	0	0	576	32000
1	1	1	0	1	0	0	0	768	24000
0	1	1	1	0	0	0	0	960	19200
0	0	0	1	0	0	0	0	960x8/7	16800
0	1	1	0	1	0	0	1	1152	16000
1	1	1	1	0	0	0	0	1280	14400
1	1	1	0	1	0	0	1	1536	12000
0	1	1	1	0	0	0	1	1920	9600 (INI)
0	1	1	0	1	0	1	0	2304	8000
1	1	1	1	0	0	0	1	2560	7200
0	1	1	1	0	0	1	0	3840	4800
0	1	1	1	0	0	1	1	7680	2400
0	1	1	1	0	1	0	0	15360	1200
0	1	1	1	0	1	0	1	30720	600
0	1	1	1	0	1	1	0	61440	300

INI : initial value

Notes : 1. The bit R2 and R3 in the TxCR2 register (bit D0 and D2) must be set to 0.
The QS bit in TxCTRL word must be set to 1 to have CS = 16.

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.4 - Transmit Bit Clock Frequency Programming. Divisor Rank

Table 14 : Transmit Bit Clock Frequency Programming. Divisor Rank

TxCR0 Register										Bit Rate Clock Frequency(Hz) Txclk = FQ/(N*R*S*T*CS) (1)			
TxCR2 D2	TxCR2 D0	D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank			
R3	R2	N0	R1	R0	S1	S0	T2	T1	T0	N	R	S	T
-	-	0	-	-	-	-	-	-	-	3(INI)			
-	-	1	-	-	-	-	-	-	-	4			
0	0	-	0	0	-	-	-	-	-		8/7		
0	0	-	0	1	-	-	-	-	-		6/5		
0	0	-	1	0	-	-	-	-	-		4/3		
0	0	-	1	1	-	-	-	-	-		1 (INI)		
0	1	-	0	0	-	-	-	-	-		12/11		
0	1	-	0	1	-	-	-	-	-		10/9		
0	1	-	1	0	-	-	-	-	-		8/7		
0	1	-	1	1	-	-	-	-	-		1		
-	-	-	-	-	0	0	-	-	-			1	
-	-	-	-	-	0	1	-	-	-			3	
-	-	-	-	-	1	0	-	-	-			5 (INI)	
-	-	-	-	-	1	1	-	-	-			7	
-	-	-	-	-	-	-	0	0	0				4
-	-	-	-	-	-	-	0	0	1				8 (INI)
-	-	-	-	-	-	-	0	1	0				16
-	-	-	-	-	-	-	0	1	1				32
-	-	-	-	-	-	-	1	0	0				64
-	-	-	-	-	-	-	1	0	1				128
-	-	-	-	-	-	-	1	1	0				256
-	-	-	-	-	-	-	1	1	1				512
1	0	-	0	0	-	-	-	-	-		11/9		
1	0	-	0	1	-	-	-	-	-		9/7		
1	0	-	1	0	-	-	-	-	-		7/5		
1	0	-	1	1	-	-	-	-	-		1		
1	1	-	0	0	-	-	-	-	-		15/13		
1	1	-	0	1	-	-	-	-	-		13/11		
1	1	-	1	0	-	-	-	-	-		11/9		
1	1	-	1	1	-	-	-	-	-		1 (INI)		

INI : initial value
Note 1 : The CS divisor is set by QS bit in TxCTRL word (QS = 1 → CS = 16, QS = 0 → CS = 8)

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.5 - Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Table 15 : Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Symbol rate (baud)	U	M x (Y or Q) ratio	Sampling Frequency(Hz)	V Over-sampling ratio	W	Capture range
600	12	4 x 8	7200	160	1	1.95E-4
600	16	4 x 6	9600	160	1	2.60E-4
1200	6	4 x 8	7200	160	1	1.95E-4
1200	8	4 x 6	9600	160	1	2.60E-4
1600	5	4 x 6	8000	192	1	2.17E-4
1600	6	4 x 6	9600	160	1	2.60E-4
2400	3	4 x 8	7200	160	1	1.95E-4
2400	4	4 x 6	9600	160	1	2.60E-4
2400	6	4 x 5	14400 (INI)	128	2	1.95E-4
2560	3	4 x 7.5	7680	160	1	2.08E-4
2560	4	3 x 7.5	10240.00	160	1	2.77E-4
2560	6	3 x 5	15360.00	160	2	2.98E-4
2742.86	3	4 x 7	8228.57	160	1	2.40E-4
2742.86	4	3 x 7	10971.43	160	1	2.98E-4
2953.85	3	4 x 6.5	8861.54	160	1	2.40E-4
2953.85	4	3 x 6.5	11815.38	160	1	3.21E-4
3000	3	4 x 8	9000	128	1	2.44E-4
3000	4	3 x 8	12000	128	1	3.26E-4
3200	3	4 x 6	9600	160	1	2.60E-4
3200	4	3 x 6	12800	160	1	3.48E-4
3200	5	3 x 6	16000	128	1	4.34E-4
3428.57	3	4 x 7	10285.71	128	1	2.79E-4
3428.57	4	3 x 7	13714.28	128	2	1.86E-4
3490.91	3	4 x 5.5	10472.73	160	1	2.84E-4
3490.91	4	3 x 5.5	13963.64	160	1	3.79E-4

INI : initial value

VI.1.6 - Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

Table 16 : Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

Symbol rate (baud)	U	M x Qratio	Sampling Frequency(Hz)	V Over-sampling ratio	W	Capture range
2800	3	4 x 6	8400	128	1	3.26E-4
2800	4	3 x 6	11200	128	2	2.17E-4
2400	3	4 x 7	7200	128	1	2.79E-4
2400	4	3 x 7	9600	128	2	1.86E-4

VI.1.7 - Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Table 17 : Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Symbol Rate (baud)	U	M x Q ratio	Sampling Frequency (Hz)	V Over-sampling ratio	W	Capture range
1600	5	3 x 6	8000	128	2	2.17E-4
1600	6	3 x 5	9600	128	2	2.60E-4
2400 (INI)	3	4 x 5	7200	128	2	1.95E-4
2400	4	3 x 5	9600	128	2	2.60E-4

INI : initial value

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.8. Transmit Sampling Clock Frequency Programming. Divisor Rank

Table 18 : Transmit Sampling Clock Frequency Programming. Divisor Rank

TxCR1 Register								Sampling Clock frequency Fsx = FQ/(MxQxV) (1)	
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	
M0	Q1	Q0	U2	U1	U0	P0	BS	M	Q (2)
0	-	-	-	-	-	-	-	3	
1	-	-	-	-	-	-	-	4 (INI)	
-	0	0	-	-	-	-	-		5 (INI) (4.5)
-	0	1	-	-	-	-	-		6 (5.5)
-	1	0	-	-	-	-	-		7 (6.5)
-	1	1	-	-	-	-	-		8 (7.5)

INI : initial value

Notes : 1. The V divider is programmed in the TxCR3 register.
2. To use the fractional Q divider bits HQ1 and HQ0 in Table 27 must be set to "1" (otherwise they are set to "0").

VI.1.9. Transmit Baud Rate Frequency Programming. Divisor Rank

Table 19 : Transmit Baud Rate Frequency Programming. Divisor Rank

TxCR1 Register								Baud rate Frequency Txrclk = Fsx / U
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank
M0	Q1	Q0	U2	U1	U0	P0	BS	U
-	-	-	0	0	0	-	-	3 (INI)
-	-	-	0	0	1	-		4
-	-	-	0	1	0	-	-	5
-	-	-	0	1	1	-	-	6
-	-	-	1	0	0	-	-	8
-	-	-	1	0	1	-	-	12
-	-	-	1	1	0	-	-	16
-	-	-	1	1	1	-	-	16

INI : initial value

VI.1.10. Highest Synchronous Transmit Frequency Programming. Divisor Rank

Table 20 : Highest Synchronous Transmit Frequency Programming. Divisor Rank

TxCR1 Register								Highest Synchronous Transmit Frequency Txhsclk=FQ/P
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank
M0	Q1	Q0	U2	U1	U0	P0	BS	P
-	-	-	-	-	-	0	-	3 (INI)
-	-	-	-	-	-	1		4

INI : initial value

VI.1.11. Band Split Mode

Table 21 : Band Split Mode

TxCR1 Register								Band Split Mode
D7	D6	D5	D4	D3	D2	D1	D0	
M0	Q1	Q0	U2	U1	U0	P0	BS	
-	-	-	-	-	-	-	0	Inactive (INI)
-	-	-	-	-	-	-	1	Active : Rx Filter Output connected to reconstruction filter input (see Figure 1).

INI : initial value

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.12 - Transmit Synchronization Signal Programming

Table 22 : Transmit Synchronization Signal Programming

TxCR2 Register								Tx DPLL Clock
D7	D6	D5	D4	D3	D2	D1	D0	Synchronization
AT1	AT0	LTX	LC	SST	R3	VF	R2	
-	-	0	1	-	-	-	-	TxSCLK (1)
-	-	1	1	-	-	-	-	RxCLK (1)
-	-	-	1	1	-	-	-	Reset on the Next falling edge of the Synchronization Signal (1) (2)
-	-	-	0	-	-	-	-	No Synchronization (INI)

INI : initial value

Notes : 1. If D4 = 1, the TxDPLL will be locked to the synchronization signal if present when programming is done. Otherwise, the Tx DPLL will be free-running.
2. The SST bit is automatically reset after its action is completed.

VI.1.13 - Clock Mode Programming & R2 & R3 Divisor

Table 23 : Clock Mode Programming & R2 & R3 Divisor

TxCR2 Register								Mode Programming & R2 & R3 Divisor
D7	D6	D5	D4	D3	D2	D1	D0	
AT1	AT0	LTX	LC	SST	R3	VF	R2	
-	-	-	-	-	-	0	-	7544 synchronization Mode (INI)
-	-	-	-	-	-	1	-	V.34 synchronization Mode
-	-	-	-	-	-	-	R2	see Table 14 - R2 = 0 (INI)
-	-	-	-	-	R3	-	-	see Table 14 - R3 = 0 (INI)

INI : initial value

VI.1.14 - Transmit Attenuator Programming

Table 24 : Transmit Attenuator Programming

TxCR2 Register								Transmit Attenuator
D7	D6	D5	D4	D3	D2	D1	D0	Attenuation (dB)
AT1	AT0	LTX	LC	SST	R3	VF	R2	
0	0	-	-	-	-	-	-	Infinite (INI)
1	0	-	-	-	-	-	-	-6
1	1	-	-	-	-	-	-	0

INI : initial value

VI.1.15 - Phase Comparator Frequency and Decimation & Interpolation Ratio

Table 25 : Phase Comparator Frequency And Decimation & Interpolation Ratio

TxCR3 Register								Tx Phase Comparator Frequency FCOMP = Txrclk / F or 2400 / F (2) and V Divisor rank	
D7	D6	D5	D4	D3	D2	D1	D0	FCOMP	Oversampling ratio
V2	V1	V0	W	HQ1	HQ0	Ts0	DL	F	V
0	0	0	-	-	-	-	-	1	128
0	0	1	-	-	-	-	-	2	128
0	1	0	-	-	-	-	-	1	160
0	1	1	-	-	-	-	-	2	160
1	0	0	-	-	-	-	-	4	128 (INI)
1	0	1	-	-	-	-	-	1	192
1	1	0	-	-	-	-	-	4	160
1	1	1	-	-	-	-	-	1	256 (1)

INI : initial value

Notes : 1. The performance is not guaranteed with this oversampling ratio.
2. FCOMP is depending of the synchronization mode (normal or V.34).

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.16 - Phase Shift Frequency

Table 26 : Phase Shift Frequency

TxCR3 Register								Phase Shift Frequency (1) FSHIFT = Fsx / W
D7	D6	D5	D4	D3	D2	D1	D0	(Average updated master clock frequency)
V2	V1	V0	W	HQ1	HQ0	Ts0	DL	W
-	-	-	0	-	-	-	-	Fsx/2 (INI) (FQ ± Fsx/2)
-	-	-	1	-	-	-	-	Fsx (FQ ± Fsx)

INI : initial value

Note 1 : The W bit selects the phase shift frequency of the TxDPLL, and hence the capture range

VI.1.17 - Transmit Test Programming

Table 27 : Transmit Test Programming

TxCR3 Register								Test Modes
D7	D6	D5	D4	D3	D2	D1	D0	
V2	V1	V0	W	HQ1	HQ0	Ts0	DL	
				0	0	0	0	Normal Mode (INI)
-	-	-	-	-	-	-	1	Digital Loop Test (1)
-	-	-	-	-	-	1	-	Test 0 (Internal use only)
-	-	-	-	0	1	-	-	Test 1 (Internal use only)
-	-	-	-	1	0	-	-	Test 2 (Internal use only)
-	-	-	-	1	1	-	-	HALF-INTEGER Q DIVIDER (see Table 18) (2)

INI : initial value

Notes : 1. To perform the digital loop test, the single serial interface and band split modes should be selected, the signal at TxD0 pin should be connected to the RxDI pin, and the Fsx should be equal to the Fsr. Under these conditions, the A/DC input will appear at the output on the D/AC. This test is useful to verify the performance of the ADC, DAC and IIR filters.

2. Test pin EOCMODE must be set to "0" in this configuration.

VI - PROGRAMMABLE FUNCTIONS (continued)

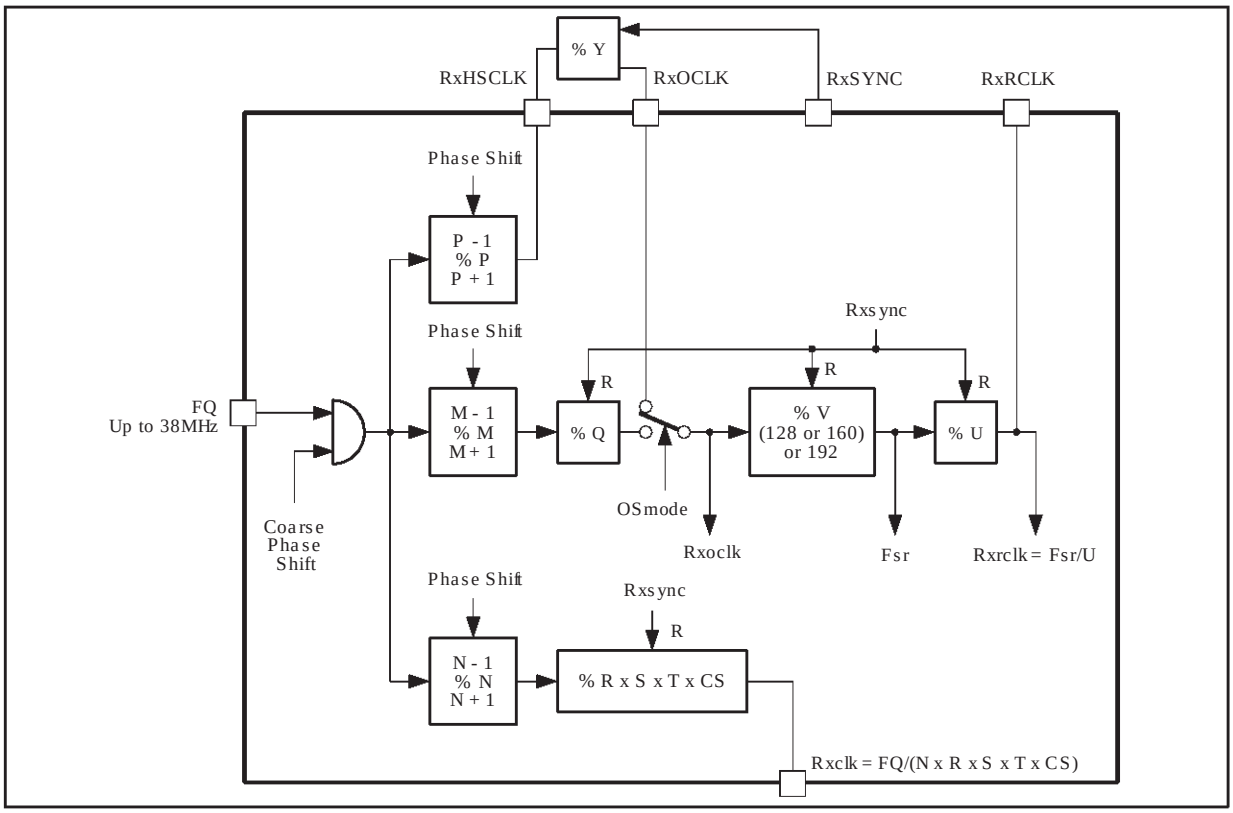
VI.2 - RECEIVE SECTION

The different Receive (Rx) clocks are derived from the master clock (FQ) using the dividers shown in Figure 11.

The counters of the Rx clock system (without the RxHSCLK) are reset when powering on the STLC7545 and when the NLPR input level is low.

They can also be reset, under software control, on the next falling edge of the RxRCLK receive baud rate clock when the RxCR0, RxCR1 or RxCR3 register are accessed : this feature is used to fix the phase of the bit rate clock with respect to the baud rate clock, e.g. after each modification of the bit or baud rate value.

Figure 11 : Receive Clock Generator



VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.1 - Receive Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Table 28 : Receive Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

RxCRO Register											Bit Rate Clock Frequency(Hz)
RxCR3 D2	RxCR3 D3	D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(FQ = 36.864MHz) Rxclk = FQ/(N*R*S*T*CS) (1)
R3	R2	N0	R1	R0	S1	S0	T2	T1	T0		
0	0	0	1	1	1	0	0	0	0	960	38400
0	0	1	1	1	0	0	0	1	0	1024	3600
0	0	0	0	0	1	0	0	0	0	960x8/7	33600
0	0	0	1	1	0	1	0	0	1	1152	32000
1	1	1	0	0	0	0	0	1	0	1024x15/13	31200
0	0	1	1	1	1	0	0	0	0	1280	28800
0	1	1	0	0	1	0	0	0	0	1280x12/11	26400
0	0	1	1	1	0	1	0	0	1	1536	24000
0	0	1	1	0	1	0	0	0	0	1280x4/3	21600
0	0	0	1	1	1	0	0	0	1	1920	19200 (INI)
0	0	0	0	0	1	0	0	0	1	1920x8/7	16800
0	0	0	1	1	0	1	0	1	0	2304	16000
0	0	1	1	1	1	0	0	0	1	2560	14400
0	0	1	1	1	0	1	0	1	0	3072	12000
0	0	0	1	1	1	0	0	1	0	3840	9600
0	0	0	1	1	0	1	0	1	1	4608	8000
0	0	1	1	1	1	0	0	1	0	5120	7200
0	0	0	1	1	1	0	0	1	1	7680	4800
0	0	0	1	1	1	0	1	0	0	15360	2400
0	0	0	1	1	1	0	1	0	1	30720	1200
0	0	0	1	1	1	0	1	1	0	61440	600
0	0	0	1	1	1	0	1	1	1	122880	300

INI : initial value
Note 1 : The QS bit (D13) in TxCTRL word must be set 1 to have CS = 16.

VI.2.2 - Receive Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

Table 29 : Receive Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

RxCRO Register										Bit Rate Clock Frequency (Hz)
RxCR3 D3	D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(FQ = 25.8048MHz) Rxclk = FQ/(N*R*S*T*CS) (1)
R2	N0	R1	R0	S1	S0	T2	T1	T0		
0	1	1	1	1	1	0	0	0	896	28800
1	1	0	0	1	1	0	0	0	896x12/11	26400
0	1	0	1	1	1	0	0	0	896x6/5	24000
0	1	1	0	1	1	0	0	0	896x4/3	21600
0	0	1	1	1	1	0	0	1	1344	19200
0	0	0	0	1	1	0	0	1	1344x8/7	16800
0	0	0	1	1	1	0	0	1	1344x6/5	16000
0	1	1	1	1	1	0	0	1	1792	14400
0	1	0	1	1	1	0	0	1	1792x6/5	12000
0	0	1	1	1	1	0	1	0	2688	9600
0	0	0	1	1	1	0	1	0	2688x6/5	8000
0	1	1	1	1	1	0	1	0	3584	7200
0	0	1	1	1	1	0	1	1	5376	4800
0	0	1	1	1	1	1	0	0	10752	2400
0	0	1	1	1	1	1	0	1	21504	1200
0	0	1	1	1	1	1	1	0	43008	600
0	0	1	1	1	1	1	1	1	86016	300

Note : 1. The QS bit (D13) in TxCTRL word must be set 0 to have CS = 8.

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.3 - Receive Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Table 30 : Receive Bit Rate Clock Frequency Programming With Master Clock Frequency FQ=18.432MHz

RxCRO Register									Bit Rate Clock Frequency (Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(FQ = 18.432MHz) Rxclk = FQ/(N*R*S*T*CS) (1)
N0	R1	R0	S1	S0	T2	T1	T0		
0	1	1	0	1	0	0	0	576	32000
1	1	1	0	1	0	0	0	768	24000
0	1	1	1	0	0	0	0	960	19200
0	0	0	1	0	0	0	0	960*8/7	16800
0	1	1	0	1	0	0	1	1152	16000
1	1	1	1	0	0	0	0	1280	14400
1	1	1	0	1	0	0	1	1536	12000
0	1	1	1	0	0	0	1	1920	9600 (INI)
0	1	1	0	1	0	1	0	2304	8000
1	1	1	1	0	0	0	1	2560	7200
0	1	1	1	0	0	1	0	3840	4800
0	1	1	1	0	0	1	1	7680	2400
0	1	1	1	0	1	0	0	15360	1200
0	1	1	1	0	1	0	1	30720	600
0	1	1	1	0	1	1	0	61440	300

INI : initial value

Notes : 1. The QS bit (D13) in TxCTRL word must be set 1 to have CS = 8.
The bit R2 in the TxCR2 register (bit D0) must be set to 0.

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.4 - Receive Bit Rate Clock Frequency Programming. Divisor Rank

Table 31 : Receive Bit Rate Clock Frequency Programming. Divisor Rank

RxCR0 Register										Bit Rate Clock Frequency(Hz) Rxclk = FQ/(N*R*S*T*CS) (1)			
RxCR3 D2	RxCR3 D0	D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank			
R3	R2	N0	R1	R0	S1	S0	T2	T1	T0	N	R	S	T
-	-	0	-	-	-	-	-	-	-	3(INI)			
-	-	1	-	-	-	-	-	-	-	4			
0	0	-	0	0	-	-	-	-	-		8/7		
0	0	-	0	1	-	-	-	-	-		6/5		
0	0	-	1	0	-	-	-	-	-		4/3		
0	0	-	1	1	-	-	-	-	-		1 (INI)		
0	1	-	0	0	-	-	-	-	-		12/11		
0	1	-	0	1	-	-	-	-	-		10/9		
0	1	-	1	0	-	-	-	-	-		8/7		
0	1	-	1	1	-	-	-	-	-		1		
-	-	-	-	-	0	0	-	-	-			1	
-	-	-	-	-	0	1	-	-	-			3	
-	-	-	-	-	1	0	-	-	-			5 (INI)	
-	-	-	-	-	1	1	-	-	-			7	
-	-	-	-	-	-	-	0	0	0				4
-	-	-	-	-	-	-	0	0	1				8 (INI)
-	-	-	-	-	-	-	0	1	0				16
-	-	-	-	-	-	-	0	1	1				32
-	-	-	-	-	-	-	1	0	0				64
-	-	-	-	-	-	-	1	0	1				128
-	-	-	-	-	-	-	1	1	0				256
-	-	-	-	-	-	-	1	1	1				512
1	0	-	0	0	-	-	-	-	-		11/9		
1	0	-	0	1	-	-	-	-	-		9/7		
1	0	-	1	0	-	-	-	-	-		7/5		
1	0	-	1	1	-	-	-	-	-		1		
1	1	-	0	0	-	-	-	-	-		15/13		
1	1	-	0	1	-	-	-	-	-		13/11		
1	1	-	1	0	-	-	-	-	-		11/9		
1	1	-	1	1	-	-	-	-	-		1 (INI)		

INI : initial value

Note 1 : The CS divisor is set by QSbit (D13) in TxCTRL word (QS = 1 → CS = 16, QS = 0 → CS = 8)

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.5 - Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Table 32 : Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Symbol Rate (baud)	U	M x Y or M x Q ratio	Sampling Frequency (Hz)	V OverSampling ratio
600	12	4 x 8	7200	160
600	16	4 x 6	9600	160
1200	6	4 x 8	7200	160
1200	8	4 x 6	9600	160
1600	5	4 x 6	8000	160
1600	6	4 x 6	9600	192
2400	3	4 x 8	7200	160
2400	4	4 x 6	9600	160
2400	6	4 x 5	14400 (INI)	128
2560	3	4 x 7.5	7680	160
2560	4	3 x 7.5	10240.00	160
2560	6	3 x 5	15360.00	160
2742.86	3	4 x 7	8228.57	160
2742.86	4	3 x 7	10971.43	160
2953.85	3	4 x 6.5	8861.54	160
2953.85	4	3 x 6.5	11815.38	160
3000	3	4 x 8	9000	128
3000	4	3 x 8	12000	128
3200	3	4 x 6	9600	160
3200	4	3 x 6	12800	160
3200	5	3 x 6	16000	128
3428.57	3	4 x 7	10285.71	128
3428.57	4	3 x 7	13714.28	128
3490.91	3	4 x 5.5	10472.73	160
3490.91	4	3 x 5.5	13963.64	160

INI : initial value

VI.2.6 - Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

Table 33 : Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

Symbol Rate (baud)	U	Mx(Y or Q)	Sampling ratio	V OverSampling Frequency (Hz)
2800	3	4 x 6	8400	128
2800	4	3 x 6	11200	128
2400	3	4 x 7	7200	128
2400	4	3 x 7	9600	128

VI.2.7 - Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Table 34 : Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Symbol Rate (baud)	U	M x Q	Sampling ratio	V OverSampling Frequency (Hz)
1600	5	3 x 6	8000	128
1600	6	3 x 5	9600	128
2400 (INI)	3	4 x 5	7200	128
2400	4	3 x 5	9600	128

INI : initial value

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.8 - Receive Sampling Clock Frequency Programming. Divisor Rank

Table 35 : Receive Sampling Clock Frequency Programming. Divisor Rank

RxCR1 Register								Sampling Clock frequency Fsr=FQ/(M x Q x V) (1)	
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	
M0	Q1	Q0	U2	U1	U0	P0	ECK	M	Q (2)
0	-	-	-	-	-	-	-	3	
1	-	-	-	-	-	-	-	4 (INI)	
-	0	0	-	-	-	-	-		5 (INI) (4.5)
-	0	1	-	-	-	-	-		6 (5.5)
-	1	0	-	-	-	-	-		7 (6.5)
-	1	1	-	-	-	-	-		8 (7.5)

INI : initial value

Notes : 1. The V divider is programmed in the RxCR3 Register
2. To use the fractional divider bits HQ1 and HQ0 in Table 41 must be set to "1" (otherwise they are set to "0").

VI.2.9 - Receive Baud Rate Frequency Programming. Divisor Rank

Table 36 : Receive Baud Rate Frequency Programming. Divisor Rank

RxCR1 Register								Baud rate frequency Rxrclk = Fsr / U
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank U
M0	Q1	Q0	U2	U1	U0	P0	ECK (1)	
-	-	-	0	0	0	-	-	3 (INI)
-	-	-	0	0	1	-	-	4
-	-	-	0	1	0	-	-	5
-	-	-	0	1	1	-	-	6
-	-	-	1	0	0	-	-	8
-	-	-	1	0	1	-	-	12
-	-	-	1	1	0	-	-	16
-	-	-	1	1	1	-	-	16

INI : initial value

Note : 1. ECK bit is used to enable the RxRCLK and RxHSCLK outputs (as well as TxRCLK and TxHSCLK clock outputs) when set at logical 1. The baud rate clock must be programmed to its correct value even though the corresponding output pin is disabled (ECK = 0).

VI.2.10 - Highest Synchronous Transmit Bit Frequency Programming. Divisor Rank

Table 37 : Highest Synchronous Transmit Bit Frequency Programming. Divisor Rank

RxCR1 Register								Highest Synchronous Receive frequency Rxhsclk=FQ/P0
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank P
M0	Q1	Q0	U2	U1	U0	P0	ECK	
-	-	-	-	-	-	0	-	3 (INI)
-	-	-	-	-	-	1	-	4
-	-	-	-	-	-	-	0	Disable RxRCLK, RxHSCLK, TxRCLK and TxHSCLK Output
-	-	-	-	-	-	-	1	Enable RxRCLK, RxHSCLK, TxRCLK and TxHSCLK Output (INI)

INI : initial value

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.11 - Receive Fine Phase Shift Programming

Table 38 : Receive Fine Phase Shift Programming

RxCR2 Register								Receive Fine Phase Shift Programming
D7	D6	D5	D4	D3	D2	D1	D0	Action on RxDPLL Number of Master Clock Pulses Suppressed
LL	PS3	PS2	PS1	PS0	AP2	AP1	AP0	
0	0	0	0	0	0	0	0	No phase shift (INI)
0	0	0	0	1	0	0	0	8
0	0	0	1	0	0	0	0	12
0	0	0	1	1	0	0	0	16
0	0	1	0	0	0	0	0	20
0	0	1	0	1	0	0	0	24
0	0	1	1	0	0	0	0	28
0	0	1	1	1	0	0	0	32
0	1	0	0	0	0	0	0	One Txoclk oversampling period (1)
1	-	-	-	-	-	-	-	As above but lead instead of lag (i.e. addition of Master-Clock pulses)

INI : initial value

Note 1 : Available only with an internal Q divider. To shift one oversampling period, the chip must know the Q divider value currently used.

VI.2.12 - Receive Coarse Phase Shift Programming

Table 39 : Receive Coarse Phase Shift Programming

RxCR2 Register								Receive Coarse Phase Shift Amplitude Programming
D7	D6	D5	D4	D3	D2	D1	D0	Number of Master Clock Pulses Suppressed
LL	PS3	PS2	PS1	PS0	AP2	AP1	AP0	
0	0	0	0	0	0	0	0	No Phase Shift (INI)
0	0	0	0	0	0	0	1	64
0	0	0	0	0	0	1	0	128
0	0	0	0	0	0	1	1	256
0	0	0	0	0	1	0	0	512
0	0	0	0	0	1	0	1	1024
0	0	0	0	0	1	1	0	2048
0	0	0	0	0	1	1	1	4096

INI : initial value

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.13 - Interpolation Ratio

Table 40 : Interpolation Ratio

RxCR3 Register								INTERPOLATION RATIO Divisor value
D7	D6	D5	D4	D3	D2	D1	D0	V
V2	V1	V0	EMX	R2	R3	HQ1	HQ0	
0	0	0	-	-	-	-	-	128
0	0	1	-	-	-	-	-	128
0	1	0	-	-	-	-	-	160
0	1	1	-	-	-	-	-	160
1	0	0	-	-	-	-	-	128 (INI)
1	0	1	-	-	-	-	-	192
1	1	0	-	-	-	-	-	160
1	1	1	-	-	-	-	-	256 (1)

INI : initial value

Note 1 : The performances are not garanted with this oversampling ratio.

VI.2.14 - Receive Test Programming & R2 & R3 Divisor

Table 41 : Receive Test Programming and R2 and R3 Divisor

RxCR3 Register								Test Mode & R2 & R3 Divisor
D7	D6	D5	D4	D3	D2	D1	D0	
V2	V1	V0	EMX	R2	R3	HQ1	HQ0	
-	-	-	-	-	0	0	0	Normal Mode (INI)
-	-	-	-	R2	-	-	-	see Table 31 (RxCR0) R2 = 0 (INI)
-	-	-	-	-	R3	-	-	see Table 31 (RxCR0) R3 = 0 (INI)
-	-	-	0	-	-	-	-	Tx RCLK output on TxRCLK pin (INI)
-	-	-	1	-	-	-	-	FCOMP output on TxRCLK pin (see Figure 10)
-	-	-	-	-	-	1	1	HALF-INTEGER Q DIVIDER (see Table 35)

INI : initial value

VII - ELECTRICAL SPECIFICATIONS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for V_{DD} = +5V , T_{amb} = 25°C and for nominal crystal frequency FQ = 36.864MHz.

VII.1 - ABSOLUTE MAXIMUM RATINGS (referenced to GND)

Table 42 : Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3 to 7.0	V
V_I,V_{IN}	Digital or Analog Input Voltage	- 0.3, V_{DD} +0.3	V
I_I,I_{IN}	Digital or Analog Input Current	± 1	mA
I_O	Digital Output Current	± 20	mA
I_{OUT}	Analog Output Current	± 10	mA
T_{oper}	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature (plastic)	- 40, + 125	°C
P_{Dmax}	Maximum Power Dissipation	500	mW
ESD	Electrostatic Discharge Pins RxA1, RxA2, TxA1, TxA2, AV_{DD}, V_{CM} All other Pins	1500 2000	V V

VII.2 - DC CHARACTERISTICS (V_{DD} = 5.0V±5%, GND = 0V, T_A = 0 to +70°C, unless otherwise specified)

VII.2.1 - Power Supply and Common Mode Voltage

Table 43 : Power Supply And Common Mode Voltage

Symbol	Parameter	Min.	Typ.	Max.	Unit
SINGLE POWER SUPPLY (DV_{DD} = AV_{DD})					
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DDA}	Analog Supply Current		8		mA
I_{DDD}	Digital Supply Current		32		mA
I_{DD}-LP	Supply Current in Low Power Mode		600		µA
V_{CM}	Output Common Mode Voltage V_{CM} Output Voltage Load Current (see Note 1)	V_{DD}/2-5%	V_{DD}/2	V_{DD}/2+5%	V
DOUBLE POWER SUPPLY (DV_{DD} # AV_{DD})					
DV_{DD}	Digital Supply Voltage	3.15	3.3	3.45	V
AV_{DD}	Analog Supply Voltage	4.75	5	5,25	V
I_{DDA}	Analog Supply Current		8		mA
I_{DDD}	Digital Supply Current		20		mA
V_{CM}	Output Common Mode Voltage (see Note 1)	V_{DD}/2-5%	V_{DD}/2	V_{DD}/2+5%	V

Note 1 : Device is very sensitive to noise on V_{CM} Pin. V_{CM} output voltage load current must be DC (<10µA). in order to drive dynamic load, V_{CM} must be buffered. AC variation in V_{CM} current magnitude decrease A/D and D/A performance.

VII.2.2 - Digital Interface (All digital pins except XTAL pins)

Table 44 : Digital Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
(T_A = 25°C, DV_{DD} = +3.3V)					
V_{IL}	Low Level Input Voltage			0.8	V
V_{IH}	High Level Input Voltage	DV_{DD}-0.5			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	±1	10	µA
V_{OH}	High Level Output Voltage (I_{LOAD} = -1mA)	DV_{DD}-0.5			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = 1mA)			0.4	V
C_{IN}	Input Capacitance		5		pF
(T_A = 25°C, DV_{DD} = +3.3V)					
V_{IL}	Low Level Input Voltage	-0.3		0.5	V
V_{IH}	High Level Input Voltage	DV_{DD}-0.5			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	±1	10	µA
V_{OH}	High Level Output Voltage (I_{LOAD} = -600µA)	DV_{DD}-0.5			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = 800µA)			0.3	V

VII - ELECTRICAL SPECIFICATIONS (continued)

VII.2.3 - Crystal Oscillator Interface (XTAL10,XTAL11)

Crystal mode only available at DV_{DD} = 5V otherwise external clock oscillator mandatory.

Table 45 : Crystal Oscillator Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage			1.5	V
V_{IH}	High Level Input Voltage	3.5			V
I_L	Low Level Input Current ($GND \le V_I \le V_{IL}$max)		-15		µA
I_H	High Level Input Current (V_{IH}min $\le V_I \le V_{DD}$)		15		µA

VII.2.4 - Analog Interface

Table 46 : Analog Interface

Symbol	Parameter		Min	Typ	Max	Unit
V_{REF}	Differential Reference Voltage Output = V_{REFP}-V_{REFN} = V_{REF} (with AV_{DD} = 5V)		2.40	2.50	2.60	V
Tempco (V_{REF})	V_{REF} Temperature Coefficient			200		ppm/°C
$V_{CMO\ IN}$	Input Common Mode Offset Voltage = $\frac{RxA1 + RxA2}{2} - V_{CM}$		-300		300	mV
$V_{DIF\ IN}$	Differential Input Voltage : RxA1-RxA2 <= 2*V_{REF}			2 * V_{REF}		Vpp
$V_{OFF\ IN}$	Differential Input DC Offset Voltage : RxA1 = RxA2 = V_{CM} (1)		-100		100	mV
$V_{CMO\ OUT}$	Output common mode voltage offset = $\frac{TxA1 + TxA2}{2} - V_{CM}$		200		200	mV
$V_{DIF\ OUT}$	Differential Output Voltage : TxA1-TxA2 <= 2*V_{REF}			2 * V_{REF}		Vpp
$V_{OFF\ OUT}$	Differential Output DC Offset Voltage : (TxA1 - TxA2)		-100		100	mV
V_{OUT}	Output Voltage EYEX,EYEY		GND		VDD	V
R_{IN}	Input Resistance RxA1, RxA2		100			kΩ
R_{OUT}	Output Resistance	TxA1,TxA2 EYEX, EYEY			20 50	Ω Ω
R_L	Load Resistance	TxA1,TxA2 EYEX, EYEY	10 1			kΩ MΩ
C_L	Load Capacitance	TxA1,TxA2 EYEX, EYEY			20 30	pF pF

Note 1 : Input DC offset can be cancelled by high-pass filtering in IIR2 filter

VII - ELECTRICAL SPECIFICATIONS (continued)

VII.3 - AC ELECTRICAL SPECIFICATIONS (V_{DD} = 5.0 V ± 5%, T_a = 0 to +70 °C)

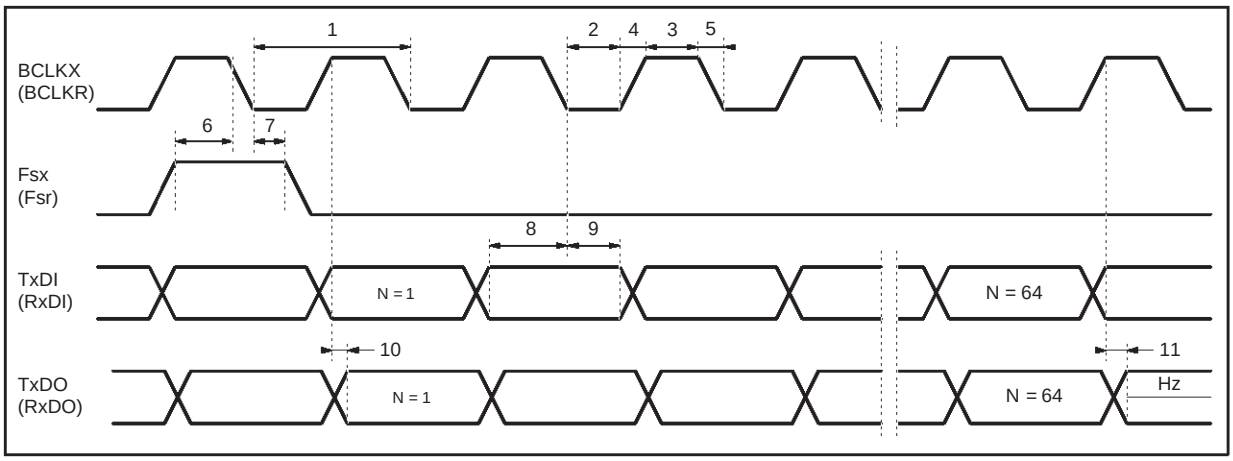
Output Load = 50 pF, Reference levels : V_{IL} = 0.8 V, V_{IH} = 2.2 V, V_{OL} = 0.4 V, V_{OH} = 2.4 V

VII.3.1 - Serial Channel Timing

Table 47 : Serial Channel Timing

Number	Parameter	Min.	Typ.	Max.	Unit
1	BCLKX, BCLKR Period	300			ns
2	BCLKX, BCLKR Width Low	135			ns
3	BCLKX, BCLKR Width High	135			ns
4	BCLKX, BCLKR Rise Time			30	ns
5	BCLKX, BCLKR Fall Time			30	ns
6	FSX, FSR to BCLKX, BCLKR Setup	100			ns
7	FSX, FSR to BCLKX, BCLKR Hold	100			ns
8	TxDI, RxDI to BCLKX, BCLKR Setup	20			ns
9	TxDI, RxDI to BCLKX, BCLKR Hold	0			ns
10	BCLKX, BCLKR High to TxDO, RxDO Valid		50	50	ns
11	BCLKX, BCLKR To TxDO, RxDO Hiz		50	50	ns

Figure 12 : Serial Channel Timming

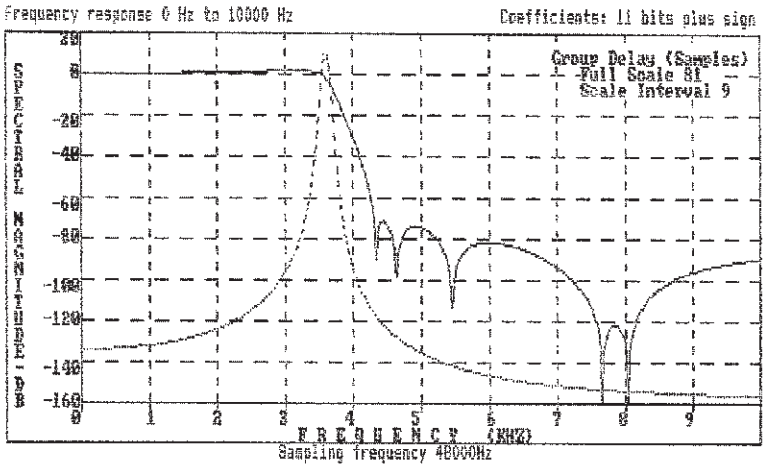


VIII - TRANSMIT CHARACTERISTICS

VIII.1 - TEST CONDITIONS

The Tx characteristics depend on the transfer function of the transmit filter. The indicated performance is measured when IIR1 filter implements the 8th order low-pass transfer function (including sinx/x correction) shown in Figure 13. This is achieved by loading the coefficients given in table 48.
The frequency response in Figure 13 includes the gain of 72.25dB in front of the biquad 1 (see Figure A1)

Figure 13 : Filter Transfer Function (Sampling frequency = 48000Hz, Fsx = 9600Hz, Sample of group delay = 1/5 x Fsx)



7545-15.TIF

Table 48 : Interpolator Filter Coefficients

WORD	7200,9600	WORD	7200,9600	WORD	7200,9600	WORD	7200,9600	WORD	7200,9600
1	0000,0000	9	0000,ca08	17	4c98,5070	25	a000,a000	33	0750,0858
2	0000,0000	10	0000,a000	18	2438,3508	26	adb8,ac18	34	6aa8,4098
3	a000,a000	11	b368,b570	19	d7a8,cfa0	27	5e70,6118	35	a000,a000
4	0000,0000	12	4400,48a0	20	a000,a000	28	0748,07a0	36	0000,0000
5	0000,0000	13	0200,2838	21	af18,aed8	29	a280,3368	37	0000,0000
6	0000,b7d8	14	d330,cb68	22	5690,59d0	30	a000,a000	38	0008,0008
7	0000,42b0	15	a000,a000	23	2118,2898	31	a910,adf0	-	-
8	a000,0118	16	b118,b268	24	4f80,dd90	32	5120,5338	-	-

Filter coefficients (HEX FORMAT) for Fsx equal to 7200 and 9600Hz respectively

VIII.2 - PERFORMANCE OF THE Tx CHAIN (from IIR1 filter input to (TxA1-TxA2) output)

Typical values are given for V_{DD} = +5V , T_{amb} = 25°C and for nominal crystal frequency FQ = 36.864MHz. Measurement band = 300Hz to 3.4kHz - Tx DPLL free running.

Table 49 : Performance of the Tx chain

Symbol	Parameter	Min	Typ	Max	Unit
Gabs	Absolute gain at 1kHz	-0.5	0	0.5	dB
THD	Total harmonic distortion (differential Tx signal : V_{OUT} = 1.6V_{PP}, f = 1kHz, OverSampling ratio 160) Fsx = 7200Hz Fsx = 9600Hz		 -89 -89		 dB dB
DR	Dynamic range (1) (f = 1kHz, OverSampling ratio 160) Fsx = 7200Hz Fsx = 9600Hz		91 92		dB dB
PSRR	Power supply rejection ratio (f = 1kHz, V_{AC} = 200mV_{PP})		50		dB
CTxRx	Crosstalk (transmit channel to receive channel)		95		dB

Note 1 : Measured over the full 0 to Fsx/2 with a -10dBr input and extrapolated to fullscale

VIII.3 - SMOOTHING FILTER TRANSFER CHARACTERISTICS

The cut-off frequency of the single pole switch-capacitor low-pass filter following the DAC (Figure 1) is :

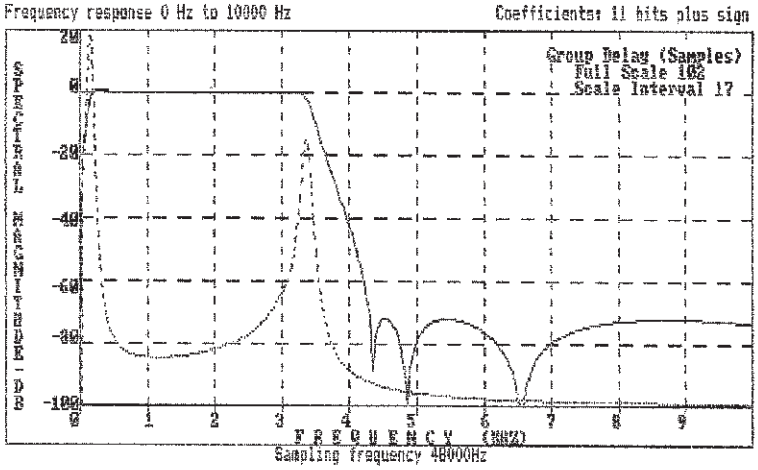
$$fc\text{-}3dB = 128*Fsx/(2*\pi*10) \text{ or } fc\text{-}3dB = 160*Fsx/(2*\pi*10)$$

IX - RECEIVE CHARACTERISTICS

IX.1 - TEST CONDITIONS

The Rx characteristics depend on the transfer function of the receive filter. The indicated performance is measured when IIR2 filter implements the 6th order band-pass transfer function shown in Figure 14. This is achieved by loading the coefficients given in Table 50.

Figure 14 : Filter Transfer Function (Sampling frequency = 48000Hz, Fsx = 9600Hz, Sample of group delay = 1/5 x Fsx)



7545-16.TIF

Table 50 : Decimator Filter Coefficients

WORD	7200,9600	WORD	7200,9600	WORD	7200,9600	WORD	7200,9600	WORD	7200,9600
1	0000,0000	9	0000,e000	17	4d90,4250	25	a000,a000	33	0d38,0618
2	0000,0000	10	e000,0000	18	25b8,2890	26	ab60,b5b0	34	0000,1a38
3	a000,a000	11	b2c0,bf38	19	d1b0,ca18	27	5a40,4e88	35	a000,a000
4	0000,0000	12	5998,4188	20	a000,a000	28	09b8,23c8	36	0000,0000
5	0000,0000	13	12c8,0188	21	b1f8,b748	29	2c30,d620	37	0000,0000
6	0000,0000	14	4c80,e000	22	4668,47a8	30	a000,a000	38	0008,0008
7	0000,0000	15	a000,0000	23	1408,1b98	31	a088,b470	-	-
8	20f8,3208	16	a5e0,b8e0	24	de78,cc80	32	6a30,5468	-	-

Filter coefficients (HEX FORMAT) for Fsx equal to 7200 AND 9600Hz respectively

IX.2 - PERFORMANCE OF THE Rx CHAIN (from (RxA1-RxA2) input to IIR2 filter output)

Typical values are given for V_{DD} = +5V , T_{amb} = 25°C and for nominal crystal frequency FQ=36.864MHz. Measurement band = 300Hz to 3.4kHz - Tx DPLL free running.

Table 51: Performance of the Rx chain

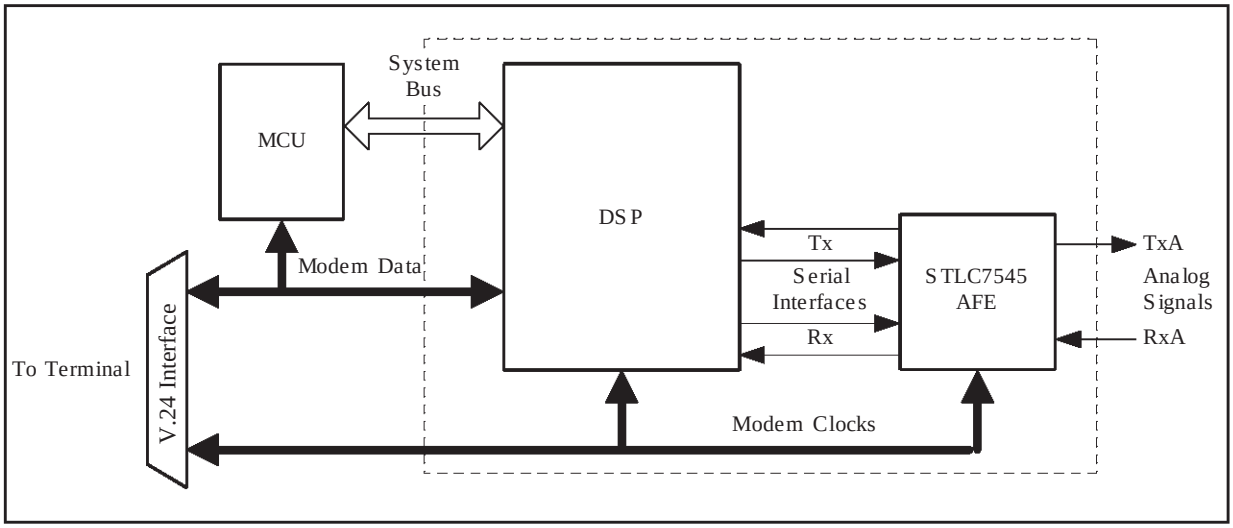
Symbol	Parameter	Min	Typ	Max	Unit
Gabs	Absolute gain at 1 kHz	-0.5	0	0.5	dB
THD	Total harmonic distortion (differential Rx signal : V_{IN} = 1.6 V_{PP}, f = 1kHz, OverSampling ratio 160) Fsx = 7200 Hz Fsx = 9600 Hz		 -89 -89		 dB dB
DR	Dynamic range (1) f = 1kHz, OverSampling ratio 160 Fsx = 7200 Hz Fsx = 9600 Hz		91 92		dB dB
PSRR	Power supply rejection ratio (f = 1kHz, V_{AC} = 200mV_{PP})		50		dB
CTxRx	Crosstalk (receive channel to transmit channel)		95		dB

Note 1 : Measured over the full 0 to Fsx/2 with a -10dBr input and extrapolated to fullscale

X - TYPICAL APPLICATIONS

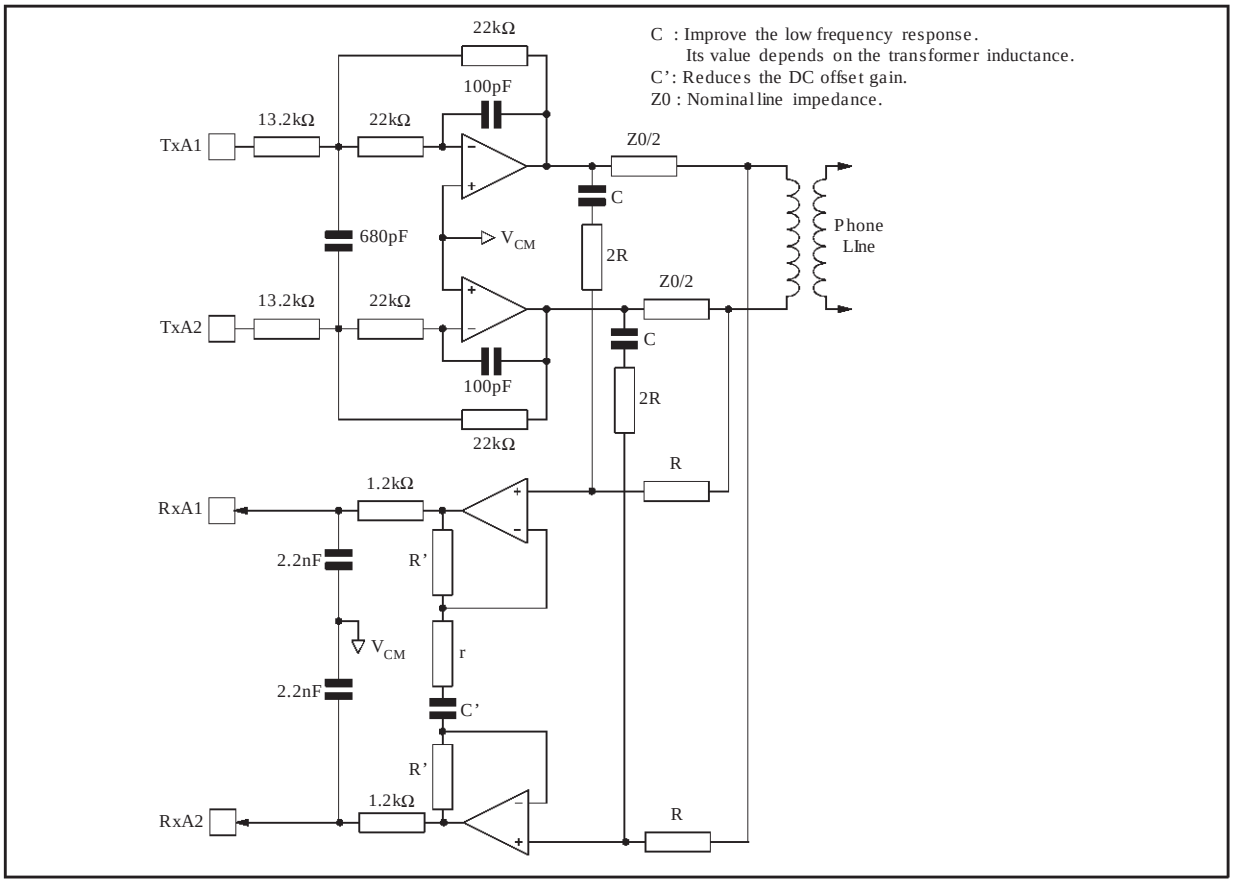
X.1 - MULTI-STANDARD MODEM WITH ECHO CANCELLING

Figure 15 : Multistandard Modem with Echo Cancelling Capability



X.2 - LINE INTERFACE

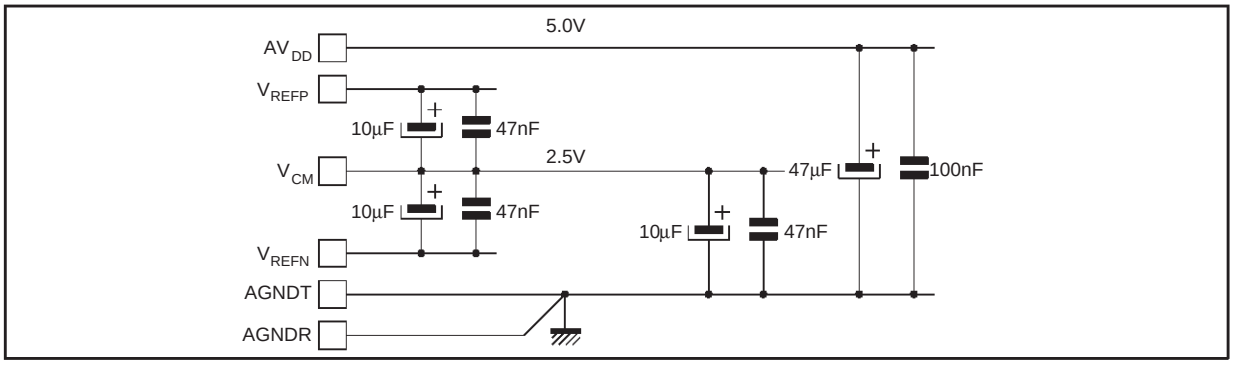
Figure 16 : Differential Duplexer



X - TYPICAL APPLICATIONS (continued)

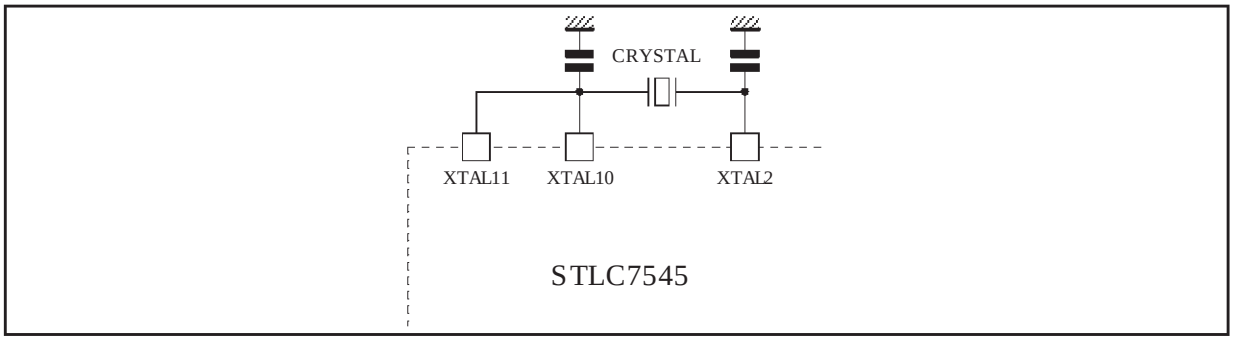
X.3 - COMMON MODE VOLTAGE GENERATION AND DECOUPLING

Figure 17 : Voltage Decoupling



X.4 - CRYSTAL OSCILLATOR

Figure 18 : External Components for Crystal Oscillator



XI - ANNEXE A

XI.1 - IIR FILTER OPERATION

Each IIR filtering section included in the ST7544 can perform up to seven biquadratic transfer functions in cascade, operating at four times the sampling frequency (see Figure A1).

Each biquad is defined by five coefficients, A, B, C, D and E (see Figure A2). An additional coefficient ,F, scales the IIR filter output.

Unused biquads are made transparent by programming A to one and the four remaining coefficients to zero. Such biquads should preferably be located in the first sections of the IIR filter in order to reduce the calculation noise.

XI.1.1 - Coefficient Rounding

Initially, coefficients of the filter to be implemented must be exclusively between +2 and -2. To derive the actual usable 12+1 bit coefficients, the rounding process described in Figure A3 must be performed.

Each 13 bit coefficient K is split into its doubling factor K2, and its 12 bit basic value K1, as the IIR architecture works with 12 bit coefficients and uses an extra accumulation when coefficient doubling is needed.

$$K2 \in [0,1] \text{ and } -2^{12} < K1 < +2^{12}$$

The coefficients are loaded into the different IIR filters through 16 bit wide time slots. The format to be used is as follows :

MSB	K1	LSB
K2	(12-bit)	0 0 0
(1 bit)		(3-bit)

<--------- 16 bit word -------->

To programme one IIR filter it is necessary to send five words per biquad followed by two additional words set to zero and the F coefficient word :

B(1), C(1), A(1), D(1), E(1), B(2),..., E(7), 0000_H, 0000_H, F

The total number of words sent is therefore 38.

XI.1.2 - Detailed Operation

The architecture of the device supporting the IIR filter is based on 28 bit data path. The basic function is as follows: one coefficient K(N) is multipled by one sample X(N) followed by one accumulation with value clampling. It can be precisely described as follows :

FUNCTION PAC K(N), X(N), S
LOCAL P
P = **TRUNC** (K1(N) x X(N)/2^{12})
S = S + P
IF ABS(S) > 2^{27} **THEN**
IF SIGN(S) > 0 **THEN CLAMP** S **TO** 2^{27}-1
ELSE CLAMP S **TO** 2^{27}

IF K2(N) = 1 **THEN** S = S + P
IF ABS(S) > 227 **THEN**
IF SIGN(S) > 0 **THEN CLAMP** S **TO** 2^{27}-1
ELSE CLAMP S **TO** 2^{27}

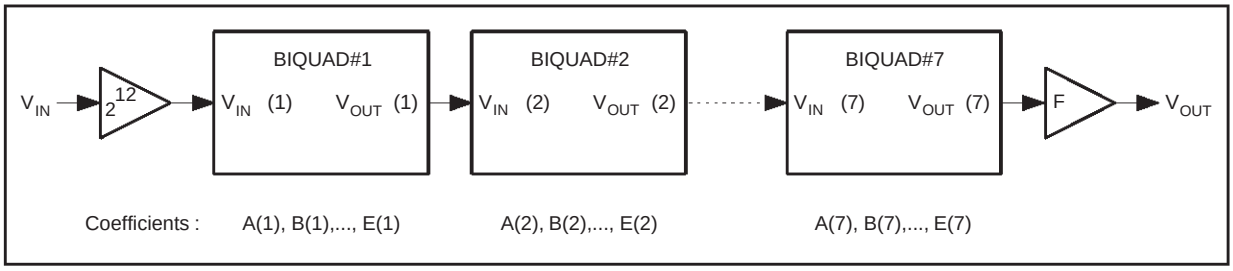
END OF FUNCTION

The TRUNC function is a two's complement truncature.

As previously mentionned, the second accumulation is controlled by the doubling factor K2(N).

The complete process of computing 16 bit output samples (V_{OUT}) from 16 bit input samples (V_{IN}) appears in Figure A4.

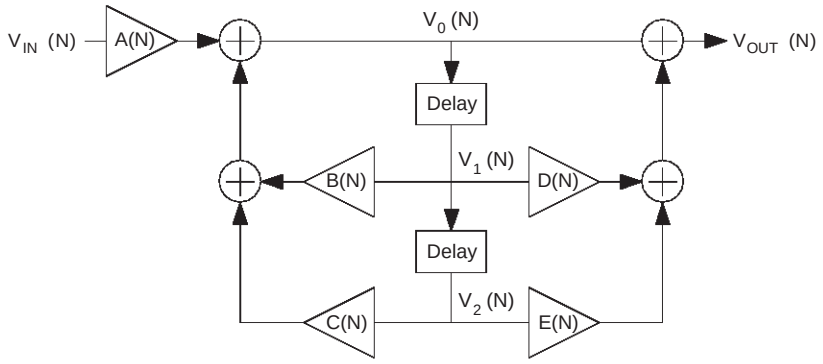
Figure A1 : IIR Filter Diagram



XI - ANNEXE A (continued)

Figure A2 : BIQUAD Structure

$$Hn(Z) = A\frac{1 + DZ^{-1} + EZ^{-2}}{1 - BZ^{-1} - CZ^{-2}}$$



Equation Set : $V_0(N) = B(N) \times V_1(N) + C(N) \times V_2(N) + A(N) \times V_{IN}(N)$ N = BIQUAD NUMBER (1:7)

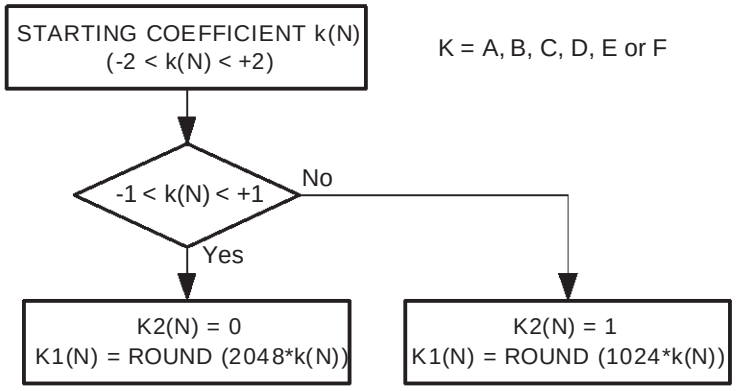
$V_{OUT}(N) = V_0(N) + D(N) \times V_1(N) + E(N) \times V_2(N)$

Next Step with : $V_2(N) = V_1(N)$

$V_1(N) = V_0(N)$

7545-22.EPS

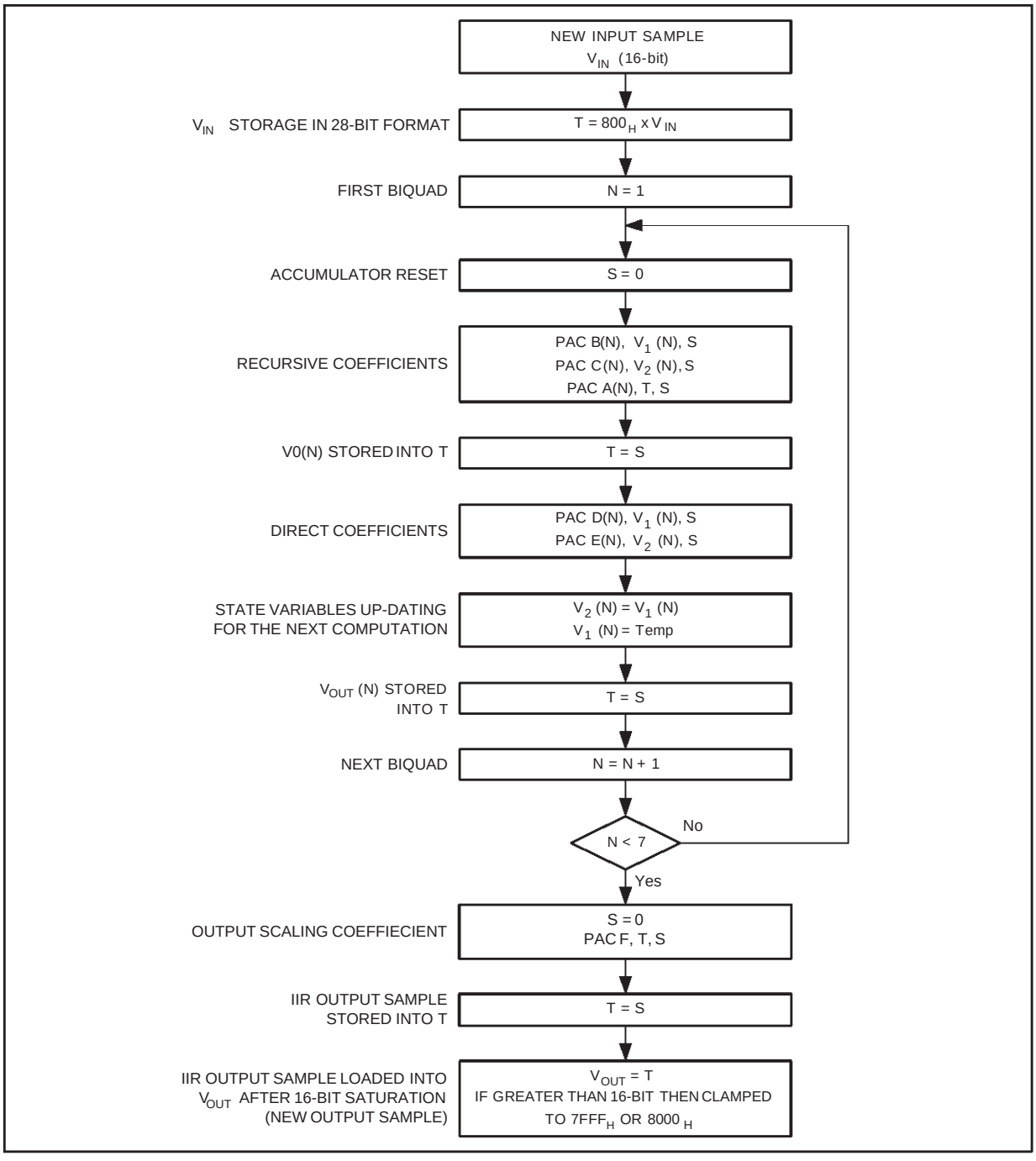
Figure A3 : IIR Coefficients Rounding



7545-23.EPS

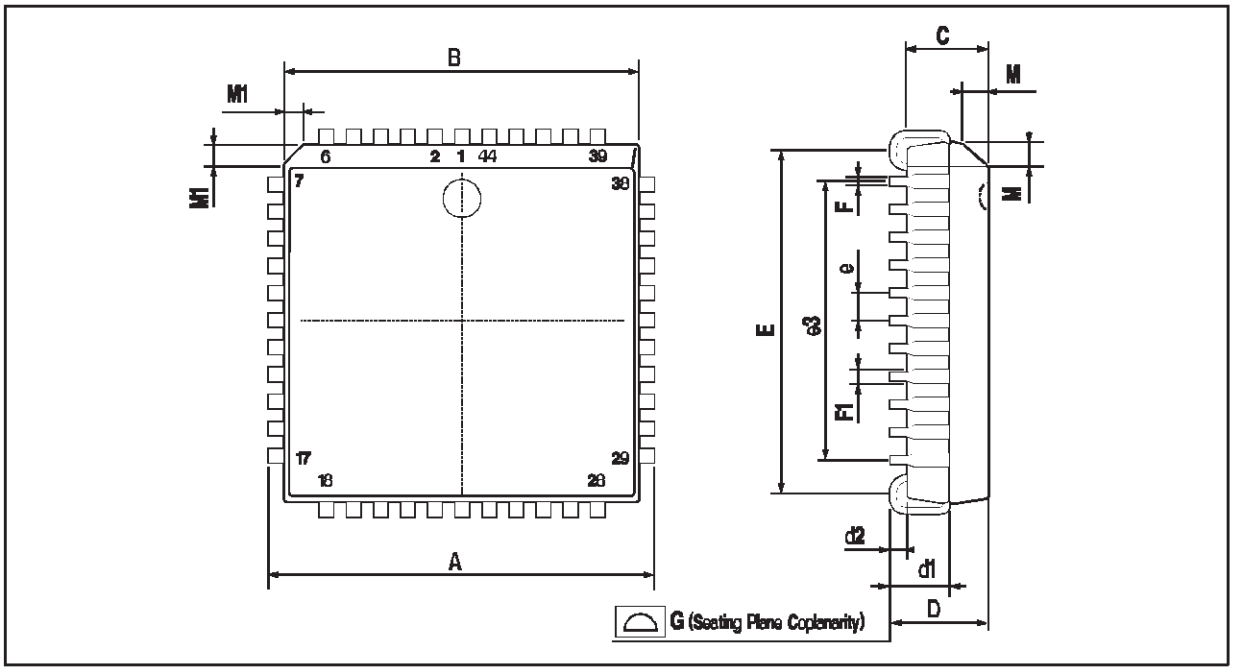
XI - ANNEXE A (continued)

Figure A4 : IIR Operating Sequence



XII - PACKAGE MECHANICAL DATA

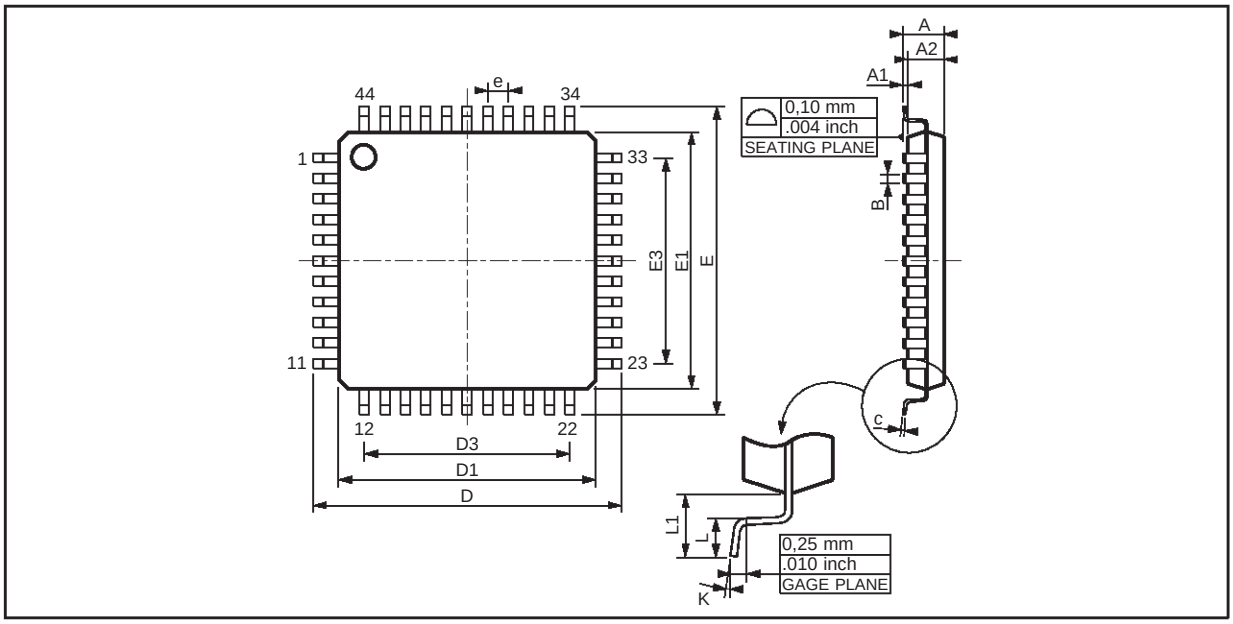
44 PINS - PLASTIC LEADED CHIP CARRIER (PLCC)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

PLCC44.TBL

PACKAGE MECHANICAL DATA (continued)
44 PINS - PLASTIC QUAD FLAT PACK (THIN) (TQFP)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.40	0.012	0.015	0.016
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					

4Y.TBL