National Semiconductor

August 2000

LM4832 Boomer® Audio Power Amplifier Series

Digitally Controlled Tone and Volume Circuit with Stereo Audio Power Amplifier, Microphone Preamp Stage and National 3D Sound

General Description

The LM4832 is a monolithic integrated circuit that provides volume and tone (bass and treble) controls as well as a stereo audio power amplifier capable of producing 250 mW (typ) into 8Ω or 90 mW (typ) into 32Ω with less than 1.0% THD. In addition, a two input microphone preamp stage, with volume control, capable of driving a 1 kΩ load is implemented on chip.

The LM4832 also features National's 3D Sound circuitry which can be externally adjusted via a simple RC network. For maximum system flexibility, the LM4832 has an externally controlled, low-power consumption shutdown mode, and an independent mute for power and microphone amplifiers .

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring few external components. Since the LM4832 incorporates tone and volume controls, a stereo audio power amplifier and a microphone preamp stage, it is optimally suited to multimedia monitors and desktop computer applications.

Key Specifications

- Output Power at 10% into 8Ω — 350mW (typ)
- Output Power at 10% into 32Ω — 100mW (typ)
- THD+N at 75mW into 32Ω at 1kHz — 0.5% (max)
- Microphone Input Referred Noise — 7µV (typ)
- Supply Current — 13mA (typ)
- Shutdown Current — 4µA (typ)

Features

- Independent Left and Right Output Volume Controls
- Treble and Bass Control
- National 3D Sound
- I^2C Compatible Interface
- Two Microphone Inputs with Selector
- Software Controlled Shutdown Function

Applications

- Multimedia Monitors
- Portable and Desktop Computers

Block Diagram

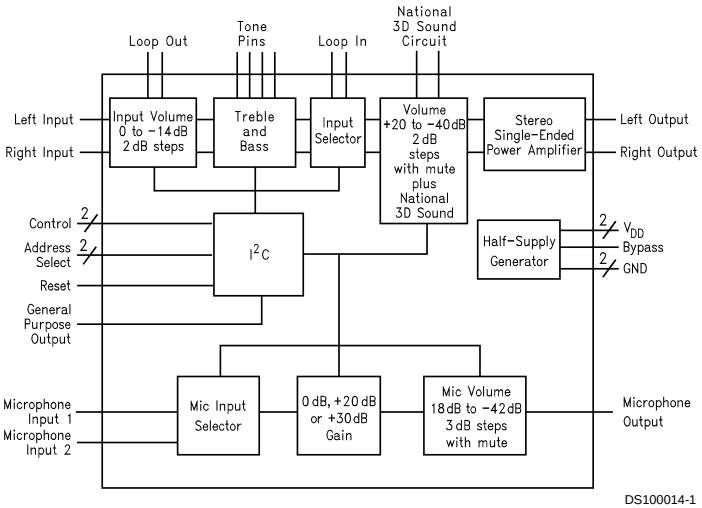
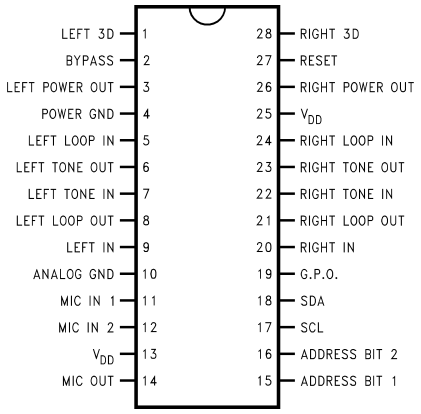


FIGURE 1. LM4832 Block Diagram

Connection Diagram



Top View
Order Number LM4832N, LM4832M
See NS Package Number N28B for DIP
See NS Package Number M28B for SOIC

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Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Note 3)	Internally limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	250V
Junction Temperature	150˚C
Soldering Information	
Small Outline Package	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C

See AN-450 "Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface mount devices.

θ_{JC} (typ)—N28B	21˚C/W
θ_{JA} (typ)—N28B	62˚C/W
θ_{JC} (typ)—M28B	15˚C/W
θ_{JA} (typ)—M28B	69˚C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	−40˚C ≤ T_A ≤ 85˚C
Supply Voltage	4.5 ≤ V_{DD} ≤ 5.5V

Electrical Characteristics for Entire IC (Notes 1, 2)

The following specifications apply for V_{DD} = 5V unless otherwise noted. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4832		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
V_{DD}	Supply Voltage	V_{IN} = 0V, I_O = 0A		4.5	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current		13	21	mA (max)
I_{SD}	Shutdown Current		2.5	9	µA (max)
INPUT ATTENUATORS					
A_R	Attenuator Range	Attenuation at 0 dB Setting		1	dB (max)
		Attenuation at −14 dB Setting		−15	dB (min)
A_S	Step Size	0 dB to −14 dB	2		dB
	Gain Step Size Error		0.1		dB (max)
E_T	Channel to Channel Tracking Error		0.15		dB (max)
BASS CONTROL					
A_R	Bass Control Range	f = 100 Hz, V_{IN} = 0.25V	±12	−14	dB (min)
				14	dB (max)
A_S	Bass Step Size		2		dB
E_{SE}	Bass Step Size Error		0.5		dB (max)
E_T	Bass Tracking Error		0.15		dB (max)
TREBLE CONTROL					
A_R	Treble Control Range	f_{IN} = 10 kHz, V_{IN} = 0.25V	±12	−13	dB (min)
				13	dB (max)
A_S	Treble Step Size		2		dB
E_{SE}	Treble Step Size Error		0.1		dB (max)
E_T	Treble Tracking Error		0.15		dB (max)
OUTPUT ATTENUATORS					
A_R	Attenuator Range	Gain at +20 dB Setting		21	dB (max)
		Attenuation at −40 dB Setting		−42	dB (min)
A_S	Step Size	+20 dB to −40 dB	2		dB
	Step Size Error		0.1		dB (max)
E_T	Channel to Channel Tracking Error		0.1		dB (max)
AUDIO PATH					
V_{OS}	Output Offset Voltage	V_{IN} = 0V	3	50	mV (max)

Electrical Characteristics for Entire IC (Notes 1, 2) (Continued)

The following specifications apply for V_{DD} = 5V unless otherwise noted. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4832		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
AUDIO PATH					
P_O	Output Power	THD = 1.0% (max), f = 1 kHz, All controls at 0dB			
		R_L = 8Ω	250		mW (min)
		R_L = 32Ω	95	75	mW (min)
THD+N	Total Harmonic Distortion+Noise	All Controls at 0 dB, THD = 10%, f = 1 kHz			
		R_L = 8Ω	350		mW
		P_O = 200 mW, R_L = 8Ω	0.15		%
		P_O = 75 mW, R_L = 32Ω	0.11		%
		V_O = 1 Vrms, R_L = 10Ω	0.08		%
PSRR	Power Supply Rejection Ratio	C_B = 1 µF, f = 100 Hz, V_{RIPPLE} = 100 mVrms, All Controls at 0 dB Setting	45		dB
A_M	Mute Attenuation	f = 1 kHz, V_{IN} = 1V	−75		dB
X_{TALK}	Cross Talk	P_O = 200 mW, R_L = 8Ω, All controls at 0 dB setting, f = 1 kHz			
		Left to Right	−85		dB
		Right to Left	−72		dB
MICROPHONE PREAMP AND VOLUME CONTROL					
A_V	Preamp Gain	0 dB Gain	0	−1, 1	dB
		+20 dB Gain	20	19, 21	dB
		+30 dB Gain	30	29, 31	dB
A_R	Attenuator Range	Gain at +18 dB Setting		20	dB (max)
		Attenuation at −42 dB Setting		−43	dB (min)
A_S	Step Size	0 dB to −42 dB	3		dB
	Step Size Error		0.4		dB (max)
V_{SWING}	Output Voltage Swing	f = 1 kHz, THD < 1.0%, R_L = 1 kΩ	1.7		V_{rms}
E_{NO}	Input Referred Noise	A-Weighted, Attenuator at 0 dB	7		µV (min)
PSRR	Power Supply Rejection Ratio	f = 100 Hz, V_{RIPPLE} = 100 mVrms, C_B = 1 µF	35		dB
A_M	Mute Attenuation		−90		dB
X_{TALK}	Cross Talk	Power Amp P_O = 200 mW, f = 1 kHz	−90		dB
THD+N	Total Harmonic Distortion Plus Noise	All controls at 0 dB, f = 1 kHz, V_O = 1V			
		0 dB Setting	0.03		%
		+20 dB Gain	0.03		%
		+30 dB Gain	0.04		%
I^2C BUS TIMING					
f_{MAX}	Maximum Bus Frequency			400	kHz
$T_{START:HOLD}$	Start Signal: Hold Time before Clock/Data Transitions			0.6	µs
$T_{D;SETUP}$	Data Setup Time			0.1	µs
$T_{C;HIGH}$	Minimum High Clock Duration			0.6	µs
$T_{C;LOW}$	Minimum Low Clock Duration			1.3	µs
$T_{STOP;SETUP}$	Stop Signal: Setup Time before Clock/Data Transitions			0.6	µs
I^2C BUS INPUT AND OUTPUT					
V_{IL}	Input Low Voltage			1.5	V (max)

Electrical Characteristics for Entire IC (Notes 1, 2) (Continued)

The following specifications apply for V_{DD} = 5V unless otherwise noted. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4832		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
I²C BUS INPUT AND OUTPUT					
V_{IH}	Input High Voltage			3	V (min)
I_{IN}	Input Current		0.15		µA
V_O	Output Voltage—SDA Acknowledge			0.4	V (max)
V_{OL}	External Power Amp Disable Low			0.4	V (max)
V_{OH}	External Power Amp Disable High			4	V (min)

Note 1: All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical applicationas shown in *Figure 1.*

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$.For the LM4832, T_{JMAX} = 150˚C, and the typical junction-to-ambient thermal resistance, when board mounted, is 69˚C/W assuming the M28B package.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Machine Model, 220 pF–240 pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

Note 7: Limits are guaranteed that all parts are tested in production to meet the stated values.

Typical Application Circuit

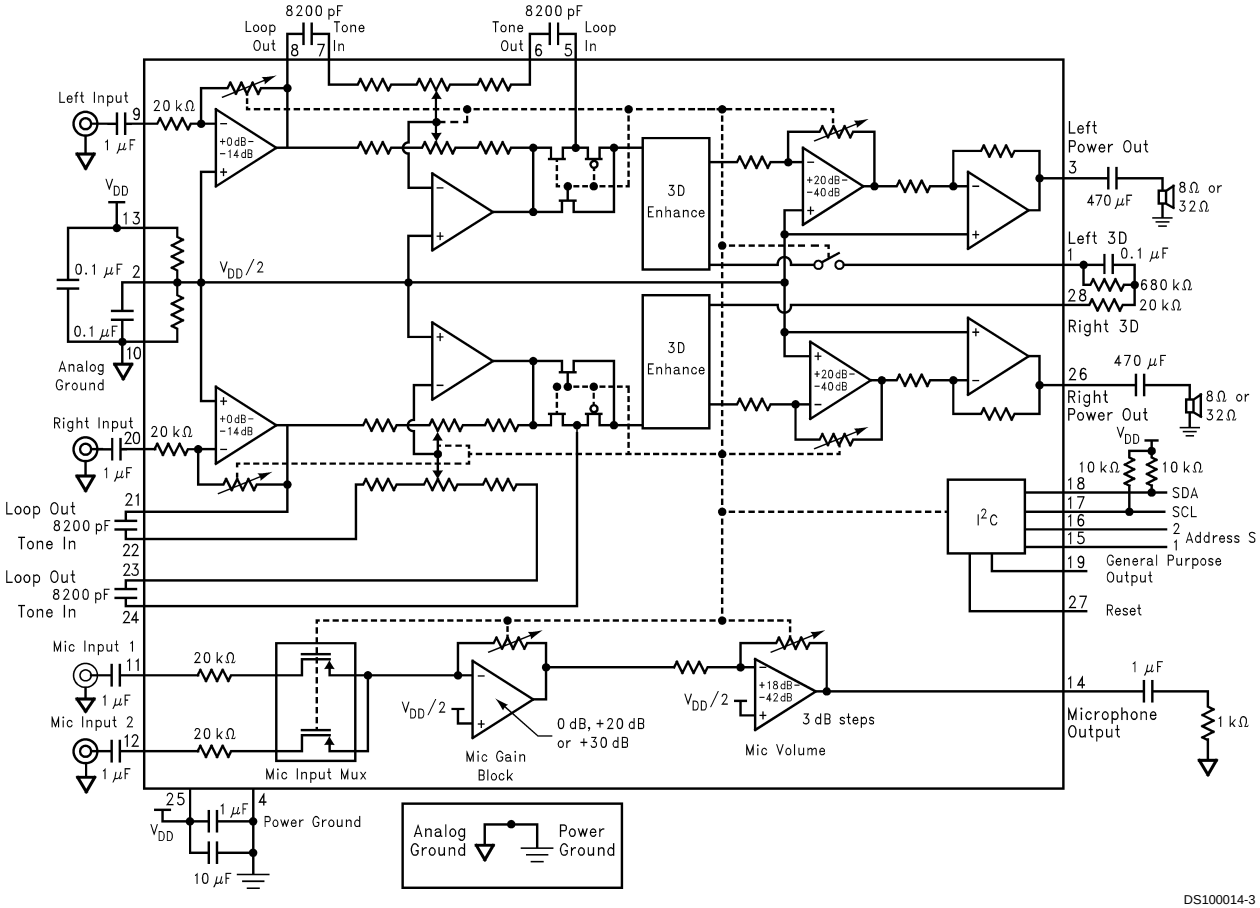
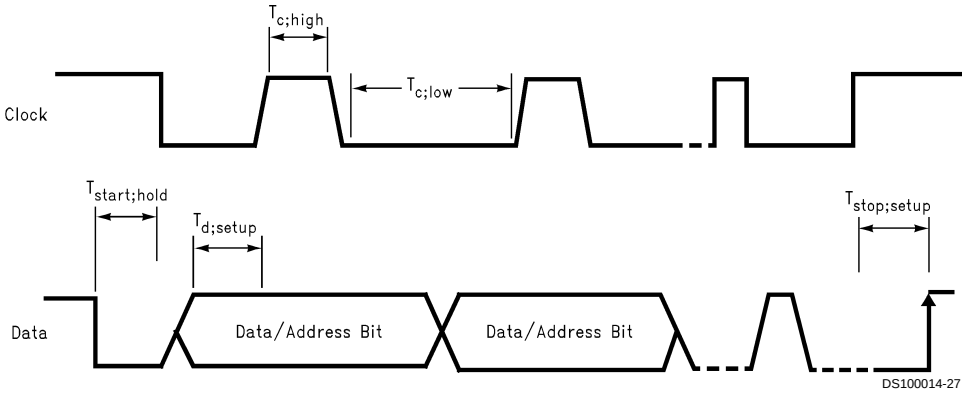


FIGURE 2. Typical Application Circuit

Pin Description

LEFT 3D (1) RIGHT 3D (28)	An external RC network is connected across these pins. This function provides left-right channel cross coupling and cancellation to create an enhanced stereo channel separation effect.
BYPASS (2)	A 0.1 µF capacitor is placed between this pin and ground to provide an AC ground for the internal half-supply voltage reference. The capacitor at this pin affects “click-pop” and THD performance. Turn-on and turn-off times are also determined by this capacitor. Refer to the Application Information section for more information.
POWER AMP OUT LEFT (3) RIGHT (26)	These outputs are intended to drive 8Ω speakers or 32Ω headphones. These outputs should be AC-coupled to the loads. Refer to the Application Information section for more information.
POWER GND (4)	This pin provides the high current return for the power output stage MOSFETs and digital circuitry.
LOOP OUT (8, 21) LOOP IN (5, 24)	These pins allow an external signal processor access to the stereo signal. Please see the Application Information section for more information.
TONE OUT (6, 23)	These pins are connected to the tone control op amp outputs and drive the power amplifier inputs. Refer to the Application Information section for more information.
TONE IN (7, 22)	These pins are connected to the inputs of the tone control op amps. A capacitor between the Tone In and Tone Out pins sets the frequency response of the tone functions. Please refer to the Application Information section for more information.
INPUTS (9, 20)	These pins are the stereo inputs for the LM4832. These pins should be AC-coupled to the input signals.
ANALOG GND (10)	This pin is the AC analog ground for the line level AC signal inputs.
MIC INPUTS (11, 12)	These pins are the two independent selectable microphone inputs. These pins should be AC-coupled.
MIC OUT (14)	This pin is the output for the microphone amplifier and should be AC-coupled to the load.
V_{DD} (13, 25)	These pins are for the 5V supply. These pins should be separately bypassed by 0.1 µF, or higher, film capacitors. The 5V supply should be bypassed by a 10 µF, or higher, tantalum or aluminum electrolytic capacitor.
ADDRESS BITS (15, 16)	These pins are used to determine the I^2C address for the LM4832.
CLOCK (17)	This pin is the input for the I^2C clock signal.
DATA (18)	This pin is the input for the I^2C data signal.
GENERAL PURPOSE OUTPUT (19)	This pin provides a general purpose TTL/CMOS output. Please refer to the Application Information section for more information.
RESET (27)	This pin is a TTL/CMOS input which is used to reset the chip logic and states.

Timing Diagram (Continued)



See Electrical Characteristics section fortiming specifications

FIGURE 4. I^2C Timing Diagram

Truth Tables

SOFTWARE SPECIFICATION

Chip Address

MSB							LSB
1	0	0	0	0	*E.C.	*E.C.	0

*E.C. = Externally Configuarable

Data Bytes (Brief Description)

MSB							LSB	Function
0	0	0	X	X	D2	D1	D0	Input Volume Control
0	0	1	X	D3	D2	D1	D0	Bass Control
0	1	0	X	D3	D2	D1	D0	Treble Control
0	1	1	D4	D3	D2	D1	D0	Right Output Vol./Mute
1	0	0	D4	D3	D2	D1	D0	Left Output Vol./Mute
1	0	1	X	$D_1$1	$D_1$0	$D_0$1	$D_0$0	Mic Input and Gain
1	1	0	D4	D3	D2	D1	D0	Microphone Volume
1	1	1	$D_4$0	$D_3$0	$D_2$0	$D_1$0	$D_0$0	General Control

Input Volume Control

MSB							LSB	Attenuation (dB)
0	0	0	X	X	0	0	0	0
0	0	0	X	X	0	0	1	−2
0	0	0	X	X	0	1	0	−4
0	0	0	X	X	0	1	1	−6
0	0	0	X	X	1	0	0	−8
0	0	0	X	X	1	0	1	−10
0	0	0	X	X	1	1	0	−12
0	0	0	X	X	1	1	1	−14
Input Volume Control Power Up State			X	X	0	0	0	Input Volume Control at 0 dB Attenuation

Bass Control

MSB							LSB	Level (dB)
0	0	1	X	0	0	0	0	−12
0	0	1	X	0	0	0	1	−10
0	0	1	X	0	0	1	0	−8
0	0	1	X	0	0	1	1	−6
0	0	1	X	0	1	0	0	−4
0	0	1	X	0	1	0	1	−2
0	0	1	X	0	1	1	0	0
0	0	1	X	0	1	1	1	2
0	0	1	X	1	0	0	0	4
0	0	1	X	1	0	0	1	6
0	0	1	X	1	0	1	0	8
0	0	1	X	1	0	1	1	10
0	0	1	X	1	1	0	0	12
Bass Control Power Up State			X	0	1	1	0	Bass Control is Flat

Truth Tables (Continued)

Treble Control

MSB							LSB	Level (dB)
0	1	0	X	0	0	0	0	−12
0	1	0	X	0	0	0	1	−10
0	1	0	X	0	0	1	0	−8
0	1	0	X	0	0	1	1	−6
0	1	0	X	0	1	0	0	−4
0	1	0	X	0	1	0	1	−2
0	1	0	X	0	1	1	0	0
0	1	0	X	0	1	1	1	2
0	1	0	X	1	0	0	0	4
0	1	0	X	1	0	0	1	6
0	1	0	X	1	0	1	0	8
0	1	0	X	1	0	1	1	10
0	1	0	X	1	1	0	0	12
Treble Control Power Up State			X	0	1	1	0	Treble Control is Flat

Left Volume Control

MSB							LSB	Function
1	0	0	0	0	0	0	0	20
1	0	0	0	0	0	0	1	18
1	0	0	. . .	. . .	. . .	. . .	. . .	. . .
1	0	0	1	1	1	0	1	−38
1	0	0	1	1	1	1	0	−40
1	0	0	1	1	1	1	1	Left Channel Mute
Left Volume Control Power Up State			1	1	1	1	1	Left Channel is Muted

General Control

MSB							LSB	Function
1	1	1					0	Chip On
1	1	1					1	Chip Shutdown
1	1	1				0		G.P.O. Output Low
1	1	1				1		G.P.O. Output High
1	1	1			0			Stereo Enhance Off
1	1	1			1			Stereo Enhance On
1	1	1		0				Stereo Operation
1	1	1		1				Mono Force On
1	1	1	0					External Loop Disable
1	1	1	1					External Loop Enable
General Control Power Up State			0	0	0	0	0	

Truth Tables (Continued)

Right Volume Control

MSB							LSB	Level (dB)
0	1	1	0	0	0	0	0	20
0	1	1	0	0	0	0	1	18
0	1	1	. . .	. . .	. . .	. . .	. . .	. . .
0	1	1	1	1	1	0	0	−38
0	1	1	1	1	1	1	0	−40
0	1	1	1	1	1	1	1	Right Channel Mute
Right Volume Control Power Up State			1	1	1	1	1	Right Channel Is Muted

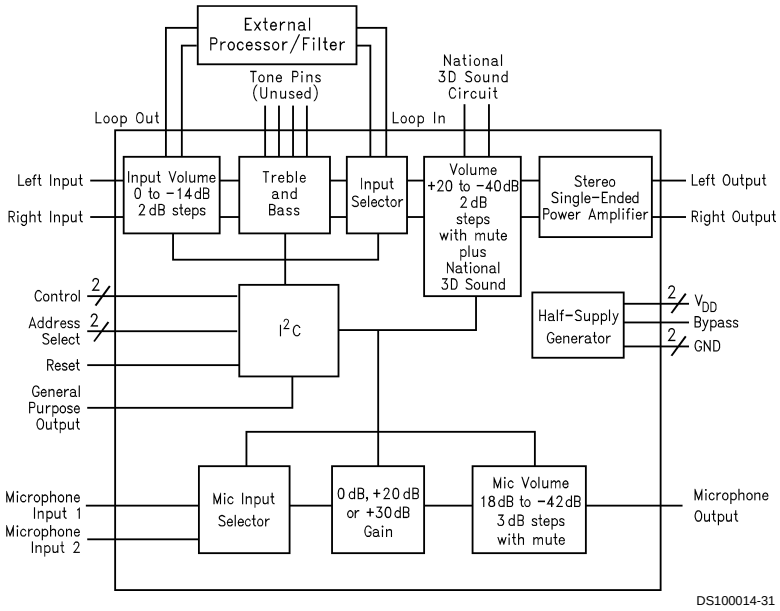
Microphone Input Selection and Gain

MSB							LSB	Function
1	0	1	X			0	0	Mic Input 1
1	0	1	X			0	1	Mic Input 2
1	0	1	X			1	X	Mic Input 1 and 2
1	0	1	X	0	0			Mic Gain (+0 dB)
1	0	1	X	0	1			Mic Gain (+20 dB)
1	0	1	X	1	0			Mic Gain (+30 dB)
Mic Input Sel. and Gain Power Up State			X	1	0	0	0	Mic 1 is selected with a +30 dB gain

Microphone Volume Control

MSB							LSB	Function
1	1	0	0	0	0	0	0	18
1	1	0	0	0	0	0	1	15
1	1	0	. . .	. . .	. . .	. . .	. . .	. . .
1	1	0	1	0	1	0	0	−42
1	1	0	1	0	1	0	1	Microphone Muted
Mic Volume Control Power Up State			1	0	1	0	1	Microphone Muted

Application Information (Continued)



LM4832 SAMPLE LAYOUT

LAYOUT PARTS LIST

Name	Type	Quantity
	Capacitors:	
C_{OUT}	1000 µF, elec., Digikey #P6205	4
C_{MOUT}	47 µF, elec., Digikey #P5202	1
C_S	0.33 µF, film, Digikey #P4669	3
C_{TONE}	8200 pF, ceramic, Digikey #P4823	4
C_{LIN}, C_{MIN}, C_{IN}	1 µF, film, Digikey #E1105	6
C_B	0.33 µF, film, Digikey #EF1334	1
C1	0.1 µF, film, Digikey #EF1104	1
	Resistors (all resistors: Digikey #(Value)QBK):	
R1	20 kΩ, 1/4W	1
R2	680 kΩ, 1/4W	1
R_{DATA}	1 kΩ, 1/4W	1
R_{GND}	100Ω, 1/4W	1
R_{PD}	100 kΩ, 1/4W	1

LAYOUT PARTS LIST

Name	Type	Quantity
	Connectors:	
Banana Jack		
Black	Mouser #164-6218	3
Red	Mouser #164-6218	3
RCA Jack	Mouser #16PJ097	7
Stereo Headphone	Shogyo #JJ-0357-3RT	1
Mono Miniplug	Shogyo #JJ-0357-B	2
36-pin Centronics	Digikey #1036RF	1

LAYOUT DESCRIPTION

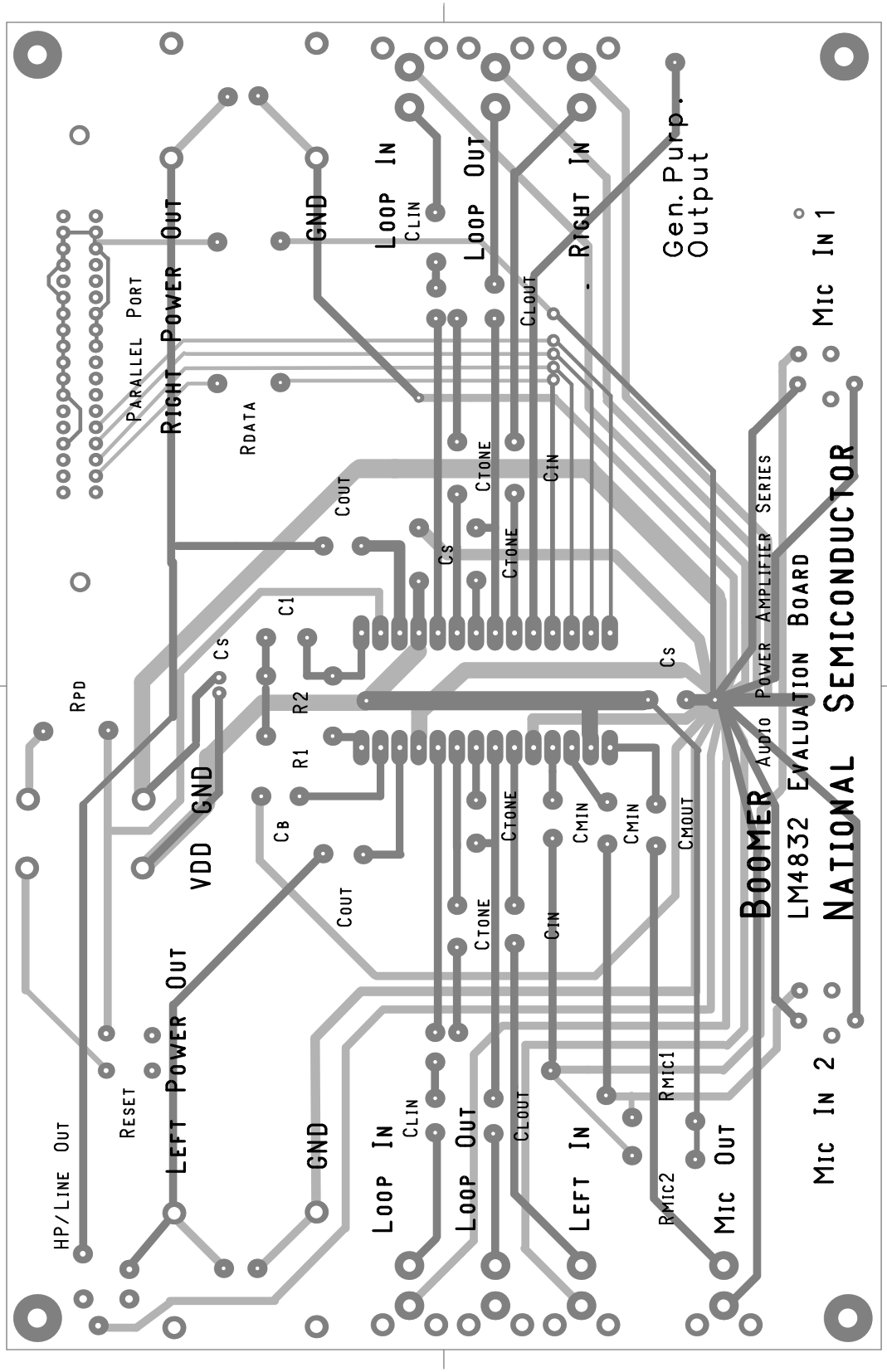
The layout given in the following pages is meant to be connected to a PC by a parallel port (printer) cable. The board is controlled by software for a Windows PC. The parallel cable must be the standard type used for hooking up a printer to a PC: one end is a DB-25 connector andthe other is a 36 pin Centronics connector.

Banana connections are provided for V_{DD}, ground, and amplifier outputs. Amplifier outputs are also routed to a stereo headphone jack. RCA connections are provided for amplifier inputs, loop in, loop out, and microphone out. Mono miniplug connectors are provided for microphone inputs.

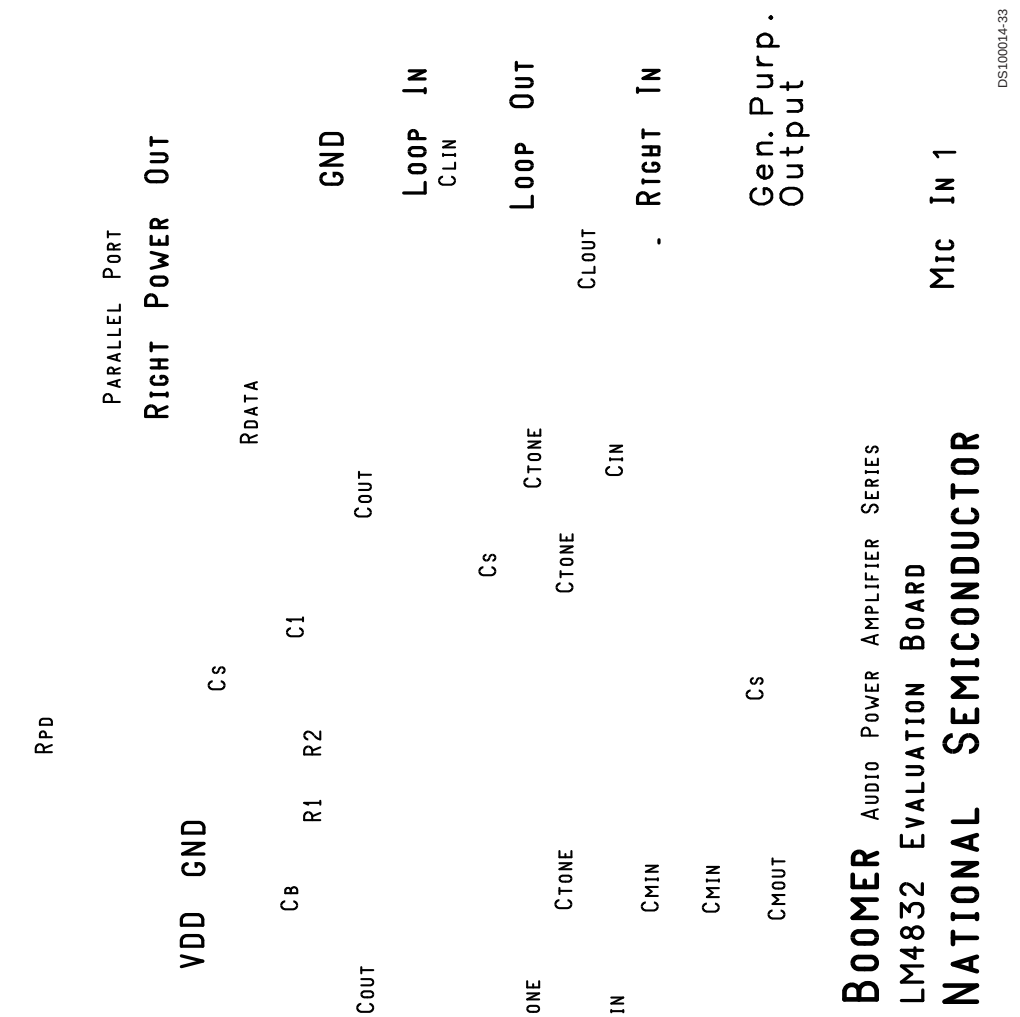
If required, microphones can be biased using the resistors R_{MIC1} and R_{MIC2}.

This layout is set up to allow the use of the internal tone-control circuitry or the external loop. The jumper next to each C_{LIN} capacitor controls which route the signal should take.

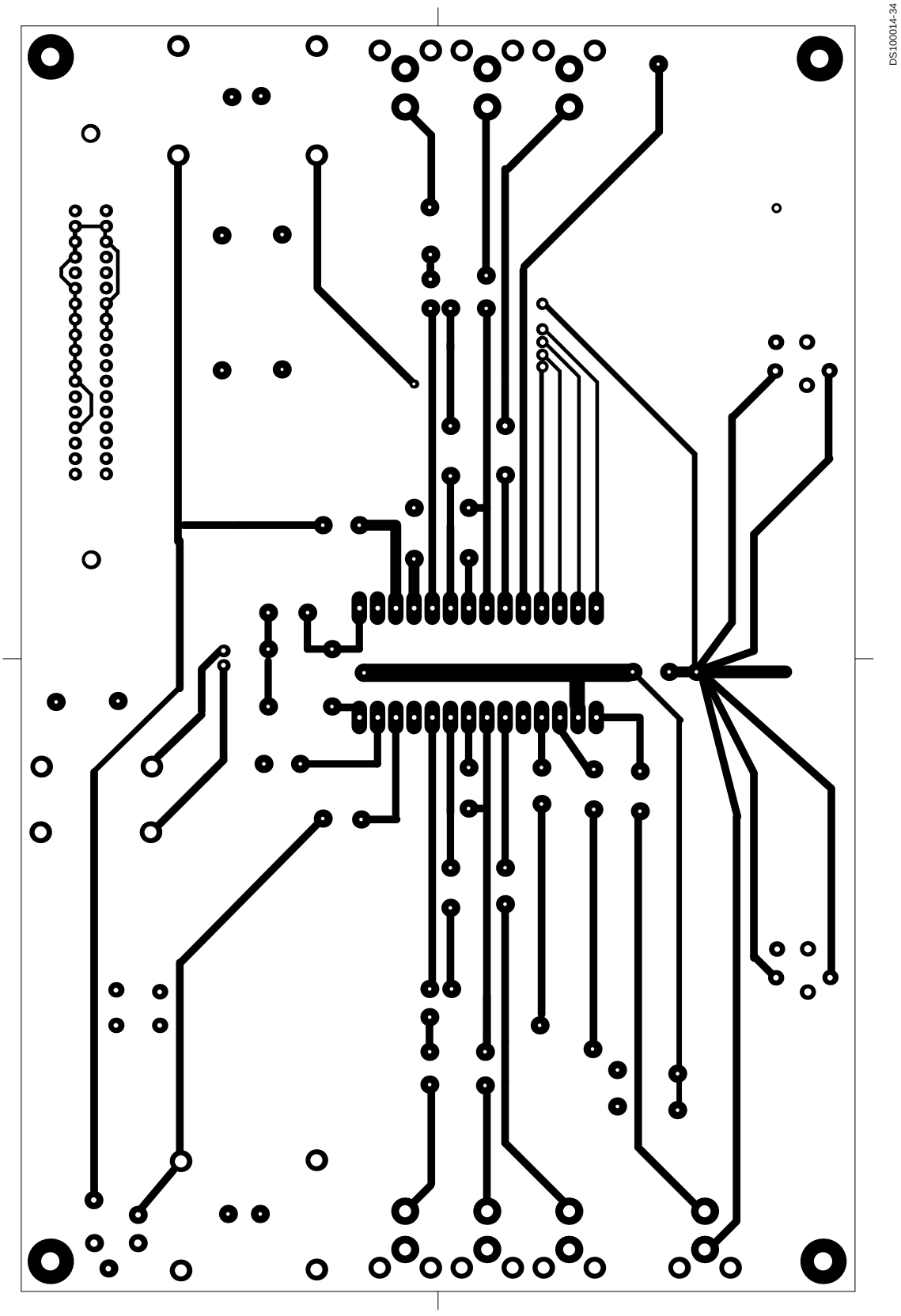
Typical Application PCB Layout (All Layers)



Typical Application PCB Layout (Silkscreen Layer)

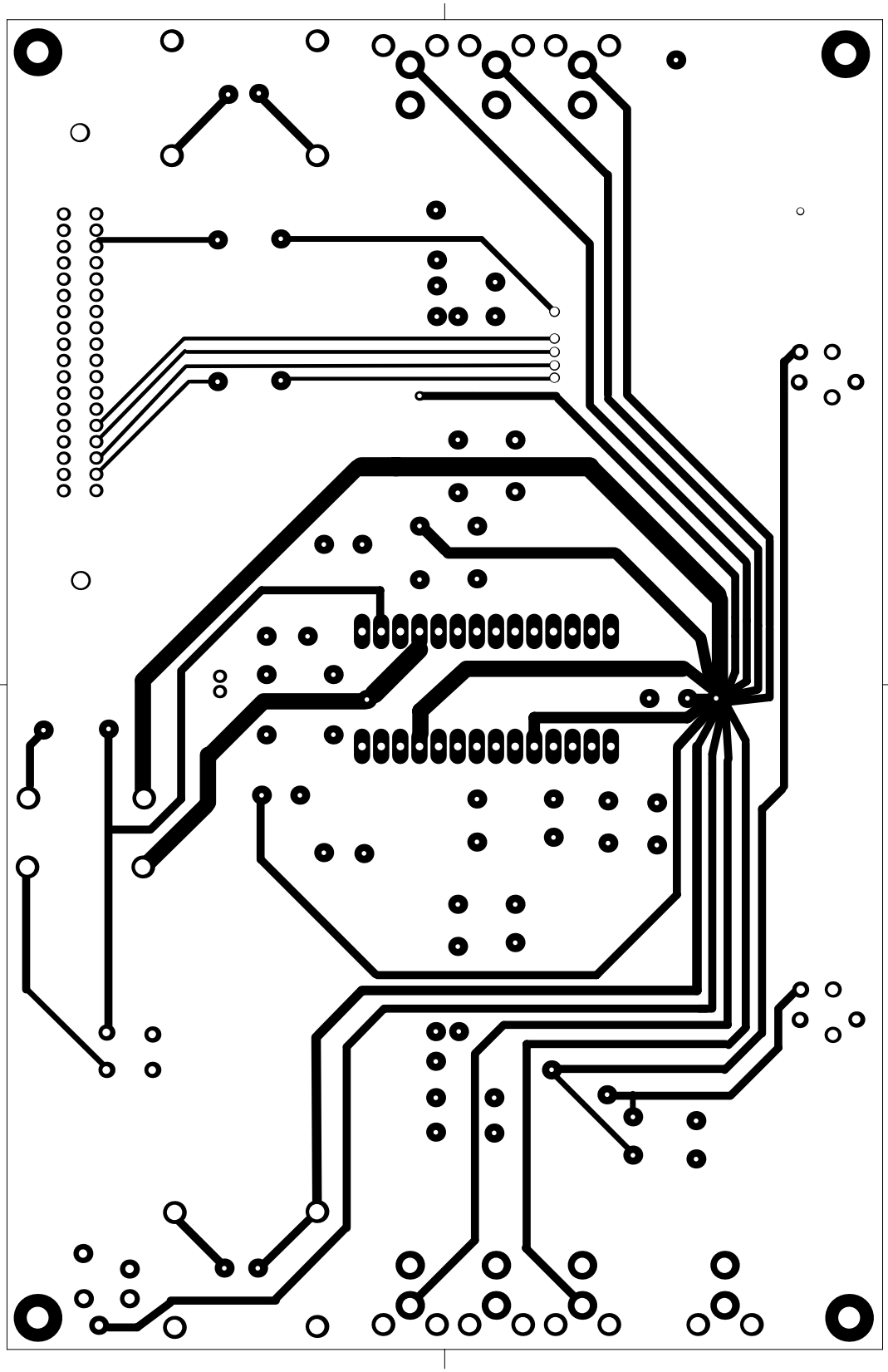


Typical Application PCB Layout (Bottom Layer)



DS100014-34

Typical Application PCB Layout (Top Layer)



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