EE121
John Wakerly
Lecture #1

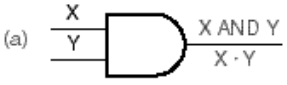
Introduction, Logic Circuits

Administrative

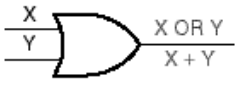
- Handouts
  - Lab Sign-Up Sheet
  - Fact Sheet
  - Course Outline (readings due **before** lecture)
  - Lab Assignment #0 (due next Friday 10/1)
- Turn in Lab Sign-Up Sheet today or Tuesday
- Subscribe to newsgroup “ee121@leland”
- Grading
  - 65-70% labs; do prelabs on-time and do a good job on documentation.
  - midterm + final (equal weight)
  - all labs and exams required; no incompletes.

Digital Logic

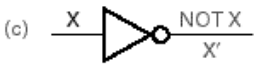
- Binary system -- 0 & 1, LOW & HIGH, negated and asserted.
- Basic building blocks -- AND, OR, NOT



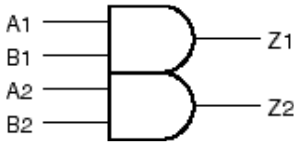
X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

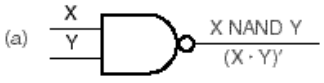


X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

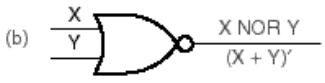


X	NOT X
0	1
1	0

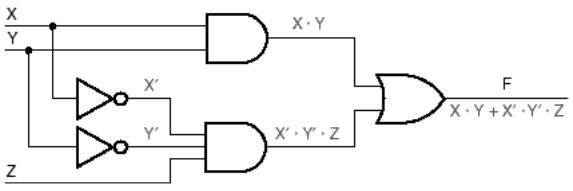




X	Y	X NAND Y
0	0	1
0	1	1
1	0	1
1	1	0

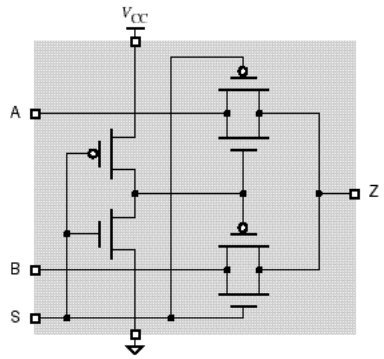


X	Y	X NOR Y
0	0	1
0	1	0
1	0	0
1	1	0



Many representations of digital logic

- Transistor-level circuit diagrams

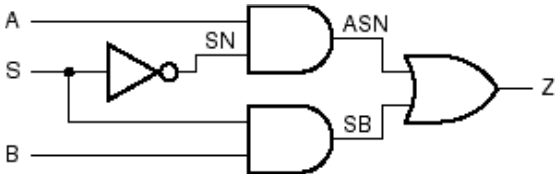


- Gate symbols (for simple elements)

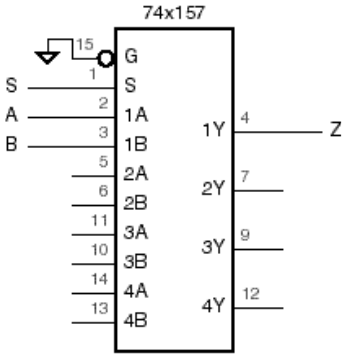
- Truth tables

S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

- Logic diagrams



- Prepackaged building blocks, e.g. multiplexer



- Equations: $Z = S' \cdot A + S \cdot B$

- Various hardware description languages
  - ABEL

```
module chap1mux
title 'Two-input multiplexer example'
CHAP1MUX device 'P16V8'

A, B, S      pin 1, 2, 3;
Z            pin 13 istype 'com';

equations

WHEN S == 0 THEN Z = A;  ELSE Z = B;

end chap1mux
```

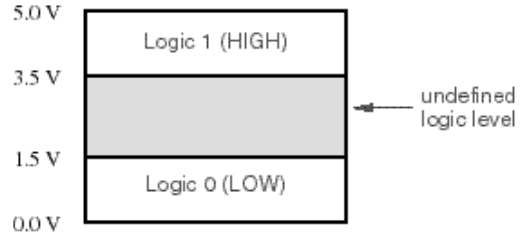
  - VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;

entity Vchap1mux is
    port ( A, B, S: in  STD_LOGIC;
           Z:       out STD_LOGIC );
end Vchap1mux;

architecture Vchap1mux_arch of Vchap1mux is
begin
  Z <= A when S = '0' else B;
end Vchap1mux_arch;
```

- We'll start with gates and work our way up

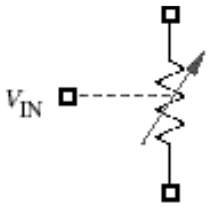
Logic levels

- Undefined region is inherent
  - digital, not analog
  - amplification, weak => strong



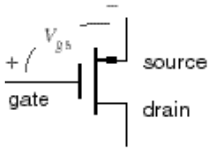
- Switching threshold varies with voltage, temp, process, phase of the moon
  - need “noise margin”
- The more you push the technology, the more “analog” it becomes.
- Logic voltage levels decreasing with process
  - 5 -> 3.3 -> 2.5 -> 1.8 V

MOS Transistors



Voltage-controlled resistance

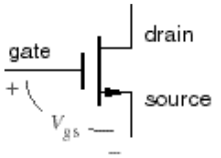
PMOS



Voltage-controlled resistance:
decrease V_{gs} ==> decrease R_{ds}

Note: normally, $V_{gs} \leq 0$

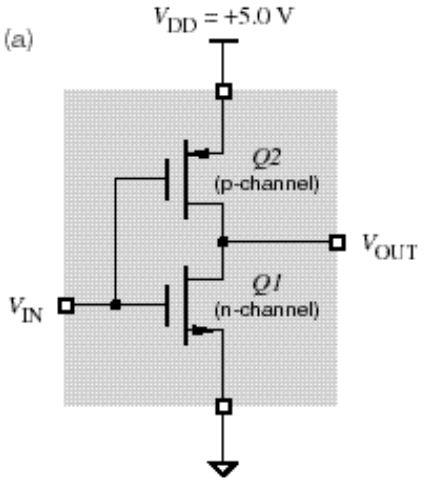
NMOS



Voltage-controlled resistance:
increase V_{gs} ==> decrease R_{ds}

Note: normally, $V_{gs} \geq 0$

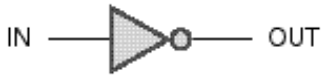
CMOS Inverter



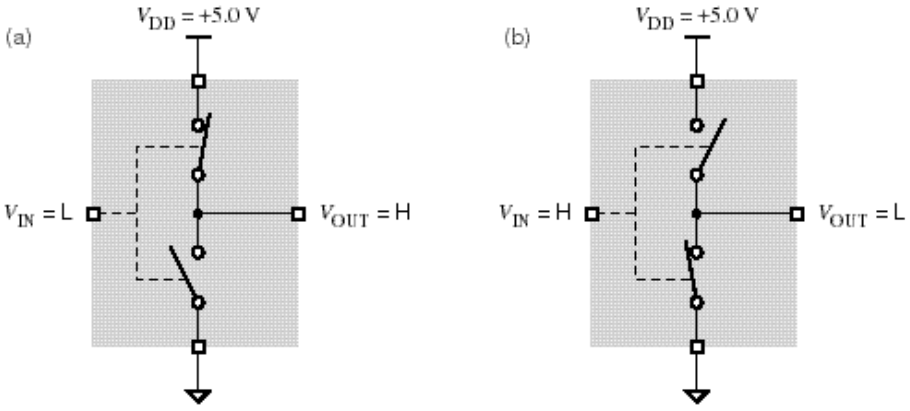
(b)

V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

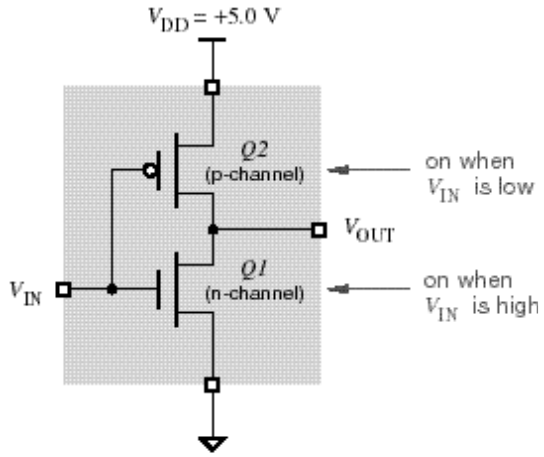
(c)



Switch model

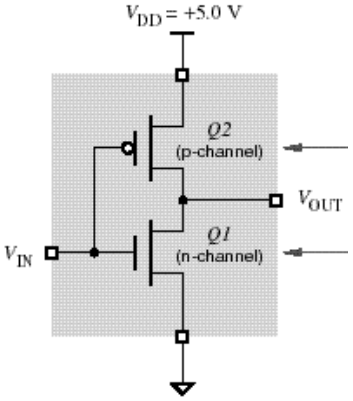


Alternate transistor symbols



CMOS Gate Characteristics

- No DC current flow into MOS gate terminal
  - However gate has capacitance ==> current required for switching (CV^2f power)
- No current in output structure except during switching
  - Both transistors partially on
  - Power consumption related to frequency
  - Slow input-signal rise times ==> more power
- Symmetric output structure ==> equally strong drive in LOW and HIGH states



- E102E announcement
- Foundation demo
- Sign up for mailing list, ee121@leland !
- Turn in lab sign-up sheet by Tuesday!