Ordering number : EN4469A

Monolithic Linear IC

LA4805V

3 V Stereo Headphone Power Amplifier

Overview

The LA4805V is a power IC developed for use in stereo headphones. It includes low frequency enhancement, beep function and output control circuits on-chip. Furthermore, the LA4805V realizes a high S/N ratio, a high ripple exclusion ratio, and low current drain.

Functions

- Stereo headphone power amplifier
- Low frequency enhancement (L.BOOST)
- Beep amplifier
- Output suppression circuit (PVSS)
- Power switch
- Muting switch

Features

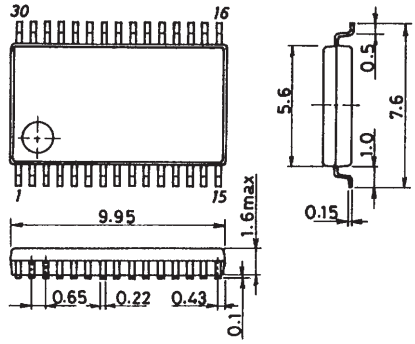
- Low current drain (8.3 mA typical)
- High S/N ratio (90 dB typical, 13 µV)
- High ripple exclusion ratio (75 dB typical)
- No output electrolytic capacitors required
- Ultra-miniature package (SSOP-30)

Package Dimensions

unit: mm

3191-SSOP30

[LA4805V]



SANYO: SSOP30

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		4.5	V
Allowable power dissipation	Pd max		500	mW
Operating temperature	Topr		–15 to +50	°C
Storage temperature	Tstg		–40 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		3.0	V
Recommended load resistance	R_L		16 to 32	Ω
Operating supply voltage range	V_{CC} op		1.8 to 3.6	V

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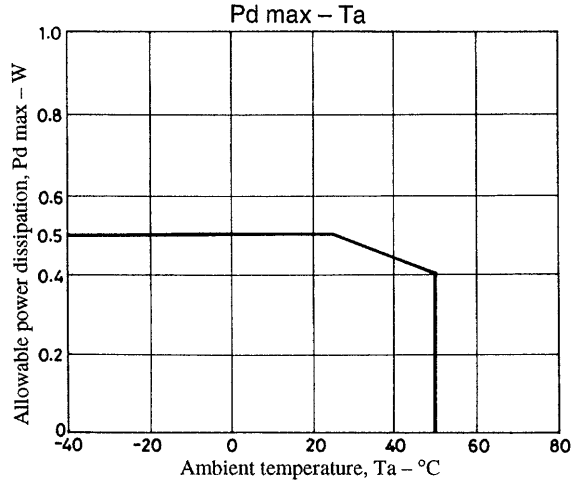
Operating Characteristics

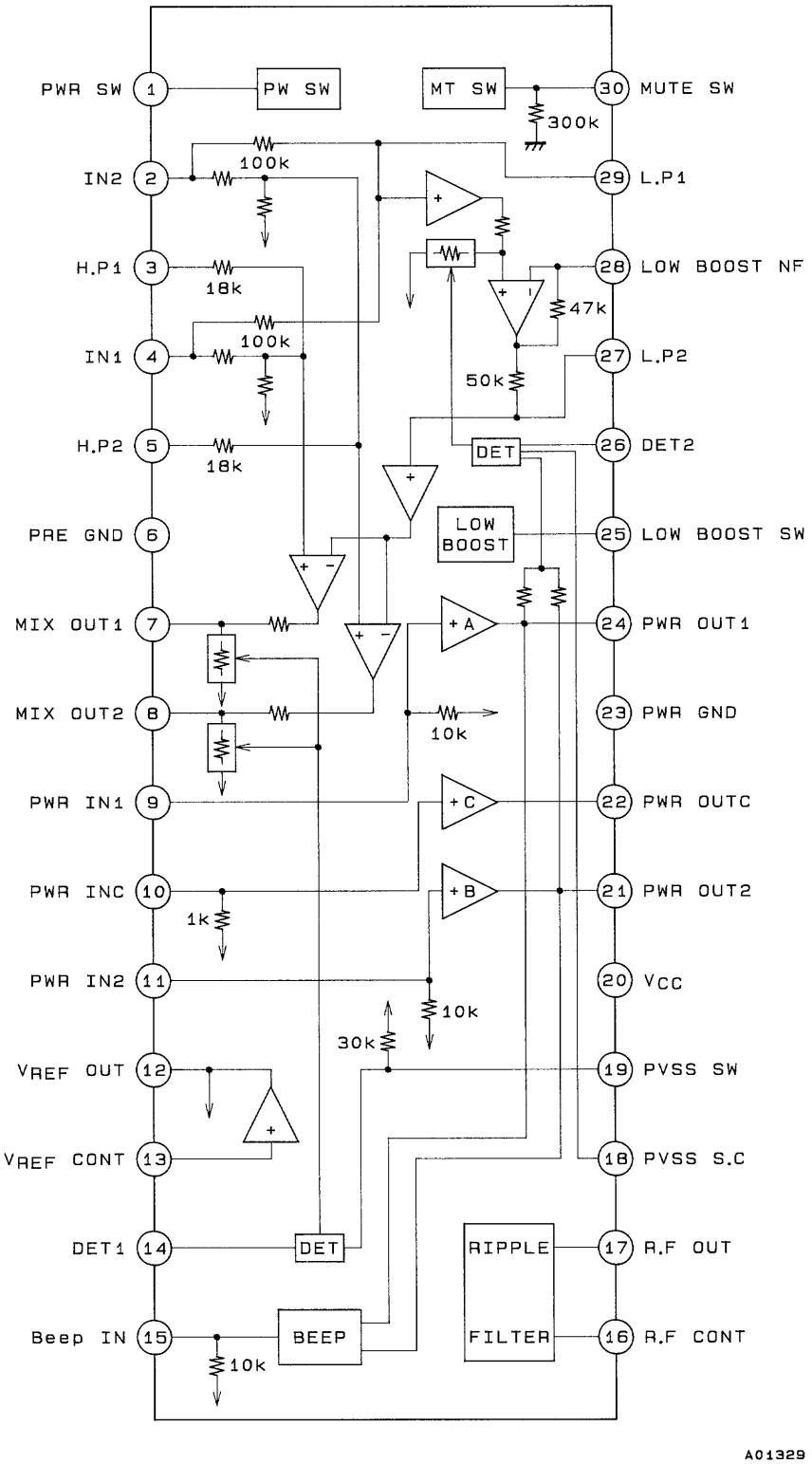
at Ta = 25°C, V_{CC} = 3.0 V, f = 1 kHz, 0.775 V = 0 dBm, R_L = 10 kΩ (L.B), R_L = 16 Ω (PWR)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[L.BOOST +PVSS + PWR]						
Quiescent current	$I_{CCO}1$	IC off		0.05	1.0	µA
	$I_{CCO}2$	Muting on	1.0	2.7	5.0	mA
	$I_{CCO}3$	Rg = 0, L.BST/PVSS off	4.0	8.3	12.0	mA
	$I_{CCO}4$	Rg = 0, L.BST/PVSS on	4.5	8.6	12.5	mA
[PWR AMP]						
Output power	P_O	THD = 10%	15	25		mW
Voltage gain	VG1	V_O = –10 dBm	15.7	17.7	19.7	dB
Channel balance	V_{BL}	V_O = –10 dBm	–1	0	1	dB
Total harmonic distortion	THD1	V_O = 0.35 V		0.1	0.3	%
Output noise voltage	$V_{NO}1$	Rg= 0, DIN AUDIO		13	25	µV
Crosstalk	CT1	V_O = –10 dBm, TUN = 1 kHz, Rg = 0	35	45		dB
Ripple exclusion ratio	SVRR1	V_{CC} = 1.8 V, f = 100 Hz, V_R = –20 dBm, TUN = 100 Hz	60	75		dB
Muting attenuation	ATT_M	THD = 1%, Rg = 0 kΩ	80	90		dB
Beep output	$V_{O\ BEEP}$	V_{IN} = –16 dBm (sine wave)	1.0	3.0		mV
Output current offset	$V_{DC\ OFF}$	V_{IN} = 0 V, Rg = 0	–20	0	20	mV
Input resistance	Ri		7	10	13	kΩ
[L.BOOST]						
Voltage gain	VG2	V_{IN} = –30 dBm, boost on/off	–3.2	–5.2	–7.2	dB
Boost*	L.BTS1	V_{IN} = –30 dBm, f = 100 Hz, boost on	13	15	17	dB
	L.BTS2	V_{IN} = –30 dBm, f = 10 kHz, boost on	3	5	7	dB
Maximum output voltage	V_O max	THD = 1%, boost on	0.2	0.4	0.6	V
Total harmonic distortion	THD2	V_O = 0.1 V, boost on		0.085	0.25	%
Crosstalk	CT2	V_O = –20 dBm, Rg = 0, boost on	25	30		dB
Output noise voltage	$V_{NO}2$	Rg = 0, boost off		3	10	µV
Ripple exclusion ratio	SVRR2	Rg = 0, f = 100 Hz, Vg = –20 dBm, boost on	50	60		dB
[L.BOOST + PWR]						
Voltage gain	VG3	V_{IN} = –30 dBm, f = 1 kHz, boost on/off	8	10	12	dB
Output voltage	V_O1	V_{IN} = –30 dBm, f = 100 Hz, boost on	0.13	0.23	0.33	V
Total harmonic distortion	THD3	V_{IN} = –30 dBm, f = 100 Hz, boost on		0.14	0.5	%
Crosstalk	CT3	V_O = –20 dBm, R_V = 0 Ω, boost on	25	32.5		dB
[L.BOOST + PVSS + PWR]: When V_O1 is maximum						
PVSS voltage	$V_{O\ PVSS}2$	V_{IN} = –30 dBm, PVSS2	–32.5	–37.5	–42.5	dBm
PVSS width	$V_{O\ PVSS}$ W	The input amplitude when the output is +3 dB over the starting point	25	30	35	dB
PVSS distortion	THD_{PVSS}	V_{IN} = –40 dBm, PVSS2		0.55	2.0	%
PVSS starting input	$V_{IN\ PVSS}$	PVSS2	–41	–46	–51	dBm

Note: * Boost levels relative to 1 kHz

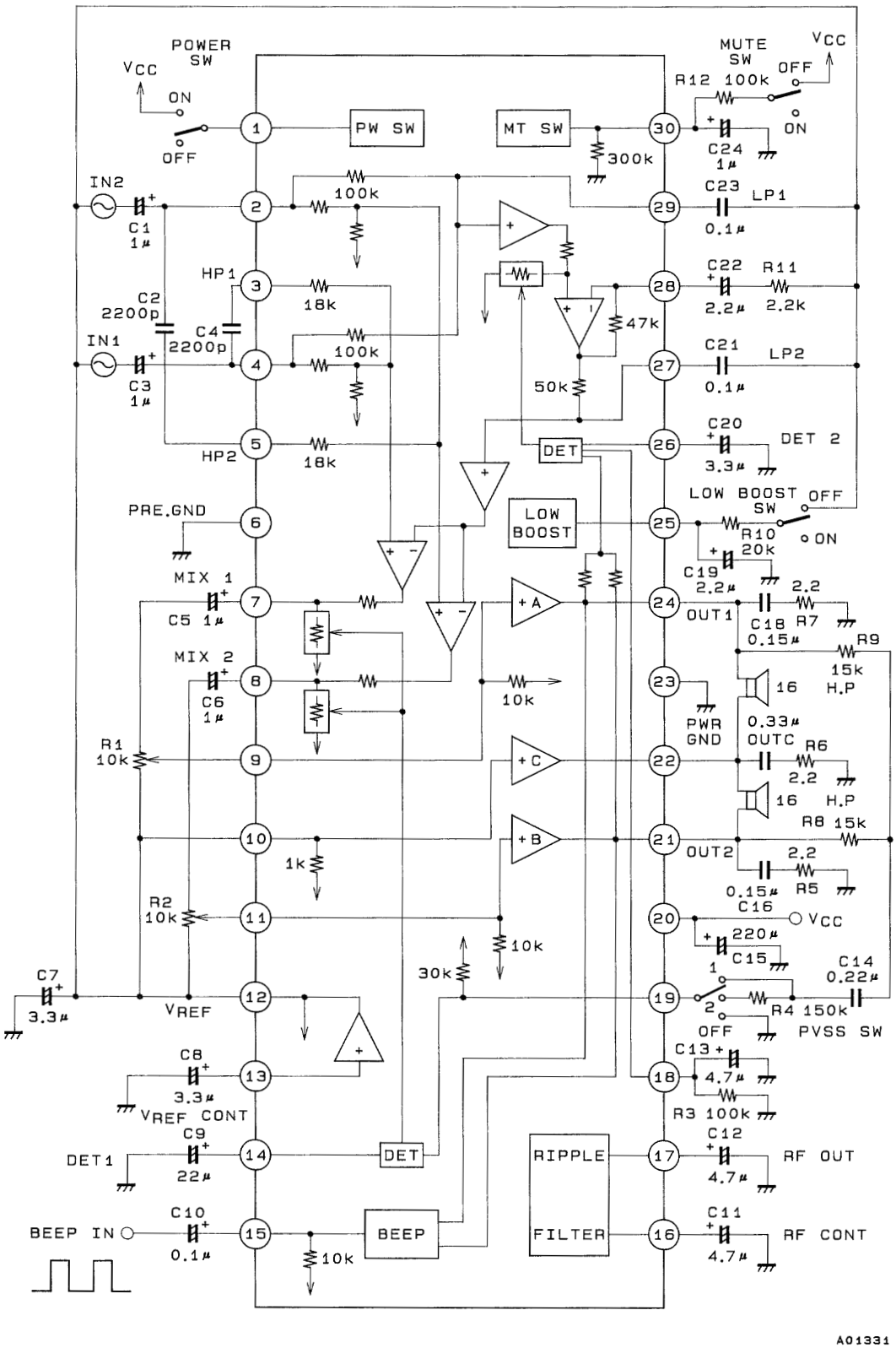


Pin Assignment and Block Diagram



Unit (resistance: Ω)

Sample Application Circuit



Unit (resistance: Ω, capacitance: F)