

1 Watt Audio Power Amplifier with Selectable Shutdown Logic Level

The LM4901 is unity-gain stable and can be configured by external gain-setting resistors.

- Improved PSRR at 217Hz & 1KHz 62dB
- Power Output at 5.0V & 1% THD 1.0W(typ.)
- Power Output at 3.0V & 1% THD 375mW(typ.)
- Shutdown Current 0.1uA(typ.)

- Available in space-saving packages: micro SMD and MSOP
- Ultra low current shutdown mode
- BTL output can drive capacitive loads
- Improved pop & click circuitry eliminates noise during turn-on and turn-off transitions
- 2.0 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Unity-gain stable
- External gain configuration capability
- User select shutdown High or Low

- Mobile Phones
- PDAs
- Portable electronic devices

The circuit diagram shows a programmable gain amplifier (PGA) with a shutdown control. The input stage consists of an audio input connected to the inverting input (-IN) of the first op-amp through a resistor R_i (20 k Ω) and a capacitor C_i (0.39 μ F). The feedback path from the output V_o to the inverting input includes a resistor R_f (20 k Ω) and a capacitor C_s (1.0 μ F). The non-inverting input (+IN) is connected to a bypass network consisting of a resistor (20 k Ω) and a capacitor C_B (1.0 μ F) to ground. The output V_o is connected to a load resistor R_L (8 Ω) to ground. The second op-amp stage is configured as a voltage follower with its non-inverting input (+) connected to $V_o/2$ and its inverting input (-) connected to the output V_o . The BIAS block provides a reference voltage $V_{DD}/2$ to the non-inverting input of the second op-amp. The shutdown control logic uses an AND gate to generate a ShutDown signal, which is connected to the ShutDown input of the BIAS block. The ShutDown signal is also connected to the Shutdown Mode input of the BIAS block. The BIAS block has two outputs: ShutDown and SD Mode. The Shutdown Mode input is connected to the SD Mode input of the BIAS block. The BIAS block is powered by V_{DD} and grounded.

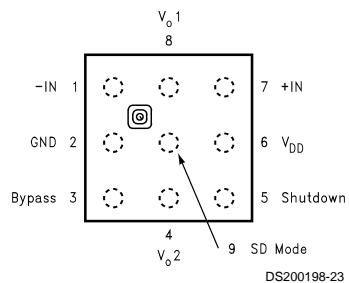
Shutdown Mode	ShutDown	Status
GND	0	Shutdown
GND	1	On
V_{DD}	0	On
V_{DD}	1	Shutdown

FIGURE 1. Typical Audio Amplifier Application Circuit

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Connection Diagrams

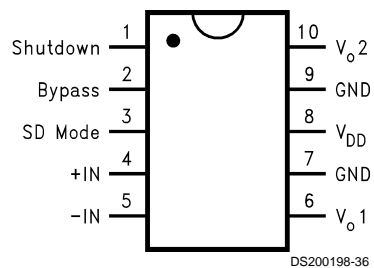
9 Bump micro SMD



Top View

Order Number LM4901IBL, LM4901IBLX
See NS Package Number BLA09AAC

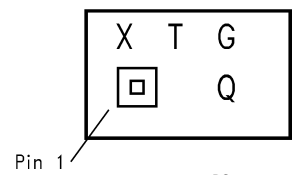
Mini Small Outline (MSOP) Package



Top View

Order Number LM4901MM
See NS Package Number MUB10A

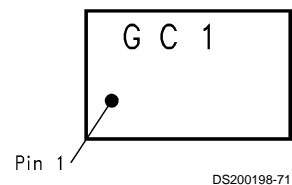
micro SMD Marking



Top View

X - Date Code
T - Die Traceability
G - Boomer Family
Q - LM4901IBL

MSOP Marking



Top View

G - Boomer Family
C1 - LM4901MM

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 11)	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to $V_{DD} + 0.3V$
Power Dissipation (Notes 3, 13)	Internally Limited
ESD Susceptibility (Note 4)	2500V
ESD Susceptibility (Note 5)	250V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (micro SMD) (Note 12)	180°C/W

 θ_{JC} (MSOP)

56°C/W

 θ_{JA} (MSOP)

190°C/W

Soldering Information

See AN-1112 'microSMD Wafers Level Chip Scale Package.'

Operating Ratings

Temperature Range

$T_{MIN} \leq T_A \leq T_{MAX}$

$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$

Supply Voltage

$2.0V \leq V_{DD} \leq 5.5V$

Electrical Characteristics $V_{DD} = 5V$ (Notes 1, 2, 8)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	LM4901		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0V, I_o = 0A$, No Load	3	7	mA (max)
		$V_{IN} = 0V, I_o = 0A$, 8 Ω Load	4	10	mA (max)
I_{SD}	Shutdown Current	$V_{SD} = V_{SD \text{ Mode}}$	0.1	2.0	μA (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD \text{ Mode}} = V_{DD}$, SD High	1.5		V (min)
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD \text{ Mode}} = V_{DD}$, SD High	1.3		V (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD \text{ Mode}} = GND$, SD Low	1.5		V (min)
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD \text{ Mode}} = GND$, SD Low	1.3		V (max)
V_{OS}	Output Offset Voltage		7	50	mV (max)
R_{OUT}	Resistor Output to GND (Note 10)		8.5	9.7	k Ω (max)
				7.0	k Ω (max)
P_o	Output Power	THD = 1% (max); $f = 1 \text{ kHz}$	1.05		W
T_{WU}	Wake-up time		100		mS (max)
THD+N	Total Harmonic Distortion+Noise	$P_o = 0.5 \text{ Wrms}$; $f = 1 \text{ kHz}$	0.2		%
PSRR	Power Supply Rejection Ratio	$V_{ripple} = 200\text{mV}$ sine p-p Input terminated with 10 Ω	60 ($f = 217\text{Hz}$) 64 ($f = 1\text{kHz}$)	55	dB (min)

Electrical Characteristics $V_{DD} = 3V$ (Notes 1, 2, 8)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	LM4901		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0V, I_o = 0A$, No Load	2	7	mA (max)
		$V_{IN} = 0V, I_o = 0A$, 8 Ω Load	3	9	mA (max)
I_{SD}	Shutdown Current	$V_{SD} = V_{SD \text{ Mode}}$	0.1	2.0	μA (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD \text{ Mode}} = V_{DD}$, SD High	1.1		V (min)
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD \text{ Mode}} = V_{DD}$, SD High	0.9		V (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD \text{ Mode}} = GND$, SD Low	1.3		V (min)
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD \text{ Mode}} = GND$, SD Low	1.0		V (max)
V_{OS}	Output Offset Voltage		7	50	mV (max)

Electrical Characteristics $V_{DD} = 3V$ (Notes 1, 2, 8)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$. (Continued)

Symbol	Parameter	Conditions	LM4901		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
R_{OUT}	Resistor Output to GND (Note 10)		8.5	9.7 7.0	k Ω (max) k Ω (max)
P_o	Output Power	THD = 1% (max); f = 1 kHz	375		mW
T_{WU}	Wake-up time		75		mS (max)
THD+N	Total Harmonic Distortion+Noise	$P_o = 0.25$ Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	$V_{ripple} = 200\text{mV}$ sine p-p Input terminated with 10 Ω	62 (f = 217Hz) 68 (f = 1kHz)	55	dB (min)

Electrical Characteristics $V_{DD} = 2.6V$ (Notes 1, 2, 8)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	LM4901		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0V$, $I_o = 0A$, No Load	2.0		mA (max)
		$V_{IN} = 0V$, $I_o = 0A$, 8 Ω Load	3.0		mA (max)
I_{SD}	Shutdown Current	$V_{SD} = V_{SD \text{ Mode}}$	0.1		μA (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD \text{ Mode}} = V_{DD}$, SD High	1.0		V (min)
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD \text{ Mode}} = V_{DD}$, SD High	0.9		V (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD \text{ Mode}} = GND$, SD Low	1.2		V (min)
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD \text{ Mode}} = GND$, SD Low	1.0		V (max)
V_{OS}	Output Offset Voltage		5	50	mV (max)
R_{OUT}	Resistor Output to GND (Note 10)		8.5	9.7 7.0	k Ω (max) k Ω (max)
P_o	Output Power (8 Ω)	THD = 1% (max); f = 1 kHz	250		mW
	(4 Ω)	THD = 1% (max); f = 1 kHz	300		
T_{WU}	Wake-up time		70		mS (max)
THD+N	Total Harmonic Distortion+Noise	$P_o = 0.15$ Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	$V_{ripple} = 200\text{mV}$ sine p-p Input terminated with 10 Ω	51 (f = 217Hz) 51 (f = 1kHz)		dB (min)

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4901, see power derating curves for additional information.

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 5: Machine Model, 220 pF–240 pF discharged through all pins.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: For micro SMD only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2 μA .

Note 9: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 10: R_{ROUT} is measured from the output pin to ground. This value represents the parallel combination of the 10k Ω output resistors and the two 20k Ω resistors.

Note 11: If the product is in Shutdown mode and V_{DD} exceeds 6V (to a max of 8V V_{DD}), then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10mA, then the device will be protected. If the device is enabled when V_{DD} is greater than 5.5V and less than 6.5V, no damage will occur, although operation life will be reduced. Operation above 6.5V with no current limit will result in permanent damage.

Application Information (Continued)

The LM4901 is unity-gain stable which gives the designer maximum system flexibility. The LM4901 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 V_{rms} are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure 1*. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection Of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100 Hz to 150 Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the LM4901 turns on. The slower the LM4901's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0 μF along with a small value of C_i (in the range of 0.1 μF to 0.39 μF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1 μF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0 μF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω Audio Amplifier

Given:

Power Output	1 W _{rms}
Load Impedance	8Ω
Input Level	1 V _{rms}
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the

Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found.

5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4901 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 2.

$$A_{VD} \geq \sqrt{(P_O R_L)} / (V_{IN}) = V_{orms} / V_{inrms} \quad (2)$$

$$R_i / R_i = A_{VD} / 2$$

From Equation 2, the minimum A_{VD} is 2.83; use A_{VD} = 3.

Since the desired input impedance was 20 kΩ, and with a A_{VD} impedance of 2, a ratio of 1.5:1 of R_i to R_i results in an allocation of R_i = 20 kΩ and R_i = 30 kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of –3 dB frequency points. Five times away from a –3 dB point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified.

$$f_L = 100 \text{ Hz} / 5 = 20 \text{ Hz}$$

$$f_H = 20 \text{ kHz} * 5 = 100 \text{ kHz}$$

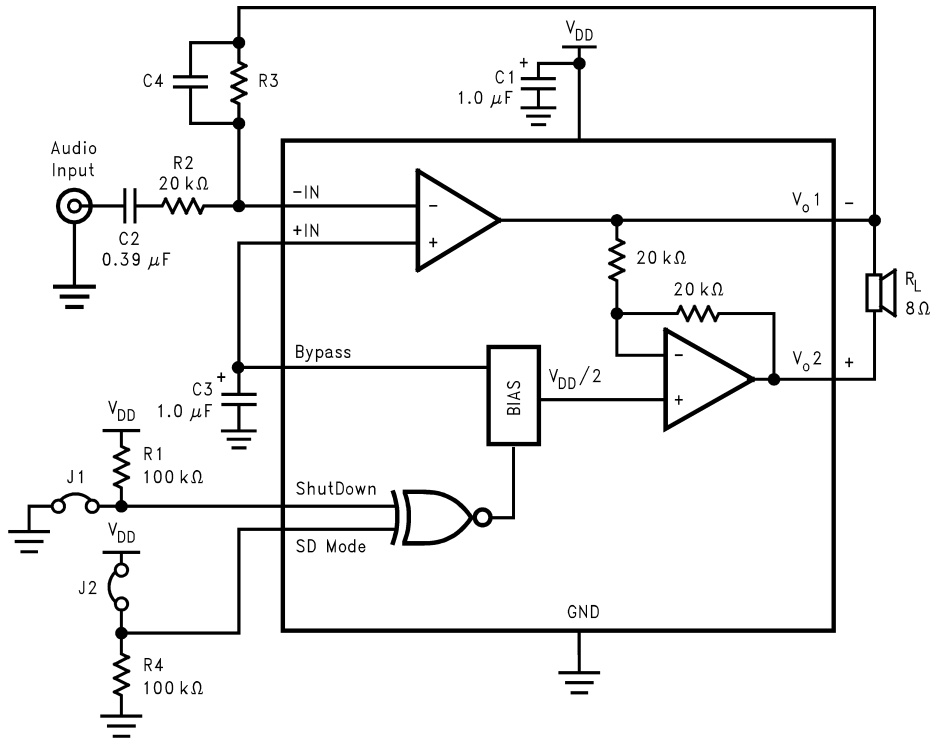
As stated in the **External Components** section, R_i in conjunction with C_i create a highpass filter.

$$C_i \geq 1 / (2\pi * 20 \text{ k}\Omega * 20 \text{ Hz}) = 0.397 \text{ }\mu\text{F}; \text{ use } 0.39 \text{ }\mu\text{F}$$

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD} = 3 and f_H = 100 kHz, the resulting GBWP = 300kHz which is much smaller than the LM4901 GBWP of 2.5MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4901 can still be used without running into bandwidth limitations.

Application Information (Continued)

HIGHER GAIN AUDIO AMPLIFIER



DS200198-24

Figure 2

The LM4901 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C_4) may be needed as shown in Figure 2 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be

taken when calculating the -3dB frequency in that an incorrect combination of R_3 and C_4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is $R_3 = 20\text{k}\Omega$ and $C_4 = 25\text{pF}$. These components result in a -3dB point of approximately 320 kHz.

Application Information (Continued)

DIFFERENTIAL AMPLIFIER CONFIGURATION FOR LM4901

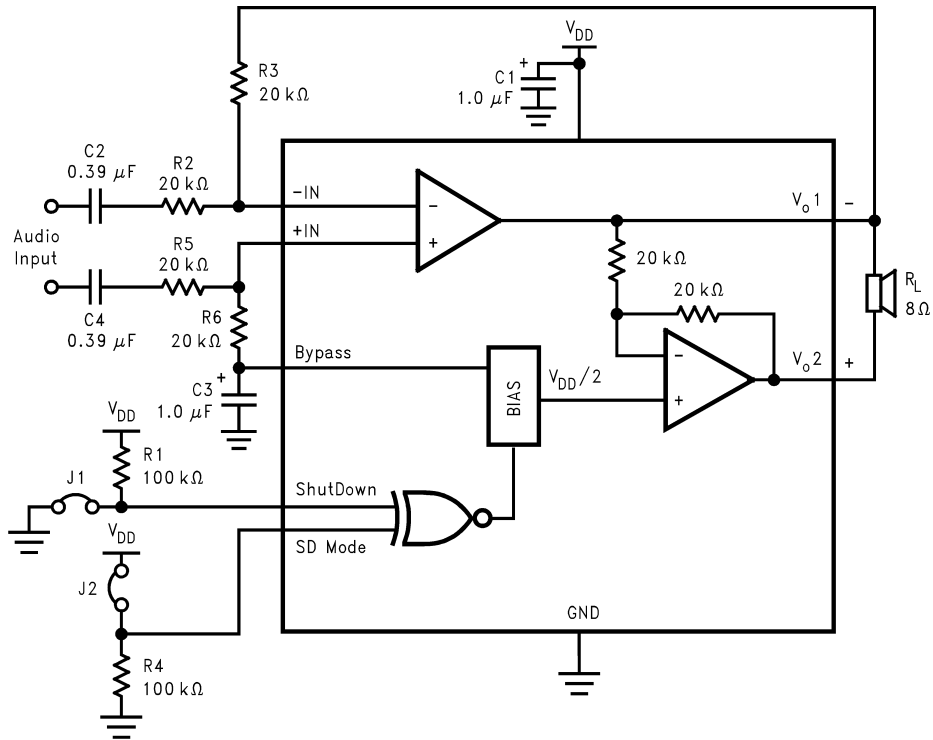
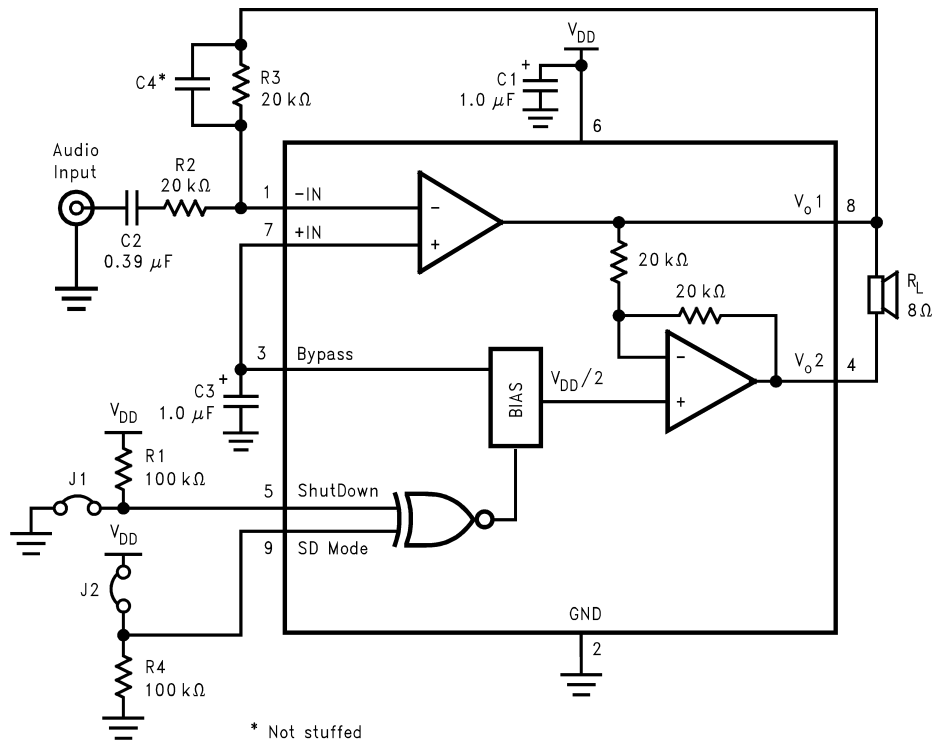


Figure 3

DS200198-29

Application Information (Continued)

REFERENCE DESIGN BOARD and LAYOUT - micro SMD



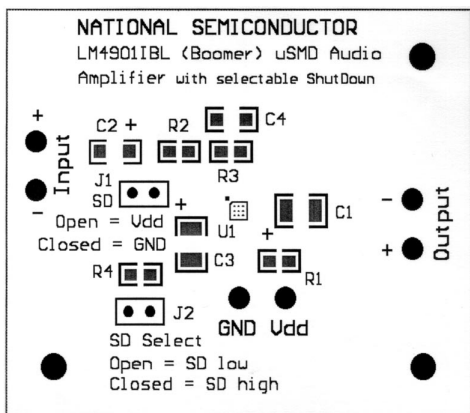
DS200198-25

Figure 4

Application Information (Continued)

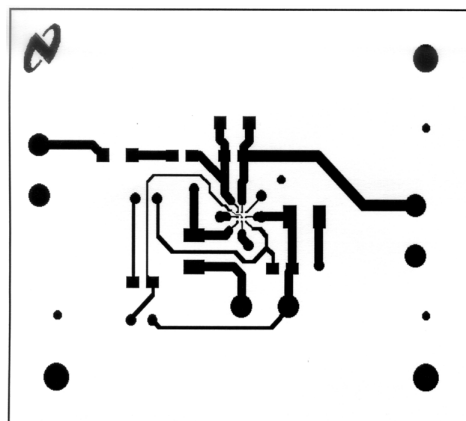
LM4901 micro SMD BOARD ARTWORK

Silk Screen



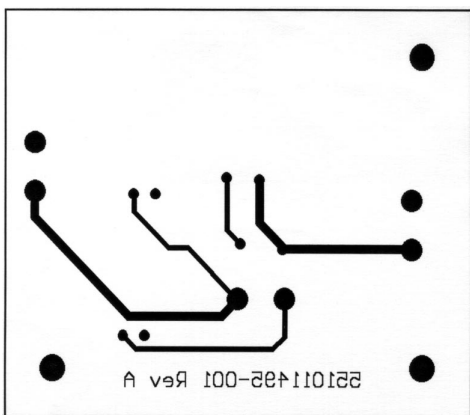
DS200198-78

Top Layer

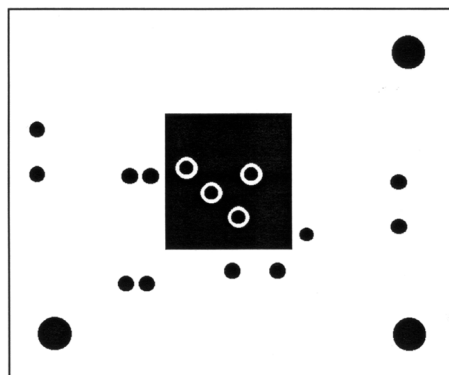


DS200198-76

Bottom Layer

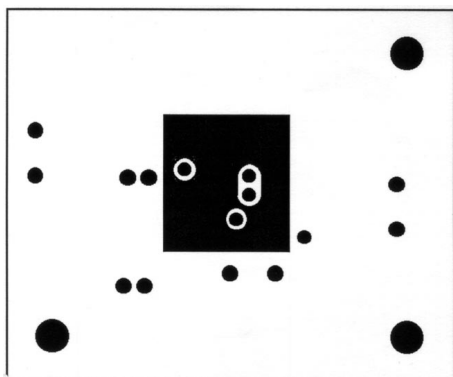


DS200198-80

Inner Layer V_{DD}

DS200198-81

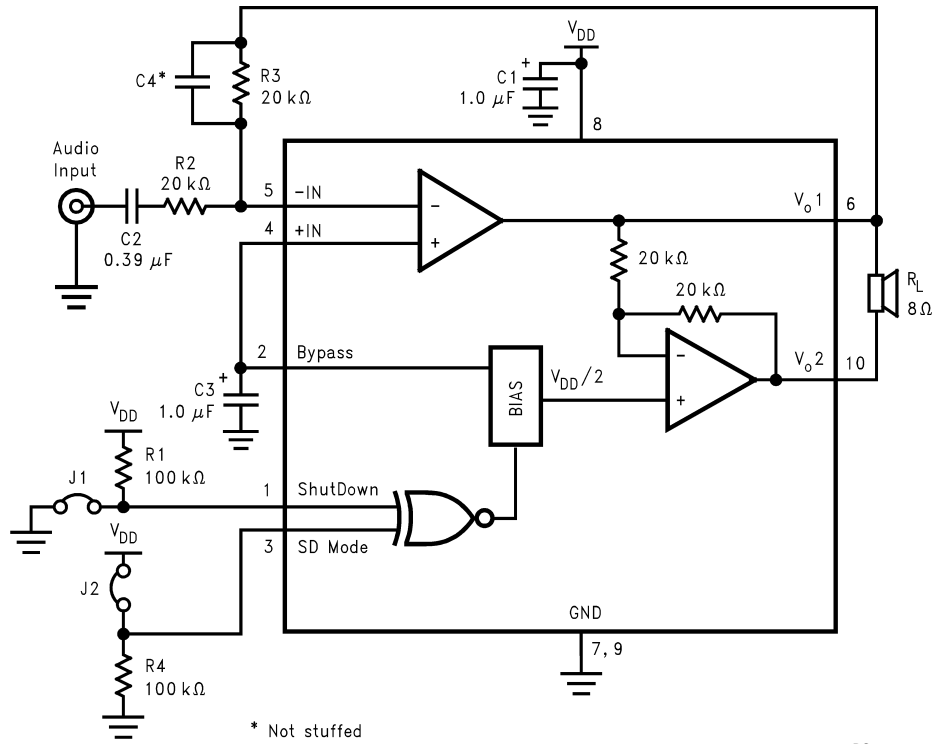
Inner Layer Ground



DS200198-82

Application Information (Continued)

REFERENCE DESIGN BOARD and PCB LAYOUT GUIDE- LINES - MSOP Boards



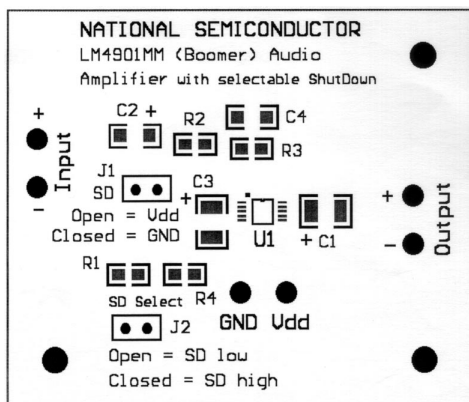
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Figure 5

Application Information (Continued)

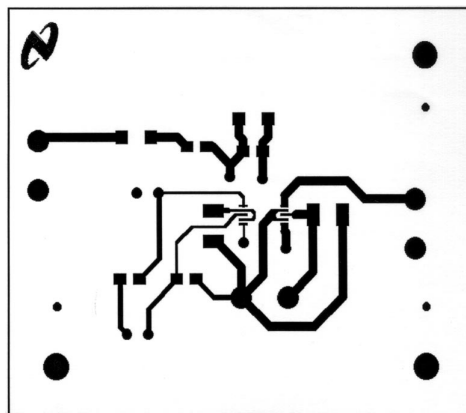
LM4901 MSOP DEMO BOARD ARTWORK

Silk Screen



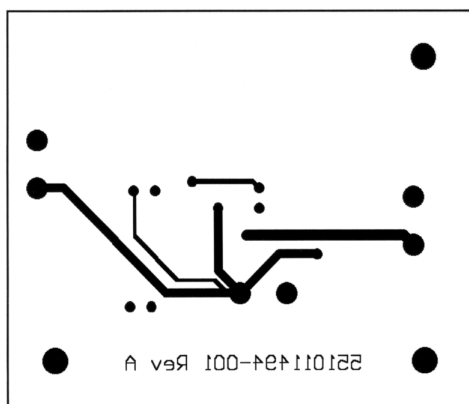
DS200198-75

Top Layer



DS200198-79

Bottom Layer



DS200198-77