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MC6850 ACIA/UART

- Designed for use in 6800-based systems
  - Precursor to 68HC11
- Device properties
  - 8 or 9 data bits
  - Even, odd, or no parity
  - 1 or 2 stop bits
  - Parity, overrun, and framing error checks
  - Internal baud clock prescaler (1, 16, 64)
  - Up to 1 MHz

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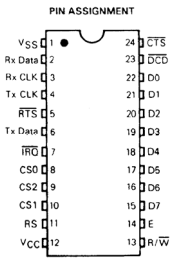
MC6850 Pin-Out



- Microprocessor pins
  - Data bus: D0-D7
  - Control: R/W, E, CS
  - Address: RS, CS
  - Other: IRQ
- EIA-232 pins
  - Data: Rx, Tx
  - Control: RTS, CTS, DCD
  - Baud Clock: Rx, Tx

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MC6850 Registers/Ports

TABLE 1 — DEFINITION OF ACIA REGISTER CONTENTS

Data Bus Line Number	Buffer Address			
	RS • $\overline{R/W}$ Transmit Data Register (Write Only)	RS • R/W Receive Data Register (Read Only)	$\overline{RS}$ • $\overline{R/W}$ Control Register (Write Only)	$\overline{RS}$ • R/W Status Register (Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear to Send ($\overline{CTS}$)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request ($\overline{IRQ}$)

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MC6850 Control

Baud Rate

CR1	CR0	Function
0	0	÷ 1
0	1	÷ 16
1	0	÷ 64
1	1	Master Reset

Framing etc.

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Special

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled.
1	1	$\overline{RTS}$ = low, Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

CR7 – Receive interrupt enable

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Other UARTs

- Wider feature set
  - 5-9 data bits
  - 1-2 stop bits in fractional steps
  - 8 or more baud rate settings
- Additional complexity
  - More than one RS pin
  - Multiple “units”

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Serial Peripheral Interface (SPI)

- Synchronous serial subsystem
  - Clock is supplied by master controller
- Allows master-slave configuration
  - Daisy-chained shift registers
- Provides higher communication speeds
  - 1 Mbit/s as master
  - 2Mbit/s as slave

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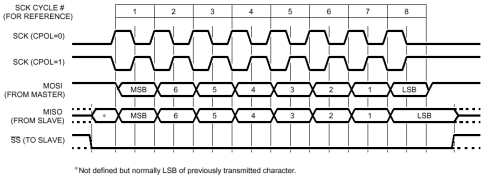
SPI Transfer Characteristic



*Not defined but normally LSB of previously transmitted character.

- SCK – Serial clock – PD4
- MISO – Master in/slave out – PD2
- MOSI – Master out/slave in – PD3
- SS – Slave select – PD5

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SPI Configuration (1)

SPCR — SPI Control Register **$1028**

	BIT 7	6	5	4	3	2	1	BIT 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

- SPE = 1: System enable
- MSTR = 1: Master selected
- CPOL: Clock polarity
  - 1 = active low (idle high)
- CPHA: Clock phase select
  - Transfer style

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SPI Configuration (2)

SPCR — SPI Control Register **$1028**

	BIT 7	6	5	4	3	2	1	BIT 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

- Data direction control
  - See DDRD, details in manual for needs
- Clocking rate (if master) SPR1,SPR0

SPR1	SPR0	E Clock Divided By
0	0	2
0	1	4
1	0	16
1	1	32

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SPI Monitoring

SPSR — SPI Status Register **$1029**

	BIT 7	6	5	4	3	2	1	BIT 0
	SPIF	WCOL	—	MODF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

- SPIE: Interrupt enable (SPCR)
  - Vector 0xFFD8,9
- SPIF: Transfer complete flag
- WCOL: Write collision
- MODF: Mode fault
  - Inconsistency detected on SS pin

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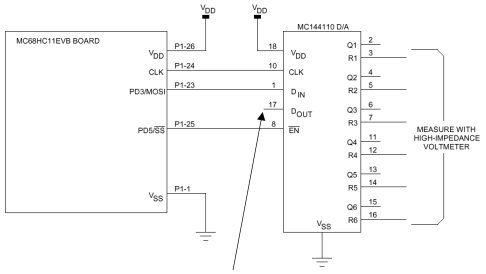
Sample SPI Wiring



Could be wired back to MISO of 68HC11 or onto another SPI device!

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Interrupt Priorities

- Based on vector address
- One can be elevated
  - PSEL3-PSEL0 (HPRIO)

PSEL3	PSEL2	PSEL1	PSEL0	Interrupt Source Promoted
0	0	0	0	Timer Overflow
0	0	0	1	Pulse Accumulator Overflow
0	0	1	0	Pulse, Accumulator Input Edge
0	0	1	1	SPI Transfer Complete
0	1	0	0	SCI Serial System
0	1	0	1	Reserved (Default to IRQ)
0	1	1	0	IRQ (External Pin or Parallel I/O)
0	1	1	1	Real-Time Interrupt
1	0	0	0	Timer Input Capture 1
1	0	1	0	Timer Input Capture 2
1	0	1	0	Timer Input Capture 3
1	0	1	1	Timer Output Compare 1
1	1	0	0	Timer Output Compare 2
1	1	0	1	Timer Output Compare 3
1	1	1	0	Timer Output Compare 4
1	1	1	1	Timer Output Compare 5

Increasing Priority

Vector Address	Interrupt Source	CCR Mask Bit	Local Mask
FFC0, C1 – FFD4, D5	Reserved	—	—
FFD6, D7	SCI Serial System*	I	
	• SCI Receive Data Register Full		RIE
	• SCI Receiver Overrun		RIE
	• SCI Transmit Data Register Empty		TIE
	• SCI Transmit Complete		TCIE
	• SCI Idle Line Detect		ILIE
FFD8, D9	SPI Serial Transfer Complete	I	SPIE
FFDA, DB	Pulse Accumulator Input Edge	I	PAII
FFDC, DD	Pulse Accumulator Overflow	I	PAOVI
FFDE, DF	Timer Overflow	I	TOI
FFE0, E1	Timer Input Capture 4/ Output Compare 5	I	I4/O5I
FFE2, E3	Timer Output Compare 4	I	OC4I
FFE4, E5	Timer Output Compare 3	I	OC3I
FFE6, E7	Timer Output Compare 2	I	OC2I
FFE8, E9	Timer Output Compare 1	I	OC1I
FFEA, EB	Timer Input Capture 3	I	IC3I
FFEC, ED	Timer Input Capture 2	I	IC2I
FFEE, EF	Timer Input Capture 1	I	IC1I
FFF0, F1	Real-Time Interrupt	I	RTII
FFF2, F3	IRQ (External Pin)	I	None
FFF4, F5	XIRQ Pin	X	None
FFF6, F7	Software Interrupt	None	None
FFF8, F9	Illegal Opcode Trap	None	None
FFFA, FB	COP Failure	None	NOCOP
FFFC, FD	Clock Monitor Fail	None	CME
FFFE, FF	RESET	None	None