SYNCHRONOUS DRAM MODULE

DESCRIPTION

The **S256M16044** is a 33,554,432 words by 64 bits SDRAM module on which 16 pieces of 32Mx4(128Mbits) SDRAM: CX133S4032TP-7B1 are assembled.
This SDRAM module provides high density and large quantities of memory in a condense space without utilizing the surface-mounting technology on the PCB.
Decoupling capacitors are mounted in places on power supply line for noise reduction.

FEATURES

- PC66/100/133- compliant
- 33,554,432 words by 64 bits organization
- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- Utilizes up to 133 MHz SDRAM components
- Non buffered
- Non-ECC pin-out
- 256Mb [32M x 64]
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Dual internal banks for hiding row access/precharge
- Programmable burst lengths; 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh modes
- Self Refresh Mode
- 64ms, 4096-cycle refresh
- All inputs, outputs and clocks LVTTL-compatible
- Serial presence detect (spd): SOIC
- Impedance control: 70Ω ±5%
- Operating Voltage: 3.15V to 3.45V

CLOCK FREQUENCY AND ACCESS TIME

CAS LATENCY	CLOCK FRQUENCY (MAX.)	CLOCK ACCESS TIME	POWER CONSUMPTION (MAX.)	
			ACTIVE	STANDBY
CL = 2	100MHz	6ns	3,744Mw	14.4mW (CMOS level input)
CL = 3	100/133MHZ	6/5.4ns	3,744Mw	

ELECTRICAL SPECIFICATIONS

- All voltages referenced to V_{SS}.
- An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured.
- V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than on third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNITS
Voltage on power supply pin relative to GND	V_{CC}	-0.5 to +4.6	V
Voltage on input pin relative to GND	V_T	-0.5 to +4.6	V
Short circuit output current	I_O	50	mA
Power dissipation	P_D	8	W
Operating ambient temperature	T_A	0 to + 70	℃
Storage temperature	T_{stg}	-55 to + 125	℃

Caution: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATIONG CONDITIONS

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS
Supply Voltage		V_{CC}	3.15	3.45	V
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	V_{CC}+0.3	V
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-0.3	+0.8	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} (all other pins not under test = 0V)	DQMB0-DQMB7	I_{I1}	-1.0	+1.0	µA
	CK0,CK2; S0#,S2#	I_{I2}	-4.0	+4.0	µA
	CKE0	I_{I3}	-8.0	+8.0	µA
	RAS#, CAS#, A0-A12, BA0, WE#	I_{I4}	-8.0	+8.0	µA
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ V_{CC})	DQ0-DQ63	I_{OZ}	-1.5	+1.5	µA
OUTPUT LEVELS Output High Voltage (I_{OUT} = -4mA)		V_{OH}	2.4	--	V
Outpuyt Low Voltage (I_{OUT} = +4mA)		V_{OL}	--	0.4	V

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

PARAMETER	SYMBOL	CONDITION		MAX	UNITS
Operating Current	I_{CC1}	Burst length = 1, $t_{RC} \geq t_{RC}$ (MIN), I_O = 0mA	CL = 3	1840	mA
			CL = 2	1760	
Precharge Standby Current in Power-Down Mode	$I_{CC2}P$	CKE ≤ V_{IL} (MAX), t_{CK} = 15ns		16	mA
	$I_{CC3}PS$	CKE ≤ V_{IL} (MAX), t_{CK} = ∞		8	mA
Precharge Standby Current in Non Power-Down Mode	$I_{CC2}N$	CKE ≥ V_{IH} (MIN), t_{CK} = 15ns, CS# ≥ V_{IH} (MIN), Input signals are changed one time during 30 ns.		320	mA
	$I_{CC2}NS$	CKE ≥ V_{IH} (MIN), t_{CK} = ∞, Input signals are stable		96	mA
Active Standby Current in Power-Down Mode	$I_{CC3}P$	CKE ≤ V_{IL} (MAX), t_{CK} = 15ns		80	mA
	$I_{CC3}PS$	CKE ≤ V_{IL} (MAX), t_{CK} = ∞		64	mA
Active Standby Current in Non Power-Down Mode	$I_{CC3}N$	CKE ≥ V_{IH} (MIN), t_{CK} = 15ns, CS# ≥ V_{IH} (MIN), Input signals are changed one time during 30 ns.		400	mA
	$I_{CC3}NS$	CKE ≥ V_{IH} (MIN), t_{CK} = ∞, Input signals are stable		192	mA
Operating Current (Burst Mode)	I_{CC4}	$t_{RC} \geq t_{CK}$ (MIN), I_O = 0mA	CL = 3	1840	mA
			CL = 2	1600	
Refresh Current	I_{CC5}		CL = 3	4320	mA
			CL = 2	4160	
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		32	mA

CAPACITANCE

PARAMETER	SYMBOL	256Mb		UNITS
		MIN	MAX	
Input Capacitance: A0-A12, BA0, RAS#, CAS#, WE#	C_{I1}	40	64	pF
Input Capacitance: CK0, CK2	C_{I2}	40	64	pF
Input Capacitance: S0#, S2#	C_{I3}	40	64	pF
Input Capacitance: CKE0	C_{I4}	40	64	pF
Input Capacitance: DQMB0#-DQMB7#	C_{I5}	40	64	pF
Data Input/Output Capacitance: DQ0-DQ63	C_{IO}	64	104	pF

AC SYNCHRONOUS CHARACTERISTICS (PC-100)

PARAMETER		SYMBOL	MIN	MAX	UNITS
Access time from CLK (positive edge)	CL = 3	t_{AC3}	--	6	ns
	CL = 2	t_{AC2}	--	6	ns
Address hold time		t_{AH}	1	--	ns
Address setup time		t_{AS}	2	--	ns
CLK high level width		t_{CH}	3	--	ns
CLK low level width		t_{CL}	3	--	ns
Clock cycle time	CL = 3	t_{CK3}	10	--	ns
	CL = 2	t_{CK2}	10	--	ns
CKE hold time		t_{CKH}	1	--	ns
CKE setup time		t_{CKS}	2	--	ns
CS#, RAS#, CAS#, WE#, DQM hold time		t_{CMH}	1	--	ns
CS#, RAS#, CAS#, WE#, DQM setup time		t_{CMS}	2	--	ns
Data-in hold time		t_{DH}	1	--	ns
Data-in setup time		t_{DS}	2	--	ns
Data-out high-impedance time	CL = 3	t_{HZ3}	3	6	ns
	CL = 2	t_{HZ2}	3	6	ns
Data-out low-impedance time		t_{LZ}	0	--	ns
Data-out hold time		t_{OH}	3	--	ns

AC ASYNCHRONOUS CHARACTERISTICS

PARAMETER		SYMBOL	MIN	MAX	UNITS
REF to REF/ACT command period		t_{RC}	70	--	ns
ACT to PRE command period		t_{RAS}	48	120,000	ns
PRE to ACT command period		t_{RP}	20	--	ns
Delay time ACT to READ/WRITE command		t_{RCD}	20	--	ns
ACT(0) to ACT(1) command period		t_{RRD}	16	--	ns
Data-in to PRE command period		t_{DPL}	8	--	ns
Data-in to ACT(REF) command period (Auto precharge)	CL = 3	t_{DAL3}	1CLK+20	--	ns
	CL = 2	t_{DAL2}	1CLK+20	--	ns
Mode register set cycle time		t_{RSC}	2	--	CLK
Transition time		t_T	0.5	30	ns
Refresh time		t_{REF}	--	64	ms

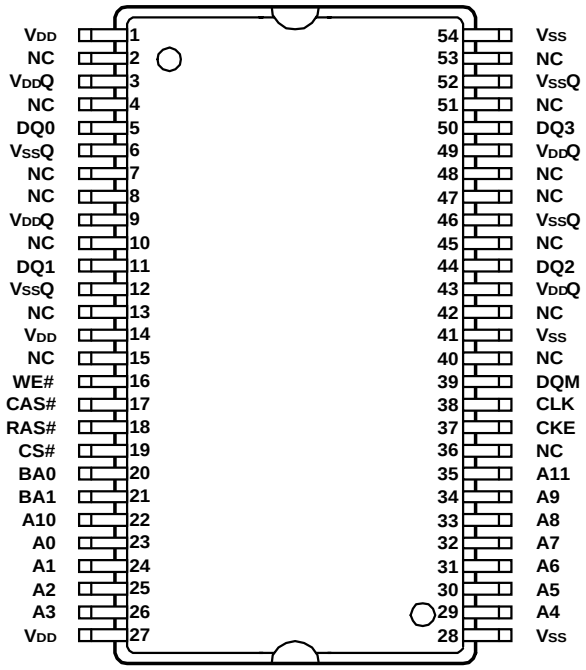
AC SYNCHRONOUS CHARACTERISTICS (PC-133)

PARAMETER		SYMBOL	MIN	MAX	UNITS
Access time from CLK (positive edge)	CL = 3	t_{AC3}	--	5.4	ns
Address hold time		t_{AH}	0.8	--	ns
Address setup time		t_{AS}	1.5	--	ns
CLK high level width		t_{CH}	2.5	--	ns
CLK low level width		t_{CL}	2.5	--	ns
Clock cycle time	CL = 3	t_{CK3}	7.5	--	ns
CKE hold time		t_{CKH}	0.8	--	ns
CKE setup time		t_{CKS}	1.5	--	ns
CS#, RAS#, CAS#, WE#, DQM hold time		t_{CMH}	0.8	--	ns
CS#, RAS#, CAS#, WE#, DQM setup time		t_{CMS}	1.5	--	ns
Data-in hold time		t_{DH}	0.8	--	ns
Data-in setup time		t_{DS}	1.5	--	ns
Data-out high-impedance time	CL = 3	t_{HZ3}	--	5.4	ns
Data-out low-impedance time		t_{LZ}	1	--	ns
Data-out hold time		t_{OH}	2.7	--	ns

AC ASYNCHRONOUS CHARACTERISTICS

PARAMETER		SYMBOL	MIN	MAX	UNITS
REF to REF/ACT command period		t_{RC}	75	--	ns
ACT to PRE command period		t_{RAS}	44	120,000	ns
PRE to ACT command period		t_{RP}	20	--	ns
Delay time ACT to READ/WRITE command		t_{RCD}	20	--	ns
ACT(0) to ACT(1) command period		t_{RRD}	66	--	ns
Data-in to PRE command period		t_{DPL}	8	--	ns
Data-in to ACT(REF) command period (Auto precharge)	CL = 3	t_{DAL3}	1CLK+20	--	ns
	CL = 2	t_{DAL2}	1CLK+20	--	ns
Mode register set cycle time		t_{RSC}	2	--	CLK
Transition time		t_T	0.3	1.2	ns
Refresh time		t_{REF}	--	64	ms

PIN ASSIGNMENT FOR 32M x 4 SDRAM 54-Pin TSOP CHIP (TOP VIEW)



Note: The # symbol indicates signal is active LOW

DIMENSIONS, ASSEMBLY DRAWING (TOP & BOTTOM) FOR TYPICAL NON-ECC MODULE

Figure 1 shows the placement of all the components on top layer of **S256M16044** 256MByte non-ECC module.

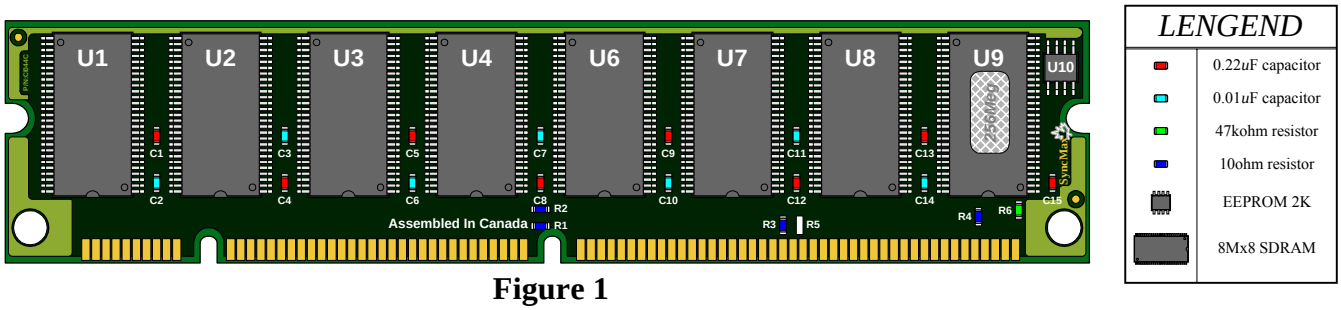


Figure 1
TOP VIEW

Figure 2 shows the dimensions of, the copper pool on bottom layer & side view of **S256M16044** 256MByte non-ECC module.

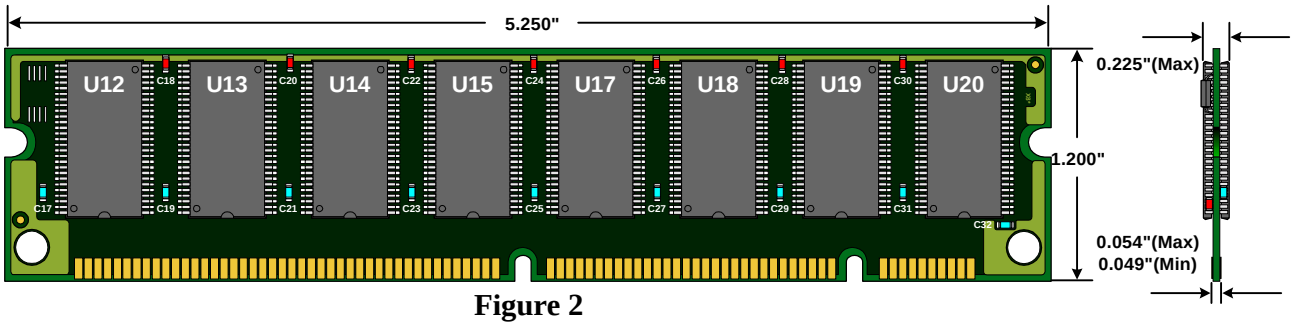


Figure 2

BOTTOM VIEW **SIDE VIEW**

Assembly Note For S256M16044 256Mb Double-Sided Module:

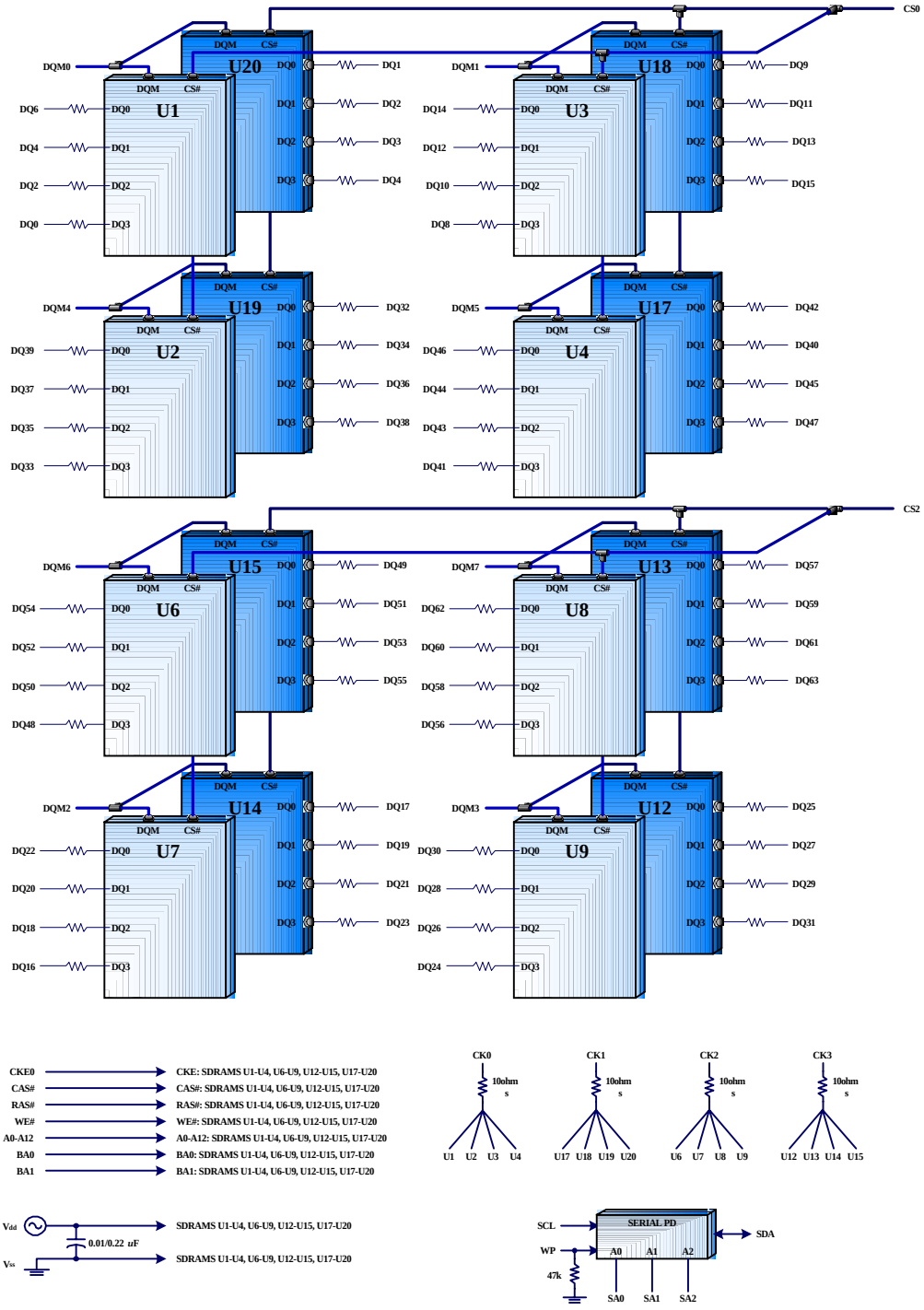
- Place all components indicated on Figure 1and 2.

BILL OF MATERIALS FOR 256Mb

For a typical 32Mx64 256Mb module, the PCB will contain the following components:

	Component Name	Part No.	Reference	Qty.
•	SDRAM, SSOP54_8MM_400	CX133S4032TP-XXX	U1-U9, U12-U20	16
•	0.22µF, SMC0603	06035C103KAT2A	C1-C16	16
•	0.01µF SMC0603	C1608Y5V1C224Z	C17-C32	16
•	10Ω ±10%, SMR0603	MCR03EZHJ100	R1-R4	4
•	47kΩ ±5%, SMR0603	807065R047.000K	R6	1
•	EEPROM 2K, SOI8	24C02N	U10	1

FUNCTIONAL BLOCK DIAGRAM
(32Mx4 CHIPS NON-ECC)



PIN ASSIGNMENT FOR 168-PIN SDRAM DIMM

PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	S0#	58	DQ19	86	DQ32	114	S1#	142	DQ51
3	DQ1	31	NC	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	NC	90	Vdd	118	A3	146	NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	S2#	73	Vss	101	DQ45	129	S3#	157	Vdd
18	Vdd	46	DQMB2	74	DQ28	102	Vdd	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	NC	160	DQ62
21	NC	49	Vdd	77	DQ31	105	NC	133	Vdd	161	DQ63
22	NC	50	NC	78	Vss	106	NC	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	WP	109	NC	137	NC	165	SA0
26	Vdd	54	Vss	82	SDA	110	Vdd	138	Vss	166	SA1
27	WE#	55	DQ16	83	SCL	111	CAS	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vdd	112	DQMB4	140	DQ49	168	Vdd

SERIAL PRESENCE-DETECT CHART (PC-100)

BYTE #	FUNCTION	SUPPORTED	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	HEX
0	# of bytes used	128 bytes	1	0	0	0	0	0	0	0	80h
1	Total SPD memory size	256 bytes	0	0	0	0	1	0	0	0	08h
2	Memory type	SDRAM	0	0	0	0	0	1	0	0	04h
3	# of row address	12	0	0	0	0	1	1	0	0	0Ch
4	# of column address	11 (8Mx4x4)	0	0	0	0	1	0	1	1	0Bh
5	# of banks	1 bank	0	0	0	0	0	0	0	1	01h
6	Data width	64 bits	0	1	0	0	0	0	0	0	40h
7	Data width (continued)	Not used	0	0	0	0	0	0	0	0	00h
8	Modules I/F levels	LVTTL (3.3V)	0	0	0	0	0	0	0	1	01h
9	SDRAM cycle time	8ns (-8)	1	0	0	0	0	0	0	0	80h
10	SDRAM access time	6ns (-8)	0	1	1	0	0	0	0	0	60h
11	Module config. type	Non-parity	0	0	0	0	0	0	0	0	00h
12	Refresh rate/type	15.625 µs	1	0	0	0	0	0	0	0	80h
13	SDRAM width	X4	0	0	0	0	0	1	0	0	04h
14	SDRAM device attributes	None	0	0	0	0	0	0	0	0	00h
15	Min. clock delay	t_{ccd} = 1 CLK	0	0	0	0	0	0	0	1	01h
16	SDRAM burst length	1, 2, 4, 8 & F	1	0	0	0	1	1	1	1	8Fh
17	# of banks on SDRAM	4 banks	0	0	0	0	0	1	0	0	02h
18	CAS latency	2 & 3	0	0	0	0	0	1	1	0	06h
19	CS latency	= 0	0	0	0	0	0	0	0	1	01h
20	Write latency	= 0	0	0	0	0	0	0	0	1	01h
21	SDRAM mod. Attributes	Non-buffered	0	0	0	0	0	0	0	0	00h
22	SDRAM dev. Attributes	14	0	0	0	0	1	1	1	0	0Eh
23	SDRAM cycle time (2nd)	192	1	0	1	0	0	0	0	0	A0h
24	SDRAM access from clk	96	0	1	1	0	0	0	0	0	60h
25	SDRAM cycle time (3rd)	0	0	0	0	0	0	0	0	0	00h
26	SDRAM access from clk	0	0	0	0	0	0	0	0	0	00h
27	Min. row precharge time	20	0	0	0	1	0	1	0	0	14h
28	Min. row active to row active	16	0	0	0	1	0	0	0	0	10h
29	Min. RAS to CAS delay	20	0	0	0	1	0	1	0	0	14h
30	Min. RAS pulse width	30	0	0	1	1	0	0	0	0	30h
31	Density of each bank on mod	256Mb	0	1	0	0	0	0	0	0	40h

SERIAL PRESENCE-DETECT CHART (PC-100) (continued)

BYTE #	FUNCTION	SUPPORTED	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	HEX
32	Command & address signal input setup time	2	0	0	1	0	0	0	0	0	20h
33	Command & address signal input hold time	1	0	0	0	1	0	0	0	0	10h
34	Data signal input setup time	2	0	0	1	0	0	0	0	0	20h
35	Data signal input hold time	1	0	0	0	1	0	0	0	0	10h
36-61	Superset info	--	0	0	0	0	0	0	0	0	00h
62	SPD rev. code	0	0	0	0	0	0	0	0	0	00h
63	Checksum (byte 0-62)	0	0	0	0	0	0	0	0	0	00h
64-71	Manufacture's JEDEC ID code	--	--	--	--	--	--	--	--	--	--
72	Manufacturing location	--	--	--	--	--	--	--	--	--	--
73-90	Manufacture's P/N	--	--	--	--	--	--	--	--	--	--
91-92	Revision code	--	--	--	--	--	--	--	--	--	--
93-94	Manufacturing date	--	--	--	--	--	--	--	--	--	--
95-98	Assembly serial number	--	--	--	--	--	--	--	--	--	--
99-125	Mfg specific	--	--	--	--	--	--	--	--	--	--
126	Intel specification frequency	100MHz	0	1	1	0	0	1	0	0	64h
127	Intel specification /CAS latency support	--	1	0	1	0	0	1	1	1	A7h

Note: The above SPD information is for reference only, since some of the timing information depends on the memory chips used.

SERIAL PRESENCE-DETECT CHART (PC-133)

BYTE #	FUNCTION	SUPPORTED	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	HEX
0	# of bytes used	128 bytes	1	0	0	0	0	0	0	0	80h
1	Total SPD memory size	256 bytes	0	0	0	0	1	0	0	0	08h
2	Memory type	SDRAM	0	0	0	0	0	1	0	0	04h
3	# of row address	12	0	0	0	0	1	1	0	0	0Ch
4	# of column address	11 (8Mx4x4)	0	0	0	0	1	0	1	1	0Bh
5	# of banks	1 bank	0	0	0	0	0	0	0	1	01h
6	Data width	64 bits	0	1	0	0	0	0	0	0	40h
7	Data width (continued)	Not used	0	0	0	0	0	0	0	0	00h
8	Modules I/F levels	LVTTL (3.3V)	0	0	0	0	0	0	0	1	01h
9	SDRAM cycle time	7.5ns (-75)	0	1	1	1	0	1	0	1	75h
10	SDRAM access time	5.4ns (-54)	0	1	1	0	0	1	0	0	54h
11	Module config. type	Non-parity	0	0	0	0	0	0	0	0	00h
12	Refresh rate/type	15.625 µs	1	0	0	0	0	0	0	0	80h
13	SDRAM width	X4	0	0	0	0	0	1	0	0	04h
14	SDRAM device attributes	None	0	0	0	0	0	0	0	0	00h
15	Min. clock delay	t_{ccd} = 1 CLK	0	0	0	0	0	0	0	1	01h
16	SDRAM burst length	1, 2, 4, 8 & F	1	0	0	0	1	1	1	1	8Fh
17	# of banks on SDRAM	4 banks	0	0	0	0	0	1	0	0	02h
18	CAS latency	2 & 3	0	0	0	0	0	1	1	0	06h
19	CS latency	= 0	0	0	0	0	0	0	0	1	01h
20	Write latency	= 0	0	0	0	0	0	0	0	1	01h
21	SDRAM mod. Attributes	Non-buffered	0	0	0	0	0	0	0	0	00h
22	SDRAM dev. Attributes	14	0	0	0	0	1	1	1	0	0Eh
23	SDRAM cycle time (2nd)	192	1	0	1	0	0	0	0	0	A0h
24	SDRAM access from clk	96	0	1	1	0	0	0	0	0	60h
25	SDRAM cycle time (3rd)	0	0	0	0	0	0	0	0	0	00h
26	SDRAM access from clk	0	0	0	0	0	0	0	0	0	00h
27	Min. row precharge time	20	0	0	0	1	0	1	0	0	14h
28	Min. row active to row active	15	0	0	0	0	1	1	1	1	0fh
29	Min. RAS to CAS delay	20	0	0	0	1	0	1	0	0	14h
30	Min. RAS pulse width	30	0	0	1	0	1	1	0	1	2dh
31	Density of each bank on mod	256Mb	0	1	0	0	0	0	0	0	40h

SERIAL PRESENCE-DETECT CHART (PC-133) (continued)

BYTE #	FUNCTION	SUPPORTED	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	HEX
32	Command & address signal input setup time	1.5	0	0	0	1	0	1	0	1	15h
33	Command & address signal input hold time	0.8	0	0	0	0	1	0	0	0	08h
34	Data signal input setup time	1.5	0	0	0	1	0	1	0	1	15h
35	Data signal input hold time	0.8	0	0	0	0	1	0	0	0	08h
36-61	Superset info	--	0	0	0	0	0	0	0	0	00h
62	SPD rev. code	0	0	0	0	0	0	0	0	0	00h
63	Checksum (byte 0-62)	0	0	0	0	0	0	0	0	0	00h
64-71	Manufacture's JEDEC ID code	--	--	--	--	--	--	--	--	--	--
72	Manufacturing location	--	--	--	--	--	--	--	--	--	--
73-90	Manufacture's P/N	--	--	--	--	--	--	--	--	--	--
91-92	Revision code	--	--	--	--	--	--	--	--	--	--
93-94	Manufacturing date	--	--	--	--	--	--	--	--	--	--
95-98	Assembly serial number	--	--	--	--	--	--	--	--	--	--
99-125	Mfg specific	--	--	--	--	--	--	--	--	--	--
126	Intel specification frequency	100MHz	0	1	1	0	0	1	0	0	64h
127	Intel specification /CAS latency support	--	1	0	1	0	0	1	1	1	A7h

Note: The above SPD information is for reference only, since some of the timing information depends on the memory chips used.