CD4071B, CD4072B, CD4075B Types

CMOS OR Gates

High-Voltage Types (20-Volt Rating)

CD4071B Quad 2-Input OR Gate
CD4072B Dual 4-Input OR Gate
CD4075B Triple 3-Input OR Gate

■ CD4071B, CD4072B, and CD4075B OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of CMOS gates. The CD4071, CD4072, and CD4075 types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

■ Medium-Speed Operation-t_{PLH}, t_{PHL} = 60 ns (typ.) at V_{DD} = 10 V
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Standardized, symmetrical output characteristics
■ Noise margin (over full package temperature range)
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

CD4071B
FUNCTIONAL DIAGRAM

CD4072B
FUNCTIONAL DIAGRAM
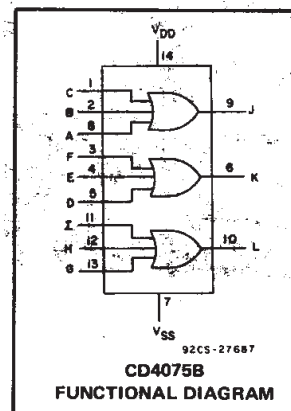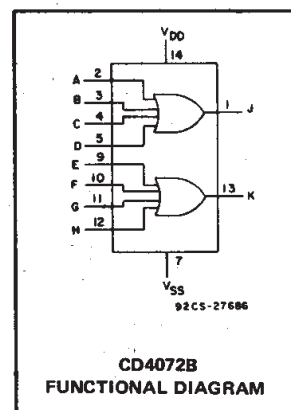

CD4075B
FUNCTIONAL DIAGRAM
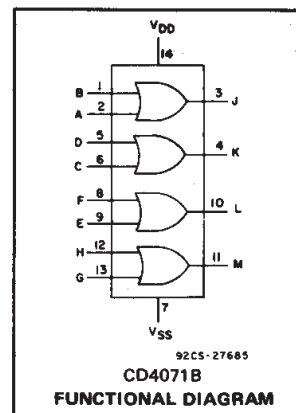
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER-ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	4.5	–	5	3.5				3.5	–	–	
	9	–	10	7				7	–	–	
	13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	±10^{-5}	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

   Voltages referenced to V_{SS} Terminal) . . . . −0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT . . . . ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

   For T_A = −55°C to +100°C 500mW

   For T_A = +100°C to +125°C . . . . Derate Linearity at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

   FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) . . . . −55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

   At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max . . . . +265°C
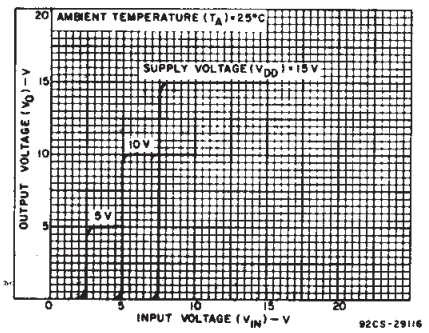
Fig. 1 — Typical voltage transfer characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS			UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF
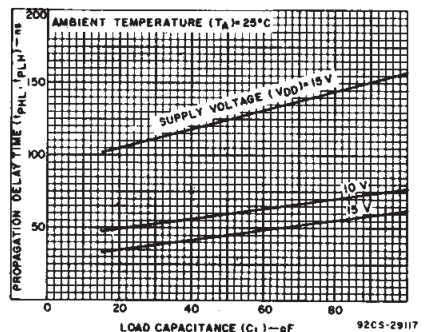
Fig. 2 — Typical propagation delay time as a function of load capacitance.

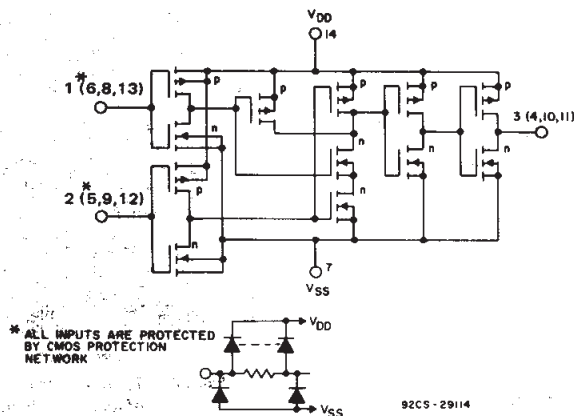* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

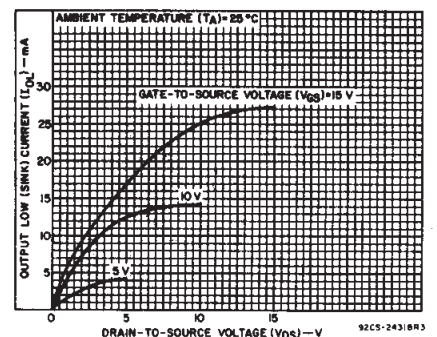Fig. 3 — Schematic diagram for CD4071B (1 of 4 identical gates).

Fig. 4 — Typical output low (sink) current characteristics.

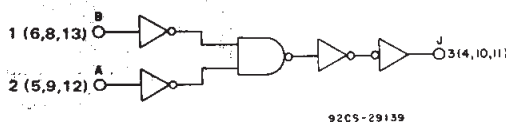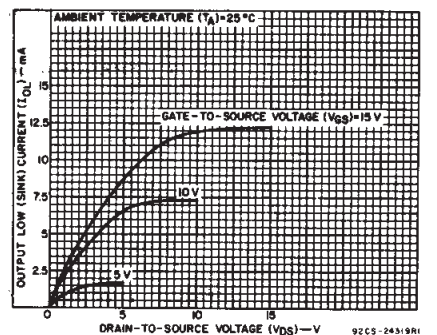Fig. 5 — Logic diagram for CD4071B (1 of 4 identical gates).

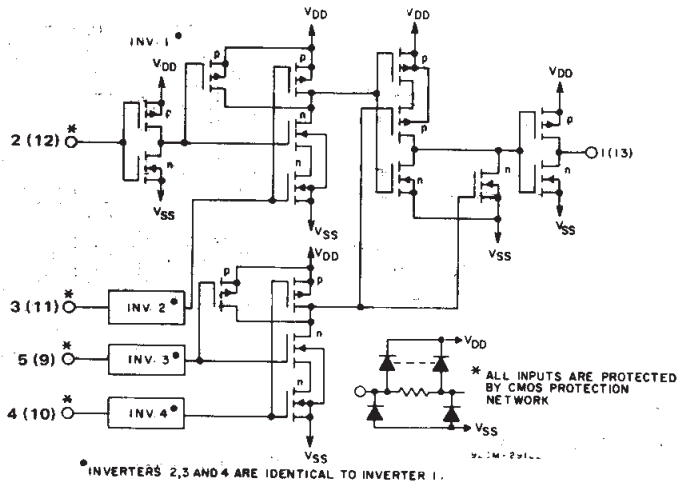Fig. 6 — Minimum output low (sink) current characteristics.

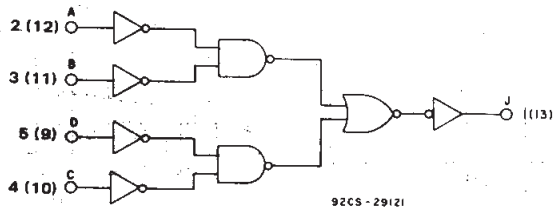Fig. 7 — Schematic diagram for CD4072B (1 of 2 identical gates).

*INVERTERS 2, 3 AND 4 ARE IDENTICAL TO INVERTER 1.

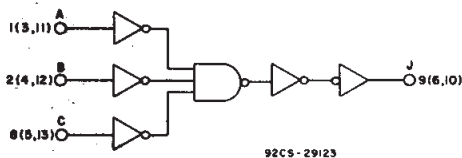* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

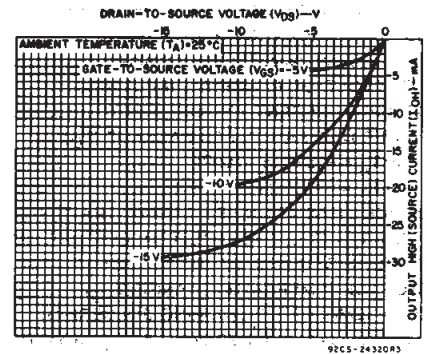
Fig. 9 — Logic diagram for CD4072B (1 of 2 identical gates).

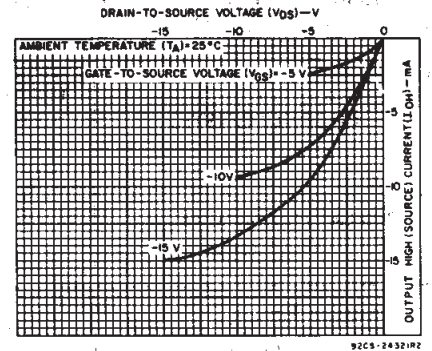Fig. 8 — Typical output high (source) current characteristics.

Fig. 10 — Minimum output high (source) current characteristics.
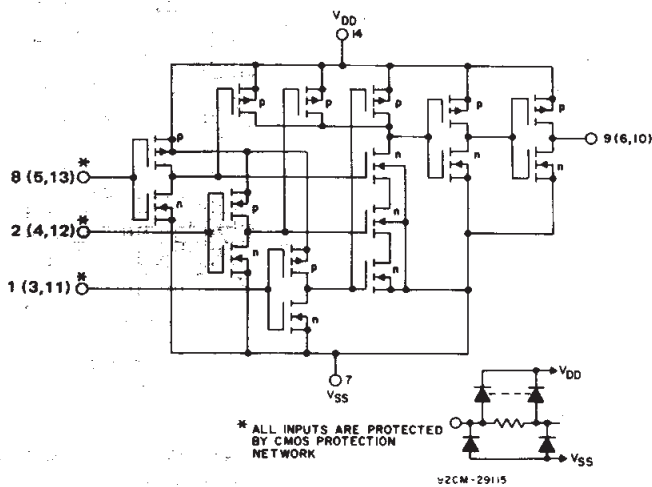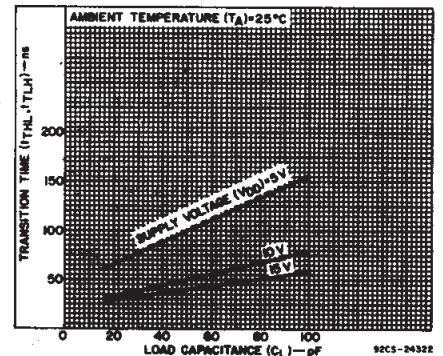

Fig. 11 — Schematic diagram for CD4075B (1 of 3 identical gates).

* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

Fig. 13 — Logic diagram for CD4075B (1 of 3 identical gates).

Fig. 12 — Typical transition time as a function of load capacitance.
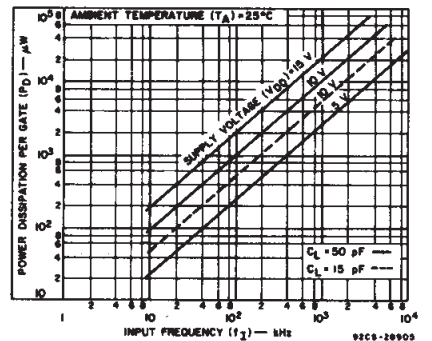
Fig. 14 — Typical dynamic power dissipation as a function of frequency.

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TERMINAL ASSIGNMENTS (TOP VIEW)

CD4071B
92CS-24494
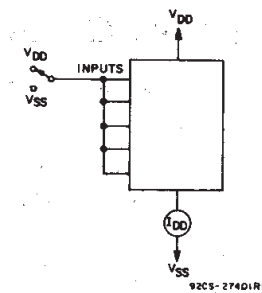

CD4072B
NC = NO CONNECTION 92CS-24496R2
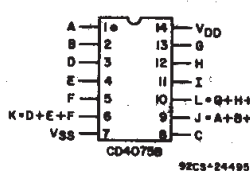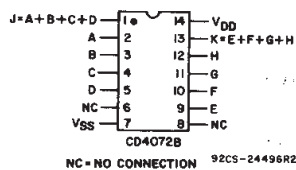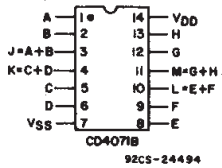

CD4075B
92CS-24495

Fig. 15 — Quiescent device current test circuit.
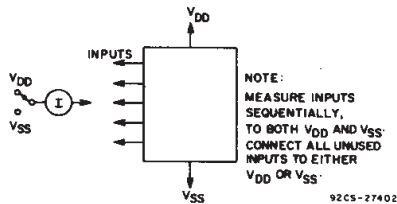
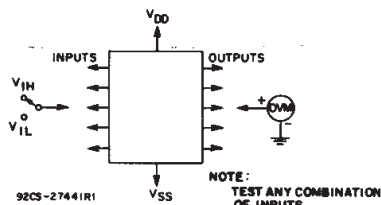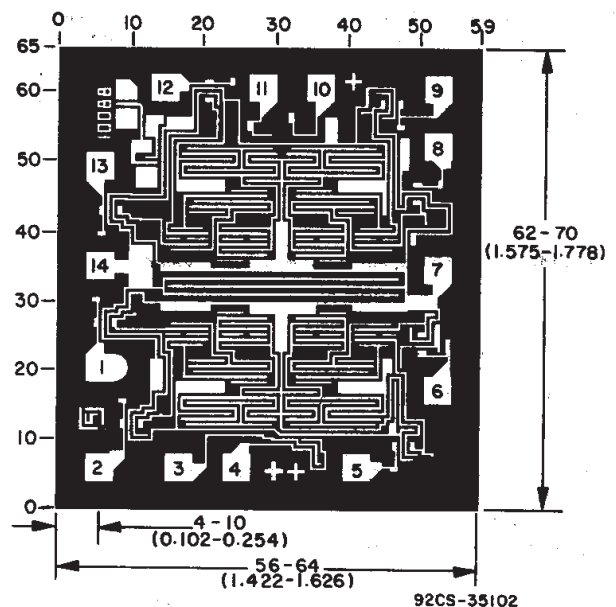*Fig. 16 — Input current test circuit.*

NOTE:
MEASURE INPUTS SEQUENTIALLY, TO BOTH V_{DD} AND V_{SS}. CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}.

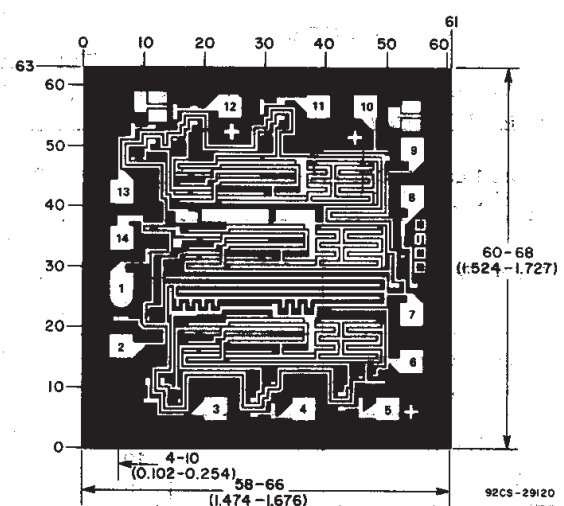*Fig. 17 — Input-voltage test circuit.*

NOTE: TEST ANY COMBINATION OF INPUTS

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Chip dimensions and pad layout for CD4071B.
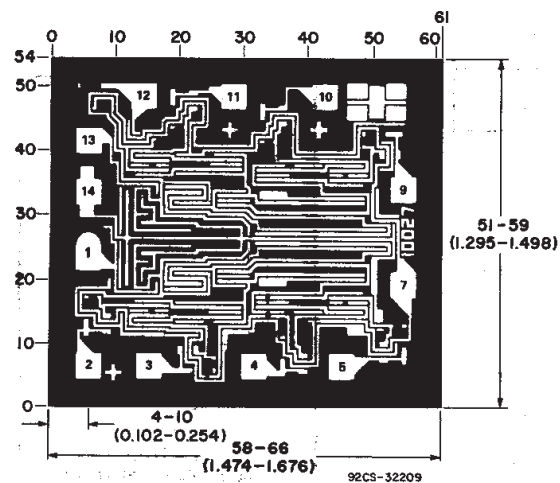
Chip dimensions and pad layout for CD4072B.

Chip dimensions and pad layout for CD4075B.

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