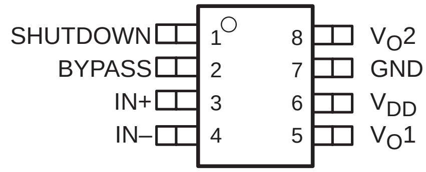
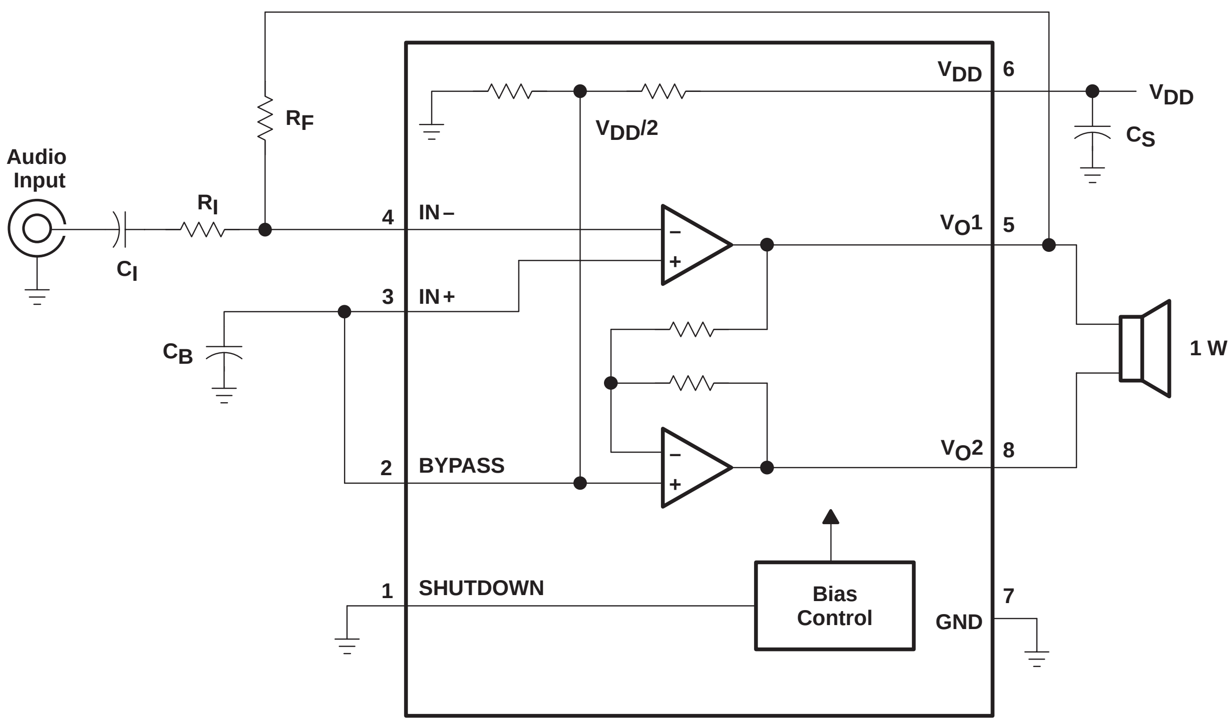
- **1-W BTL Output (5 V, 0.11 % THD+N)**
- **3.3-V and 5-V Operation**
- **No Output Coupling Capacitors Required**
- **Shutdown Control (I_{DD} = 0.6 μA)**
- **Uncompensated Gains of 2 to 20 (BTL Mode)**
- **Surface-Mount Packaging**
- **Thermal and Short-Circuit Protection**
- **High Supply Ripple Rejection Ratio (56 dB at 1 kHz)**
- **LM4861 Drop-In Compatible**

D PACKAGE
(TOP VIEW)



description

The TPA4861 is a bridge-tied load (BTL) audio power amplifier capable of delivering 1 W of continuous average power into an 8-Ω load at 0.2% THD+N from a 5-V power supply in voiceband frequencies (f < 5 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output in most applications. Gain is externally configured by means of two resistors and does not require compensation for settings of 2 to 20. Features of the amplifier are a shutdown function for power-sensitive applications as well as internal thermal and short-circuit protection. The TPA4861 works seamlessly with TI's TPA4860 in stereo applications. The amplifier is available in an 8-pin SOIC surface-mount package that reduces board space and facilitates automated assembly.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE SMALL OUTLINE† (D)
–40°C to 85°C	TPA4861D

† The D package is available tape and reeled. To order a tape and reeled part, add the suffix R to the part number (e.g., TPA4861DR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	2	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1 µF – 1.0 µF capacitor when used as an audio power amplifier.
GND	7		GND is the ground connection.
IN–	4	I	IN– is the inverting input. IN– is typically used as the audio input terminal.
IN+	3	I	IN+ is the noninverting input. IN+ is typically tied to the BYPASS terminal.
SHUTDOWN	1	I	SHUTDOWN places the entire device in shutdown mode when held high ($I_{DD} \le 0.6\ \mu A$).
V_O1	5	O	V_O1 is the positive BTL output.
V_O2	8	O	V_O2 is the negative BTL output.
V_{DD}	6		V_{DD} is the supply voltage terminal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{DD} . . . . 6 V
Input voltage, V_I . . . . –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation . . . . Internally Limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2.7	5.5	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	1.25	2.7	V
	V_{DD} = 5 V	1.25	4.5	V
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPA4861			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1			20	mV
PSRR	Power supply rejection ratio ($\Delta V_{DD} / \Delta V_{OO}$)	V_{DD} = 3.2 V to 3.4 V		75		dB
I_{DD}	Supply current			2.5		mA
$I_{DD(SD)}$	Supply current, shutdown			0.6		μA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4861			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = –2 V/V		400		mW
			THD = 2%, f = 1 kHz, A_V = –2 V/V		500		mW
B_{OM}	Maximum output power bandwidth		Gain = –10 V/V, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection ratio	BTL	f = 1 kHz, C_B = 0.1 μF		56		dB
		SE	f = 1 kHz, C_B = 0.1 μF		30		dB
V_n	Noise output voltage, see Note 3		Gain = –2 V/V		20		μV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

electrical characteristics at specified free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	TPA4861			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1			20	mV
PSRR	Power supply rejection ratio ($\Delta V_{DD} / \Delta V_{OO}$)	V_{DD} = 4.9 V to 5.1 V		70		dB
I_{DD}	Supply current			3.5		mA
$I_{DD(SD)}$	Supply current, shutdown			0.6		μA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristic, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4861			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = –2 V/V		1000		mW
			THD = 2%, f = 1 kHz, A_V = –2 V/V		1100		mW
B_{OM}	Maximum output power bandwidth		Gain = –10 V/V, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection ratio	BTL	f = 1 kHz, C_B = 0.1 μF		56		dB
		SE	f = 1 kHz, C_B = 0.1 μF		30		dB
V_n	Noise output voltage, see Note 3		Gain = –2 V/V		20		μV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OO}	Output offset voltage	Distribution	1,2
I_{DD}	Supply current distribution	vs Free-air temperature	3,4
THD+N	Total harmonic distortion plus noise	vs Frequency	5,6,7,8,9, 10,11,15, 16,17,18
		vs Output power	12,13,14, 19,20,21
I_{DD}	Supply current	vs Supply voltage	22
V_n	Output noise voltage	vs Frequency	23,24
	Maximum package power dissipation	vs Free-air temperature	25
	Power dissipation	vs Output power	26,27
	Maximum power output	vs Free-air temperature	28
	Output power	vs Load resistance	29
		vs Supply voltage	30
	Open-loop gain	vs Frequency	31
k_{SVR}	Supply ripple rejection ratio	vs Frequency	32,33

TYPICAL CHARACTERISTICS

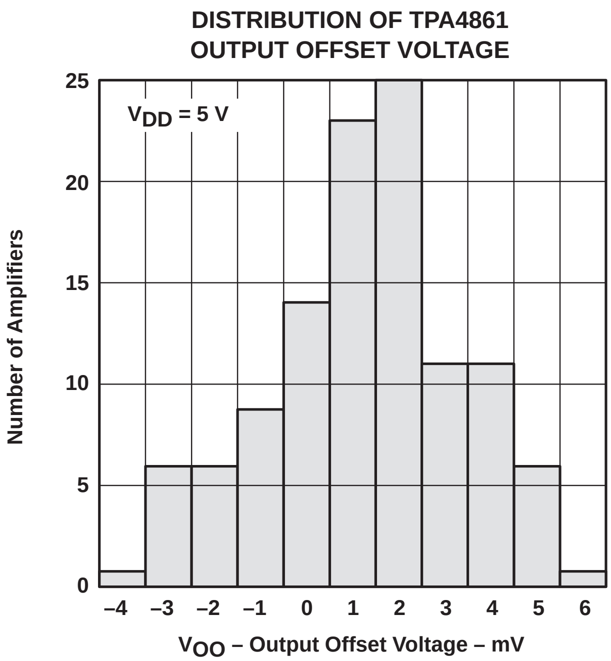


Figure 1

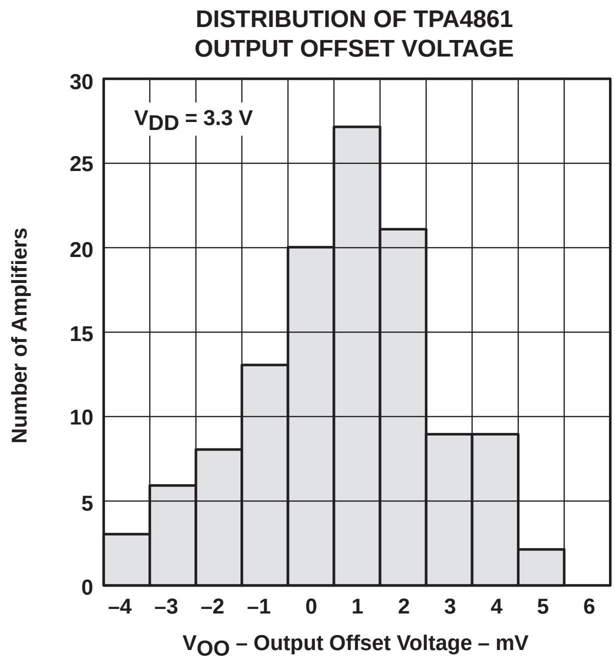


Figure 2

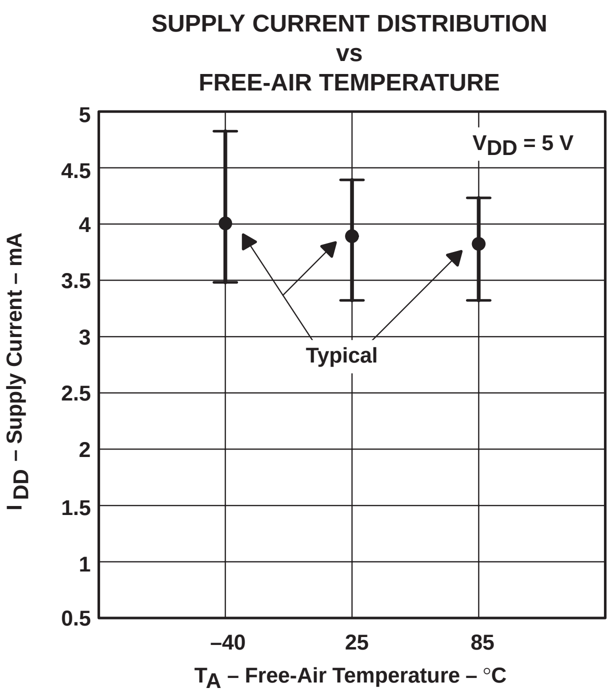


Figure 3

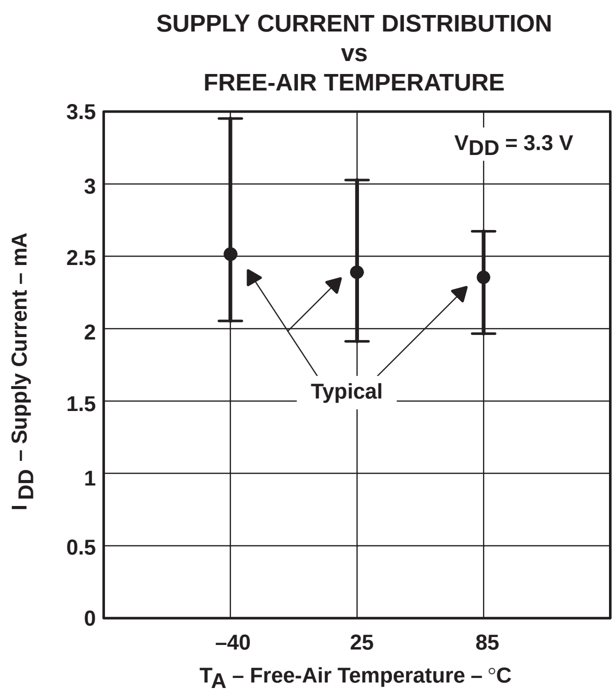


Figure 4

APPLICATION INFORMATION

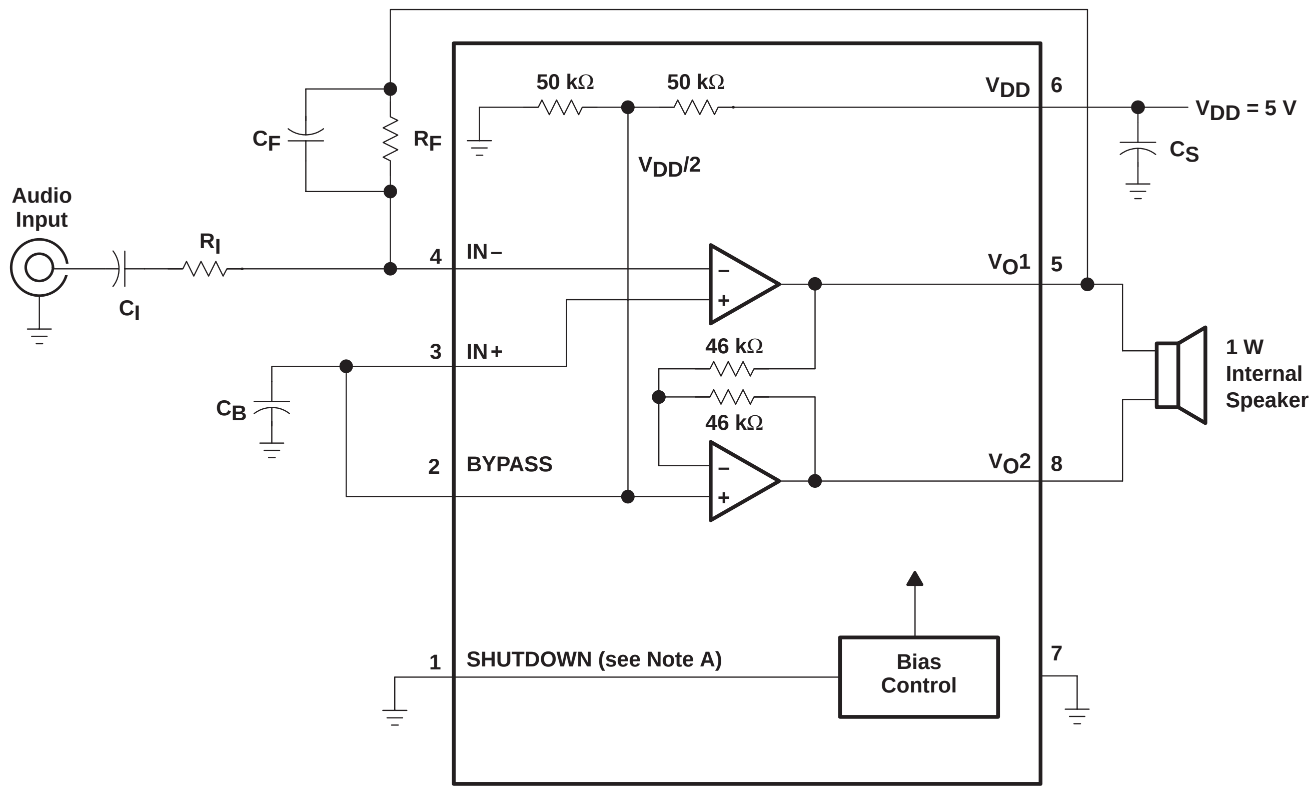
BTL amplifier efficiency (continued)

A final point to remember about linear amplifiers, whether they are SE or BTL configured, is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

For example, if the 5-V supply is replaced with a 10-V supply (TPA4861 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1 then efficiency at 1 W would fall to 31% and internal power dissipation would rise to 2.18 W from 0.59 W at 5 V. Then for a stereo 1-W system from a 10-V supply, the maximum draw would be almost 6.5 W. Choose the correct supply voltage and speaker impedance for the application.

selection of components

Figure 37 is a schematic diagram of a typical notebook computer application circuit.



NOTE A: SHUTDOWN must be held low for normal operation and asserted high for shutdown mode.

Figure 37. TPA4861 Typical Notebook Computer Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA4861 is set by resistors R_F and R_I according to equation 5.

$$\text{Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA4861 is a MOS amplifier, the input impedance is very high; consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The gain of the amplifier would be –10 V/V and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{7}$$

For example if R_F is 100 kΩ and Cf is 5 pF then f_{co} is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \tag{8}$$

The value of C_I is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_{co}} \tag{9}$$

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

single-ended operation

Figure 38 is a schematic diagram of the recommended SE configuration. In SE mode configurations, the load should be driven from the primary amplifier output (V_O1, terminal 5).

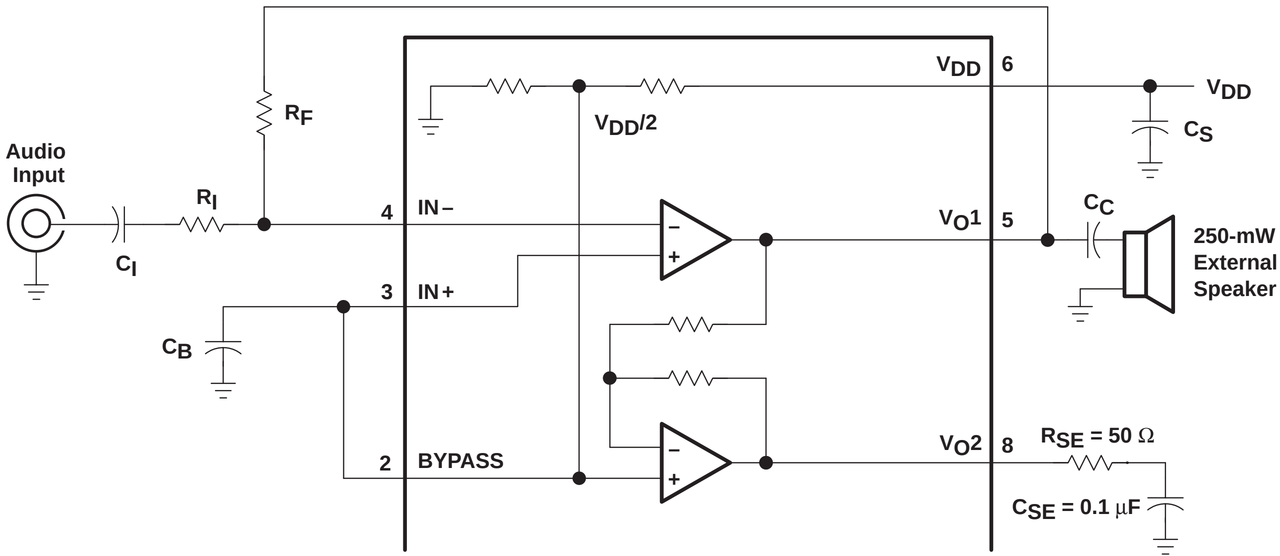


Figure 38. Singled-Ended Mode

Gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2 is not included.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{11}$$

The phase margin of the inverting amplifier into an open circuit is not adequate to ensure stability, so a termination load should be connected to V_O2. This consists of a 50-Ω resistor in series with a 0.1-µF capacitor to ground. It is important to avoid oscillation of the inverting output to minimize noise and power dissipation.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{1}{\left(C_B \times 25\ \text{k}\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \tag{12}$$