3. Mechanical Specifications

Table 1

Parameter	Specifications	Unit
Outline dimensions	206 (W) × 146 (H) × 7MAX (D) *1	mm
Effective viewing Area	151 (W) × 113.4 (H)	mm
Display format	640 (W) × 480 (H) full dot	—
Dot size	0.21 × 0.21	mm
Dot spacing	0.02	mm
Dot color	Black *2*3	—
Background color	White *2*3	—
Weight	Approx. 290	g

*1 Excluded the allowance of deformation.

*2 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*3 Positive-type display
Displayed data 'H': Dots ON : Black
Displayed data 'L': Dots OFF: White

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	V_{DD}-V_{SS}	0	6.0	V	Ta=25°C
Supply voltage (LCD drive)	V_{DD}-V_{EE}	0	30.0	V	Ta=25°C
Input voltage	V_{IN}	0	V_{DD}	V	Ta=25°C

5. Electrical Specifications

5-1 Electrical characteristics

Tabel 4 $Ta=25°C, V_{DD}=5V\pm5\%$

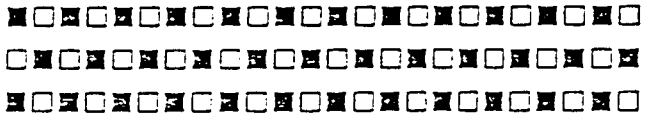
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	$V_{DD}-V_{SS}$		4.75	5.0	5.25	V
Supply voltage (LCD drive)	$V_{EE}-V_{SS}$	Note 1) Note 2)	-23.0	-18.7	-14.1	V
Input signal voltage	V_{IH}	'H' level	0.8V_{DD}	—	V_{DD}	V
		'L' level	0	—	0.2V_{DD}	V
Input leakage current	I_{IL}	'H' level	—	—	250	μA
		'L' level	-250	—	—	μA
Supply current (Logic)	I_{DD}	Note 3)	—	25	35	mA
Supply current (LCD drive)	I_{EE}		—	21	28	mA
Power consumption	Pd		—	520	700	mW

Note 1) The viewing angle θ at which the optimum contrast is obtained by adjusting $V_{EE}-V_{SS}$. Refer to Fig.4 for the definition of θ.

Note 2) Max. and Min. values are specified as the Max. and Min. voltage within the condition of operational temperature range (0~45°C).
Typ. values are specified as the typical voltage at 25°C.

Note 3) Display high frequency pattern.
V_{DD} = 5V, V_{EE} - V_{SS} = -18.7V, Frame frequency = 85Hz, Display pattern = 1bit checker

display pattern



5-2 Input capacitance

Table 5

Signal	Input capacitance
S	40pF TYP
CP1, DISP	250pF TYP
CP2	200pF TYP
DU0~DU3	200pF TYP
DL0~DL3	200pF TYP

5-3 Interface signals

Table 6

○ LCD (connector No. 1)

Pin No	Symbol	Description	Level
1	S	Scan start-up signal	'H'
2	CP1	Input data latch signal	H→L
3	CP2	Data input clock signal	H→L
4	DISP	Display control signal	Display on..'H' off..'L'
5	V_{DD}	Power supply for logic and LCD (+5V)	—
6	V_{SS}	Ground potential	—
7	V_{EE}	Power supply for LCD (-)	—
8	DU0	Display data signal (Upper half)	H (ON), L (OFF)
9	DU1		
10	DU2		
11	DU3		
12	DL0	Display data signal (Lower half)	H (ON), L (OFF)
13	DL1		
14	DL2		
15	DL3		

○ SENSOR BOARD (Connector No. 2)

Pin No	Symbol	Description	Type
1	DGND	Digitizer Ground line	
2~15	A28~15	Sensor Input/Output	analog

○ SENSOR BOARD (Connector No. 3)

Pin No	Symbol	Description	Type
1~14	A14~1	Sensor Input/Output	analog
15	DGND	Digitizer Ground line	

Note 1) The symbols like 'A1','A2'····are corresponding to the Input/Output pin No. of WACOM switch IC 'W6002F'.

Note 2) Pin No. and its location are shown in Fig. 8.

Used connector (CN1) : 52271-1517 (MOLEX)

Used connector (CN2, 3) : 52207-1517 (MOLEX)

Mating cable (CN1~3) : 15pins 1mm Pitch FFC or FPC, Conductor width 0.7mm
length 2.7mm
Contact portion
thickness 0.3mm

Table 7 Interface timing ratings

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle	T_{FRM}	8.0*1		16.9	ms
CP2 clock cycle	T_{CP2}	152			ns
'H' level clock width	t_{CWH}	65			ns
'L' level clock width	t_{CWL}	65			ns
'H' level latch clock width	t_{LWH}	70			ns
Data set up time	t_{SU}	50			ns
Data hold time	t_H	40			ns
S set up time	t_{SSU}	100			ns
S hold time	t_{SH}	100			ns
CP2↑ clock allowance time from CP1↓	t_{SU1}	0			ns
CP1↑ clock allowance time from CP2↓	t_{SU2}	0			ns
Clock rise/fall time	tr, tf			t_{rf}*2	ns

*1 : LCD unit functions at the minimum frame cycle of 8 ms (Maximum frame frequency of 125Hz). Owing to the characteristics of LCD unit, 'shadowing' will become more eminent as frame frequency goes up, while flicker will be reduced.

According to our experiments, frame cycle of 11.7 ms Min. or frame frequency of 85 Hz Max. will demonstrate optimum display quality in terms of flicker and 'shadowing'. But since judgement of display quality is subjective and display quality such as 'shadowing' is pattern dependent, it is recommended that decision of frame cycle or frame frequency, to which power consumption of the LCD unit is propotional, be made based on your own through testing on the LCD unit with every possible patterns displayed on it.

*2 : $t_{rf} = 50$ in case $t_{cr}=(T_{CP2}-t_{CWH}-t_{CWL})/2 \geq 50$

$t_{rf} = t_{cr}$ in case $t_{cr}=(T_{CP2}-t_{CWH}-t_{CWL})/2 < 50$

6. Display Driving Method

6.1 Circuit configuration

Fig.7 shows the block diagram of the Unit's circuitry.

6.2 Display Face Configuration

The display face electrically consists of two (upper and lower) display segments so that the unit may offer higher contrast by reducing drive duty ratio. Each display segment (640×240 dots) is driven at 1/240 duty ratio.

6.3 Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits.

Display data which are externally divided into data for each row (640dots) will be sequentially transferred in the form of 4-bit parallel data through shift registers by Clock Signal CP2 from the left top of the display face.

When data of one row (640dots) have been input, they will be latched in the form of parallel data for 640 lines of signal electrodes by latch signal CP1. Then the corresponding drive signal will be transmitted to the 640 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal S has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st rows of upper and lower half of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD.

While the 1st rows of data are being displayed, the 2nd rows of data are entered. When 640 dots of data have been transferred then latched on the falling edge of CP1 clock, the display face proceeds to the 2nd rows of display.

Such data input will be repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display by time sharing method. Then data input proceeds to the next display face.

Scan start-up signal S generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction which will

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit goes up as the operating frequency CP2 increases. Thus the driver LSI applies the system of tranferring 4-bits parallel data through the 4 lines of shift registers to reduce the data transfer speed CP2. Thanks to the LSI, the power consumption of the unit will be minimized.

In this circuit configuration, 4-bit display data shall be therefore input to data input pins of DU_{0-3} (upper display segment) and DL_{0-3} (lower display segment).

Furthermore the LCD unit adopts bus line system for data input to minimize the power consumption. In this system data input terminal of each driver LSI activated only when relevant data input is fed.

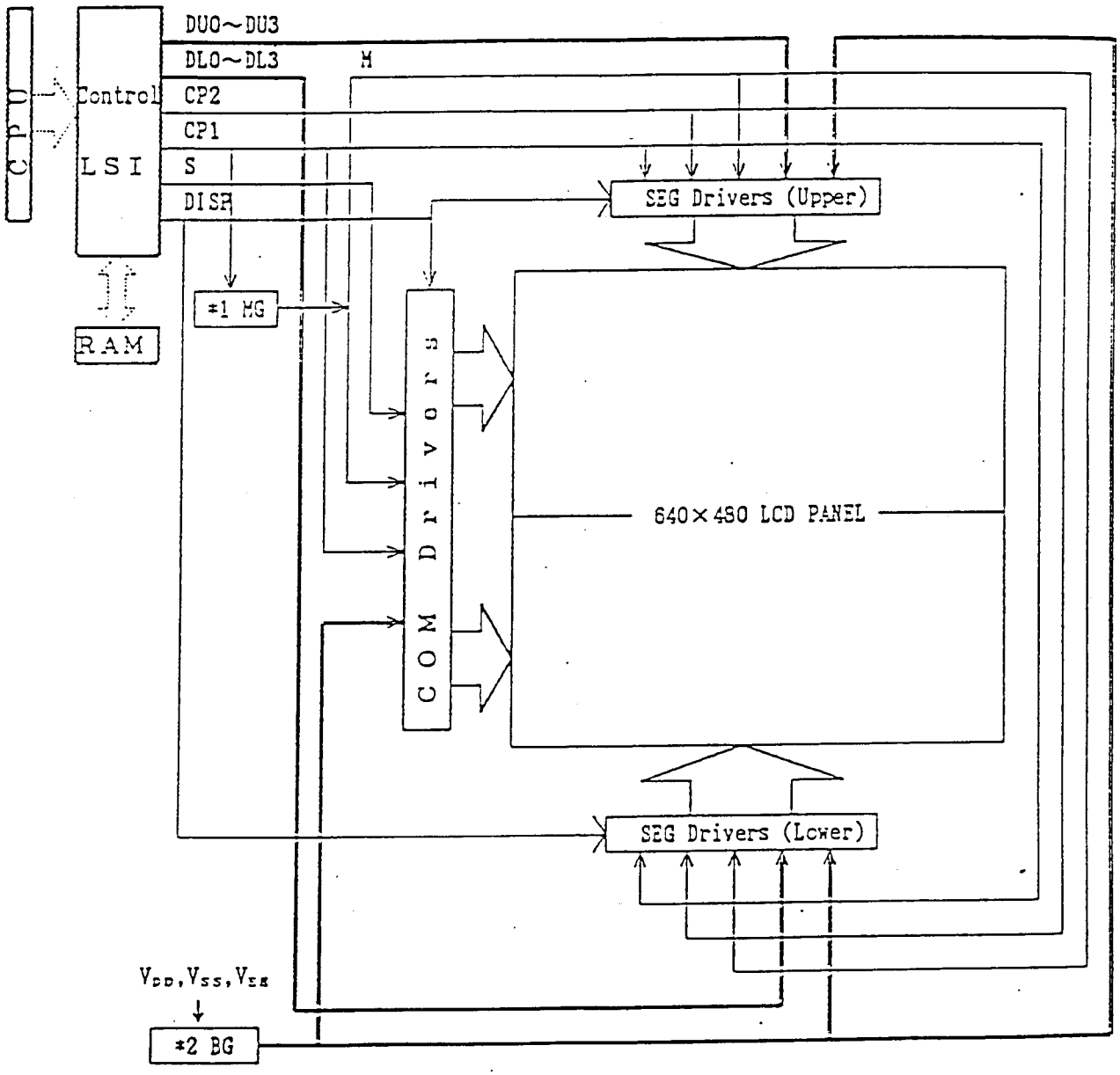
Data input for column electrodes of both the upper and the lower display segment and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.

This process is simultaneously followed at the column drivers LSI's of both the upper and the lower display segments. Thus data input for both the upper and the lower display segments must be fed through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no reflesh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig. 3 and Table 7.



*1 MG: M GENERATOR CIRCUIT
*2 BG: BIAS GENERATOR CIRCUIT

Fig 7. Circuit block diagram

8. Digitizer Specifications

8-1. Performance specification

1) Sensing method system	:Electromagnetic Give and Receive Action
2) Active area	:149.2 (W) × 112.4 (H) mm
3) Resolution	:0.1mm
4) Accuracy	:±0.5mm (measured on protective glass)
5) Coordinate reading speed (tracking speed)	:205 pps (or 2m per sec)
6) Proximity with specified accuracy	:0~5mm above protective glass
7) Power voltage	:DC +5V±10%, DC -5V±5%
8) Power requirement	:Low scan 35mW (typ)
	High scan 300mW (typ)
9) I/F	:8 bit parallel bus
	Wacom standard serial

8-2. Conditions

ISD Evaluation Baby Board	:EB-A221-194F	(WACOM)
ISD Serial Mother Board	:EB-A179	(WACOM)
Baby Board - Sensor I/F Cable	:EB-A231	(WACOM)

The specifications shown above are defined by using above Evaluation Board and Serial Mother Board.
Since the digitizer technology used in the LCD unit is sensitive to metal mass/various noises, the performance is system dependent.
Thorough evaluation of the LCD unit with its host equipment shall be conducted, therefore, to ensure the specified performance with production unit of host equipment.

8-3. Configuration of integral-components to drive built-in sensor board

The following components shall be procured separately to drive the sensor board of LM64194F properly.

Stylus	UP series	(WACOM)
Co-processor	M37700 series	(WACOM)
I/F controller	W50007	(WACOM)
Analog controller	W60017	(WACOM)
Switch IC	W60027	(WACOM)

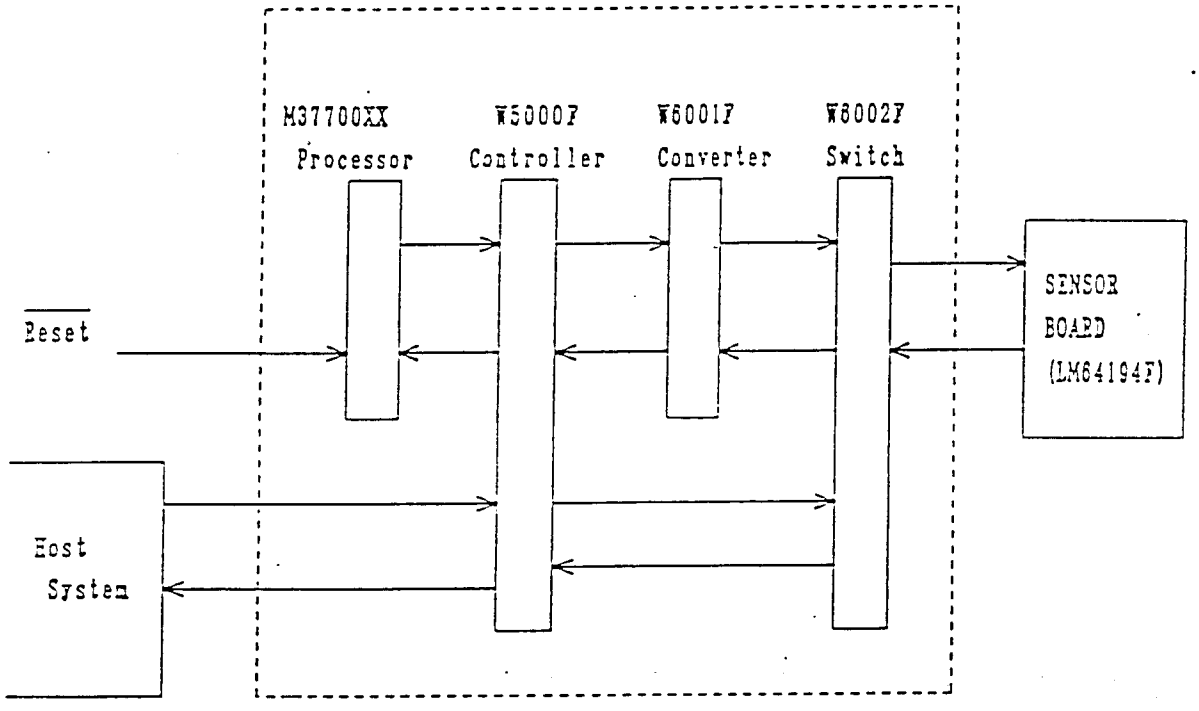
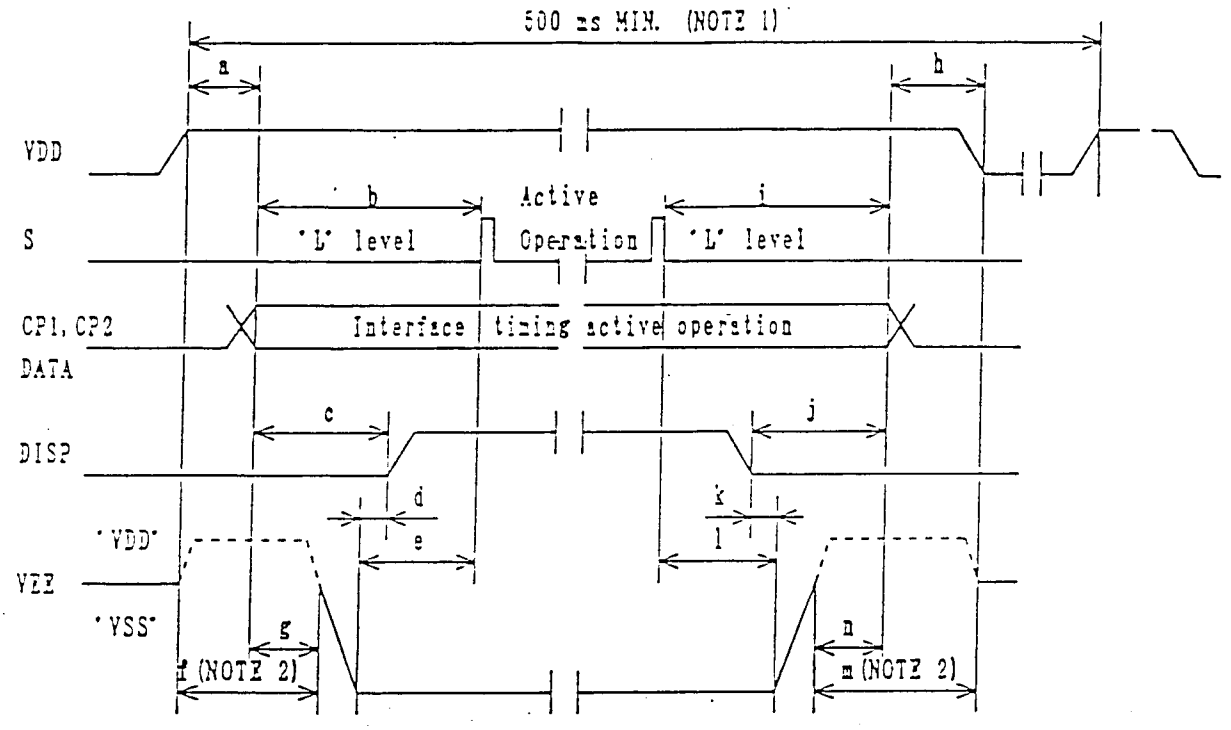


Fig. 9 Configuration

Supply voltage sequence condition



POWER ON		
SYMBOL	With DISP control	Without DISP control
a	0 ms MIN.	0 ms MIN. 20 ms MAX.
b	0 ms MIN.	20 ms MIN.
c	20 ms MIN.	-
d	0 ms MIN.	-
e	-	0 ms MIN.
f	0 ms MIN.	(NOTE2)
g	-	0 ms MIN. 100 ms MAX.

POWER OFF		
SYMBOL	With DISP control	Without DISP control
h	0 ms MIN.	0 ms MIN. 20 ms MAX.
i	0 ms MIN.	20 ms MIN.
j	20 ms MIN.	-
k	0 ms MIN.	-
l	-	0 ms MIN.
m	0 ms MIN.	(NOTE2)
n	-	100 ms MIN.

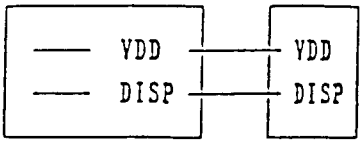
(NOTE 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.

(NOTE 2) VEE to be set at 'VDD level' or 'open'. VEE should be in accordance with the dotted line when DISP (display control signal) is not used.

(NOTE 3) Connection of DISP (pin. No. 4)

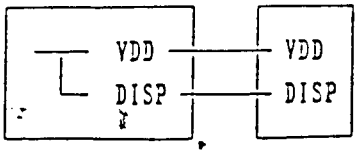
○With DISP control

Input DISP control signal shown on this page.



○Without DISP control

DISP to be connected with VDD.

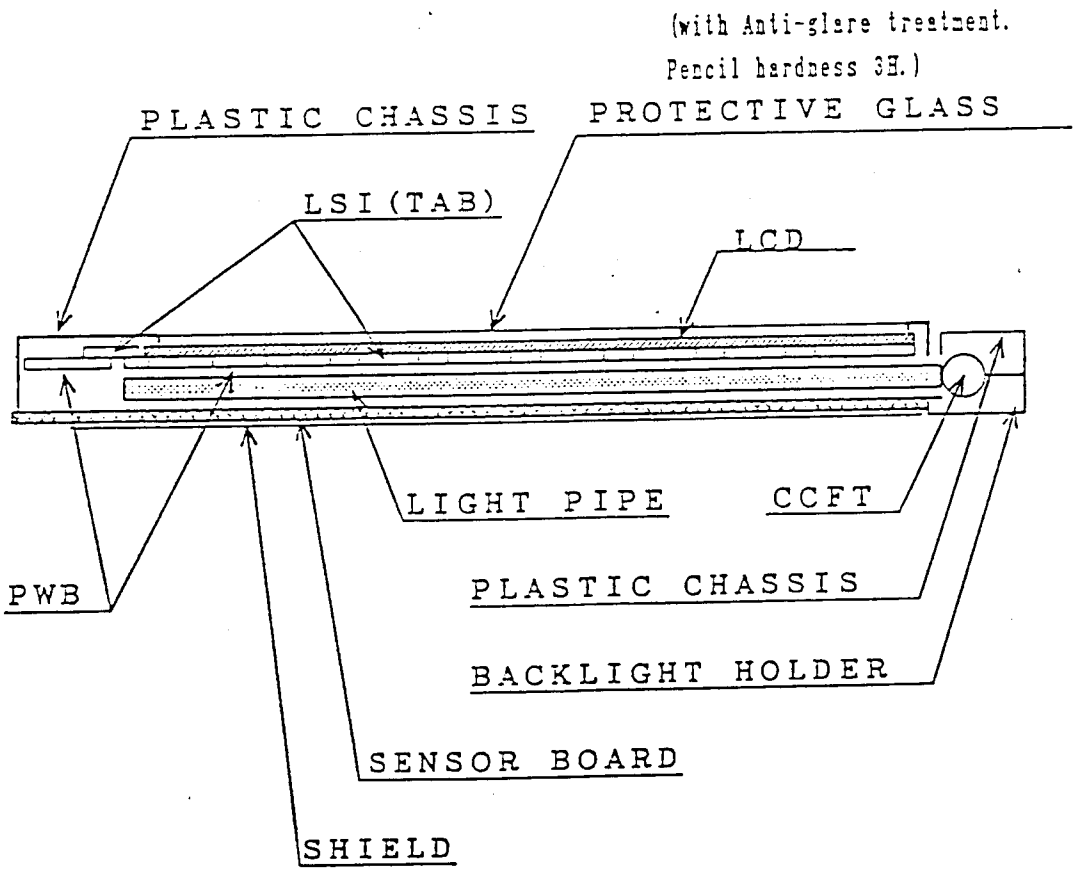


1. Application

This data sheet is to introduce the specification of LM64P90, Passive Matrix type LCD Unit with digitizer board built in.

2. Construction and Outline

Construction: 640×480 dots display unit consisting of an LCD panel, PWB (printed wiring board) with electronic components mounted onto, TAB (tape automated bonding) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT backlight and digitizer board, and plastic chassis to fix them mechanically.



Outline : See Fig. 10

Connection : See Fig. 10 and Table 6