SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

STLC7546 - ANALOG FRONT-END

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I - INTRODUCTION

The STLC7546 is a high resolution analog-to-digital and digital-to-analog converter targeted for V.34 and 56Kbps modem and consumer audio applications. This device has a 16 bit oversampling ADC and DAC, filters and control logic for the serial interface. The oversampling ratio consequently the sampling frequency for the ADC and DAC are user programmable. The devices operation is controlled by reading the 16-bit information control register.

The major functions of the STLC7546 are :

- To convert the audio-signal to 16-bit 2's complement data format through ADC channel.
- To communicate with an external digital signal processor via serial interface logic.
- To convert 16-bit 2's complement data from a digital signal processor to an audio signal through the DAC channel.

The STLC7546 consists of two signal-processing channels, an ADC channel and a DAC channel, and the associated digital control. The two channels operate synchronously so that the transmitted data to the DAC channel and received data from the ADC channel occur during the same time interval. The data transfer is in 2's complement format.

To save power, the low-power reset mode can be used to reduce the power consumption to less than 1mW (typ. 50µW).

II - DIGITAL INTERFACE (9 Pins)

The STLC7546 is a very simple device to use thanks to the preprogrammed filters and its only one control register. In a short time you will be familar to the high efficiency integration function.

II.1 - Data Exchange

The data exchange (DATA and CONTROL) are done through the pins Data in (Din) and Data out (Dout) (see Table 1).

II.2 - Mode Selection

Two modes of serial transfer are available :

- First : Software mode for 15-bit transmit data transfer and 16-bit receive data transfer
- Second : hardware mode for 16-bit data transfer.

Both modes are selected by the Hardware Control pins (HC0, HC1) (see Table 2).

The data to the device, input/output are MSB-first in 2's complement format (see Figure 1).

When Control Mode is selected, the device will internally generate an additional Frame Synchronization Pulse (Secondary Frame Synchronization Pulse) at the midpoint of the original Frame Period. The Original Frame Synchronization Pulse will also be referred to as the Primary Frame Synchronization Pulse.

Table 1

Pin	Data Mode	Control Mode
Din	Word is input of the DAC	Data word followed by control register word
Dout	Word is ADC conversion result	Data word followed by register read

Table 2 : Mode Selection

HC1	HC0	LSB	Useful Data	Secondary FSYNC	Description
0	0	0	15bits	No	Software Mode for Data Transfer only.
0	0	1	15bits (+16bits reg.)	Yes	Software Mode for Data Transfer + Control Register Transfer.
0	1	X	16bits	No	Hardware Mode for Data Transfer only.
1	X	X	16bits (+16bits reg.)	Yes	Hardware Mode for Data Transfer + Control Register Transfer.

Figure 1 : Data Mode

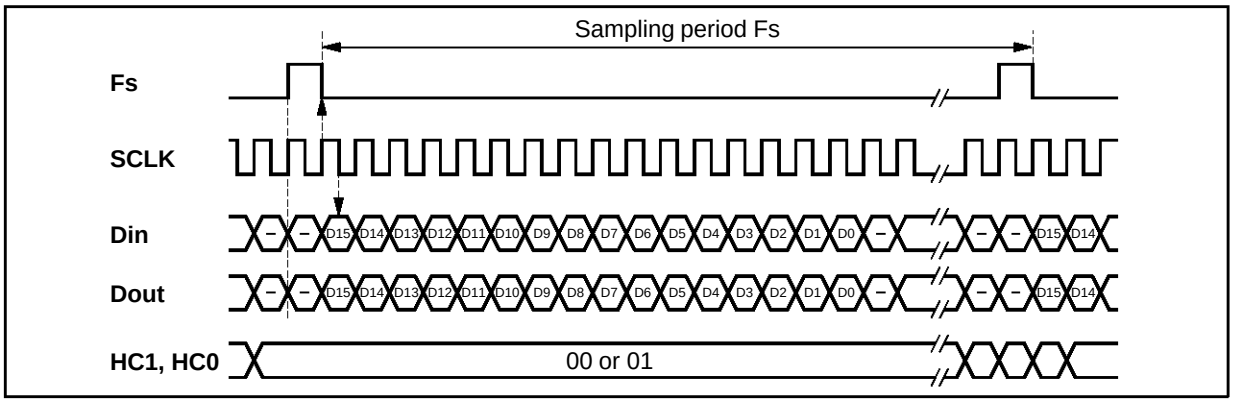
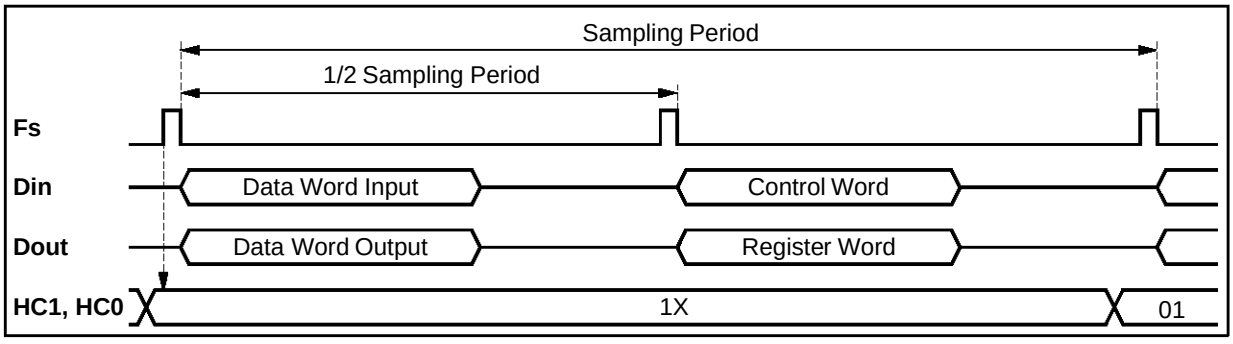


Figure 2 : Access Register Mode (obtained also with LSB data = "1")



II - DIGITAL INTERFACE (9 Pins) (continued)

II.3 - Clocks Signals

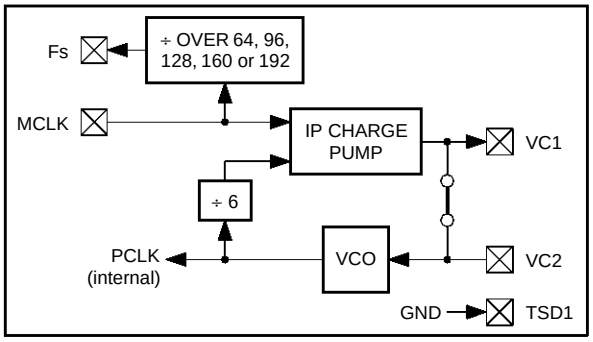
- MCLK : Master Clock Input. This signal is the oversampling clock of the D/A and A/D convertor. It also provides the clocks of the serial interface (Fs, SCLK). The master clock is equal to Fs x OVER (OVER = oversampling ratio = 64, 96, 128, 160 or 192). For proper operation there must be no jitter on MCLK.
- Fs : Frame Synchronization (Sampling frequency) signal generated internally goes low on rising edge of SCLK. This signal indicates that the STLC7546 is ready to send or receive data.
- SCLK : Serial bit clock clocks data into Din and out of Dout during Fs. SCLK = MCLK

The clock generator provides, via an internal PLL, the clocks needed for the computation in the digital section (PCLK = Processing Clock). The MCLK clock is used by the PLL for the clock reference.

Thanks to the control register, different configurations can be obtained for the clock generator. We use the bits D15 and D14 of the control register.

D15	D14	Mode
0	X	PLL normal mode, TSD1 Pin is grounded internally
1	0	PLL open loop, Tsd1 Pin = PCLK output (TEST3)
1	1	PLL open loop, Tsd1 Pin = PCLK input (TEST4)

Figure 3 : Normal Mode



TEST3 : see Figure 4
In this mode you can observe the Processing clock on Pin TSD1. Do not forget to connect externally the Pin VC1 and VC2 for the PLL loop.

TEST 4 : see Figure 5
If you are in the mode to enter the processing clock which is equal to 6 times the MCLK do not forget to provide the Master clock to the STLC7546.

II.4 - Reset - Power Down

RESET : The reset function is to initialize the internal counters and control register. A minimum low pulse of 100ns is required to reset the STLC7546. This reset initiates the serial data communications.

The reset will initialize the register to default value providing the following status for the STLC7546 :
- Oversampling ratio equal to 160
- Serial interface in data mode
- DAC attenuation set to infinite
- ADC gain set to 0dB
- Differential input mode selected on ADC convertor
- Multiplexor set on main inputs IN+ and IN-

After a reset the first frame synchronization corresponds to the primary channel.

POWER DOWN (PWRDWN) : The PWRDWN powers down the entire chip (50µW). When this pin is set low the internally programmed state is maintained. Full operation can be resumed within 5ms by putting back PWRDWN pin to High. When not used this pin should be tied to V_{DD}.

Figure 4 : TEST3

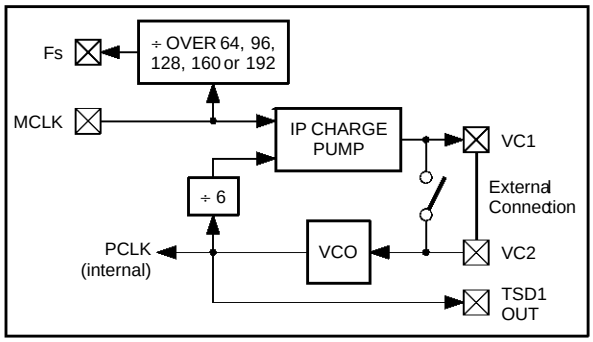


Figure 5 : TEST4

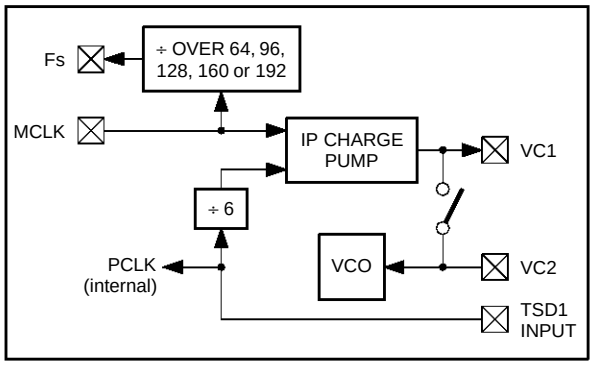
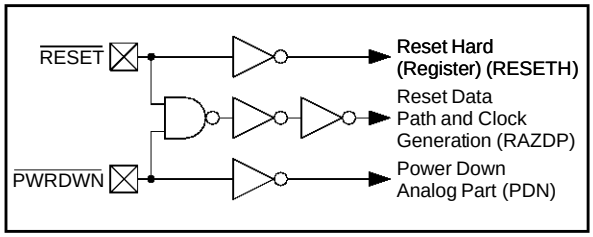


Figure 6



III - TEST FEATURES

Some test features have been introduced in the STLC7546 in order to help you for the debug. These features are accessed through the bit D13 and D12 of the control register or by setting a certain level on Pin Tstd2.

III.1 - Control Register Test Features

D13	D12	Function
0	0	Normal Mode
0	1	Digital Test (TEST 1)
1	0	Analog Test (TEST 2)
1	1	Reserved

TEST 1 : Digital Test (see Figure 7)
In order to test only the digital path, in this mode internally we connect the transmit output Noise Shaper to the Receive FIR filter. So the test does not depend on the analog hardware.

TEST 2 : Analog Test (see Figure 8)
In order to check the analog hardware, in this mode we connect internally the sigma delta modulator output to the DAC (1 bit) input.

Figure 7 : TEST1

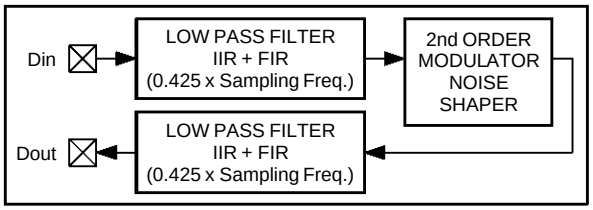
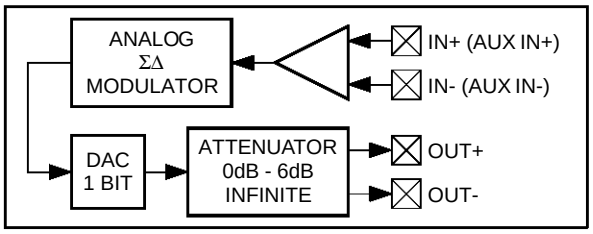


Figure 8 : TEST2



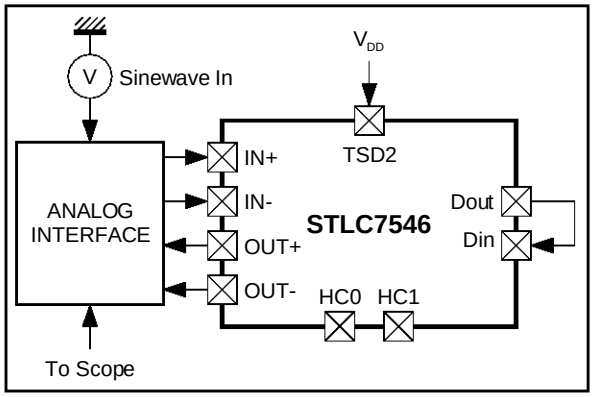
III.2 - Pin Tstd2 Features

In normal mode the pin Tstd2 is set to Ground (0V). Two differents test features could be obtained by setting this pin to V_{DD} or $V_{DD}/2$.

III.2.1 - Tstd2 = V_{DD}

In this configuration we force the transmit attenuator to 0dB. In that case you can test the complete device plus the analog interface by doing a RESET (see default configuration at Chapter II.4) and then you set the Pin Tstd2 to V_{DD} and connect externally the Pin Dout to the Pin Din. You enter a sinewave on the input receive and you will get a sinewave at the transmit output. This feature is good to check your complete hardware without having doubt on your DSP software as this one is not used.

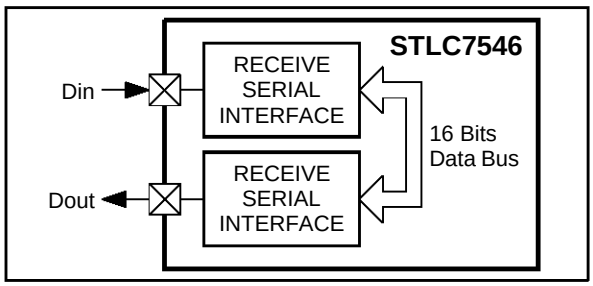
Figure 9



III.2.2 - Tsd2 = V_{DD} / 2

In this configuration we connect internally the output of the transmit serial interface to the input of the receive serial interface. So you will be able to check what has really been taken into account in the device on the received data.

Figure 10



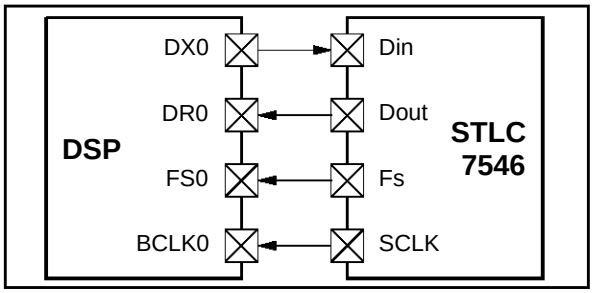
IV - DSP INTERFACE

The interface of the STLC7546 and a DSP is done through a SSI (Synchronous Serial Interface) or SERIAL PORT. Any wellknown DSP on the market has such communication port.

We will see the interconnection for 3 types of DSP : SGS-THOMSON, MOTOROLA and TEXAS INSTRUMENTS.

IV.1 - SGS-THOMSON Microelectronics DSP

Figure 11



IV. 2 - MOTOROLA DSP (see Figure 12)

The SSI of the 56000 family DSP must be programmed as following :

SYN	bit = 1	Synchronous mode
GCK	bit = 0	Continuous clock
SCKD	bit = 0	External source clock
SCD2	bit = 0	SCK set to input mode
FSL	bit = 1	Frame sync length equal 1 bit
WL1-WL0	bits = 10	Word length set to 16 bits
DC4_DC0	bits = 0000	Number of time slot (1)

IV.3 - TEXAS INSTRUMENTS DSP (see Figure 13)

The SERIAL PORT of the TMS320C5x DSP family has to be programmed through the serial port control register as following :

DLB	bit = 1	With MCM=0 we have CLKX=CLKR (external)
MCM	bit = 0	External clock bit source
FO	bit = 0	Word length is 16 bits
FSM	bit = 1	Frame sync pulse required for each word
TXM	bit = 0	FSX pin is an input

Figure 12

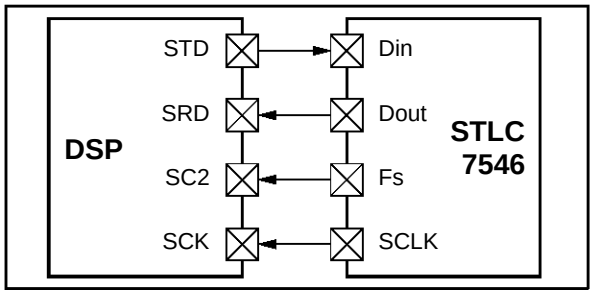
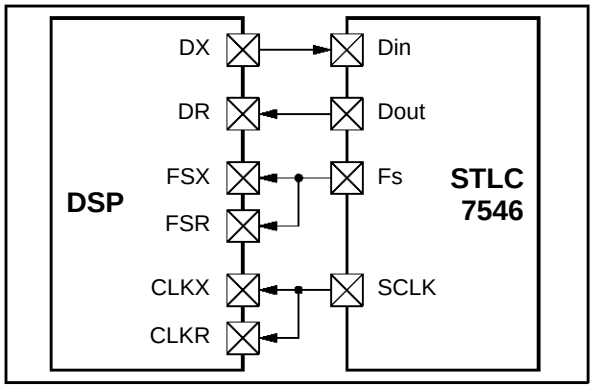


Figure 13



V - ANALOG INTERFACE

STLC7546 is targeted for V.34bis standard and 56kbps new standard and for low-power application. Line interface has to present :

- good performances to allow high speed communication,
- a supply around 5V,
- small size to allow the modem to fit in portable applications for which low-power solutions are usually dedicated.

An overview of the proposed modem line interface is shown on Figure 14. The STLC7546 transmit and receive signals from the phone line via a duplexor (that isolates modem from phone line, filters and amplifies signal) and a bridge (to allow the modem to work even Tip and Ring are inverted).

A ring detect block signals to the digital controller via the RING signal incoming calls. Then the line is taken with a ON HOOK/OFF HOOK switch, and by driving a constant current (current driver block). The different blocks are detailed hereafter.

V.1 - Duplexor

V.1.1 - Differential Duplexor

This duplexor is also called hybrid for it interfaces the 2-wire bi-directional phone line in two separate differential and unidirectional lines to the codec (Transmit and Receive). A differential duplexor for the modem part is given on Figure 15. Hybrid performances are mainly depending on a good impedance matching with the phone line and a good Transmit rejection on the Receive input (loss).

Figure 14 : Line Interface Overview

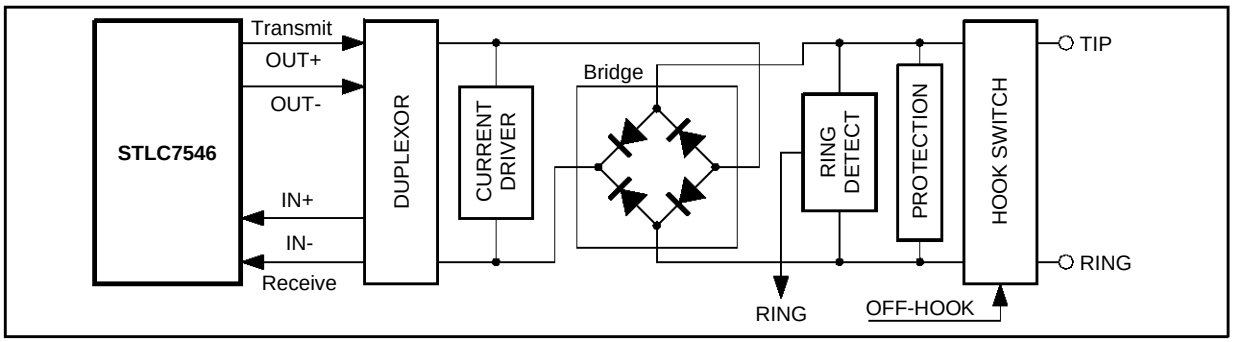
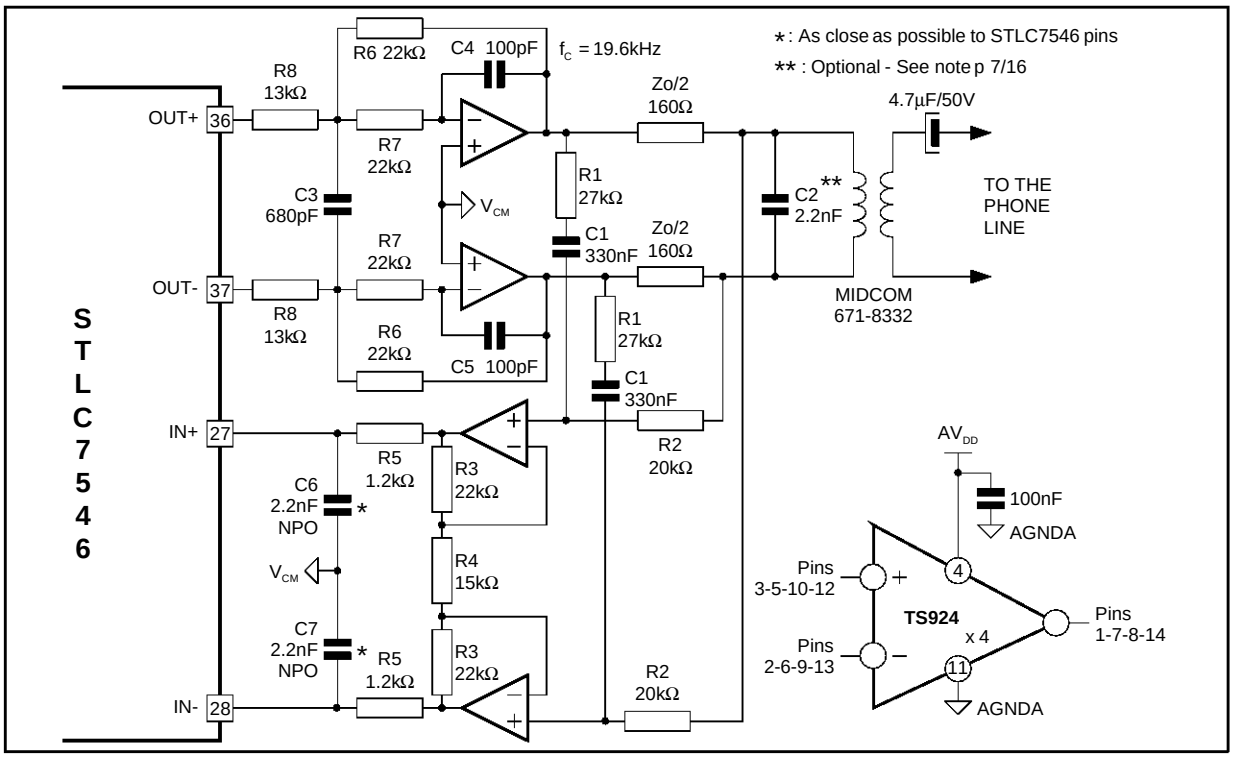
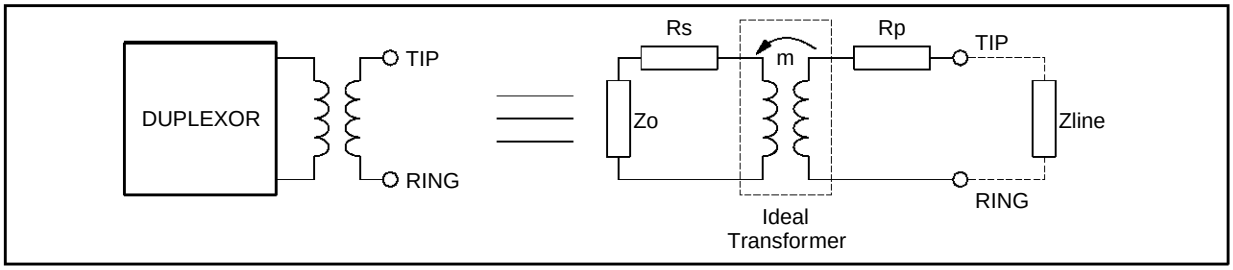


Figure 15 : Differential Duplexor



V - ANALOG INTERFACE (continued)

Figure 16 : Line Interface Equivalent Model



A. Phone Line Impedance Matching

Impedance mismatches between line and DAA cause reflections and interference between Transmit and Receive signals giving echoes that limit modem speed. The impedance matching is related to the phone line impedance (Zline) - that depends on the country, line length, and the signal frequency only the 600Ω line impedance, will be considered in this application note.

Figure 16 shows the equivalent model of a line interface, where Zo is the duplexor equivalent impedance, R_P and R_S the transformer resistance, and Zline the phone line impedance.

The impedance matching condition is :

$$R_P + Z_O/m^2 + R_S/m^2 = Zline \quad [1]$$

Application :

The MIDCOM 671-8332 transformer used gives the following performances :

- $R_P = 155\Omega$, $R_S = 150\Omega$
- turns ratio m = 1 ± 1%
- longitudinal balance : 40dB min.
- total harmonic distortion : 82dB
- insertion loss : 3.0dB Typ.

Zline = 600Ω

[1] = $Z_O = (Zline-Rp) \cdot m^2 - R_S = 295\Omega$

Impedance recommended by MIDCOM is 316Ω. We take $Z_O/2 = 160\Omega$.

**Note : the capacitor C2 is used to add a third external pole for DAC-channel noise rejection. Nevertheless, it can increase electrical echo on receive section. It is dependent on the phone line type.

B. Transmit Rejection

For full duplex communication a Transmit signal rejection on the Receive part is made by resistor R1 and R2. In that way, only the incoming phone line signal is present on the Receive output.

The loss of Transmit signal is given by (see Figure 17) :

$$LOSS = \frac{V_{Receive}}{V_{Transmit\ (No\ signal\ received)}} \quad [2]$$

$$= 20 \cdot Log\left(\frac{Z_{EQ}}{Z_{EQ}+Z_O} \cdot \frac{R1}{R1+R2} - \frac{R2}{R1+R2}\right)$$

with Zeq being the equivalent impedance of the phone line impedance seen from the secondary of the transformer.

Maximum loss is achieved when :

$$\frac{Z_{EQ}}{Z_{EQ}+Z0} = \frac{R2}{R1} \quad [3]$$

Application :

R2 = 20kΩ, Zo = 320Ω

$Z_{EQ} = R_S + Rp \cdot m^2 + Zline.m^2 = 905\Omega$

[3] => $R1 = (Z_{EQ} + Z0) \cdot R2/Z_{EQ} = 27.07k\Omega$.

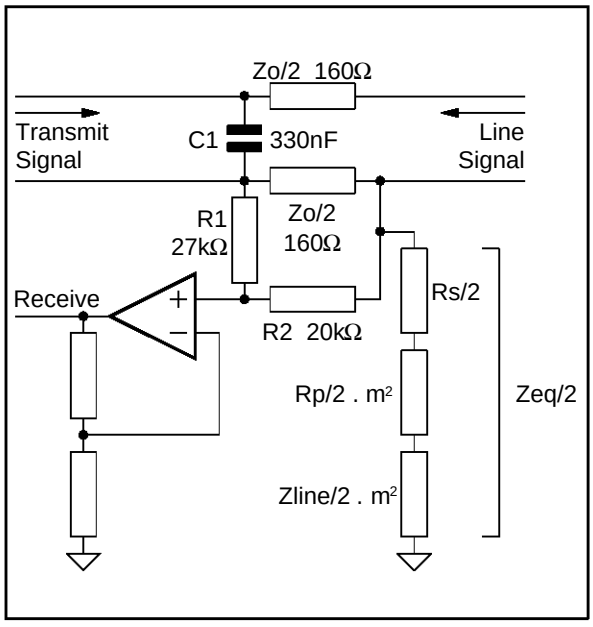
We take R1 = 27kΩ.

[2] => Loss = -59dB (theoretical value, resistor values should be certified at 1% for good performances).

C1 = 330nF.

C1, R1 improves the low frequency response. These values depend on the transfer function of the transformer. Filter transfer function made by C1, R1 must compensate for the loss in transformer at low frequencies. If a compensation is not needed, the capacitor C1 can be suppressed.

Figure 17 : Transmit Rejection simplified AC Schematic



V - ANALOG INTERFACE (continued)

C. Transmit Filter *(see Figure 18)*

A two-pole continuous time external filter must follow the output pin in order to remove quantization noise. The filter characteristics are :

Transfer function with :

$$H = G_T \cdot \frac{1}{1 + 2 \cdot x \cdot s + s^2} \text{ with } s = j \frac{\omega}{2\pi \cdot f_C}$$

DC gain :

$$GT = \frac{R6}{R8}$$

Overvoltage factor :

$$x = \frac{1}{2} \cdot \left(\sqrt{\frac{R7}{R6}} + \sqrt{\frac{R6}{R7}} + \frac{\sqrt{R6 \cdot R7}}{R8} \right) \cdot \sqrt{\frac{C4}{2 \cdot C3}}$$

Cutoff frequency :

$$f_C = \frac{1}{2\pi \sqrt{R_7 \cdot R_6 \cdot C_4 \cdot 2 \cdot C_3}} \text{ with } f_C > 2 \cdot f_S \text{ [4]}$$

f_C must be at least twice the value of the sampling frequency.

The filter also amplifies (with a gain G_T) the Transmit signal to compensate the loss (L_T) due to the divider made of resistor Z0 and equivalent line impedance Z_{EQ}. The gain condition that makes the codec maximum output level A_C to match with maximum phone line level A_L is :

$$A_C \cdot L_T \cdot G_T = m \cdot A_L$$

$$\text{with } G_T = \frac{R_6}{R_8} \text{ and } L_T = \frac{Z_{line}}{Z_O + Z_{EQ}} \text{ [5]}$$

Application

DTMF level is considered as the highest level to be transmitted. Levels used in this application are :

- High group tone level : -9dBV + 2/-2.5 ($1V_{PP}$)
- Low group tone level : -11dBV + 2.5/-2 ($0.80V_{PP}$)
- The level of the tone in the high group must be 1dB to 4dB higher than the level of the tone in the low group.

In consequence maximum DTMF signal level is within 1.38 and $2.32V_{PP}$. The maximum phone line level is set to 2.2V (corresponding to a 0dBm single tone).

$2 \cdot A_L = 2.2V_{PP}$ ($2 \cdot A_L$ because of differential structure)
$\Rightarrow A_L = 1.1V_{PP}$
Z0 = 320Ω, Zline = 600Ω, Z_{EQ} = 905Ω, [5] gives $L_T = 0.490$, A_C =1.25V, m = 1
[5] gives $G_T = m \cdot A_L / (A_C \cdot L_T) = 1.795 = +5dB$

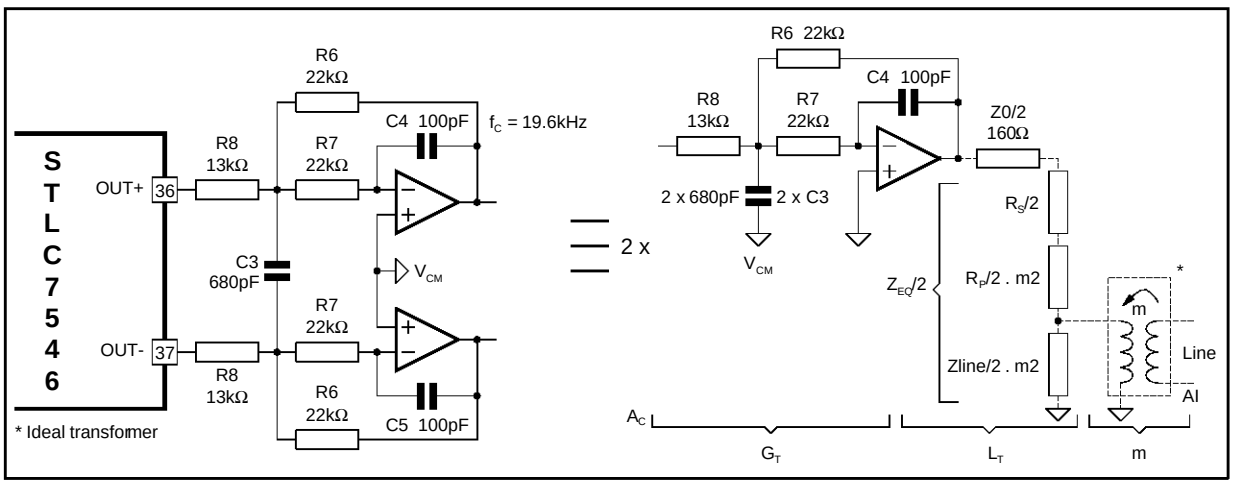
Choosing R6 = 22kΩ gives R8 = 13kΩ (STLC7546 minimum load is 10kΩ) and $G_T = 2$

[6] $A_C \cdot G_T = 2.5V_{PP}$

Note : The maximum line level during V.34 communication is around $1.2V_{PP}$. This gives a maximum signal level on codec output pin around $0.6V_{PP}$ [$1.2/(2 \cdot G_T \cdot L_T)$] that gives a good dynamic with no distortion.

Sampling frequency : 9.6kHz gives f_C # 19.2kHz choosing R7 = 22kΩ, C3 = 680pF and C4 = 100pF, [4] gives f_C = 19.6kHz

Figure 18 : Transmit Filter



V - ANALOG INTERFACE (continued)

D. Receive Amplifier

Receive amplifier compensate with a gain G_R :
- the loss L_R due to the resistor R1 and R2 divider,
- the loss L_T due to the transformer, composed by the resistor Z_O and the transformer impedance $R_S + Rp \cdot m2$

The gain condition that makes the maximum line level A_L match with the maximum STLC7546 input level A_S is :

Application :
m = 1
Maximum line level : 0dBm,
$2 \cdot A_L$ = 0dBm = $2.2V_{PP}$, $A_L = 1.1V_{PP}$,
R1 = 27kΩ, R2 = 20kΩ, L_R = 0.57,
Z_O = 320Ω, R_S = 150Ω, Rp = 155Ω,
L_T = 0.512,
A_S =$1.25V_{PP}$
$G_R = A_S/(A_L \cdot L_R \cdot L_T) = 3.89 = 11.8dB$

We take R3 = 22kΩ and R4 = 15kΩ, gives G_R = 3.93 = +11.90dB.

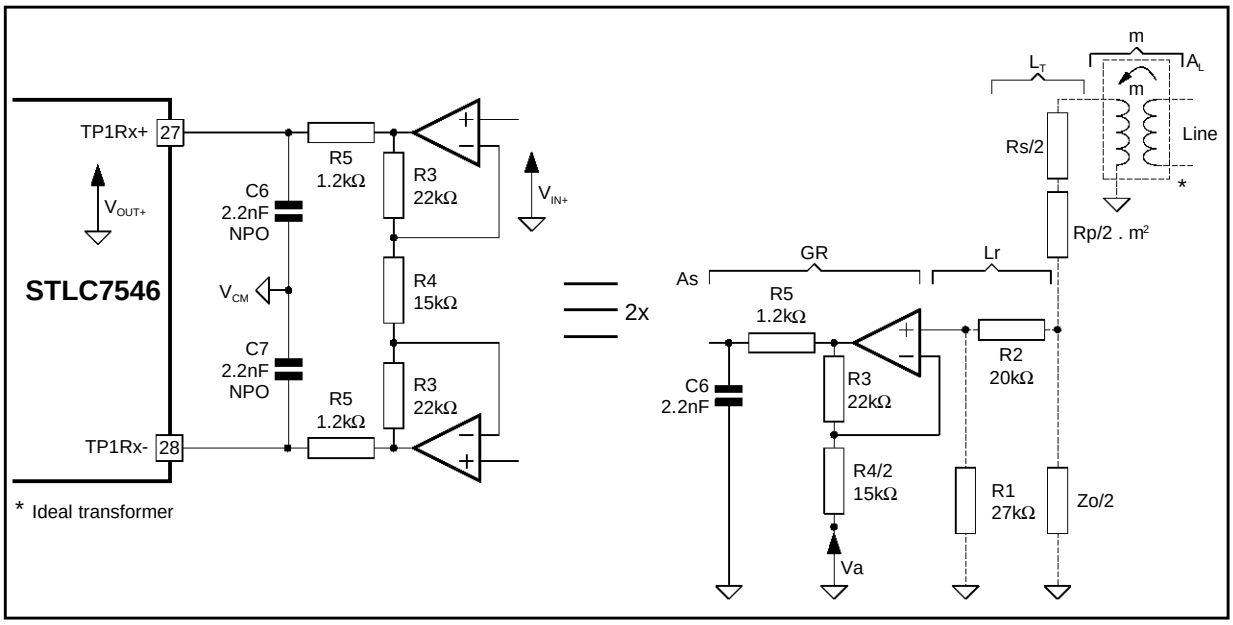
Note : The maximum line level during V.34 communication is around $1.2V_{PP}$. This gives a maximum signal level on codec input pin around $0.68V_{PP}$ [(1.2 /2). $L_R \cdot L_T \cdot G_R$)] that gives a good dynamic with no distortion.

Resistor R4 has also the function of balancing signal TP1Rx+ and TP1Rx- to improve symmetry.

Note : Va is the average voltage between V_{OUT}+ and Vout- that represents the output asymmetry. In ideal conditions it should be equal to 0.

The single pole anti-aliasing filter (R5, C6) removes high frequency noises. C6 must be put as close as possible to the chip. The cut-off frequency must be lower than one half of the oversampling frequency (i.e. lower than 460kHz).

Figure 19 : Receive Amplifier



V - ANALOG INTERFACE (continued)

V.1.2 - Low Cost DAA using A 1:1 Transformer

A duplexor for low-cost application is proposed on Figure 20. Performance depends mainly on a good impedance matching with the phone line and a good Transmit rejection on the Receive input (loss).

A. Phone Line Impedance Matching

See VI.1.1 Differential duplexor.

=> $Z_O = 320\Omega$

B. Receive Amplifier

The amplifier gain G_R (fixed by R5 and R7) is chosen to compensate the loss (L_R) given by the divider composed by resistor Z_O and transformer impedance (R_S + Rp · m2), with $V_{transmit}$ = 0 (see Figure 21). The condition to make maximum line level AL match with maximum codec input level A_S is :

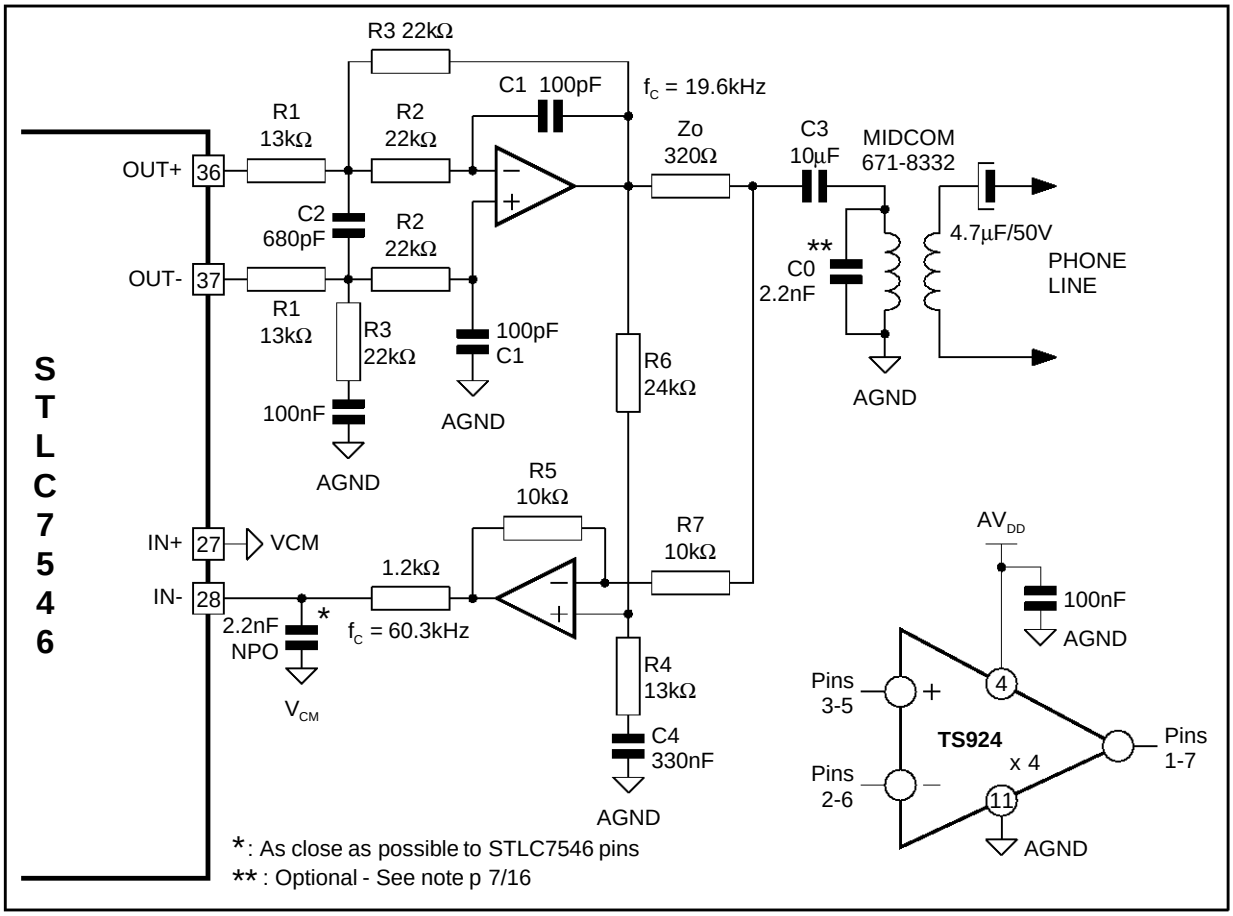
Application :

m = 1,
AL = 0dBm = $2.2V_{PP}$,
R_S + Rp · m2 = 305Ω, Z_O = 320Ω, L_R = 0.512,
A_S = $1.25V_{PP}$,
$G_R = AS/(m \cdot AL \cdot LR) = 1.109 = +0.9dB$

Choosing R5 = 10kΩ gives R7 = 10kΩ and GR = 1.

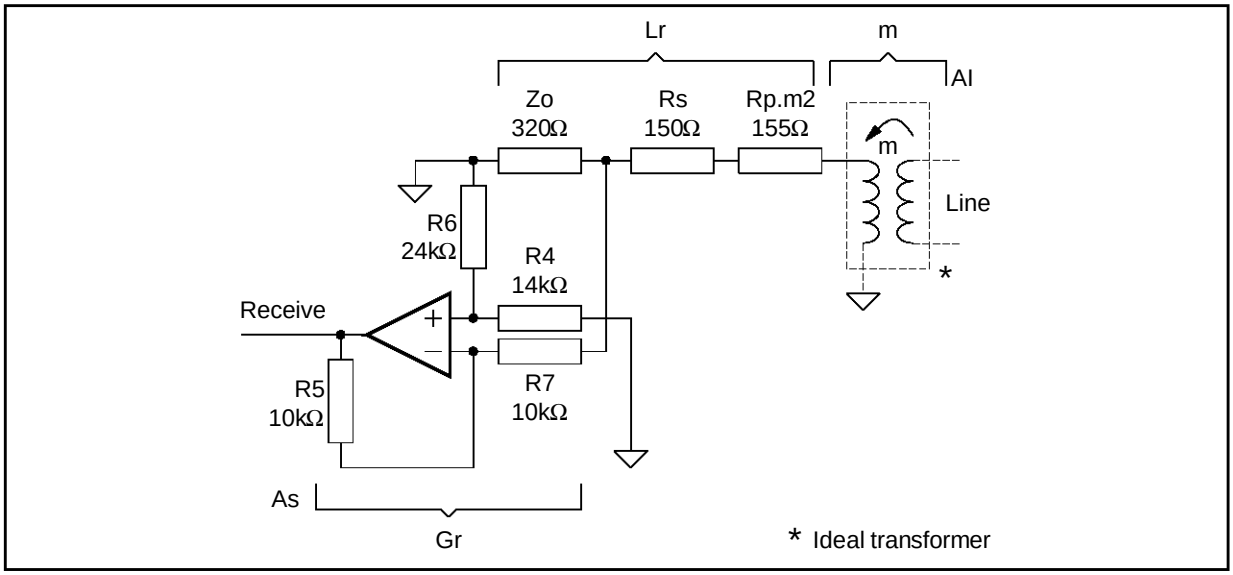
Note : The maximum line level during V.34 communication is around $1.2V_{PP}$. This gives a maximum signal level on codec output pin around $0.6V_{PP}$ [1.2 · m · L_R + G_R] that gives a good dynamic with no distortion.

Figure 20 : Low Cost Duplexor



V - ANALOG INTERFACE (continued)

Figure 21 : Receive Amplifier Simplified AC Schematic (View From Line, No Transmit Signal)



C. Transmit Rejection

For full duplex communication a Transmit signal rejection is made on the Receive amplifier by subtracting the $V_{transmit\ signal}$.
The loss is given by :

$$LOSS = \frac{V_{Receive}}{V_{Transmit(No\ signal\ received)}} \quad [7]$$

$$= 20 \cdot Log\left(\frac{Z_{EQ}}{Z_{EQ}+Z_O} \cdot \frac{R5}{R7} - \frac{R4}{R4+R6} \cdot \frac{R7+R5}{R7}\right)$$

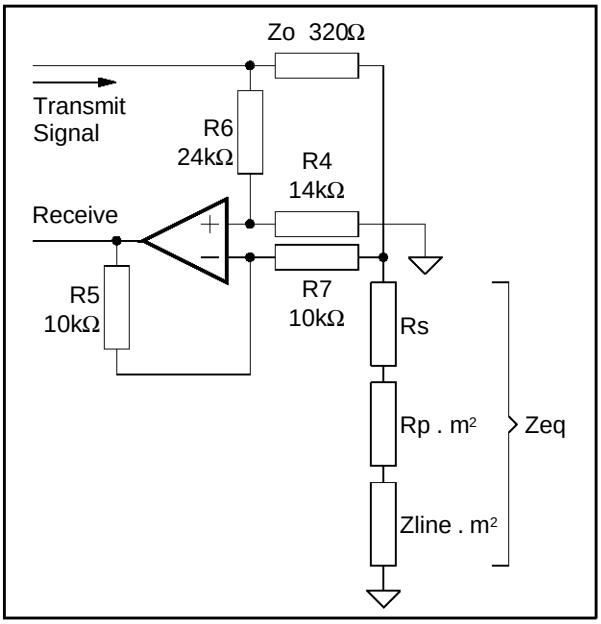
with Z_{EQ} the equivalent impedance of the phone line seen from the secondary.
Maximum loss is achieved when :

$$\frac{Z_{EQ}}{Z_{EQ}+Z_0} = \frac{R4}{R4+R6} \cdot \frac{R7+R5}{R5}$$

Application :
R 5 = 10kΩ, R6 = 24kΩ, R7 = 10kΩ,
R4 = 14kΩ, Z_{EQ} = 905Ω , Z_O = 320Ω

[7] = L_{OSS} = -54dB (Theoretical value, resistor values should be certified at 1% for good performances.)

Figure 22 : Transmit Rejection Simplified AC Schematic (View from Transmit Amplifier, No Signal Received from The Line)



V - ANALOG INTERFACE (continued)

D. Transmit filter

A two-pole continuous time external filter must follow the output pin in order to remove quantization noise. The filter characteristics are :

Transfer function :

$$H = \frac{V_{OUT}}{V_{IN}} = G_T \cdot \frac{1}{1 + 2 \cdot x \cdot s + s^2} \text{ with } s = j \frac{\omega}{2\pi \cdot f_C}$$

DC gain : $G_T = -\frac{R3}{R1}$

Peak factor :

$$x = \frac{1}{2} \cdot \left[\sqrt{\frac{R2}{R3}} + \sqrt{\frac{R3}{R2}} + \frac{\sqrt{R2 \cdot R3}}{R1} \right] \sqrt{\frac{C1}{2 \cdot C2}}$$

Cutoff frequency : $f_C = \frac{1}{2\pi \sqrt{R_2 \cdot R_3 \cdot C_1 \cdot 2 \cdot C_2}}$

with $f_C > 2 \cdot f_S$ [8]

f_C must be at least twice the value of the sampling frequency.

The filter also amplifies (with a gain G_T) the Transmit signal to compensate the loss (L_T) due to the divider made of resistor Z_O and equivalent line impedance Z_{EQ}. The condition that makes the codec maximum output level A_C match with maximum phone line level A_L is :

$$A_C \cdot L_T \cdot G_T = m \cdot A_L$$

with $G_T \frac{R3}{R1}$ and $L_T = \frac{Z_{line} \cdot m^2}{Z_O + Z_{EQ}}$ [9]

Application :

DTMF level is considered as the highest level to be transmitted. Levels used in this application are :

- High Group tone level is -9dBV +2/-2.5
- Low Group tone level is -11dBV +2.5/-2
- The level of the tone in the high group must be 1dB to 4dB higher than the level of the tone in the low group.

In consequence, maximum DTMF signal level is within 1.38 and 2.32 V_{PP}. Maximum phone line level is set to 2.2V (corresponding to a 0dBm single tone).

A_L = 2.2V_{PP}, m = 1,

[9] Zline = 600Ω, Z_{EQ} = 905Ω, Z0 = 320Ω, L_T = 0.490,

A_C = 2*1.25V (differential codec output), A_C = 2.5V_{PP}

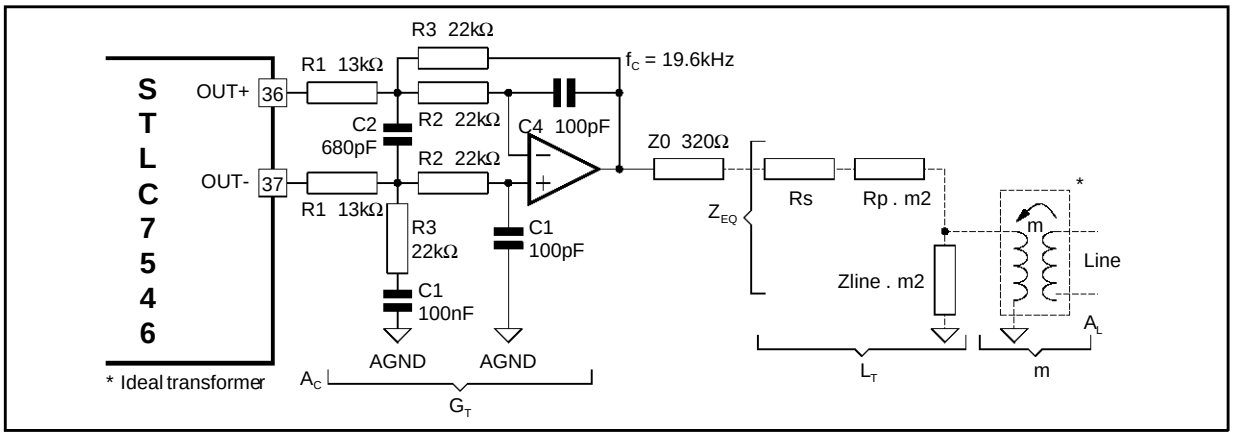
[9] $G_T = A_L \cdot m / (A_C \cdot L_T) = 1.796 = +5.1dB$

Choosing R3 = 22kΩ, (STLC7546 minimum load is 10kΩ,) gives R1 = 13kΩ, G_T = 1.69 = +4.6dB

Note : The maximum line level during V.34 communication is around 1.2V_{PP}. This gives a maximum signal level on codec output pin around 0.6V_{PP} [1.2 · m/(2 · G_T · L_T)] that gives a good dynamic with no distortion.

[10] $A_C \cdot G_T$ = 4.23V_{PP}

Figure 23 : Transmit Filter AC Schematic



VI - PERFORMANCES

We have seen 2 differents kind of analog interface :
- Case A : fully differential
- Case B : single-ended mono supply

VI.1 - Fully Differential

The measurements have been done with a RODHE&SCHWARZ AUDIO ANALYZER 2Hz-300kHz UPD.

Figure 24 is the output spectrum on the receive side, the analog input signal is at 1kHz / -9dBr (relative to V_{REF}). We have the total harmonic distorsion + noise equal to -85dB. The sampling frequency is 9.6kHz and oversampling ratio equal to 160.
Figure 25 is the output spectrum on the receive side, the analog input signal is at 2kHz / -9dBr (relative to V_{REF}). We have the total harmonic distorsion + noise equal to -78dB. The sampling frequency is 22.5kHz and the oversampling ratio is equal to 96.
Figure 26 is the output spectrum is obtained in digital loop-back so we input an analog input signal on the receive side and we measure the analog output signal with rejector on fondamental (transmit and receive noise are added in this case).

The input level is -20dBr at frequency 1kHz.
In the following chart (Figures 28 and 29) we can see the complete dynamic range of the receive side alone and the receive plus transmit (in that case the transmit and receive noise are added).
The measurements have been done for two sampling frequency 9.6kHz and 22.5kHz.

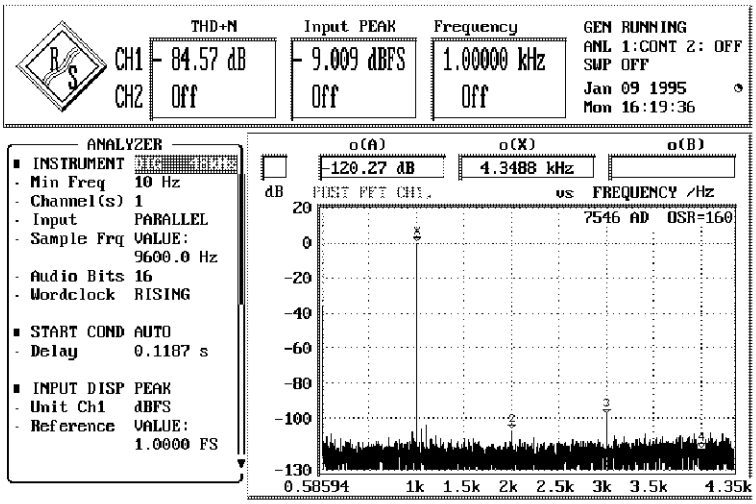
VI.2 - Single-ended Application Board

The measurements have been done with a R&S audio analyzer and ST DSP emulator PC board.

Transmit Side *(D/A)*
We generate a digital waveform at 1kHz and the DSP send the word to the AFE whose output is connected to the R&S analyzer (Figures 27, 30).

Receive Side *(A/D)*
For testing the receive side we use a sine generator type 1051 from BRUEL & KJAER for the input signal and we perform a Fast Fourier Transform on the digital receive signal (Figures 31, 32).

Figure 24



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VI - PERFORMANCES (continued)

Figure 25

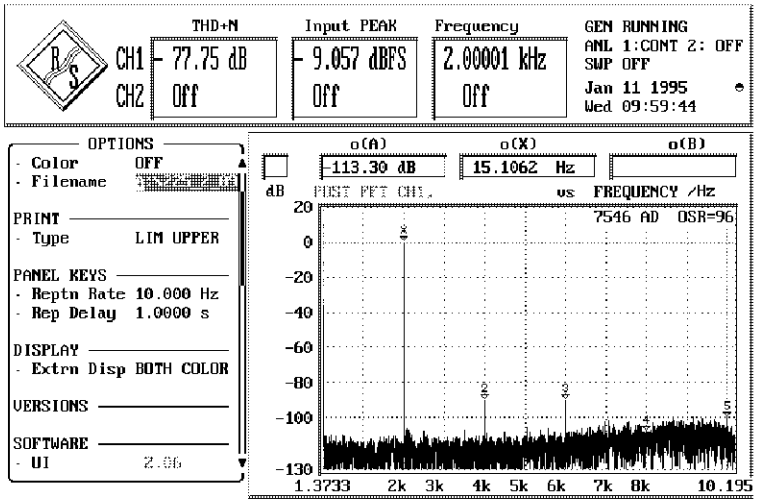

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Figure 26

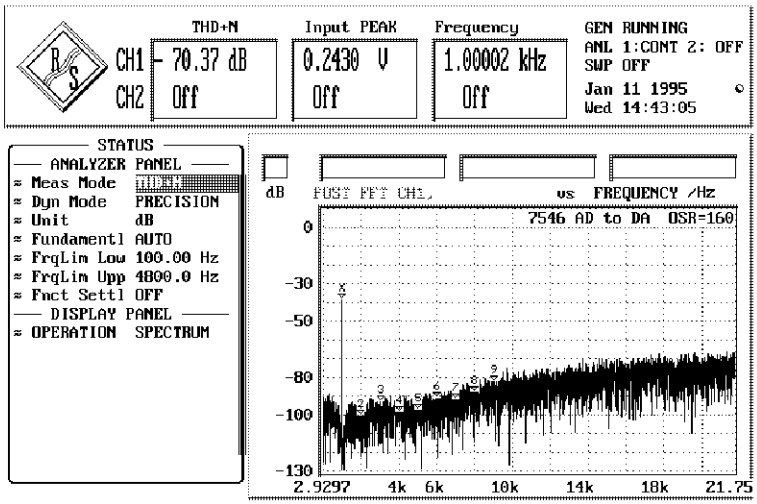

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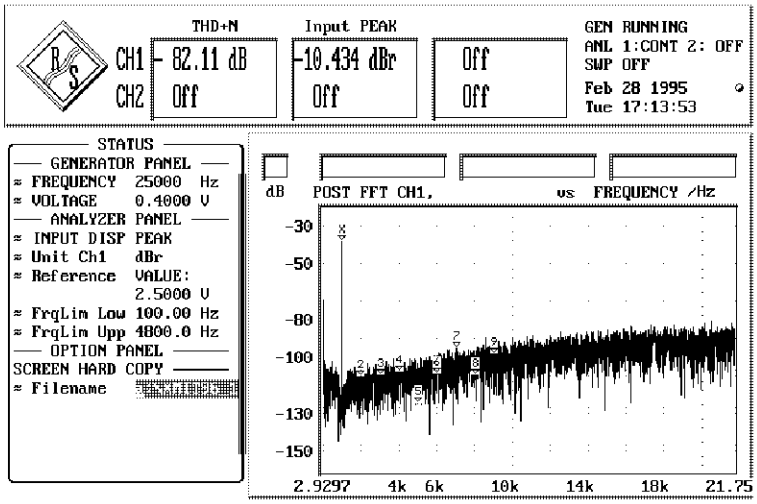
Figure 27



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VI - PERFORMANCES (continued)

Figure 28 : F_S = 9.6kHz, MCLK = 1.536MHz and OVER = 160

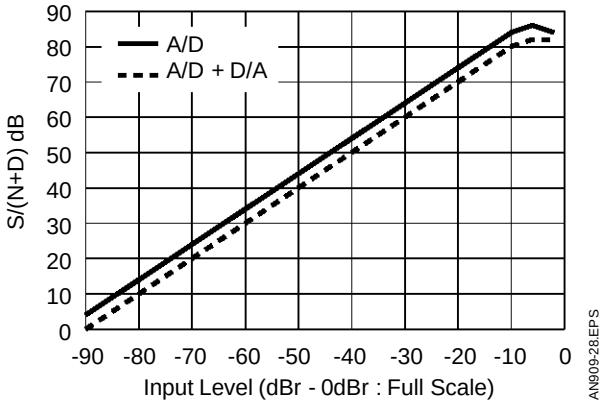


Figure 29 : F_S = 22.5kHz, MCLK = 2.16MHz and OSR = 96

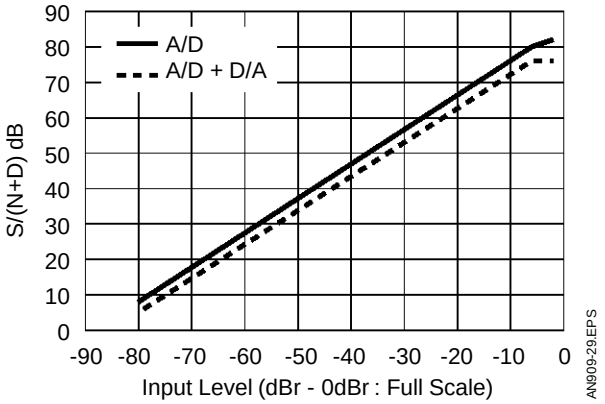


Figure 30 : F_S = 9.6kHz, MCLK = 1.536MHz and OSR = 160

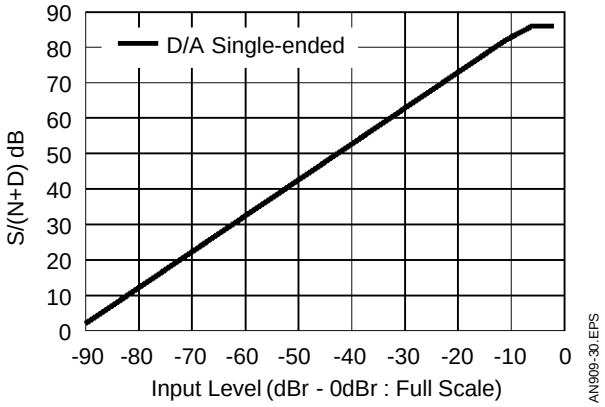
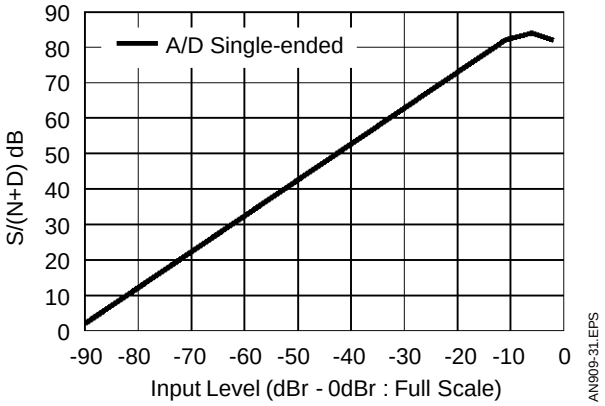


Figure 31 : F_S = 9.6kHz, MCLK = 1.536MHz and OSR = 160



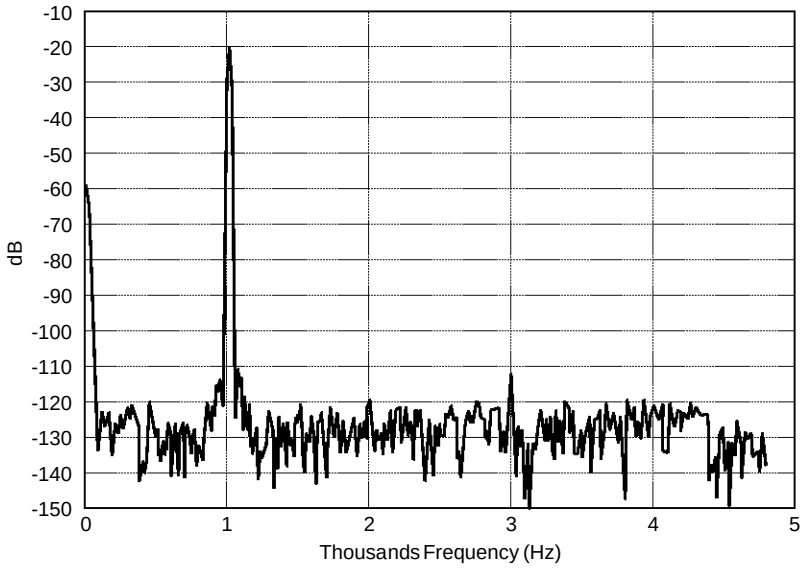
VI - PERFORMANCES (continued)

VI.3 - Conclusions

We have seen different type of analog interface differential and single-ended.We observe difference of around 2dB between the two types.

With standard two layers printed circuit board we have outstanding performances at least 92dB of dynamics.

Figure 32 : F_S = 9.6kHz, MCLK = 1.536MHz



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