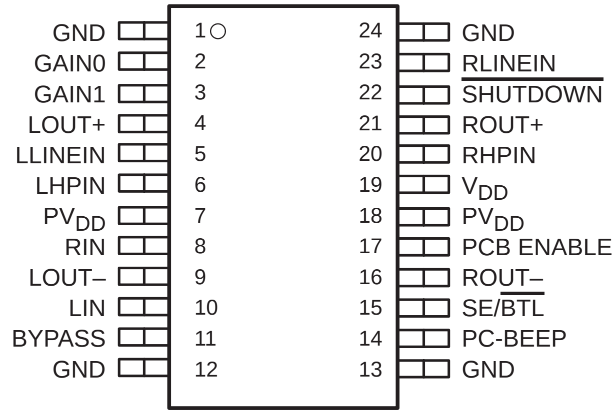
- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **2-W/Ch Output Power Into 3-Ω Load**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0112 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, simplifying the design, and freeing up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0112 has less than 0.8% THD+N across its specified frequency range.

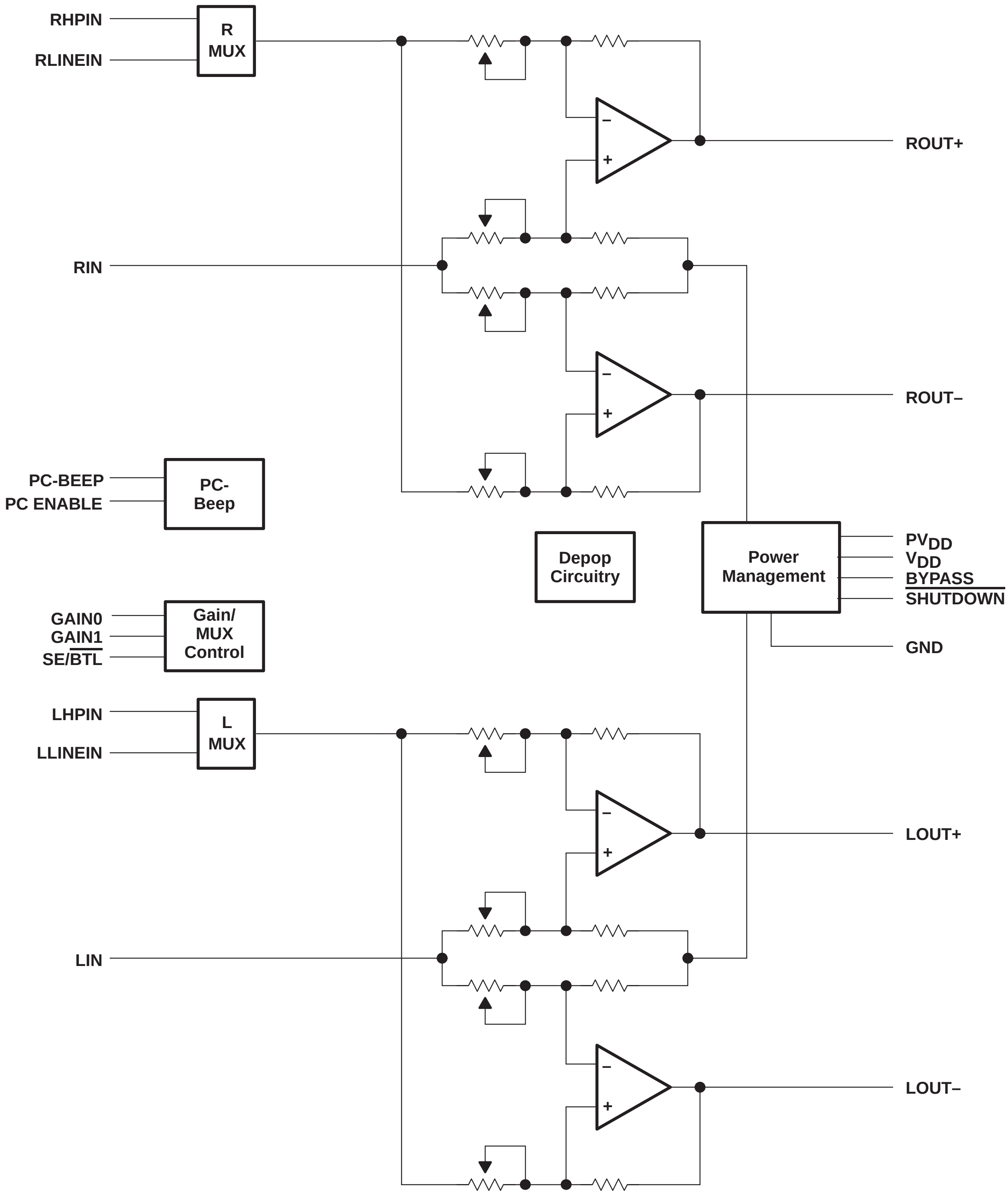
Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is internally configured and controlled by way of two terminals (GAIN0 and GAIN1). BTL gain settings of –2, –6, –12, and –24 V/V are provided, while SE gain is always configured as –1 V/V for headphone drive. An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0112 automatically switches into SE mode when the SE/$\overline{\mathrm{BTL}}$ input is activated, and this reduces the gain to –1 V/V.

The TPA0112 consumes only 6 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to less than 150 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0112 to operate at full power into 8-Ω loads at an ambient temperature of 85°C.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE TSSOP† (PWP)
–40°C to 85°C	TPA0112PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0112PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
GAIN0	2	I	Bit 0 of gain control
GAIN1	3	I	Bit 1 of gain control
GND	1, 12, 13, 24		Ground connection for circuitry. Connected to the thermal pad.
LHPIN	6	I	Left channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs.
LLINEIN	5	I	Left channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left channel positive output in BTL mode and positive output in SE mode
LOUT–	9	O	Left channel negative output in BTL mode and high-impedance in SE mode
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
PCB ENABLE	17	I	If this terminal is high, the detection circuitry for PC-BEEP is overridden and passes PC-BEEP through the amplifier, regardless of its amplitude. If PCB ENABLE is floating or low, the amplifier continues to operate normally.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs.
RLINEIN	23	I	Right channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right channel positive output in BTL mode and positive output in SE mode
ROUT–	16	O	Right channel negative output in BTL mode and high-impedance in SE mode
$\overline{\text{SHUTDOWN}}$	22	I	Places entire IC in shutdown mode when held low, except PC-BEEP remains active
SE/$\overline{\text{BTL}}$	15	I	Input MUX control input. When this terminal is held high, the LHPIN or RHPIN and SE output is selected. When this terminal is held low, the LLINEIN or RLINEIN and BTL output are selected.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} . . . . 6 V
Input voltage, V_I . . . . –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation . . . . internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{\text{BTL}}$	4		V
	$\overline{\text{SHUTDOWN}}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{\text{BTL}}$		3	V
	$\overline{\text{SHUTDOWN}}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	$V_I = 0$, $A_V = 2$			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4 V to 5 V		77		dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
I_{DD}	Supply current	BTL mode		6	8	mA
		SE mode		3	4	
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	μA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω, Gain = –2 V/V, BTL mode

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%, R_L = 4 Ω	f = 1 kHz,		1.9		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.75%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 μF	BTL mode		68		dB
SNR	Signal-to-noise ratio				105		dB
V_n	Noise output voltage	C_B = 0.47 μF, f = 20 Hz to 20 kHz	BTL mode		16		μV_{RMS}
			SE mode		30		
Z_I	Input impedance				See Table 1		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4–7, 10–13, 16–19, 21
		vs Frequency	2, 3, 8, 9, 14, 15, 20, 22
		vs Output voltage	23
V_n	Output noise voltage	vs Bandwidth	24
	Supply ripple rejection ratio	vs Frequency	25, 26
	Crosstalk	vs Frequency	27–29
	Shutdown attenuation	vs Frequency	30
SNR	Signal-to-noise ratio	vs Frequency	31
	Closed loop respone		32–35
P_O	Output power	vs Load resistance	36, 37
P_D	Power dissipation	vs Output power	38, 39
		vs Ambient temperature	40

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 41) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

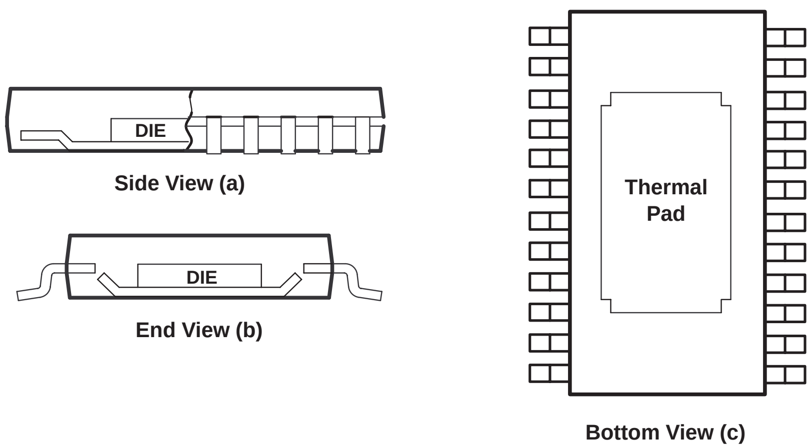
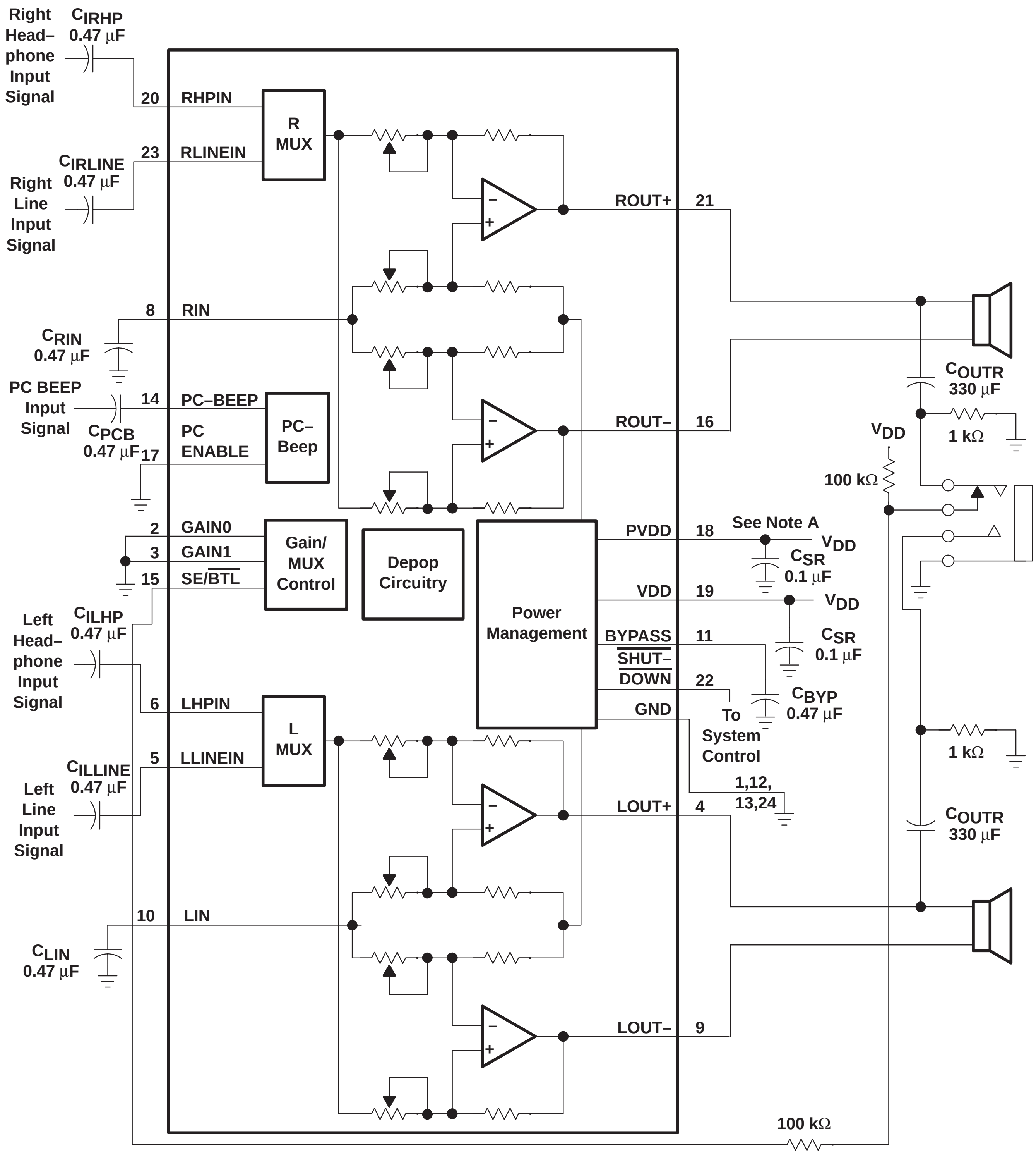


Figure 41. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

selection of components

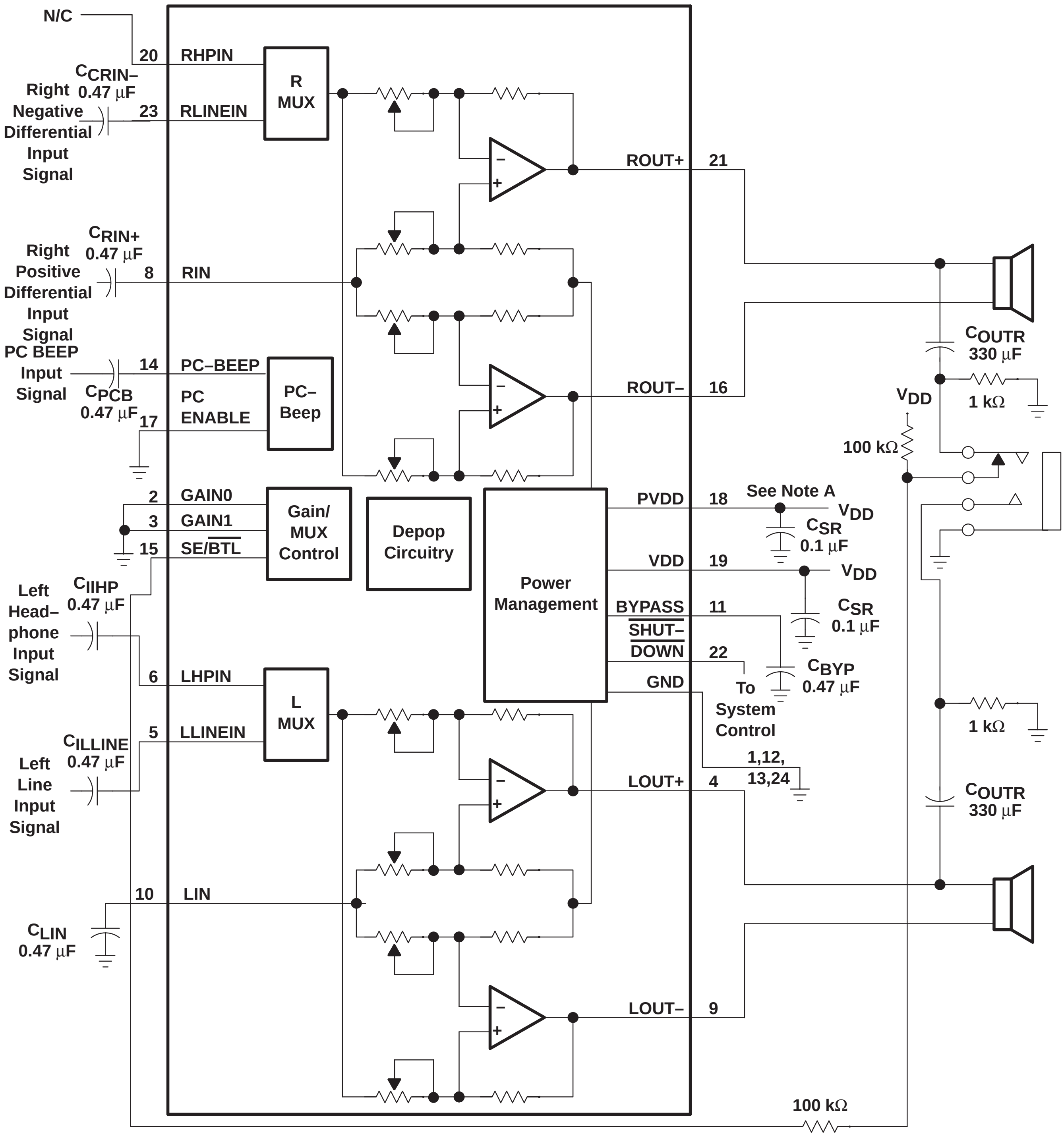
Figure 42 and Figure 43 are a schematic diagrams of typical notebook computer application circuits.



NOTE A: A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 42. Typical TPA0112 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



NOTE A: A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 43. Typical TPA0112 Application Circuit Using Differential Inputs