National Semiconductor

April 1998

LF411
Low Offset, Low Drift JFET Input Operational Amplifier

General Description

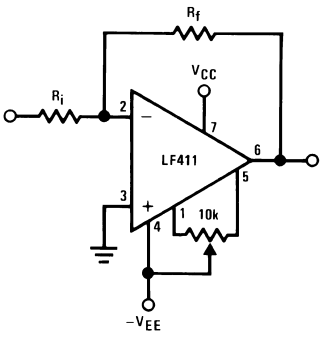
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage: 0.5 mV(max)
- Input offset voltage drift: 10 µV/°C(max)
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/$\sqrt{\text{Hz}}$
- Wide gain bandwidth: 3 MHz(min)
- High slew rate: 10V/µs(min)
- Low supply current: 1.8 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion A_V=10, R_L=10k, V_O=20 Vp-p, BW=20 Hz−20 kHz: <0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 µs

Typical Connection



DS005655-1

Ordering Information

LF411XYZ

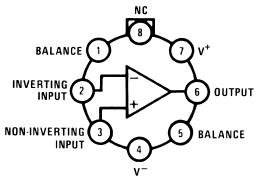
X indicates electrical grade

Y indicates temperature range
- "M" for military
- "C" for commercial

Z indicates package type
- "H" or "N"

Connection Diagrams

Metal Can Package

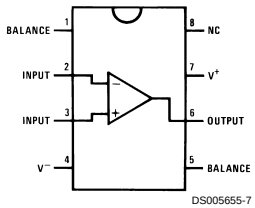


DS005655-5

Note: Pin 4 connected to case.

Top View
Order Number LF411ACH
or LF411MH/883 (Note 1)
See NS Package Number H08A

Dual-In-Line Package

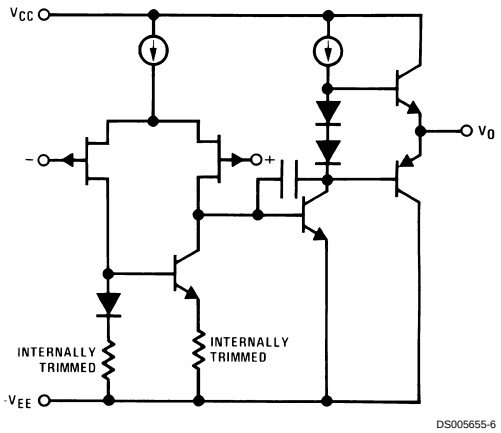


DS005655-7

Top View
Order Number LF411ACN,
LF411CN or LF411MJ/883 (Note 1)
See NS Package Number N08E or J08A

BI-FET II™ is a trademark of National Semiconductor Corporation.

Simplified Schematic



DS005655-6

Note 1: Available per JM38510/11904

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF411A	LF411
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 3)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package
Power Dissipation (Notes 4, 11)	670 mW	670 mW
$T_j$max	150˚C	115˚C
θ_jA	162˚C/W (Still Air) 65˚C/W (400 LF/min Air Flow)	120˚C/W
θ_jC	20˚C/W	
Operating Temp. Range	(Note 5)	(Note 5)
Storage Temp. Range	−65˚C≤T_A≤150˚C	−65˚C≤T_A≤150˚C
Lead Temp. (Soldering, 10 sec.)	260˚C	260˚C
ESD Tolerance	Rating to be determined.	

DC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions		LF411A			LF411			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25˚C			0.3	0.5		0.8	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ (Note 7)			7	10		7	20 (Note 7)	µV/˚C
I_{OS}	Input Offset Current	V_S=±15V (Notes 6, 8)	T_j=25˚C		25	100		25	100	pA
			T_j=70˚C			2			2	nA
			T_j=125˚C			25			25	nA
I_B	Input Bias Current	V_S=±15V (Notes 6, 8)	T_j=25˚C		50	200		50	200	pA
			T_j=70˚C			4			4	nA
			T_j=125˚C			50			50	nA
R_{IN}	Input Resistance	T_j=25˚C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, V_O=±10V, R_L=2k, T_A=25˚C		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	R_S≤10k		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 9)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

AC Electrical Characteristic (Note 6)

Symbol	Parameter	Conditions	LF411A			LF411			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	V_S=±15V, T_A=25˚C	10	15		8	15		V/µs
GBW	Gain-Bandwidth Product	V_S=±15V, T_A=25˚C	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25˚C, R_S=100Ω, f=1 kHz		25			25		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_A=25˚C, f=1 kHz		0.01			0.01		pA/$\sqrt{Hz}$

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

AC Electrical Characteristic (Note 6) (Continued)

Note 4: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_jA.

Note 5: These devices are available in both the commercial temperature range $0^\circ C \le T_A \le 70^\circ C$ and the military temperature range $-55^\circ C \le T_A \le 125^\circ C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 6: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF411A and for $V_S = \pm 15V$ for the LF411. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 7: The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

Note 8: The input bias currents are junction leakage currents which approximately double for every $10^\circ C$ increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

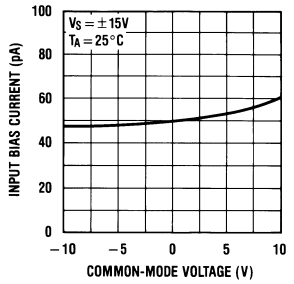
Note 9: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from ±15V to ±5V for the LF411 and from ±20V to ±5V for the LF411A.

Note 10: RETS 411X for LF411MH and LF411MJ military specifications.

Note 11: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

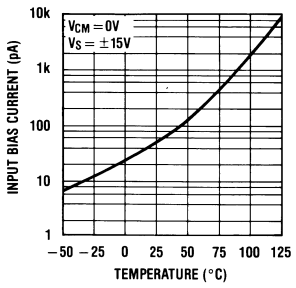
Typical Performance Characteristics

Input Bias Current



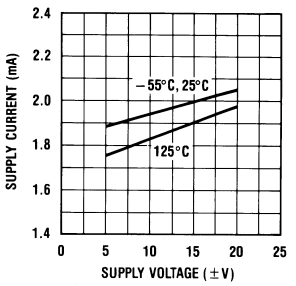
DS005655-11

Input Bias Current



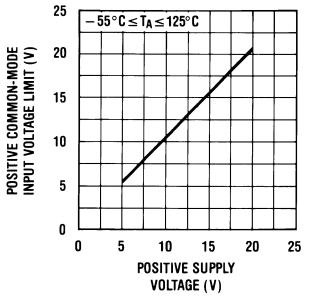
DS005655-12

Supply Current



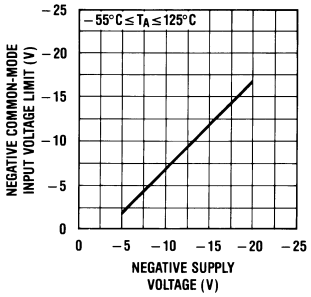
DS005655-13

Positive Common-Mode Input Voltage Limit



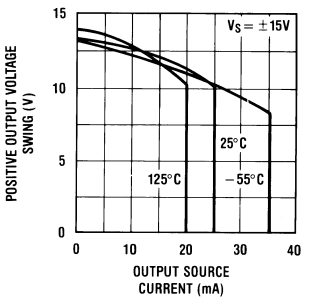
DS005655-14

Negative Common-Mode Input Voltage Limit



DS005655-15

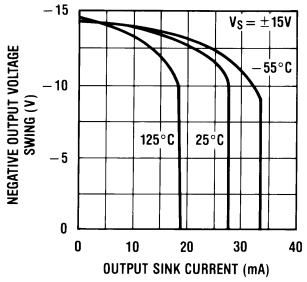
Positive Current Limit



DS005655-16

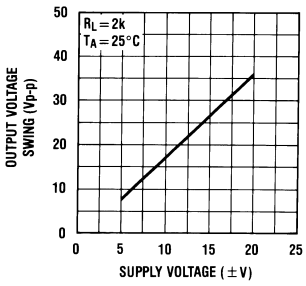
Typical Performance Characteristics (Continued)

Negative Current Limit



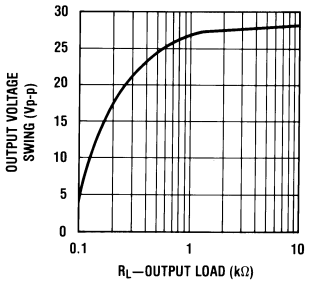
DS005655-17

Output Voltage Swing



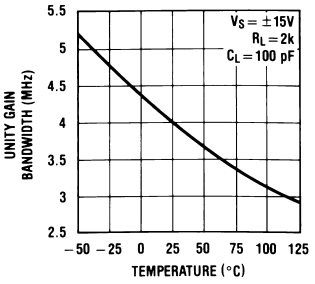
DS005655-18

Output Voltage Swing



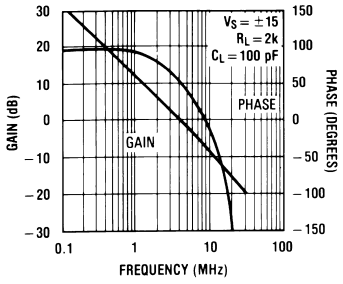
DS005655-19

Gain Bandwidth



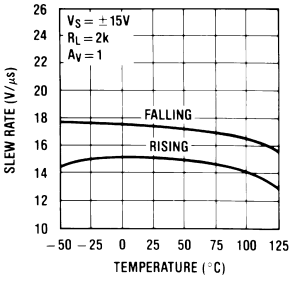
DS005655-20

Bode Plot



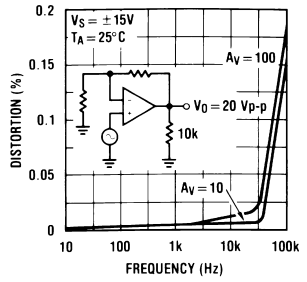
DS005655-21

Slew Rate



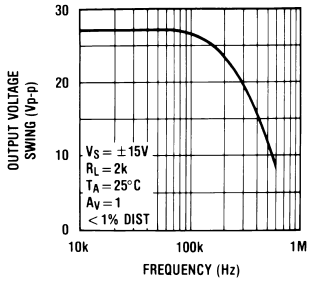
DS005655-22

Distortion vs Frequency



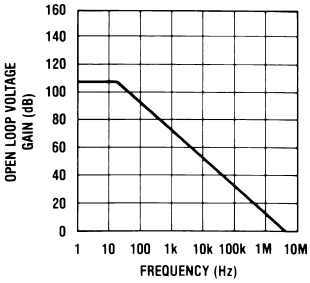
DS005655-23

Undistorted Output Voltage Swing



DS005655-24

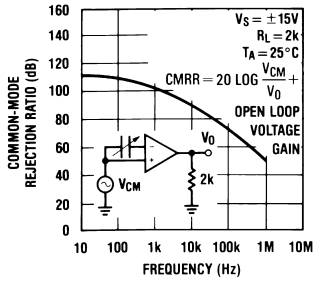
Open Loop Frequency Response



DS005655-25

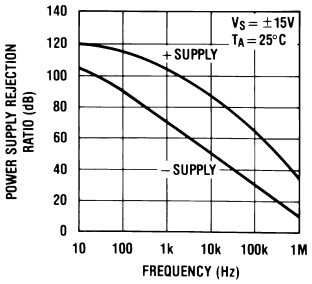
Typical Performance Characteristics (Continued)

Common-Mode Rejection Ratio



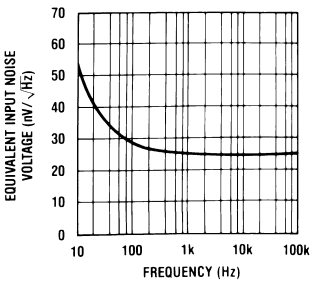
DS005655-26

Power Supply Rejection Ratio



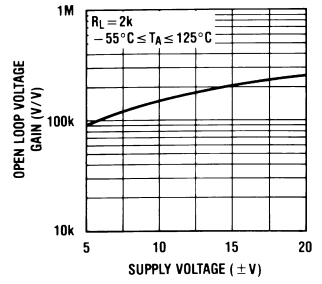
DS005655-27

Equivalent Input Noise Voltage



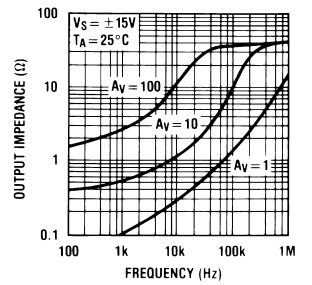
DS005655-28

Open Loop Voltage Gain



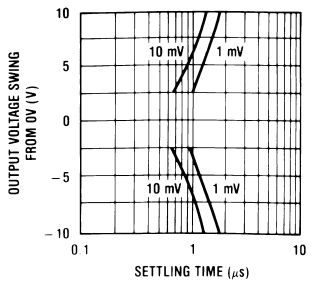
DS005655-29

Output Impedance



DS005655-30

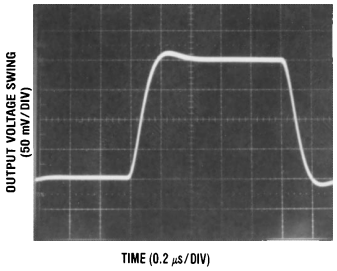
Inverter Settling Time



DS005655-31

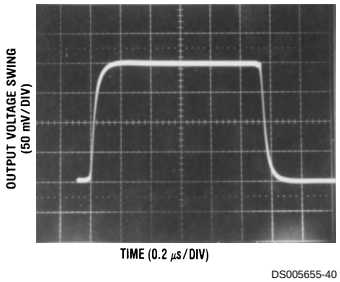
Pulse Response R_L=2 kΩ, C_L10 pF

Small Signal Inverting



DS005655-39

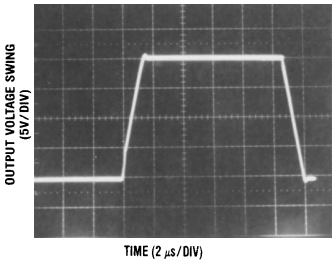
Small Signal Non-Inverting



DS005655-40

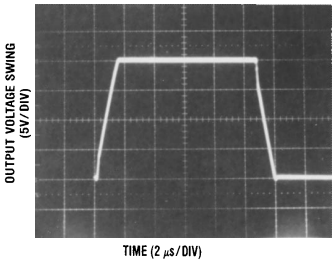
Pulse Response R_L=2 kΩ, C_L10 pF (Continued)

Large Signal Inverting



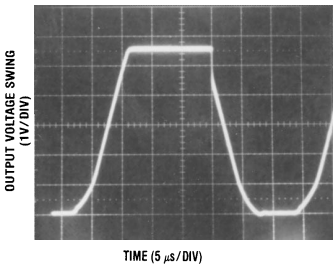
DS005655-41

Large Signal Non-Inverting



DS005655-42

Current Limit (R_L=100Ω)



DS005655-43

Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

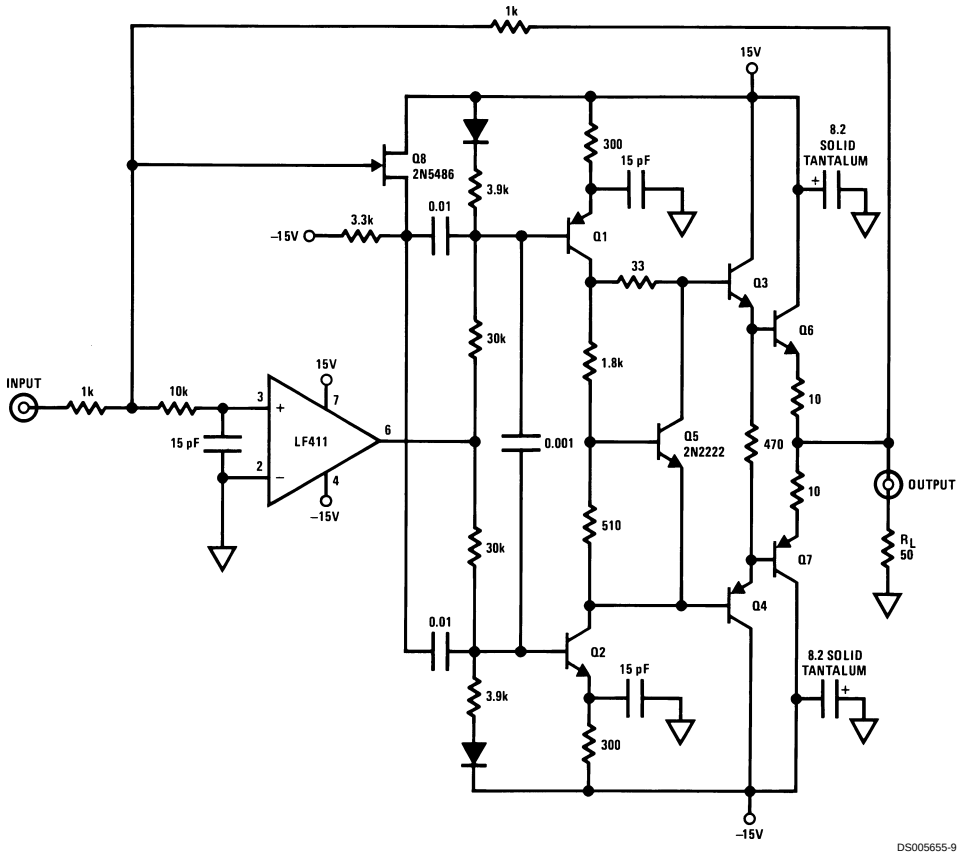
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed

Application Hints (Continued)

from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

High Speed Current Booster

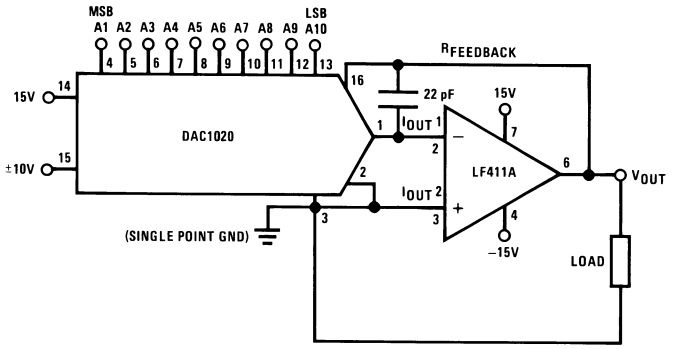


DS005655-9

PNP=2N2905
NPN=2N2219 unless noted
TO-5 heat sinks for Q6-Q7

Typical Applications (Continued)

10-Bit Linear DAC with No V_{OS} Adjust



DS005655-32

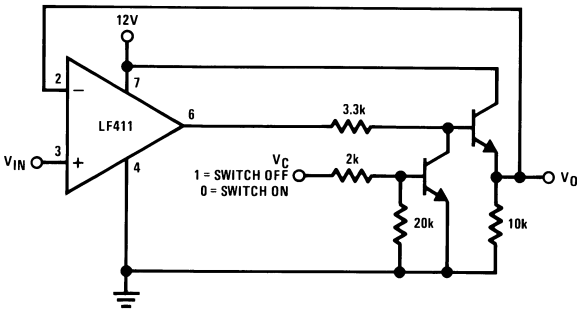
$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

$$-10V \leq V_{REF} \leq 10V$$

$$0 \leq V_{OUT} \leq -\frac{1023}{1024} V_{REF}$$

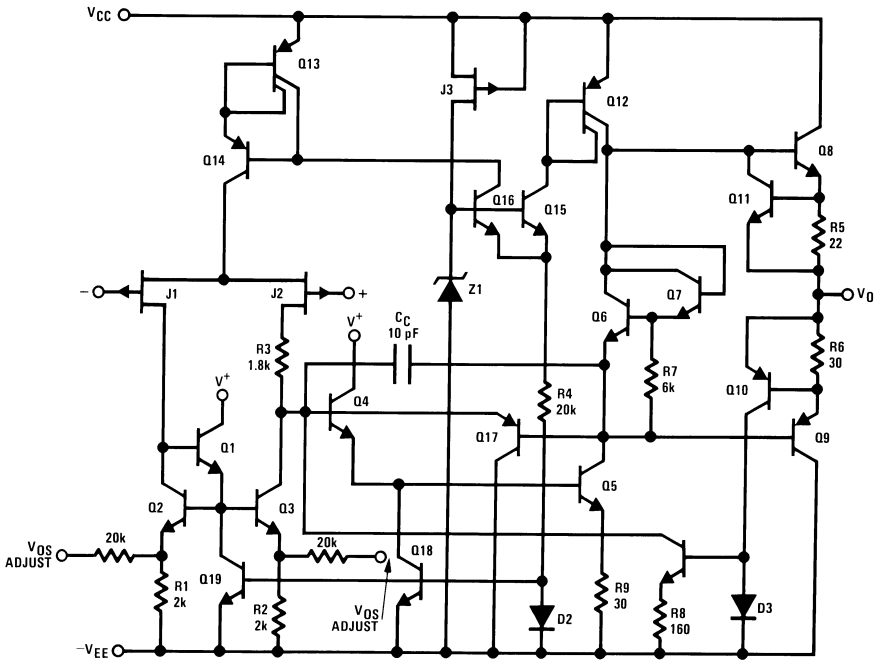
where A_N=1 if the A_N digital input is high
A_N=0 if the A_N digital input is low

Single Supply Analog Switch with Buffered Output

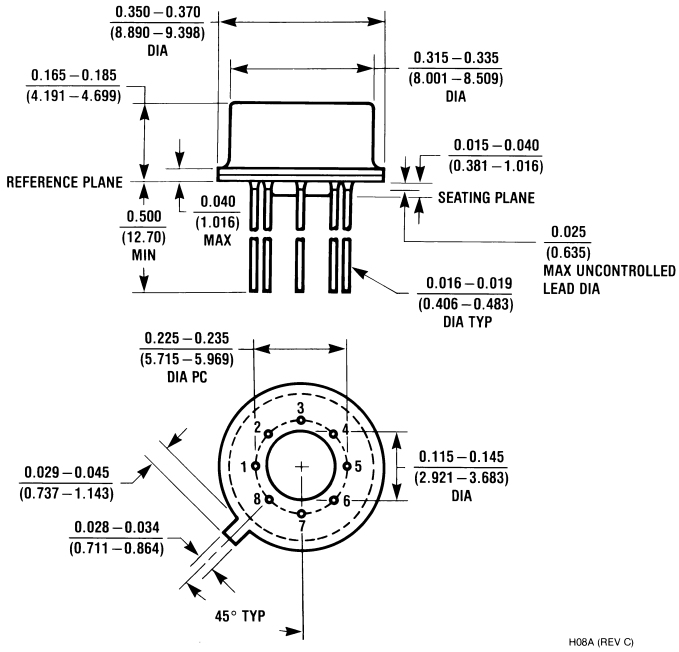


DS005655-33

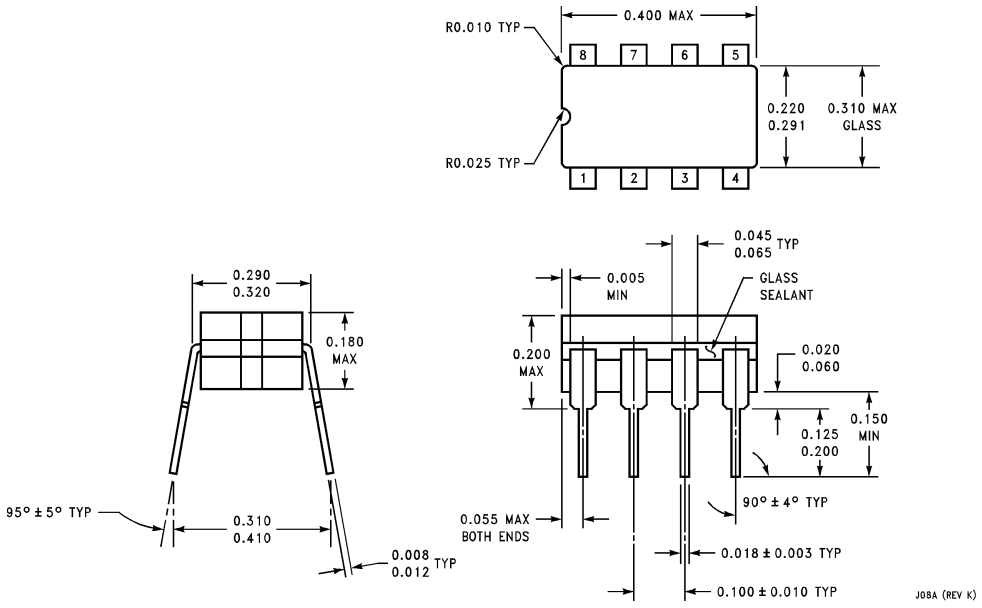
Detailed Schematic



Physical Dimensions inches (millimeters) unless otherwise noted

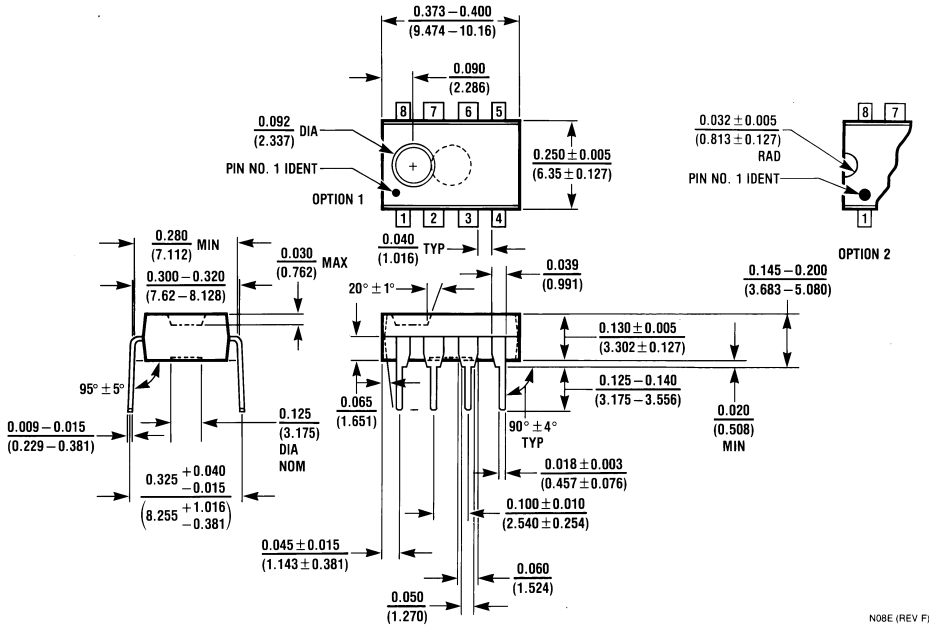


Metal Can Package (H)
Order Number LF411MH/883 or LF411ACH
NS Package Number H08A



Ceramic Dual-In-Line Package (J)
Order Number LF411MJ/883
NS Package Number J08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number LF411ACN or LF411CN
NS Package Number N08E

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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