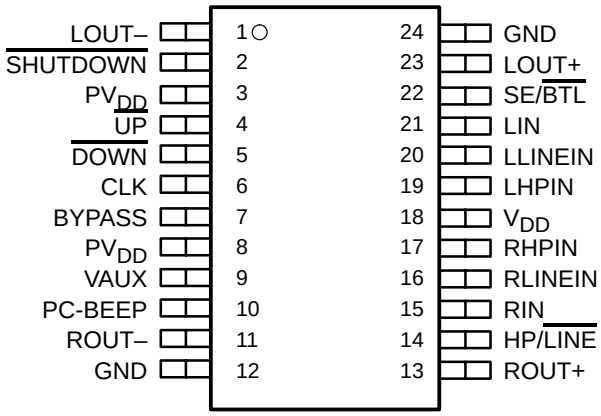
- **Internal Memory Restores Volume Setting After Shutdown or Power Down**
- **Digital Volume Control From 20 dB to –40 dB**
- **2-W/Ch Output Power Into 3-Ω Load**
- **Stereo Input MUX**
- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **PC-Beep Input**
- **Depop Circuitry**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0252 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, which simplifies the design and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0252 has less than 0.3% THD+N across its specified frequency range.

Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is controlled by two terminals, $\overline{\text{UP}}$ and $\overline{\text{DOWN}}$. There are 31 discrete steps covering the range of 20 dB (maximum volume setting) to –40 dB (minimum volume setting) in 2 dB steps. By pressing either button momentarily, the volume steps up or down 2 dB. By continuing to hold the button down, the device starts stepping through volume settings at a rate determined by the capacitor on the CLK terminal. An internal input MUX, controlled by the HP/$\overline{\text{LINE}}$ pin, allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0252 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated. This effectively reduces the gain by 6 dB.

The TPA0252 includes a VAUX terminal that is used to power the volume-setting registers when the device is in $\overline{\text{SHUTDOWN}}$, and even if the main V_{DD} power supply is removed. As long as the VAUX terminal is held above 3 V, the registers are maintained. If the VAUX terminal is allowed to go below 3 V, then the data in the registers is lost, and the default gain of –10 dB is loaded into the registers.

The TPA0252 consumes only 9 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to less than 150 μA.

The PowerPAD™ package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA0252 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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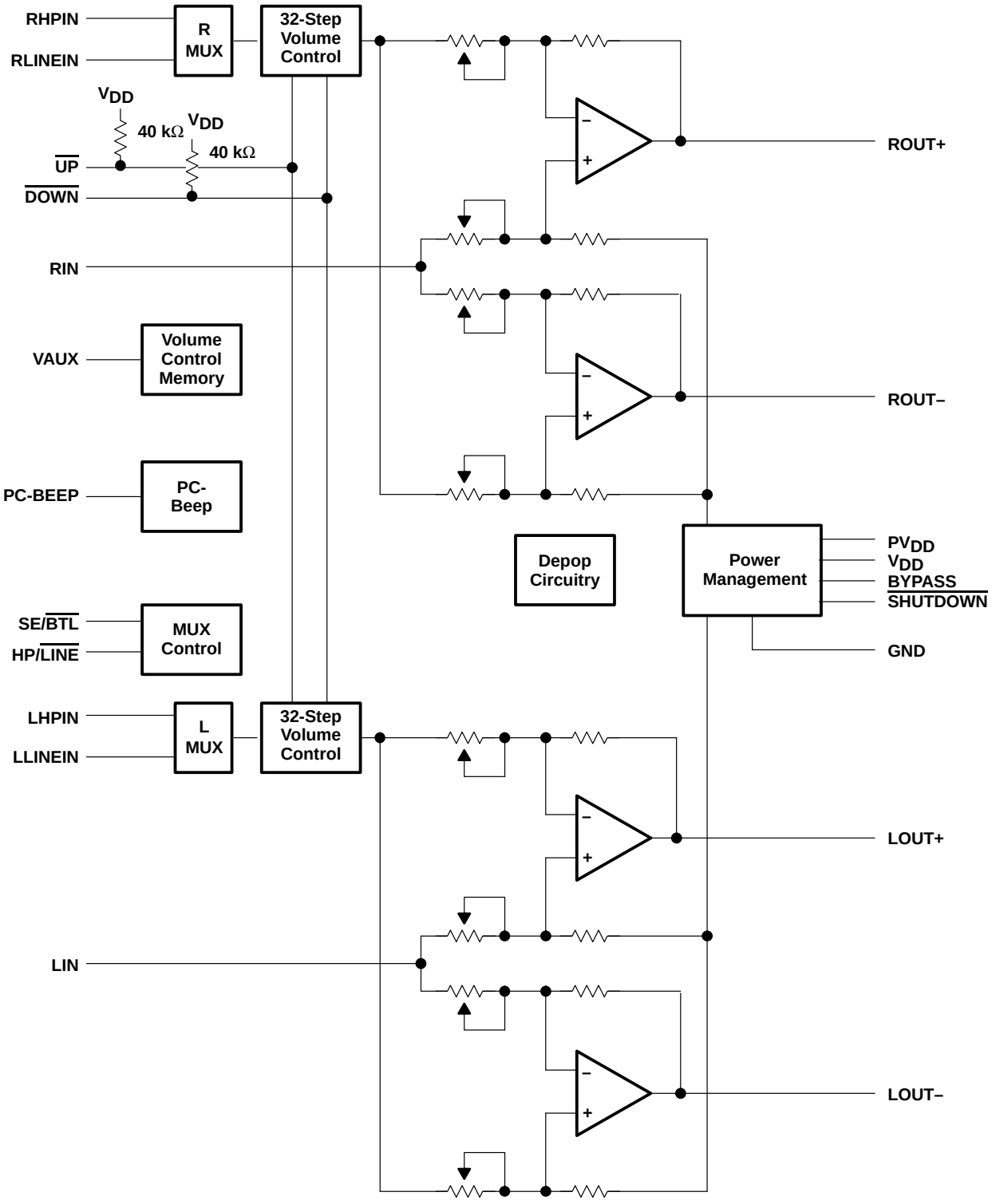
functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0252PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0252PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	7		Tap to voltage divider for internal mid-supply bias generator
CLK	6	I	If a 47-nF capacitor is attached, the TPA0252 generates an internal clock. An external clock can override the internal clock input to this terminal.
$\overline{\text{DOWN}}$	5	I	A momentary pulse on this terminal decreases the volume level by 2 dB. Holding the terminal low for a period of time steps the amplifier through the volume levels at a rate determined by the capacitor on the CLK terminal.
GND	12, 24		Ground connection for circuitry. Connected to thermal pad
HP/$\overline{\text{LINE}}$	14	I	Input MUX control. When terminal is high, the LHPIN and RHPIN inputs are selected. When terminal is low, LLINEIN and RLINEIN inputs are selected.
LHPIN	19	I	Left-channel headphone input, selected when HP/$\overline{\text{LINE}}$ is held high
LIN	21	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	20	I	Left-channel line negative input, selected when HP/$\overline{\text{LINE}}$ is held low
LOUT+	23	O	Left-channel positive output in $\overline{\text{BTL}}$ mode and positive in SE mode
LOUT–	1	O	Left-channel negative output in $\overline{\text{BTL}}$ mode and high impedance in SE mode
PC-BEEP	10	I	The input for PC beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP.
PV_{DD}	3, 8	I	Power supply for output stage
RHPIN	17	I	Right channel headphone input, selected when HP/$\overline{\text{LINE}}$ is held high
RIN	15	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	16	I	Right-channel line input, selected when HP/$\overline{\text{LINE}}$ is held low
ROUT+	13	O	Right-channel positive output in $\overline{\text{BTL}}$ mode and positive in SE mode
ROUT–	11	O	Right-channel negative output in $\overline{\text{BTL}}$ mode and high impedance in SE mode
SE/$\overline{\text{BTL}}$	22	I	Input and output MUX control. When this terminal is held high SE outputs are selected. When this terminal is held low BTL outputs are selected.
$\overline{\text{SHUTDOWN}}$	2	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
$\overline{\text{UP}}$	4	I	A momentary pulse on this terminal increases the volume level by 2 dB. Holding the terminal low for a period of time steps the amplifier through the volume levels at a rate determined by the capacitor on the CLK terminal.
VAUX	9	I	Volume control memory supply. Connect to system auxiliary that stays active when device is powered down.
V_{DD}	18	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} . . . . . 6 V
Input voltage, V_I . . . . . –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation . . . . . internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ See the Texas Instruments document, *PowerPAD™ Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD™ package. The thermal data measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD™* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
Volume control memory supply voltage, V_{AUX}		3	5.5	V
High-level input voltage, V_{IH}	CLK	4.5		V
	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$, $\overline{\text{UP}}$, $\overline{\text{DOWN}}$	4		
	$\overline{\text{SHUTDOWN}}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$		3	V
	$\overline{\text{SHUTDOWN}}$		0.8	
	$\overline{\text{UP}}$, $\overline{\text{DOWN}}$, CLK		0.5	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage (measured differentially)		V_I = 0,	A_V = 2			25	mV
	Supply ripple rejection ratio		V_{DD} = 4.9 V to 5.1 V			67		dB
$\|I_{IH}\|$	High-level input current	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$, $\overline{\text{SHUTDOWN}}$, $\overline{\text{UP}}$, $\overline{\text{DOWN}}$	V_{DD} = 5.5 V,	$V_I = V_{DD}$			1	μA
$\|I_{IL}\|$	Low-level input current	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$, $\overline{\text{SHUTDOWN}}$	V_{DD} = 5.5 V,	V_I = 0 V			1	μA
		$\overline{\text{UP}}$, $\overline{\text{DOWN}}$					125	μA
I_{DD}	Supply current		BTL mode			9	15	mA
			SE mode			4.5	7.5	
$I_{DD(SD)}$	Supply current, shutdown mode					150	300	μA
$I_{DD(VAUX)}$	Supply current, VAUX pin (see Figure 29)		VAUX = 5 V,	V_{DD} = 0 V		0.7		nA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω, Gain = 20 dB, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%,	f = 1 kHz		2		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.3%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 μF	BTL mode		65		dB
			SE mode, Gain = 14 dB		60		
V_n	Noise output voltage	C_B = 0.47 μF, f = 20 Hz to 20 kHz	BTL mode, Gain = 6 dB		17		μV_{RMS}
			SE mode, Gain = 0 dB		44		

TYPICAL CHARACTERISTICS

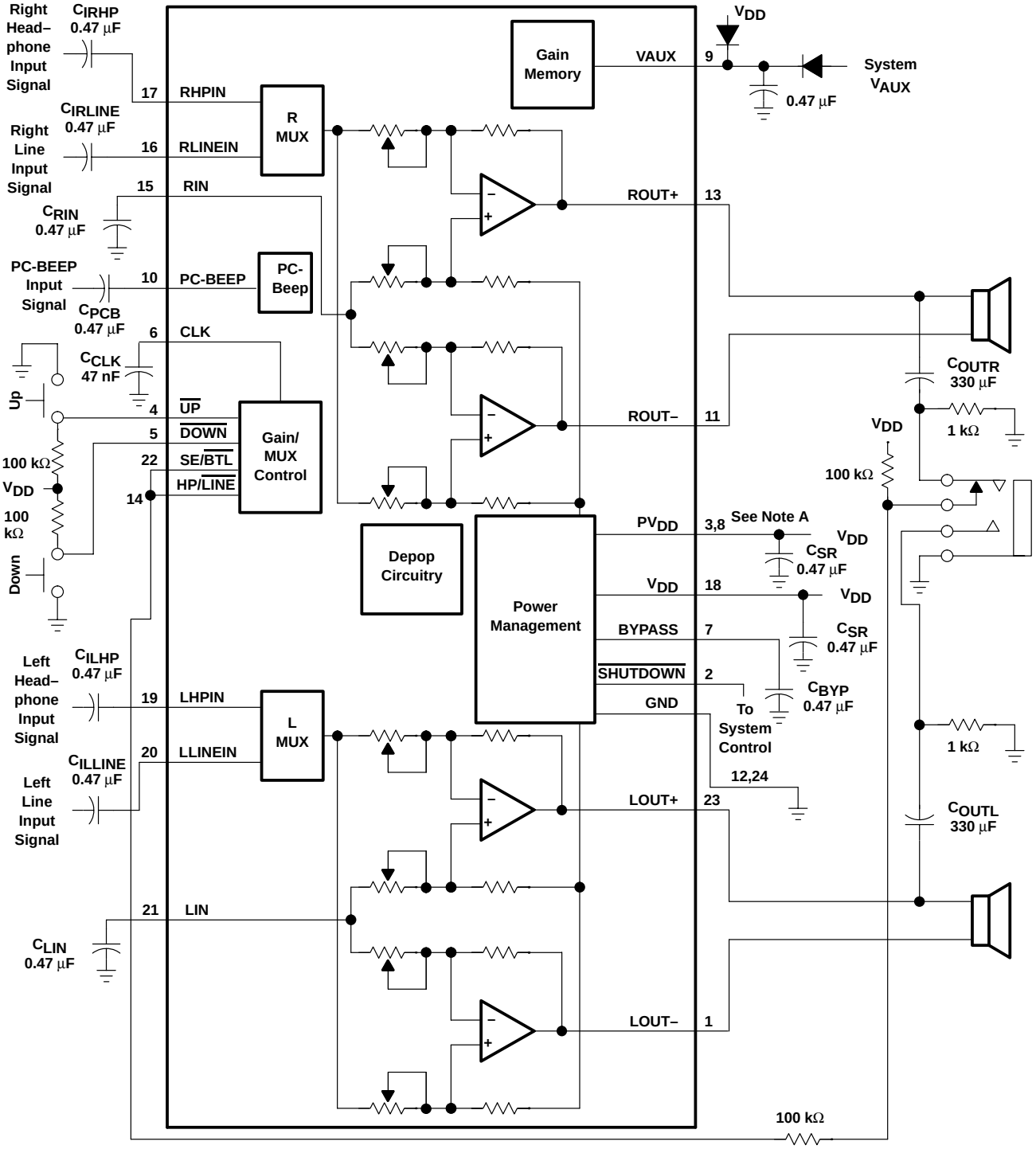
Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4, 6, 8, 10
		vs Voltage gain	2
		vs Frequency	3, 5, 7, 9, 11, 12
V_n	Output noise voltage	vs Frequency	13
	Supply ripple rejection ratio	vs Frequency	14, 15
	Crosstalk	vs Frequency	16, 17, 18
	Shutdown attenuation	vs Frequency	19
SNR	Signal-to-noise ratio	vs Frequency	20
	Closed loop response		21, 22
P_O	Output power	vs Load resistance	23, 24
P_D	Power dissipation	vs Output power	25, 26
		vs Ambient temperature	27
R_I	Input resistance	vs Gain	28
$I_{DD(VAUX)}$	Supply current	vs V_{AUX}	29

APPLICATION INFORMATION

selection of components

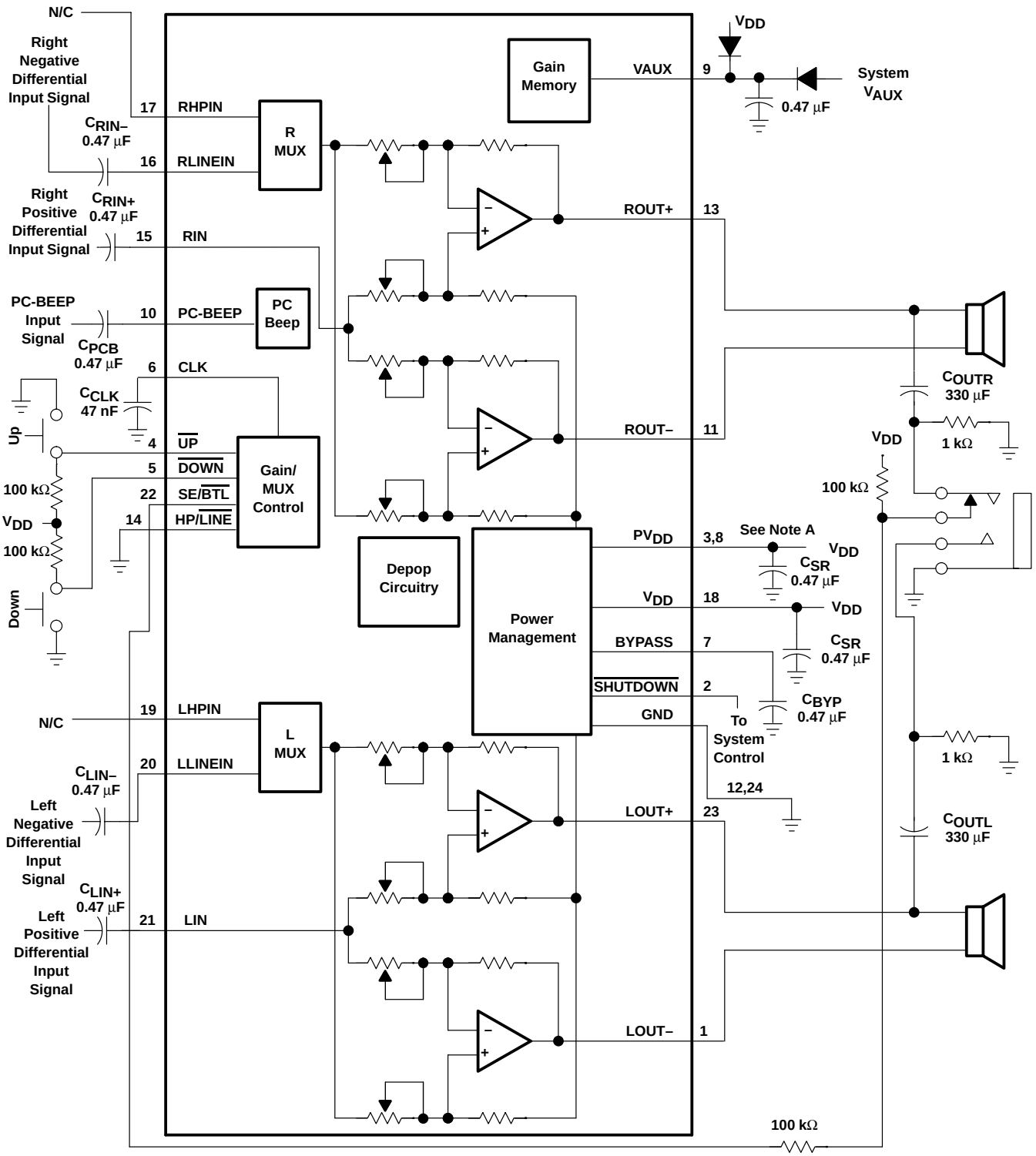
Figures 30 and 31 are schematic diagrams of typical notebook computer application circuits.



NOTE A: A 0.47 µF ceramic capacitor must be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater must be placed near the audio power amplifier.

Figure 30. Typical TPA0252 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



NOTE A: A 0.47 µF ceramic capacitor must be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater must be placed near the audio power amplifier.

Figure 31. Typical TPA0252 Application Circuit Using Differential Inputs