

2SC3799, 2SC3799A

Silicon NPN triple diffusion planar type
For high breakdown voltage high-speed switching

■ Features

- High-speed switching
- High collector to base voltage V_{CBO}
- Low collector to emitter saturation voltage $V_{CE(sat)}$
- Full-pack package which can be installed to the heat sink with one screw

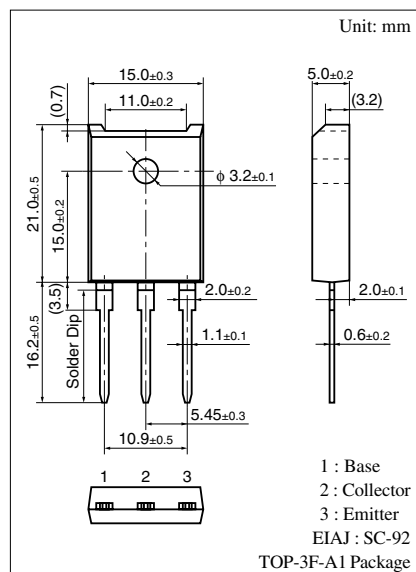
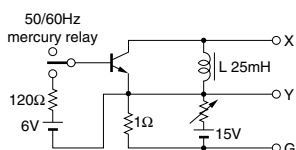
■ Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

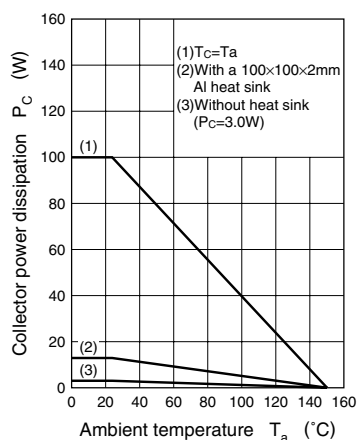
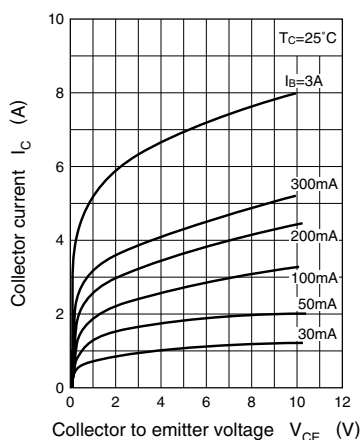
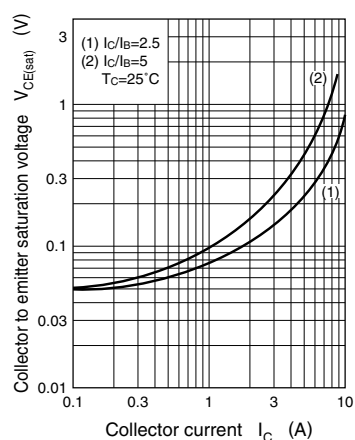
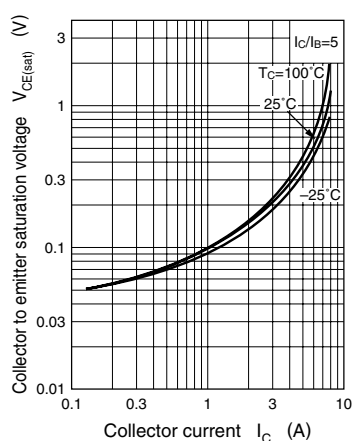
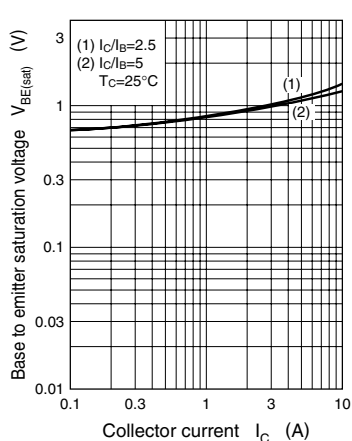
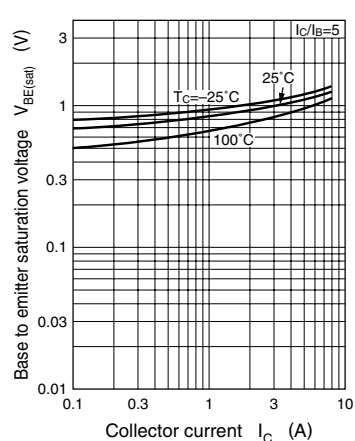
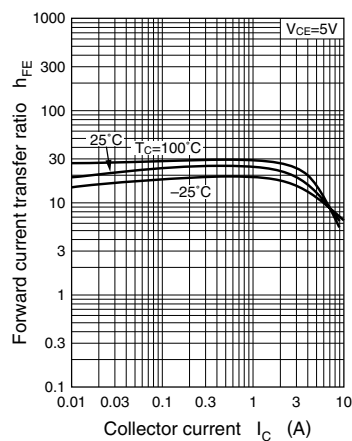
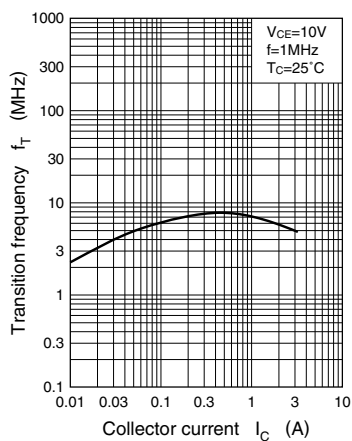
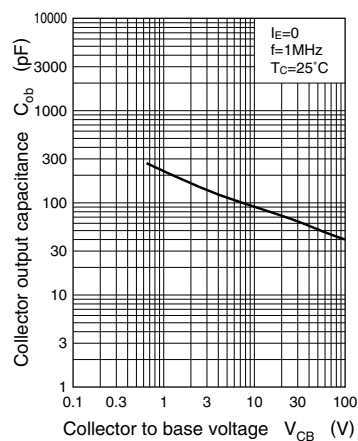
Parameter		Symbol	Rating	Unit
Collector to base voltage	2SC3799	V_{CBO}	800	V
	2SC3799A		900	
Collector to emitter voltage	2SC3799	V_{CES}	800	V
	2SC3799A		900	
Collector to emitter voltage		V_{CEO}	500	V
Emitter to base voltage		V_{EBO}	8	V
Peak collector current		I_{CP}	15	A
Collector current		I_C	7	A
Base current		I_B	4	A
Collector power dissipation	$T_C = 25^\circ\text{C}$	P_C	100	W
	$T_a = 25^\circ\text{C}$		3	
Junction temperature		T_j	150	$^\circ\text{C}$
Storage temperature		T_{stg}	-55 to +150	$^\circ\text{C}$

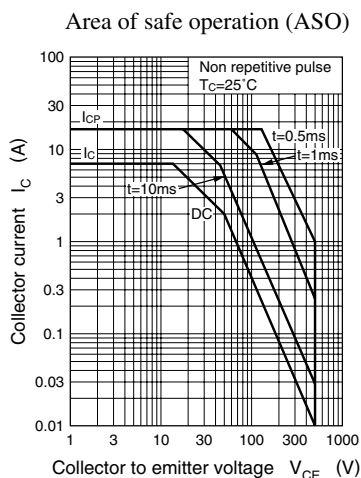
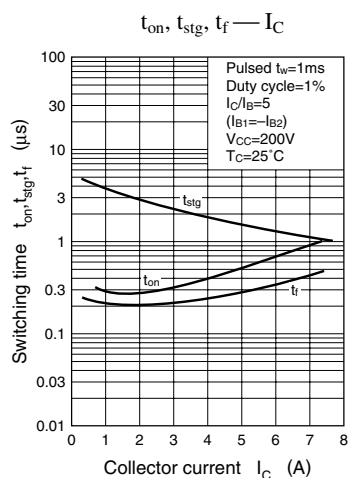
■ Electrical Characteristics $T_C = 25^\circ\text{C}$

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Collector cutoff current	2SC3799	I _{CBO}	V _{CB} = 800 V, I _E = 0			100	μA
	2SC3799A		V _{CB} = 900 V, I _E = 0			100	
Emitter cutoff current		I _{EBO}	V _{EB} = 5 V, I _C = 0			100	μA
Collector to emitter voltage *		V _{CEO(sus)}	I _C = 0.2 A, L = 25 mH	500			V
Forward current transfer ratio		h _{FE1}	V _{CE} = 5 V, I _C = 0.1 A	15			
		h _{FE2}	V _{CE} = 5 V, I _C = 5 A	8			
Collector to emitter saturation voltage		V _{CE(sat)}	I _C = 5 A, I _B = 1 A			1	V
Base to emitter saturation voltage		V _{BE(sat)}	I _C = 5 A, I _B = 1 A			1.5	V
Transition frequency		f _T	V _{CE} = 10 V, I _C = 0.5 A, f = 1 MHz		8		MHz
Turn-on time	2SC3799	t _{on}	I _C = 5 A, I _{B1} = 1 A, I _{B2} = −1 A, V _{CC} = 200 V			1	μs
	2SC3799A					1.2	
Storage time		t _{stg}				3	μs
Fall time	2SC3799	t _f				1	μs
	2SC3799A					1.2	

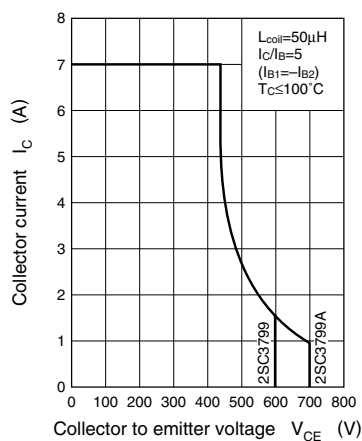
Note) *: $V_{CEO(sus)}$ Test circuit



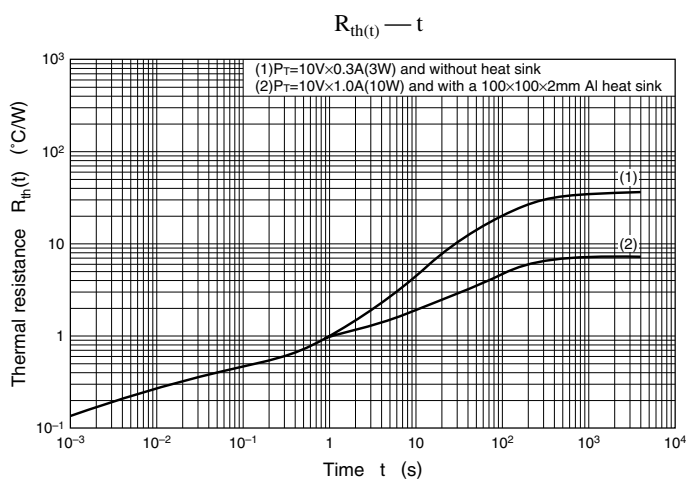
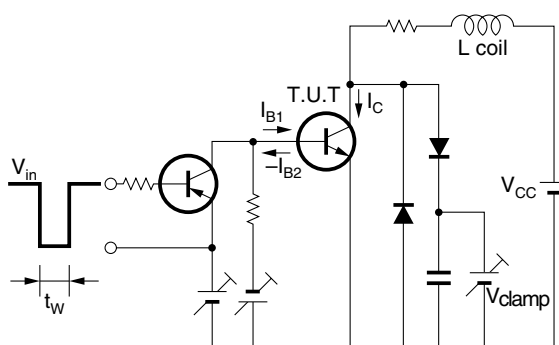
$P_C - T_a$  $I_C - V_{CE}$  $V_{CE(sat)} - I_C$  $V_{CE(sat)} - I_C$  $V_{BE(sat)} - I_C$  $V_{BE(sat)} - I_C$  $h_{FE} - I_C$  $f_T - I_C$  $C_{ob} - V_{CB}$ 



Area of safe operation, reverse bias ASO



Reverse bias ASO measuring circuit



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