FAIRCHILD SEMICONDUCTOR™

June 1999

# Si9955DY*

## Dual N-Channel Enhancement Mode MOSFET

### General Description

These N-Channel Enhancement Mode MOSFETs are produced using Fairchild Semiconductor's advance process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

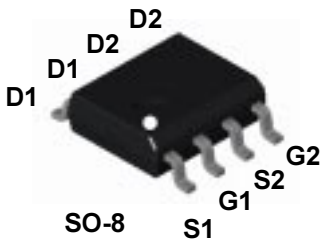
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

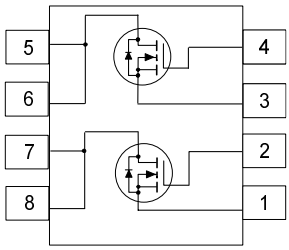
### Features

- 3.0 A, 50 V. $R_{DS(ON)}$ = 0.130 Ω @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ = 0.200 Ω @ $V_{GS}$ = 4.5 V
- Low gate charge.
- Fast switching speed.
- High power and current handling capability.

### Applications

- Battery switch
- Load switch
- Motor controls




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 50 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | 3.0 | A |
| | - Pulsed | | 10 | |
| $P_D$ | Power Dissipation for Single Operation | | 2.0 | W |
| | Power Dissipation for Single Operation | (Note 1a) | 1.6 | |
| | | (Note 1b) | 1 | |
| | | (Note 1c) | 0.9 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | | 62.5 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 40 | °C/W |

## Package Outlines and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|
| 9955 | SI9955DY | 13" | 12mm | 2500 units |

* Die and manufacturing source subject to change without prior notification.

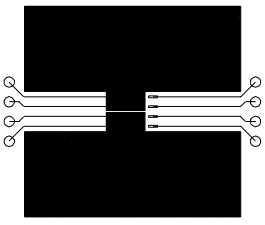
## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

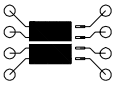
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 50 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | 60 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V<br>$V_{DS}$ = 40 V, $V_{GS}$ = 0 V, $T_J$ = 55°C | | | 2<br>25 | µA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | | | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | -4.5 | | mV/°C |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 3 A<br>$V_{GS}$ = 10 V, $I_D$ = 3 A, $T_J$=125°C<br>$V_{GS}$ = 4.5 V, $I_D$ = 1.5 A | | 0.076<br>0.124<br>0.103 | 0.130<br>0.200<br>0.200 | Ω |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | 10 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 15 V, $I_D$ = 3 A | | 5.3 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 345 | | pF |
| $C_{oss}$ | Output Capacitance | | | 110 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 25 | | pF |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 25 V, $I_D$ = 1 A, $R_L$ = 25 Ω<br>$V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 5 | 20 | ns |
| $t_r$ | Turn-On Rise Time | | | 7.5 | 20 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 20 | 70 | ns |
| $t_f$ | Turn-Off Fall Time | | | 7 | 50 | ns |
| $t_{rr}$ | Drain-Source Reverse Recovery Time | $I_F$ = 1.5 A, di/dt = 100A/µs | | 40 | 100 | nS |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 25 V, $I_D$ = 2 A,<br>$V_{GS}$ = 10 V | | 13 | 30 | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 1.7 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 3.2 | | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | 2.0 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.5 A (Note 2) | | 0.8 | 1.2 | V |

**Notes:**

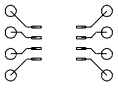
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 78° C/W when mounted on a 0.5 in² pad of 2 oz. copper.



b) 125° C/W when mounted on a 0.02 in² pad of 2 oz. copper.



c) 135° C/W when mounted on a 0.003 in² pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

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## PRODUCT STATUS DEFINITIONS

### Definition of Terms

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|---|---|---|
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