National Semiconductor

May 1998

LPC661
Low Power CMOS Operational Amplifier

General Description

The LPC661 CMOS operational amplifier is ideal for operation from a single supply. It features a wide range of operating supply voltage from +5V to +15V, rail-to-rail output swing and an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the supply current requirement is typically 55 µA.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC660 datasheet for a Quad CMOS operational amplifier or the LPC662 data sheet for a Dual CMOS operational amplifier with these same features.

Features

(Typical unless otherwise noted)

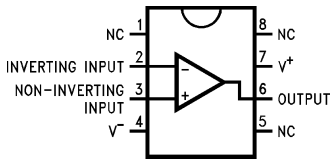
- Rail-to-rail output swing
- Low supply current 55 µA
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 µV/˚C
- Ultra low input bias current 2 fA
- Input common-mode range includes GND
- Operating range from +5V to +15V
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/µs

Applications

- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Connection Diagram

8-Pin DIP/SO



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Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55˚C to +125˚C	Industrial −40˚C to +85˚C		
8-Pin Small Outline		LPC661AIM LPC661IM	M08A	Tape and Reel Rail
8-Pin Molded DIP	LPC661AMN	LPC661AIN LPC661IN	N08E	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	16V
Differential Input Voltage	±Supply Voltage
Output Short Circuit to V^+	(Notes 2, 9)
Output Short Circuit to V^-	(Note 2)
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature	
(Soldering, 10 sec.)	260˚C
Junction Temperature (Note 3)	150˚C
Power Dissipation	(Note 3)
ESD Rating	
(C=100 pF, R=1.5 kΩ)	1000V
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Voltage Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Current at Power Supply Pin	35 mA

Operating Ratings (Note 1)

Supply Voltage	$4.75V \le V^+ \le 15.5V$
Junction Temperature Range	
LPC661AM	$-55˚C \le T_J \le +125˚C$
LPC661AI	$-40˚C \le T_J \le +85˚C$
LPC661I	$-40˚C \le T_J \le +85˚C$
Power Dissipation	(Note 7)
Thermal Resistance (θ_{JA}) (Note 8)	
8-Pin DIP	101˚C/W
8-Pin SO	165˚C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25˚C$.

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
V_{OS}	Input Offset Voltage		1	3 **3.5**	3 **3.3**	6 **6.3**	mV
TCV_{OS}	Input Offset Voltage Average Drift		1.3				µV/˚C
I_B	Input Bias Current		0.002	20 **100**	 **4**	 **4**	pA max
I_{OS}	Input Offset Current		0.001	20 **100**	 **2**	 **2**	pA max
R_{IN}	Input Resistance		>1				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70 **68**	70 **68**	63 **61**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	70 **68**	70 **68**	63 **61**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84 **82**	84 **83**	74 **73**	dB min
V_{CM}	Input Common Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V min
A_V	Large Signal Voltage Gain	Sourcing $R_L = 100$ kΩ (Note 5)	1000	400 **250**	400 **300**	300 **200**	V/mV min
		Sinking $R_L = 100$ kΩ (Note 5)	500	180 **70**	180 **120**	90 **70**	V/mV min
		Sourcing $R_L = 5$ kΩ (Note 5)	1000	200 **150**	200 **160**	100 **80**	V/mV min
		Sinking $R_L = 5$ kΩ (Note 5)	250	100 **35**	100 **60**	50 **40**	V/mV min

DC Electrical Characteristics (Continued)

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25˚C.

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
V_O	Output Swing	V^+ = 5V R_L = 100 kΩ to 2.5V	4.987	4.970 **4.950**	4.970 **4.950**	4.940 **4.910**	V min
			0.004	0.030 **0.050**	0.030 **0.050**	0.060 **0.090**	V max
		V^+ = 5V R_L = 5 kΩ to 2.5V	4.940	4.850 **4.750**	4.850 **4.750**	4.750 **4.650**	V min
			0.040	0.150 **0.250**	0.150 **0.250**	0.250 **0.350**	V max
		V^+ = 15V R_L = 100 kΩ to 7.5V	14.970	14.920 **14.880**	14.920 **14.880**	14.880 **14.820**	V min
			0.007	0.030 **0.050**	0.030 **0.050**	0.060 **0.090**	V max
		V^+ = 15V R_L = 5 kΩ to 7.5V	14.840	14.680 **14.600**	14.680 **14.600**	14.580 **14.480**	V min
			0.110	0.220 **0.300**	0.220 **0.300**	0.320 **0.400**	V max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **12**	16 **14**	13 **11**	mA min
		Sinking, V_O = 5V	21	16 **12**	16 **14**	13 **11**	mA min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	40	19 **19**	28 **25**	23 **20**	mA min
		Sinking, V_O = 13V (Note 9)	39	19 **19**	28 **24**	23 **19**	mA min
I_S	Supply Current	V^+ = 5V, V_O = 1.5V	55	60 **70**	60 **70**	70 **85**	µA max
		V^+ = 15V, V_O = 1.5V	58	75 **85**	75 **85**	90 **105**	µA max

AC Electrical Characteristics

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25˚C.

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
SR	Slew Rate	(Note 6)	0.11	0.07 **0.04**	0.07 **0.05**	0.05 **0.03**	V/µs min
GBW	Gain-Bandwidth Product		350				kHz
ϕm	Phase Margin		50				Deg
G_M	Gain Margin		17				dB
e_n	Input Referred Voltage Noise	F = 1 kHz	42				nV/$\sqrt{\text{Hz}}$
i_n	Input Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{\text{Hz}}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, A_V = −10 R_L = 100 kΩ, V_O = 8 V_{PP} V^+ = 15V	0.01				%

AC Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}-T_A)/\theta_{JA}$.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: V+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 6: V+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

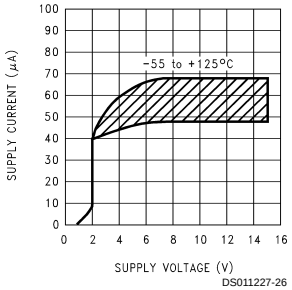
Note 7: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J-T_A)/\theta_{JA}$.

Note 8: All numbers apply for packages soldered directly into a PC board.

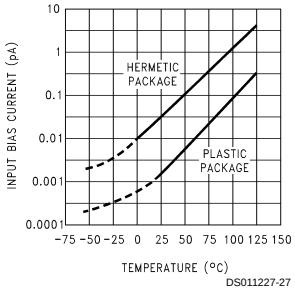
Note 9: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics V_S = ±7.5V, T_A = 25˚C unless otherwise specified

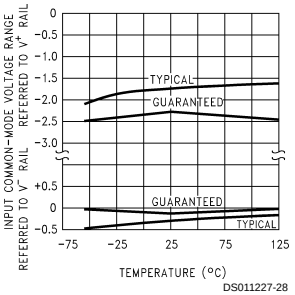
Supply Current vs Supply Voltage



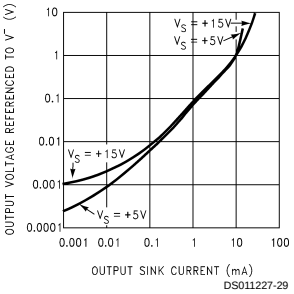
Input Bias Current vs Temperature



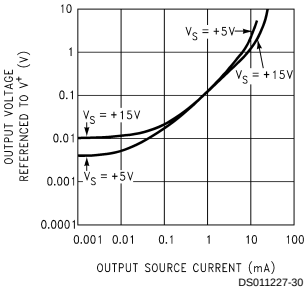
Common-Mode Voltage Range vs Temperature



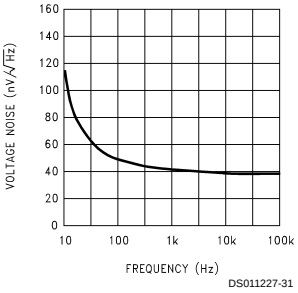
Output Characteristics Current Sinking



Output Characteristics Current Sourcing

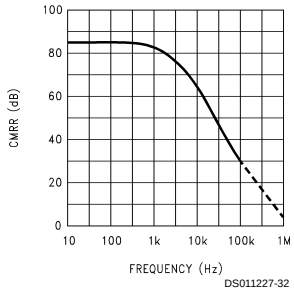


Input Voltage Noise vs Frequency

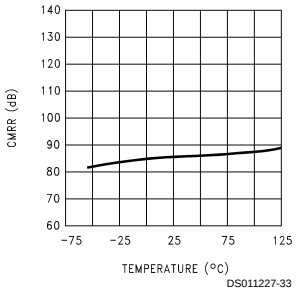


Typical Performance Characteristics V_S = ±7.5V, T_A = 25˚C unless otherwise specified (Continued)

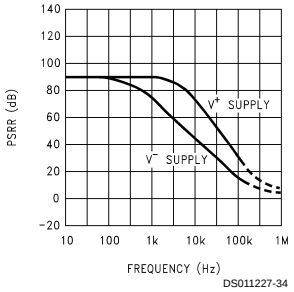
CMRR vs Frequency



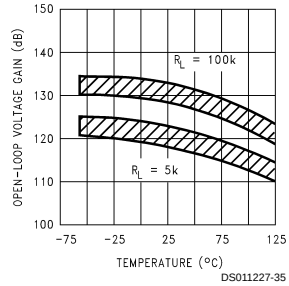
CMRR vs Temperature



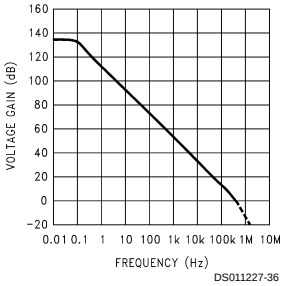
Power Supply Rejection Ratio vs Frequency



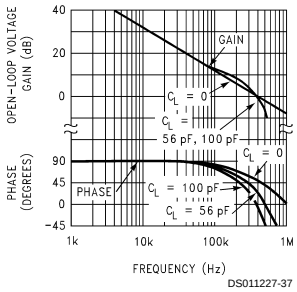
Open-Loop Voltage Gain vs Temperature



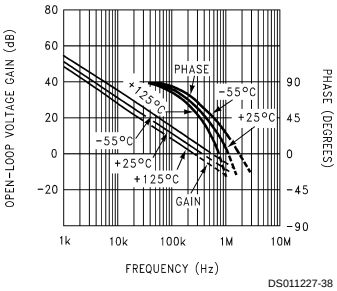
Open-Loop Frequency Response



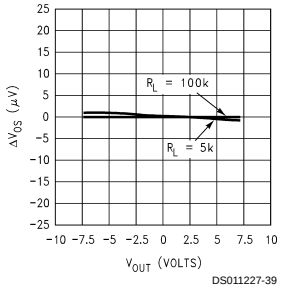
Gain and Phase Responses vs Load Capacitance



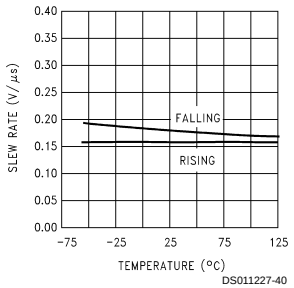
Gain and Phase Responses vs Temperature



Gain Error (V_{OS} vs V_{OUT})

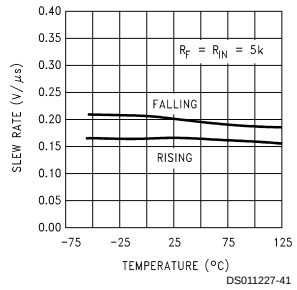


Non-Inverting Slew Rate vs Temperature



Typical Performance Characteristics V_S = ±7.5V, T_A = 25˚C unless otherwise specified (Continued)

Inverting Slew Rate vs Temperature



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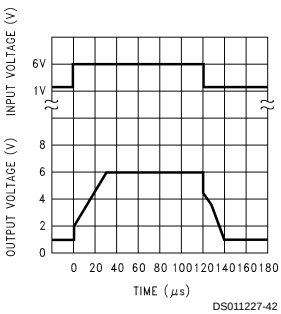
Large-Signal Pulse Non-Inverting Response (A_V = +1)



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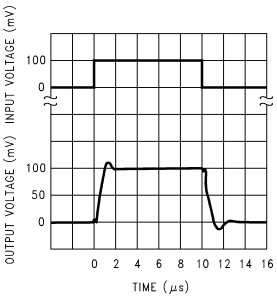
Non-Inverting Small Signal Pulse Response (A_V = +1)



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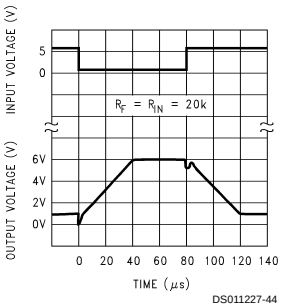
Inverting Large-Signal Pulse Response



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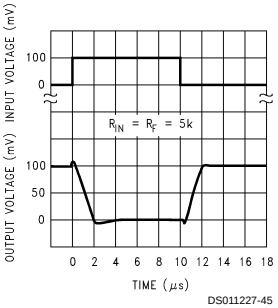
Inverting Small-Signal Pulse Response



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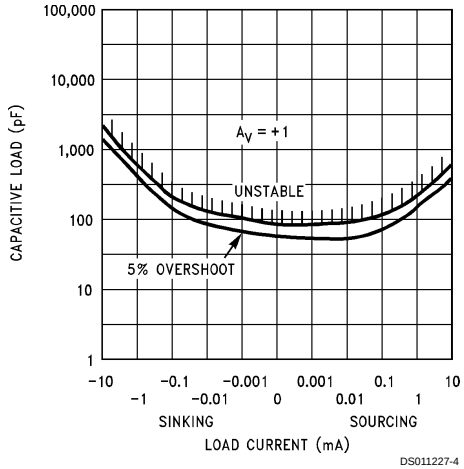
Stability vs Capacitive Load



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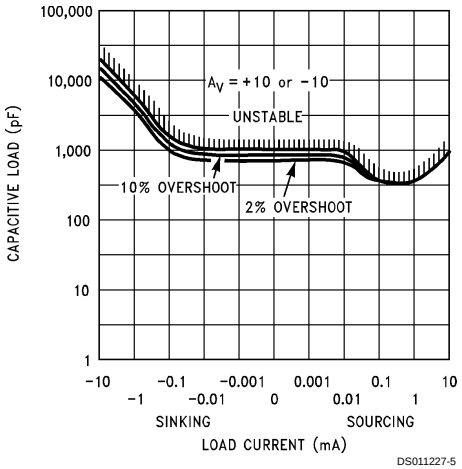
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Stability vs Capacitive Load



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Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LPC661 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

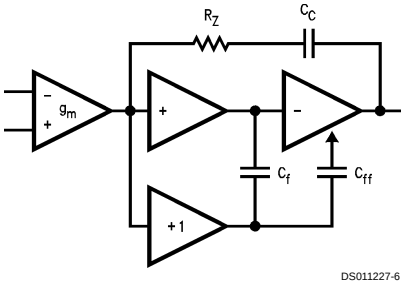


FIGURE 1. LPC661 Circuit Topology

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC661 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

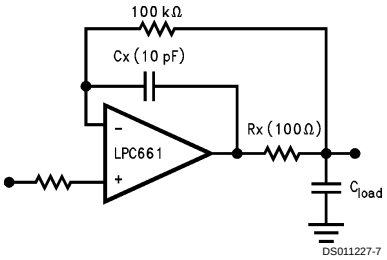


FIGURE 2. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 3*). Typically a pull up resistor conducting 50 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

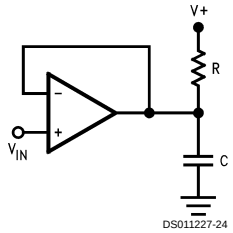


FIGURE 3. Compensating for Large Capacitive Loads with A Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC661, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC661's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 4.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor

Application Hints (Continued)

(2:1) degradation of the amplifier's performance. See *Figures 5, 6, 7* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 8*.

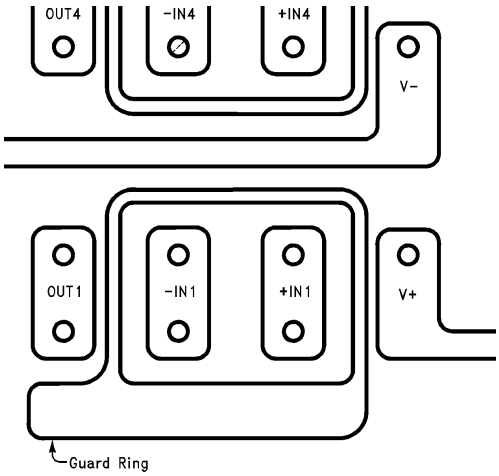


FIGURE 4. Example of Guard Ring in P.C. Board Layout, Using the LPC660

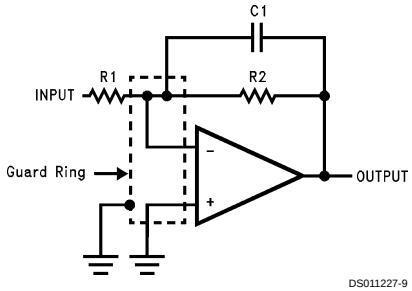


FIGURE 5. Inverting Amplifier Guard Ring Connections

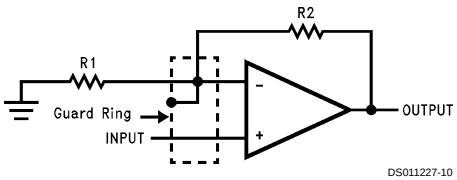


FIGURE 6. Non-Inverting Amplifier Guard Ring Connections

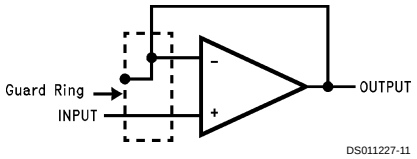


FIGURE 7. Follower Guard Ring Connections

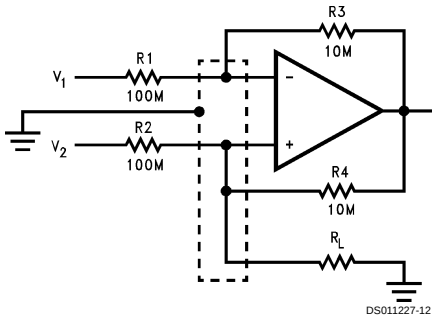
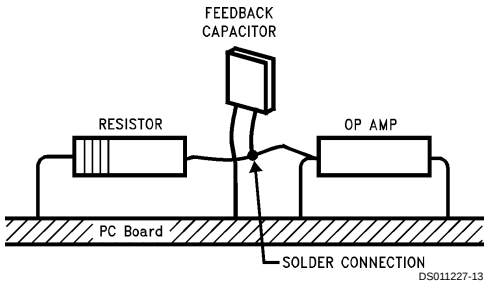


FIGURE 8. Howland Current Pump Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board con-

Application Hints (Continued)

struction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 9*.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 9. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 10* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$

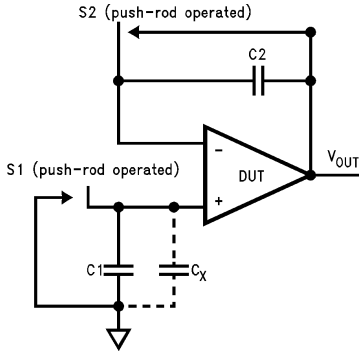


FIGURE 10. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

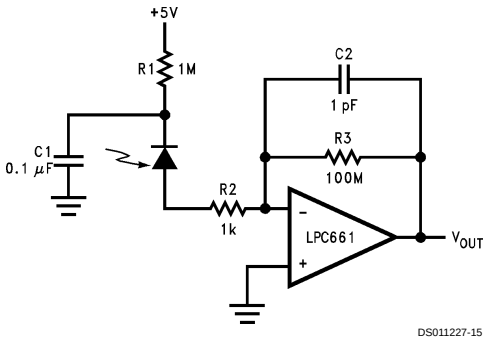
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

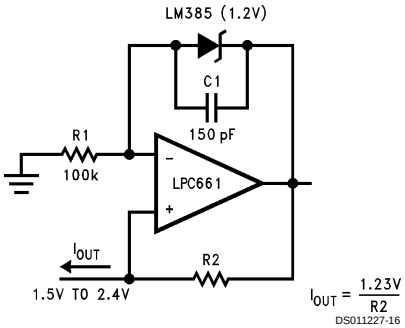
Typical Single-Supply Applications ($V+ = 5.0\ V_{DC}$)

Photodiode Current-toVoltage Converter



Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

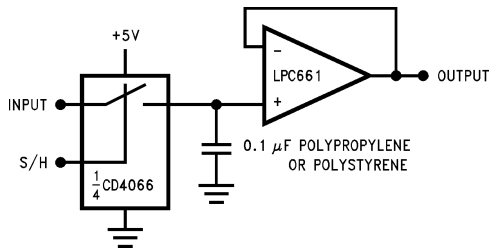
Micropower Current Source



(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

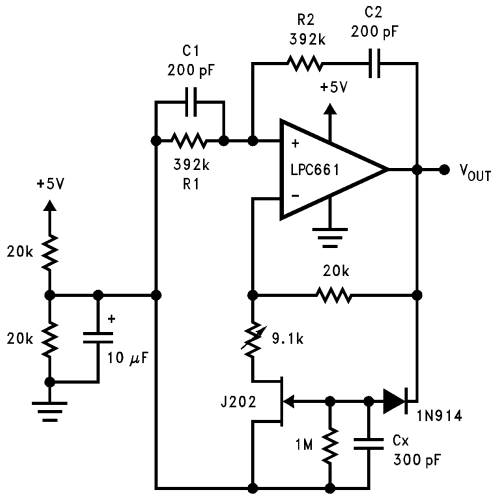
Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)

Low-Leakage Sample-and-Hold



DS011227-17

Sine-Wave Oscillator

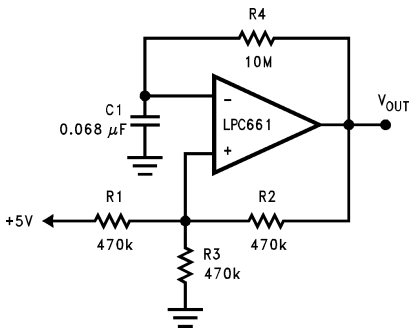


DS011227-18

Oscillator frequency is determined by R1, R2, C1, and C2:
$f_{OSC} = 1/2\pi RC$
where R = R1 = R2 and C = C1 = C2.

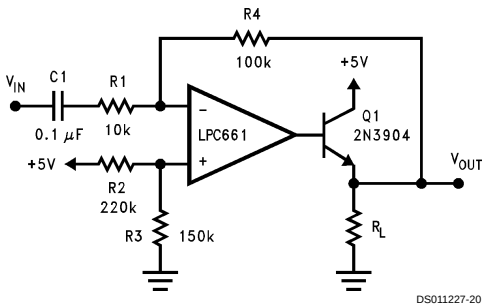
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator



DS011227-19

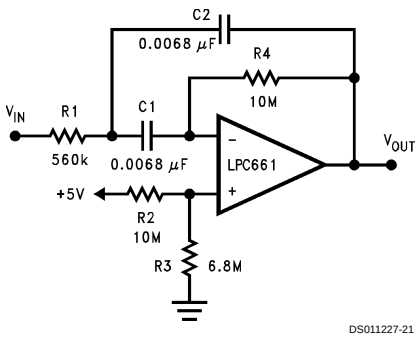
Power Amplifier



DS011227-20

Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)

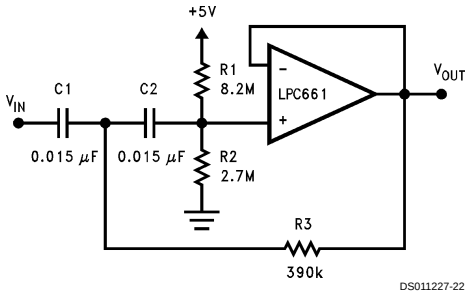
10 Hz Bandpass Filter



DS011227-21

f_O = 10 Hz
Q = 2.1
Gain = 18.9 dB

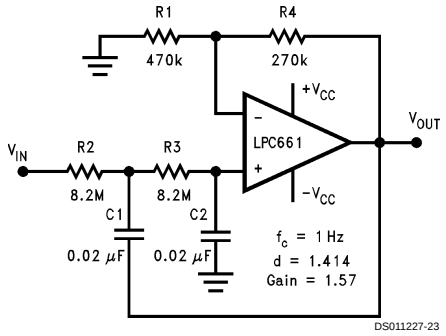
10 Hz High-Pass Filter (2 dB Dip)



DS011227-22

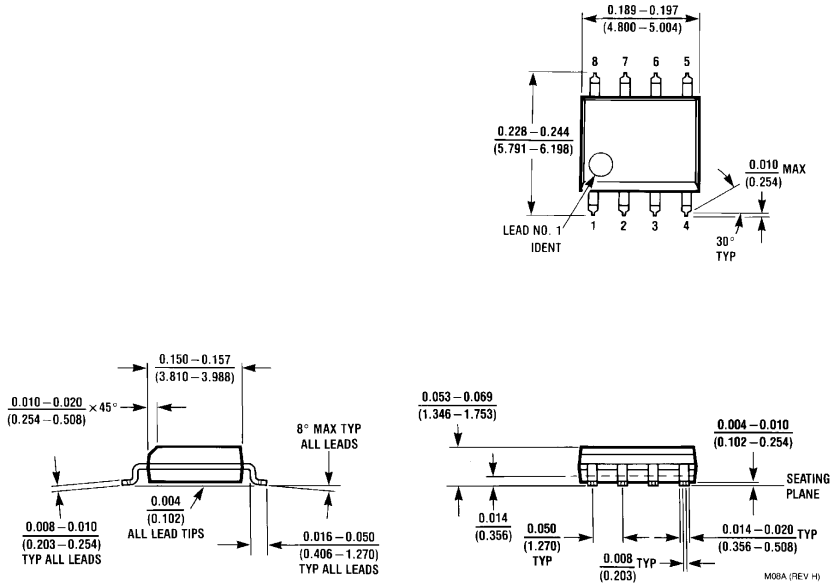
f_c = 10 Hz
d = 0.895
Gain = 1

1 Hz Low-Pass Filter
(Maximally Flat, Dual Supply Only)

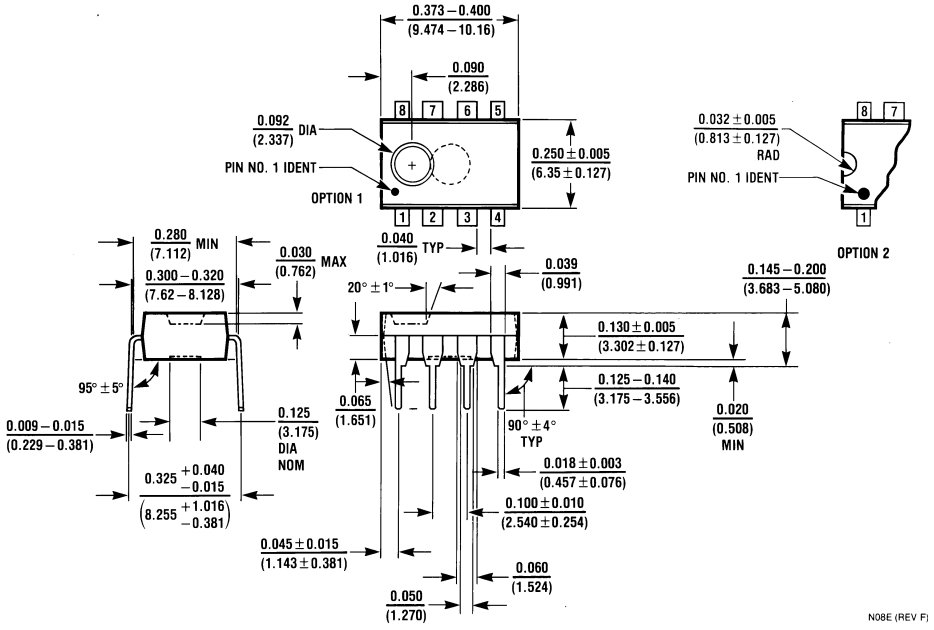


DS011227-23

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Small Outline Molded Package (M)
Order Number LPC661AIM or LPC661IM
NS Package Number M08A



8-Pin Molded Dual-In-Line Package (N)
Order Number LPC661AIN, LPC661IN or LPC661AMN
NS Package Number N08E

Notes

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