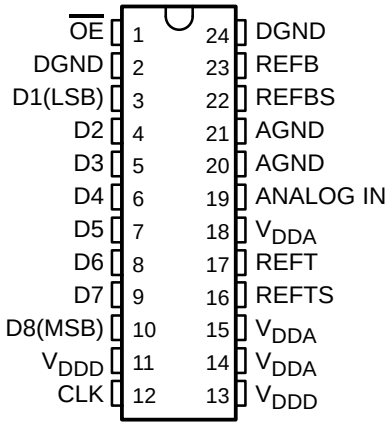
features

- **8-Bit Resolution**
- **Linearity Error**
  - **±0.75 LSB Max (25°C)**
  - **±1 LSB Max (–20°C to 75°C)**
- **Differential Linearity Error**
  - **±0.5 LSB (25°C)**
  - **±0.75 LSB Max (–20°C to 75°C)**
- **Maximum Conversion Rate**
  - **20 Mega-Samples per Second (MSPS) Min**
- **5-V Single-Supply Operation**
- **Low Power Consumption . . . 90 mW Typ**
- **Interchangeable With Sony CXD1175**

applications

- **Digital TV**
- **Medical Imaging**
- **Video Conferencing**
- **High-Speed Data Conversion**
- **QAM Demodulators**

NS PACKAGE†
(TOP VIEW)



† Available in tape and reel only and ordered as the TLC5510INSLE.

AVAILABLE OPTIONS

T_A	NS PACKAGE (TAPE AND REEL ONLY)
–20°C to 75°C	TLC5510INSLE

description

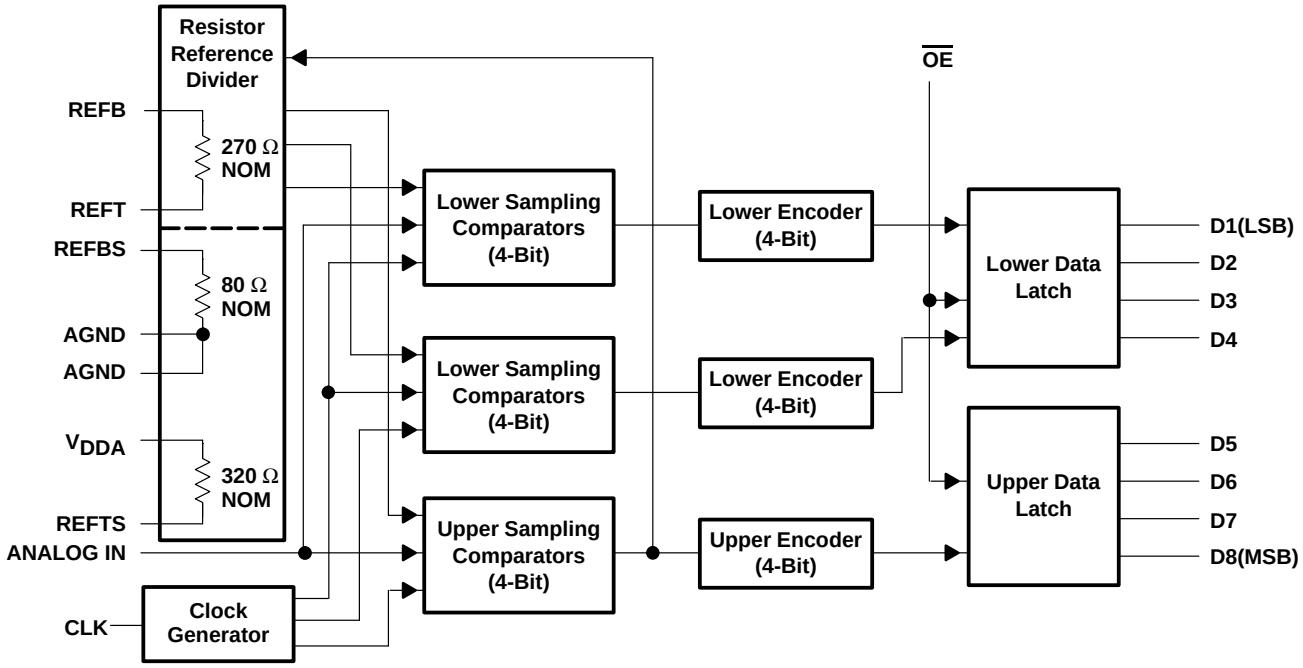
The TLC5510 is a CMOS, 8-bit, 20 MSPS analog-to-digital converter (ADC) that utilizes a semiflash architecture. The TLC5510 operates with a single 5 V supply and consumes only 100 mW of power typically. Also included is an internal sample and hold circuit, parallel outputs with high impedance mode, and internal reference resistors.

The semiflash architecture reduces power consumption and die size compared to flash converters. By implementing the conversion in a 2-step process, the number of comparators is significantly reduced. The latency of the data upon conversion is 2.5 clocks.

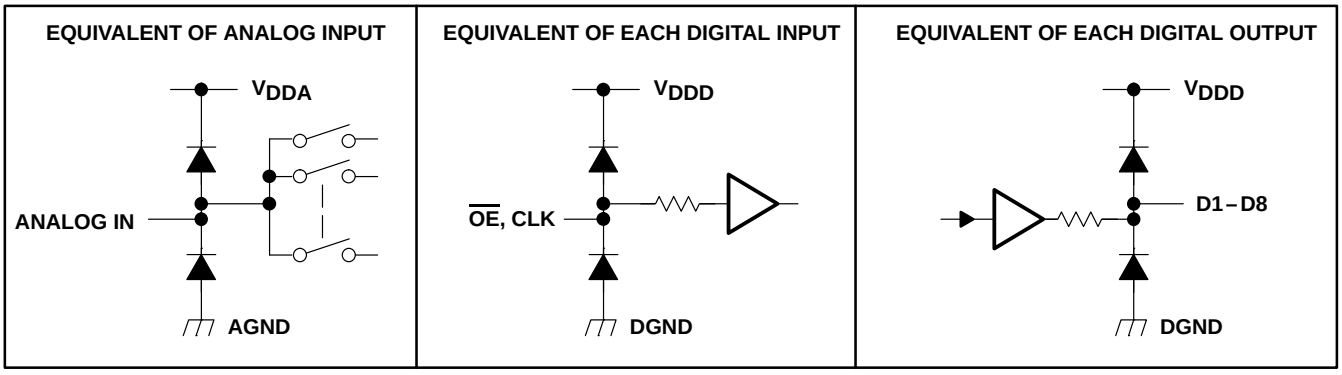
The internal reference resistors can create a standard, 2-V, full-scale conversion range using V_{DDA}. Only external jumpers are required to implement this option. This reduces the need for external references or resistors. Differential linearity is 0.5 LSB at 25°C and a maximum of 0.75 LSB over the full operating temperature range. Dynamic characteristics are specified with a differential gain of 1% and differential phase of 0.7%.

The TLC5510 is characterized for operation from –20°C to 75°C.

functional block diagram



schematics of inputs and outputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock in
DGND	2, 24		Digital ground
D1–D8	3–10	O	Digital data out. D1:LSB, D8:MSB
$\overline{OE}$	1	I	Output enable. When $\overline{OE}$ = L, data is enabled. When $\overline{OE}$ = H, D1–D8 is in high impedance state.
V_{DDA}	14, 15, 18		Analog V_{DD}
V_{DDD}	11, 13		Digital V_{DD}
REFB	23	I	Reference voltage in (bottom)
REFBS	22		Reference voltage (bottom). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFB terminal (see Figure 2).
REFT	17	I	Reference voltage in (top)
REFTS	16		Reference voltage (top). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFT terminal (see Figure 2).

absolute maximum ratings†

Supply voltage, V_{DDA}, V_{DDD} . . . . . 7 V
Reference voltage input range, $V_{ref(T)}$, $V_{ref(B)}$, $V_{ref(BS)}$, $V_{ref(TS)}$ . . . . . AGND to V_{DDA}
Analog input voltage range, $V_{I(ANLG)}$ . . . . . AGND to V_{DDA}
Digital input voltage range, $V_{I(DGTL)}$ . . . . . DGND to V_{DDD}
Digital output voltage range, $V_{O(DGTL)}$ . . . . . DGND to V_{DDD}
Operating free-air temperature range, T_A . . . . . –20°C to 75°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{DDA}–AGND	4.75	5	5.25	V
	V_{DDD}–AGND	4.75	5	5.25	
	AGND–DGND	–100	0	100	mV
Reference input voltage (top), $V_{ref(T)}$		$V_{ref(B)}$+2	$V_{ref(B)}$+2	2.7	V
Reference input voltage (bottom), $V_{ref(B)}$		0	0.6	$V_{ref(T)}$–2	V
Analog input voltage range, $V_{I(ANLG)}$ (see Note 1)		$V_{ref(B)}$		$V_{ref(T)}$	V
High-level input voltage, V_{IH}		4			V
Low-level input voltage, V_{IL}				1	V
Pulse duration, clock high, $t_{w(H)}$		25			ns
Pulse duration, clock low, $t_{w(L)}$		25			ns

NOTE 1: REFT – REFB ≥ 2.4 V maximum

electrical characteristics at V_{DD} = 5 V, $V_{ref(T)}$ = 2.5 V, $V_{ref(B)}$ = 0.5 V, f_{conv} = 20 MSPS, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
E_L	Linearity error	f_{conv} = 20 MSPS, V_I = 0.5 V to 2.5 V	T_A = 25°C			±0.4	±0.75	LSB
			T_A = –20°C to 75°C				±1	
E_D	Linearity error, differential		T_A = 25°C			±0.3	±0.5	
			T_A = –20°C to 75°C				±0.75	
	Self bias (1)	Short REFB to REFBS,	Short REFT to REFTS		0.57	0.61	0.65	V
	Self bias (2)				1.9	2.02	2.15	
	Self bias (3)	Short REFB to AGND,	Short REFT to REFTS		2.18	2.29	2.4	
I_{ref}	Reference voltage current	$V_{ref(T)} - V_{ref(B)}$ = 2 V			5.2	7.5	10.5	mA
R_{ref}	Reference voltage resistor	Between REFT and REFB terminals			190	270	350	Ω
C_i	Analog input capacitance	$V_{I(ANLG)}$ = 1.5 V + 0.07 V_{rms}				16		pF
E_{ZS}	Zero-scale error	V_{ref} = REFT – REFB = 2 V			–18	–43	–68	mV
E_{FS}	Full-scale error				–20	0	20	
I_{IH}	High-level input current	V_{DD} = MAX,	V_{IH} = V_{DD}				5	µA
I_{IL}	Low-level input current	V_{DD} = MAX,	V_{IL} = 0 V				5	
I_{OH}	High-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN,	V_{OH} = V_{DD} – 0.5 V	–1.5			mA
I_{OL}	Low-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN,	V_{OL} = 0.4 V	2.5			
I_{OZH}	High-level high-impedance-state output leakage current	$\overline{OE}$ = V_{DD},	V_{DD} = MAX	V_{OH} = V_{DD}			16	µA
I_{OZL}	Low-level high-impedance-state output leakage current	$\overline{OE}$ = V_{DD},	V_{DD} = MIN	V_{OL} = 0 V			16	
I_{DD}	Supply current	f_S = 20 MSPS,	National Television System Committee (NTSC) ramp wave input			18	27	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

operating characteristics at V_{DD} = 5 V, V_{RT} = 2.5 V, V_{RB} = 0.5 V, f_s = 20 MSPS, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{conv}	Maximum conversion rate	$V_{I(ANLG)}$ = 0.5 V – 2.5 V, f_I = 1-kHz ramp wave form	20			MSPS
BW	Analog input bandwidth	At – 1 dB		14		MHz
t_{dd}	Digital output delay time	$C_L \le 10$ pF (see Note 2)		18	30	ns
	Differential gain	NTSC 40 Institute of Radio Engineers (IRE) modulation wave, f_{conv} = 14.3 MSPS		1%		
	Differential phase			0.7		degrees
t_{AJ}	Aperture jitter time			30		ps
$t_{d(s)}$	Sampling delay time			4		ns

NOTE 2: C_L includes probe and jig capacitance

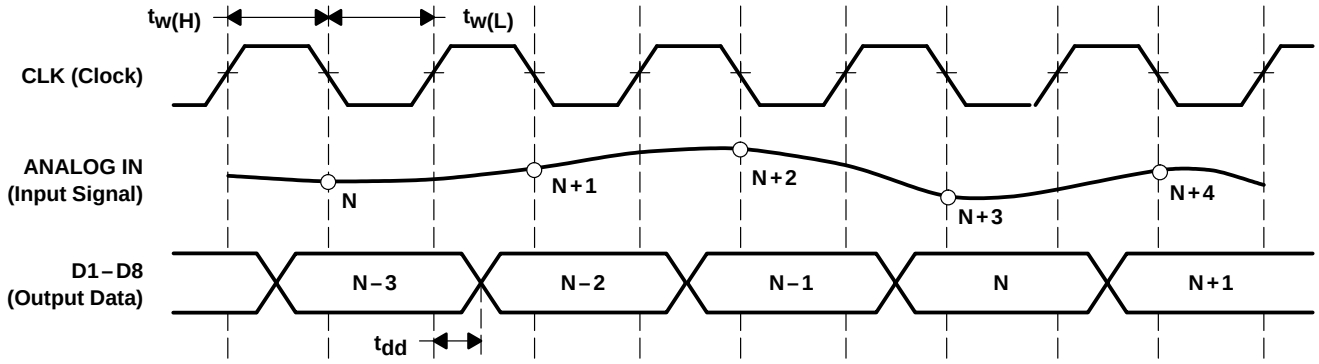


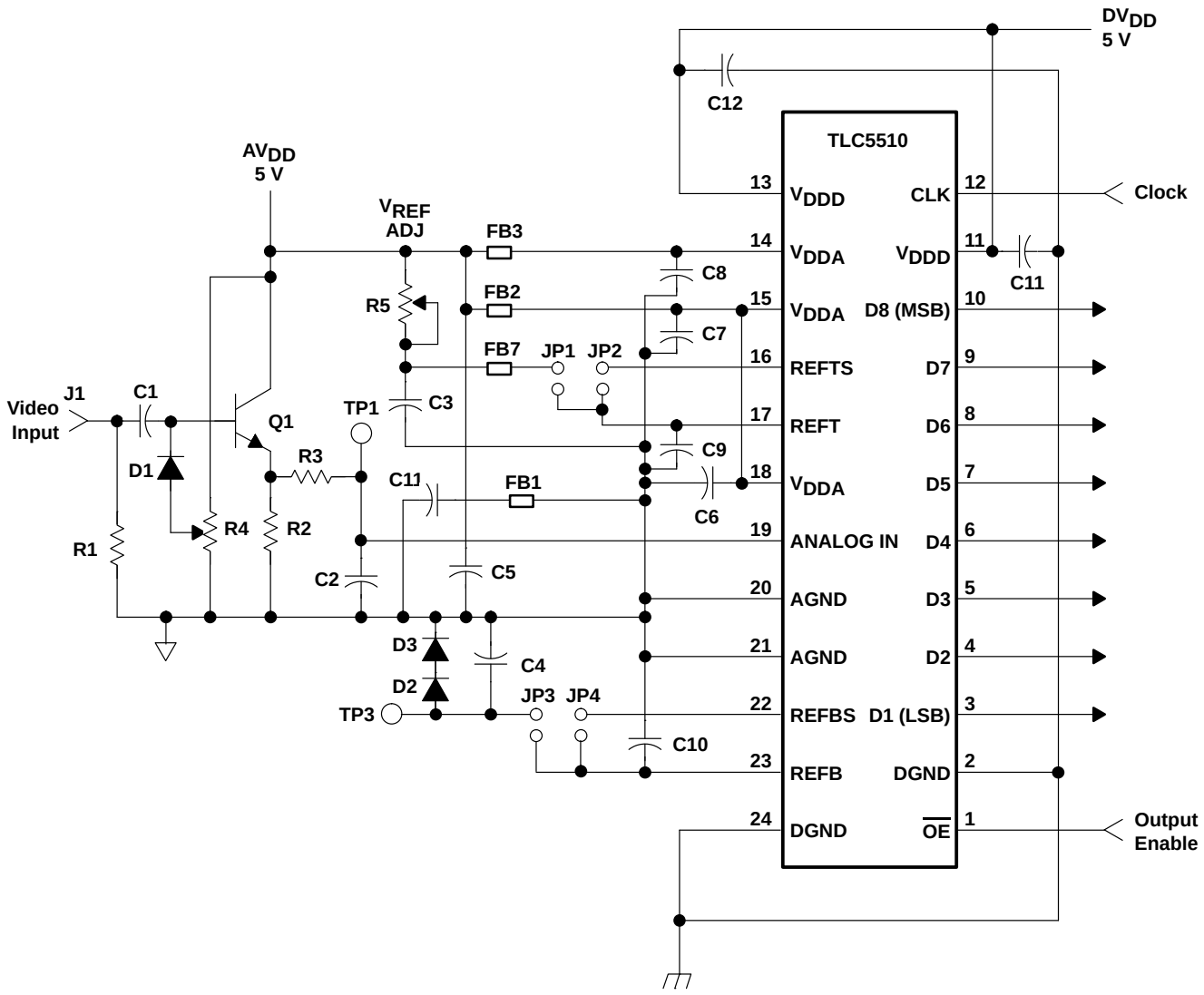
Figure 1. I/O Timing Diagram

APPLICATION INFORMATION

The following notes are design recommendations that should be used with the TLC5510.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
- Since AGND and DGND are not connected internally, these terminals need to be connected externally. With breadboards, these ground lines should be connected through separate leads with correct supply bypassing. A good method to use is separate twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts.
- V_{DDA} to AGND and V_{DDD} to DGND should be decoupled with 1-μF and 0.01-μF capacitors, respectively, and placed as close as possible to the affected device terminals. A ceramic-chip capacitor is recommended for the 0.01-μF capacitor. Care should be exercised to ensure a solid noise-free ground connection for the analog and digital grounds.
- V_{DDA}, AGND, and ANALOG IN terminals should be shielded from the higher frequency terminals, CLK and D0–D7. When possible, AGND traces should be placed on both sides of the ANALOG IN traces on the PCB for shielding.
- In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

APPLICATION INFORMATION



LOCATION	DESCRIPTION
C1, C3–C4, C6–C12	0.1-μF Capacitor
C2	10-pF Capacitor
C5	47-μF Capacitor
FB1, FB2, FB3, FB7	Ferrite Bead
Q1	2N3414 or equivalent
R1, R3	75-Ω resistor
R2	500-Ω resistor
R4	10-kΩ resistor, clamp voltage adjust
R5	300-Ω resistor, reference-voltage fine adjust

Figure 2. Application and Test Schematic

NOTE A: JP1, JP2, JP3, and JP4 allow adjustment of the reference voltage by R5 using temperature-compensating diodes D2, D3.

PRINCIPLES OF OPERATION

functional description

The TLC5510 is a semiflash ADC featuring two lower comparator blocks of four bits each.

As shown in Figure 3, input voltage $V_I(1)$ is sampled with the falling edge of CLK1 to the upper comparators block and the lower comparators block(A), S(1). The upper comparators block finalizes the upper data UD(1) with the rising edge of CLK2, and simultaneously, the lower reference voltage generates the voltage RV(1) corresponding to the upper data. The lower comparators block (A) finalizes the lower data LD(1) with the rising edge of CLK3. UD(1) and LD(1) are combined and output as OUT(1) with the rising edge of CLK4. According to the above internal operation described, output data is delayed 2.5 clocks from the analog input voltage sampling point.

Input voltage $V_I(2)$ is sampled with the falling edge of CLK2. UD(2) is finalized with the rising edge of CLK3, and LD(2) is finalized with the rising edge of CLK4 at the lower comparators block(B). OUT(2) is output with the rising edge of CLK5.

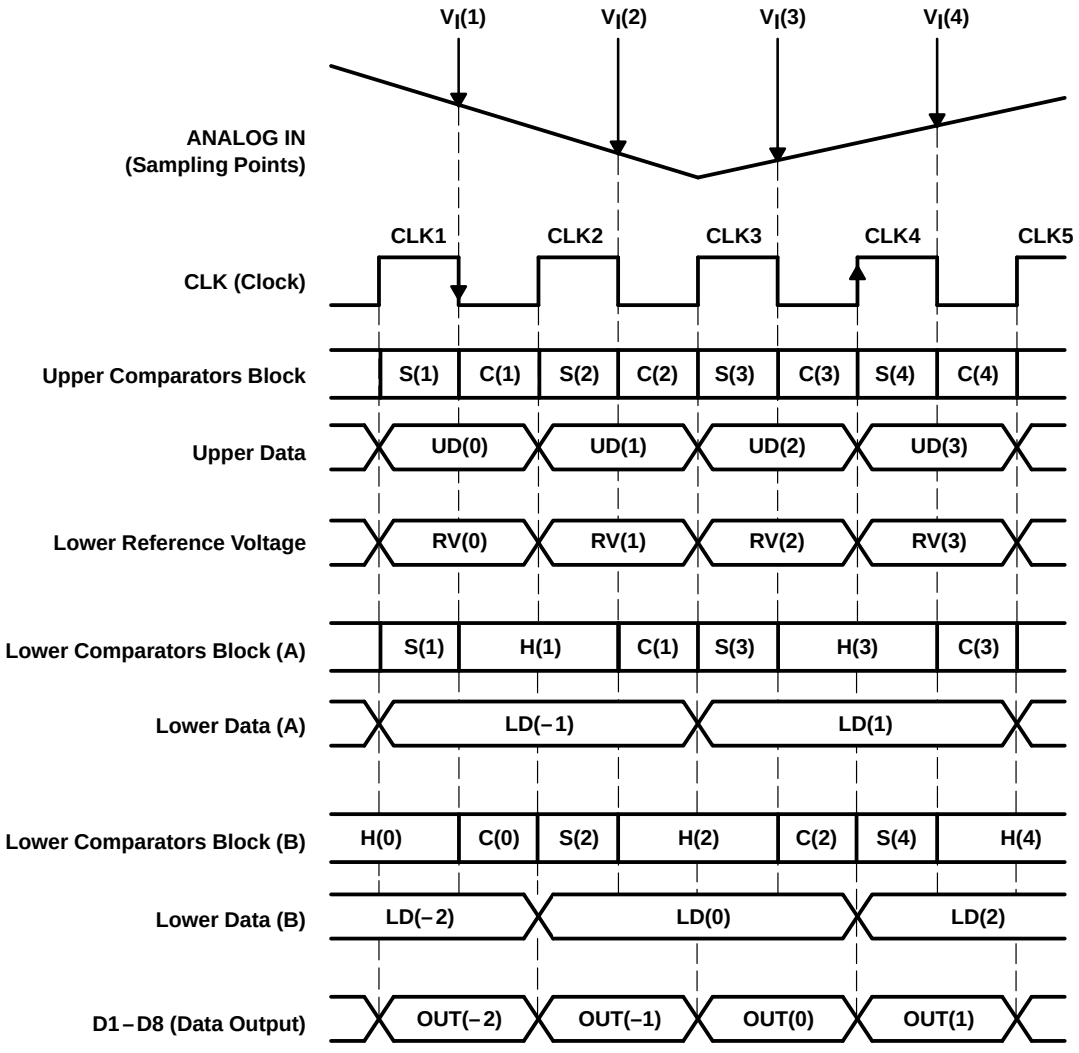


Figure 3. Internal Functional Timing Diagram

PRINCIPLES OF OPERATION

internal referencing

Three internal resistors are provided so that the device can generate an internal reference voltage. These resistors are brought out on terminals V_{DDA}, REFTS, REFT, REFB, REFBS, and AGND.

To use the internally generated reference voltage, terminal connections should be made as shown in Figure 4. This connection provides the standard video 2-V reference for the nominal digital output.

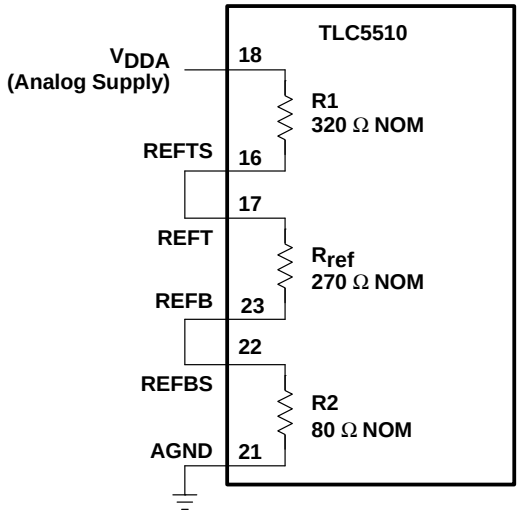


Figure 4. External Connections for Using the Internal-Reference Resistor Divider

functional operation

The TLC5510 functions as shown in Table 1.

Table 1. Functional Operation

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
$V_{ref(T)}$	0	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	127	1	0	0	0	0	0	0	0
•	128	0	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
$V_{ref(B)}$	255	0	0	0	0	0	0	0	0

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.