TS4872

RAIL TO RAIL INPUT/OUTPUT
1W AUDIO POWER AMPLIFIER WITH STANDBY MODE

- OPERATING FROM V_{CC} **= 2.2V to 5.5V**
- RAIL TO RAIL **INPUT/OUTPUT**
- **1W** OUTPUT POWER @ Vcc=5V, THD=1%, f=1kHz, with **8**Ω Load
- ULTRA LOW CONSUMPTION IN STANDBY MODE **(10nA)**
- **75dB** PSRR @ 217Hz @ 5 & 2.6V
- ULTRA LOW POP & CLICK
- ULTRA LOW DISTORTION **(0.05%)**
- UNITY GAIN STABLE
- **8 X170µm BUMPS FLIP CHIP PACKAGE**

DESCRIPTION

The TS4872 is an Audio Power Amplifier capable of delivering 1W of continuous RMS Ouput Power into 8Ω load @ 5V.

This Audio Amplifier is exhibiting 0.1% distortion level (THD) from a 5V supply for a Pout = 250mW RMS. An external standby mode control reduces the supply current to less than 10nA. An internal shutdown protection is provided.

The TS4872 has been designed for high quality audio applications such as mobile phones and to minimize the number of external components.

The unity-gain stable amplifier can be configured by external gain setting resistors.

APPLICATIONS

- Mobile Phones (Cellular / Cordless)
- PDAs
- Laptop/Notebook computers
- Portable Audio Devices

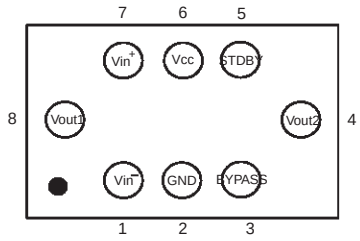
ORDER CODE

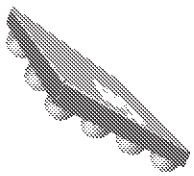
Part Number	Temperature Range	Package	Marking
		J	
TS4872IJT	-40, +85°C	•	YW4872

J = Flip Chip Package - only available in Tape & Reel (JT)

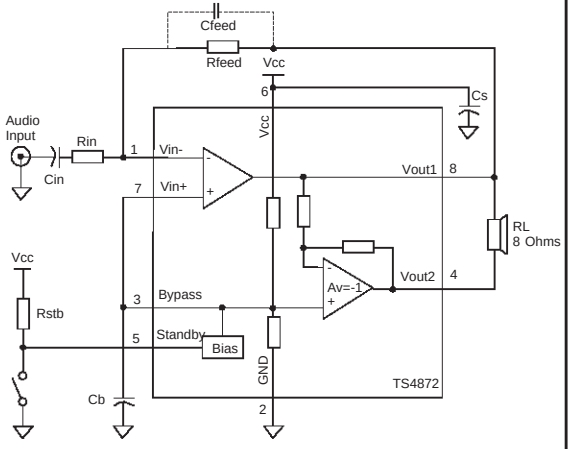
PIN CONNECTIONS (Top View)

TS4872IJT - FLIP CHIP





TYPICAL APPLICATION SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	6	V
V_i	Input Voltage [2]	G_{ND} to V_{CC}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Flip Chip Thermal Resistance Junction to Ambient [3]	165	°C/W
Pd	Power Dissipation	Internally Limited	
ESD	Human Body Model	2	kV
ESD	Machine Model	200	V
Latch-up	Latch-up Immunity	Class A	
	Lead Temperature (soldering, 10sec)	260	°C

1. All voltages values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V
3. Device is protected in case of over temperature by a thermal shutdown active @ 150°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.2 to 5.5	V
V_{ICM}	Common Mode Input Voltage Range V_{CC} from 2.6V to 5V V_{CC} < 2.6V	 G_{ND} to V_{CC} V_{CC} / 2	
V_{STB}	Standby Voltage Input : Device ON Device OFF	 $G_{ND} \leq V_{STB} \leq 0.5V$ V_{CC} - 0.5V ≤ $V_{STB} \leq V_{CC}$	V
RL	Load Resistor	4 - 32	Ω
R_{thja}	Flip Chip Thermal Resistance Junction to Ambient [1]	95	°C/W

1. With Heat Sink Surface = 125mm^2

ELECTRICAL CHARACTERISTICS

V_{CC} = **+5V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6	8	mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = Vcc, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω		1		W
THD + N	Total Harmonic Distortion + Noise Po = 250mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio [2] f = 217Hz, RL = 8Ω, RFeed = 22KΩ, Vripple = 200mV rms		75		dB
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to Vcc
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz

V_{CC} = **+3.3V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified) [3]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = Vcc, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω		450		mW
THD + N	Total Harmonic Distortion + Noise Po = 250mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio [2] f = 217Hz, RL = 8Ω, RFeed = 22KΩ, Vripple = 100mV rms		68		dB
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to Vcc
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz
3 All electrical values are made by correlation between 2.6v and 5v measurements

ELECTRICAL CHARACTERISTICS

V_{CC} = **2.6V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = Vcc, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω		260		mW
THD + N	Total Harmonic Distortion + Noise Po = 200mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio [2] f = 217Hz, RL = 8Ω, RFeed = 22KΩ, Vripple = 200mV rms		75		dB
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to Vcc
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz

V_{CC} = **2.2V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		4.5		mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = Vcc, RL = 8Ω		10		nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		2		mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω		180		mW
THD + N	Total Harmonic Distortion + Noise Po = 200mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio [2] f = 217Hz, RL = 8Ω, RFeed = 22KΩ, Vripple = 100mVpp		75		dB
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to Vcc
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz

Components	Functional Description
Rin	Inverting input resistor which sets the closed loop gain in conjunction with Rfeed. This resistor also forms a high pass filter with Cin (fc = 1 / (2 x Pi x Rin x Cin))
Cin	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal
Rfeed	Feed back resistor which sets the closed loop gain in conjunction with Rin
Cs	Supply Bypass capacitor which provides power supply filtering
Cb	Bypass pin capacitor which provides half supply filtering
Cfeed	Low pass filter capacitor allowing to cut the high frequency (low pass filter cut-off frequency 1 / (2 x Pi x Rfeed x Cfeed))
Rstb	Pull-up resistor which fixes the right supply level on the standby pin
Gv	Closed loop gain in BTL configuration = 2 x (Rfeed / Rin)

REMARKS

1. All measurements, except PSRR measurements, are made with a supply bypass capacitor Cs = 100µF.
2. External resistors are not needed for having better stability when supply @ Vcc down to 3V. By the way, the quiescent current remains the same.
3. The standby response time is about 1µs.

APPLICATION INFORMATION

Fig. 80 : Demoboard Schematic

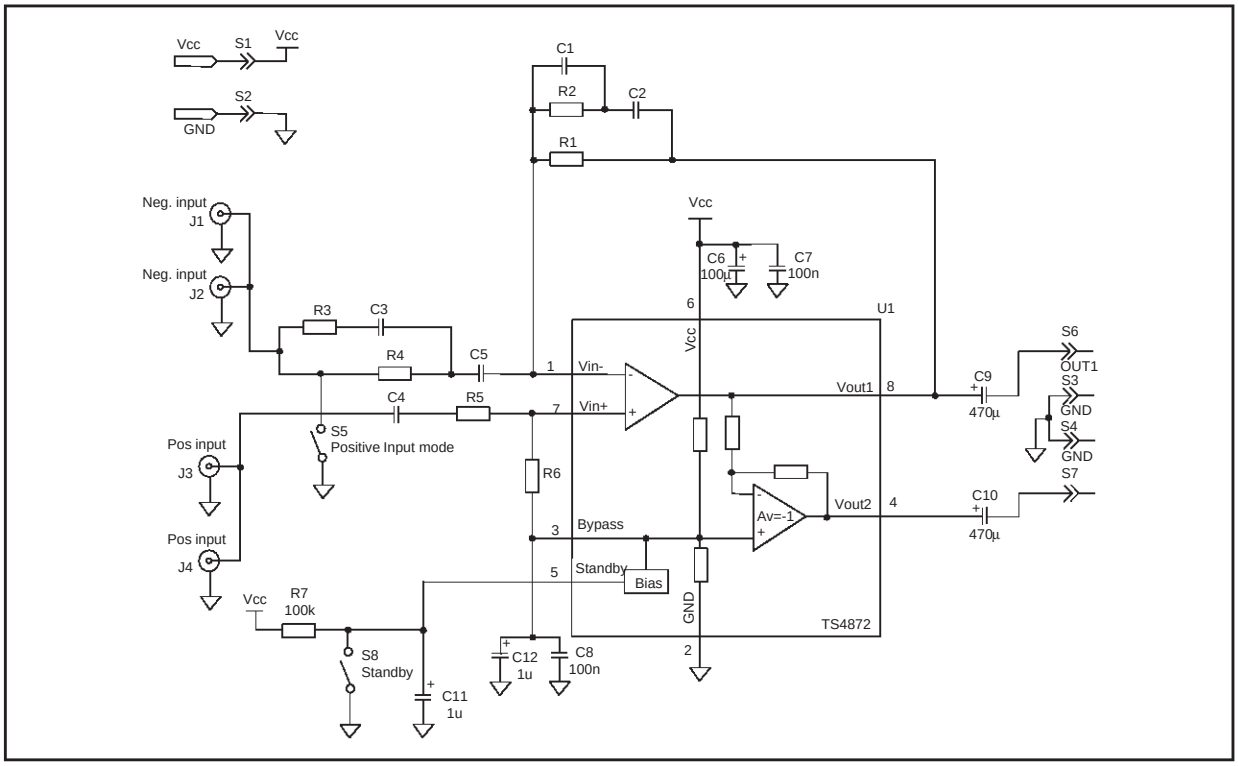


Fig. 81 : Flip Chip Demoboard Components Side

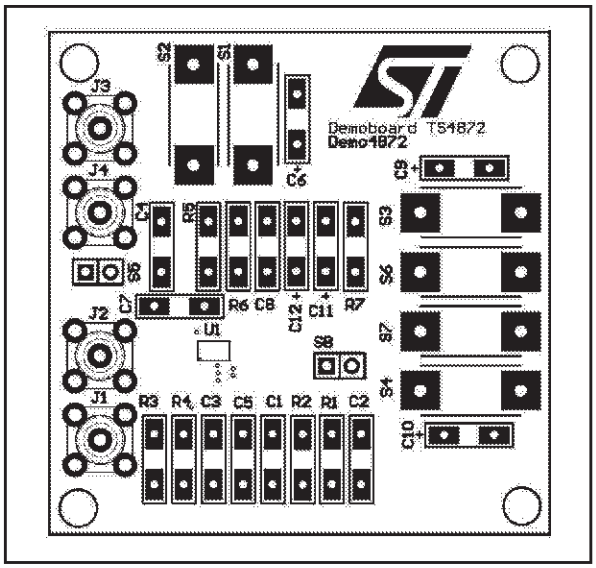


Fig. 82 : Flip Chip Demoboard Top Layer

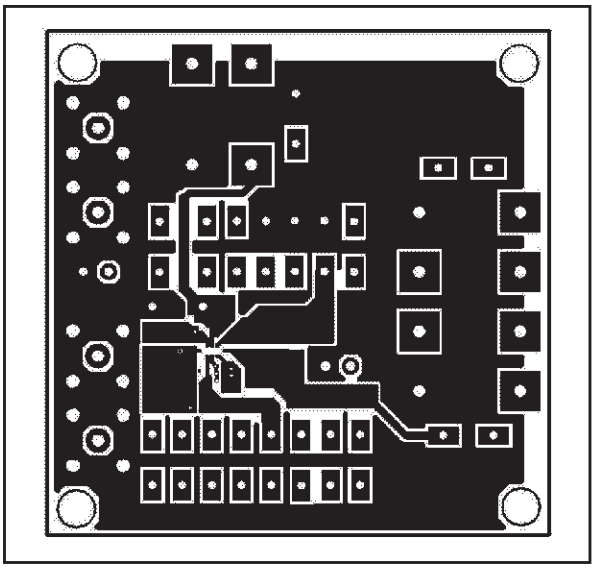
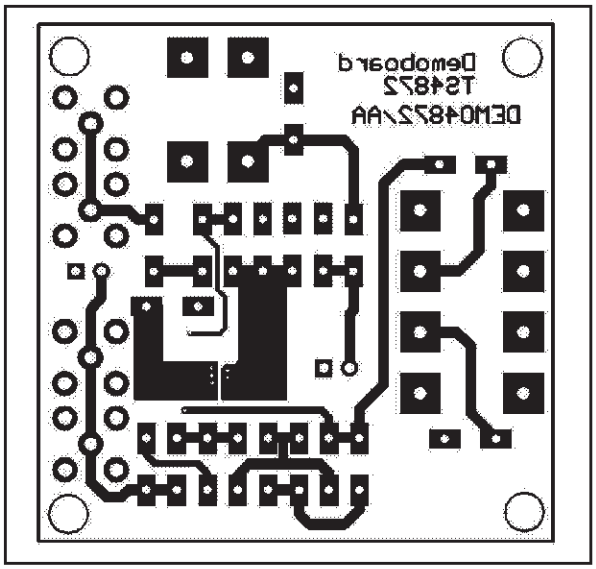


Fig. 83 : Flip Chip Demoboard Bottom Layer



■ BTL Configuration Principle

The TS4872 is a monolithic power amplifier with a BTL output type. BTL (Bridge Tied Load) means that each end of the load is connected to two single ended output amplifiers. Thus, we have :

Single ended output 1 = Vout1 = Vout (V)
Single ended output 2 = Vout2 = -Vout (V)

And Vout1 - Vout2 = 2Vout (V)

The output power is :

$$Pout = \frac{(2\,Vout_{RMS})^2}{R_L} (W)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

■ Gain In Typical Application Schematic (cf. page 1)

In flat region (no effect of Cin), the output voltage of the first stage is :

$$Vout1 = -Vin\frac{Rfeed}{Rin} (V)$$

For the second stage : Vout2 = -Vout1 (V)

The differential output voltage is

$$Vout2 - Vout1 = 2Vin\frac{Rfeed}{Rin} (V)$$

The differential gain named gain (Gv) for more convenient usage is :

$$Gv = \frac{Vout2 - Vout1}{Vin} = 2\frac{Rfeed}{Rin}$$

Remark : Vout2 is in phase with Vin and Vout1 is 180 phased with Vin. It means that the positive terminal of the loudspeaker should be connected to Vout2 and the negative to Vout1.

■ Low and high frequency response

In low frequency region, the effect of Cin starts. Cin with Rin forms a high pass filter with a -3dB cut off frequency .

$$F_{CL} = \frac{1}{2\pi\,Rin\,Cin} \quad (Hz)$$

In high frequency region, you can limit the bandwidth by adding a capacitor (Cfeed) in parallel on Rfeed. Its form a low pass filter with a -3dB cut off frequency .

$$F_{CH} = \frac{1}{2\pi\,Rfeed\,Cfeed} \quad (Hz)$$

■ Power dissipation and efficiency

Hypothesis :

- Voltage and current in the load are sinusoidal (Vout and Iout)
- Supply voltage is a pure DC source (Vcc)

Regarding the load we have :

$$V_{OUT} = V_{PEAK} \sin\omega t (V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} (A)$$

and

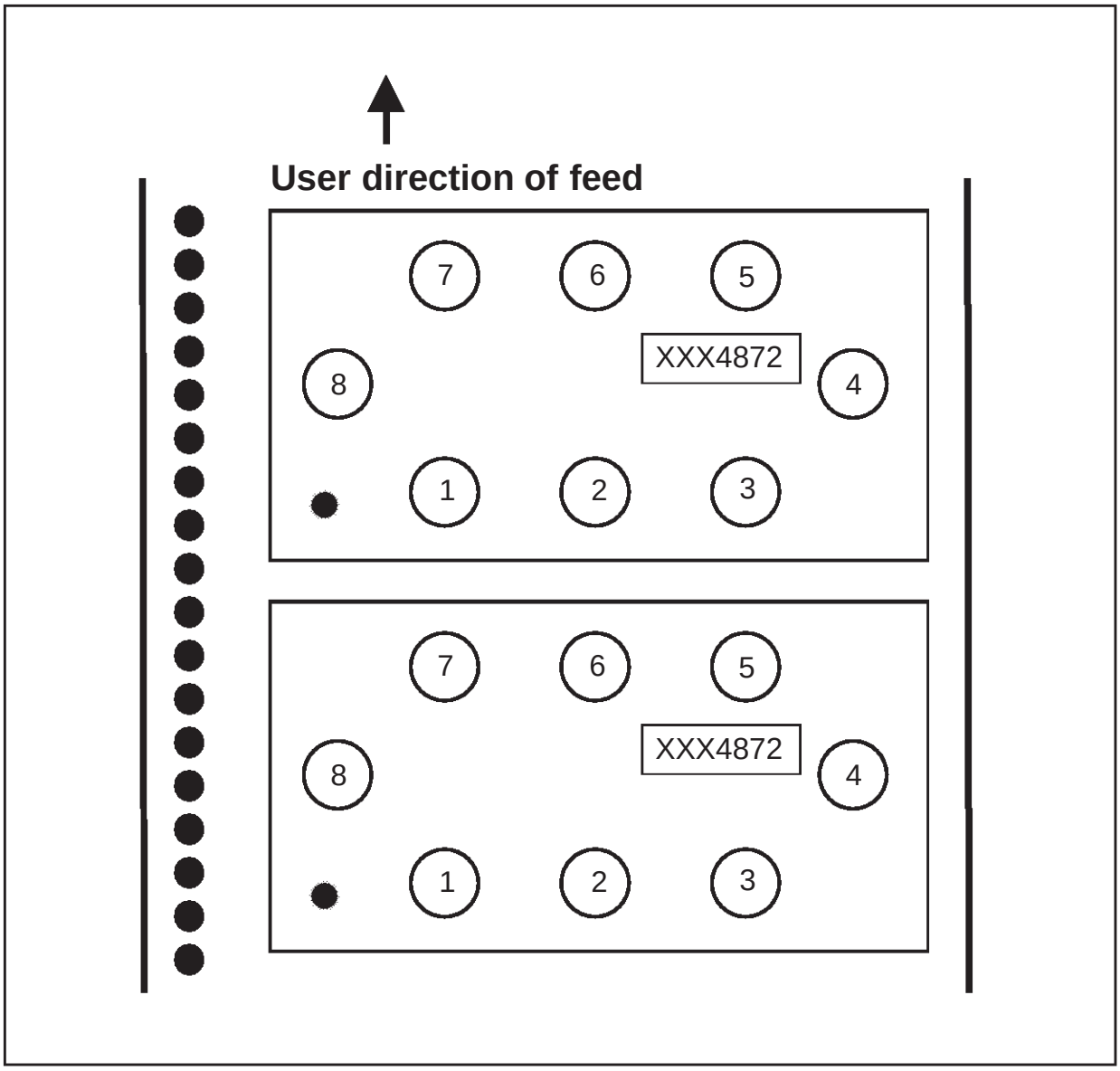
$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} (W)$$

Then, the average current delivered by the supply voltage is

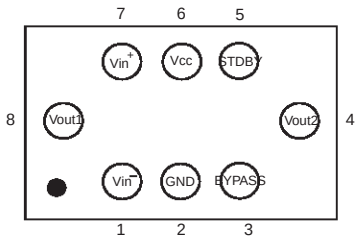
$$Icc_{AVG} = 2\frac{V_{PEAK}}{\pi R_L} (A)$$

The power delivered by the supply voltage is
Psupply = Vcc Icc_{AVG} (W)

TAPE & REEL SPECIFICATION (top view)

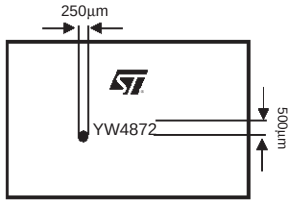


PIN OUT (top view)



■ Balls are underneath

MARKING (top view)



■ Y : Year
■ W : Week with two digits
■ Example : 1254872

PACKAGE MECHANICAL DATA

FLIP CHIP - 8 BUMPS

■ Die size : (3.02mm ±10%) x (1.52mm ±10%)
■ Die height (including bumps) : 540µm ±50µm
■ Bumps diameter : 140µm ±15µm
■ Silicon thickness : 400µm ±25µm
■ Pitch: 500µm ±10µm and 750µm ±10µm