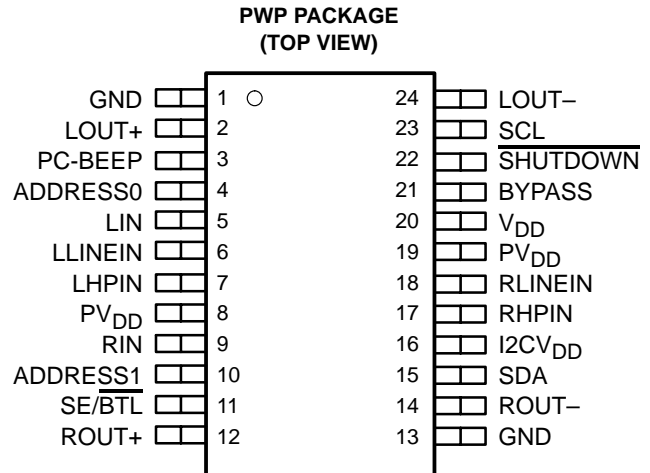


# TPA0172 2-W STEREO AUDIO POWER AMPLIFIER WITH I<sup>2</sup>C BUS

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- I<sup>2</sup>C Bus Controllable
- 2-W/Ch Output Power Into 4-Ω Load
- Low Supply Current and Shutdown Current
- Depop Circuitry
- Digital Volume Control From 20 dB to –60 dB
- Internal Gain Control, Which Eliminates External Gain-Setting Resistors
- Fully Differential Input
- Stereo Input MUX
- PC-Beep Input
- Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load
- Compatible With PC 99 Portable Into 8-Ω Load
- Surface-Mount Power Packaging  
24-Pin TSSOP PowerPAD™



## description

The TPA0172 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 4-Ω loads. This device utilizes the I<sup>2</sup>C bus to control its functionality, which minimizes the number of external components needed, simplifies the design, and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0172 has less than 0.2% THD+N from 20 Hz to 20 kHz.

Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers at power up, power down, and while transitioning in and out of shutdown mode.

The overall gain of the amplifier is controlled digitally by the volume control registers which are programmed via the I<sup>2</sup>C interface. At power up, the amplifier defaults to –60 dB in BTL mode, or –66 dB in SE mode. There are four registers that contain the gains: left BTL, right BTL, left SE, and right SE. Each register contains six bits, which allows 64 gain steps from –60 dB to 20 dB in 1.25-dB steps, and two bits that mute the amplifier.

The TPA0172 only consumes 6.5 mA of supply current during normal operation. A shutdown mode is included that reduces supply current to less than 15 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable on TO-200-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA0172 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

## AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0172PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0172PWPR).



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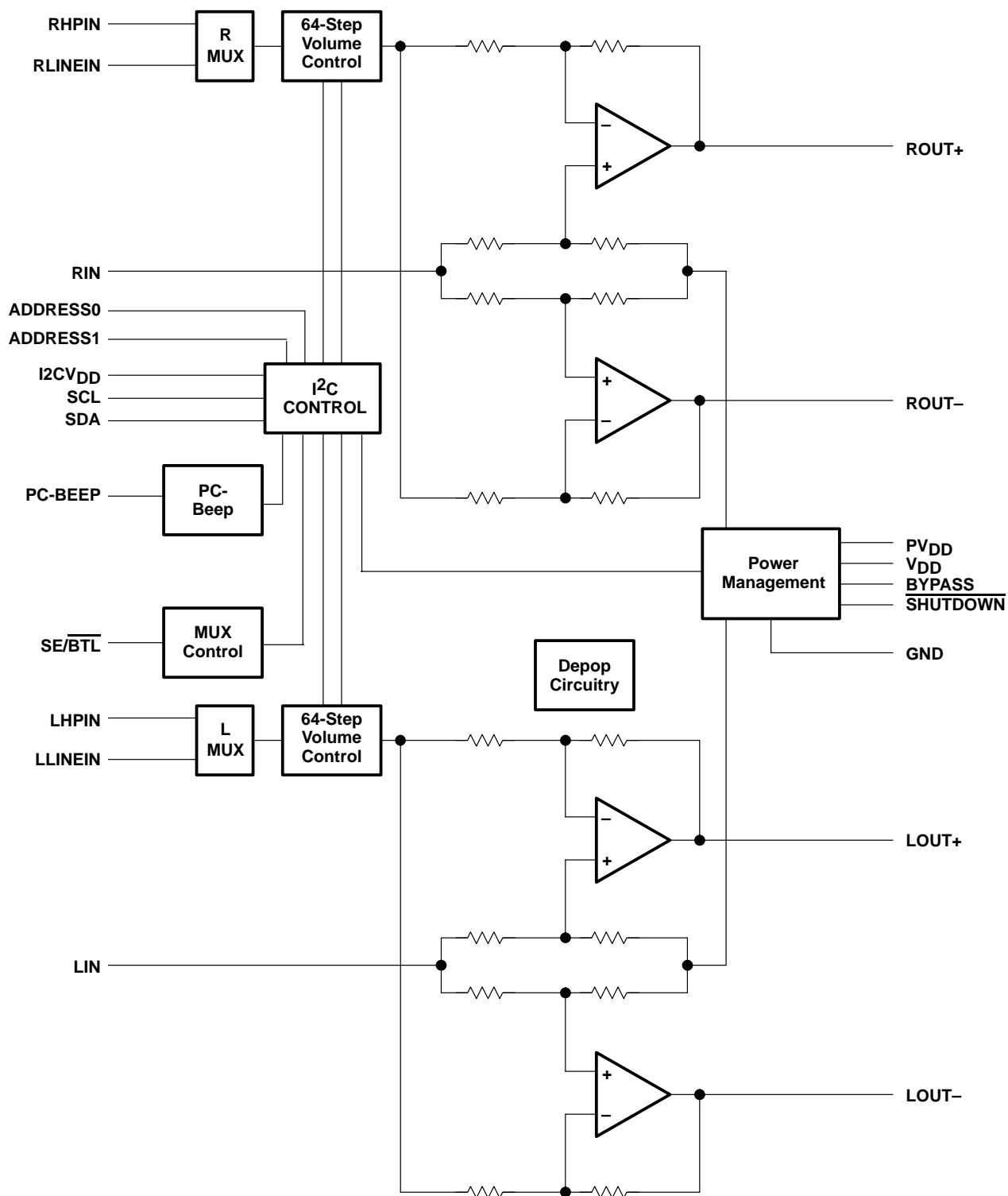
# TPA0172

## 2-W STEREO AUDIO POWER AMPLIFIER

### WITH I<sup>2</sup>C BUS

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#### functional block diagram



**TPA0172**  
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### Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ADDRESS0	4	I	Bit 0 of user-settable portion of device's I <sup>2</sup> C address.
ADDRESS1	10	I	Bit 1 of user-settable portion of device's I <sup>2</sup> C address.
BYPASS	21		Tap to voltage divider for internal midsupply bias generator.
GND	1, 13		Ground connection for circuitry. Connect to thermal pad
LHPIN	7	I	Left-channel headphone input, selected when SE/BTL is held high, or programmed via I <sup>2</sup> C.
LIN	5	I	Common left input for fully differential input. AC ground for single-ended inputs.
LLINEIN	6	I	Left-channel line input, selected when SE/BTL is held low, or programmed via I <sup>2</sup> C.
LOUT+	2	O	Left-channel positive output in BTL mode, and positive output in SE mode.
LOUT–	24	O	Left-channel negative output in BTL mode, and high impedance in SE mode.
PC-BEEP	3	I	The input for PC-BEEP mode which is enabled when a > 1-V (peak-to-peak) square wave is input to this terminal, when PCB ENABLE is held high, or programmed via I <sup>2</sup> C. If not used, ground this terminal.
I2CVDD	16	I	The voltage on this terminal sets the trip points for the I <sup>2</sup> C interface. If the system I <sup>2</sup> C bus is running at 3.3 V, then tie this terminal to 3.3 V. If the system I <sup>2</sup> C bus is running at 5 V, then tie this terminal to 5 V.
PVDD	8, 19	I	Power supply
RHPIN	17	I	Right-channel headphone input, selected when SE/BTL is held high, or programmed via I <sup>2</sup> C.
RIN	9	I	Common right input for fully differential input. AC ground for single-ended inputs.
RLINEIN	18	I	Right-channel line input, selected when SE/BTL is held low, or programmed via I <sup>2</sup> C.
ROUT+	12	O	Right-channel positive output in BTL mode, and positive output in SE mode.
ROUT–	14	O	Right-channel negative output in BTL mode, and high impedance in SE mode.
SCL	23	I	I <sup>2</sup> C clock line
SDA	15		Serial data line of the I <sup>2</sup> C bus. Pullup resistor must comply with the I <sup>2</sup> C standard: minimum value = 3 kΩ, maximum value = 19 kΩ. Pull up to I2CVDD
SE/BTL	11	I	Input MUX control input. When this terminal is held high, the LHPIN or RHPIN, and the SE output are selected. When this terminal is held low, the LLINEIN or RLINEIN, and the BTL output are selected. This functionality can also be programmed via I <sup>2</sup> C.
SHUTDOWN	22	I	When held low, this terminal places the device in the shutdown mode, except for the PC-BEEP input and the I <sup>2</sup> C bus.
VDD	20	I	Power supply



# TPA0172

## 2-W STEREO AUDIO POWER AMPLIFIER

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{DD}$	6 V
Bus voltage, I <sup>2</sup> CV <sub>DD</sub>	6 V
Input voltage, $V_I$	–0.3 V to $V_{DD}$ 0.3 V
Continuous total power dissipation	Internally Limited (see Dissipation Rating Table)
Operating free-air temperature range, $T_A$	–40°C to 85°C
Operating junction temperature range, $T_J$	–40°C to 150°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$
PWP	2.7 W <sup>‡</sup>	21.8 mW/°C	1.7 W	1.4 W

<sup>‡</sup> See the Texas Instruments document, *PowerPAD™ Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD™* on page 33 of the before mentioned document.

#### recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{DD}$		4.5	5.5	V
Bus voltage, I <sup>2</sup> CV <sub>DD</sub> (see Note1)		3	5.5	V
High-level input voltage, $V_{IH}$	SE/BTL	4		V
	SHUTDOWN	2		
	ADDRESS0, ADDRESS1	3.5		
	SDA, SCL	0.7 I <sup>2</sup> CV <sub>DD</sub>		
Low-level input voltage, $V_{IL}$	SE/BTL		3	V
	SHUTDOWN		0.8	
	ADDRESS0, ADDRESS1		0.8	
	SDA, SCL		0.3 I <sup>2</sup> CV <sub>DD</sub>	
Operating free-air temperature, $T_A$		–40	85	°C

NOTE 1: I<sup>2</sup>CV<sub>DD</sub> must be less than or equal to  $V_{DD}$ .

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**electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OS</sub>	Output offset voltage (measured differentially)	$V_I = 0\text{ V}$ , $A_V = 20\text{ dB}$			20	mV
PSRR	Power supply rejection ratio	$V_{DD} = 4.5\text{ V to }5.5\text{ V}$		75		dB
I <sub>IH</sub>	High-level input current	$V_{DD} = 5.5\text{ V}$ , $V_I = V_{DD}$			1	$\mu\text{A}$
I <sub>IL</sub>	Low-level input current	$V_{DD} = 5.5\text{ V}$ , $V_I = 0\text{ V}$			1	$\mu\text{A}$
Z <sub>i</sub>	Input impedance		7.5			k $\Omega$
I <sub>DD</sub>	Supply current	BTL mode		8	12	mA
I <sub>DD(SD)</sub>	Supply current, shutdown mode	PC-BEEP = 0 V		15	35	$\mu\text{A}$
		PC-BEEP = $V_{DD}/2$		50	90	$\mu\text{A}$

**operating characteristics,  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 4\text{ }\Omega$ , Gain = 20 dB, BTL mode (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>O</sub>	Output power	THD = 0.08%, $f = 1\text{ kHz}$		2		W
THD + N	Total harmonic distortion plus noise	P <sub>O</sub> = 1 W, $f = 20\text{ Hz to }20\text{ kHz}$		0.3%		
B <sub>OM</sub>	Maximum output power bandwidth	THD = 1%		>20		kHz
	Supply ripple rejection ratio	$f = 1\text{ kHz}$ , $C_B = 0.47\text{ }\mu\text{F}$				dB
		BTL mode		-58		
		SE mode		-52		
V <sub>n</sub>	Noise output voltage	$C_B = 0.47\text{ }\mu\text{F}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , Gain = 6 dB BTL, 0 dB SE		29		$\mu\text{VRMS}$
		SE mode		23		

## TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power
		1, 2, 4, 6
V <sub>n</sub>	Output noise voltage	vs Frequency
		3, 5, 7
	Supply ripple rejection ratio	vs Frequency
		8, 9
	Crosstalk	vs Frequency
		10, 11
	Shutdown attenuation	vs Frequency
		12
	Closed loop response	13, 14
P <sub>O</sub>	Output power	vs Load resistance
		15, 16
P <sub>D</sub>	Power dissipation	vs Output power
		17, 18
		vs Ambient temperature
		19



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## selection of components

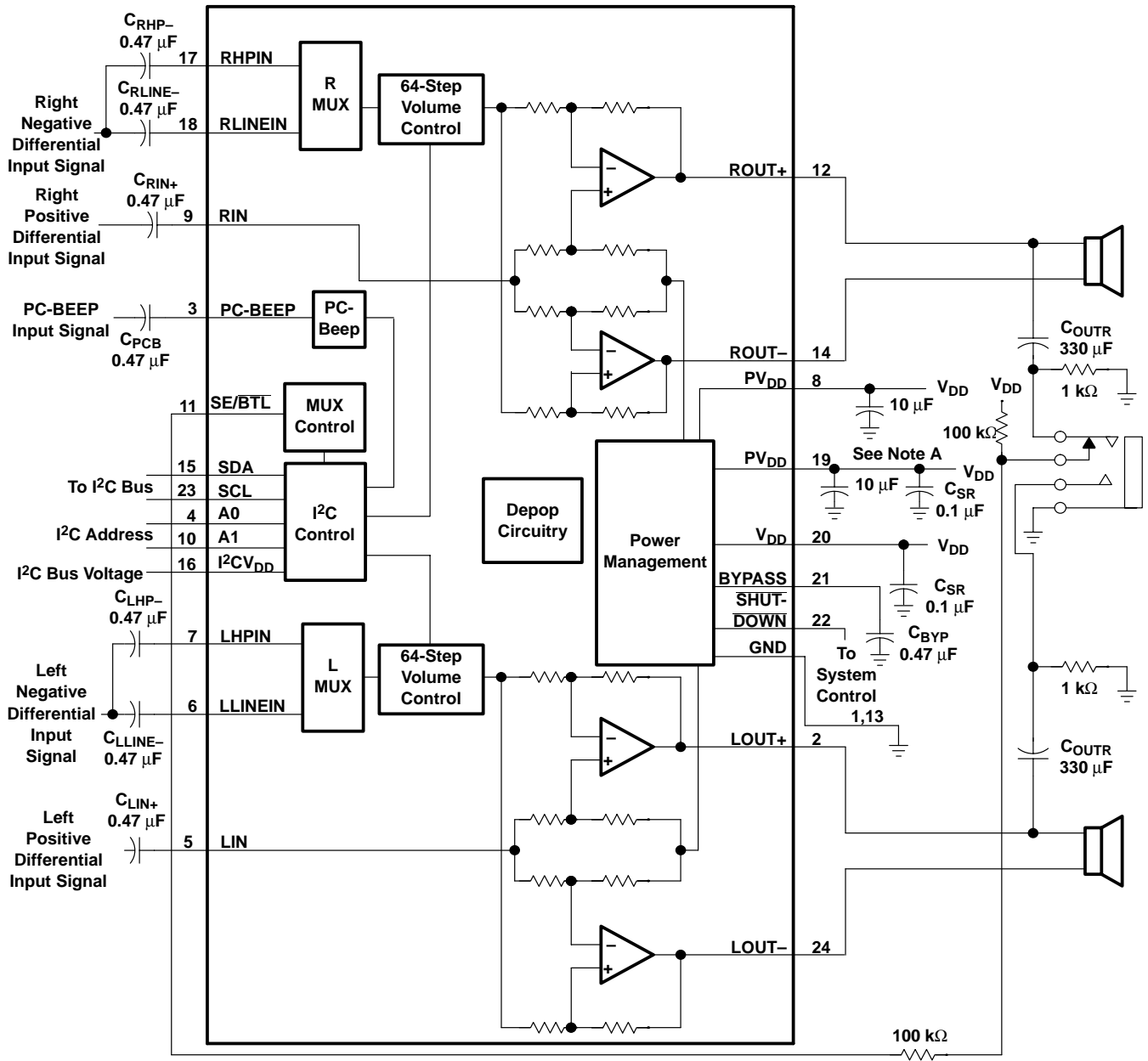
The schematic diagram illustrates the internal architecture of the AD1981 audio codec. Key components and connections include:

- Inputs:** Right Headphone Input Signal (17), Right Line Input Signal (18), Left Headphone Input Signal (7), Left Line Input Signal (6), PC-BEEP Input Signal (3), I<sup>2</sup>C Address (4, 10), I<sup>2</sup>C SDA (15), I<sup>2</sup>C SCL (23), and I<sup>2</sup>C Bus Voltage (16).
- Internal Blocks:** R MUX, L MUX, 64-Step Volume Control (for both channels), I<sup>2</sup>C Control, MUX Control, PC-BEEP, and Power Management.
- Outputs:** ROUT+ (12), ROUT- (14), LOUT+ (2), and LOUT- (24).
- Power and Control:** PV<sub>DD</sub> (8, 19), V<sub>DD</sub> (20), BYPASS (21), SHUT-DOWN (22), and GND (22).
- External Components:** Capacitors (C<sub>IRHP</sub>, C<sub>IRLINE</sub>, C<sub>RIN</sub>, C<sub>ILHP</sub>, C<sub>ILLINE</sub>, C<sub>LIN</sub>, C<sub>PCB</sub>, C<sub>OUTR</sub>, C<sub>BYP</sub>, C<sub>CSR</sub>) and resistors (100 kΩ, 1 kΩ, 330 μF).

**Figure 20. Typical TPA0172 Application Circuit Using Single-Ended Inputs and Input MUX**

## APPLICATION INFORMATION

### selection of components (continued)



NOTE A: A 0.1-μF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 μF or greater should be placed near the audio power amplifier.

**Figure 21. Typical TPA0172 Application Circuit Using Differential Inputs**