Unit 6: Elements of Digital Electronics

Xueqi Li*
(Dated: Apr 28, 2018)

INTRODUCTION

Binary

To change a number to binary or to convert back to decimal, one can use following equation:

$$\begin{aligned}&(B_nB_{n-1}\cdots B_2B_1B_0)_2 \qquad (1)\\ :=&\sum_{i=0}^{n} B_i 2^i = \sum_{i=0}^{k} D_i 10^i\\ =:&(D_kD_{k-1}\cdots D_2D_1D_0)_{10}\end{aligned}$$

On the other hand, for any base-n to base-m numberal system:

$$\begin{aligned}&(N_aN_{a-1}\cdots N_2N_1N_0)_2 \qquad (2)\\ :=&\sum_{i=0}^{a} N_i n^i = \sum_{i=0}^{b} M_i m^i\\ =:&(M_bM_{b-1}\cdots M_2M_1M_0)_{10}\end{aligned}$$

For example, if one wants to convert $(137)_{10}$, using Equation 2, one can find following:

$$\begin{aligned}&(137)_{10}\\ &=1\times 10^2+3\times 10^1+7\times 10^0\\ &=1\times 2^7+1\times 2^3+1\times 2^0\\ &=(10001001)_2\end{aligned}$$

On the other hand, if one wants to convert $(100101)_2$ to decimal, using Equation 2,one can obtain:

$$\begin{aligned}&(100101)_2\\ &=1\times 2^5+1\times 2^2+1\times 2^0\\ &=3\times 10^1+7\times 10^0\\ &=37\end{aligned}$$

Logic and Truth Table

It is well-know that from logic equation to truth table, one can just plug in all possible input, and calculate the output. On the other hand, one may wants to convert a truth table into logic equation. To do so, one can chose each output 1 line from the truth table, and add (or) them up.

For example, a selector have n input, and $\log_2(n)$ select input. The select input select the input to be the output.

A	B	X	Y	O
1	0	0	1	1
1	1	0	1	1
0	0	0	1	0
0	1	0	1	0
0	1	1	0	1
1	1	1	0	1
0	0	1	0	0
1	0	0	0	0

TABLE I: Truth table of a 2 selector. A,B are input; X,Y are select input

For example, a 2 selector have truth table as Table I. We can chose the output 1 one and add them, Thus we have

$$O=A\bar{B}\bar{X}Y+AB\bar{X}Y+\bar{A}BX\bar{Y}+ABX\bar{Y}$$

Transistor-transistor Logic

In TTL system, the binary number can be present as high or low voltage. In ideal case, 0V is low and 5V is high. However, in real world, it is not possible to always obtain a 5V or 0V voltage. Thus, for TTL standard, any input higher than 2V is high, and any input lower than 0.8V is low. On the other hand, any output 3.5V is high and any ouput 0.5V is low.

Logic Gate

A logic gate accept some inputs and gives an output. The logic gate's truth table is same as mathematical logic. In the lab, we use NOT, AND, NAND, OR, NOR, XOR, and XNOR gate. The truth table is given in the appendix.

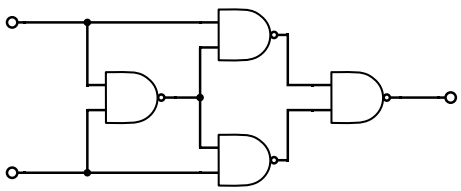


FIG. 1: Form a XOR gate using NAND gate

One can use NAND gate to form any other logic gate. For example, Figur 1 present how to form a XOR gate from NAND gate. The truth table is in the appendix.

Full-adder

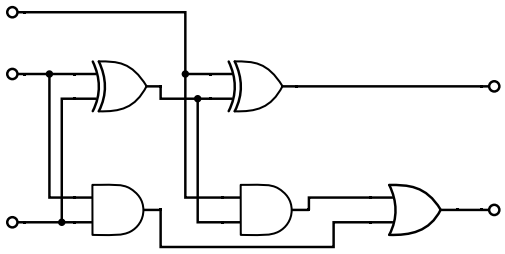


FIG. 2: A full-adder

One importent application of logic gate is full-adder, presented in Figure 2, where the left side is input and the right side is output. The output of a full-adder is the result of binary addition of the input.

Two Bit Half-adder

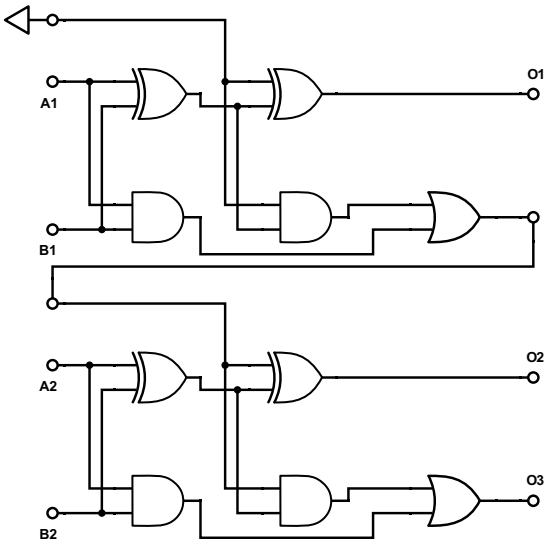


FIG. 3: A Two Bit Half-adder

Once obtain a full-adder, one can use full-adder to form a higher bit adder. For example, one can obtain a two bit half-adder as in Figure 3

Flip-flop

A Flip-flop, shown in Figure 4, can output one or zern when input are different and hold the output when two ouput are zero. There are a few application of flip-flop.

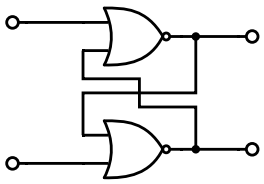
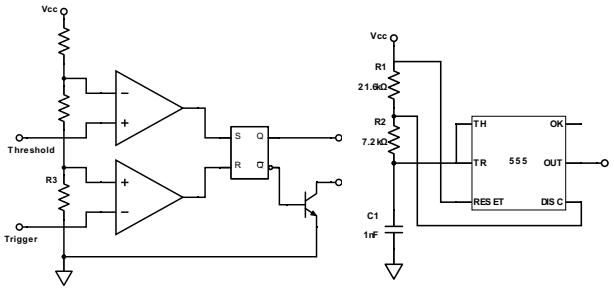


FIG. 4: A Flip-flop

Clocks



(a) 555 Chip (b) A Clock

FIG. 5: An application of flip-flop

A nice application of flip-flop is clock. The key of the clock is the 555 chip, which is an application of flip-flop. The circuit of a 555 chip is present in Figure 5a, where all resistors are 5kΩ. The 555 chip divide $V_{\rm CC}$ into 3 parts, when trigger voltage is larger than 1/3 $V_{\rm CC}$ and threshold voltage is smaller than 2/3 $V_{\rm CC}$, the out put is hold, otherwise it the output is 1 or zero if trigger voltage is below 1/3 $V_{\rm CC}$ or threshold voltage is higher than 2/3 $V_{\rm CC}$.

Than the clock is present in Figure 5b. This circuit can let the voltage periodically output zero or one, depending on the RC circuit. Thus, using by calculate the voltage in capastor, one can find the period of the circuit.

$$\begin{aligned} V_C &= V_{\rm CC}(1-e^{-\frac{t}{RC}}) \\ \Rightarrow t_{\rm high} &= (R_1+R_2)C\ln(2) \\ t_{\rm low} &= R_2C\ln(2) \\ \Rightarrow T &= (R_1+2R_2)C\ln(2) \end{aligned}$$

The duty cycle is how much time the voltage ouput is high:

$$\frac{t_{\rm high}}{T} = \frac{R_1+R_2}{R_1+2R_2}$$

For example, if one wants to have a 40kHz frequency clock with a 80% duty cycle, by above equation, one can use a 2.164kΩ and 7.213kΩ resistors and a 1nF capastor, as the value shown in Figure 5b.

Clock Edge

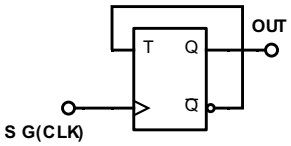


FIG. 6: Clock Edge

Another example of using D flip-flop is Clock Edge, as in Figur 6. The effect of it is simple. When clock is reasing from low to high, the output Q is same as the input D, otherwise it holds. Thus we see that if we connect $\bar{Q}$ to D, than the output Q will give a clock with double the period.

Debounce

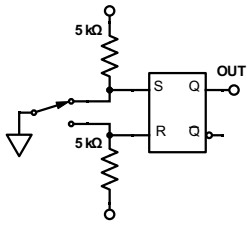


FIG. 7: A Debouncer Example

Another nice application is a debouncer, as presented in Figur 7. This use the hold function so that the output not mistakenly change the output for counter.

DATA AND CALCULATION

Clocks

In the lab, we wish to obtain a frequency of 40 kHz and a duty cycle of 80%. By using Equation 5, we find $R_1 = 21640\Omega$ and $R_2 = 7213\Omega$ if we want to use a 1nF capastor. In lab, we use a 20.73(2)kΩ and 7.19(1)kΩ resistor and a 1.00(1)nF capastor, as shown in Figure 5.

Signal Generator

The signal generator on TTL mode can only give square wave. This wave does not change on high frequency.

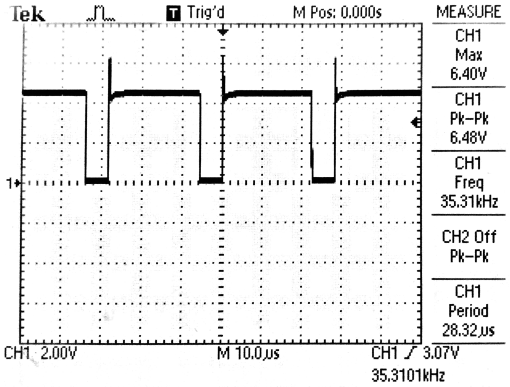


FIG. 8: Result for clock

XOR gate

We want to build a XOR gate using NAND gate, as in Figure 1. The result is same as the truth table of XOR gate.

Two Bit Half-adder

Following Figure 3, we obtained a two bit half-adder. The result is same as the truth table of a two bit half-adder.

Threshold Test

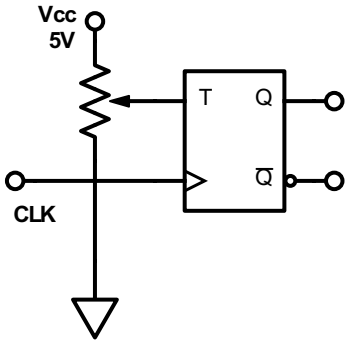


FIG. 9: circuit for Threshold Test

We using the circuit as in Figure 9. By changing the input voltage, we obtained a result as in Table II.

Clock Edge

Using a circuit as in Figure 6, we obtained a result as in Figure 10.

D [V]	Error on D [V]	Q	$\bar{Q}$
5.00	0.02	1	0
4.95	0.02	1	0
4.92	0.02	1	0
4.90	0.02	1	0
1.7	0.02	1	0
1.43	0.02	1	0
1.47	0.02	0	1

TABLE II: Result of threshold test

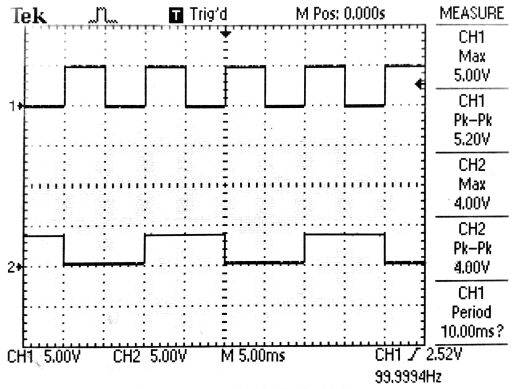
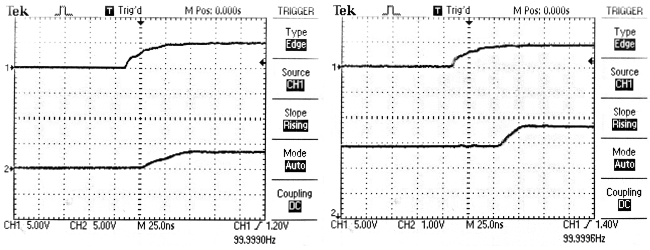


FIG. 10: Result of clock edge

Propagation Delay



(a) Delay for a D flip-flop (b) Delay for a 7404 chip

FIG. 11: Measure Propagation Dela

Using the clock edge circuit, one can measure the propagation delay of the flip-flop chip. A result is obtained in Figure 11. On the other hand, as a comparison, we also measure a delay of a 7404 chip. We see that the delay of a D flip-flop chip is 15(2)ns. On the other hand, the delay of a 7494 chip is 50(5)ns, which means each component is 8(5)ns.

Debouncer

Following Figure 7, we can obtained a debouncer. The result of the debouncer is shown as in Figur 12. We see that the voltage use 60(10)ns from low to high. Indeed, in the lab we see that the output shows the same behavior.

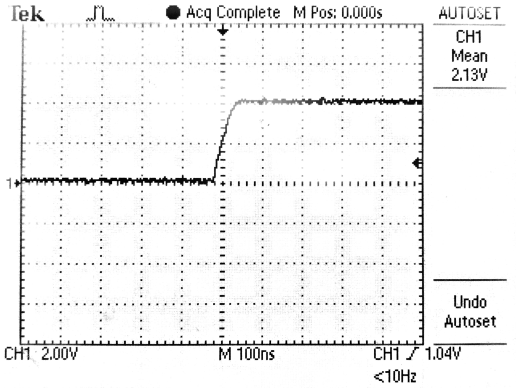


FIG. 12: Result of debouncer

By connect the debouncer to a 74393 chip, we obtained a counter of switch press.

ANALYSIS

Clock

From the result we see that we achieve a 35.3(2)kHz clock, it is within a 15% range of a 40kHz clock. We see that it is a 79(1)% duty cycle. This result is good.

Signal Generator

From the lab we see that signal generator can give a square wave in TTL mode. The wave is independent from the frequency.

XOR Gate

In the lab, we successfully achieve a XOR gate by using NAND gate.

Two bit half-adder

In the lab, we successfully achieve a two bit half-adder.

Threshold Test

From the Table II, we see that the output of Q and $\bar{Q}$ changed at 1.45(2)V. This agree with the TTL standard.

Clock Edge

From Figure 10, we see that the output change in the rising edge. We see that the propagation delay of clock

edge is lower than the 7404 chip.

Debounce

A debouncer have indeed been achieved in the lab. With counter, the circuit behavior properly.

CONCLUSION

The result of this lab is good. One can use a more precise resistor as calculation to achieve a better result on the clock.

---

* Partner: Tianming Hai