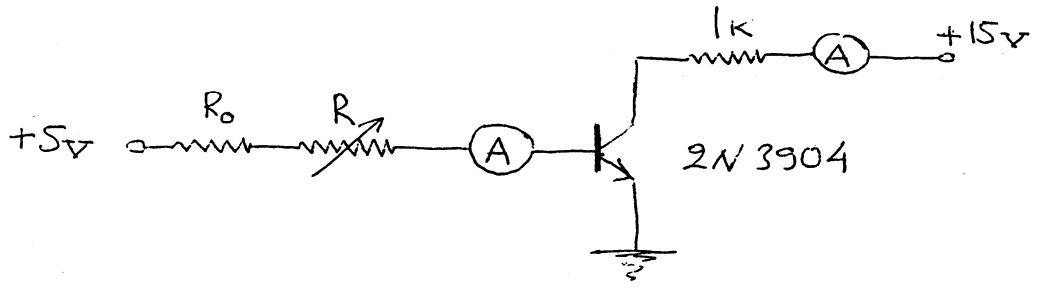
Phy 335, Unit 4
Transistors and transistor circuits (part one)

Mini-lecture topics (multiple lectures):

- **p-n junctions re-visited**
- **How does a bipolar transistor works; analogy with a valve**
- **Basic circuit rules for transistors**
- **BJT-based current source and its limits of operation**
- **Emitter follower design in detail**
- **Simple transistor circuits revisited; in BJT amp, what limits the amplification for $R_E = 0$?**
- **Effective collector resistance r_E in BJT**
- **JFET and MOSFET: types, principles of operation and characteristics**
- **Basic FET circuits**

1. Make a circuit with the transistor 2N 3904 or similar, as shown, and measure **current gain**:



Change variable R and measure the base current and the collector current. Calculate the current gain. Keep in mind that with current gain β of about 100, if you pass 1 mA in the base, the collector current is going to be about 100 mA. Higher base currents may be too high for the transistor to handle (look up transistor specs). Choose the limiting resistor R_0 accordingly. Your variable resistor R should be much higher than R_0 to provide base currents from a few μA to about 1 mA. Measure the voltage drop between collector and emitter and convince yourself that your BJT is not in saturation (explain what this means). Is β that you measure really constant over the whole current range?

2. **Emitter Follower:** Design, build and test an AC-coupled **emitter follower** circuit using 2N 2222 BJT or a similar BJT.

NOTES: Choose the emitter resistor R_E for the quiescent (DC, or zero signal) current to be around 5 mA. This is done keeping in mind that the emitter voltage should be chosen at approximately at 7.5 V (plus-minus 0.5 V), i.e. it should be positioned in the approximate center with respect to +15 V power supply. Explain why this centering of V_E is desirable; think of what happens at the emitter when you will apply AC signal of a significant amplitude to the base (you will see this experimentally a little later).

To achieve the desired voltage level at the emitter, the base should be appropriately DC biased. Choose the *ratio* of the base biasing resistors accordingly. Further, choose biasing resistor *values* so that the DC bias of the base remains fixed to within 10%. To achieve this, consider the Thevenin equivalent of the base biasing voltage divider, and also consider the effective input resistance of the transistor base. For the latter recall the follower's main useful function, and assume current gain β of 100.

In this particular design the signal is coupled to the base through a capacitor to exclude DC shifts and/or slow signal level drifts (this is not necessarily so in all followers, of course, but in this case we want to have an AC coupled signal). Having this capacitor additionally creates a high-pass filter at the input. This can further help to exclude unwanted low frequencies. For example, if we know that the signal frequency will be always higher than, say, 300 Hz, we can exclude 60 Hz interference[1]. Choose the AC coupling capacitor so that –3 dB low frequency cut off of the effective RC filter is at about 300 Hz. Think very carefully about what effective resistor value should be used in this calculation.

Draw the circuit, show all calculations, label the elements (R's, C) and build the circuit. Measure and record all DC voltages at the 3 transistor terminals. Drive your follower from the function generator and observe the input and the output signals on the scope. If your follower works properly, you will see identical signals, shifted by about 0.6 V. This by itself is not very impressive. How can you prove that the follower indeed performs its main function of greatly increasing the effective load (emitter) resistance?

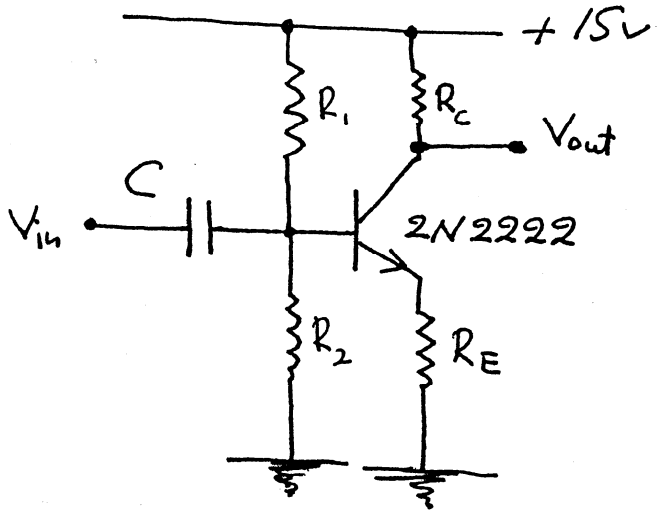
Hint: Try to drive the same load without a transistor, keeping all the other circuit elements the same (namely, keeping the same voltage divider). Do you see the difference? Record the results, and compare them to what you get using a follower.

Using the 2 V p-p signal from the signal generator(SG), measure and plot V_{out}/V_{in} vs. log(f) from 100 Hz to 1 MHz. Measure the phase shift between V_{in} and V_{out}. Explain the phase shift based on the RC filter theory (phasors again!).

[1] 60 Hz from the AC wall-socket power lines often interferes with small signals we want to measure.

Set f = 10 kHz, and vary V_{in} from 2 V to 20 V p-p. Measure V_{out} and explain what you see. Again, think about the reason we chose quiescent emitter voltage at about $V_E \approx 0.5$ V_{CC}.

3. Build a BJT amplifier



Design a common emitter amplifier(amp) with the following parameters.

- V_{CC} = +15 V
- Output centered at 7.5 V
- Voltage gain of 15x
- Quiescent current of 0.5 mA
- Capacitive input rolloff frequency 200 Hz.

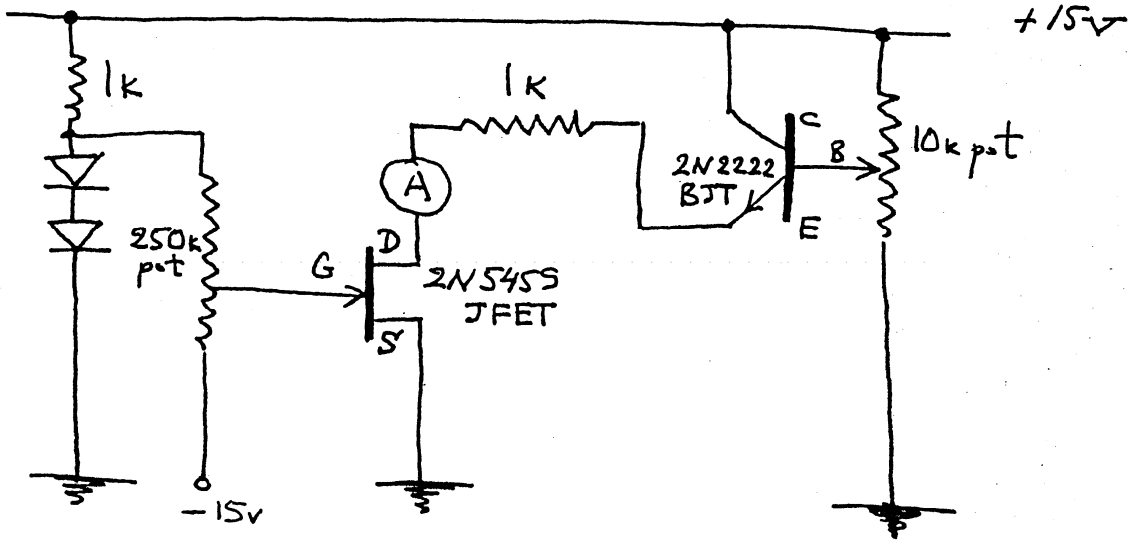
(Aim at being at least 15% within these specs.) Read the H&H book pp. 76-77 and the Lab Manual, pp. 98 and 115-117[2]. Ignore the temperature stability issues.

Explain BJT amp principle based on transistor rules, derive the formula for voltage gain. Describe in details how you designed your amplifier, with all the calculations shown. Explain why the divider looking into the base must be asymmetric here, while it is almost symmetric in the emitter follower. Test your amp at different frequencies below 200 Hz and much greater than 200 Hz (several kHz) with sinusoidal input signals. Make sure to provide small enough input. It will be multiplied by 15x, and you want to avoid violating the transistor rules. Is the output direct or inverted compared to the input? Think of the role of the RC filter at the input. Will this filter produce a phase shift at high frequency? Is the output shifted up by 7.5 V? What if you increase the input so that the output amplitude becomes greater than 7.5 V. Describe what happens. Sketch what you see on

[2] Erratum: R2 instead of R1 on p. 115.

the oscilloscope. Given your chosen R_E and the measured gain, find the transistor transconductance in Siemens.

4. FET characteristics. Wire the following circuit to measure JFET characteristics.



Circuit Notes:

1. This circuit allows measuring transistor characteristics: I_D as a function of V_{GS}, and I_D as a function of V_{DS}.
2. The indicated JFET has an n-type channel and p-type gate. This means that the gate-source would be forming a forward-biased p-n junction at gate voltages higher than the normal diode drop of about 0.6 V. Thus we can not apply positive potential to the gate significantly over that value, or the gate-source junction will conduct large current into the transistor.
3. As a result of the above consideration, in this circuit we use two diodes making a clip and thus limiting positive voltage from the divider to about 1.4 V, so that the divider can deliver from –15 V to +1.4 V. We will need only a few negative volts to pinch off the transistor (see the transistor characteristics printout.)
4. The emitter-follower which you built previously is used here to increase the impedance and to allow a second voltage divider to deliver full voltage to the JFET's drain. This will be used to change V_{DS} in measuring I_D vs. V_{DS}.

Determine the pinch-off voltage (also called gate-source cutoff voltage) V_P, defined as the voltage at which the current drops to about 1 μA. Compare what you found with the device specs sheet values. Determine I_{DSS} for $V_{GS} = 0$ at the highest V_{DS} you can get with your setup (up to +15V). You can short the gate to the ground, or dial zero volts from the divider. As before, compare your results with the device specs. With V_{DS} still at the highest value, plot the relationship between I_D and V_{GS} from $V = V_P$ (a few volts negative) to about V = 0.7 V positive. Next plot the relationship between I_D and V_{DS} up to the highest V_{DS} you can get with your setup. Do this plot once for $V_{GS} = 0$ and another

for the V_{GS} which gives a current I_D = 1 mA on the plateau (i.e., at large V_{DS} values). This current occurs at some V_{GS} between V_P and V=0. Show that at low voltages the transistor behaves as a voltage-dependent resistor. Plot this part of the two curves on an expanded scale separately. Calculate resistor values for the two curves. Calculate the FET's transconductance (in Siemens or inverse ohms[3]) at V_{GS} = 0 and at the V_{GS} corresponding to I_D = 1 mA.

[3] Inverse ohms are sometimes called mhos, particularly in data sheets.