DICE
DEPARTMENT OF INTERDISCIPLINARY COURSES IN ENGINEERING

CHITKARA UNIVERSITY

TOPIC:

Direct Memory Access (DMA)

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Direct Memory Access

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- In DMA, the CPU is idle and the peripheral device manage the memory buses directly.

● DMA controller takes over the buses to manage the transfer directly between the I/O device and memory.

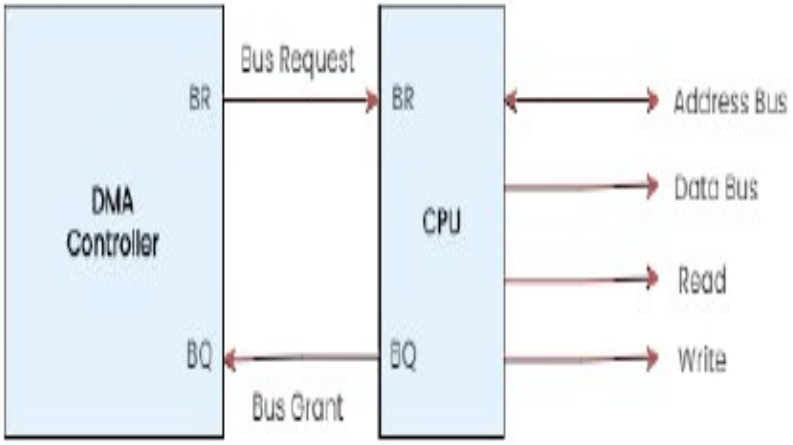
● The DMA transfer can be made in several ways.

● Burst Transfer - A block of memory words is transferred in a continuous burst at a time. Used for fast devices such as magnetic disks, where data transmission cannot be stopped or slowed down until an entire block is transferred.

● Cycle Stealing - Allows the DMA controller to transfer one data word at a time, after which it must return control of the buses to the CPU.

- The CPU merely delays its operation for one memory cycle to allow the direct memory I/O transfer to “steal” one memory cycle.

Working of DMA



- The Bus Request (BR) input is used by the DMA controller to request the CPU to relinquish control of the buses.

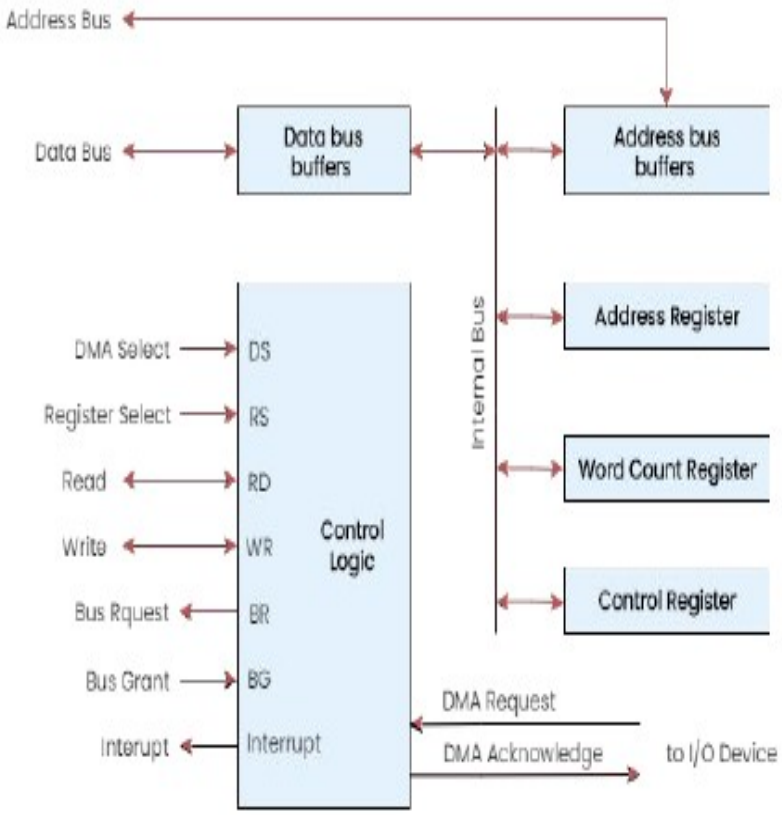
● When this input is active, the CPU terminates the execution of the current instruction and places the address bus, the data bus, and the read and write lines into a high-impedance state.(like an open circuit)

● The CPU activates the Bus Grant (BG) output to inform the external DMA that the buses are in the high-impedance state.(available)

● The DMA takes control of the buses to conduct memory transfers without processor intervention.

● When the DMA terminates the transfer, it disables the bus request line and the CPU disables the bus grant, takes control of the buses, and returns to its normal operation.

Direct and Indirect Addressing Modes



- The registers in the DMA are selected by the CPU through the address bus by enabling the DMA Select (DS) and Register Select (RS) inputs.

● When the BG (bus grant) = 0, the CPU can communicate with the DMA registers.

● When BG = 1 DMA can communicate directly with the memory.

● The DMA controller has three registers.

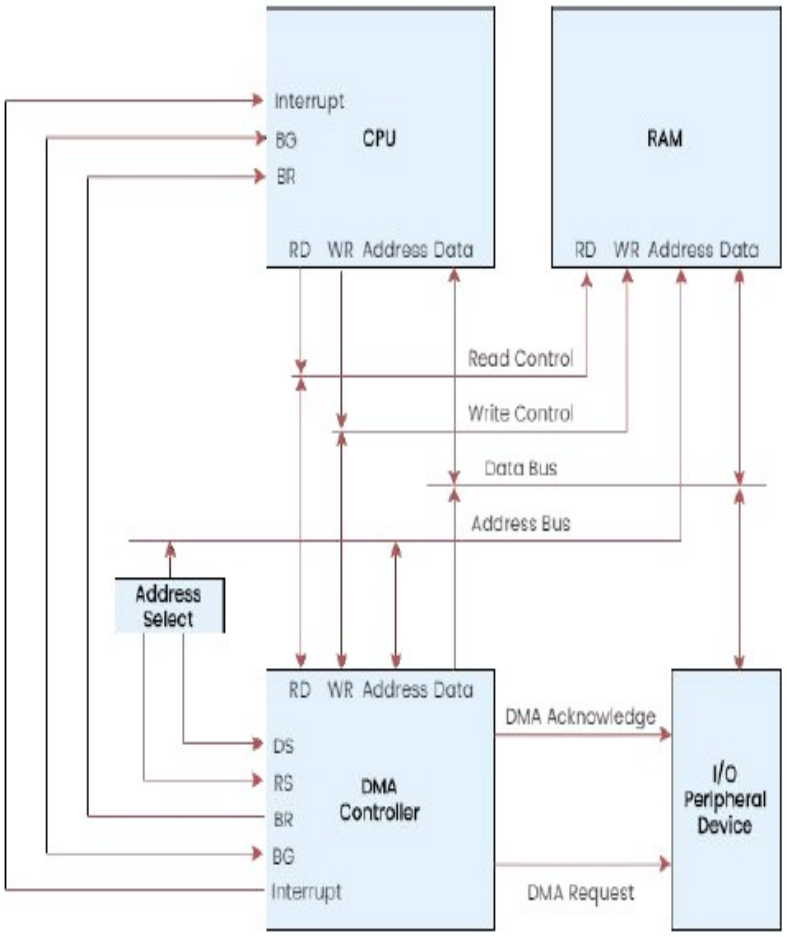
● The Address register contains an address to specify the desired location in memory.

● The Word Count Register holds the number of words to be transferred.

● The Control Register specifies the mode of transfer.

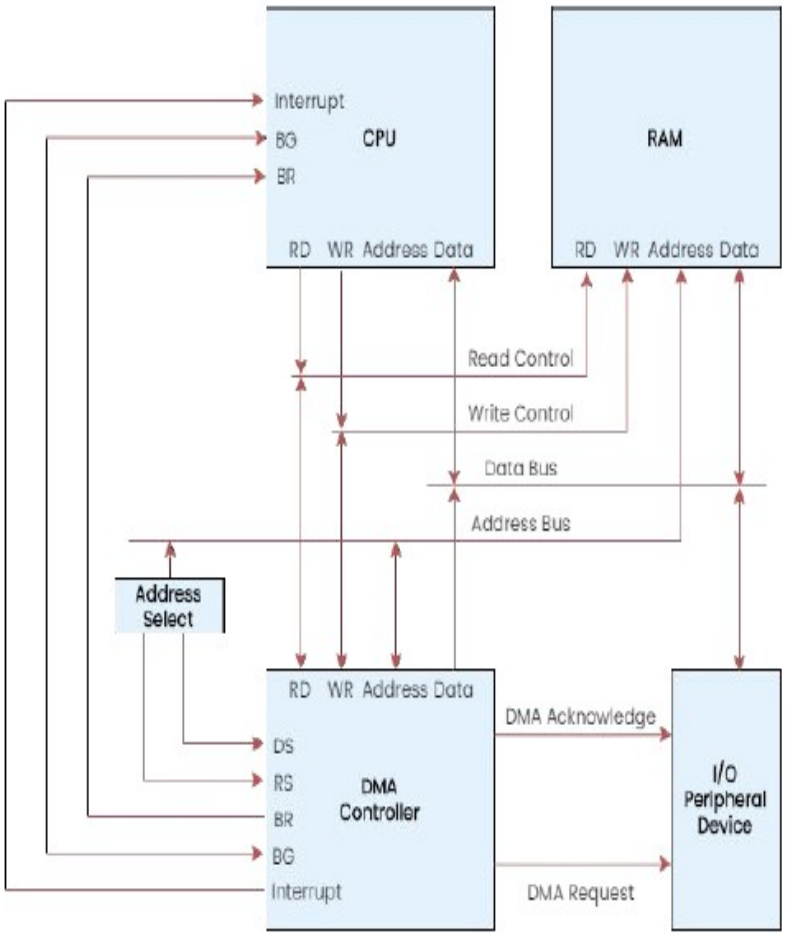
● The DMA communicates with the external peripheral through the request and acknowledge lines.

DMA Transfer



- I/O Device sends a DMA request.
- ➜ DMA Controller activates the BR line.
- ➜ CPU responds with BG line.
- ➜ The DMA puts the current value of its address register into the address bus, initiates the RD or WR signal, and sends a DMA acknowledge to the I/O device.
- ➜ I/O device puts a word in the data bus (for write) or receives a word from the data bus (for read).
- ➜ The peripheral unit can then communicate with memory through the data bus for direct transfer between the two units while the CPU is momentarily disabled.

DMA Transfer



➜ For each word that is transferred, the DMA increments its address register and decrements its word count register.
➜ If the word count does not reach zero, the DMA checks the request line coming from the I/O Device.
➜ If there is no request ,the DMA disables BR so that the CPU continues to execute its own program.
➜ When CPU requests another transfer, DMA requests bus again.
➜ If the word count register reaches zero, the DMA stops any further transfer and removes its bus request. It also informs the CPU of the termination by an interrupt.

Thank You