CHITKARA UNIVERSITY

Central Processing Unit: Introduction, General Register Organization

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Outline

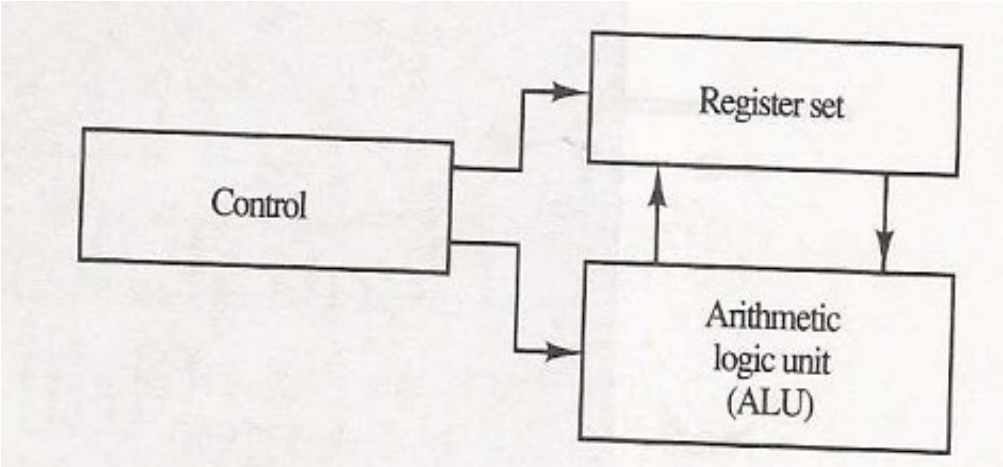
Central Processing Unit (CPU)

- Introduction
- General Register Organization

Introduction

- The part of computer that performs the bulk of data-processing operations is called the ***central processing unit*** and is referred to as the ***CPU***.
- The CPU is made up of three major parts:

1. The register set: stores intermediate data used during the execution of the instruction.
2. The ALU: performs the required microoperations for executing the instructions.
3. The control unit: supervise the transfer of information among the registers and instruct the ALU as to which operation to perform.

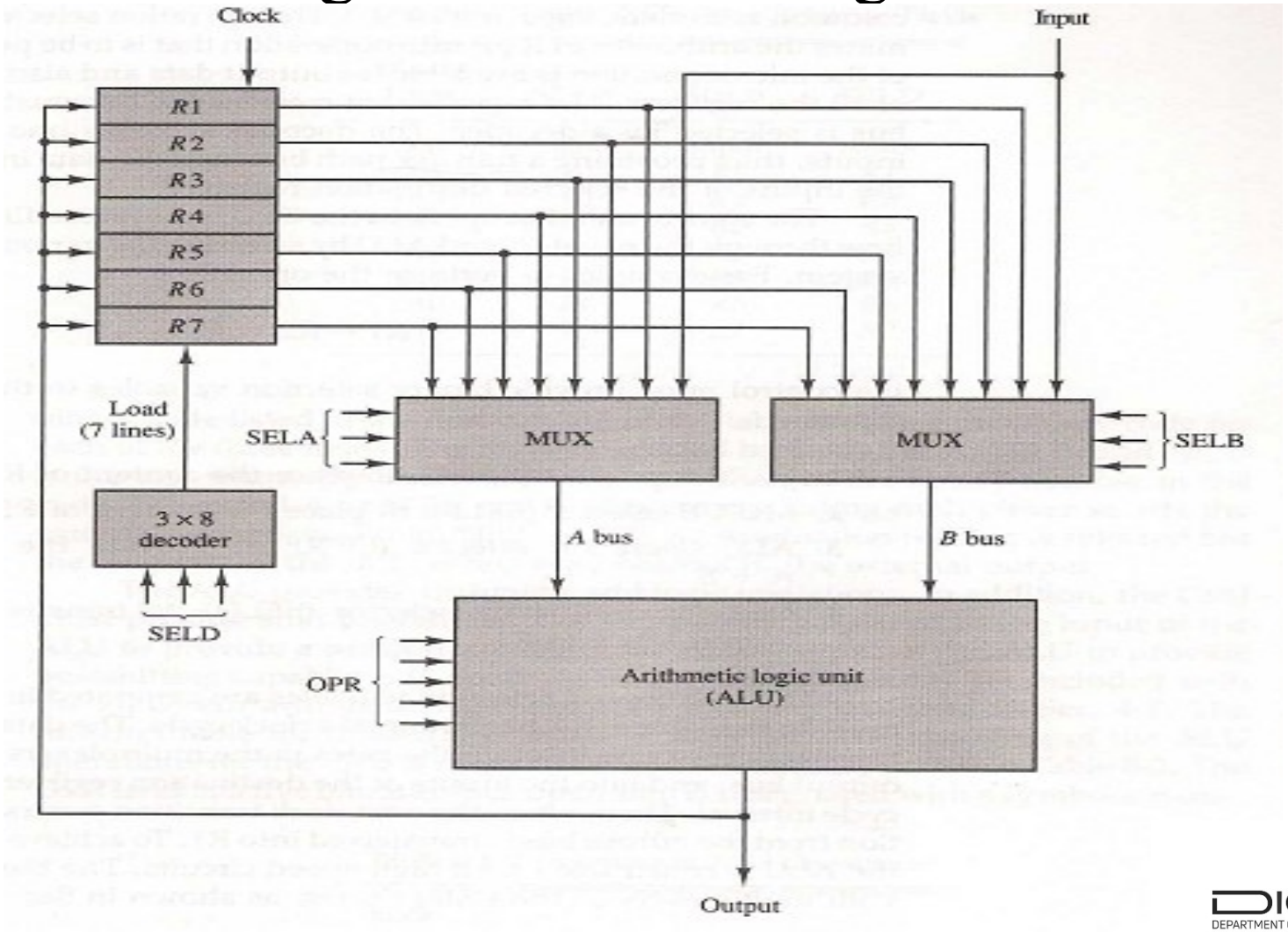


General Register Organization

- Memory locations are needed for storing pointers, counters, return address, temporary result etc. Having to refer to memory location for such applications is time consuming.
- because ***memory access is the most time-consuming operation in the computer.***
- It is more convenient and more efficient to store these intermediate values in processor registers. All of these registers are connect to a common bus system.
- The register communicate with each other not only for direct data transfer, but also while performing various micro operations.

BUS System

- The bus organization of 7-registers:



BUS System

- To perform operation: $R1 \leftarrow R2 + R3$

- The control must provide binary selection variables to the following sectors inputs:

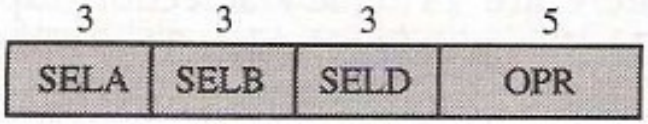
1. MUX A Sector (SELA): to place the content of R2 into bus A.
2. MUX B Sector (SELB): to place the content of R3 into bus B.
3. ALU operation Selector (OPR): To provide the arithmetic addition A+B.
4. Decoder Destination Selector (SELD): To transfer content of output bus in to R1.

BUS System

- The four control selection variables are generated in control unit and must be available at the beginning of clock cycle.
- The data from two source registers propagates through the gates in the multiplexers and the ALU, to the output bus, and into inputs of the destination register, all during the clock cycle interval.
- When the next clock transition occurs, the binary information from the output bus is transferred into R1.

Control Word

- There are 14 binary selection inputs in the unit, and their combined value specifies a ***control word***.



- The encoding of register selection field as:

Binary Code	SELA	SELB	SELD
000	Input	Input	None
001	*R1*	*R1*	*R1*
010	*R2*	*R2*	*R2*
011	*R3*	*R3*	*R3*
100	*R4*	*R4*	*R4*
101	*R5*	*R5*	*R5*
110	*R6*	*R6*	*R6*
111	*R7*	*R7*	*R7*

Control Word

- The encoding of ALU operation as:

OPR Select	Operation	Symbol
00000	Transfer A	TSFA
00001	Increment A	INCA
00010	Add $A + B$	ADD
00101	Subtract $A - B$	SUB
00110	Decrement A	DECA
01000	AND A and B	AND
01010	OR A and B	OR
01100	XOR A and B	XOR
01110	Complement A	COMA
10000	Shift right A	SHRA
11000	Shift left A	SHLA

- ALU provides arithmetic and logic operations. In addition, the CPU must provide shift operations.
- The shifter may be placed in the input of the ALU to provide preshift capability, or at the output of ALU to provide postshift capability. Some times it included in ALU.

Microoperations

- A control word of 14 bits is needed to specify a microoperations in the CPU.

E.g.

$$R1 \leftarrow R2 - R3$$

Field:	SELA	SELB	SELD	OPR
Symbol:	R2	R3	R1	SUB
Control word:	010	011	001	00101

➢A memory unit that stores control word is referred to as a CONTROL MEMORY.

➢By reading consecutive control words from memory, it is possible to initiate the desire sequence of microoperations for the CPU. This type of control is referred As micro-programmed control.

Microoperations

Microoperation	Symbolic Designation SELA	SELB	SELD	OPR	Control Word
$R1 \leftarrow R2 - R3$	R2	R3	R1	SUB	010 011 001 00101
$R4 \leftarrow R4 \vee R5$	R4	R5	R4	OR	100 101 100 01010
$R6 \leftarrow R6 + 1$	R6	—	R6	INCA	110 000 110 00001
$R7 \leftarrow R1$	R1	—	R7	TSFA	001 000 111 00000
Output $\leftarrow R2$	R2	—	None	TSFA	010 000 000 00000
Output $\leftarrow$ Input	Input	—	None	TSFA	000 000 000 00000
$R4 \leftarrow$ sh1 $R4$	R4	—	R4	SHLA	100 000 100 11000
$R5 \leftarrow 0$	R5	R5	R5	XOR	101 101 101 01100

Self Assessment

- ***State whether the following statements are true or false-***

1. The control unit fetches the instructions from the registers, decodes and then executes it.
2. The registers store the status of the CPU as well as information about the currently executing program.

MCQ

- The CPU reads and writes data to and from _____and transfers data to and from I/O devices.

(i) Memory system

(ii) Register

(iii) Control unit

(iv) Arithmetic and logic unit

- Constant registers is used to store _____.

(i) Floating point numbers

(ii) Read-only values

(iii) Addresses

(iv) Programs

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Thank You

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