11.52) ECM UE 3 Vorbereitung A Komplementare MOS-Logik (CMOS) 1) (MOS-Inverder n-Hanal MOSFET ZW2106A & p-Hoinel MOSFET ZVP2106A 0-Koung (MOSFET U, Vo & B n-Kanal MOSFET 0"=OV ante dusch was Worthheirs howelle: U/V9 intera 2 1"\$5V Gate - Isolierus durch SiOz - Schicht: Crate intern nill. 0-MOSFET ST 2) CMOS-NAND B 0-MOSTET Va H B n-MOSTET 0, UE UL Og 00 1 n-MOSTET 1 NAND 1, ausen wern alle imputs 1, 9 " sind h-Koinal - MOSFET: VDS,max = 60V Vas,min = 0.88 (Vas,max = 2.4V)
(Busing ye gemais data sheat) 24 (Sissing Temporatur Gare: L: [-55, 150]°C p- Wand -MOSFET: Vps, mov = -60V (Vas, mov = -3,5V) rubissiger Betriebstenpenahnbergit: I-55, 150 JC For "0" eine Spanning von <0,7 V = ideal OV -11 = 5 V (beir großer "0") (6) Berlitz



