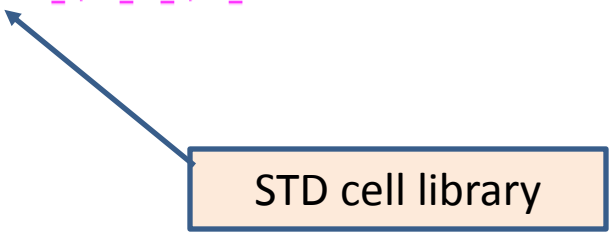
Lab 6: Synthesis (Design Compiler)

Important Files

- common.tcl: Path to common libraries
  - Standard Cell Library
- timing.tcl: Contains the Timing information
  - Timing Constrain
  - Clock Skew/Slew
  - Input/Output Delay
- DESIGN.tcl: Synthesis flow commands

common.tcl

```
set search_path [list "." "/tools4/syn2007.12/libraries/syn/"]
set synthetic_library [list "dw_foundation.sldb"]
set link_library [list "*" "/tools2/courses/ee6321/share/ibm13rflpvt/synopsys/scx3_cmos8rf_lpvt_tt_1p2v_25c.db" "dw_foundation.sldb"]
set target_library "/tools2/courses/ee6321/share/ibm13rflpvt/synopsys/scx3_cmos8rf_lpvt_tt_1p2v_25c.db"
```



- You can also add your own standard cells .db file here to tell design compiler to use them for mapping.
- You can also use set_dont_use CELLNAME to tell design compiler to not use certain cells when mapping.

timing.tcl

```
# Setting variables
set clk_period 12
set clk_uncertainty 0
set clk_transition 1.5
set typical_input_delay 0
set typical_output_delay 3
set typical_wire_load 0.001

#Create real clock if clock port is found
if {[sizeof_collection [get_ports clk]] > 0} {
  set clk_name "clk"
  set clk_port "clk"
  #If no waveform is specified, 50% duty cycle is assumed
  create_clock -name $clk_name -period $clk_period [get_ports $clk_port]
  set_drive 0 [get_clocks $clk_name]
}

#Set clock uncertainty
set_clock_uncertainty $clk_uncertainty [get_clocks $clk_name]
#Propagated clock used for gated clocks only
set_clock_transition $clk_transition [get_clocks $clk_name]

# Configure the clock network
set_dont_touch_network $clk_port


# Set delays: Input, Output
set_input_delay $typical_input_delay [all_inputs] -clock $clk_name
remove_input_delay -clock $clk_name [find port $clk_port]

set_output_delay $typical_output_delay [all_outputs] -clock $clk_name

# Set loading of outputs
set_load $typical_wire_load [all_outputs]
```

Define Variables

Find real clock
Or create fake clock if none
Clock is needed for timing reference

Set clock uncertainty/slew rate

Set_input_delay: amount of time the input signal is availabe after clock edge

Set_output_delay: amount of time the the signal is required before clock edge on output signals

Load cap values used on ports/nets

DESIGN.tcl (1)

```
########################################
# READ Design and Library              #
########################################
set BEHAVIORROOT "../rtl/"

set top_level lfsr1
source -verbose "common.tcl"
read_verilog {../rtl/lfsr1.v}
list_designs

########################################
# Design Constranits                   #
########################################
current_design $top_level
link
source -verbose "timing.tcl"
set_max_capacitance 0.001 [all_inputs]
set_max_fanout 4 $top_level
set_max_fanout 2 [all_inputs]
set_max_area 0
```

Read-in common.tcl

Read-in Design

Display design current read in

Read-in timing.tcl

Sets the max fanout DC can uses

Sets the target area
"0" means optimize for smallest possible

DESIGN.tcl (2)

```
########################################
# Compile for combinational logic      #
########################################
check_design
compile_ultra


########################################
# Write outputs                        #
########################################
set verilogout_no_tri TRUE
write -hierarchy -format verilog -output "${top_level}.nl.v"

# Generate Standard Delay Format (SDF) file
write_sdf -context verilog "${top_level}.temp.sdf"
# Generate report file
set maxpaths 20
set rpt_file "${top_level}.dc.rpt"
check_design > $rpt_file
report_area  >> ${rpt_file}
report_power -hier -analysis_effort medium >> ${rpt_file}
report_design >> ${rpt_file}
report_cell >> ${rpt_file}
report_port -verbose >> ${rpt_file}
report_compile_options >> ${rpt_file}
report_constraint -all_violators -verbose >> ${rpt_file}
report_timing -path full -delay max -max_paths $maxpaths -nworst 100 >> ${rpt_file}

quit
```

Check for errors/warning

COMPILE!!!

Avoid using “tri” nets

Generate output .nl.v

Generate SDF file

Report Synthesis REULTS

.dc.rpt (1)

```
Number of ports:                32
Number of nets:                 70
Number of cells:                41
Number of references:            6

Combinational area:          89.280004
Noncombinational area:      849.599993
Net Interconnect area:       undefined  (No wire load specified)

Total cell area:            938.879996
Total area:                  undefined
1
```

BE AWARE: This is just area from synthesis
(Doesn’t have actual interconnect/floor plan)

.dc.rpt (2)

```
Startpoint: lfsr_out_reg[27]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: lfsr_out[27]
          (output port clocked by clk)
Path Group: clk
Path Type: max

Point                                     Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                     0.00       0.00
clock network delay (ideal)               0.00       0.00
lfsr_out_reg[27]/CK (DFFSXLTS)            0.00       0.00 r
lfsr_out_reg[27]/QN (DFFSXLTS)            1.46       1.46 r
lfsr_out[27] (out)                        0.00       1.46 r
data arrival time                                    1.46

clock clk (rise edge)                    12.00      12.00
clock network delay (ideal)               0.00      12.00
output external delay                    -3.00       9.00
data required time                                   9.00
-----------------------------------------------------------
data required time                                   9.00
data arrival time                                   -1.46
-----------------------------------------------------------
slack (MET)                                          7.54
```

Delay Path Calculation

Actual Required time
With clock
uncertainity/slew
& set_output_delay

MAKE SURE ITS MET!

WAYS TO STUDY

- If you don't understand what a command is doing…
- Go into design compiler by dc_shell
- And type "man COMMAND"
  - Ex) man set_input_delay