NATIONAL INSTITUTE OF TECHNOLOGY PATNA

Department of Electronics and Communication Engineering

MID-SEMESTER EXAMINATION

B.Tech.: Semester-I

Course Name: Digital Design

Course Code: EC14102

Maximum Time: 2 hours Max. Marks: 30

Instruction:

1. Attempt all questions.

2. Assume any suitable data, if necessary.

3. The Marks, CO (Course Outcome), and BL (Bloom's Level) related to questions are mentioned on the right-hand side margin.

Convert the following numbers with the indicated bases to the other indicated base $(101011000.11)_2 \rightarrow (1)_{16}$

Marks CO BL
5 CO1 U

b) (ECE)₁₆→()₈

 $(4021.2)_5 \rightarrow ()_{10}$

d) $(25)_{10} \rightarrow ()_4$

 $(CAD)_{16} \rightarrow ()_2$

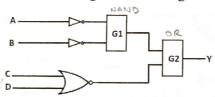
Using Boolean notation, write an expression that is a 1 whenever one of more of its variables (A, B, C, and D) are 1s. A+B+C+D

Simplify the given function $F = \prod m(0, 1, 2, 3, 4, 6, 10, 11, 13)$ to SOP and POS form

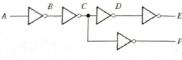
2.5 co₁ U

Determine the gates G1 and G2 in the figure shown to get the output $Y = AB + \overline{C}\overline{D}$

2.5 co1 A



A combination of inverters is shown in Figure 1(a). If the waveform in Figure 1(b) is 2.5 co A applied to point A in Figure 1(a), determine the waveforms at points D.



V_{IN} HIGH LOW

Figure 1(a) Figure 1(b)

What are the limitations of the encoder? Design and explain the 8 × 4 priority

5 CO2 R
encoder with a valid output.

Implement $f(A, B, C) = \sum m(1, 2, 4, 5, 7)$ using 4:1 MUX with A and C as a select 5 Co2 U line.

Derive the logic expression of SUM and CARRY for full adder circuit. Implement the full adder circuit by using half adder and OR gate.