National Institute of Technology Patna

Department of Electronics and Communication Engineering
Digital Design (EC-14102)
Practice Sheet-1

B.Tech. Semester-1, CSE-I & CSE-II | **Session: Jul-Dec 2024**
Unit: I | **Topic: Logic Gates**
Date: 10/09/2024 | **Faculty: Dr. Rajan Agrahari**

PROBLEMS

1. A combination of inverters is shown in Figure 1(a). If a LOW is applied to point A, determine the net output at points E and F. If the waveform in Figure 1(b) is applied to point A in Figure 1(a), determine the waveforms at points B through F.

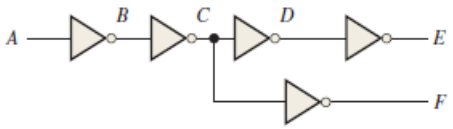


Figure 1(a)

Figure 1(b)

2. The waveforms in Figure 2 are applied to points A and B of a 2-input AND gate followed by an inverter. Draw the output waveform.

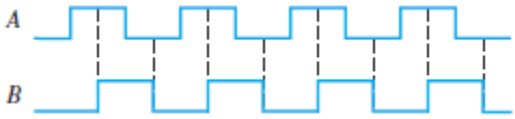


Figure 2

3. The input waveforms applied to a 4-input AND gate are as indicated in Figure 3. The output of the AND gate is fed to an inverter. Draw the net output waveform of this system

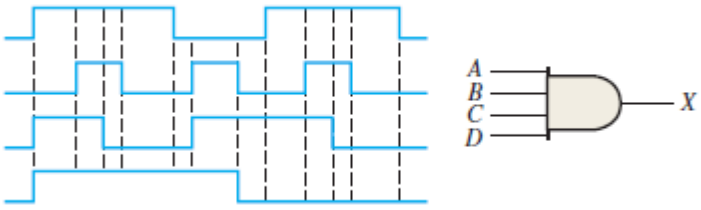


Figure 3

4. Determine the output for a 2-input OR gate when the input waveforms are as in Figure 2 and draw a timing diagram.
5. Repeat Problem 3 for a 4-input OR gate.
6. For the waveform given in Figure 4, following operation has been done:
   (i) A and B are ANDed with output F
   (ii) D and E are ANDed with output G
   (iii) C, F, and G are ORed
   Draw the net output waveform.

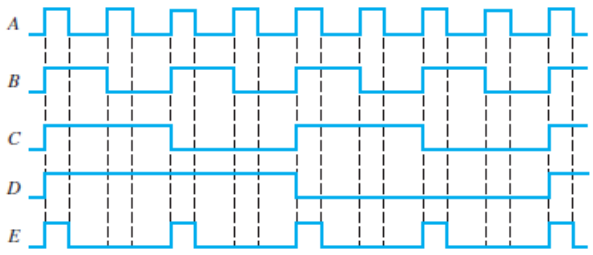


Figure 4

7. For the set of input waveforms in Figure 5, determine the output for the gate shown and draw the timing diagram.

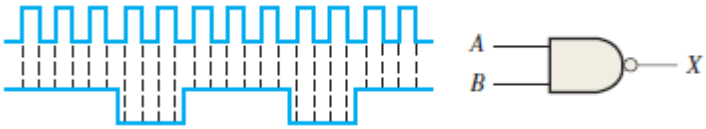


Figure 5

8. Determine the gate output for the input waveforms in Figure 6 and draw the timing diagram.

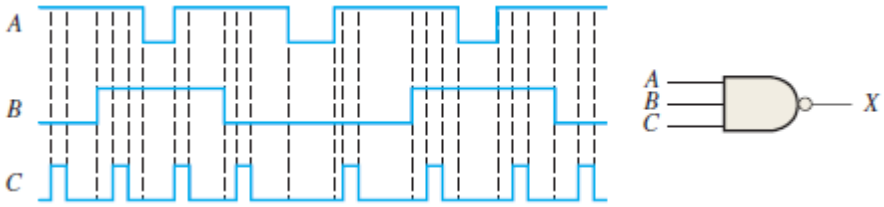


Figure 6

9. Repeat Problem 7 for 2-input NOR gate.
10. Repeat Problem 8 for 3-input NOR gate.
11. Determine the output waveform in Figure 7 and draw the timing diagram:

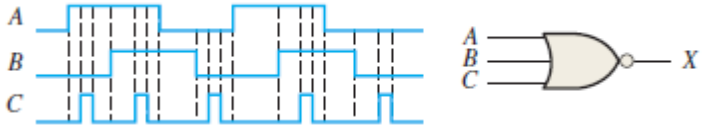
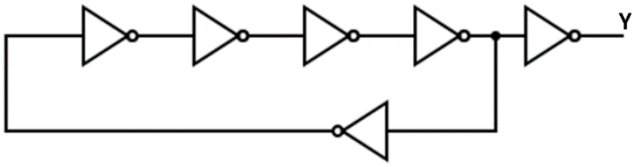
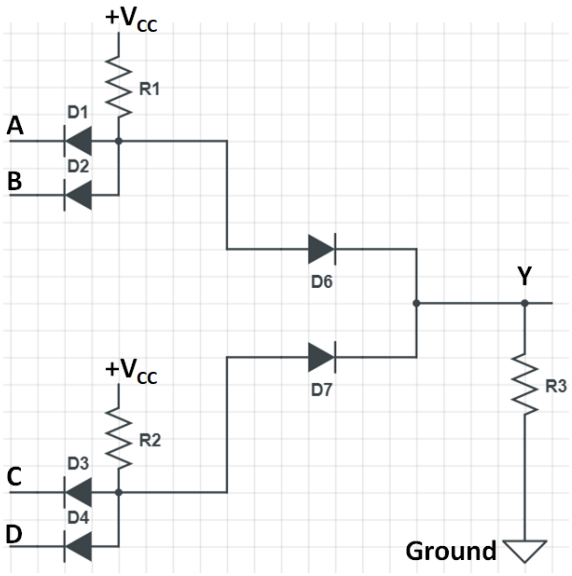


Figure 7

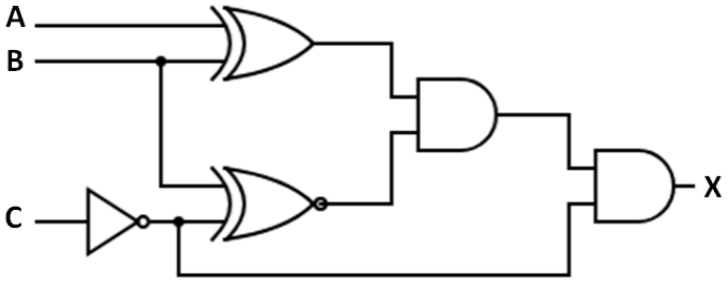
12. Repeat Problem 7 for an exclusive-OR gate.
13. Repeat Problem 7 for an exclusive-NOR gate.
14. Determine the output of an exclusive-NOR gate for the inputs shown in Figure 2 and draw a timing diagram
15. In the given circuit, the propagation delay of each inverter is 100 ps. Evaluate the time-period of the generated square waveform at Y.



16. In the circuit shown below, the diode has a negligible voltage across it under forward bias. If Vcc is +5 V, A, B, C, and D are digital signals with 0V as logic 0 and Vcc as logic 1. What will be the Boolean expression for Y ?



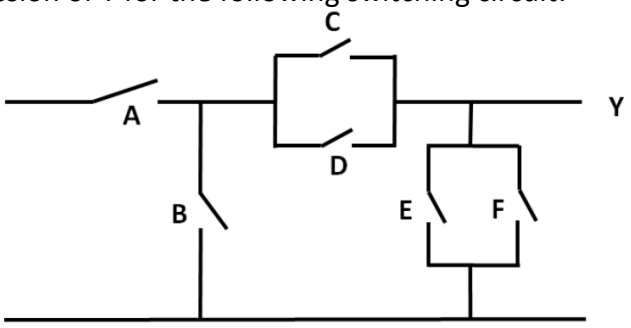
17. If X = 1 in the logic equation [X + Z {Y' + (Z' + XY')}].{X' + Z (X + Y)} = 1, then find Y and Z.
18. Calculate the number of minterms present in canonical SOP expression A + B'C.
19. For the logic circuit shown in the figure, find the input condition (A, B, C) to make the output (X) = 1



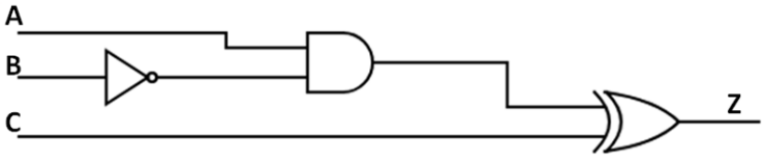
20. Evaluate the minimum number of NAND gate required to implement AB'+ABC'+ABC.
21. Simplify the Boolean expression (A + B)(A + B') + (A'B' + A')'.
22. The K-map for a Boolean function is shown in the figure. Calculate the number of essential prime implicant for this function.

	00	01	10	11
00	1	1	0	1
01	0	0	0	1
10	1	0	0	1
11	1	0	0	1

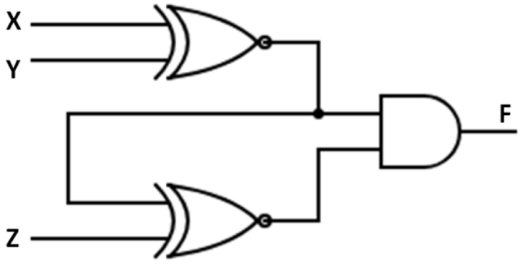
23. Find the logic expression of Y for the following switching circuit.



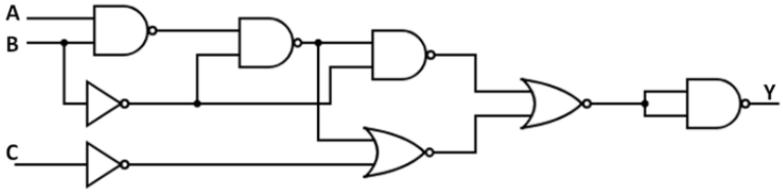
24. All the logic gates shown in the figure have a propagation delay of 40 ns. Let A = C = 0 and B = 1 until time t = 0. At t = 0, all the inputs flip (i.e., A = C = 1 and B = 0) and remain in that state. For t>0, Calculate the duration for output Z = 1.



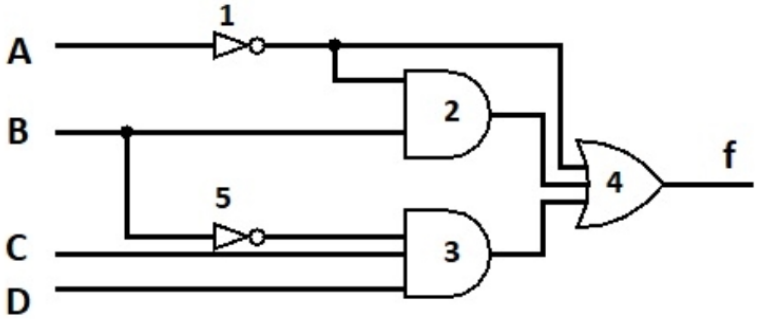
25. A function of Boolean variables X, Y, and Z is expressed in terms of the min-terms as $\boldsymbol{F}$ ($\boldsymbol{X}$, $\boldsymbol{Y}$, $\boldsymbol{Z}$) = $\boldsymbol{\Sigma}$ (, $\boldsymbol{2}$, $\boldsymbol{4}$, $\boldsymbol{6}$). Find the Boolean expression of the product of sums which is equal to the function $\boldsymbol{F}$ ($\boldsymbol{X}$, $\boldsymbol{Y}$, $\boldsymbol{Z}$).
26. What will be the output F in the digital circuit shown in the figure?



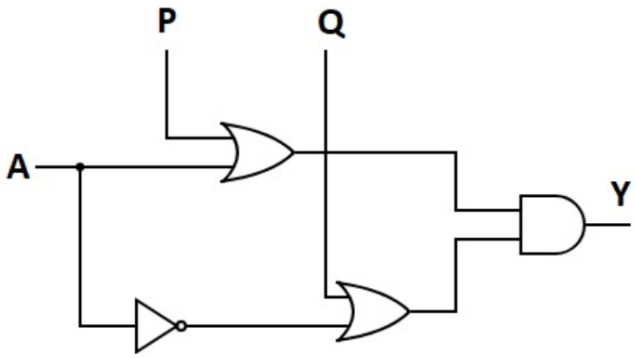
27. For the logic circuit shown in the figure, evaluate the simplified Boolean expression for the output Y.



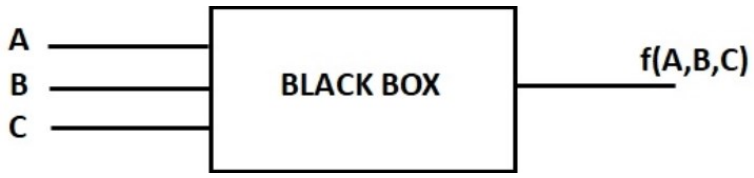
28. In a 4-variable Karnaugh map, a 2-variable product term is produced by _____ cell group of 1's.
29. Convert decimal 62 in Hexadecimal and BCD number system.
30. A new Binary Coded Hexa (BCH) number system is proposed in which every digit of a base-6 number is represented by its corresponding 3-bit binary code. For example, the base-6 number 35 will be represented by its BCH code 011101. In this numbering system, Find the corresponds decimal number for the BCH code 101011100010.
31. Simplify sum of products expression for the Boolean function F = m0 + m2 + m3 + m5 + m7; m0, m2, m3, m5, and m7 are minterms corresponding to the inputs A, B, and C with A as the MSB and C as the LSB.
32. Consider the logic circuit with their gate number. Find the redundant gate.



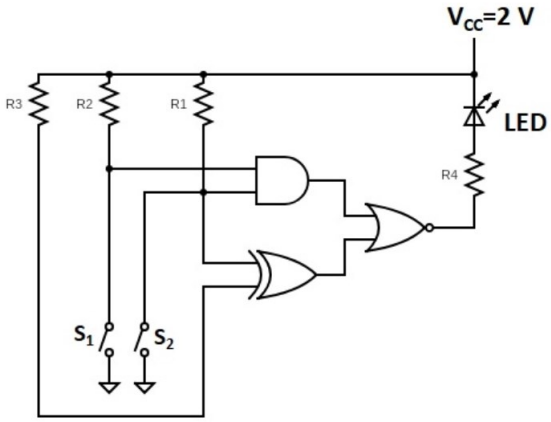
33. What will be the value of P and Q for the output Y=A' + B of the circuit shown



34. The black box in the figure shown below consists of a minimum complexity circuit that uses only AND, OR, and NOT gates. The function f(A,B,C) = 1 whenever A and C are different and 0 otherwise. What will be the Boolean expression for the minimum complexity circuit?



35. In the figure, assume negligible voltage drop across the LED diode, 0 V for logic 0 and +5V for logic 1. Find the position of the switch S1 and S2 (i.e., open or close) to emit the light from LED.



36. A Boolean function of three variables A, B, and C is defined as follows:
f(0,0,1)=f(0,1,1)=f(1,1,0)=f(1,1,1)=1;
f(0,0,0)=f(0,1,0)=f(1,0,0)=f(1,0,1)=0;
Assuming complements of A, B, and C are not available. What will be the total minimum cost for realizing f using only 2-input NOR gates, 2-input AND gates, and 2-input OR gates (each having unit cost).
37. What is the minimized logic expression in SOP corresponding to the following POS Boolean function f(A,B,C,D)=$\prod(\mathbf{0},\mathbf{1},\mathbf{2},\mathbf{6},\mathbf{8},\mathbf{10},\mathbf{11},\mathbf{12})$.