National Institute of Technology Patna

Department of Electronics and Communication Engineering
Digital Design (EC-14102)
Practice Sheet- 4

B.Tech.: Semester-I CSE- I/II | **Session: Jul-Dec 2024**
Unit: II | **Topic: Combinational Circuits**
Date: 22/10/2024 | **Faculty: Dr. Rajan Agrahari**

Objective Questions

1. A half-adder is characterized by
   (a) two inputs and two outputs (b) three inputs and two outputs
   (c) two inputs and three outputs (d) two inputs and one output

2. A full-adder is characterized by
   (a) two inputs and two outputs (b) three inputs and two outputs
   (c) two inputs and three outputs (d) two inputs and one output

3. The inputs to a full adder are A = 1, B = 0, Cin = 1. The outputs are
   (a) $\sum = 0$, C_{out} = 1 (b) $\sum = 1$, C_{out} = 0
   (c) $\sum = 0$, C_{out} = 0 (d) $\sum = 1$, C_{out} = 1

4. A 3-bit parallel adder can add
   (a) three 2-bit binary numbers (b) two 3-bit binary numbers
   (c) three bits at a time (d) three bits in sequence

5. To expand a 2-bit parallel adder to a 4-bit parallel adder, you must
   (a) use two 2-bit adders with no interconnections
   (b) use two 2-bit adders and connect the sum outputs of one to the bit inputs of the other
   (c) use four 2-bit adders with no interconnections
   (d) use two 2-bit adders with the carry output of one connected to the carry input of the other

6. If a 74HC85 magnitude comparator has A = 1000 and B = 1010, the outputs are
   (a) A > B = 0, A < B = 0, A = B = 0 (b) A > B = 0, A < B = 0, A = B = 1
   (c) A > B = 0, A < B = 1, A = B = 0 (d) A > B = 0, A < B = 1, A = B = 1

7. If a 1-of-16 decoder with active-LOW outputs exhibits a LOW on the decimal 12 output, what are the inputs?
   (a) $A_3A_2A_1A_0$ = 1010 (b) $A_3A_2A_1A_0$ = 1110
   (c) $A_3A_2A_1A_0$ = 1100 (d) $A_3A_2A_1A_0$ = 0100

8. A BCD-to-7 segment decoder has 0100 on its inputs. The active outputs are
   (a) a, c, f, g (b) b, c, f, g
   (c) b, c, e, f (d) b, d, e, g

9. If an octal-to-binary priority encoder has its 0, 2, 5, and 6 inputs at the active level, the active-HIGH binary output is
   (a) 110 (b) 010
   (c) 101 (d) 000

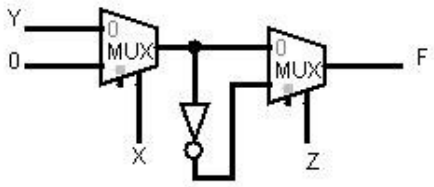
10. In general, a multiplexer has
    (a) one data input, several data outputs, and selection inputs
    (b) one data input, one data output, and one selection input
    (c) several data inputs, several data outputs, and selection inputs
    (d) several data inputs, one data output, and selection inputs

11. Data distributors are basically the same as
    (a) decoders (b) demultiplexers
    (c) multiplexers (d) encoders

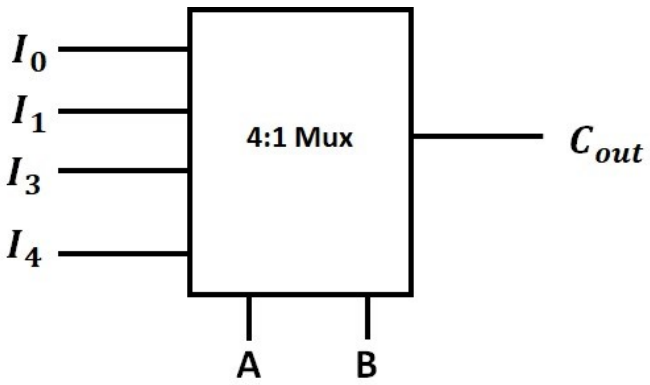
12. Which of the following codes exhibit even parity?
    (a) 10011000 (b) 01111000
    (c) 11111111 (d) 11010101
    (e) all (f) both answers (b) and (c)

Problems

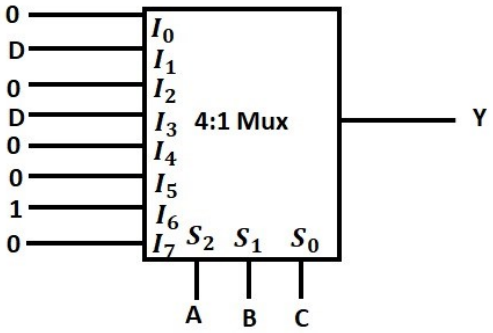
1. Find the Boolean expression F implemented by the circuit shown in figure



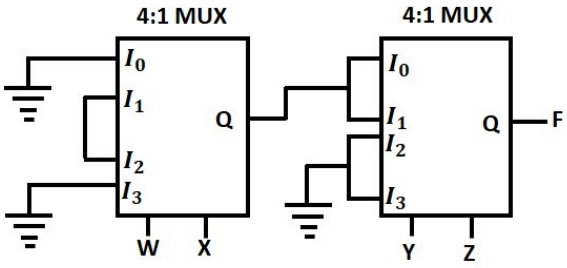
2. A 4:1 multiplexer is to be used for generating the output carry of a full adder. A and B are the bits to be added while C_{in} is the input carry and C_{out} is the output carry. A and B are to be used as the select bits with A being the most significant select bit. What will be the values of the inputs I_0, I_1, I_2, and I_3 so that the output will be C_{out}.



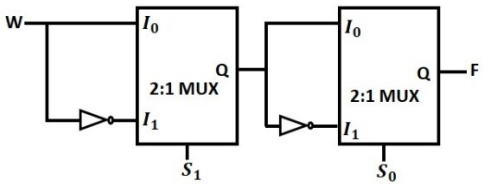
3. What is the output of the following circuit?



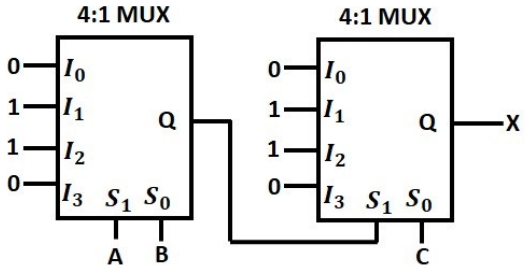
4. Implement a half subtractor by using 2:1 MUX.
5. Determine the output of the following combinational circuit, where W and Y are the MSBs of the control inputs.



6. Find the Boolean function of F in the given circuit.



7. Derive the logic expressions of Borrow (M) and Difference (N = X-Y) for the half subtractor circuit.
8. Design 2-bit magnitude comparator with logic diagram and truth table.
9. What are the limitations of the encoder? Design and explain the 8×4 priority encoder with a valid output.
10. Implement $F(A, B, C, D) = \sum m(2,3,5,7,8,9,12)$ by using 4×1 multiplexer and {A,B} as a select line.
11. Implement $P(XOR)Q$ with 4:1 multiplexer.
12. Design 2-input AND gate and 2-input Ex-OR gate by using 2:1 Multiplexer.
13. Determine the logic expression for X in the following circuit



14. Realize 4:1 multiplexer by using 2:1 multiplexer.