

ECE 592 (091)

Resonant Power Converters

Zeljko Pantic, Associate Professor

Department of Electrical and Computer Engineering
North Carolina State University, Raleigh, NC

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Introductory lecture

Syllabus overview

Topic 1

Introduction to Resonant Power Conversion

Introduction to Resonant Power Conversion

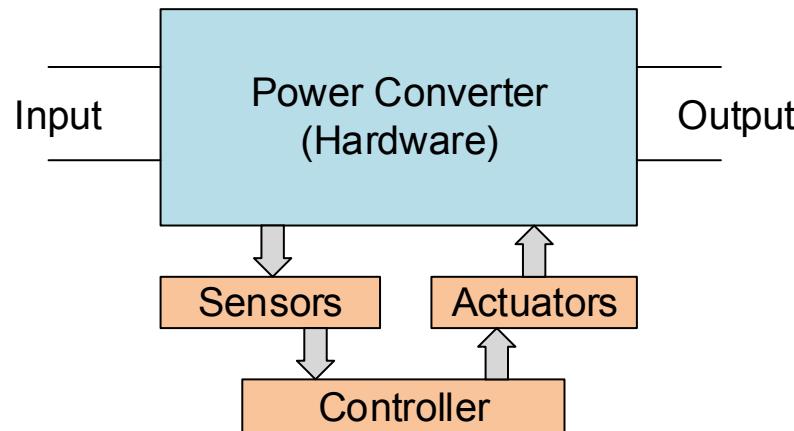
- Electric energy generation, transmission, processing, and storage are some of the dominant challenges of the modern world.
- Electric Power Converters receive **electric power** from an input and transform it into a different form of **electric power** at the output in a **controllable manner**.
- Based on the type of the input and output powers, four types of converters can be identified: Inverters, Rectifiers, DC-DC converters, and Matrix converters.
- **Resonant Inverters, Rectifiers, and DC-DC converters** will be studied in this course

Input power	Type of transformation	Type of device	Output power
DC	DC-DC conversion	DC-DC converter	DC
DC	Inversion	Inverter	AC
AC	Rectification	Rectifier	DC
AC	AC-AC conversion	Cycloconverter, Matrix converter	AC

Introduction to Resonant Power Conversion

Autonomous operation and control

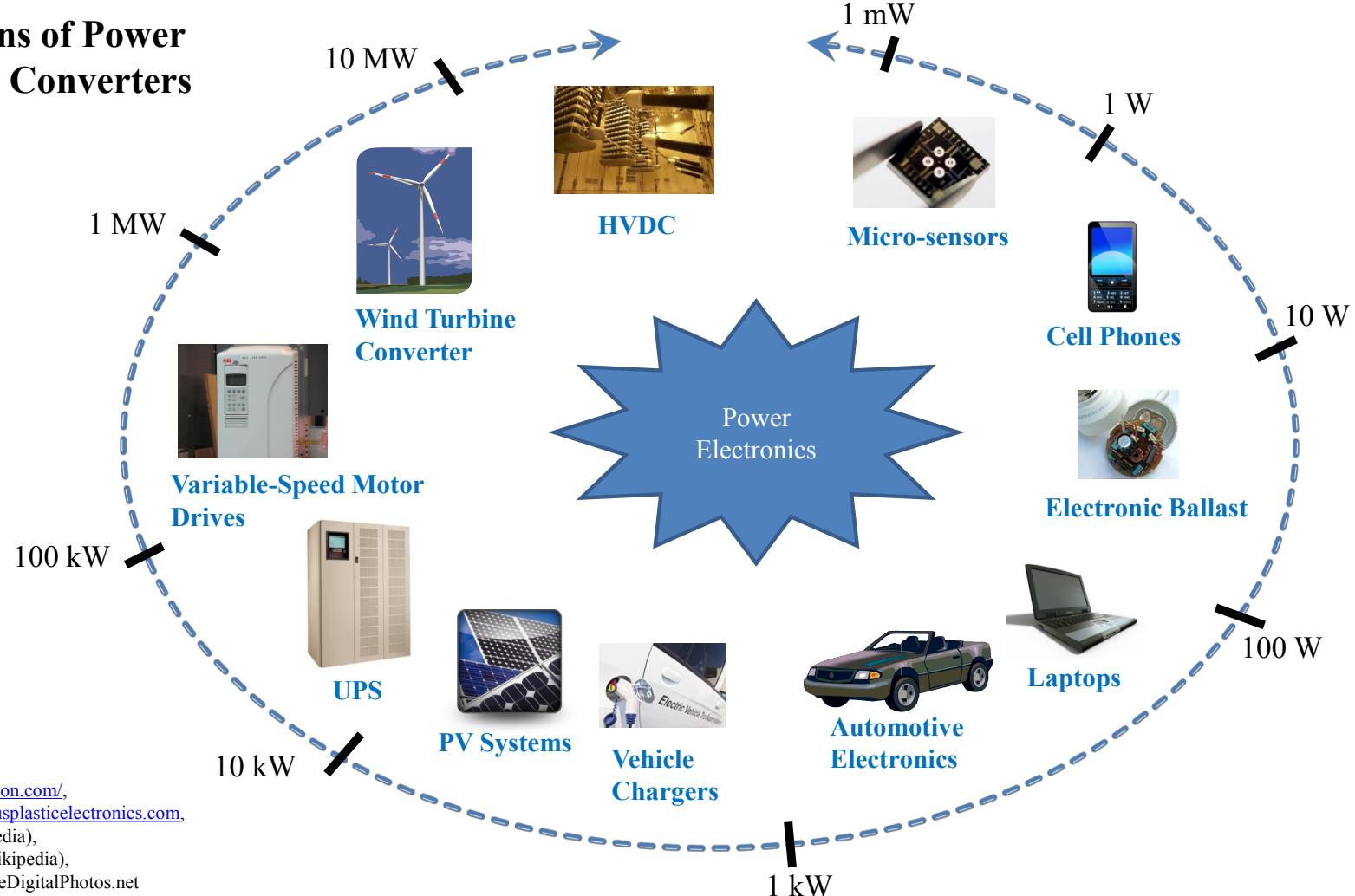
- Modern power converters are autonomous systems.
- Autonomous system: a system capable of identifying, measuring, understanding, and responding to unanticipated events during operation without human intervention.
- Three critical elements of an autonomous system are sensing, control, and actuation.



- Typical sensing devices: voltage, current, temperature sensors, ...
- Typical actuation devices: (gate) drivers for semiconductor devices and relays

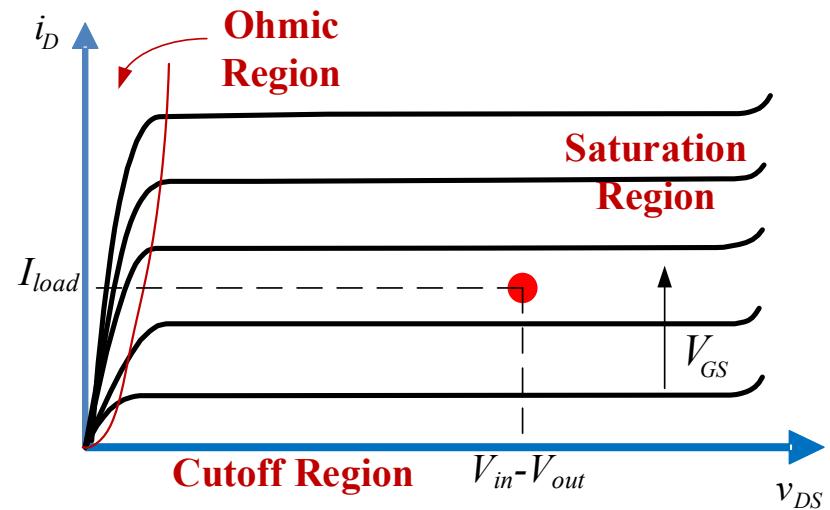
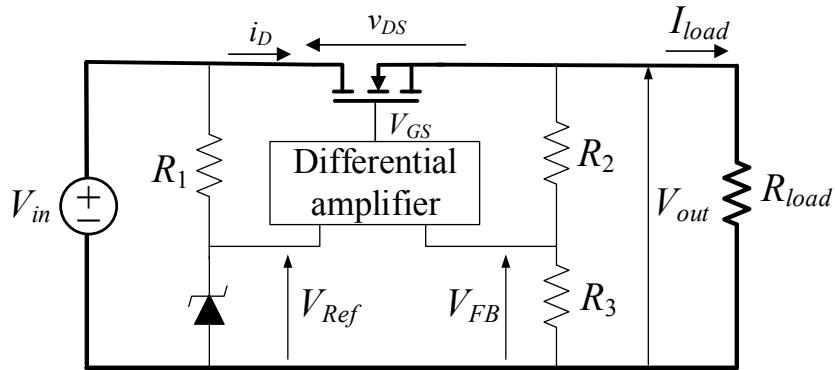
Introduction to Resonant Power Conversion

Applications of Power Electronics Converters



Introduction to Resonant Power Conversion

Series linear voltage regulator



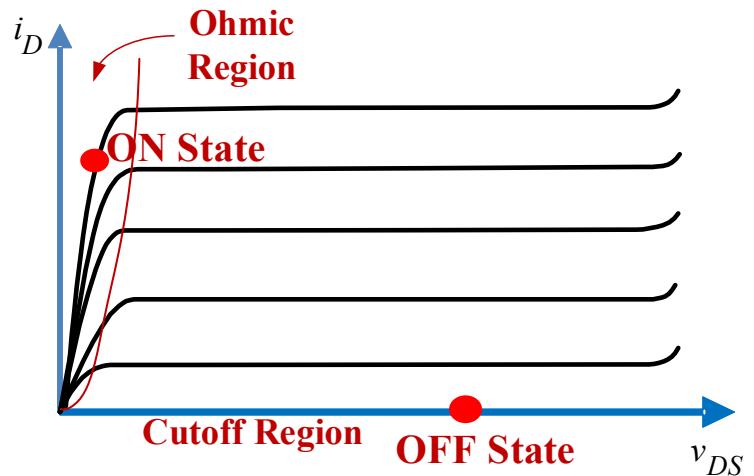
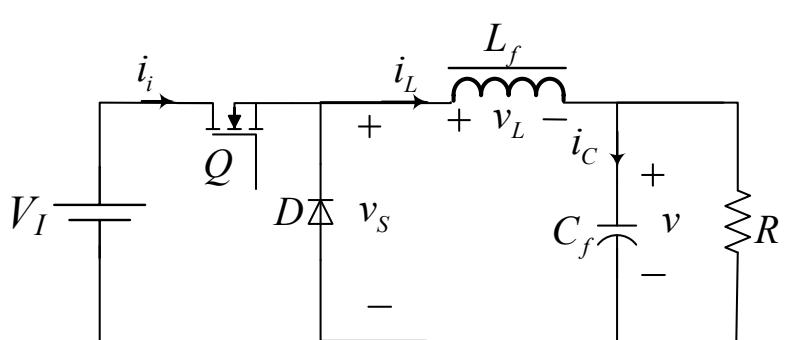
- A linear regulator employs an active switch (BJT or MOSFET)
- Active switch is connected in series or as a shunt
- The output voltage is compared with the reference voltage, and the error signal is processed through an amplifier to adjust the switch control signal

$$P_{loss} = I_{load} (V_{in} - V_{out})$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}}{V_{in}}$$

Introduction to Resonant Power Conversion

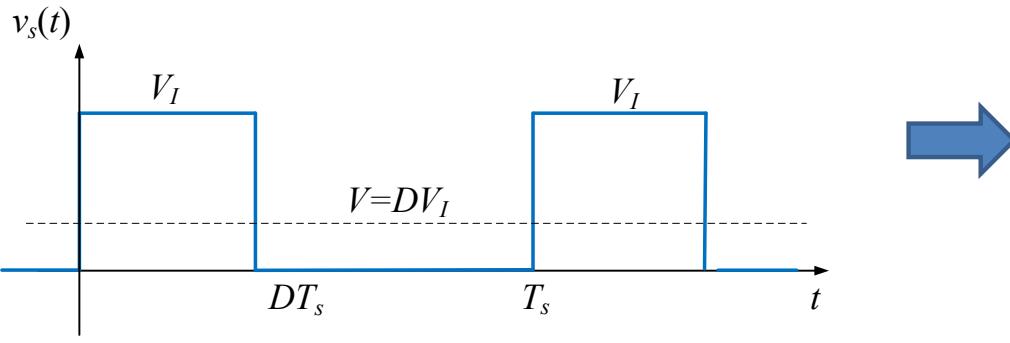
Switch-mode DC-DC converter (e.g. a buck converter)



- Active switch is ON for the period $0-DT_s$ and OFF during DT_s-T_s
- D is duty ratio (duty cycle) $D=t_{on}/T_s$
- By varying D , the output voltage can be controlled $V=DV_I$
- During each period T_s , the operating point moves from Cutoff to Ohmic Region and vice versa.

Introduction to Resonant Power Conversion

Switch-mode DC-DC converter (e.g. a buck converter)

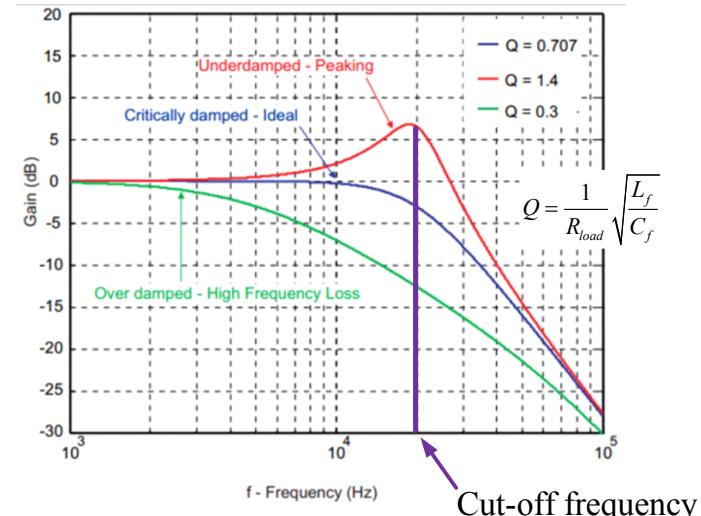
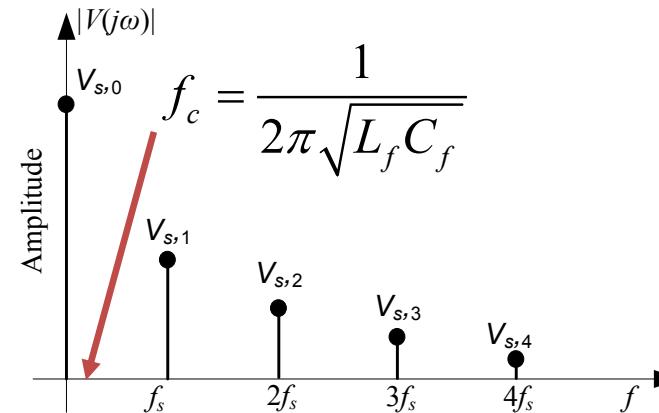


- DC loads cannot operate when supplied with a pulsating voltage. A filter circuit must be inserted between $v_s(t)$ and $v(t)$ to eliminate harmonics. C, L, or LC filters are commonly used.

- Cut-off frequency f_c and characteristic impedance Z_c determines the filter's transfer function

$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}} \quad Z_c = \sqrt{\frac{L_f}{C_f}}$$

- The optimum position of f_c is between $(0.05-0.2)f_s$
- Lower f_c provides better filtering but **requires larger components** and makes the converter slower.



Introduction to Resonant Power Conversion

Mass, Volume, and Cost of a converter are primarily determined by the size of its reactive elements

- The intrinsic converter cost is highly correlated with its mass
- More power integration leads to cost reduction on raw materials
- Heatsinks and magnetic devices determine the weight, while heatsinks and capacitors determine the volume
- Converter integration is allowed by applying higher switching frequency or by using advanced methods, such as 3D interconnection, the power dies embedded in the PCB, etc.
- Size reduction (power density increase) must be followed by improving efficiency since a highly integrated converter is more difficult to cool.
- The efficiency can be improved by using more efficient switching devices (Wide-bandgap devices: SiC, GaN, ...) or by improving the converter topology.

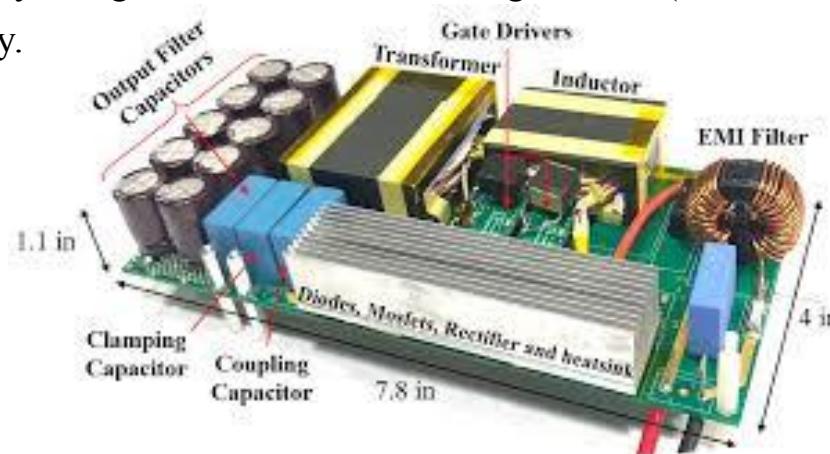
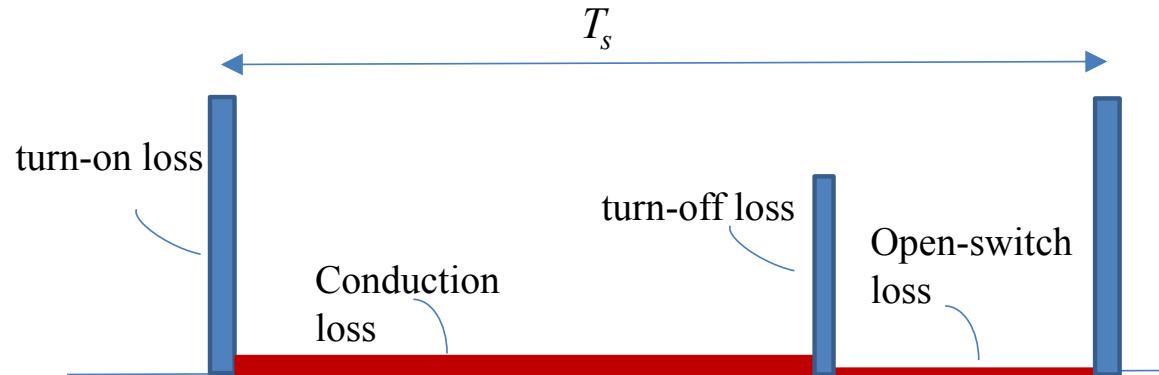


Photo source IEEE (D. Wu, R. Ayyanar, M. Sondharangalla, and T. Meyers, "High-Performance Active-Clamped Isolated SEPIC PFC Converter With SiC Devices and Lossless Diode Clamp")

Introduction to Resonant Power Conversion

Time diagram of the switch instantaneous power loss:



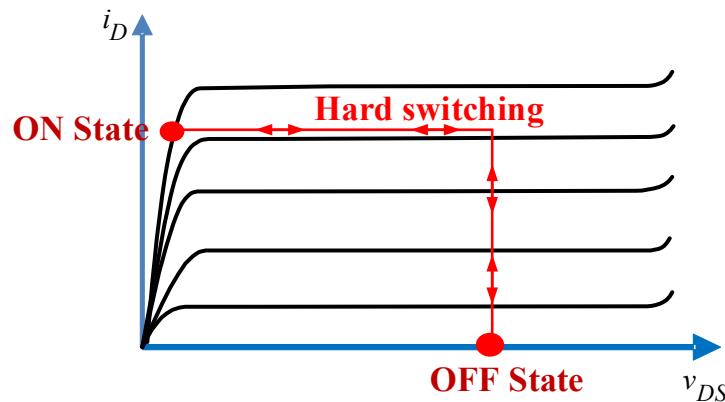
Switch instantaneous power loss $p(t)$:

$$p(t) = v_{sw}(t)i_{sw}(t)$$

$$W_{tot} = \int_o^{T_s} p(t) dt \approx W_{cond} + W_{sw}$$

$$P_{avg} = \frac{1}{T_s} \int_o^{T_s} p(t) dt = \frac{W_{tot}}{T_s} = W_{tot} f_s$$

Conduction loss P_{cond} and switching loss P_{sw} occurs in the switches.

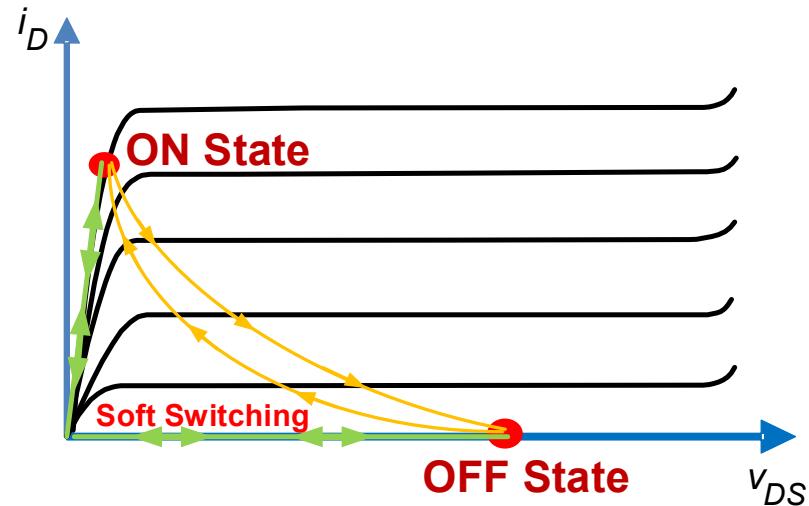
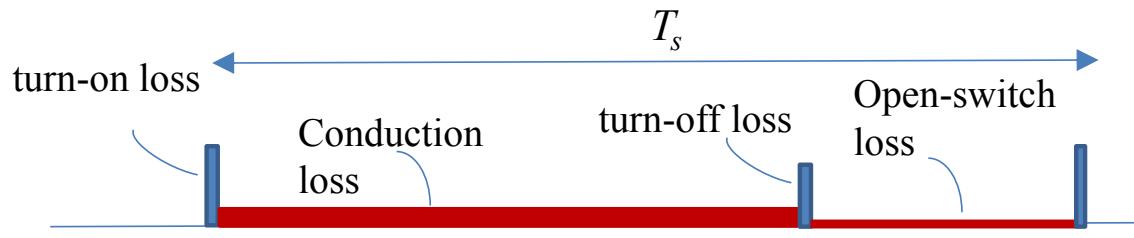


$$W_{cond} \text{ proportional to } DT_s \Rightarrow P_{cond} = W_{cond} f_s = const$$
$$W_{sw} = const \Rightarrow P_{sw} = W_{sw} f_s \text{ proportional to } f_s$$

Transition through the active (saturation) region causes excessive switching loss!

Introduction to Resonant Power Conversion

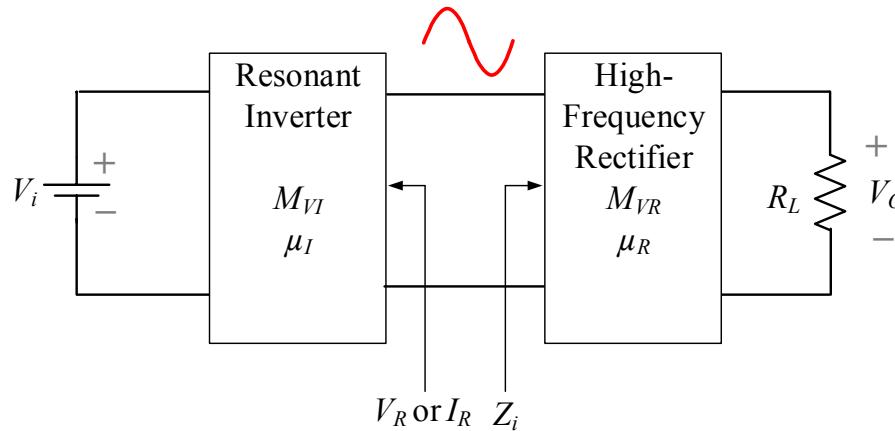
- By improving switch characteristics and by designing new gate drivers, it is possible to reduce the switching losses. However, the primary need is to eliminate hard-switching!



- **PWM rectangular voltage and current** waveforms cause turn-on and turn-off losses that limit the operating frequency. With rectangular voltage and currents through the switch, it is impossible to avoid hard-switching!
- Voltage or current must have an **alternating waveform** in order to create soft-switching. Sinusoidal voltage and current waveforms are easy to create with the help of a resonant circuit with a sufficiently high quality factor. That is how RESONANT CONVERTERS are born!
- There are two soft-switching operation modes: **zero-voltage switching (ZVS)** or **zero-current switching (ZCS)**
- Soft-switching improves efficiency and reduces **the potential for electromagnetic interference (EMI)** since the signals have less harmonics.

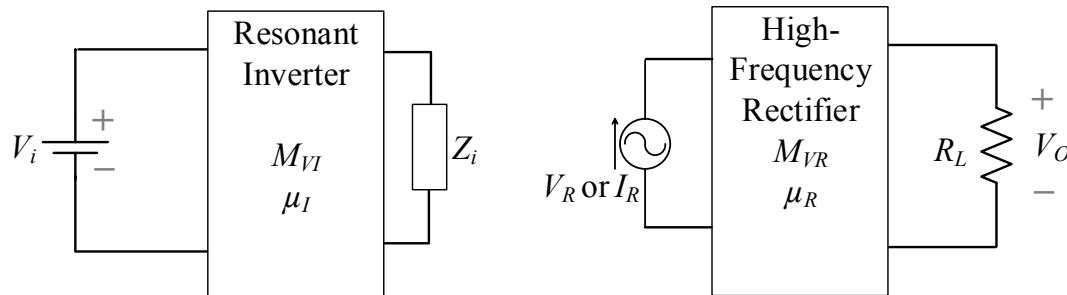
Introduction to Resonant Power Conversion

- A resonant DC-DC converter consists of a **cascaded** connection of a resonant inverter and a high-frequency rectifier that should be compatible with each other.



- Z_i – input impedance of the rectifier
- V_R or I_R – output voltage or current of the inverter

- The analysis of a cascaded DC-DC converter can be divided into independent analyses of a Resonant Inverter and a High-Frequency Rectifier. Z_i and V_R (or I_R) are used to “close” the open terminals of the inverter and the rectifier, respectively.



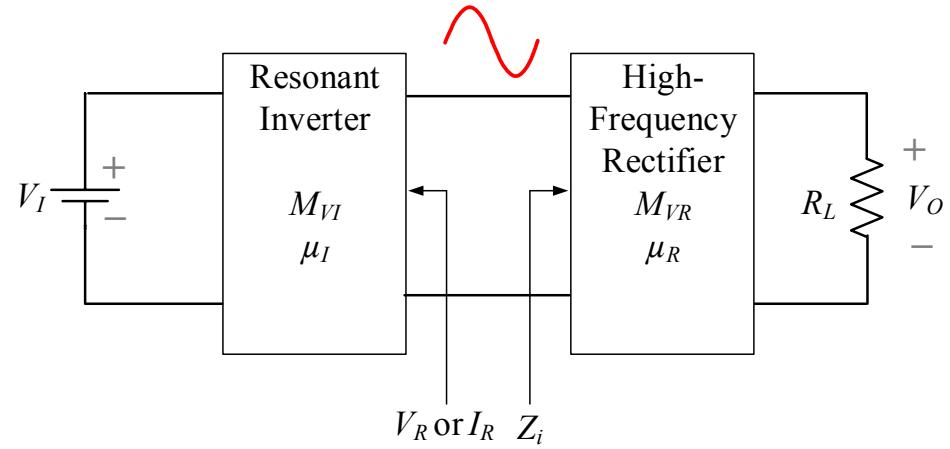
- Z_i is resistive if Class D rectifiers are used, and it includes both resistance and reactance in the case of Class E rectifiers

Introduction to Resonant Power Conversion

- Two parameters are relevant for a DC-DC converter
 - Voltage transfer function $M_V = V_O/V_I$
 - Converter efficiency $\eta = P_O/P_I$
- M_V and η for a DC-DC converter can be calculated as the products of voltage transfer functions and efficiencies of the Resonant Inverter and the High-Frequency Rectifier independently:

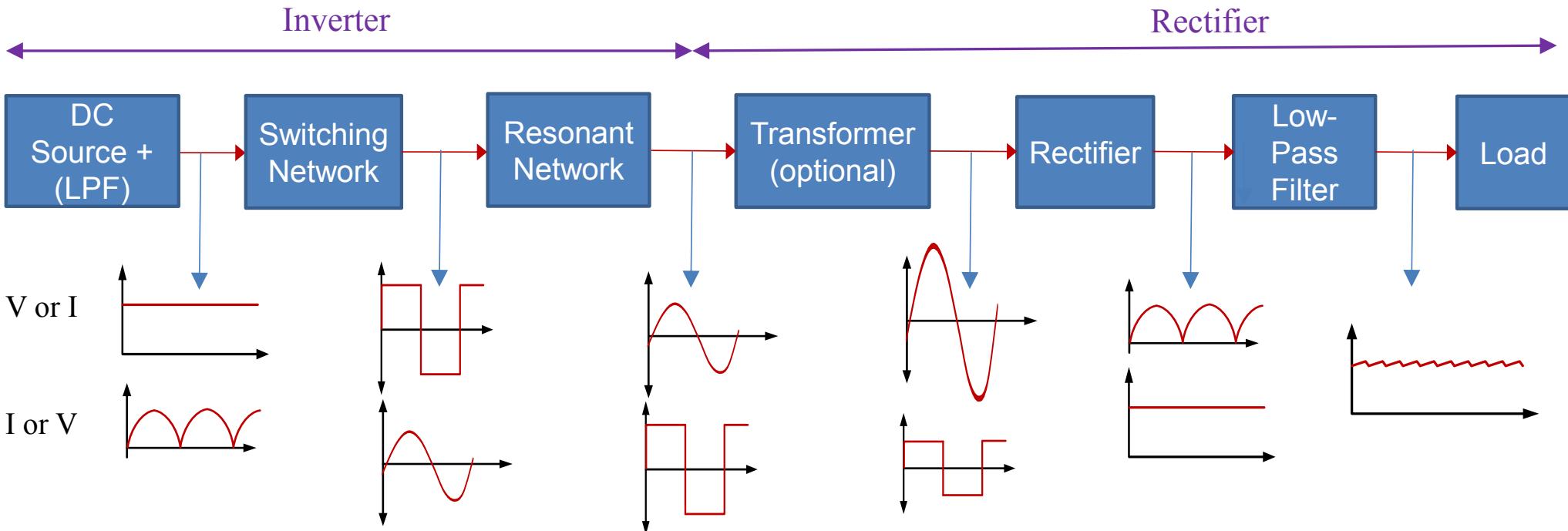
$$M_V = \frac{V_O}{V_I} = \frac{V_O}{V_R} \frac{V_R}{V_I} = M_{VI} M_{VR}$$

$$\eta_V = \frac{P_O}{P_I} = \frac{P_O}{P_R} \frac{P_R}{P_I} = \eta_{VI} \eta_{VR}$$



Introduction to Resonant Power Conversion

- There are two main categories of Resonant Power Converters: **Class D and Class E converters**, and many of their derivatives, Class DE, Class EF_n, Class E/F_n, Class Φ2, etc.
- The general structure of a Class D resonant converter (**cascaded** connection of an **Inverter** and a **Rectifier**):

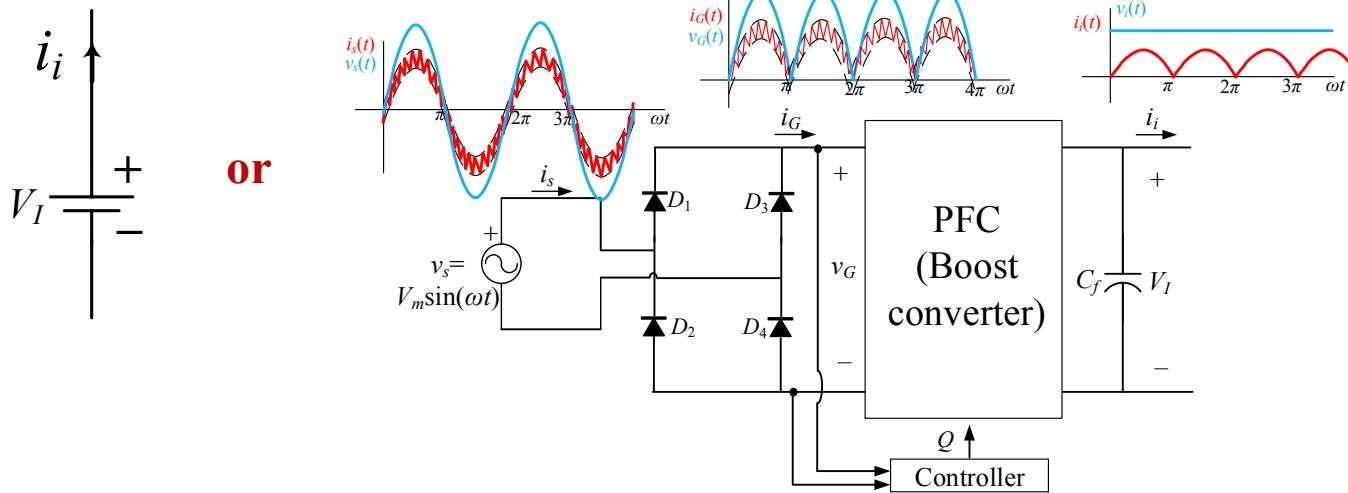


- Let us make an overview of individual blocks.

Introduction to Resonant Power Conversion

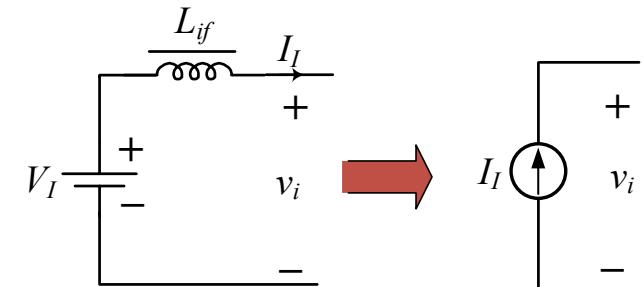
- The DC source can be a **Voltage Source** or a **Current Source**.
- The voltage source can be a Battery (electrochemical energy source) or a voltage obtained by rectifying an AC (grid) voltage. Passive filters or PFC converters are often used to improve the grid power factor and reduce THD.
- There is no battery equivalent that generates a constant current. Therefore, a current source is obtained by connecting a large inductor (choke) in series with a voltage source.

DC Voltage Source



or

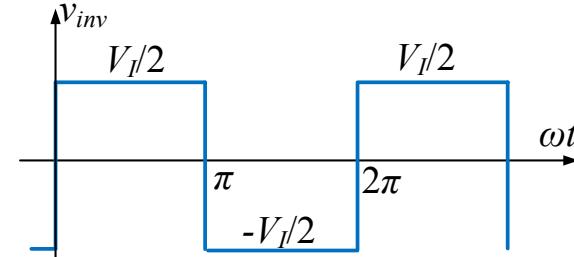
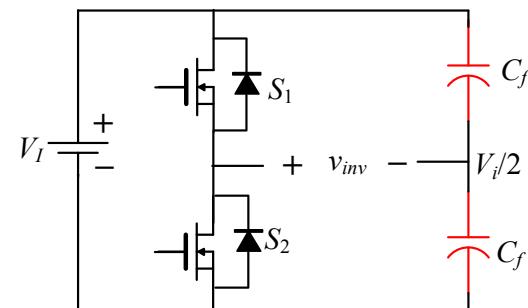
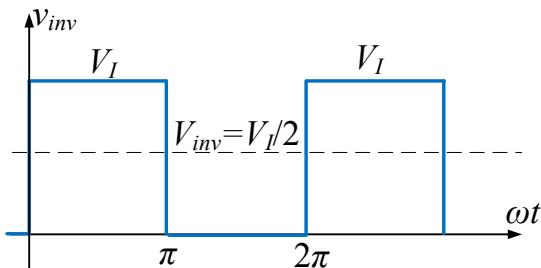
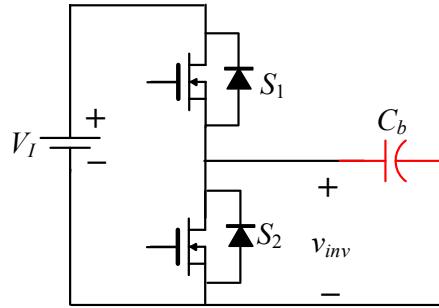
DC Current Source



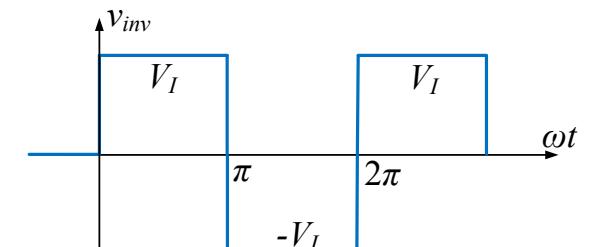
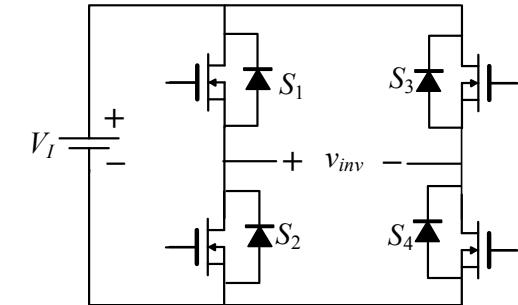
Introduction to Resonant Power Conversion

- Two types of switching networks are used in Class D converters: Half- and Full-Bridge topologies.
- Half-Bridge topology utilizes two switches. The output voltage produces a unipolar voltage with a DC component. To block the voltage DC component, a blocking capacitor should be used.
- DC voltage in half-bridge topologies can also be eliminated by using two filtering capacitors arranged in an auxiliary branch.
- Full-bridge topology utilizes four switches arranged in two branches. In ideal case, it generates symmetrical alternating voltage with a zero DC value.

Half-Bridge Network

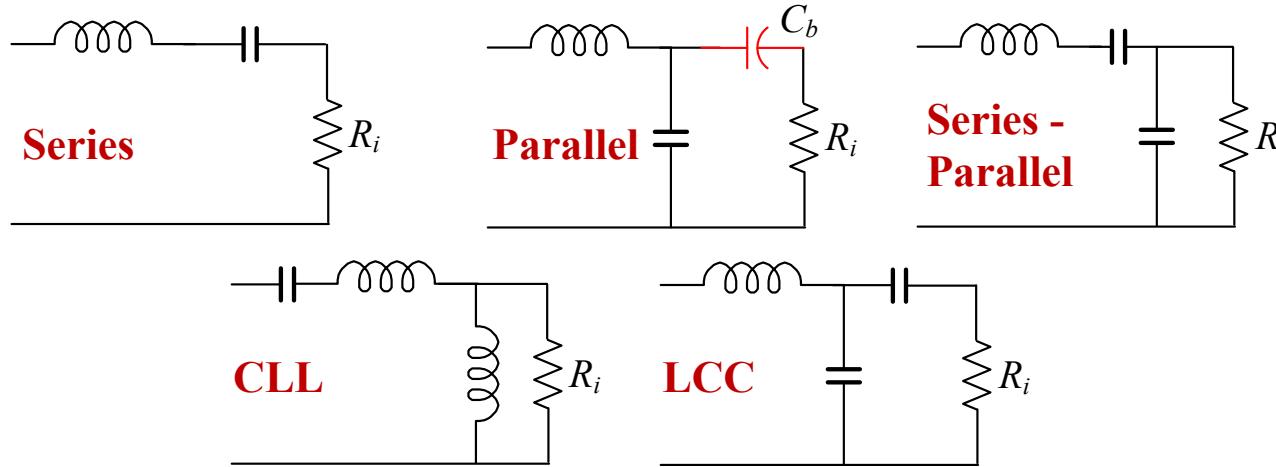


Full-Bridge Network



Introduction to Resonant Power Conversion

- Various Resonant Network are employed to achieve different goals and some of them are shown below:

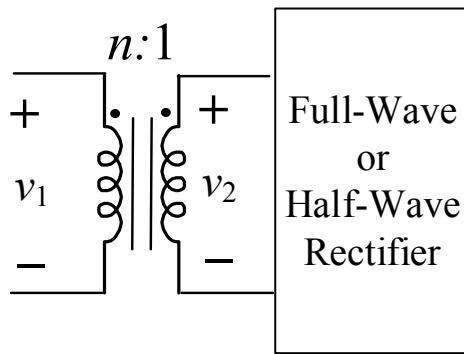


- It is important to differentiate whether the resonant network supplies a sinusoidal current to the load R_i (acts as a current source) or supplies sinusoidal voltage to the load (acts as a voltage source).
 - If R_i establishes a direct series connection with a reactive element – the resonant network acts as a current source
 - If R_i establishes a direct parallel connection with a reactive element – the resonant network acts as a voltage source
- The type of the rectifier depends on the type of the resonant network:
 - A resonant network operating as a current source must be followed by a current-driven rectifier.
 - A resonant network operating as a voltage source must be followed by a voltage-driven rectifier.

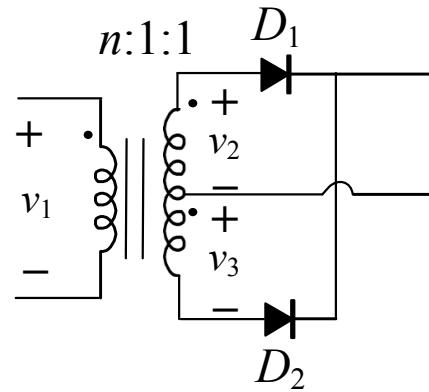
Introduction to Resonant Power Conversion

- Two types of transformers are utilized in resonant power converters:
 - Transformer with a single output
 - Dual-output center-tapped transformer

Single-output transformer



Transformer with center-tapped secondary

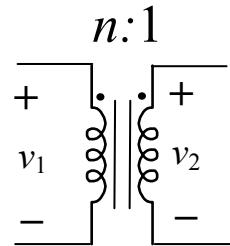


- The role of the transformer is to provide circuit isolation and impedance scaling.
- Center-tapped transformer allows for only two rectifier diodes to be used at the secondary while still providing full-wave rectification.
- Since the diode is often the lossiest element in a resonant converter, eliminating one diode can significantly improve efficiency.

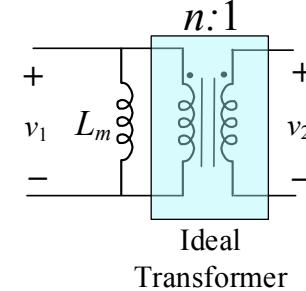
Introduction to Resonant Power Conversion

- Different level of complexity and (accuracy!) in modeling of a transformer

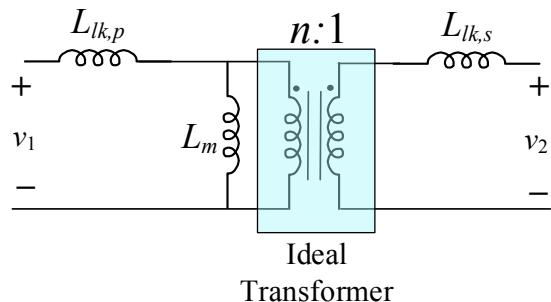
Ideal Transformer



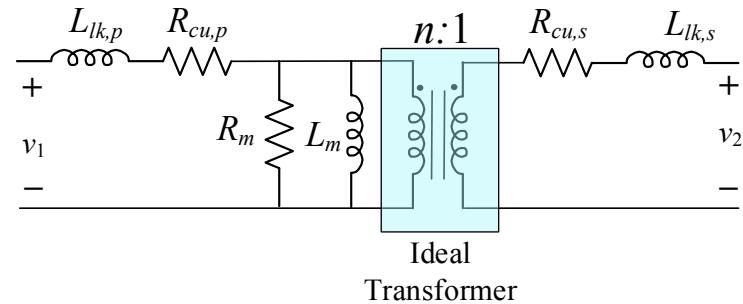
Transformer model with magnetizing inductance



Transformer model with leakage inductances included



Transformer model with losses included



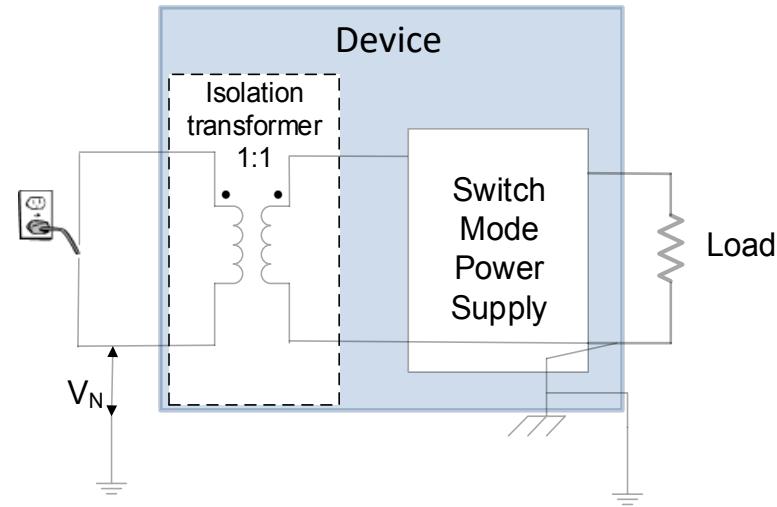
Introduction to Resonant Power Conversion

Benefits of transformer integration in a power converter

1) TRANSFORMER ISOLATION EFFECT

Why the isolation (isolation transformer) is needed:

- **Satisfy safety standards (OSHA, IEC)** Neutral-to-ground voltage can be eliminated. Allow ground and neutral conductor to be re-bond at secondary if necessary
- **Prevents ground loop problem**
- Helps in the **power line signal filtering**
- Prevents **high-frequency converter harmonics** from the converter to propagate back to the grid



2) Allows for an **IMPEDANCE SCALING** by a factor n^2

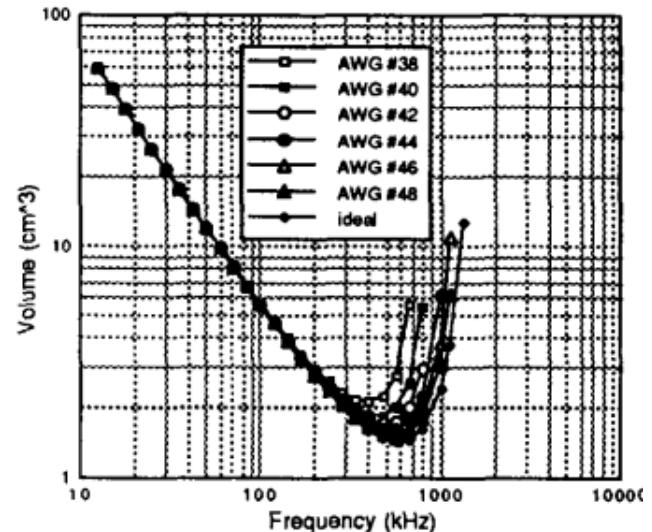
3) Allows **MULTIPLE OUTPUTS** by means of multiple secondary windings and secondary circuits

4) **REDUCES STRESS** on switching elements by adjusting the voltage and current levels

Introduction to Resonant Power Conversion

Benefits of transformer integration in a power converter

- Isolation transformers are bulky (operate at 50-60 Hz).
- The induced voltage is proportional to the signal frequency → It is expected that the volume of the transformers reduces as $1/f_s$
- At very high frequencies, the required volume increases again due to the additional hysteresis and eddy-current losses in the core and eddy and proximity current losses in the windings.
 - High-frequency transformers are much smaller than low-frequency ones while transferring the same power.
 - In resonant converters, transformers operate at tens or hundreds of kHz.
- Very high-frequency transformers use Litz wire instead of a solid wire to reduce winding resistance due to eddy-current and proximity effects



(b) Given Size of Strands, Efficiency = 99.3%, 3F3 EE

Fig.11 Volume at constant efficiency.

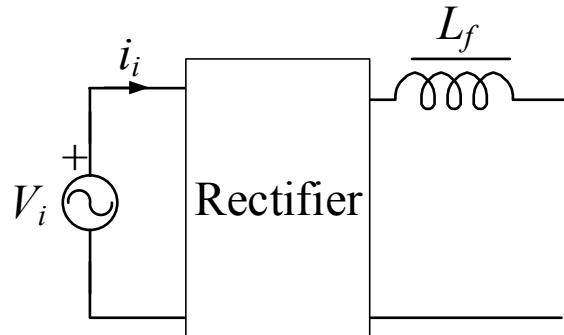
Gu, Liu:
"A Study of Volume and Weight vs. Frequency for High-Frequency Transformers"

Introduction to Resonant Power Conversion

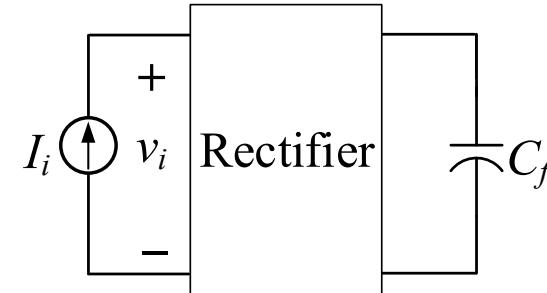
Rectifiers

- Rectifiers can be **voltage- or current-driven rectifiers**. A voltage-driven rectifier has a voltage source at the input, while a current-source rectifier has a current source.
- Rectifier switches must not connect two voltage sources in parallel or two current sources in series. Therefore:
 - Voltage-driven rectifiers have a current source (inductor) connected in series at the output.
 - Current-driven rectifiers have a voltage source (capacitor) connected in parallel at the output.

Voltage-driven rectifier



Current-driven rectifier



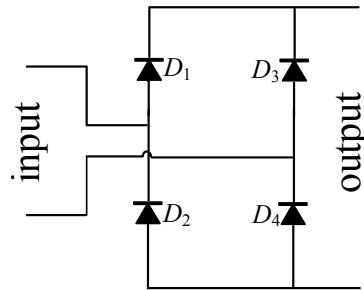
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Rectifiers

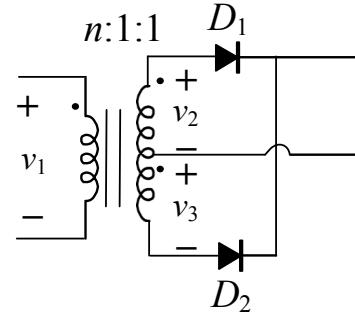
- There are two types of rectifiers: Half-Wave (HW) and Full-Wave (FW) rectifiers:
 - Half-wave rectifiers use only the half cycle of the input signal to supply power to the load.
 - Full-wave rectifiers use both cycles of the input signal to supply the load.
- Full-wave rectifiers can be Full-Bridge (FB) or Center-Tapped (CT) configurations.
- HW and CT rectifiers use only two diodes.
- HW and CT rectifiers have only one diode conducting at a time. CT rectifiers are the most efficient rectifiers since they conduct 50% less current than HW rectifiers.
- The disadvantage of a CT rectifier is that its diodes should block twice the voltage of HW or FB rectifiers.

Full-Wave Rectifiers

Full-Bridge

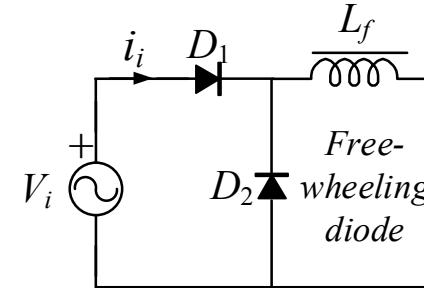


Center-Tapped

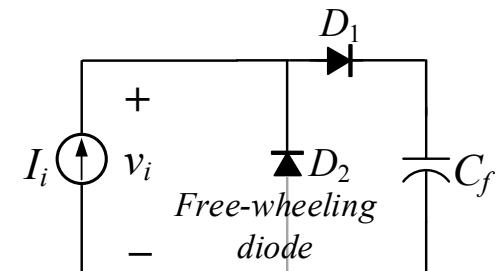


Half-Wave Rectifier

Voltage-Driven



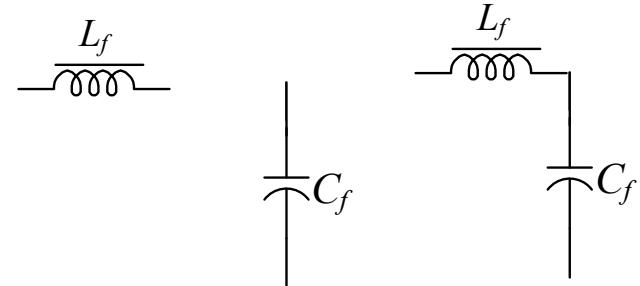
Current-Driven



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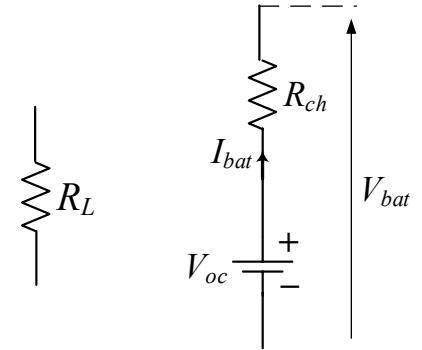
Filters:

- Typically, inductive (L_f), capacitive (C_f), and second-order $L_f C_f$ filters are applied. Third-order “π” or “T” filter networks are used when an advanced filtration is needed, and the available space is limited.
- The output filters are sized based on the output voltage and the current ripple. Typical output voltage ripple is limited to 1% of the nominal voltage.
- Inductive filters are often used in charging applications where the charging current is regulated.

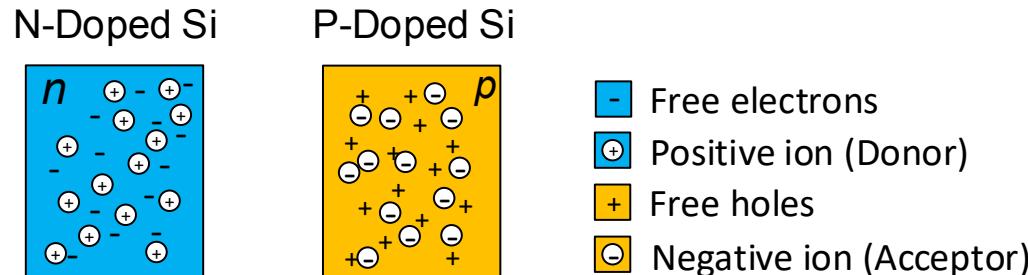


Loads:

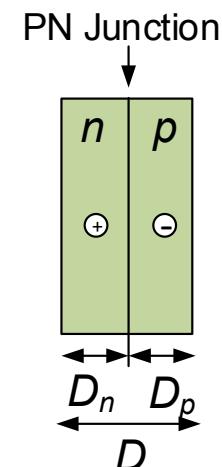
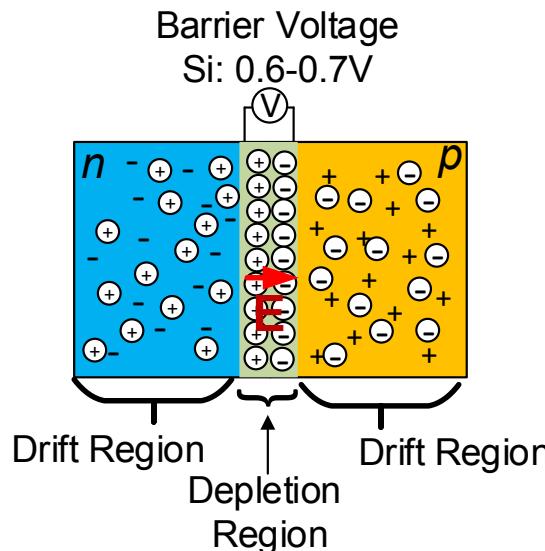
- Resistive loads are used almost exclusively in the textbook to model the load.
- The most common DC load in practice is a battery. Battery should be modeled by a series connection of an ideal voltage source V_{oc} (open-circuit voltage) and charging-discharging resistance R_{ch} . One should keep in mind that R_{ch} varies significantly with temperature and battery age.
- Often a battery is replaced by an equivalent resistor $R_{bat} = V_{bat}/I_{bat}$. While this modification is justifiable for a steady-state analysis, it alters the converter dynamics and should be avoided when designing a controller.



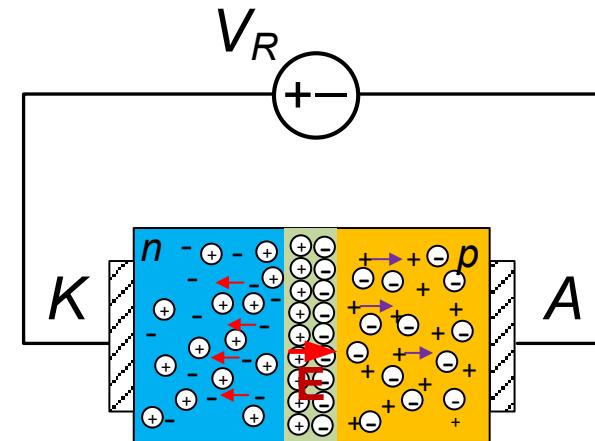
- Electronically neutral P- and N-doped Silicon semiconductors constitute a diode.
- n_p and n_n are the concentrations of dopants in p- and n-doped semiconductors.



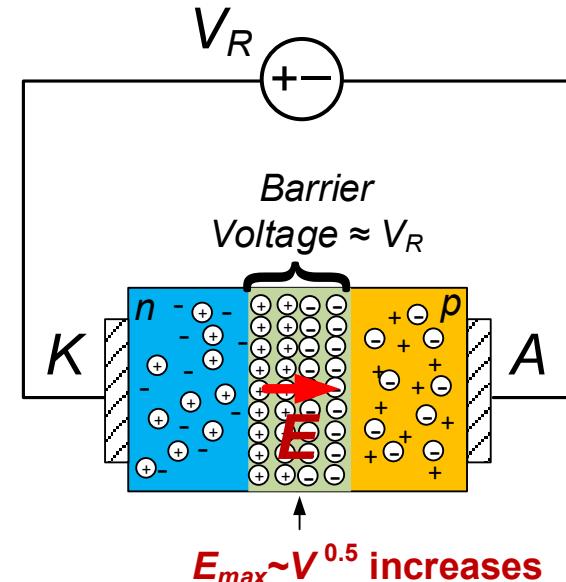
- When a **PN junction** is created, it allows free electrons and holes to migrate to opposite sides.
- Ions in the **depletion region** create a field that eventually stops the migration of free electrons and holes, creating a depletion region.
- The field is strongest along the PN junction line.
- The depletion region spreads to p and n sides; if the number of dopants is the same, the depletion region widths are the same $D_p=D_n$.
- Barrier voltage is established inside the diode (0.6-0.7 V for an Si diode)



- Let us consider that a diode is reverse biased: the anode is connected to the negative terminal of a voltage source and the cathode to the positive terminal.
- The positive voltage source terminal attracts free electrons, and the negative one attracts free holes – depletion region increases

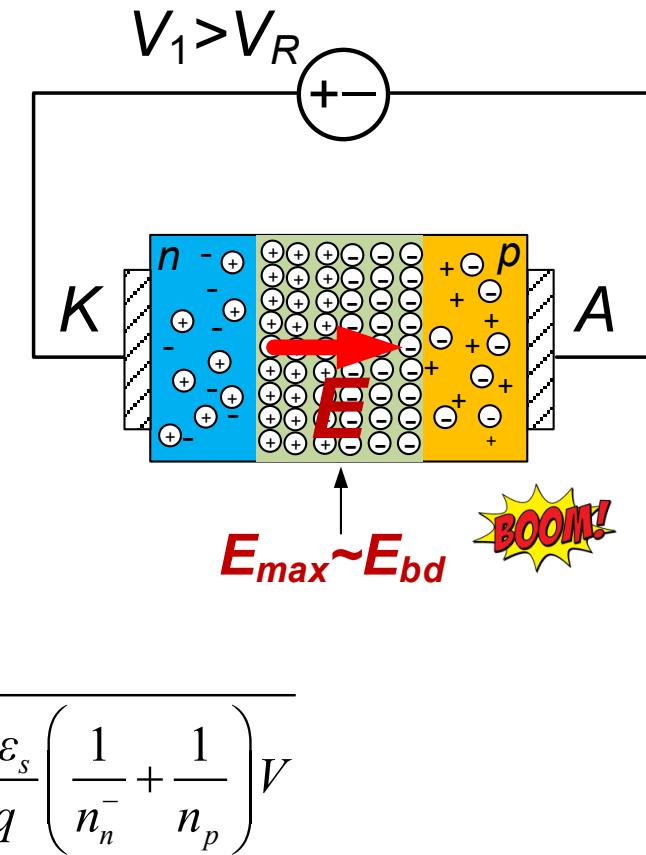


- The field inside the depletion region increases, causing the barrier voltage to increase, too.
- Balance is established when the barrier voltage reaches the polarization voltage V_R .

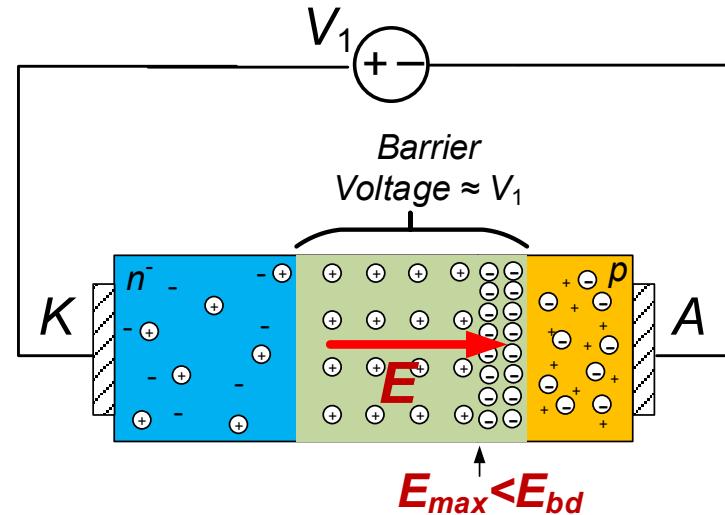


- If we continue increasing the external voltage, the electric field will further increase until it reaches the breakdown value E_{bd} .
- At E_{bd} , the field is strong enough to pull out electrons from ions in the PN junction region – electrons are then accelerated and crashed into neighboring ions – more electrons are created
- Avalanche effect – the destruction of the PN junction and the diode malfunctions.
- Field strength is proportional to the dopant concentrations n_n and n_p :
- To reduce the field, we choose to reduce n_n
- Lower n_n will increase the width of the depletion region:
- The depletion region primarily expands to the low-doped side because:

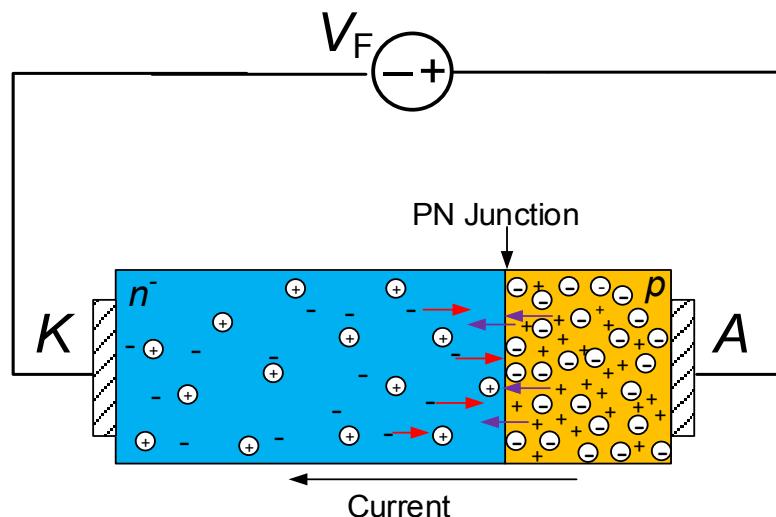
$$D_n n_n = D_p n_p$$



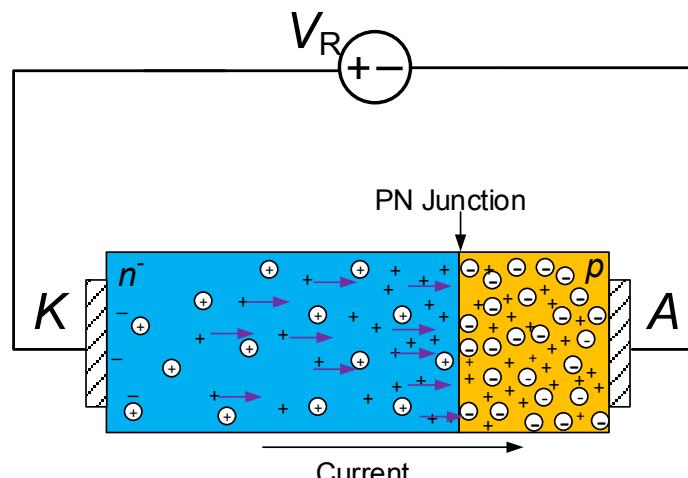
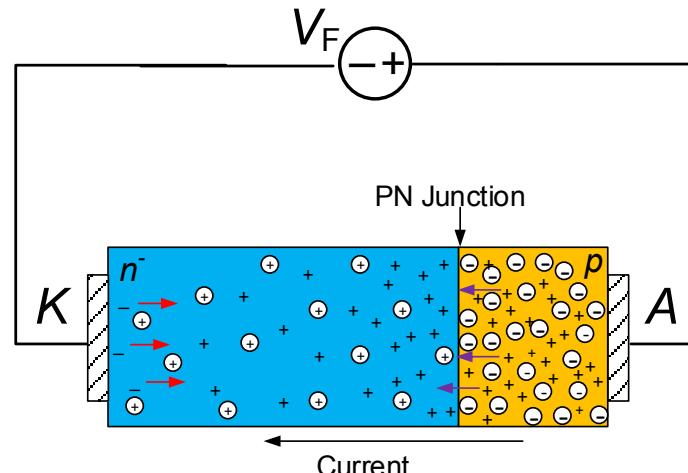
- Therefore, the n drift region must be low doped (designated as n^-)
- The drift region absorbs the depletion layer of the reverse-biased p+n- junction and determines the V_{bd} (E_{bd}) voltage of the diode
- The wide drift region can cause problems during forward-biased (conduction) interval by increasing the ohmic resistance in the current path



- When the polarity of the voltage source changes and the diode becomes forward biased, the depletion region will disappear
- Free holes and electrons will rush to opposite regions, where they become minority carriers
- As minority carriers, they use the diffusion method to move.

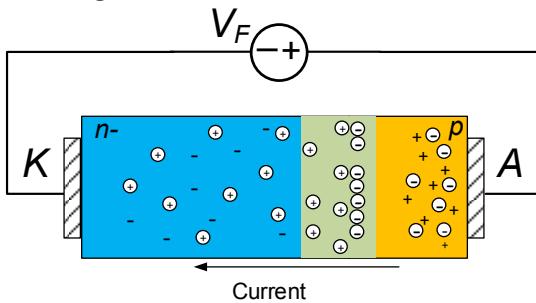


- Due to the disparity between the number of free holes and free electrons, the free holes flood the n- region and effectively turn it into p- – this phenomenon is called “**Conductivity Modulation.**”
- Electrons do not need to drift through n-; instead, they immediately recombine with available holes
- The diode resistance is significantly reduced
- However, the price is paid during the ON \rightarrow OFF transition.
- A significant current in K \rightarrow A direction is needed to remove or recombine free holes in the n- area.
- Only after the holes are removed, the diode will be able to build the depletion region and block voltage V_R .
- Removing minority hole carriers takes a long time.
- This process is called “**Reverse Recovery.**”

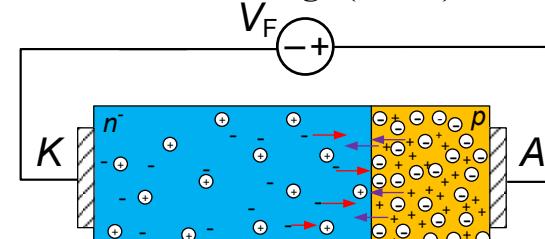


Zone 2 (turn-on transition - 1st part)

- A positive current eliminates the depletion region

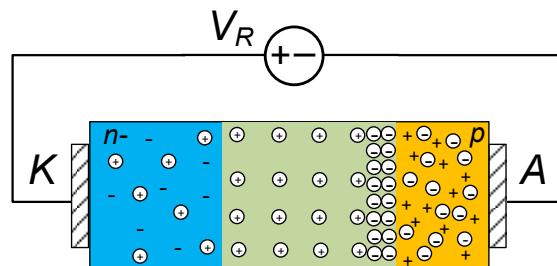
Zone 2 (turn-on transition – 2nd part)

- Depletion zone is removed; “+” and “-” can flow
- Int the beginning, there is no conductivity modulation, and **V** is large ($\times 10V$)



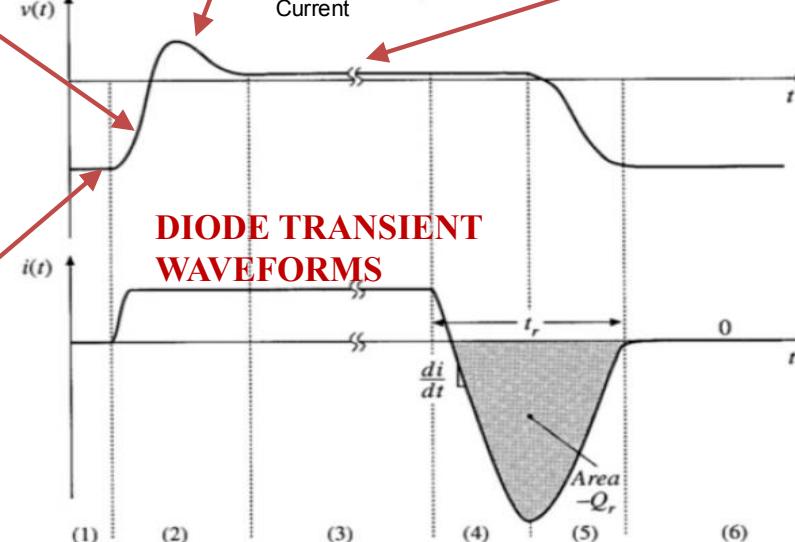
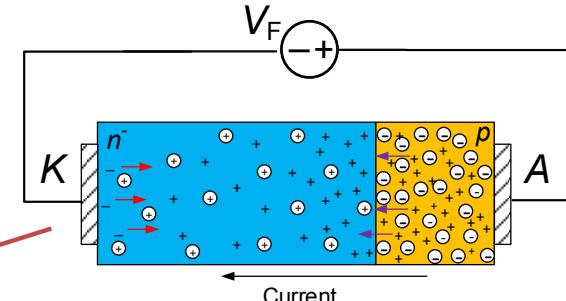
Zone 1 (OFF state)

- There is no current flowing
- Reverse bias voltage V_R appears as the built-in barrier voltage



Zone 3 (ON state)

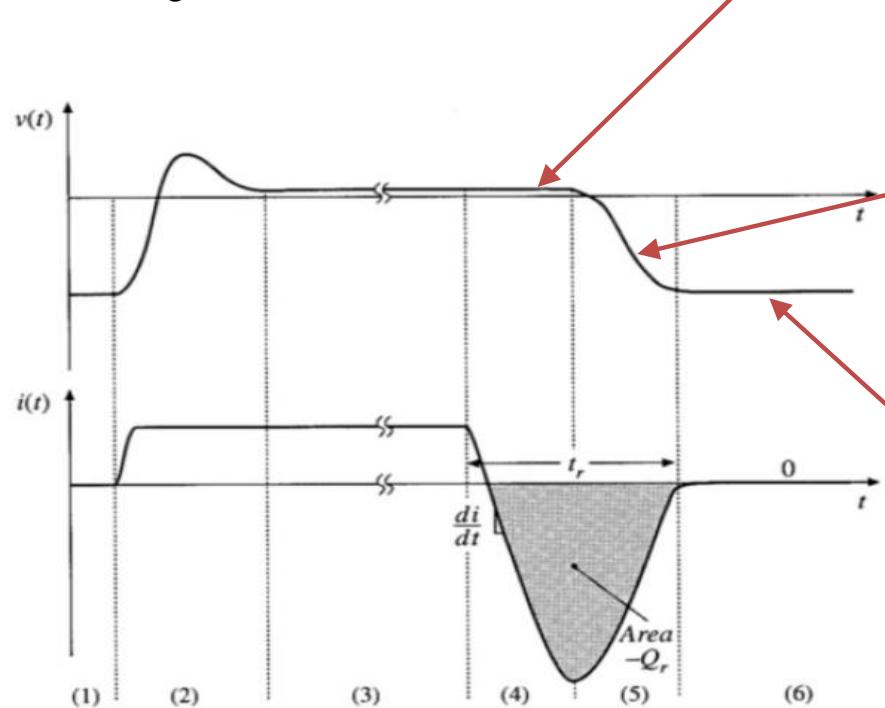
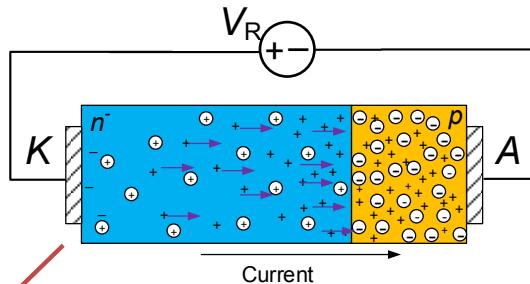
- Positive current, small positive voltage
- Conductivity modulation has reduced the resistance of the n- drift region



Power Diode

Zone 4 (turn-off transition – 1st part)

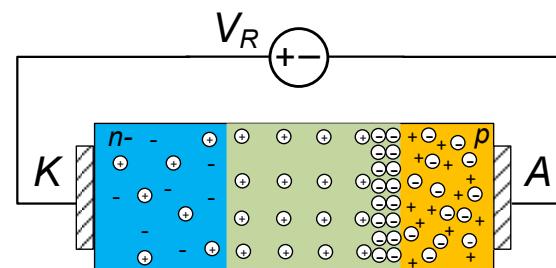
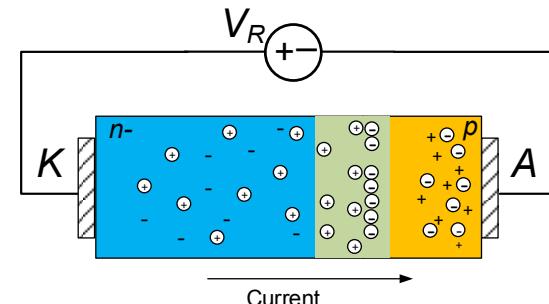
- Negative current through recombination eliminates minority charges from the n- region
- Voltage stays positive until all minority charges are eliminated from the n- zone



DIODE TRANSIENT WAVEFORMS

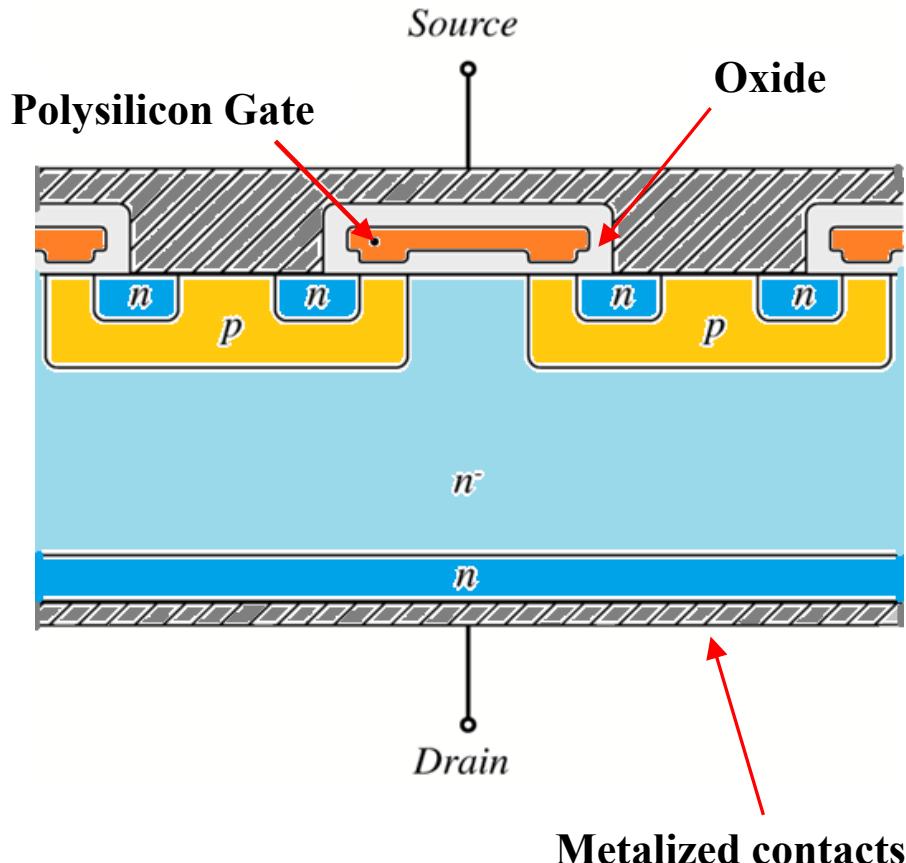
Zone 5 (turn-off transition – 2nd part)

- Negative current reestablishes the depletion region
- The diode is ready to block the voltage



Zone 6 (OFF state)

- The diode is reverse biased and blocks the negative voltage
- No current is flowing

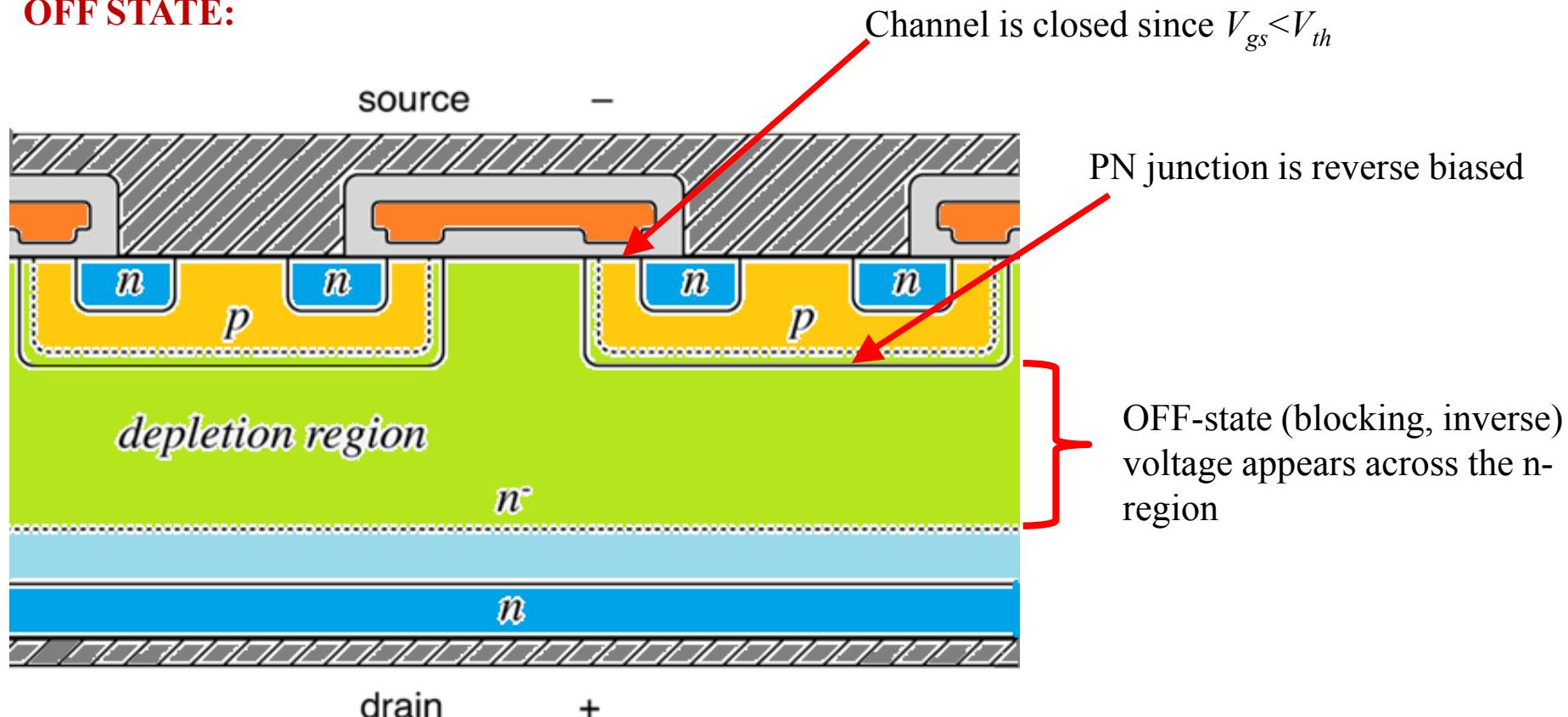


MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) – design characteristics

- An n-channel device is shown in the figure.
- A power MOSFET consists of thousands of small parallel-connected enhancement mode MOSFET cells on a silicon wafer.
- Unlike the signal MOSFETs, which are lateral structures, a power MOSFET is a **vertical structure**. Vertical structures allow higher current rating, larger channel width, and higher blocking voltage.
- **Polysilicon** is used instead of metal for gate connectors due to better manufacturing characteristics and lower threshold voltage.
- The channel length is **below 1 μm** .

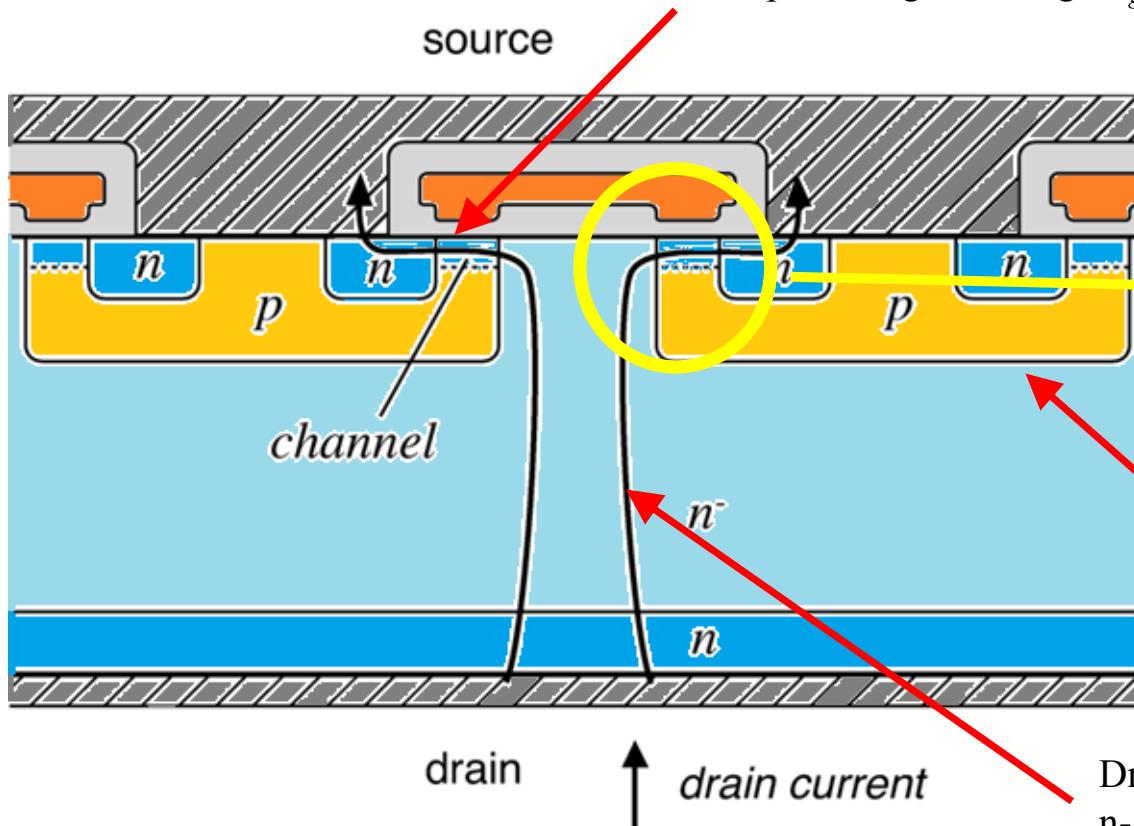
Power MOSFET

OFF STATE:



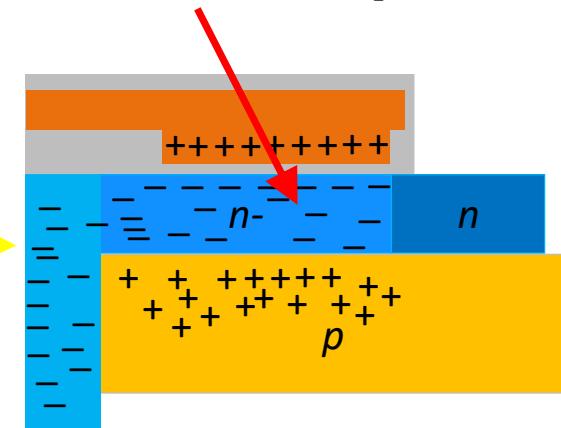
Power MOSFET

ON STATE:



Conducting channel induced by the positive gate voltage $V_{gs} > V_{th}$

A positively polarized gate pushes holes away and attracts electrons to create a channel inside the p zone

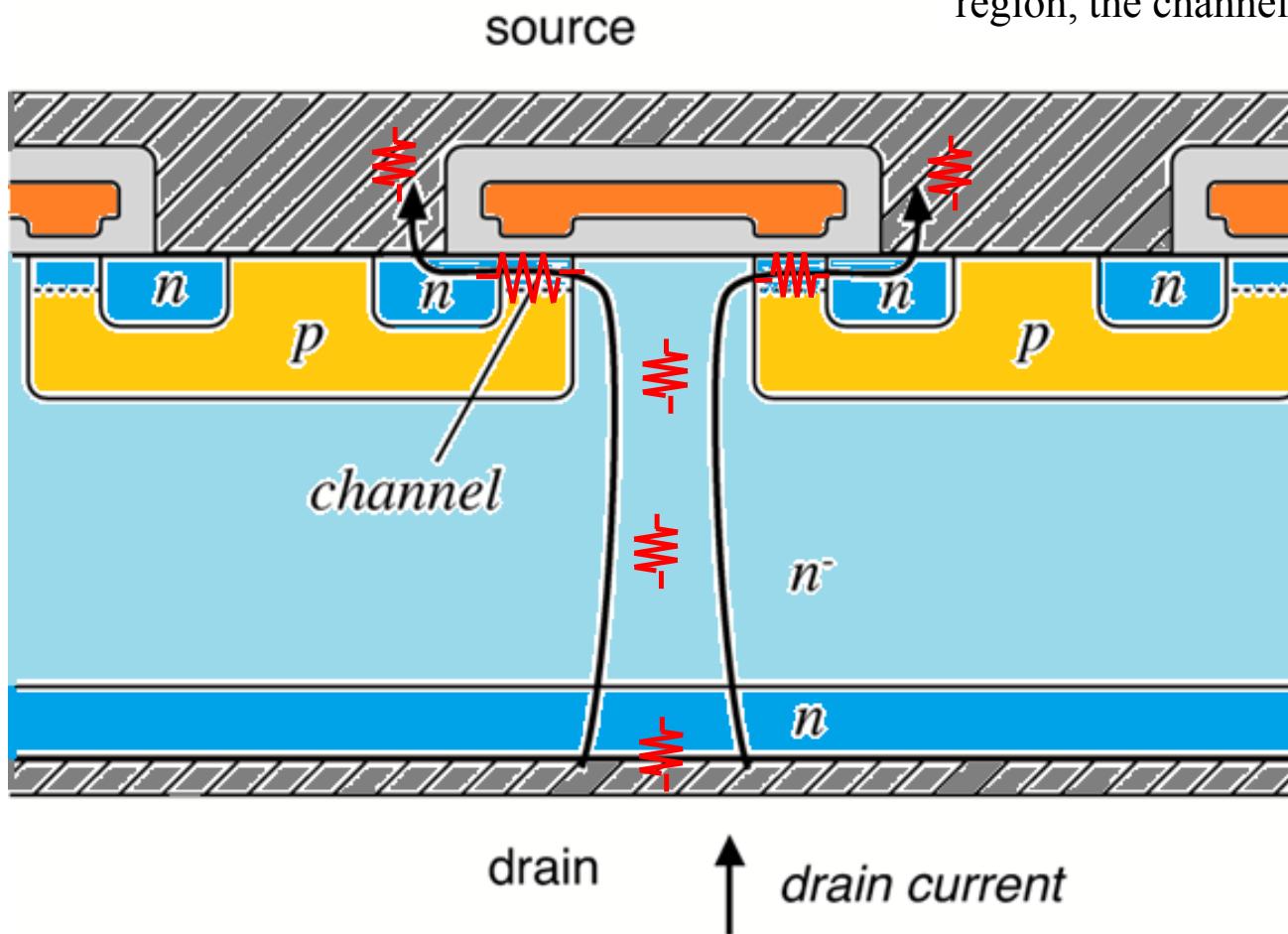


The PN junction is still slightly reverse-biased – there is no current through the PN junction

Drain current flows through the n- region and the conductive channel

Power MOSFET

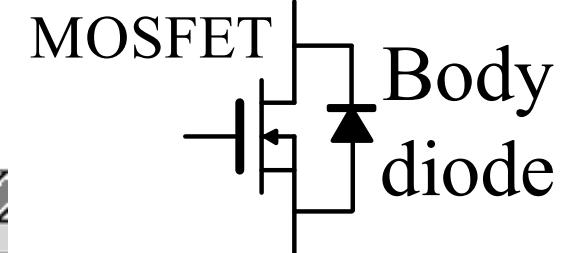
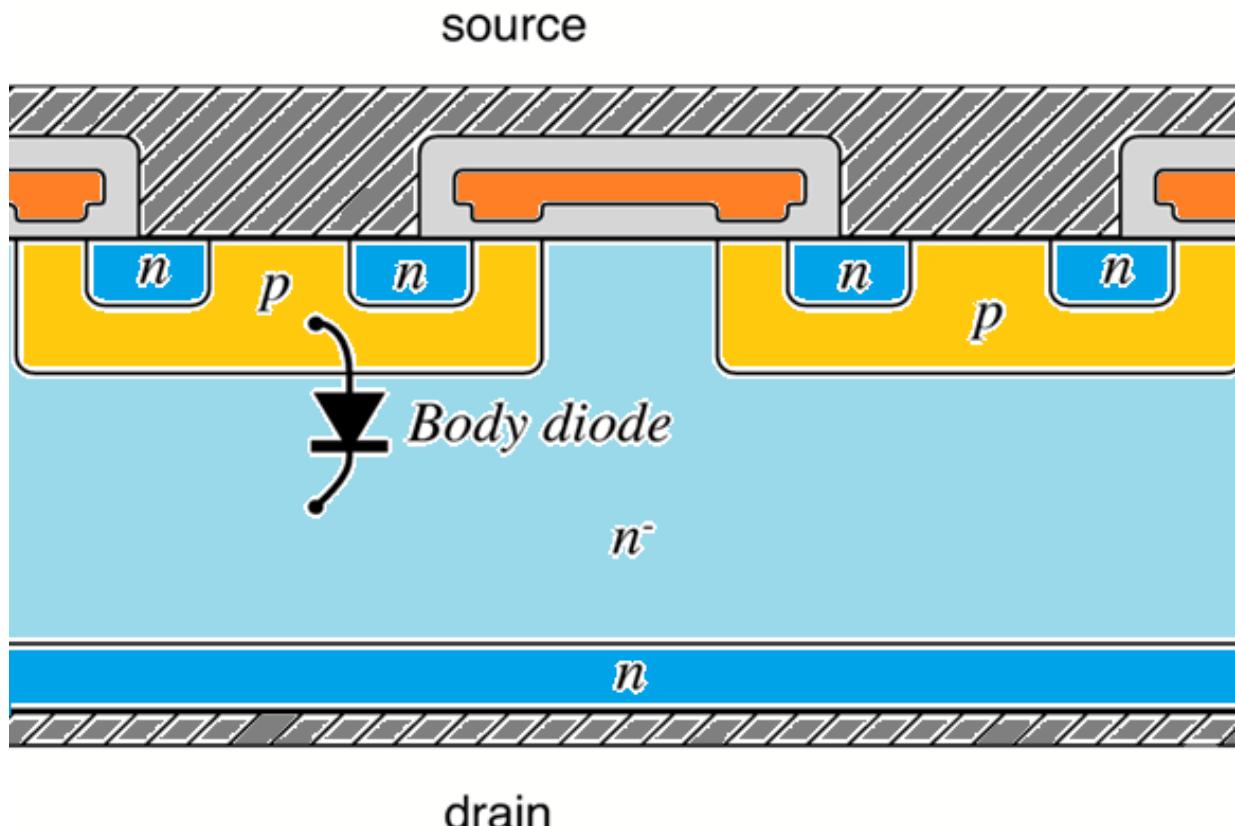
ON STATE:



On-resistance $R_{ds,on}$ is the sum of resistances of the n-region, the channel, and S and D contacts

Power MOSFET

BODY DIODE

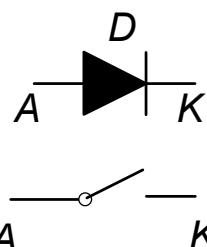
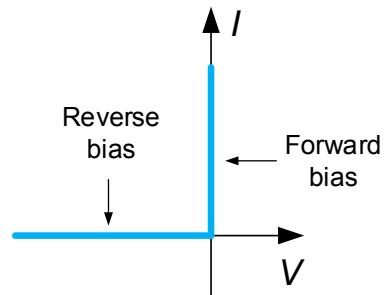


- p-n- junction forms an effective diode in parallel with the channel.
- Negative drain-to-source voltage can forward-bias the body diode.
- The diode can conduct the full MOSFET rated current.
- Diode switching speed is not optimized – body diode is slow, Q_r is large.

Power Diode

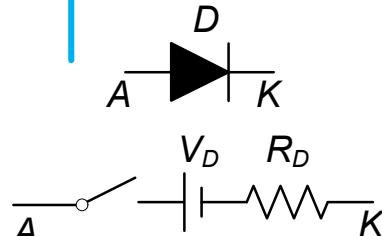
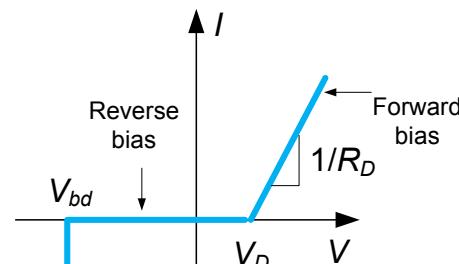
Diode Models:

Ideal diode



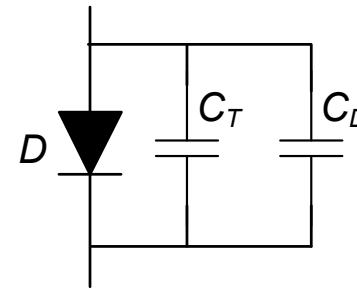
Use it for preliminary study of a converter

Diode with losses modeled



Use it for the loss analysis of a converter

High-frequency transient model



$$C_T = \frac{C_{T0}}{\sqrt{1 - \frac{V_D}{0.7}}}, \quad V_D < 0$$

$$C_D = C_{D0} e^{\frac{qV_D}{kT}}, \quad V_D > 0$$



- C_T – transition capacitance – valid only during the OFF state when it dominates over C_D
- C_D – diffusion capacitance - dominates during the ON state

Power Diode

I-V characteristic of a real diode

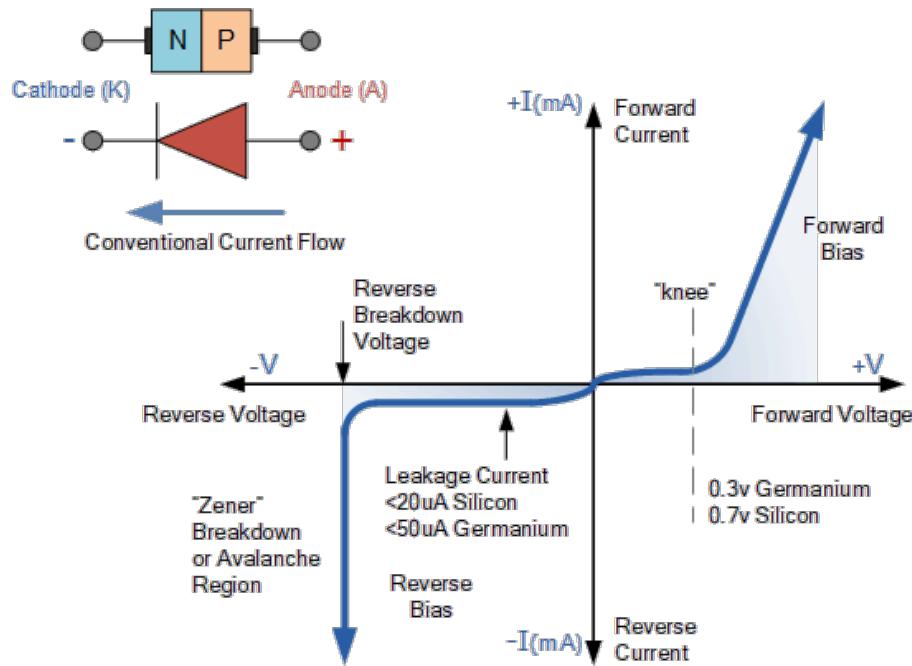
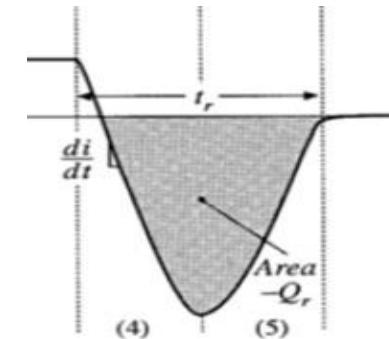


Figure credit: https://www.electronics-tutorials.ws/diode/diode_3.html



Critical parameters for a PN diode selection:
Voltage and current ratings, t_r (or t_r), and Q_r

Standard recovery diodes:

- recovery time is not specified,
- intended for 50/60 Hz applications

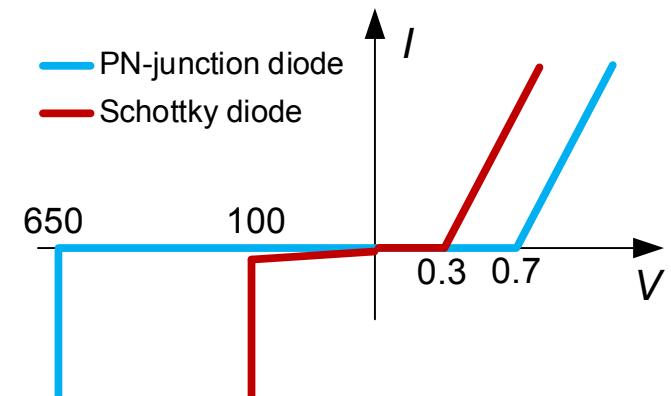
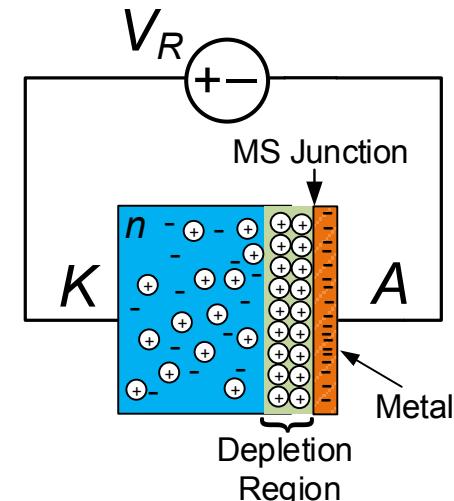
Fast and ultra-fast recovery diodes:

- t_r and Q_r specified
- Intended for switch-mode converter applications

Power Diode

SCHOTTKY DIODES

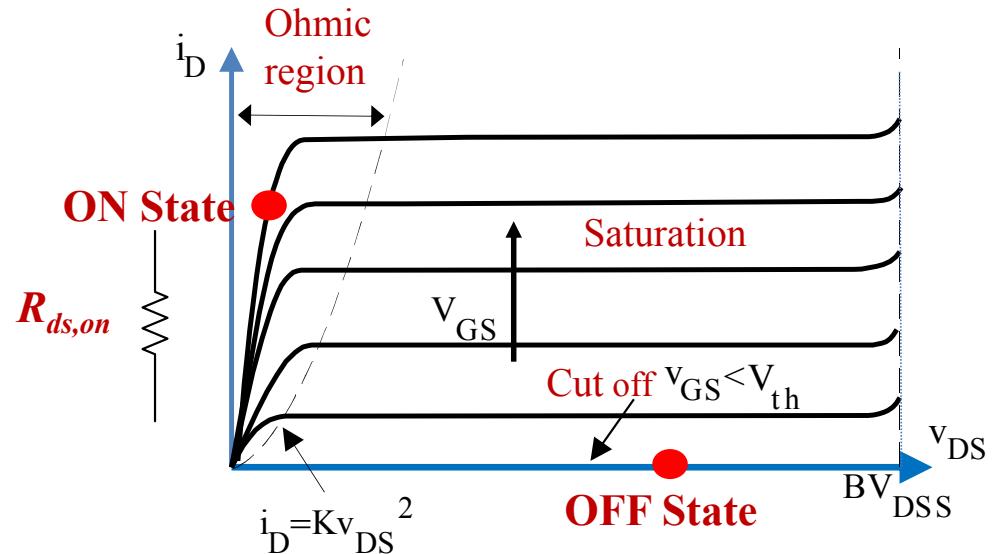
- **Metal–semiconductor (MS) junction:** compound metal electrode bonded on n-doped silicon
- There is no p region – only electrons participate in current flow – Schottky diode is a **majority carrier device**
- Significantly shorter depletion region results in smaller barrier voltage (0.3-0.5 V vs. 0.6-0.7 V in PN junction diodes) – **lower losses**
- No holes – no conductivity modulation – no need for removing holes from n- zone - **much faster turn-off** (nano-second range)
- No conductivity modulation – low doped n- cannot be used – Schottky diode cannot block high voltage – **Lower maximum reverse (breakdown) voltage (<200 V)**. New SiC Schottky diodes have a blocking voltage up to 500 V.



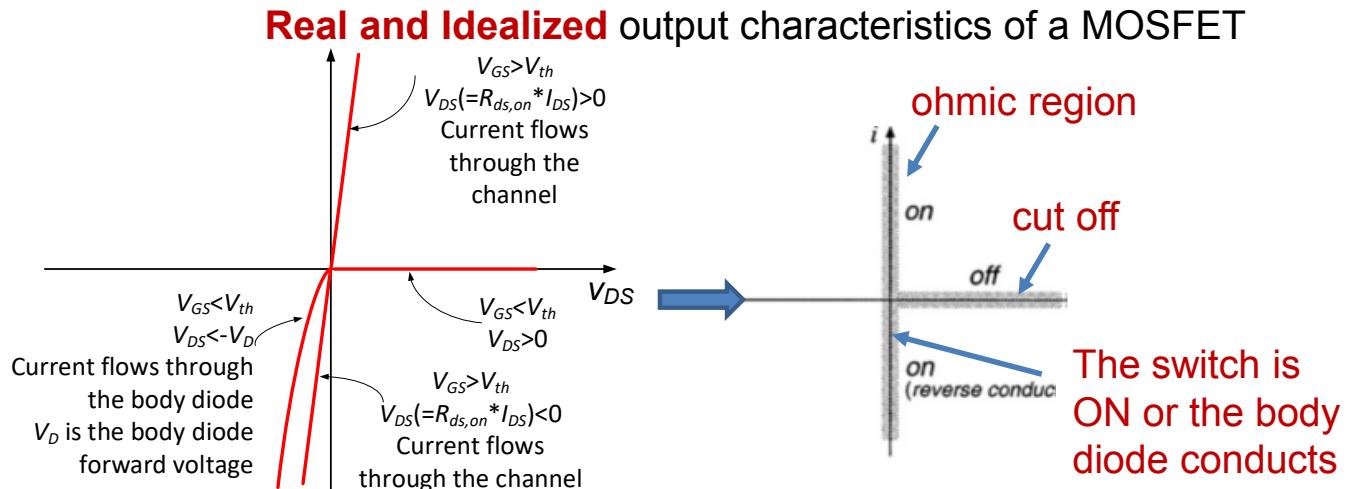
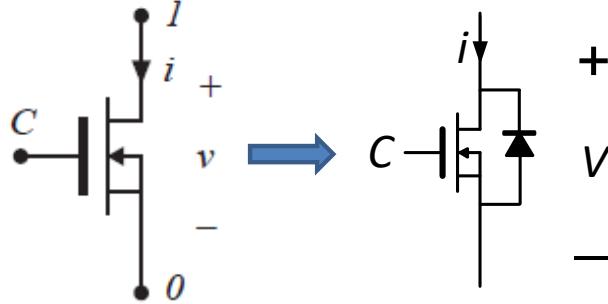
Power MOSFET

MOSFET Static Characteristics

- OFF state: $V_{GS} < V_{th}$
- ON state: $V_{GS} \gg V_{th}$
- V_{th} is usually measured at $I_{ds} = 0.25$ mA. Common values are 2-4V (high-voltage devices) and 1-2V for lower voltage, logic-compatible devices.
- MOSFET OFF state is ideal – the operating point is located at $i_D = 0$ axes
- In ON state, there is a voltage drop over the MOSFET: $R_{ds,on} * I_D$

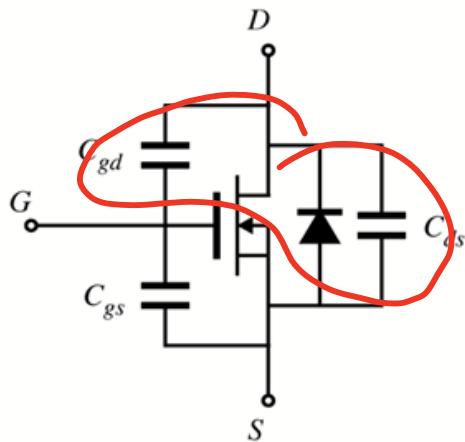


MOSFET Symbols



Power MOSFET

High-frequency and transient model (parasitic capacitances included)



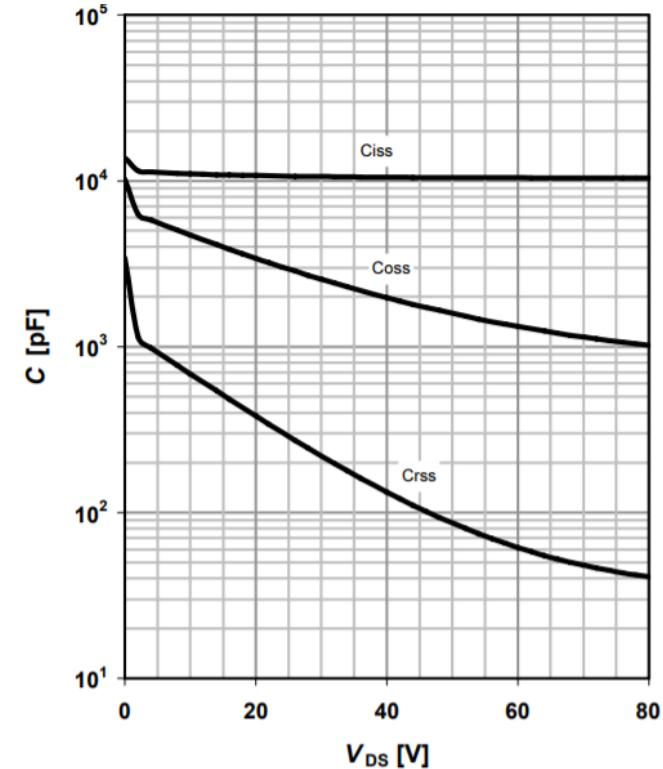
- C_{gs} : large, essentially constant
- C_{gd} : small, highly nonlinear
- C_{ds} : intermediate in value, highly nonlinear
- Switching time is determined by the rate at which the gate driver charges and discharges C_{gs} and C_{gd}

How datasheets provide these parameters:

- Input capacitance $C_{iss} = C_{gd} + C_{gs}$,
- Reverse transfer capacitance (Miller's) capacitance $C_{rss} = C_{gd}$
- Output capacitance $C_{oss} = C_{gd} + C_{ds}$

$$C_{ds} = C_{oss} - C_{iss}$$

V_{DS}	120	V
$R_{DS(on),max}$	3.6	mΩ
I_D	180	A



Power MOSFET – Conclusions

- A majority carrier device: fast switching speed
- Typical switching frequencies: tens of kHz to low MHz range.
- On resistance increases rapidly with the rated blocking voltage.
- Easy to drive – requires the voltage type of a gate driver.
- 4000-V are available, but their practical area of application is up to 900 V.
- Product $R_{ds,on} * Q_g$ is often used as a figure of merit when selecting a MOSFET: a lower value is better.
- The current rating rarely imposes any limit when selecting a MOSFET.

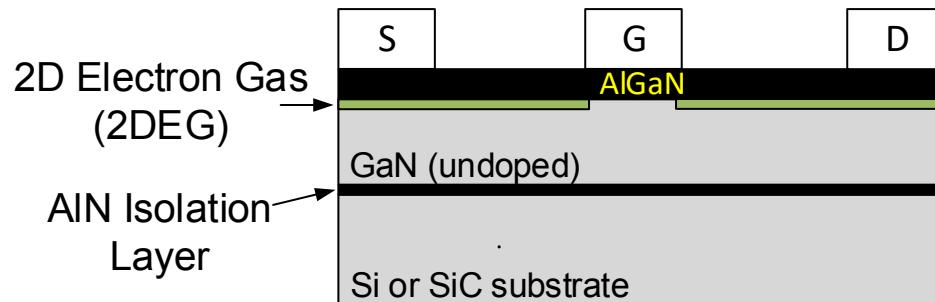
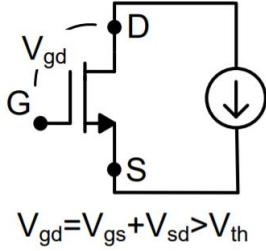
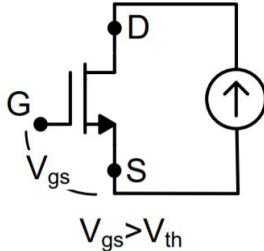
Wide Bandgap Semiconductors

- Wide bandgap semiconductor materials belong to the III-nitride group and demonstrate bandgaps significantly higher than the bandgap of silicon
- The most promising WBG semiconductors are Silicon Carbide (SiC) and Gallium Nitride (GaN)
- Wide-bandgap semiconductor switches operate at much higher voltages (SiC - 6 kV), frequencies (GaN – 10 MHz), and temperatures (SiC – 300°C)
- The disadvantages of WBG semiconductor switches:
 - More expensive than Si switches
 - They are not a direct replacement for Si-based switches – there is a need for new topologies and circuits that will effectively utilize the advantages of WBG devices.
 - New packaging methods are needed.
- SiC MOSFET is a vertical structure very similar to an Si MOSFET.
- GaN MOSFET is a lateral (planar) structure grown on a Si or SiC substrate.

	Unit	SI	SiC	GaN
Band Gap	ev	1.12	3.26	3.39
Critical Field	MV/cm	0.23	2.2	3.3
Electron Mobility	cm ² /(Vs)	1400	950	1500
Thermal Conductivity	W/(cm*K)	1.5	3.8	1.3

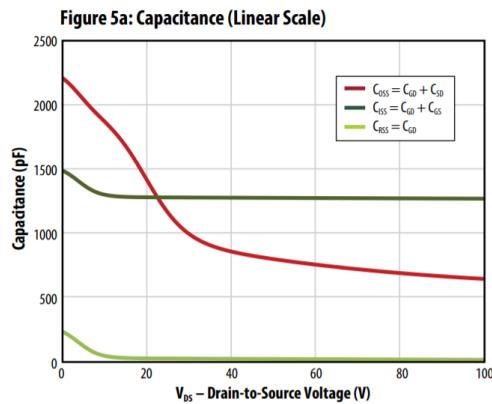
GaN Power Switch

- The two-dimensional electron gas (2DEG) is created at the contact between GaN and AlGaN hetero-epitaxy layers.
- 2DEG is a thin channel with an abundance of highly mobile electrons.
- Implementation of the gate depletes the 2DEG underneath, and a positive gate voltage is needed to re-establish it
- No minority carriers → No reverse-recovery
- GaN MOSFET does not have a body diode!
- However, it still cannot block negative voltage!
- Voltage V_{gd} greater than V_{th} would open the channel, too

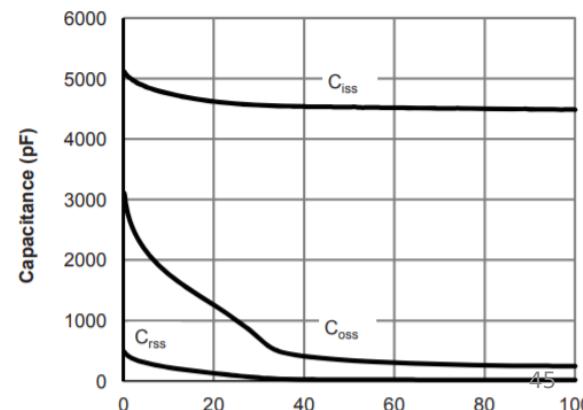


Comparison: GaN vs. Si

GaN: 100 V, 48 A, 4 mΩ

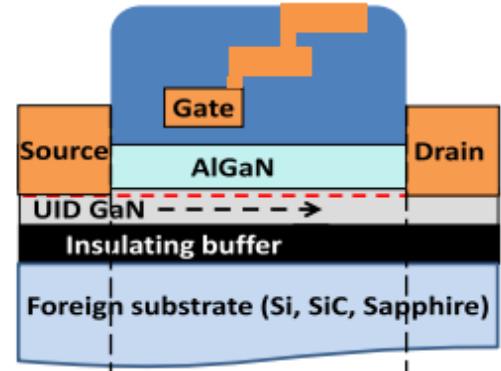


AON6220: 100 V, 48 A, 6.2 mΩ



GaN Power Switch

- Higher breakdown field and lateral structure → smaller device → all parasitic capacitances reduced → faster commutations.
- Very high electron mobility at the interface between GaN and AlGaN (Two-Dimensional Electron Gas (2DEG)) and smaller device → reduced resistance.
- Large bandgap energy → provides better temperature stability and allows a broader temperature range (up to 400° C).
- History of GaN devices:
 - High electronic mobility was discovered by Mimura (1975).
 - GaN Metal Semiconductor Field Effect Transistor (MESFET) (1993).
 - The first commercial depletion-mode HEMT-GaN (2004).
 - The first HEMT-GaN on a Si substrate (2005).
 - The first commercial enhance-mode GaN (eGaN) (2009).



S. Chowdhury and U. K. Mishra, "Lateral and Vertical Transistors Using the AlGaN/GaN Heterostructure," in *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3060-3066, Oct. 2013.

GaN Power Switch

Application characteristics (blue – positive, red – negative)

- Q_{GD} is reduced to 20% of an equivalent Si MOSFET value.
- Q_{OSS} is reduced to half, compared to an Si MOSFET, and it is less nonlinear.
- Q_{GS} is reduced to 25-35% of the value for an Si device of the same $R_{ds,on}$.
- Lateral structure → no parasitic bipolar junction → no minority carriers → Q_{rr} is zero.
- $R_{ds,on}$ in GaN is lower for about 10-15% due to higher mobility of major carriers and smaller devices.
- The temperature coefficient of resistance $R_{ds,on}$ is positive and around 80% of Si MOSFET one.
- The temperature range of operation of AlGaN/GaN HEMT is expected to exceed the one of the Si MOSFET (150-175°C). 450+°C operation is demonstrated [*]
- V_{Th} is around 1.6-2.5 V, and it is stable with temperature
- V_{DRV} is 5-6 V, which is around the half of V_{DRV} in Si MOSFETs
- **No body diode, but there is a diode effect → V_F approximately twice the value in Si MOSFETs**
- **Gate leakage current is higher (in the mA range - due to the Schottky barrier replacing the oxide).**

[*] D. Maier *et al.*, "Testing the Temperature Limits of GaN-Based HEMT Devices," in *IEEE Transactions on Device and Materials Reliability*, vol. 10, no. 4, pp. 427-436, Dec. 2010.

Switching losses

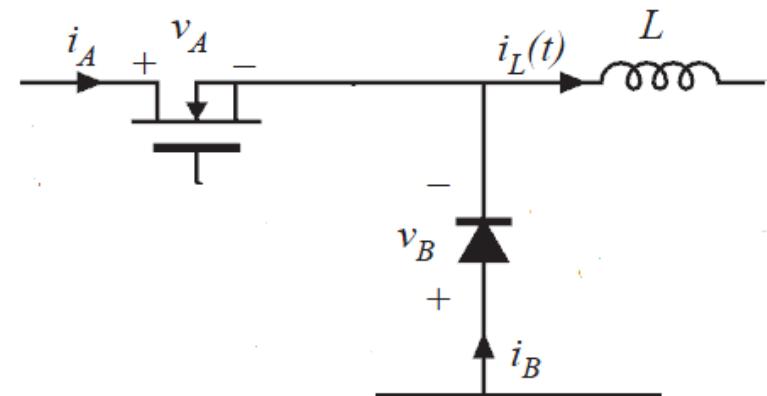
What determines the switching losses?

- Switch physics – studied in Advance Power Electronics courses.
- Converter topology – we will review it here.

Why is the circuit topology important?

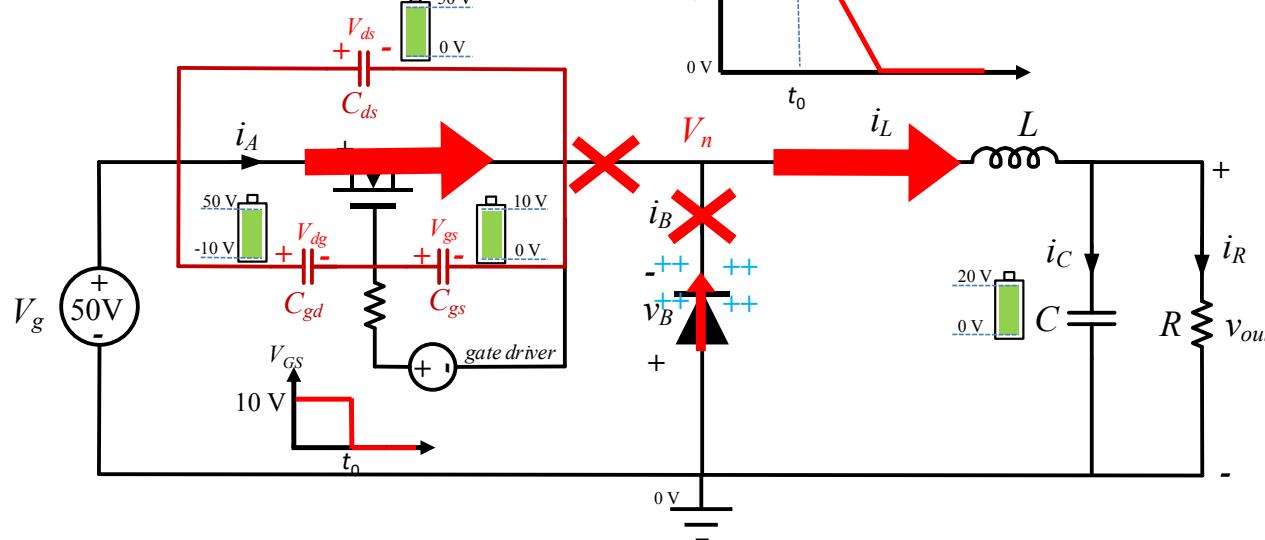
- The converter topology often **forces its switches to generate both the non-zero voltage and current during transitions.**
- Example: **clamped-inductive load** - it consists of an active switch, a diode, and an inductive load (inductor). Switches transfer the inductive load $i_L(t)$ current to each other during the switching transition.
- Since the switching interval is short, the **inductor current is constant** during the entire switching transition.

$$i_L(t) = i_A(t) + i_B(t) = \text{const}$$



- Buck converter and clamped-inductive load will be used to investigate losses in switches below.
- For simplicity, waveforms are often approximated by piecewise-linear segments

Turn-off Power Loss

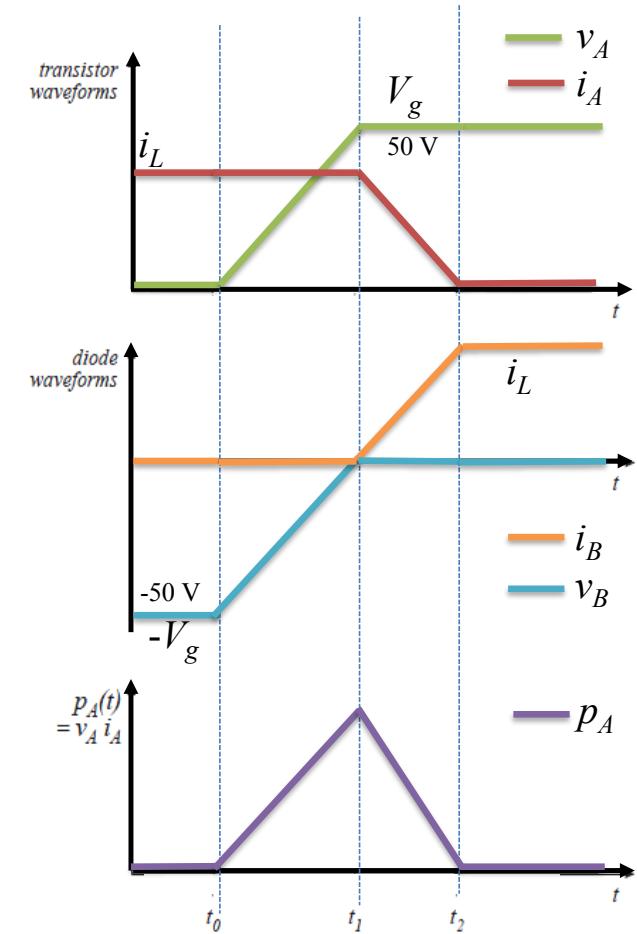


$t < t_0$ MOSFET is on, the diode is off; $i_A(t) = i_L$, $i_B(t) = 0$

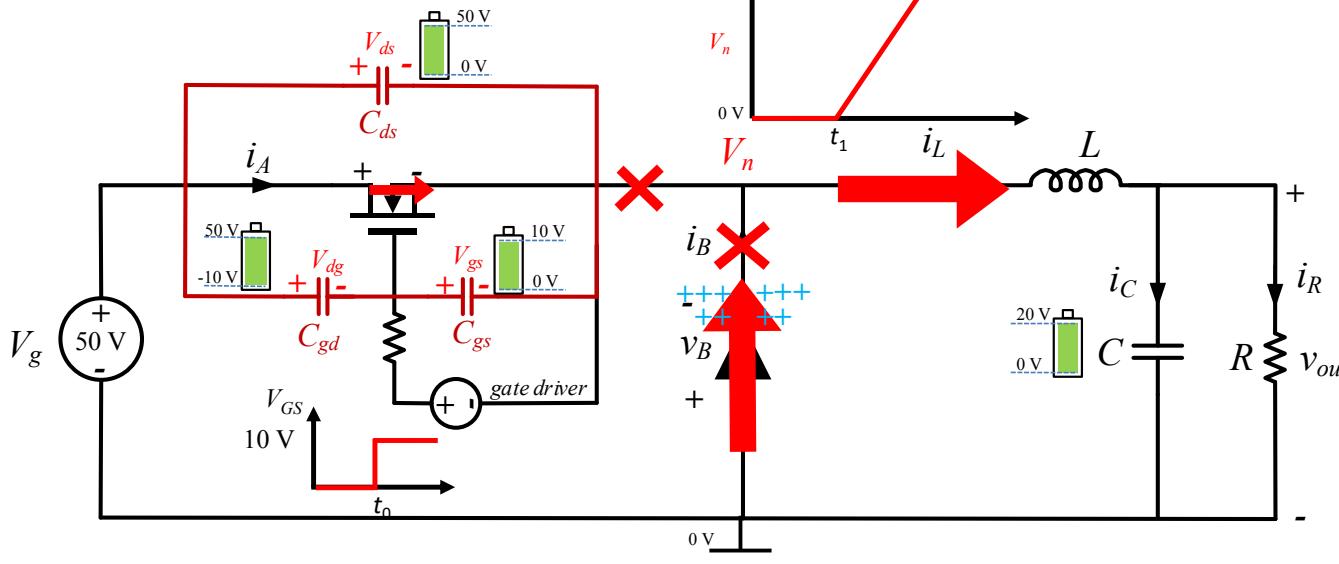
$t_0 < t < t_1$ Gate-driver charges the C_{gd} , and voltage $v_A(t)$ across the switch increase; At $t=t_1$, the diode becomes forward-biased

$t_1 < t < t_2$ Gate-driver discharges C_{gs} ; V_{gs} decreases and causes the reduction of $i_A(t)$. Current begins to commute from MOSFET to the diode. When $V_{gs} < V_{th}$ - MOSFET stops conducting

$t_2 < t$ $v_B(t) = 0$. and the diode conducts the entire current I_L



Turn-on Power Loss

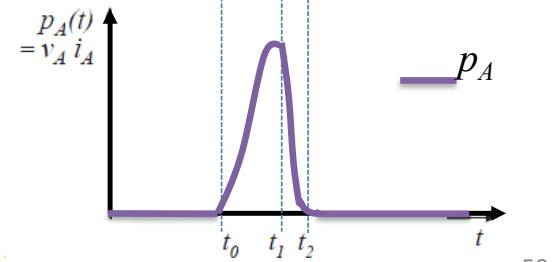
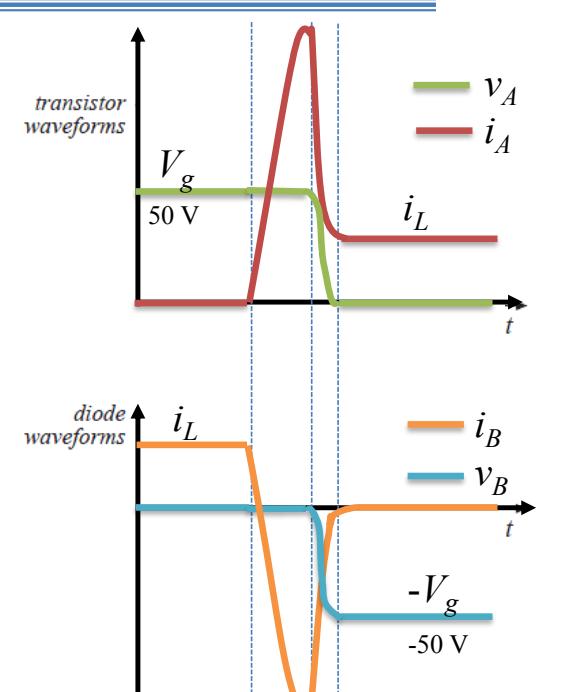


$t < t_0$ The diode conducts current, and MOSFET is off. In the diode, free holes are in the n- zone (conductivity modulation).

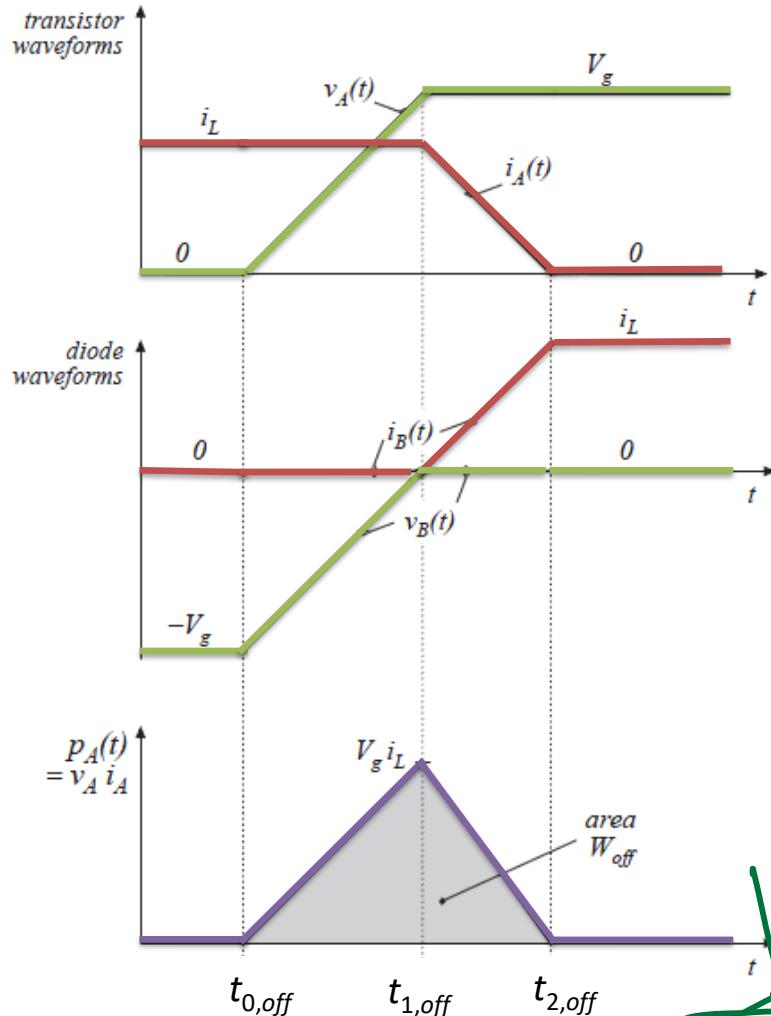
$t_0 < t < t_1$ MOSFET is conducting. The current provided by the MOSFET flows through the diode (K to A direction) to eliminate p holes from the n- region

$t_1 < t < t_2$ Holes are removed from the n- region, and the current is establishing the depletion region. The MOSFET still provides this current!

$t_2 < t$ The diode is finally off, and it blocks voltage V_g . The MOSFET conducts i_L



Turn-off Switching Loss

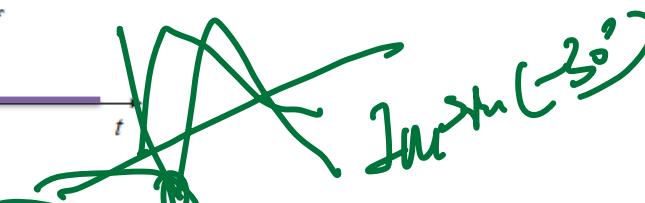


The energy lost inside a MOSFET during its turn-off transition:

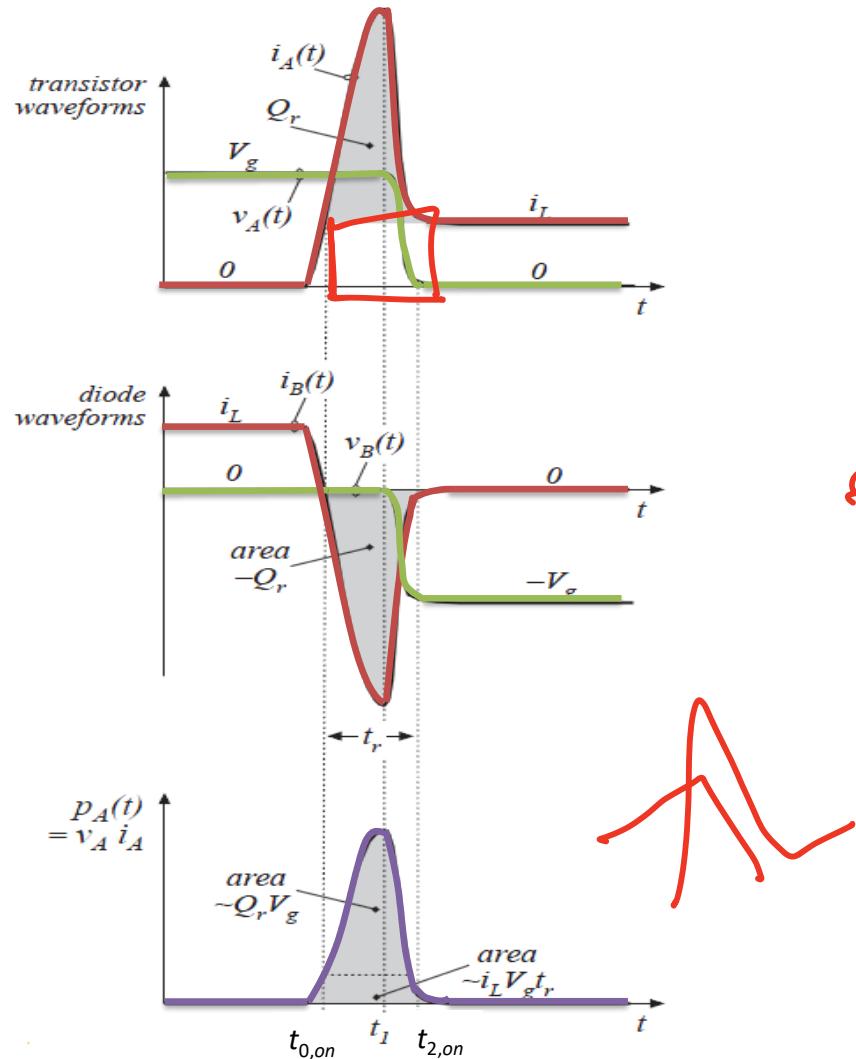
$$W_{off} = \underbrace{\int_{t_{0,off}}^{t_{2,off}} p(t) dt}_{\text{area under } p(t) \text{ curve}} = \frac{1}{2} V_g i_L (t_{2,off} - t_{0,off}) = \frac{1}{2} V_g i_L (t_{Vr} + t_{If})$$

Tip: V_g is used in the expression, but that may not be the case in other converters. Always use the blocking voltage of a MOSFET in the energy loss expressions (including the next one, too)

turn off
energy



Turn-on Switching Loss *and difference*



of Overlapping VI

Losses during the turn-on transition if the diode demonstrates a reverse recovery characteristic:

$$W_{on} = \int_{\text{switching transitions}} v_A(t) i_A(t) dt \approx [V_g i_L t_r + V_g Q_r]$$

t_{rr} – reverse recovery time

Q_r – reverse recovery charge

If the diode does not show reverse recovery behavior (e.g., a Schottky diode), losses during the turn-on transition are very similar to W_{off} :

$$W_{on} = \int_{t_{0,on}}^{t_{2,on}} p(t) dt = \frac{1}{2} V_g i_L (t_{2,on} - t_{0,on}) = \frac{1}{2} V_g i_L (t_{Ir} + t_{Vf})$$

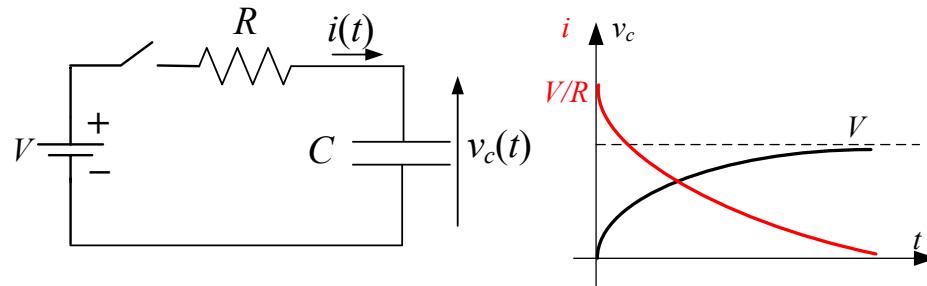
area under $p(t)$ curve

$\Sigma V_g i_{tr} + V_g Q_r$

Charging and Discharging a Linear Capacitor

Let us first understand the losses while charging a linear (voltage-independent) capacitor.

Charging capacitor from a voltage source:



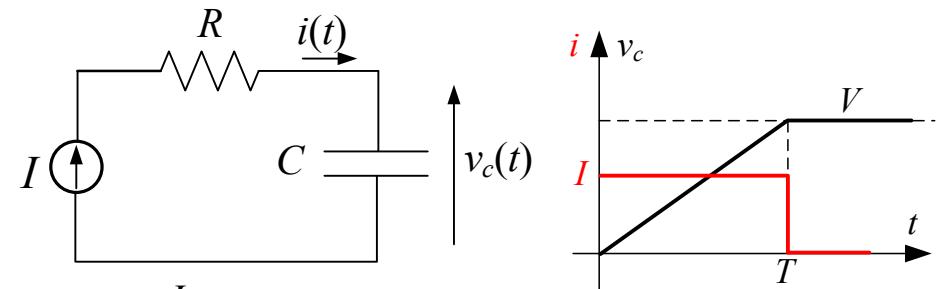
$$v_c(t) = V \left(1 - e^{-\frac{t}{RC}} \right) \quad i(t) = \frac{V}{R} e^{-\frac{t}{RC}}$$

$$p_{loss}(t) = R i^2(t) = \frac{V^2}{R} e^{-\frac{2t}{RC}}$$

$$W_{V,loss} = \int_0^{+\infty} p_{loss}(t) dt = \frac{1}{2} C V^2 \quad \Rightarrow \quad W_{V,loss} = W_{V,c} = \frac{1}{2} C V^2$$

- Loss during charging is always equal to the energy stored in the capacitor. The source provides both portions.
- The energy loss cannot be reduced by reducing the parasitic resistance R .

Charging capacitor from a current source:



$$v_c(t) = \frac{It}{C} \quad i(t) = I$$

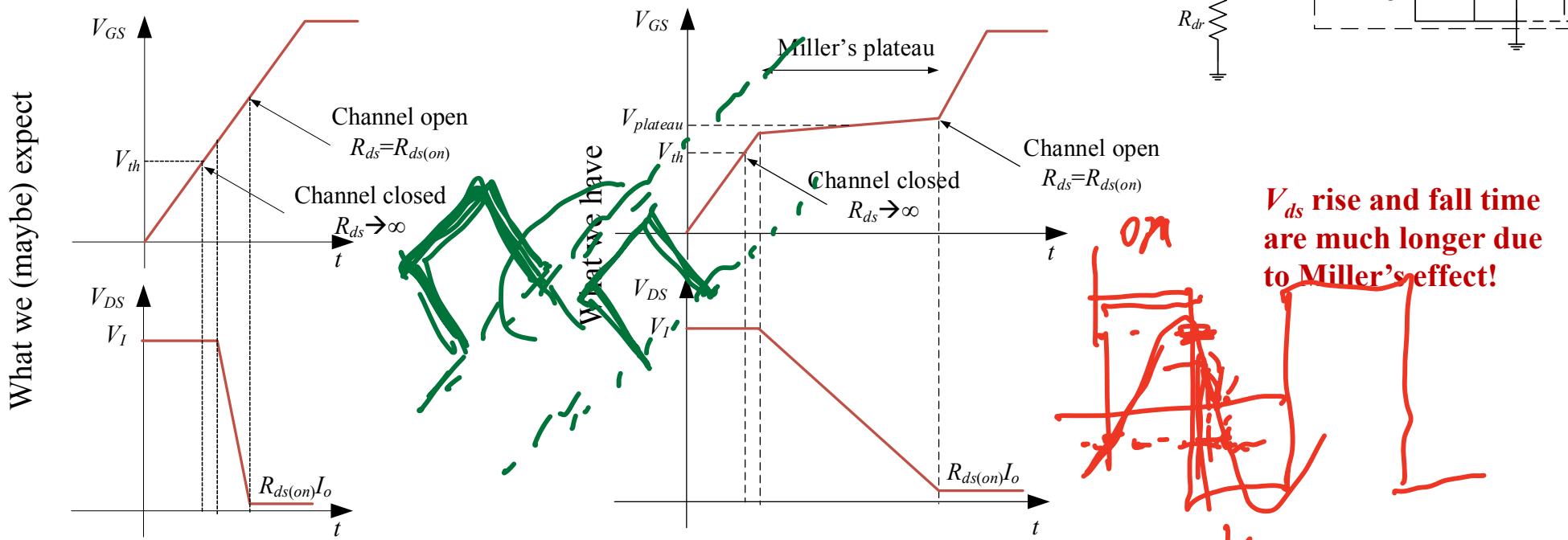
$$p_{loss}(t) = R i^2(t) = RI^2$$

$$W_{I,loss} = \int_0^{+\infty} p_{loss}(t) dt = RI^2 T = RCVI$$

- $W_{I,loss}$ is always less than $W_{V,loss}$ when charging the same C to the same voltage V for the same time T .
- The energy loss can be reduced by reducing the parasitic resistance R .

Effect of the Miller's Capacitance on Switching Losses

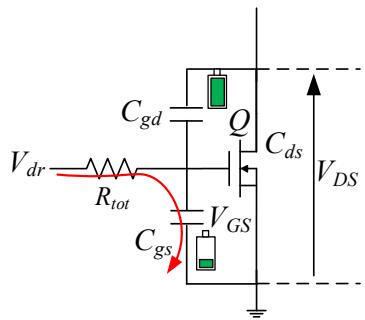
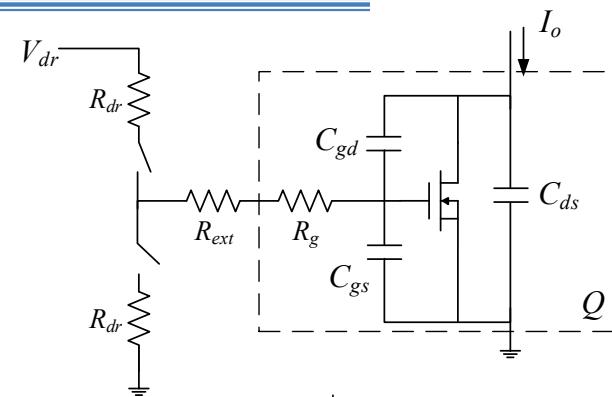
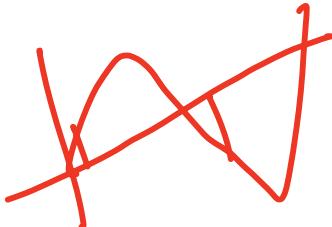
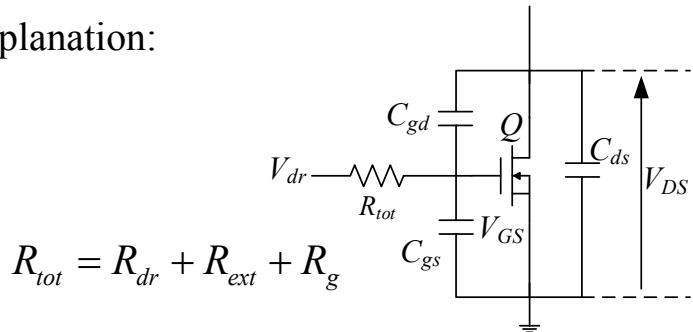
- Miller's effect is caused by the parasitic capacitance C_{gd} (often called Miller's capacitance) and was named by John Milton Miller who identified and explained the similar behavior in vacuum tubes in 1920.
- Let us study the turn-on transition of a switch to understand Miller's effect.



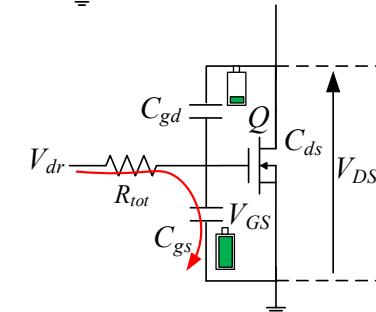
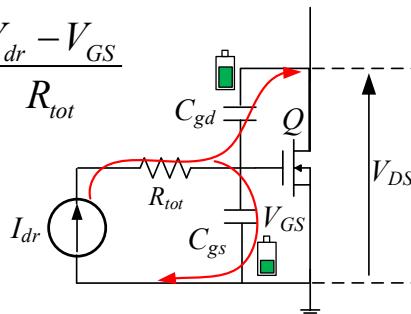
Note: the gate threshold voltage V_{th} defines the beginning of the conduction of the channel: the required gate-source voltage at a specified drain current (typically around 250 μ A), at the room temperature, and for $V_{DS}=V_{GS}$.

Effect of the Miller's Capacitance on Switching Losses

Explanation:



$$I_{dr} = \frac{V_{dr} - V_{GS}}{R_{tot}}$$



$$dQ_{dr} = C_{gs} dV_{GS} + C_{gd} dV_{GD} = C_{gs} dV_{GS} + C_{gd} (dV_{GS} - dV_{DS}) = \left(C_{gs} + C_{gd} \left(1 - \frac{dV_{DS}}{dV_{GS}} \right) \right) dV_{GS} = C_{gs,eq} dV_{GS}$$

$$C_{gs,eq} = C_{gs} + C_{gd} \left(1 - \frac{dV_{DS}}{dV_{GS}} \right) = C_{gs} + C_{gd} (1 + |A_v|)$$

Since the voltage gain A_v is very high (often greater than 100), effective capacitance seen at the gate is increased many times during the Miller's plateau interval

Gate Circuit Loss

Gate driver loss

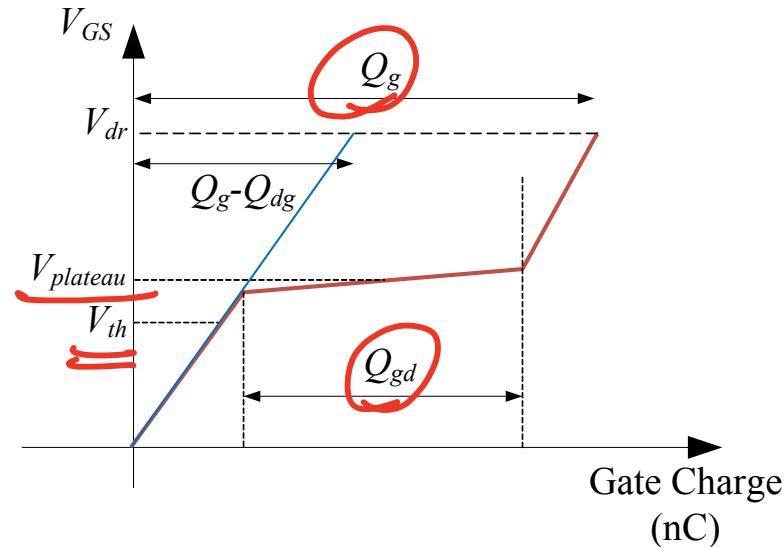
- The input capacitance of a power MOSFET C_{iss} is nonlinear. Therefore, estimating the gate-drive power based on the input capacitance is difficult. A more straightforward method relies on the concept of the gate charge Q_g . The energy required to charge and discharge the MOSFET input capacitance is:

$$\text{ZVS } \left(\frac{dV_{DS}}{dV_{GS}} \approx 0 \right): W_G = (Q_g - Q_{gd}) V_{GSpp} \Rightarrow P_G = f(Q_g - Q_{gd}) V_{GSpp}$$

$$\text{Hard Switching } \left(\frac{dV_{DS}}{dV_{GS}} \gg 0 \right): W_G = Q_g V_{GSpp} \Rightarrow P_G = f Q_g V_{GSpp}$$

V_{GSpp} - the peak-to-peak gate-to-source voltage – can be different than V_{dr} *ds L*

- G_{gd} depends on the final value of V_{ds} . However, since C_{gd} is very small for high voltage, that impact disappears after a certain voltage.
- At high frequency (MHz range), P_G becomes significant and should be taken into consideration **MHz**

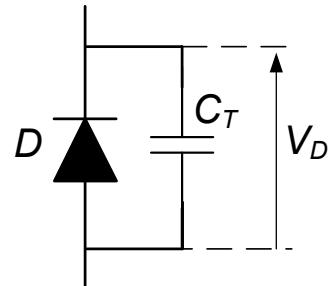


Q_g	Total Gate Charge	—	70	98	nC pF	$V_{DD} = 100V, I_D = 46A, V_{GS} = 10V$ ③
Q_{gd}	Gate-to-Drain Charge	—	23	—		$V_{GS} = 0V$
C_{iss}	Input Capacitance	—	4600	—		$V_{DS} = 25V$
C_{oss}	Output Capacitance	—	460	—		$f = 1.0\text{MHz}$,
C_{rss}	Reverse Transfer Capacitance	—	91	—		

For more details on gate charge, read: <https://www.vishay.com/docs/73217/an608a.pdf>

Losses Due to Charging - Discharging C_{oss}/C_{ds}

PN-Junction Transition Capacitance:



$$C_j = \frac{C_{j0}}{\left(1 + \frac{|V_D|}{V_B}\right)^m}$$

V_B - barrier potential (0.5-0.7 V)

C_{j0} - zero-voltage junction capacitance

m - grading coefficient ($m=1/2$ for step junctions and $m=1/3$ for graded junctions)

$$V_B = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$$C_{j0} = A \sqrt{\frac{\epsilon_0 \epsilon_r q}{2V_B \left(\frac{1}{N_D} + \frac{1}{N_A}\right)}} \approx A \sqrt{\frac{\epsilon_0 \epsilon_r q N_D}{2V_B}} \quad \text{for } N_D \ll N_A$$

V_T - thermal voltage

N_A - acceptor concentration

N_D - donor concentration

$n_i = 1.5 \times 10^{10}$ - intrinsic carrier concentration

$q = 1.602 \times 10^{-19}$ C - charge of an electron

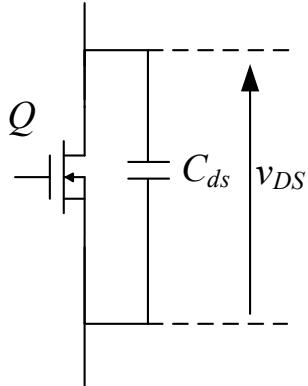
A - junction area

$\epsilon_0 \epsilon_r$ - permittivity of the material (silicon)

Losses Due to Charging - Discharging C_{oss}/C_{ds}

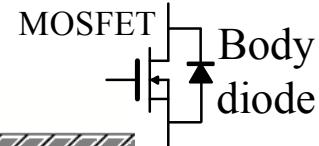
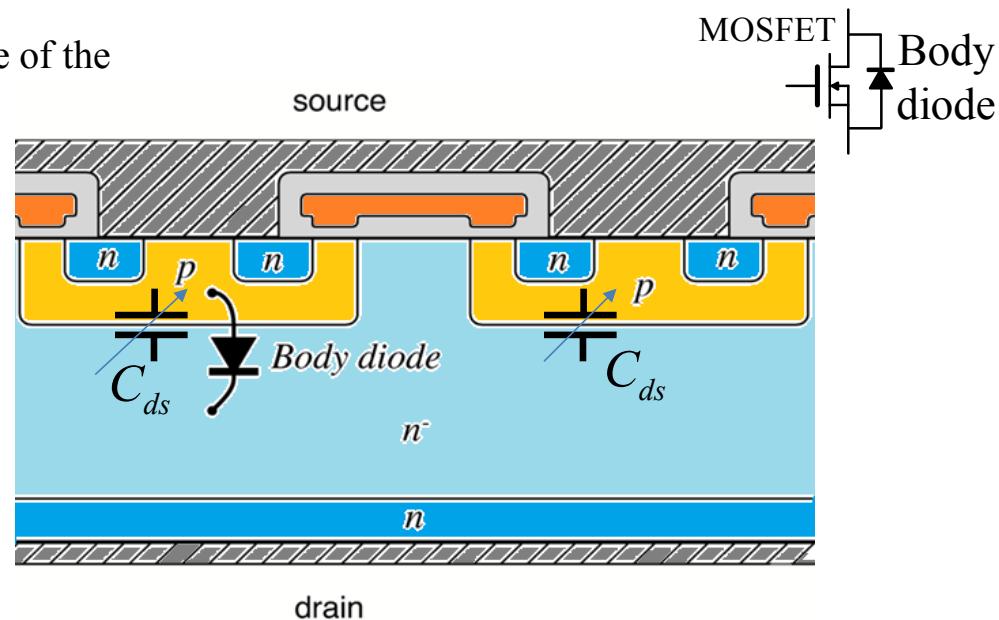
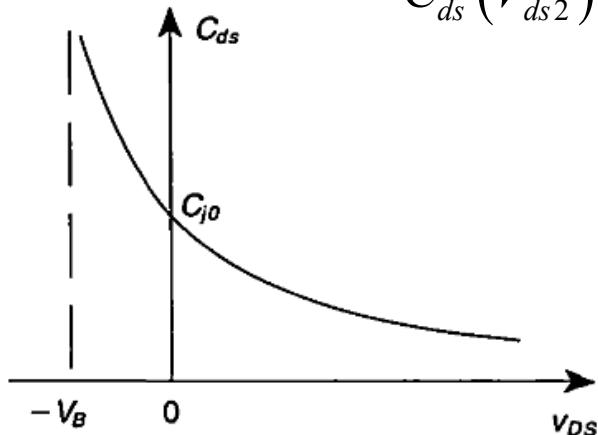
ds

The MOSFET's drain-source capacitance C_{ds} is the capacitance of the body-drain PN step junction diode



$$C_{ds} = \frac{C_{j0}}{\sqrt{1 + \frac{v_{ds}}{V_B}}}$$

$$\frac{C_{ds}(V_{ds1})}{C_{ds}(V_{ds2})} = \sqrt{\frac{V_{ds2} + V_B}{V_{ds1} + V_B}}$$

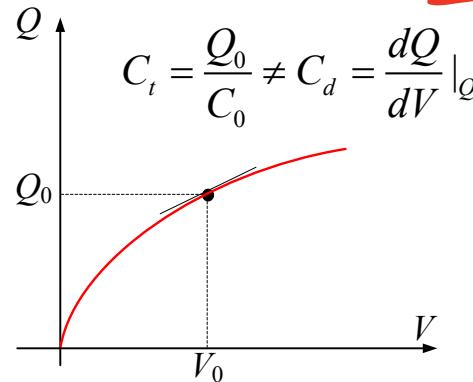
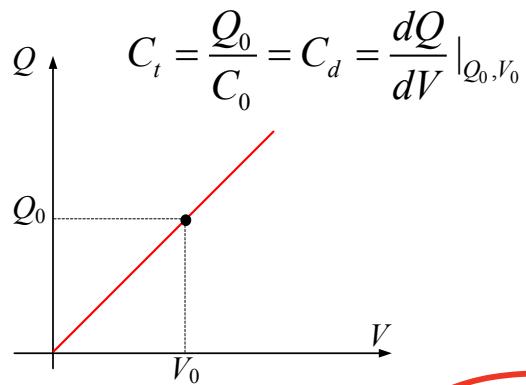


Often, datasheets provide C_{ds} measured for $V_{ds}=25$ V. That value can be used to calculate capacitance for any arbitrary V_{ds}

$$C_{ds}(V_{ds}) = C_{ds}(25) \sqrt{\frac{25 + V_B}{V_{ds} + V_B}} \approx \frac{5C_{ds}(25)}{\sqrt{V_{ds}}} \quad \text{if } V_{ds} \gg V_B$$

Losses Due to Charging - Discharging C_{oss}/C_{ds}

Two types of capacitance can be defined for a nonlinear capacitor, differential C_d and total C_t (for a linear capacitor, they are identical). Differential capacitances are reported in a datasheet as C_{iss} , C_{rss} , and C_{oss} .



$$\begin{aligned} i &= \frac{dQ}{dt} = C_d \frac{dV}{dt} \\ i &= \frac{dQ}{dt} = \frac{d(C_t V)}{dt} = C_t \frac{dV}{dt} + V \frac{dC_t}{dt} = \\ &= C_t \frac{dV}{dt} + V \frac{dC_t}{dV} \frac{dV}{dt} = \left(C_t + V \frac{dC_t}{dV} \right) \frac{dV}{dt} \\ C_d &= C_t + V \frac{dC_t}{dV} \end{aligned}$$

The charge stored in the drain-source junction capacitance at V_{DS} can be found as:

$$Q_j(v_{DS}) = \int_0^{v_{DS}} dQ_j = \int_0^{v_{DS}} C_{ds}(v_{DS}) dv_{DS} = C_{j0} \int_0^{v_{DS}} \frac{1}{\sqrt{1 + \frac{v_{DS}}{V_B}}} dv_{DS} = 2C_{j0}V_B \sqrt{1 + \frac{v_{DS}}{V_B}} \Big|_0^{v_{DS}} = 2C_{j0}V_B \sqrt{1 + \frac{v_{DS}}{V_B}} - 2C_{j0}V_B = 2C_{j0}V_B \left(\sqrt{1 + \frac{v_{DS}}{V_B}} - 1 \right)$$

$$v_{DS} \gg V_B \Rightarrow Q_j(v_{DS}) \approx 2C_{j0}V_B \sqrt{1 + \frac{v_{DS}}{V_B}} = 2(v_{DS} + V_B)C_{ds}(v_{DS})$$

The energy stored in the drain-source junction capacitance C_{ds} at v_{DS} :

$$W_j(v_{DS}) = \frac{1}{2} \int_0^{v_{DS}} Q_j dv_{DS} = 2C_{j0}V_B \int_0^{v_{DS}} \left(\sqrt{1 + \frac{v_{DS}}{V_B}} \right) dv_{DS} = \frac{2}{3} C_{j0} \sqrt{V_B} (v_{DS} + V_B)^{\frac{3}{2}} \Big|_0^{v_{DS}} = \frac{2}{3} C_{j0} V_B^2 \left(\left(1 + \frac{v_{DS}}{V_B} \right)^{\frac{3}{2}} - 1 \right) \approx \frac{2}{3} C_{j0} V_B^2 \left(1 + \frac{v_{DS}}{V_B} \right)^{\frac{3}{2}}$$

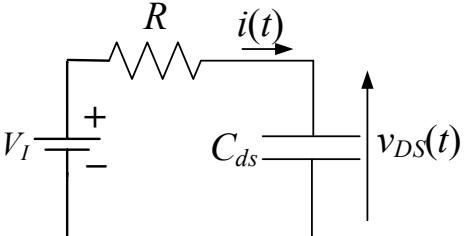
$$W_j(V_I) = \frac{2}{3} C_{ds}(V_I) V_I^2$$

I can not identify gate loss ⁵⁹

Losses Due to Charging - Discharging C_{oss}/C_{ds}

Charging loss

The energy transferred from the DC source V_I after the upper transistor is turned off (if a voltage source supplies the switch):



This is the average power loss when the transistor turns on and the capacitor is discharged through r_{DS}

The energy lost in the resistance of the **charging path** during the charging process of the capacitance C_{ds} from a voltage source

The corresponding power associated with charging the C_{ds}

The total switching power loss per transistor when supplied from a voltage source:

Equivalent linear capacitance C_{eq} $fC_{eq}V_I^2 = 2fC_{ds}(V_I)V_I^2$

$$W_I(V_I) = \int_0^{V_I} V_I idt = V_I \int_0^{V_I} idt = V_I Q_j(V_I)$$

$$= V_I 2(V_I + V_B) C_{ds}(V_I) \approx 2C_{ds}(V_I) V_I^2$$

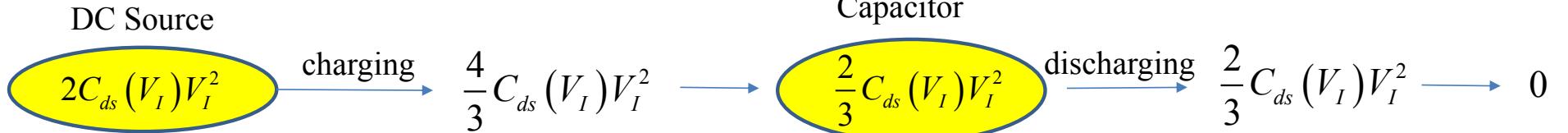
$$P_{turn-on} = fW_j(V_I) = \frac{2}{3} fC_{ds}(V_I) V_I^2$$

$$W_{char} = W_I(V_I) - W_j(V_I) = \frac{4}{3} C_{ds}(V_I) V_I^2$$

$$P_{char} = fW_{char}(V_I) = \frac{4}{3} fC_{ds}(V_I) V_I^2$$

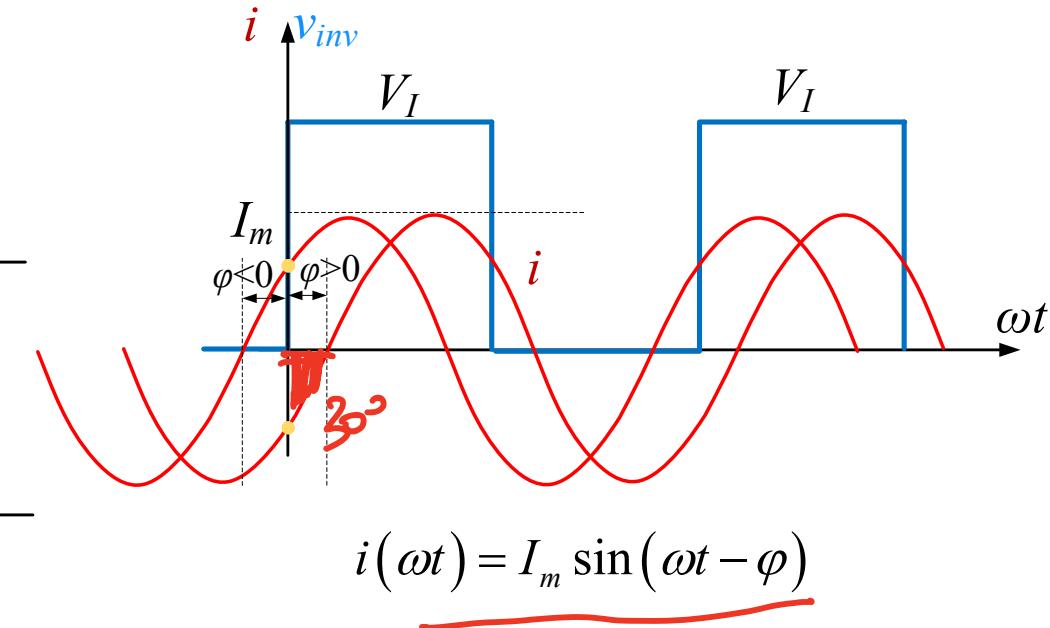
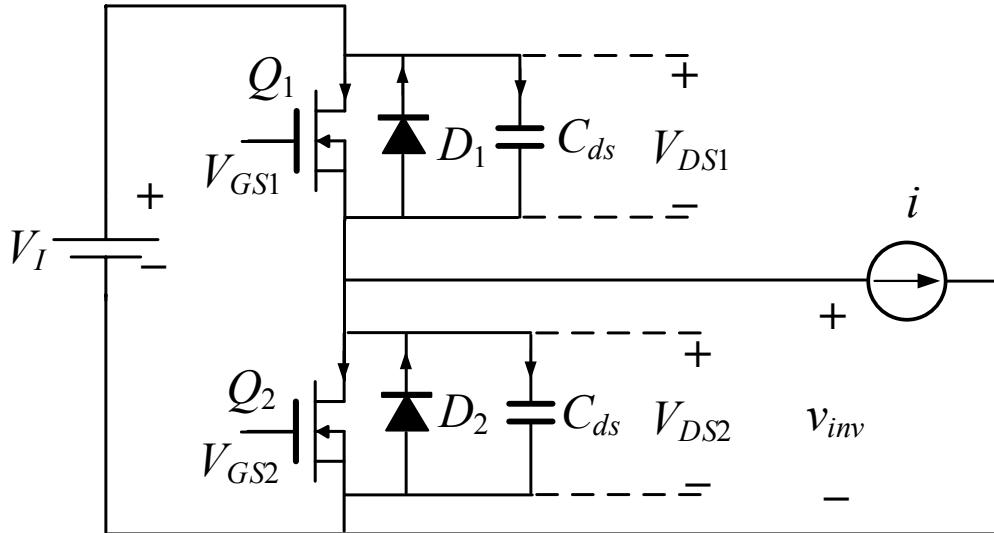
$$P_{sw} = fW_I(V_I) = 2fC_{ds}(V_I) V_I^2$$

$$\boxed{C_{eq} = 2C_{ds}(V_I)}$$



Switching Losses in a Half-Bridge Inverter

Let us study switching losses in a half-bridge, voltage-fed (voltage-source) inverter with the sinusoidal load current:

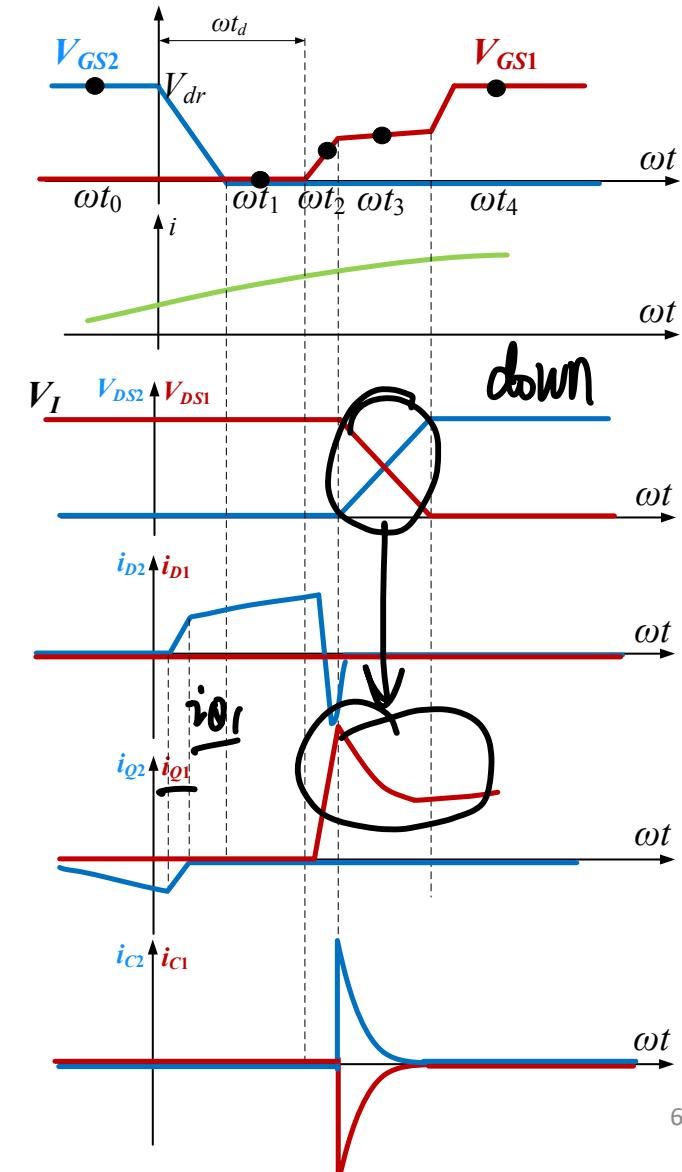
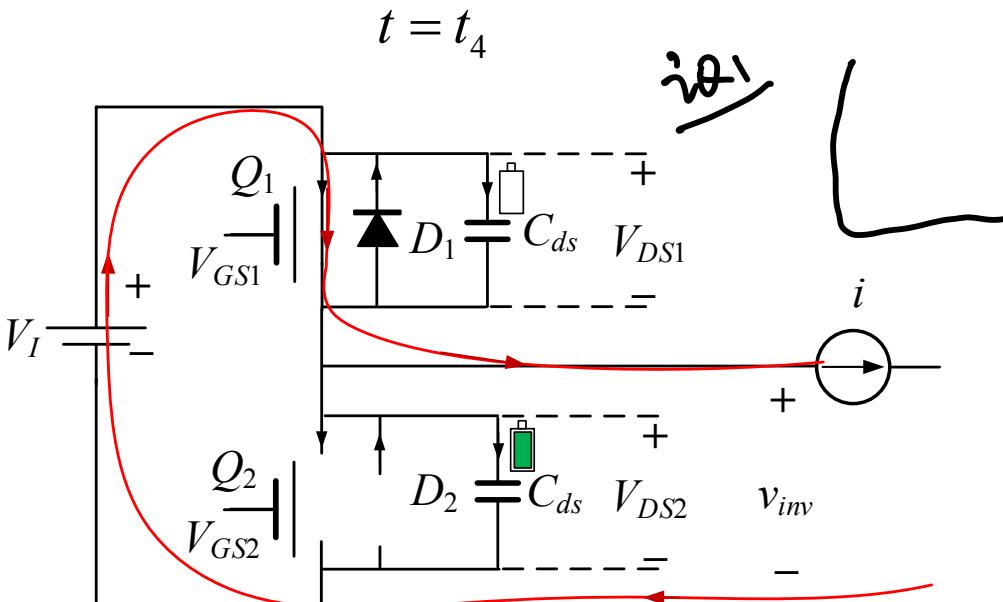


- $\varphi > 0$ – current is lagging the voltage, $\varphi < 0$ – current is leading the voltage
- Phase angle determines POLARITY of the current at the switching instant: ($\varphi > 0 \rightarrow i(0) < 0$, $\varphi < 0 \rightarrow i(0) > 0$)
- We will study only one of the two switching intervals. Due to sinusoidal current, the second switching transition is symmetrical in terms of waveforms and identical in terms of switching losses.

Switching Losses in a HB Inv. – Leading Current

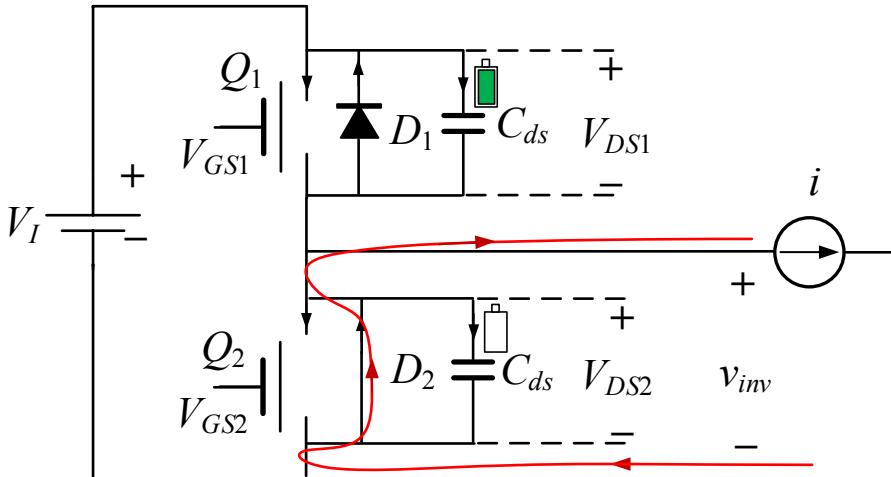
Let us first study the case when the current i is leading the voltage v_{inv}

$$\varphi < 0 \Rightarrow i(0) = I_m \sin(-\varphi) > 0$$

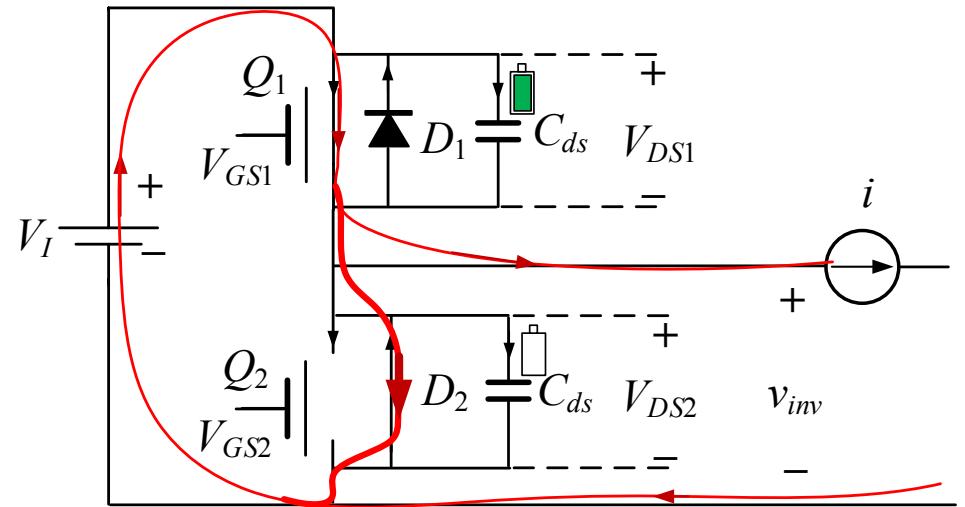


Switching Losses in a Half-Bridge Inverter – Leading Current

$t = t_1$

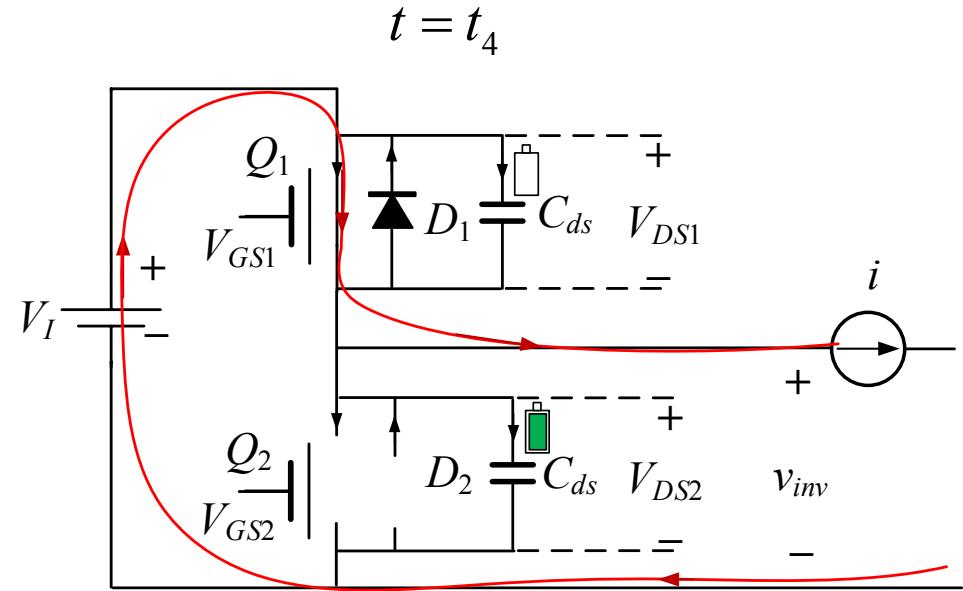
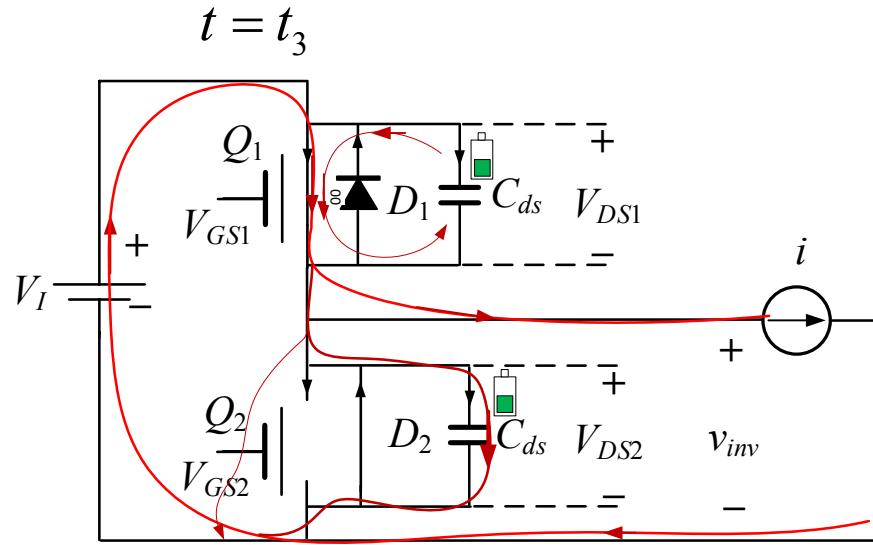


$t = t_2$



kind of

Switching Losses in a Half-Bridge Inverter – Leading Current



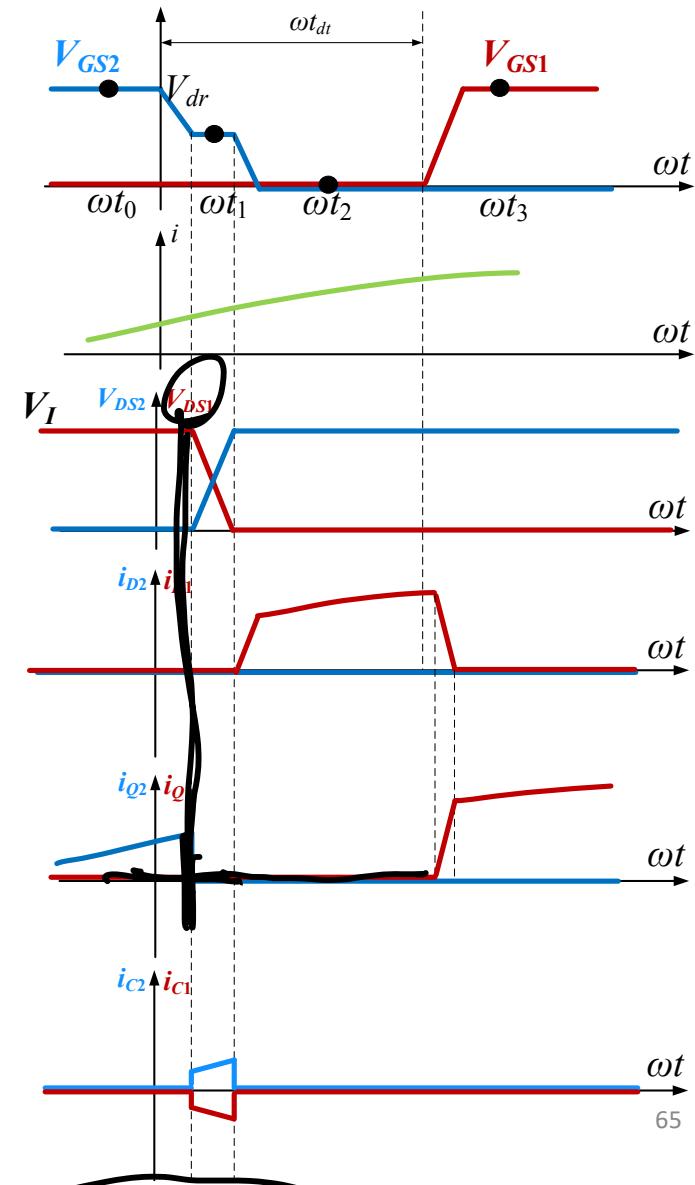
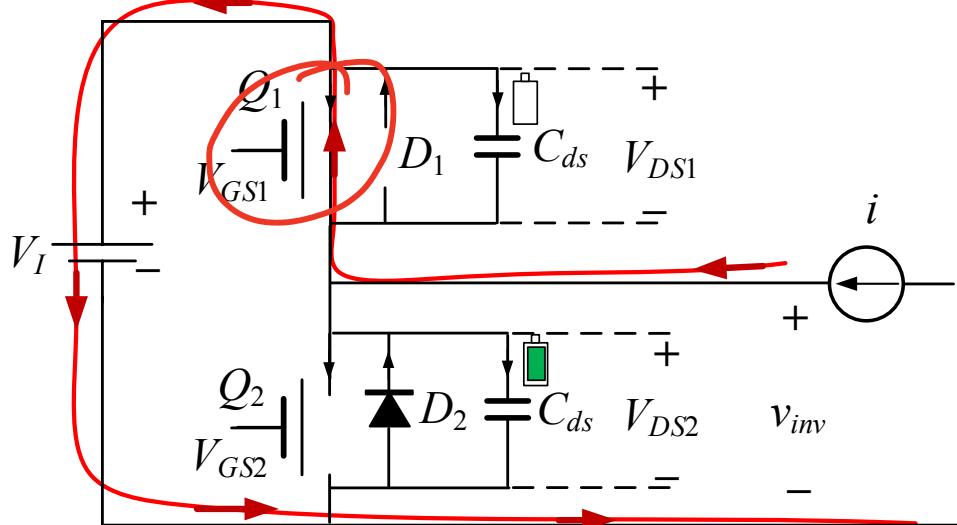
	V-I Overlapping	Reverse Recovery	C_{oss} charge-discharge	Gate circuit loss	Miller's effect
Turn-off	No	No	No	Yes	No
Turn-on	Yes	Yes	Yes	Yes	Yes

This losses should be multiplied by 2 for HB and by 4 for FB structures

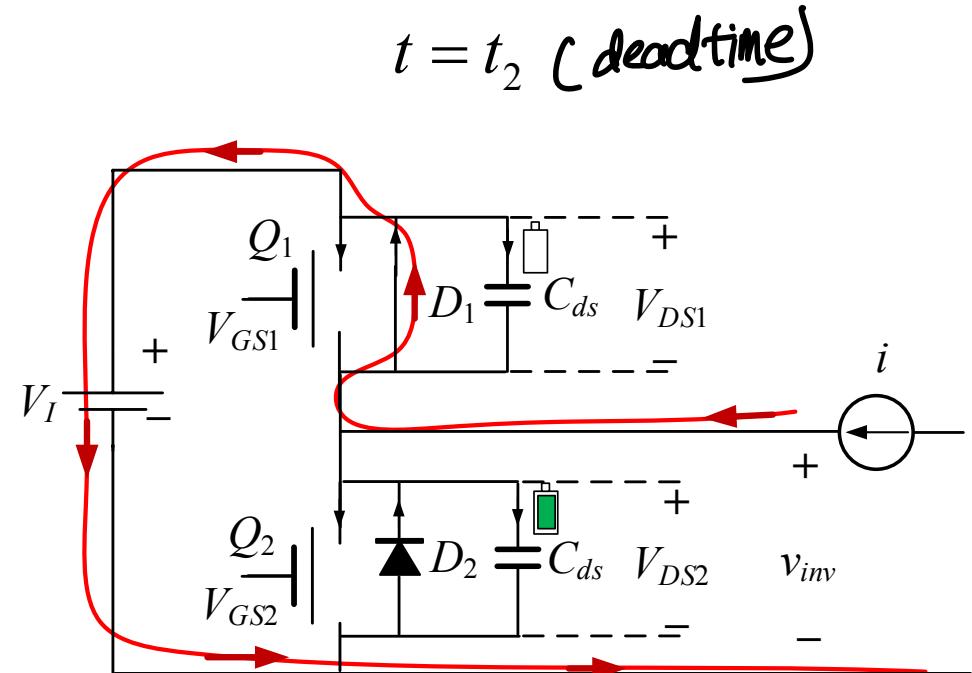
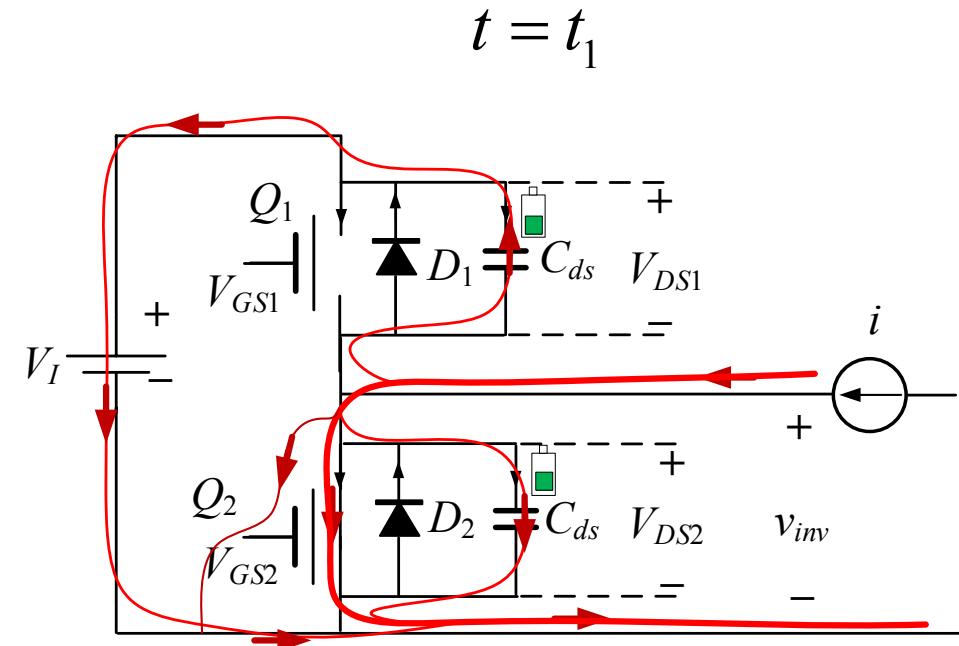
Switching Losses in a HB Inv. – Lagging Current

Let us now study the case when the current i is lagging the voltage v_{inv}

$$\varphi > 0 \Rightarrow i(0) = I_m \sin(-\varphi) < 0 \quad \text{It is literally for the top one}$$



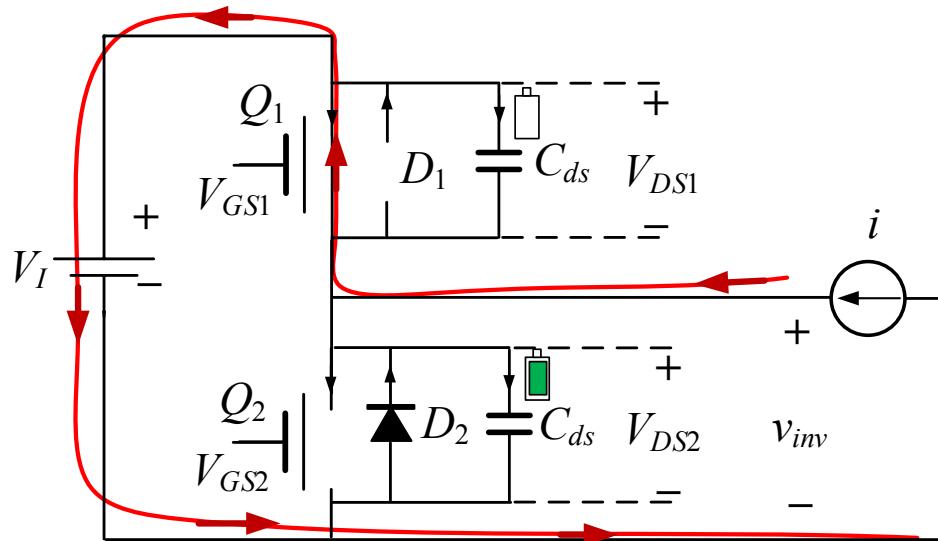
Switching Losses in a Half-Bridge Inverter - Lagging Current



Lagging current | voltage lead,

Switching Losses in a Half-Bridge Inverter – Lagging Current

$$t = t_3$$



	V-I Overlapping	Reverse Recovery	C_{oss} charge-discharge	Gate circuit loss	Miller's effect
Turn-off	No	No	No	Yes	No
Turn-on	No	No	No	Yes	No

This losses should be multiplied by 2 for HB and by 4 for FB structures

Condition for ZVS Switching

Current should be able to provide enough charge to maintain ZVS turn on!

Charge the load current can provide during dead time:

$$Q_I = - \int_0^{t_d} I_m \sin(\omega t - \varphi) dt = - \frac{I_m}{\omega} (\cos \varphi - \cos(\varphi - \omega t_d))$$

Charge one capacitor needs to flip its voltage from 0 to V_I or vice versa

$$Q_j(v_{DS}) = 2(v_{DS} + V_B)C_{ds}(v_{DS}) \Rightarrow Q_j(V_I) = 2C_{ds}(V_I)(V_I + V_B)$$

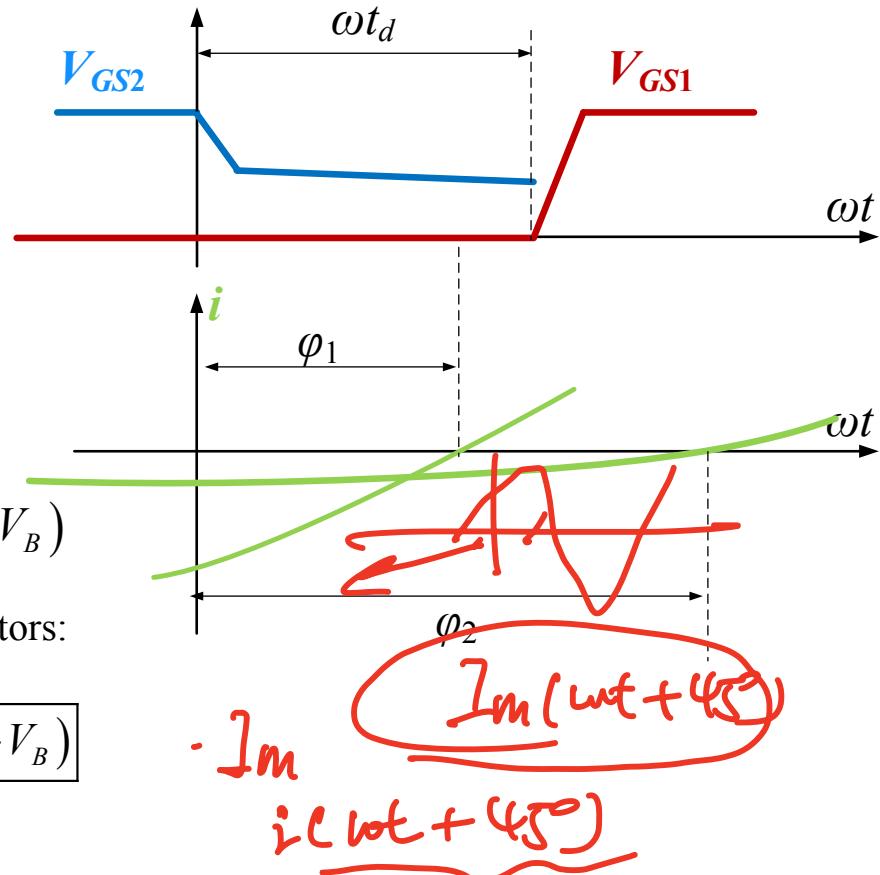
Load current charge should be enough to charge and discharge two capacitors:

$$Q_I > 2Q_j(V_I) \Rightarrow -I_m (\cos \varphi - \cos(\varphi - \omega t_d)) > 4\omega C_{ds}(V_I)(V_I + V_B)$$

Minimum dead time to guarantee a ZVS turn-on:

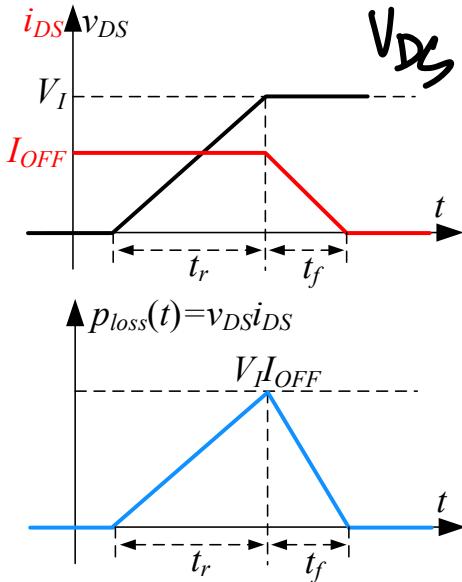
$$\cos \varphi + \frac{4\omega C_{ds}(V_I)}{I_m}(V_I + V_B) < \cos(\varphi - \omega t_d) \Rightarrow$$

$$\omega t_{d,\min} > \varphi - \cos^{-1} \left(\cos \varphi + \frac{4\omega C_{ds}(V_I)}{I_m}(V_I + V_B) \right)$$



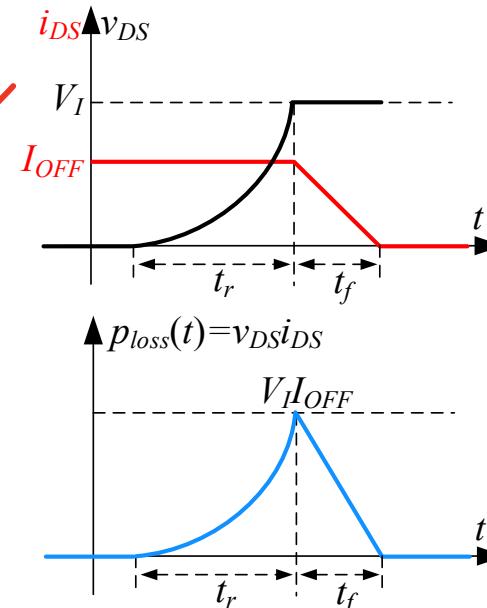
Modified VI Overlapping Switch Loss due to nonlinear C_{ds}

- Due to nonlinear C_{oss} , the v_{DS} voltage waveform is not linear as we assumed before. It increases slower at low v_{DS} values and much faster for higher v_{DS} . This is because the MOSFET output capacitance is highly nonlinear, and it is much larger at low v_{DS} voltage than at high v_{DS} voltage. The current that charges this capacitance is assumed to be constant.
- Let us analyze this modification on the example of switch turn-off transition:



$$I = C_{ds} (v_{DS}) \frac{dv_{DS}(t)}{dt}$$

turn off stage



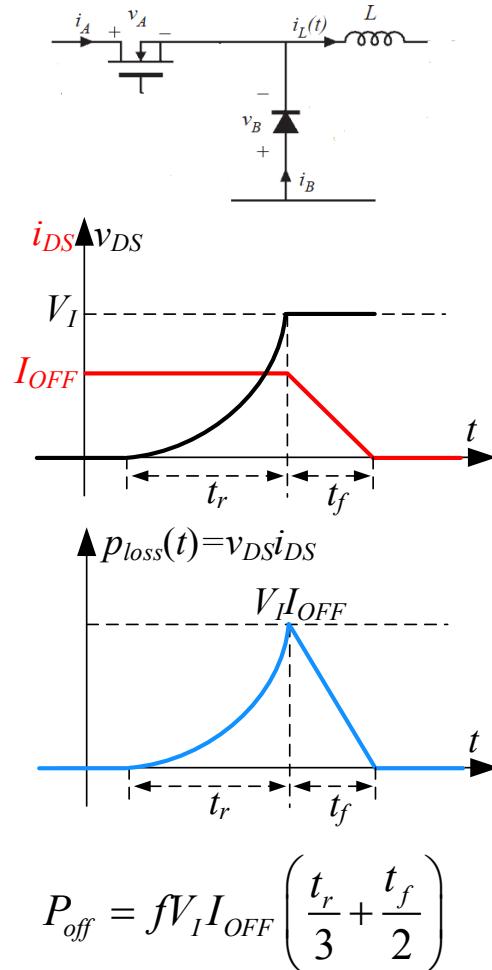
$$P_{off} = \frac{1}{T_s} \int_0^{T_s} p_{loss}(t) dt = \boxed{fV_I I_{OFF} \left(\frac{t_r}{2} + \frac{t_f}{2} \right)}$$

$$P_{off} = \frac{1}{T_s} \int_0^{T_s} p_{loss}(t) dt = \boxed{fV_I I_{OFF} \left(\frac{t_r}{3} + \frac{t_f}{2} \right)}$$

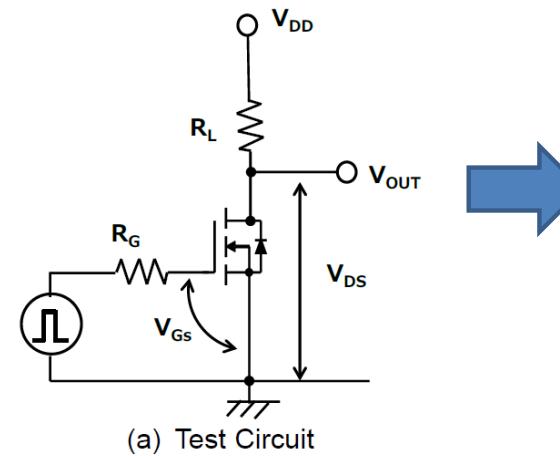
Derivation details: Course Textbook, Section 6.7.3

Analytical Calculation of VI Overlapping Switch Loss using Datasheet Data

What we need:



What the datasheet provides:

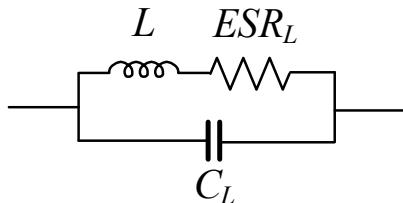


Turn-on delay time	$t_{d(on)}$	$V_{DD}=100\text{ V}, V_{GS}=10\text{ V}, I_D=12\text{ A}, R_G=1.6\Omega$	-	10	-	ns
Rise time	t_r		-	10	-	
Turn-off delay time	$t_{d(off)}$		-	22	-	
Fall time	t_f		-	8	-	

$$P_{overlap} = fV_I I_{OFF} \left(\frac{t_r}{3} \cdot \frac{V_I}{V_{test}} \right) \quad \text{or} \quad P_{overlap} = fV_I I_{OFF} \left(\frac{t_f}{3} \cdot \frac{V_I}{V_{test}} \right)$$

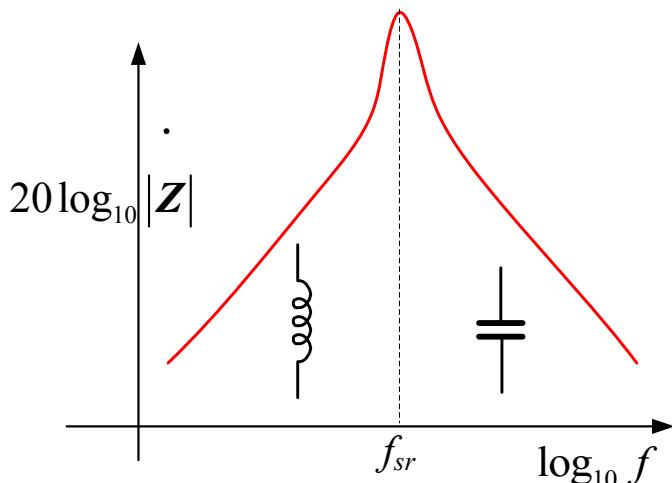
Modeling a Real Inductor

- Model of a real inductor includes the inductance L , Equivalent Series Resistance (ESR_L), and parasitic capacitance C_L



$$Z = \frac{ESR_L + j\omega_s L}{1 - \omega_s LC_L + jESR_L \omega_s C_L}$$

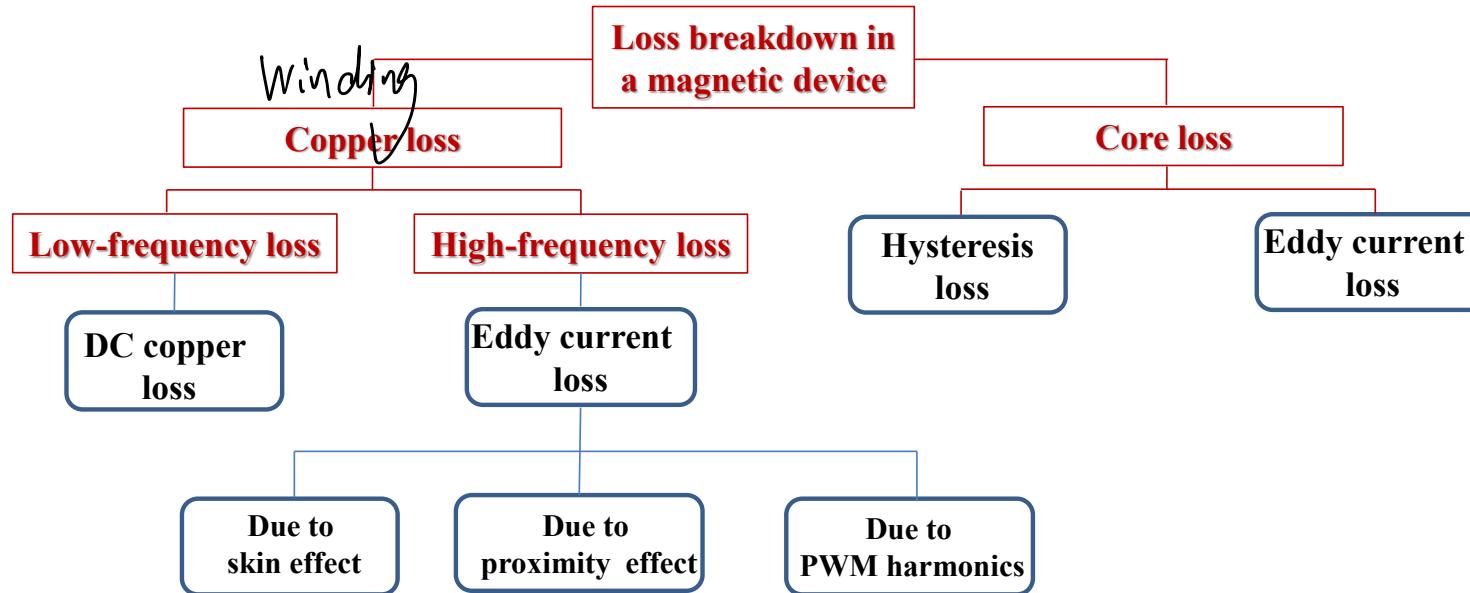
- C_L models the parasitic capacitance between turns.
- Inductor impedance as a Bode Plot:



- The designer should assure that the inductor operates below its self-resonant frequency.
- Self-resonant frequency:
$$f_{sr} = \frac{1}{2\pi\sqrt{LC_L}}$$
- Parasitic capacitance is usually very small, and the resonant frequency is typically much higher than the switching frequency.

Modeling a Real Inductor

- Losses in inductors cannot typically be neglected.
- Losses in an inductor have a complex structure:



- **Coil DC resistance** is given by $ESR_{L,dc} = \rho \frac{l_w}{A_w}$

l_w – the wire length

A_w – the bare cross-sectional area

- Resistivity changes significantly with temperature:

Soft-annealed cooper	T=25°C	T=100°C
Resistivity [Ωcm]	1.724*10 ⁻⁶	2.3*10 ⁻⁶

Modeling a Real Inductor

Hysteresis

Core loss: hysteresis loss

- Hysteresis loss is directly proportional to applied frequency, core volume, and the size of the hysteresis loop:

$$P_H = fW_H = f(A_c l_m) \int_{\text{one cycle}} H(t) dB(t)$$

Core volume The B-H loop area

? I don't understand this part ???

- For the power loss density, the empirical Steinmetz equation is typically used:

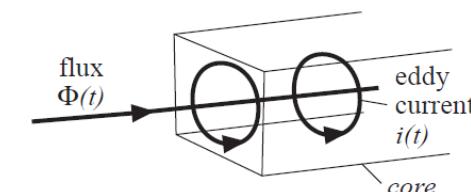
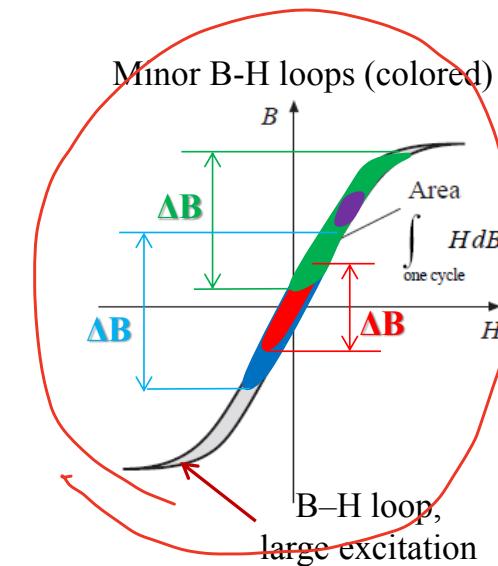
$$p_H = \frac{P_H}{A_c l_m} = f \int_{\text{one cycle}} H(t) dB(t) \approx f K_H (\Delta B)^\alpha \left[\frac{W}{m^3} \right]$$

- Parameters K_H and α are typically determined experimentally

Core loss: eddy current loss

- Except ferrites, magnetic core materials are **reasonably good conductors** of electric current
- According to Lenz's law, magnetic fields within the core induce currents ("**eddy currents**") to **flow within the core**.
- Eddy currents generate flux which opposes changes in the core flux to **prevent it from penetrating the core** (core shielding)
- Steinmetz equation describes power loss density for eddy current loss in a core:

$$p_E = \frac{P}{A_c l_m} \approx K_E f^2 (\Delta B)^2 \left[\frac{W}{m^3} \right]$$



Modeling a Real Inductor

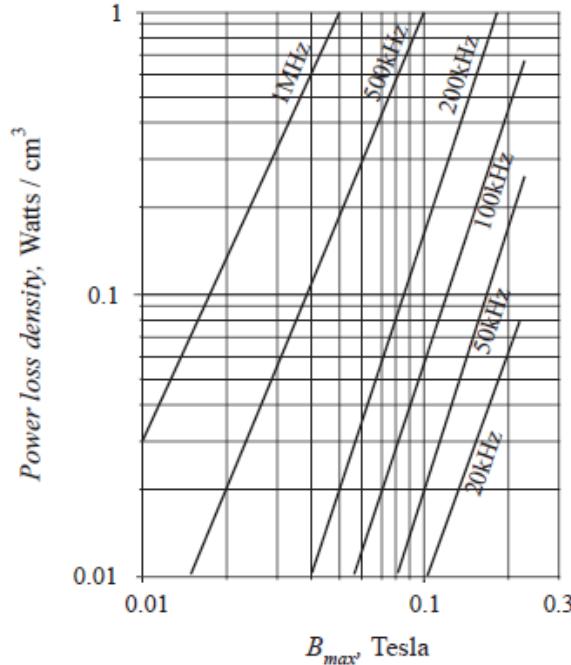
Total core loss:

- Empirical Steinmetz equation:

$$P_{fe} \approx (A_c l_m) K_{fe}(f)(\Delta B)^\beta [W]$$

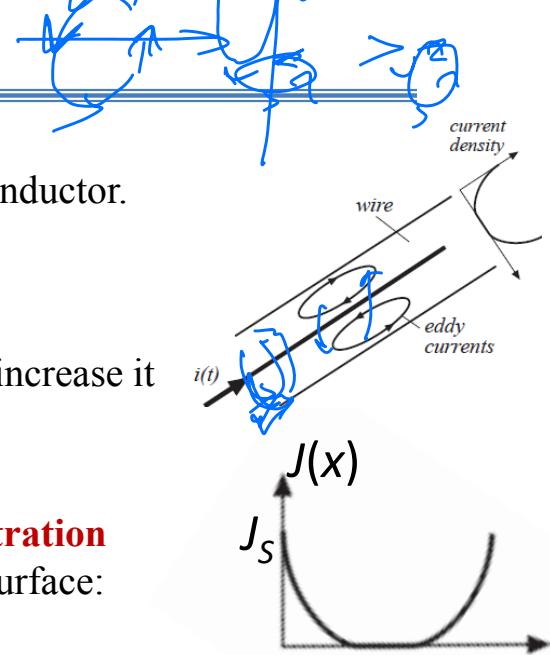
- or:

$$P_{fe} \approx (A_c l_m) K_{fe,0} f^\alpha (\Delta B)^\beta [W]$$



- Powdered cores made of hydrogen reduced iron have higher permeability but lower Q; used for EMI filters and low-frequency chokes. Iron powdered cores are produced by gluing small particles using nonconductive epoxy resin. Typical shape – toroid.
- Ferrites are ceramic compounds of the transition metals (Zink, Nickel, Manganese) with oxygen; ~~ferromagnetic but nonconductive~~ (ceramic is insulation). Low eddy current losses, but hysteresis losses can still occur - ~~Manganese-Zinc~~ (below 1 MHz); Nickel-Zink above 1MHz; Very fragile and brittle.
- For very high-frequency resonant converters, coreless inductors are often used.
- Interleaved converter designs can reduce the core losses, too.

Modeling a Real Inductor



High-frequency copper loss: skin effect *increase resistance R*

- Current $i(t)$ flows through the conductor and creates the magnetic field INSIDE the conductor.
- Field lines follow the circular part and penetrate the conductor's material.
- Eddy current appears, and their field opposes the external field.
- The direction of the eddy current tends to reduce the current density in the center and increase it near the conductor's surface.
- Current density is governed by Maxwell's equations
- The characteristic parameter related to this phenomenon is called **skin depth or penetration depth δ** , after which $J(x)$ reduces to 37% ($1/e$) of maximum current density J_s at the surface:

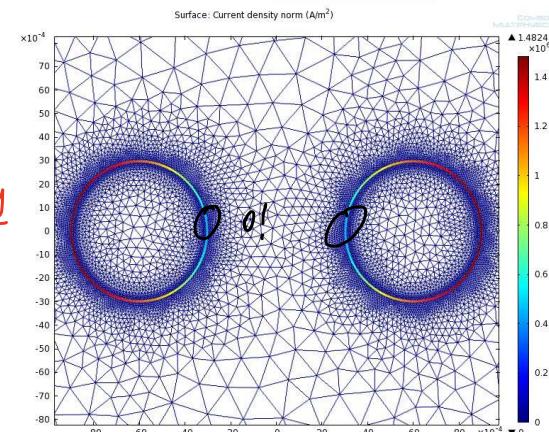
$$J(x) = J_s e^{-\frac{x}{\delta}}$$

$$\delta(f) = \sqrt{\frac{\rho}{\pi f \mu}}$$

$$\delta_{cu, T=100^0C}(f) = \frac{7.5}{\sqrt{f}} [\text{cm}]$$

High-frequency copper loss: proximity effect

- AC current in a conductor induces eddy currents in adjacent conductors through a phenomenon called **proximity effect**
- Proximity effect causes significant power loss in the windings of high-frequency transformers and AC inductors.



Modeling a Real Inductor

Remedy for Skin and Proximity effects: Use of Litz wire and twisted strands

LITZ WIRE - A way to increase conductor area while maintaining low skin-effect losses

- Many strands of small-gauge wire are bundled together and are externally connected in parallel
- **Strands are twisted** so that each strand passes equally through each position inside and outside the bundle. This prevents the circulation of currents between strands.
- **Strand diameter should be sufficiently smaller** than the skin depth
- The Litz wire bundle itself is composed of multiple layers
- Advantage: when properly sized, it can significantly reduce proximity loss
- Disadvantage: **increased cost and decreased amount of copper** within the core window

Why twisted them?

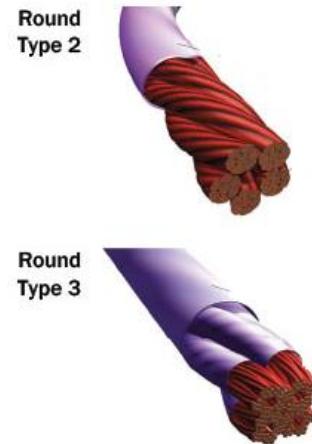
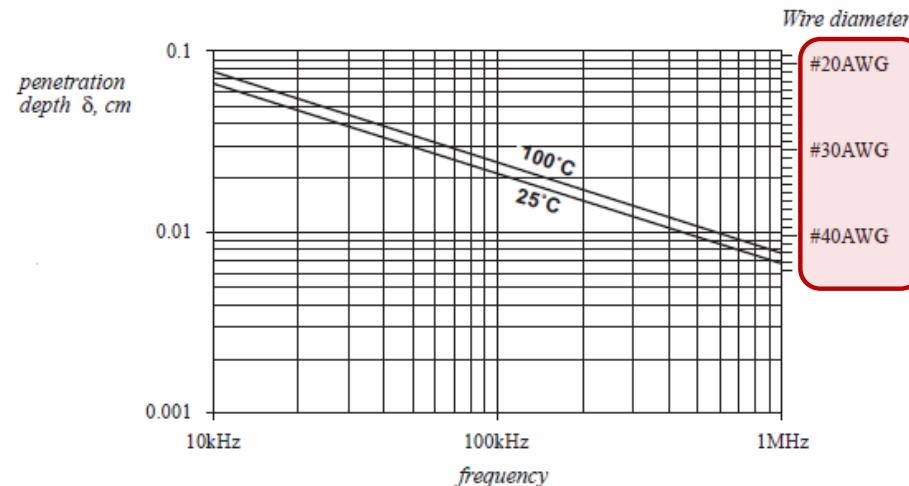


Figure credit

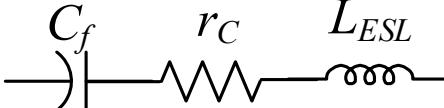
<http://newenglandwire.com>

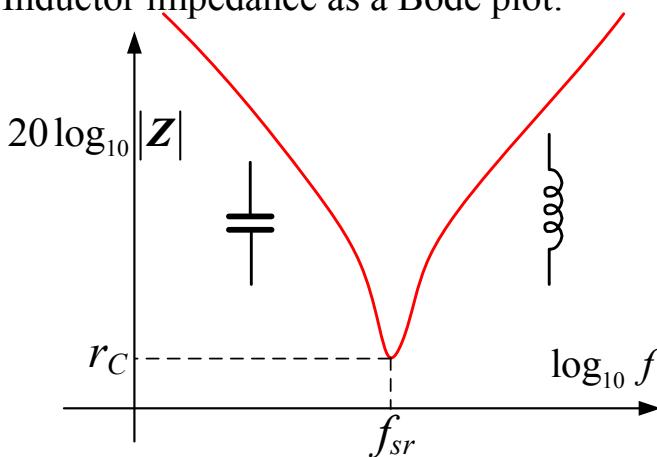


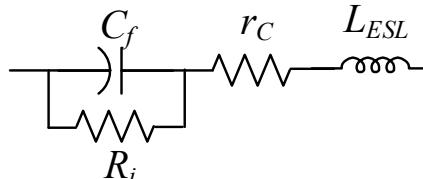
Equivalent standard American Wire Gauge conductors whose diameter d is equal to skin depth δ



Modeling a Real Capacitor

- Model of a real capacitor includes the capacitance C , Equivalent Series Resistance (r_c), and parasitic inductance L_{ESL}
- 
- $$Z = \frac{1}{j\omega C_f} + j\omega L_{ESL} + r_c \Rightarrow |Z| = \sqrt{r_c^2 + \left(\omega L_{ESL} - \frac{1}{\omega C_f}\right)^2}$$
- L_{ESL} (equivalent series inductance - *ESL*) models the parasitic inductance due to capacitor's internal connectors, plates, and terminals.
 - SMD capacitors have smaller *ESL* than through-hole capacitors. *ESL* strongly depends on the size of the capacitor package: the smaller the package, the lower the ESL is. Typically values for different packages are: 0402 - 0.7 nH, 0603 - 0.9 nH, and 0805 - 1.2 nH.
 - Inductor impedance as a Bode plot:

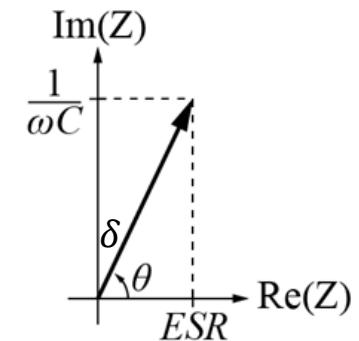
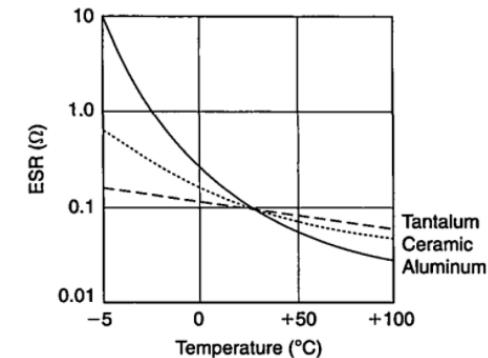


- Self-resonant frequency: $f_{sr} = \frac{1}{2\pi\sqrt{L_{ESL}C_f}}$
 - When it is important to describe the ability of a capacitor to hold its charge, insulation resistance is added to the model:
- 
- Typical range of R_i is 10 kΩ to 1 GΩ; R_i should be considered when the capacitor voltage is high (typically over 200 V).

Modeling a Real Capacitor

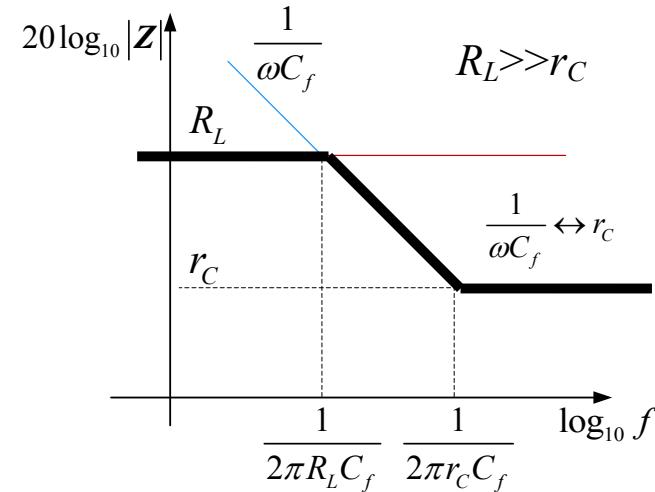
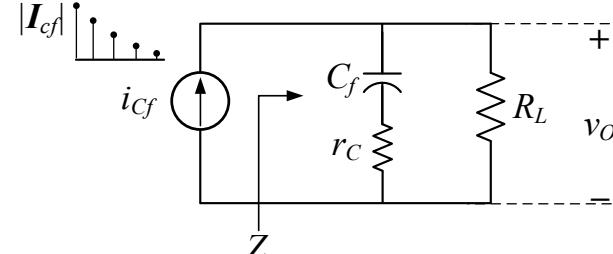
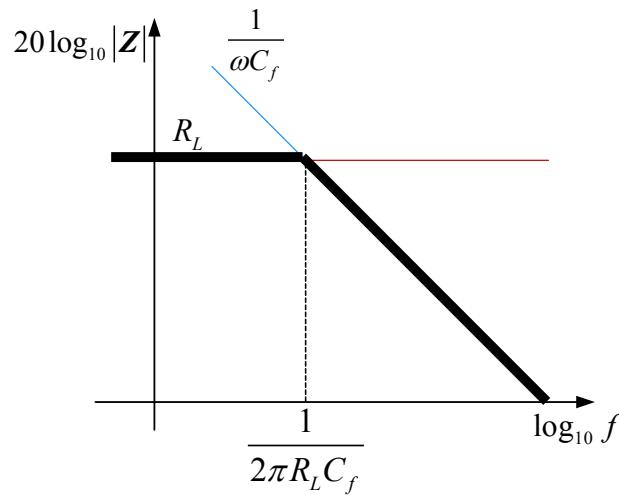
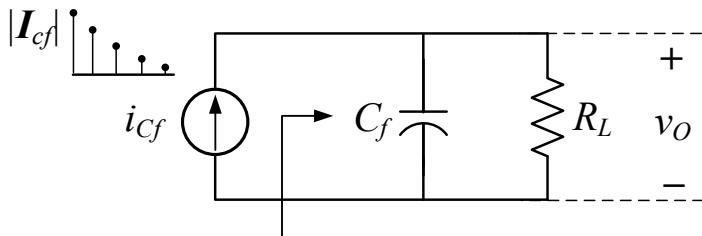
- Two main types of capacitors are used in Resonant Power Converters:
 - Electrolytic capacitors (aluminum or tantalum).
 - Ceramic Capacitors (CC) – referring to Class I C0G type, typically multilayer (ML) form.
- Electrolytic capacitors are polarized capacitors, and they are typically used as filtering/energy storage capacitors. They have very large energy density ($5\text{-}6 \text{ J/cm}^3$) and relatively high ESR ($40 \text{ m}\Omega$ - 2Ω) and ESL ($>10 \text{ nF}$ – through-hole components). Maximum operation temperature is low (typically $85\text{-}105^\circ\text{C}$) due to accelerated evaporation of the dielectric.
- MLCCs have a much lower energy density ($<0.5 \text{ J/cm}^3$) but also much lower ESR and ESL ($<5 \text{ nF}$ through-hole and below 2 nF SMD). The capacitance value is very stable with temperature (e.g., $\pm 30 \text{ ppm}$ for the range from -55°C to $+85^\circ\text{C}$) and does not depend on capacitor voltage
- ESR is temperature dependent, as shown in the figure
- For MLCCs, the product between ESR and capacitance is approximately constant for a wide range of values
- ESR is highly frequency dependent. Therefore, manufacturers more often use **loss factor D** to describe the loss, since it proved to be less dependent on f (δ is typically called loss angle):

$$D = \tan(\delta) = \frac{ESR}{1/\omega C} \rightarrow ESR = D/\omega C$$



Modeling a Real Capacitor

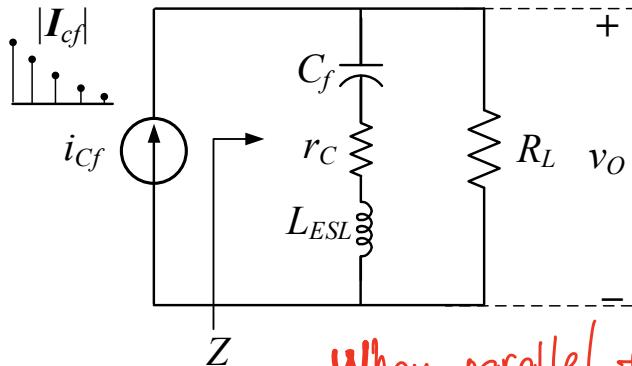
- It is not uncommon that the self-resonance of a capacitor is low, particularly for electrolytic capacitors. Let us understand the impact that parasitics have on the filtering characteristics of a real capacitor.
- We will apply the method of asymptotes to plot the approximate magnitude Bode plot of the filter impedance (studied in Section 8.3 and 8.4 Erickson, Maksimovic textbook – review if necessary)



$$Z = R_L \parallel r_C \frac{s + \frac{1}{C_f r_C}}{s + \frac{1}{C_f (R_L + r_C)}}$$

Modeling a Real Capacitor

- Bode plots of the impedance for the case when the ESL is included in the model:



$$WL = \frac{1}{\sqrt{C}}$$

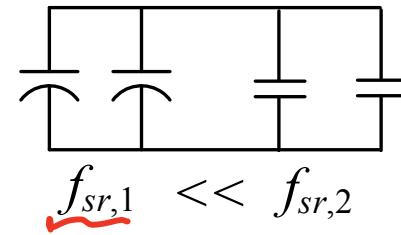
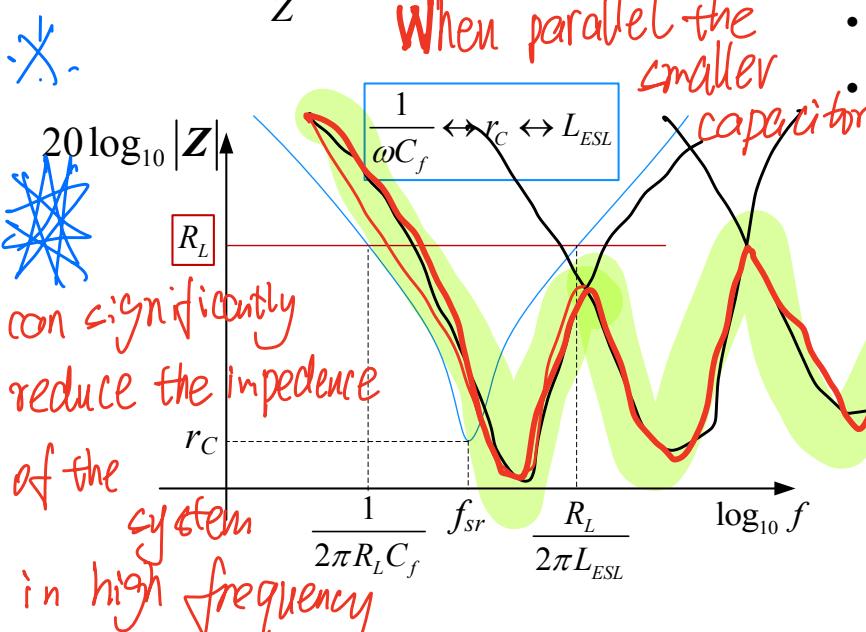
$$\omega^2 = \frac{1}{LC}$$

$$Z = R_L \frac{1 + sr_c C_f + s^2 L_{ESL} C_f}{1 + s(r_c + R_L) C_f + s^2 L_{ESL} C_f}$$

- Due to L_{ESL} , the high-frequency current harmonics will not be filtered. High-frequency $|Z|$ increases back to the R_L value, reducing the filtering effect.

$$f_{sr} = \frac{1}{2\pi\sqrt{LC}}$$

- All important harmonics should be below f_{sr} .
- Electrolytic capacitors have low f_{sr} , and they are often combined with smaller ceramic capacitors with smaller ESR and ESL. Those capacitors have lower current ratings, but they are intended only to filter higher harmonics.



- For a detailed derivation, read Section 2.6 from the course textbook

Figures of Merits of Resonant Power Converters

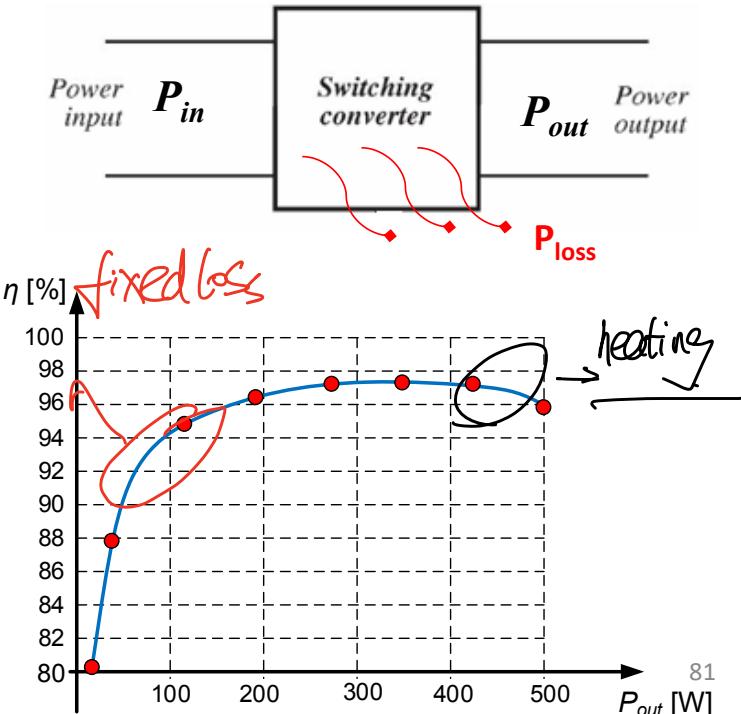
- Variables used to evaluate topology suitability and performance of a Resonant Power Converter are:
 - Efficiency η
 - Current and voltage component stresses
 - Power-output capability c_P
 - Input signal Power Factor (PF)
 - Input signal Total Harmonic Distortion (THD) coefficient

Efficiency η

Efficiency calculation:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} = 1 - \frac{P_{loss}}{P_{in}}$$

- High efficiency impacts all other objectives due to reduced cooling requirements:
 - Reduces size, weight, and increases power density: up to 15 kW/dm³ (discrete solutions), 20-30 kW/dm³ (integrated high freq. solutions); Laboratory prototypes over 50 kW/dm³ (EVs)
 - Reduces cost
 - Saves energy
- Efficiency typically drops for low output power due to fixed, power-independent losses in the converter.



Figures of Merits of Resonant Power Converters

Current and voltage stress of switching components

- Peak (maximum) values of the voltage and current $V_{sw,M}$ and $I_{sw,M}$ during one period of operation in steady-state. No safety margin is included.

Power-Output capabilities c_P

$$c_P = \frac{P_O}{V_{sw,M} I_{sw,M}}$$

where P_O is the output power, $V_{sw,M}$ and $I_{sw,M}$ are the peak voltage and current of the converter switch.

Input signal Power Factor (PF)

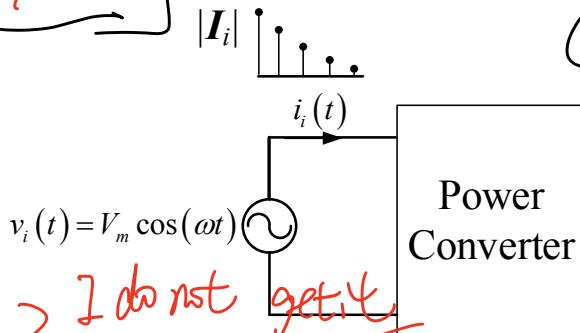
- (TRUE) Power Factor (PF) is defined as the ratio of real power in (W) and the apparent power in (VA)

$$PF = \frac{\text{Input Real Power}}{\text{Input Apparent Power}} = \frac{P_i}{S_i} = \frac{V_{rms} I_{rms} \cos\phi}{V_{rms} I_{rms}} = \cos\phi$$

- Two special cases of interest are when the converter is supplied from
 - ideal voltage source
 - ideal current source
- In that case, the input real power is delivered only by the first harmonic

Figures of Merits of Resonant Power Converters

?????

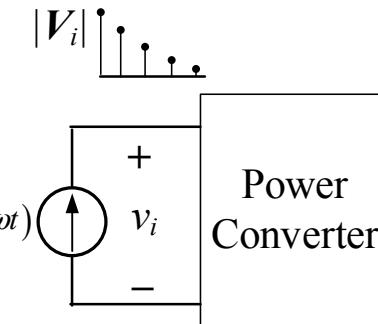


$$(\sqrt{V_1^2 + V_2^2 + V_3^2}) \cos \phi$$

0 $\sqrt{V_2^2 + V_3^2 + V_4^2}$

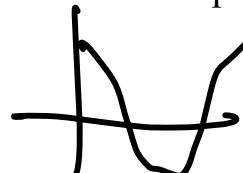
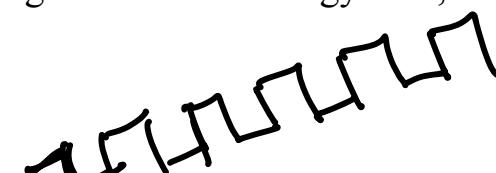
RMS - not mean square
有效值

$$\begin{aligned} TPF &= \frac{P_i}{S_i} = \frac{V_{i,rms} I_{i,rms,1} \cos \phi_1}{V_{i,rms} I_{i,rms}} = \frac{I_{i,rms,1} \cos \phi_1}{I_{i,rms}} = \\ &= \frac{I_{i,rms,1}}{\sqrt{I_0^2 + I_{i,rms,1}^2 + I_{i,rms,2}^2 + I_{i,rms,3}^2 + \dots}} \cos \phi_1 < \text{lower} \end{aligned}$$



$$\begin{aligned} TPF &= \frac{P_i}{S_i} = \frac{V_{i,rms,1} I_{i,rms} \cos \phi_1}{V_{i,rms} I_{i,rms}} = \frac{V_{i,rms,1} \cos \phi_1}{V_{i,rms}} = \\ &= \frac{V_{i,rms,1}}{\sqrt{V_0^2 + V_{i,rms,1}^2 + V_{i,rms,2}^2 + V_{i,rms,3}^2 + \dots}} \cos \phi_1 \end{aligned}$$

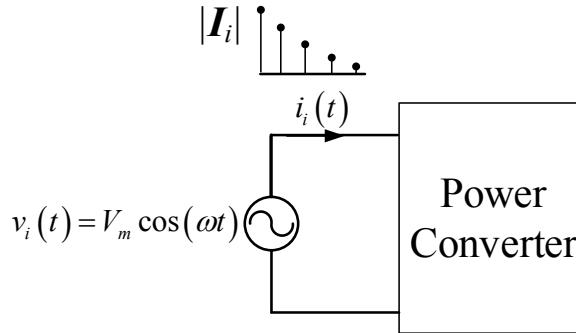
- Utilities typically charge an additional cost to commercial customers for a $TPF < 0.9$.
- To be designated as an Energy Star, PC chargers must have a power factor greater than 0.9 at 100% of the rated power.



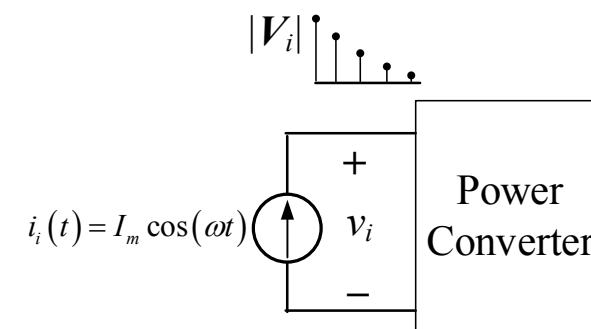
Figures of Merits of Resonant Power Converters

Input signal Total Harmonic Distortion (THD) coefficient

- **TOTAL HARMONIC DISTORTION (THD)** is the measure of the harmonic distortion present in a signal and is defined as the ratio of the sum of powers of all harmonic components to the power of the fundamental frequency



$$THD_I = \frac{\sqrt{I_0^2 + I_{i,rms,2}^2 + I_{i,rms,3}^2 + \dots}}{I_{i,rms,1}} = \sqrt{\frac{1}{TPF^2} - 1}$$



$$THD_V = \frac{\sqrt{V_0^2 + V_{i,rms,2}^2 + V_{i,rms,3}^2 + \dots}}{V_{i,rms,1}} = \sqrt{\frac{1}{TPF^2} - 1}$$

- US MIL-STD-461B: for loads of 1kW or greater, no current harmonic magnitude may be greater than 3% of the fundamental magnitude, and harmonics should decay faster than $1/n$, where n is the harmonic order
- IEC 61000-3-2 Electromagnetic compatibility (EMC) – Part 3-2 standard is used in Europe for loads below 16 A – it sets the maximum harmonic current levels up to 40th harmonic
- IEEE STD 519-2014: Recommends harmonic limits for voltage and current distortion at the point of common coupling (PCC) and defines measurement procedures