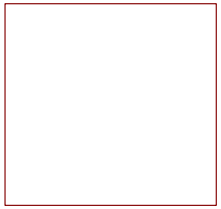
PRISM

Sensors

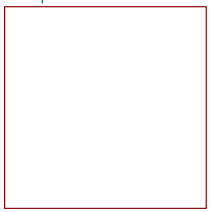


File: sensors.kicad_sch

Power

File: power.kicad_sch

Peripherals



File: LCD50.kicad_sch

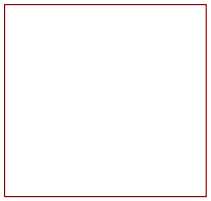
USB

File: USB.kicad_sch

DDR3

File: DDR3.kicad_sch

Audio



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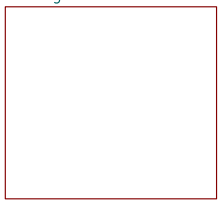
Storage



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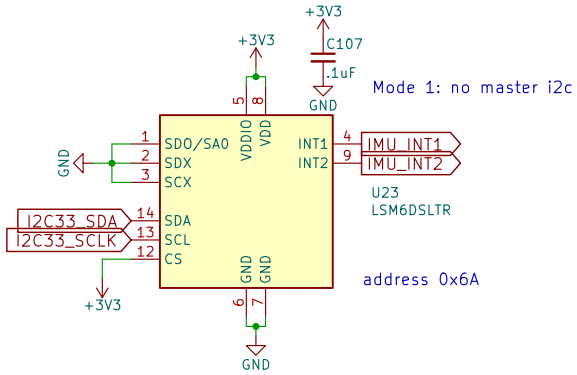
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.9		Id: 1/8

Sensors



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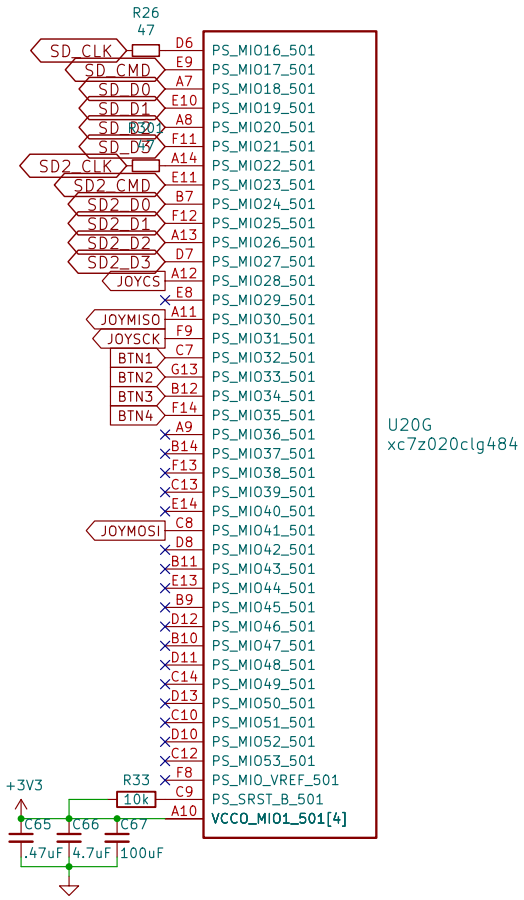
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.9		Id: 2/8

USB Host and Device



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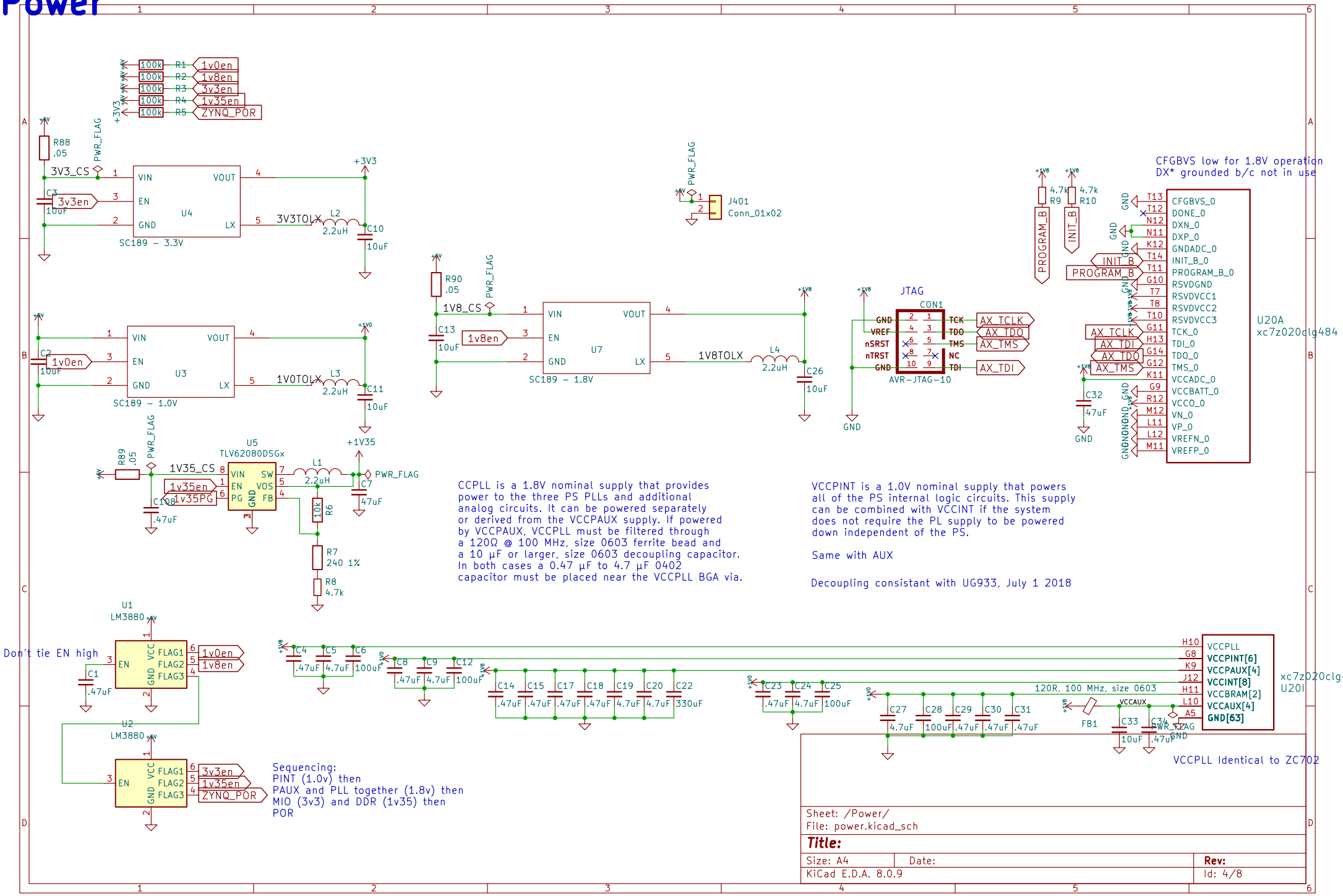
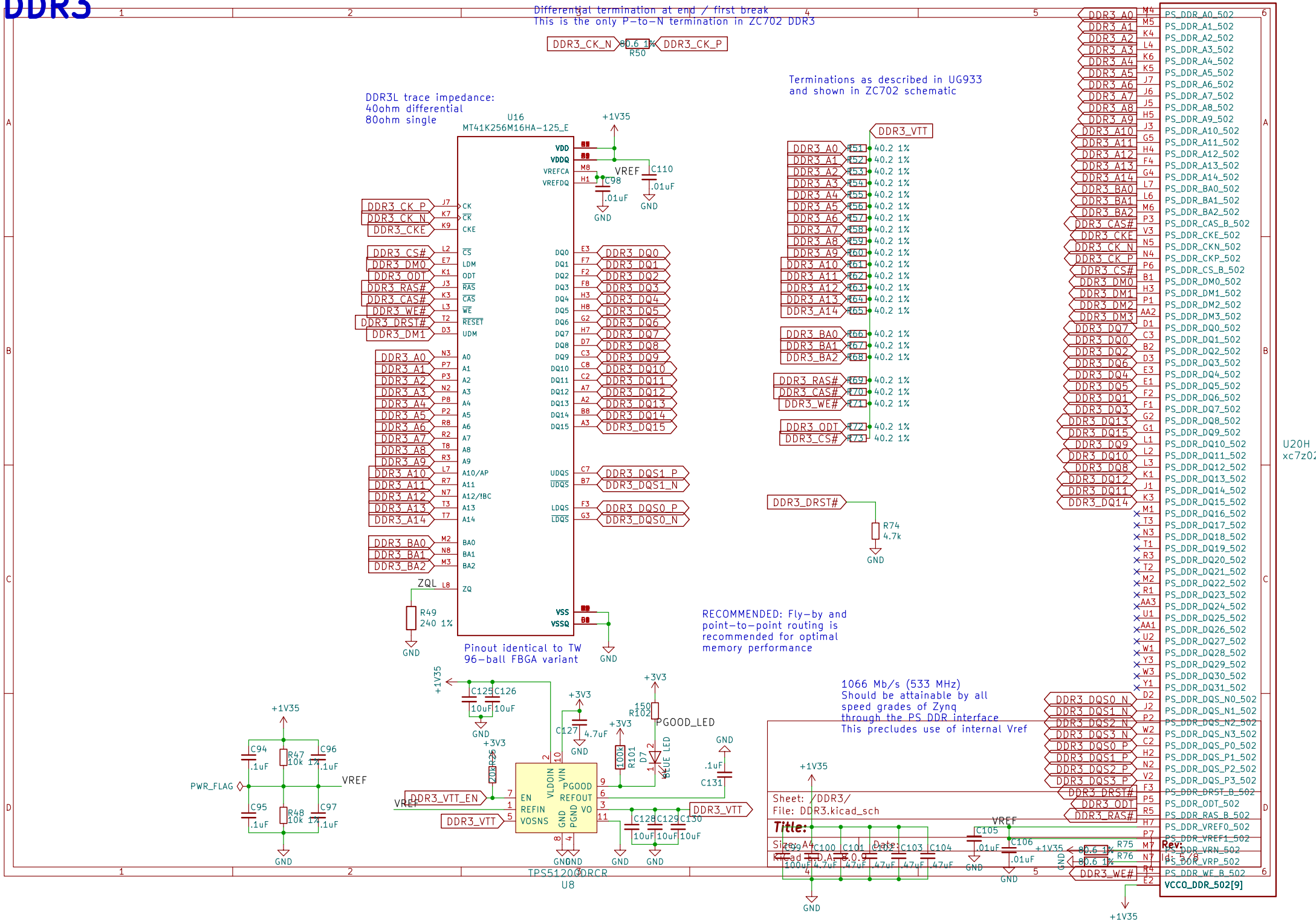
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.9		Id: 3/8

Power

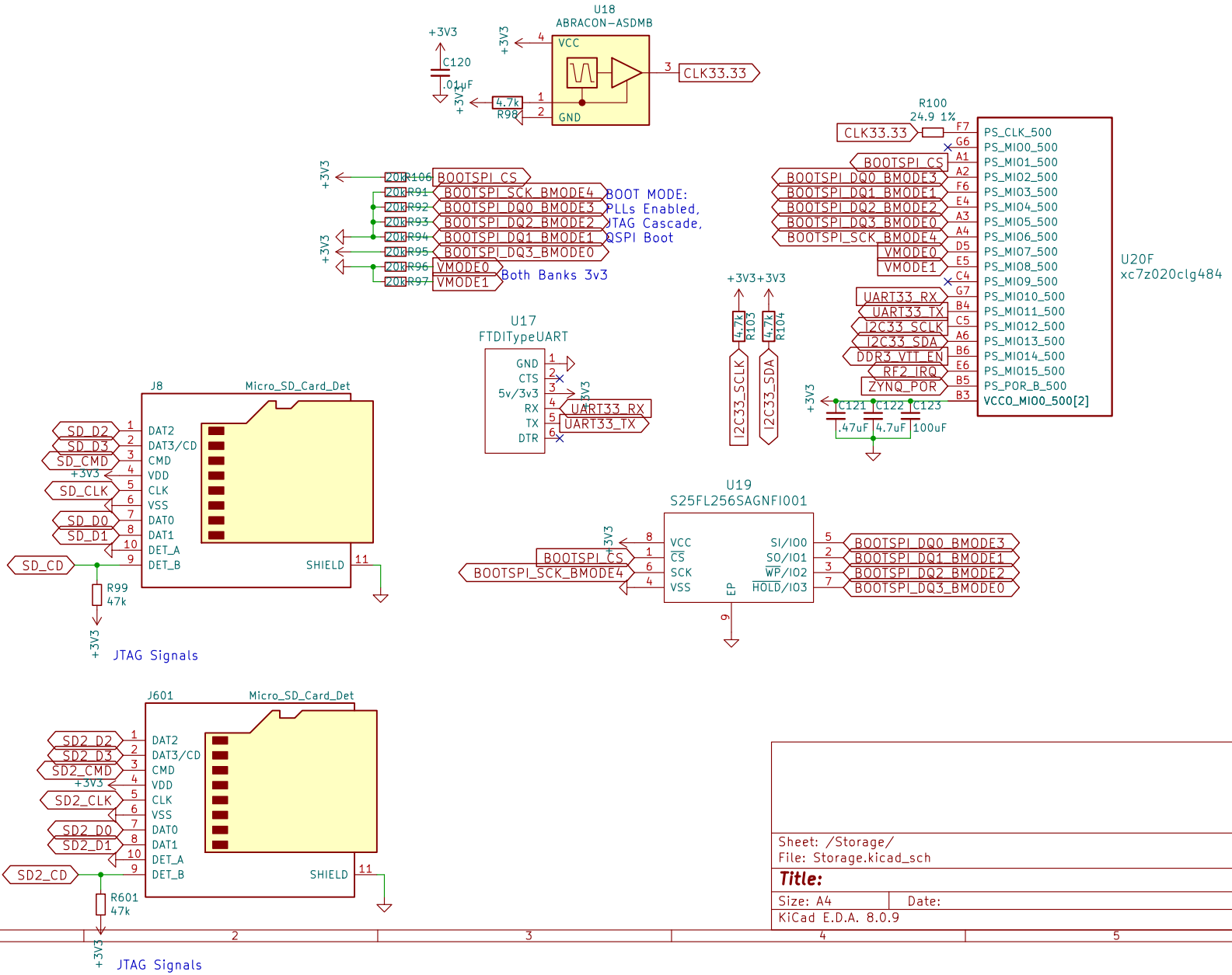

100k R1 1v0en
100k R2 1v8en
100k R3 3v3en
100k R4 1v35en
100k R5 ZYNQ_POR
+3V3
R88 .05
PWR_FLAG
3V3_CS
U4
VIN VOUT EN GND LX
SC189 – 3.3V
C3 10uF
3v3en
3V3TOLX
L2 2.2uH
C10 10uF
R90 .05
1V8_CS
U7
SC189 – 1.8V
1V8TOLX
L4 2.2uH
C26 10uF
C2 10uF
1v0en
U3
SC189 – 1.0V
1V0TOLX
L3 2.2uH
C11 10uF
R89 .05
1V35_CS
U5
TLV62080DSGx
VIN SW EN VOS PG FB GND
1v35en
1v35PG
L1 2.2uH
C7 47uF
C10 .47uF
10k R6
R7 240 1%
R8 4.7k
+1V35
J401
Conn_01x02
JTAG
CON1
GND VREF nSRST nTRST
TCK TDO TMS NC TDI
AX_TCLK AX_TDO AX_TMS AX_TDI
AVR-JTAG-10
C32 47uF
4.7k R9
4.7k R10
PROGRAM_B
INIT_B
CFGBVS low for 1.8V operation
DX* grounded b/c not in use
CFGBVS_0 DONE_0 DXN_0 DXP_0 GNDADC_0 INIT_B_0 PROGRAM_B_0 RSVDGND RSVDVCC1 RSVDVCC2 RSVDVCC3 TCK_0 TDI_0 TDO_0 TMS_0 VCCADC_0 VCCBATT_0 VCCO_0 VN_0 VP_0 VREFN_0 VREFP_0
U20A
xc7z020clg484
CCPLL is a 1.8V nominal supply that provides power to the three PS PLLs and additional analog circuits. It can be powered separately or derived from the VCCPAUX supply. If powered by VCCPAUX, VCCPLL must be filtered through a 120Ω @ 100 MHz, size 0603 ferrite bead and a 10 µF or larger, size 0603 decoupling capacitor. In both cases a 0.47 µF to 4.7 µF 0402 capacitor must be placed near the VCCPLL BGA via.
VCCPINT is a 1.0V nominal supply that powers all of the PS internal logic circuits. This supply can be combined with VCCINT if the system does not require the PL supply to be powered down independent of the PS.
Same with AUX
Decoupling consistant with UG933, July 1 2018
U1
LM3880
Don't tie EN high
EN VCC GND FLAG1 FLAG2 FLAG3
C1 .47uF
U2
LM3880
Sequencing:
PINT (1.0v) then
PAUX and PLL together (1.8v) then
MIO (3v3) and DDR (1v35) then
POR
C4 C5 .47uF 4.7uF C6 100uF
C8 C9 .47uF 4.7uF C12 100uF
C14 C15 C17 C18 C19 C20 C22 .47uF 4.7uF 330uF
C23 C24 .47uF 4.7uF C25 100uF
120R, 100 MHz, size 0603
C27 4.7uF C28 100uF C29 .47uF C30 .47uF C31 .47uF
FB1
VCCAUX
C33 10uF C34 .47uF
PWR_JTAG
GND
H10 G8 K9 J12 H11 L10 A5
VCCPLL
VCCPINT[6]
VCCPAUX[4]
VCCINT[8]
VCCBRAM[2]
VCCAUX[4]
GND[63]
xc7z020clg484
U20I
VCCPLL Identical to ZC702
Sheet: /Power/
File: power.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.9
Id: 4/8

DDR3



Differential termination at end / first break
This is the only P-to-N termination in ZC702 DDR3
DDR3_CK_N
DDR3_CK_P
R50
Terminations as described in UG933
and shown in ZC702 schematic
DDR3L trace impedance:
40ohm differential
80ohm single
U16
MT41K256M16HA-125_E
+1V35
VREF
C110
.01uF
C98
.01uF
GND
DDR3_VTT
DDR3_CK_P
DDR3_CK_N
DDR3_CKE
DDR3_CS#
DDR3_DM0
DDR3_ODT
DDR3_RAS#
DDR3_CAS#
DDR3_WE#
DDR3_DRST#
DDR3_DM1
DDR3_DQ0
DDR3_DQ1
DDR3_DQ2
DDR3_DQ3
DDR3_DQ4
DDR3_DQ5
DDR3_DQ6
DDR3_DQ7
DDR3_DQ8
DDR3_DQ9
DDR3_DQ10
DDR3_DQ11
DDR3_DQ12
DDR3_DQ13
DDR3_DQ14
DDR3_DQ15
DDR3_DQS1_P
DDR3_DQS1_N
DDR3_DQS0_P
DDR3_DQS0_N
DDR3_BA0
DDR3_BA1
DDR3_BA2
ZQL
R49
240 1%
DDR3_DRST#
R74
4.7k
RECOMMENDED: Fly-by and
point-to-point routing is
recommended for optimal
memory performance
Pinout identical to TW
96-ball FBGA variant
1066 Mb/s (533 MHz)
Should be attainable by all
speed grades of Zynq
through the PS DDR interface
This precludes use of internal Vref
+3V3
PGOOD_LED
R102
150
R101
100k
D7
BLUE LED
C131
.1uF
C125
C126
10uF
C127
4.7uF
C94
.1uF
R47
10k 1%
C96
.1uF
PWR_FLAG
VREF
C95
.1uF
R48
10k 1%
C97
.1uF
DDR3_VTT_EN
EN
REFIN
VOSNS
VLDOIN
VIN
PGOOD
REFOUT
VO
GND
PGND
C128
C129
C130
10uF
TPS51200DRCR
U8
Sheet: /DDR3/
File: DDR3.kicad_sch
Title:
Size: A4
Date:
Rev:
Id: 5/8
C99
C100
C101
C102
C103
C104
C105
C106
.01uF
R75
R76
80.6 1%
PS_DDR_A0_502
PS_DDR_A1_502
PS_DDR_A2_502
PS_DDR_A3_502
PS_DDR_A4_502
PS_DDR_A5_502
PS_DDR_A6_502
PS_DDR_A7_502
PS_DDR_A8_502
PS_DDR_A9_502
PS_DDR_A10_502
PS_DDR_A11_502
PS_DDR_A12_502
PS_DDR_A13_502
PS_DDR_A14_502
PS_DDR_BA0_502
PS_DDR_BA1_502
PS_DDR_BA2_502
PS_DDR_CAS_B_502
PS_DDR_CKE_502
PS_DDR_CKN_502
PS_DDR_CKP_502
PS_DDR_CS_B_502
PS_DDR_DM0_502
PS_DDR_DM1_502
PS_DDR_DM2_502
PS_DDR_DM3_502
PS_DDR_DQ0_502
PS_DDR_DQ1_502
PS_DDR_DQ2_502
PS_DDR_DQ3_502
PS_DDR_DQ4_502
PS_DDR_DQ5_502
PS_DDR_DQ6_502
PS_DDR_DQ7_502
PS_DDR_DQ8_502
PS_DDR_DQ9_502
PS_DDR_DQ10_502
PS_DDR_DQ11_502
PS_DDR_DQ12_502
PS_DDR_DQ13_502
PS_DDR_DQ14_502
PS_DDR_DQ15_502
PS_DDR_DQ16_502
PS_DDR_DQ17_502
PS_DDR_DQ18_502
PS_DDR_DQ19_502
PS_DDR_DQ20_502
PS_DDR_DQ21_502
PS_DDR_DQ22_502
PS_DDR_DQ23_502
PS_DDR_DQ24_502
PS_DDR_DQ25_502
PS_DDR_DQ26_502
PS_DDR_DQ27_502
PS_DDR_DQ28_502
PS_DDR_DQ29_502
PS_DDR_DQ30_502
PS_DDR_DQ31_502
PS_DDR_DQS_N0_502
PS_DDR_DQS_N1_502
PS_DDR_DQS_N2_502
PS_DDR_DQS_N3_502
PS_DDR_DQS_P0_502
PS_DDR_DQS_P1_502
PS_DDR_DQS_P2_502
PS_DDR_DQS_P3_502
PS_DDR_DRST_B_502
PS_DDR_ODT_502
PS_DDR_RAS_B_502
PS_DDR_VREF0_502
PS_DDR_VREF1_502
PS_DDR_VRN_502
PS_DDR_VRP_502
PS_DDR_WE_B_502
VCCO_DDR_502[9]
U20H
xc7z02

Non-volatile memory

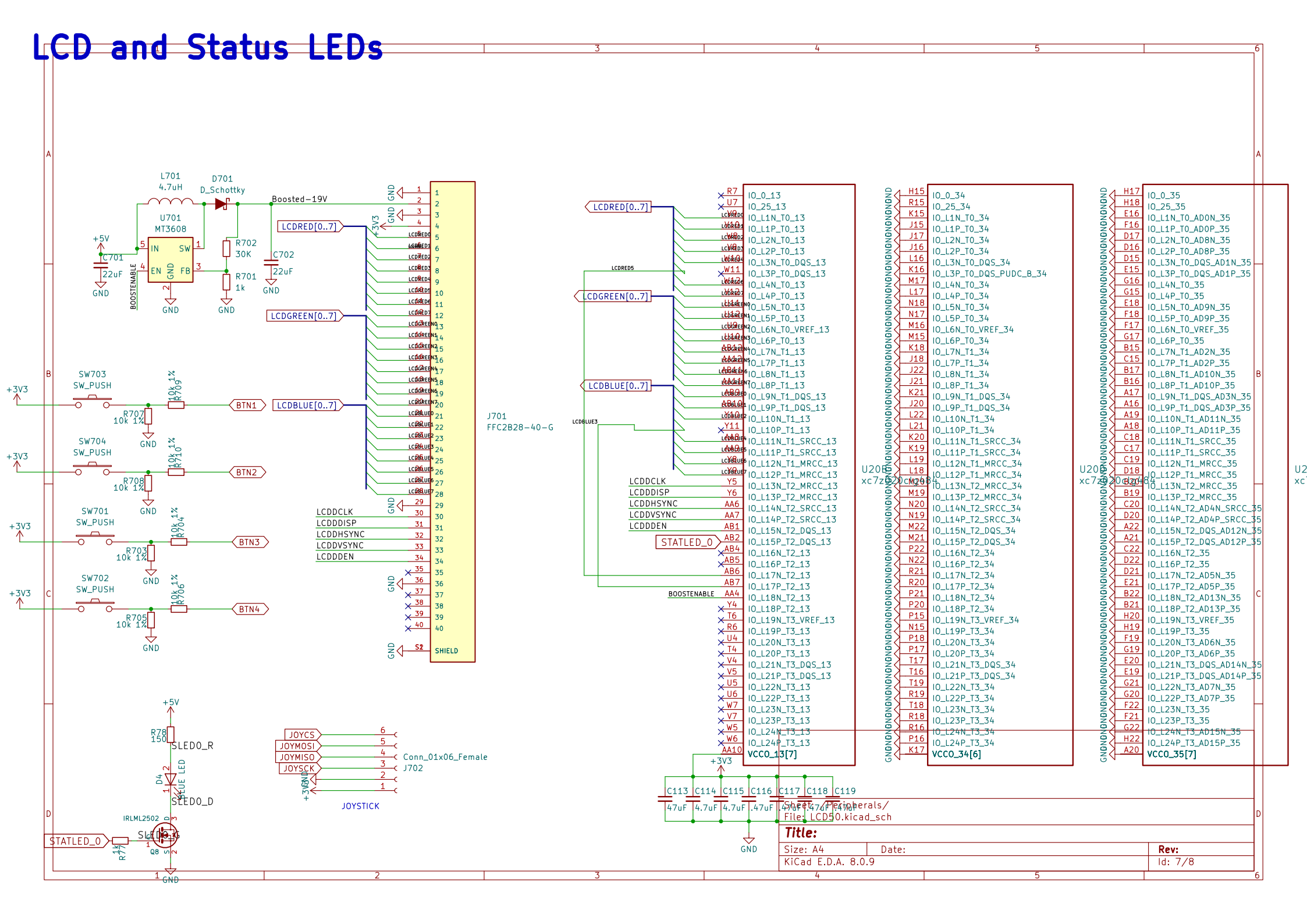
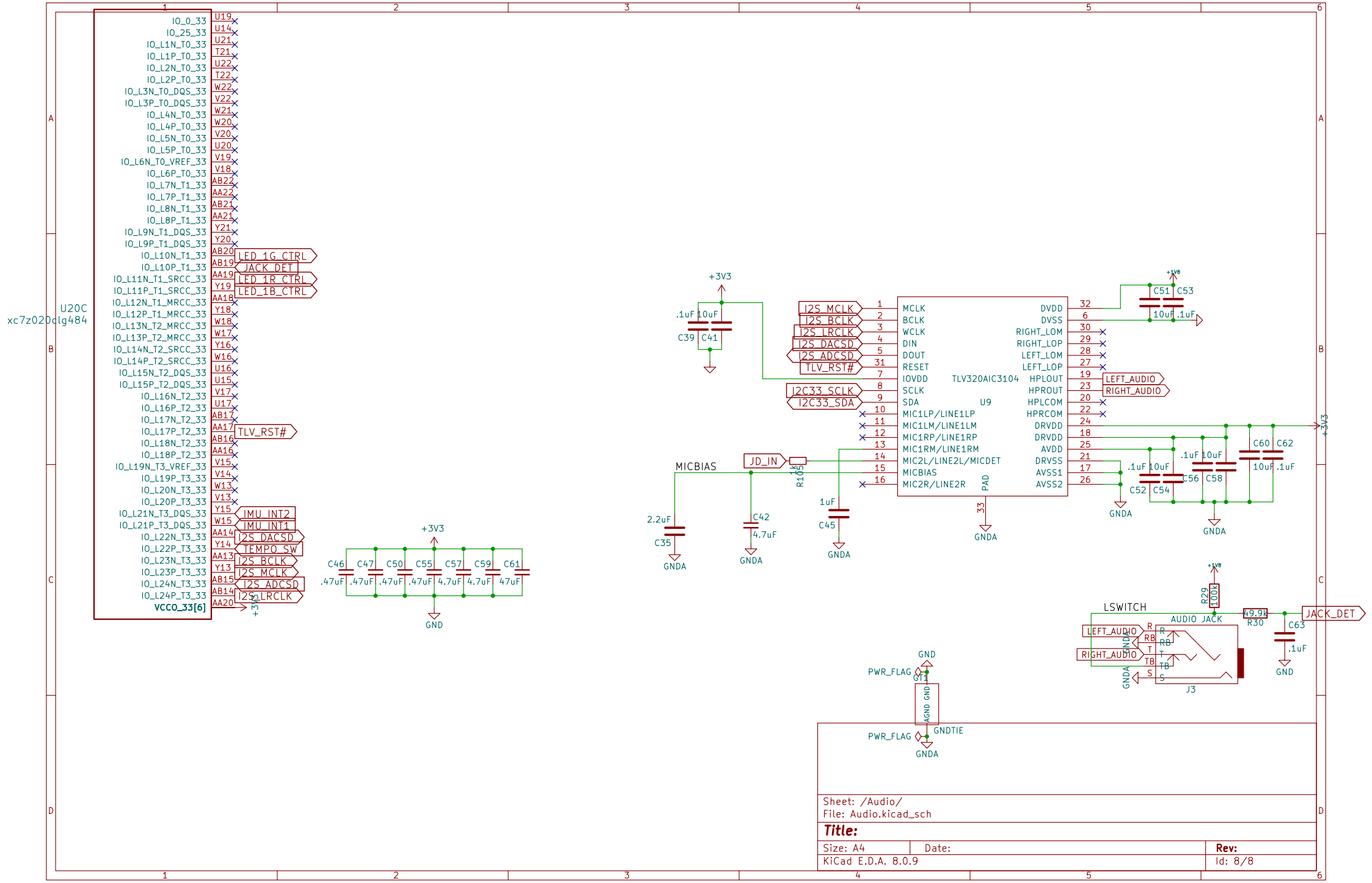


Sheet: /Storage/
File: Storage.kicad_sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.9		Id: 6/8

LCD and Status LEDs



Audio and HDMI