Project: Simulate a 4-bit CLA (Carry Lookahead Adder), and provide the circuit schematic, waveform to verify the correctness of the circuit, and measure its delay time.

報告：模擬 4-bit CLA，請提供電路圖、波形圖以確保電路正確性，並量測其延遲時間。

$$c_{i+1} = a_i.b_i + (a_i \oplus b_i).c_i$$
$$s_i = (a_i \oplus b_i) \oplus c_i$$

The above two equations can be written in terms of two new signals carry generate and carry propagate (Gi and Pi)

$$c_{i+1} = G_i + P_i.c_i$$
$$s_i = P_i \oplus c_i$$

where

$$G_i = a_i.b_i$$
$$P_i = a_i \oplus b_i$$

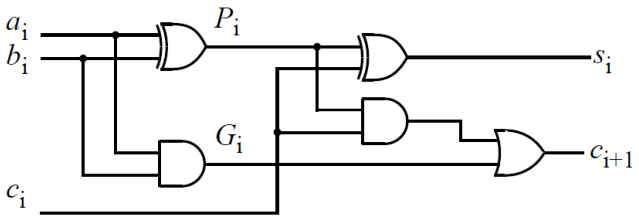

Figure 1: 1-bit CLA

$$c_1 = G_0 + P_0.c_0$$
$$c_2 = G_1 + P_1.G_0 + P_1.P_0.c_0$$
$$c_3 = G_2 + P_2.G_1 + P_2.P_1.G_0 + P_2.P_1.P_0.c_0$$
$$c_4 = G_3 + P_3.G_2 + P_3.P_2.G_1 + P_3.P_2.P_1.G_0 + P_3.P_2.P_1.P_0.c_0$$

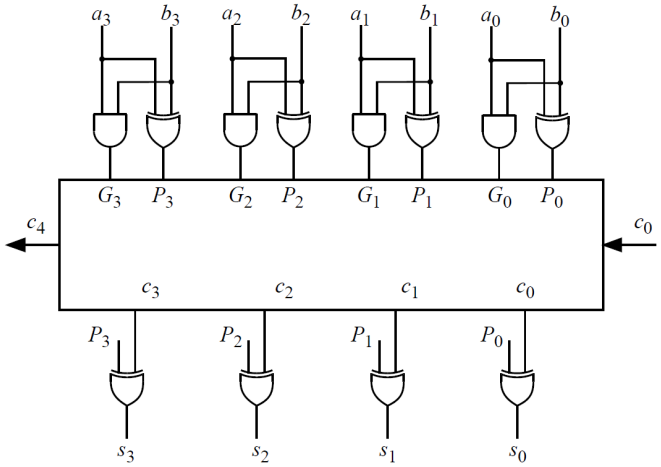

Figure 2: 4-bit CLA