System High-Level Design Document

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Analysis & Design

Common Platform

Doc No:	AD6000-D4B-SHD-V1.0EN
Version:	V1.0
Release date:	2016-08-28
Classification:	Internal

Keywords
System High-Level Design Document
Keypad

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Document Revision History

Revision	Date	Author	Description
V1.0	2016-12-20	Perry Hsu	Initial Release.

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1 Introduction

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1.1 Purpose

This document provides the high/low level design description for the keypad and associated modules. This manual also elaborates the mechanism required to use the keypad.

1.2 Scope

Table 1-1 presents the reference information of the modules which are used but beyond the scope.

Table 1-1. Reference Information beyond Scope

Modules	Reference information
Keypad driver	The Keypad driver.

1.3 Who Should Read This Document

This document is primarily intended for:

- Engineers with technical knowledge of the keypad
- Customers who integrate the keypad with user-defined applications

1.4 How to Use This Manual

This segment explains how information is distributed in this document, and presents some cues and examples to simplify finding and understanding information in this document. Table 1-2 presents an overview of the chapters and appendices in this document.

Table 1-2. Chapter Overview

#	Chapter	Contents
1	Introduction	Describes the scope and layout of this document.
2	References	References of this document
3	Definitions	The definitions of terms in this document
4	Abbreviations	The abbreviations of terms in this document
5	Overview	Gives a brief description of the modules of the system
6	Register Definition	Definition of keypad registers.

1.4.1 Terms and Conventions

This document uses special terms and typographical conventions to help you easily identify various information types in this document. These cues are designed to simply finding and understanding the information this document contains.

Table 1-3. Conventions

Convention	Usage	Example
N/A	N/A	N/A

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

[1] MTK Company Profile, http://brandclips.mediatek.inc/uploads/Company-profile-1H-2016_0418-Lite-final.pptx

[2] Keypad Driver document, http://dms.mediatek.inc/

3 Definitions

For the purposes of the present document, the following terms and definitions apply:

Single Key: Each (row, column) entry can detect one key in the key matrix.

Double Key: Each(row, column) is a group that can detect two keys in the key matrix, that redcues pin couts, but introduces more limitations.

Table 3-1. Single Key and Double Key Comparison

	Single Key	Double Key
Features	Able to detect 1 or 2 key-pressed simultaneously with any combination.	Minimize the pin counts for low cost phones
Key Scan	Row Sacn	Row Scan + Column Scan
Limiation	Simultaneously pressing more than 2 keys may not function correctly, if they are located on the same row/column.	Simultaneously pressing more than 2 keys may not function correctly, if they are located on the same row/column. Cannot detect 2 keys pressed simultaneously when the 2 keys are in the same group

Smartphones generally have few necessary keys: power key, volume up, and volume down. Single key is adopted in most schematic design.

4 Abbreviations

Please note the abbreviations and their explanations provided in Table 4-1. They are used in many fundamental definitions and explanations in this document and are specific to the information that this document contains.

Table 4-1. Abbreviations

Abbreviations	Explanation
MTK	MediaTek, Asia's largest fabless IC design company.
ASIC	Application-specific integrated circuit
KP	Keypad
COL	Column of Keypad Matrix
ROW	Row of Keypad Matrix
EN	Enable
SEL	Select

☞ [Random filler text. Not intended for actual reading.] Must keep the chapter even it have empty content.

5 Overview

5.1 Phyiscal Architecture

The keypad supports two types of keypads: 3*3 single keys and 2*2 configurable double keys.

The keypad can be divided into two parts:

1. The keypad interface. (see Figure 5-1, and Figure 5-2)
2. The key detection block provides key pressed, key released and de-bounce mechanisms.

Note: The keypad was cost downed from legacy 8*8 single keys and 3*3 double key design. The interace of MT6763 only supports 3*3 single or 2*2 double, but internal ASIC still detect keys in the manner of 8*8 single, and 3*3 double. The registers and key codes still follows the legacy naming.

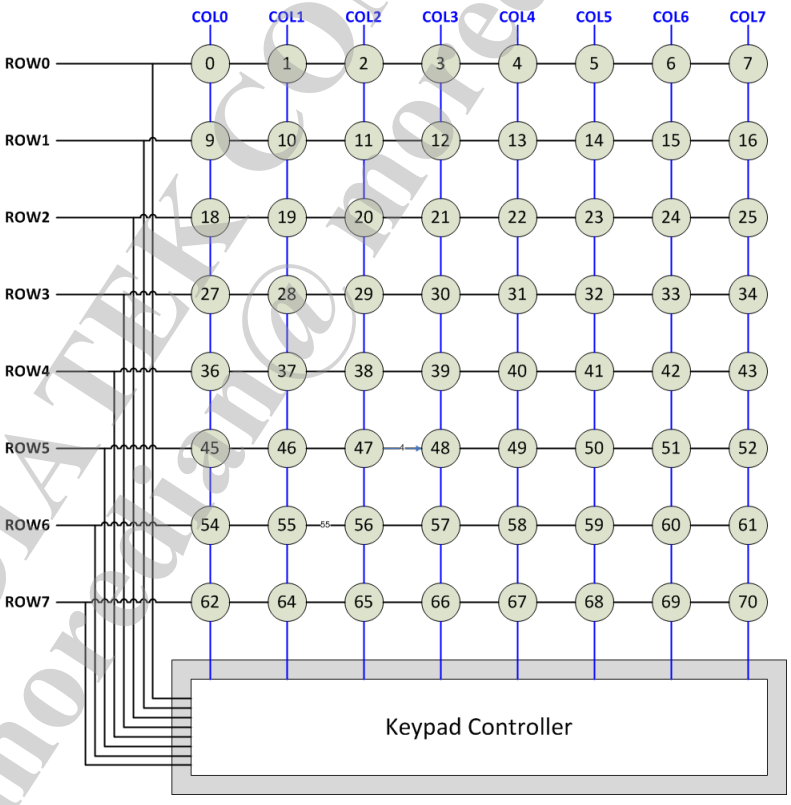

*Figure 5-1. 8*8 single key matrix*

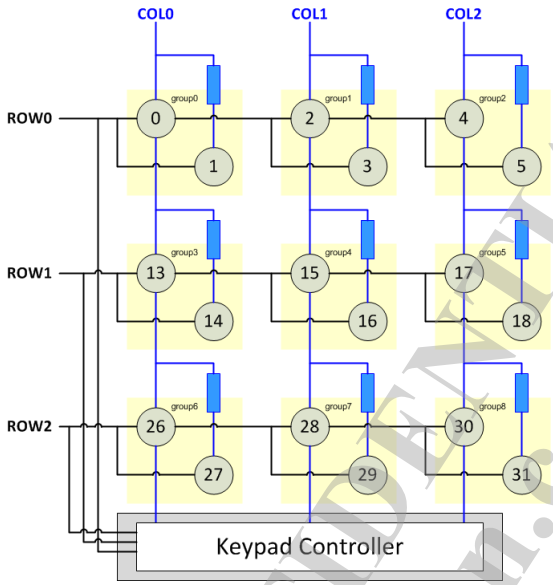

*Figure 5-2. 3*3 double key matrix*

Each time the key is pressed or released, i.e. something different in the key matrix, the key detection block senses the change and recognizes if a key has been pressed or released. Whenever the key status changes and is stable, a KEYPAD IRQ will be issued. The MCU can then read the key(s) pressed directly in the KP_MEM1, KP_MEM2, KP_MEM3, KP_MEM4 and KP_MEM5 registers. To ensure the key pressed information is not missed, the status register in keypad will not be read-cleared by the APB read command. The status register can only be changed by the key-pressed detection FSM.

5.1.1 Single Key Detection

This keypad detects one or two keys pressed simultaneously with any combination. Figure 5-3 shows the one key pressed condition. Figure 5-4 illustrate the cases of two keys pressed. Since the key pressed detection depends on the HIGH or LOW level of the external keypad interface, if the keys are pressed at the same time, and there exists a key that is on the same column and the same row with other keys, the pressed key cannot be correctly decoded. For example, if there are three key pressed: key1 = (x1, y1), key2 = (x2, y2), and key3 = (x1, y2), both key3 and key4 = (x2, y1) will be detected, and therefore they cannot be distinguished correctly. Hence, the keypad detects only one or two keys pressed simultaneously in any combination. More than two keys pressed simultaneously in a specific pattern will retrieve the wrong information.

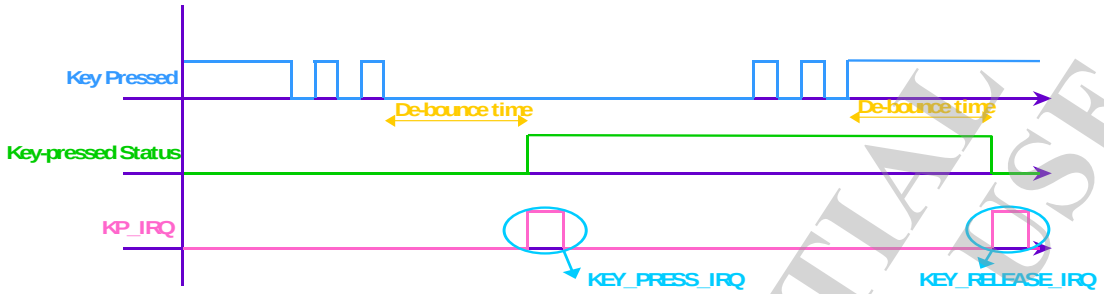

Figure 5-3. One key pressed with de-bounce mechanism denoted

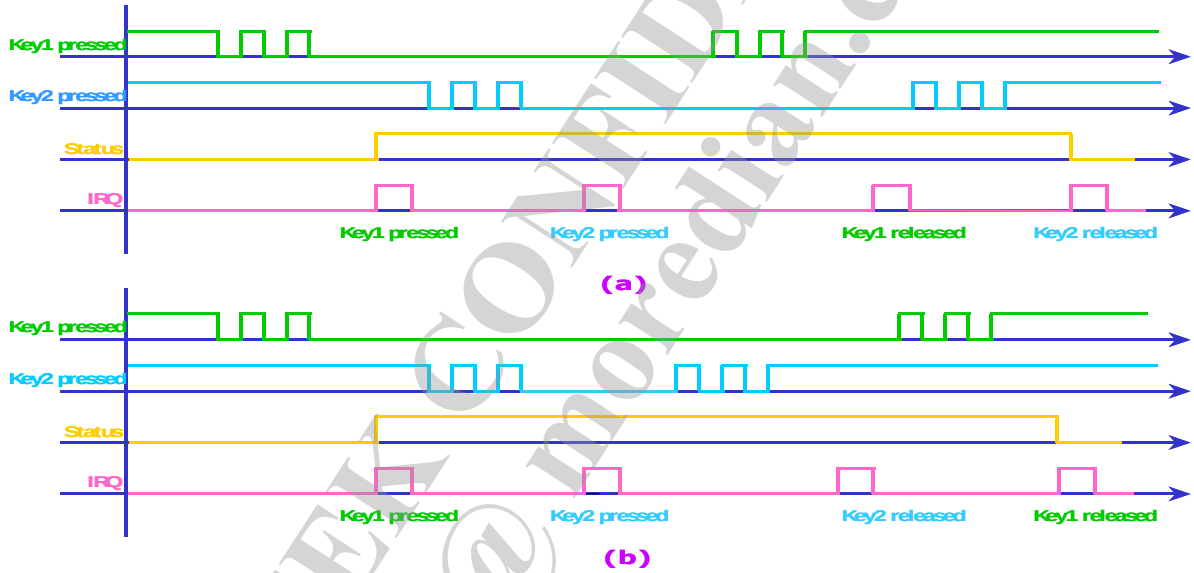

Figure 5-4. (a) Two keys pressed, case 1; (b) Two keys pressed, case 2

5.1.2 Double Key Detection

The 2*2 keypad supports a 2*2*2 = 8 keys matrix. The 8 keys are divided into 4 sub groups, and each group consists of 2 keys and a 20 ohm resistor. Besides the limitation of the single keypad, 2*2 keypad has another limitation, which is it cannot detect two keys pressed simultaneously when the two keys are in one group. For example in Figure 5-2, the double keypad cannot detect key 0 and key 1 pressed simultaneously or key 13 and key 14 pressed simultaneously.

5.2 Hardware Key Codes

5.2.1 Single Key

*Table 5-1. Hardware Key Codes: 3*3 Single Key*

HW Key Code	Col0	Col1	Col2
ROW0	0	1	2
ROW1	9	10	11
ROW2	18	19	20

5.2.2 Double Key

*Table 5-2. Hardware Key Codes: 2*2 Doule Key*

HW Key Code	Col0	Col1
ROW0	0/1	2/3
ROW1	13/14	15/16

6 Register Definition

6.1 List of Registers

The registers are listed in Table 6-1.

Table 6-1. List of Registers

Address	Name	Width	Register Function
10010000	KP_STA	16	Keypad Status
10010004	KP_MEM1	16	Keypad Scanning Output Register
10010008	KP_MEM2	16	Keypad Scanning Output Register
1001000c	KP_MEM3	16	Keypad Scanning Output Register
10010010	KP_MEM4	16	Keypad Scanning Output Register
10010014	KP_MEM5	16	Keypad Scanning Output Register
10010018	KP_DEBOUNCE	16	De-bounce Period Setting
1001001C	KP_SCAN_TIMING	16	Keypad Scan Timing Adjustment Register
10010020	KP_SEL	16	Keypad Selection Register
10010024	KP_EN	16	Keypad Enable Register

6.2 Register Tables

Table 6-2. Keypad Status Register: KP_STA

(Address) 10010000 H **(Short Name)** KP_STA **(Full Name)** Keypad Status **(Reset Value)** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																STA
Type																RO
Reset																0

(Register description)

Bit Field	Name	Description
0	STA	Indicates keypad status This register will not be cleared by the read operation. 0: No key pressed 1: Key pressed

Table 6-3. Keypad Scanning Output Register: KP_MEM1

(Address) 10010004 H | (Short Name) KP_MEM1 | (Full Name) Keypad Scanning Output Register | (Reset Value) 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY15	KEY14	KEY13	KEY12	KEY11	KEY10	KEY9	KEY8	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Register description)

Bit Field	Name	Description
15	KEY15	0: Key pressed 1: Key released
14	KEY14	0: Key pressed 1: Key released
13	KEY13	0: Key pressed 1: Key released
12	KEY12	0: Key pressed 1: Key released
11	KEY11	0: Key pressed 1: Key released
10	KEY10	0: Key pressed 1: Key released
9	KEY9	0: Key pressed 1: Key released
8	KEY8	0: Key pressed 1: Key released
7	KEY7	0: Key pressed 1: Key released
6	KEY6	0: Key pressed 1: Key released
5	KEY5	0: Key pressed 1: Key released
4	KEY4	0: Key pressed 1: Key released
3	KEY3	0: Key pressed 1: Key released
2	KEY2	0: Key pressed 1: Key released
1	KEY1	0: Key pressed 1: Key released
0	KEY0	0: Key pressed 1: Key released

Table 6-4. Keypad Scanning Output Register: KP_MEM2

(Address) 10010008 H | (Short Name) KP_MEM2 | (Full Name) Keypad Scanning Output Register | (Reset Value) 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY31	KEY30	KEY29	KEY28	KEY27	KEY26	KEY25	KEY24	KEY23	KEY22	KEY21	KEY20	KEY19	KEY18	KEY17	KEY16
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Register description)

Bit Field	Name	Description
15	KEY31	0: Key pressed 1: Key released
14	KEY30	0: Key pressed 1: Key released
13	KEY29	0: Key pressed 1: Key released
12	KEY28	0: Key pressed 1: Key released
11	KEY27	0: Key pressed 1: Key released
10	KEY26	0: Key pressed 1: Key released
9	KEY25	0: Key pressed 1: Key released
8	KEY24	0: Key pressed 1: Key released
7	KEY23	0: Key pressed 1: Key released
6	KEY22	0: Key pressed 1: Key released
5	KEY21	0: Key pressed 1: Key released
4	KEY20	0: Key pressed 1: Key released
3	KEY19	0: Key pressed 1: Key released
2	KEY18	0: Key pressed 1: Key released
1	KEY17	0: Key pressed 1: Key released
0	KEY16	0: Key pressed 1: Key released

Table 6-5. Keypad Scanning Output Register: KP_MEM3

(Address) 1001000C H | (Short Name) KP_MEM3 | (Full Name) Keypad Scanning Output Register | (Reset Value) 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY47	KEY46	KEY45	KEY44	KEY43	KEY42	KEY41	KEY40	KEY39	KEY38	KEY37	KEY36	KEY35	KEY34	KEY33	KEY32
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Register description)

Bit Field	Name	Description
15	KEY47	0: Key pressed 1: Key released
14	KEY46	0: Key pressed 1: Key released
13	KEY45	0: Key pressed 1: Key released
12	KEY44	0: Key pressed 1: Key released
11	KEY43	0: Key pressed 1: Key released
10	KEY42	0: Key pressed 1: Key released
9	KEY41	0: Key pressed 1: Key released
8	KEY40	0: Key pressed 1: Key released
7	KEY39	0: Key pressed 1: Key released
6	KEY38	0: Key pressed 1: Key released
5	KEY37	0: Key pressed 1: Key released
4	KEY36	0: Key pressed 1: Key released
3	KEY35	0: Key pressed 1: Key released
2	KEY34	0: Key pressed 1: Key released
1	KEY33	0: Key pressed 1: Key released
0	KEY32	0: Key pressed 1: Key released

Table 6-6. Keypad Scanning Output Register: KP_MEM4

(Address) 10010010 H | (Short Name) KP_MEM4 | (Full Name) Keypad Scanning Output Register | (Reset Value) 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY63	KEY62	KEY61	KEY60	KEY59	KEY58	KEY57	KEY56	KEY55	KEY54	KEY53	KEY52	KEY51	KEY50	KEY49	KEY48
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Register description)

Bit Field	Name	Description
15	KEY63	0: Key pressed 1: Key released
14	KEY62	0: Key pressed 1: Key released
13	KEY61	0: Key pressed 1: Key released
12	KEY60	0: Key pressed 1: Key released
11	KEY59	0: Key pressed 1: Key released
10	KEY58	0: Key pressed 1: Key released
9	KEY57	0: Key pressed 1: Key released
8	KEY56	0: Key pressed 1: Key released
7	KEY55	0: Key pressed 1: Key released
6	KEY54	0: Key pressed 1: Key released
5	KEY53	0: Key pressed 1: Key released
4	KEY52	0: Key pressed 1: Key released
3	KEY51	0: Key pressed 1: Key released
2	KEY50	0: Key pressed 1: Key released
1	KEY49	0: Key pressed 1: Key released
0	KEY48	0: Key pressed 1: Key released

Table 6-7. Keypad Scanning Output Register: KP_MEM5

(Address) 10010014 H | (Short Name) KP_MEM5 | (Full Name) Keypad Scanning Output Register | (Reset Value) 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY1[1:0]		KEY77	KEY76	KEY75	KEY74	KEY73	KEY72	KEY71	KEY70	KEY69	KEY68	KEY67	KEY66	KEY65	KEY64
Type	RO		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Register description)

Bit Field	Name	Description
15:14	DUMMY1[1:0]	
13	KEY77	0: Key pressed 1: Key released
12	KEY76	0: Key pressed 1: Key released
11	KEY75	0: Key pressed 1: Key released
10	KEY74	0: Key pressed 1: Key released
9	KEY73	0: Key pressed 1: Key released
8	KEY72	0: Key pressed 1: Key released
7	KEY71	0: Key pressed 1: Key released
6	KEY70	0: Key pressed 1: Key released
5	KEY69	0: Key pressed 1: Key released
4	KEY68	0: Key pressed 1: Key released
3	KEY67	0: Key pressed 1: Key released
2	KEY66	0: Key pressed 1: Key released
1	KEY65	0: Key pressed 1: Key released
0	KEY64	0: Key pressed 1: Key released

Table 6-8. De-bounce Period Setting: KP_DEBOUNCE

(Address)	(Short Name)	(Full Name)	(Reset Value)
10010018 H	KP_DEBOUNCE	De-bounce Period Setting	00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEBOUNCE[13:0]													
Type			R/W													
Reset			0	0	0	1	0	0	0	0	0	0	0	0	0	0

(Register description)

Bit Field	Name	Description
13:0	DEBOUNCE[13:0]	De-bounce time = KP_DEBOUNCE/32 ms Reset Default is 0x400, 1024/32 = 32ms.

Table 6-9. Keypad Scan Timing Adjustment Register: KP_SCAN_TIMING

(Address) 1001001C H	(Short Name) KP_SCAN_TIMING	(Full Name) Keypad Scan Timing Adjustment Register	(Reset Value) 00000011

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COL_HIGH_PULSE[3:0]				ROW_HIGH_PULSE[3:0]				COL_SCAN_DIV[3:0]				ROW_SCAN_DIV[3:0]			
Type	R/W				R/W				R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

(Register description)

Bit Field	Name	Description
15:12	COL_HIGH_PULSE [3:0]	Sets up the COL SCAN high pulse, i.e. cycles of the scan high pulse Default 0 means the high scan pulse needs 1 cycle.
11:8	ROW_HIGH_PULSE [3:0]	Sets up the ROW SCAN high pulse, i.e. cycles of the scan high pulse Default 0 means the high scan pulse needs 1 cycle.
7:4	COL_SCAN_DIV[3:0]	Sets up the COL SCAN cycle which includes COL_INTERVAL_DIV and the high pulse period Default 1 means there are 2 cycles for each scan, including 1 cycle high pulse and 1 cycle interval.
3:0	ROW_SCAN_DIV[3:0]	Sets up the ROW SCAN cycle which includes ROW_INTERVAL_DIV and the high pulse period Default 1 means there are 2 cycles for each scan, including 1 cycle high pulse and 1 cycle interval.

Table 6-10. Keypad Selection Register: KP_SEL

(Address)	(Short Name)	(Full Name)	(Reset Value)
10010020 H	KP_SEL	Keypad Selection Register	00001C70

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KP1_COL_SEL[5:0]						KP1_ROW_SEL[5:0]									KP_SEL
Type	R/W						R/W									D/C
Reset	0	0	0	1	1	1	0	0	0	1	1	1				0

(Register description)

Bit Field	Name	Description
15:0	KP1_COL_SEL[5:0]	Selects which cols are used when double keypad is used MT6763 supports maximum 2*2 double key. Only row1 and row0 can be used. 0: Disable corresponding column 1: Enable corresponding column
9:4	KP1_ROW_SEL[5:0]	Selects which rows are used when double keypad is used MT6763 supports maximum 2*2 double key. Only row1 and row0 can be used. 0: Disable corresponding row 1: Enable corresponding row
0	KP_SEL	Selects to use single keypad or double keypad 0: Use single keypad 1: Use double keypad

Table 6-11. Keypad Enable Register: KP_EN

(Address)	(Short Name)	(Full Name)	(Reset Value)
10010024 H	KP_EN	Keypad Enable Register	00000011

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																KP_EN
Type																RW
Reset																1

(Register description)

Bit Field	Name	Description
0	KP_EN	0: Disable keypad (Both single and double keypad will not work.) 1: Enable keypad (Either single or double keypad will work.)

6.3 Register Table Definitions

The following abbreviations are defined for register types:

- **R/W:** Read Write. The field can be accessed both in write and read mode.
- **RO**: Read Only. The field can be accessed in read mode only. A write with one or zero has no effect.
- **WO:** Write Only. The field can be accessed in write mode only. A read has no effect and return zero.
- **RC:** Read Clear. The field can be accessed in read mode only. A read clears the bit if set. A write with one or zero has no effect.
- **RS**: The field can be accessed in read mode only. A read sets the bit if not set. A write with one or zero has no effect.
- **WS:** Write Set.
- **WC:** Write Clear.
- **I/O:** Input and Output

It should be noted that the abbreviations shall be clearly defined in the documents for clarification.

The following abbreviations are defined for reference register types:

- **R/W1S**: Read and write 1 set. The field can be accessed in both read and write mode. Setting this bit provokes certain functions in the circuit. A write with zero has no effect.
- **R/W0C**: Read and write 0 clear. The field can be accessed in both read and write mode. A write with zero clears the bit if set. A write with one has no effect.
- **R/W1C**: Read and write 1 clear. The field can be accessed in both read and write mode. A write with one clears the bit if set. A write with zero has no effect.
- **R/WaC**: Read and write with auto clear. The field can be accessed in both read and write mode. Setting this field provokes certain functions in the circuit. It is automatically cleared when the function is completed.