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93 modem Typical case study of RF driver setting

ACS1/RF
20180521

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Overview

- 93 Modem RF Driver Setting notice
- 93 Modem typical Case study
- 93 Modem RF Driver reference document list
- Q&A

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Note 1: LTE Modem

- RX ON/OFF ,TX ON/OFF do not need to add 0X1C 0X38 and 0X1C 0XB8

RX ON

```
LTE_MIPI_DATA_SUBBAND_TABLE_T LTE_Band1_MIPI_RX_DATA_SetDefault[] =
{
   //No.      elm type      , port_sel          , data_seq      , USID                    ,{ { subband-0 freq    ,addr ,data }, { subband-1
   { /* 0  */ LTE_MIPI_ASM , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_ASM0_SetDefault   ,{ { 21100 /*100 kHz*/ ,0x00 ,0x16 }, {
   { /* 1  */ LTE_MIPI_ASM , LTE_MIPI_PORT3    , LTE_REG_W     , MIPI_USID_ASM1_SetDefault   ,{ { 21100 /*100 kHz*/ ,0x00 ,0x08 }, {
   { /* 2  */ LTE_MIPI_ASM , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_ASM0_SetDefault   ,{ { 21100 /*100 kHz*/ ,0x00 ,0x00 }, {
   { /* 3  */ LTE_MIPI_ASM , LTE_MIPI_PORT3    , LTE_REG_W     , MIPI_USID_ASM1_SetDefault   ,{ { 21100 /*100 kHz*/ ,0x00 ,0x00 }, {
   { /* 4  */ LTE_MIPI_NULL, 0                 , 0             , 0                       ,{ { 0     /*100 kHz*/ ,0    ,0    }, { 0     /*10
};
```

TX ON

```
 LTE_MIPI_DATA_SUBBAND_TABLE_T LTE_Band1_MIPI_TX_DATA_SetDefault[] =
] {
    //No.      elm type      , port_sel          , data_seq      , USID                    ,{ { subband-0 freq    ,addr ,data }, { subband-1 f
    { /* 0  */ LTE_MIPI_PA  , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_PA0_SetDefault    ,{ { 19200 /*100 kHz*/    ,0x00 , 0x7a},
    { /* 1  */ LTE_MIPI_PA  , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_PA0_SetDefault    ,{ { 19200 /*100 kHz*/    ,0x01 , 0x00},
    { /* 2  */ LTE_MIPI_PA  , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_PA0_SetDefault    ,{ { 19200 /*100 kHz*/    ,0x03 , 0x00},
    { /* 3  */ LTE_MIPI_PA  , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_PA0_SetDefault    ,{ { 19200 /*100 kHz*/    ,0x00 , 0x00},
    { /* 4  */ LTE_MIPI_ASM , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_ASM0_SetDefault   ,{ { 19200 /*100 kHz*/    ,0x00 , 0x16},
    { /* 5  */ LTE_MIPI_NULL, 0                 , 0             , 0                       ,{ { 0     /*100 kHz*/    ,0    , 0   }, { 0     /*
};
```

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Note2: LTE Modem

- Qorvo PA TX ON data do not need 0x2 0x00, but Skyworks PA need 0x2 0x00

Qorvo

```
LTE_MIPI_DATA_SUBBAND_TABLE_T LTE_Band40_MIPI_TX_DATA_SetDefault[] =
]{
    //No.       elm type      , port_sel          , data_seq      , USID                    ,{ { subband-0 freq    ,addr ,data }, { subband-1
    { /* 0  */ LTE_MIPI_PA   , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_PA0_SetDefault   ,{ { 23000 /*100 kHz*/  ,0x00 , 0x7a},
    { /* 1  */ LTE_MIPI_PA   , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_PA0_SetDefault   ,{ { 23000 /*100 kHz*/  ,0x01 , 0x00},
    { /* 2  */ LTE_MIPI_PA   , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_PA0_SetDefault   ,{ { 23000 /*100 kHz*/  ,0x03 , 0x00},
    { /* 3  */ LTE_MIPI_PA   , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_PA0_SetDefault   ,{ { 23000 /*100 kHz*/  ,0x00 , 0x00},
    { /* 4  */ LTE_MIPI_ASM  , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_ASM0_SetDefault  ,{ { 23000 /*100 kHz*/  ,0x00 , 0x27},
    { /* 5  */ LTE_MIPI_NULL, 0                   , 0             , 0                          ,{ { 0     /*100 kHz*/  ,0    , 0   }, { 0     /*1
};
```

SKYWORKS

```
LTE_MIPI_DATA_SUBBAND_TABLE_T LTE_Band40_MIPI_TX_DATA_Set0[] =
{
    //No.       elm type      , port_sel          , data_seq      , USID                    ,{ { subband-0 freq    ,addr ,data
    { /* 0  */ LTE_MIPI_PA   , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_PA0_Set0     ,{ { 23000 /*100 kHz*/  ,0x00 , 0x0C}, {
    { /* 1  */ LTE_MIPI_PA   , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_PA0_Set0     ,{ { 23000 /*100 kHz*/  ,0x01 , 0x00}, {
    { /* 2  */ LTE_MIPI_PA   , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_PA0_Set0     ,{ { 23000 /*100 kHz*/  ,0x02 , 0x00}, {
    { /* 3  */ LTE_MIPI_PA   , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_PA0_Set0     ,{ { 23000 /*100 kHz*/  ,0x03 , 0x00}, {
    { /* 4  */ LTE_MIPI_PA   , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_ASM0_Set0    ,{ { 23000 /*100 kHz*/  ,0x04 , 0x11}, {
    { /* 5  */ LTE_MIPI_PA   , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_PA0_Set0     ,{ { 23000 /*100 kHz*/  ,0x00 , 0x00}, {
    { /* 6  */ LTE_MIPI_PA   , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_ASM0_Set0    ,{ { 23000 /*100 kHz*/  ,0x04 , 0x00}, {
    { /* 7  */ LTE_MIPI_ASM  , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_ASM0_Set0    ,{ { 23000 /*100 kHz*/  ,0x05 , 0x08}, {
    //{ /* 7  */ LTE_MIPI_ASM  , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_ASM0_Set0    ,{ { 23000 /*100 kHz*/  ,0x03 , 0x00},
    { /* 8  */ LTE_MIPI_NULL, 0                   , 0             , 0                          ,{ { 0     /*100 kHz*/  ,0    , 0
};
```


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Note3: LTE Modem

- 93 Modem does not call bypass path. We call it filter path.
- 93 Modem does not support Tx Bypass Feature; **these CW don't need to set**

```
LTE_MIPI_DATA_SUBBAND_TABLE_T LTE_Band38_MIPI_FILTER_TX_DATA_SetDefault[] =
{
    //No.       elm type      , port_sel          , data_seq      , USID                ,{ { subband-0 freq    ,addr ,data }, { subband-1
    { /* 0  */ LTE_MIPI_PA   , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_PA0_SetDefault   ,{ { 25700 /*100 kHz*/  ,0x02 , 0x00},
    { /* 1  */ LTE_MIPI_PA   , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_PA0_SetDefault   ,{ { 25700 /*100 kHz*/  ,0x00 , 0x3E},
    { /* 2  */ LTE_MIPI_PA   , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_PA0_SetDefault   ,{ { 25700 /*100 kHz*/  ,0x01 , 0x00},
    { /* 3  */ LTE_MIPI_PA   , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_PA0_SetDefault   ,{ { 25700 /*100 kHz*/  ,0x03 , 0x00},
    { /* 4  */ LTE_MIPI_PA   , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_ASM0_SetDefault  ,{ { 25700 /*100 kHz*/  ,0x04 , 0x18},
    { /* 5  */ LTE_MIPI_PA   , LTE_MIPI_PORT2    , LTE_REG_W     , MIPI_USID_ASM2_SetDefault  ,{ { 25700 /*100 kHz*/  ,0x00 , 0x00},
    { /* 6  */ LTE_MIPI_PA   , LTE_MIPI_PORT1    , LTE_REG_W     , MIPI_USID_PA0_SetDefault   ,{ { 25700 /*100 kHz*/  ,0x00 , 0x00},
    { /* 7  */ LTE_MIPI_PA   , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_ASM0_SetDefault  ,{ { 25700 /*100 kHz*/  ,0x04 , 0x00},
    { /* 8  */ LTE_MIPI_ASM  , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_ASM0_SetDefault  ,{ { 25700 /*100 kHz*/  ,0x03 , 0x20},
    //{ /* 7  */ LTE_MIPI_ASM , LTE_MIPI_PORT0    , LTE_REG_W     , MIPI_USID_ASM0_SetDefault  ,{ { 25700 /*100 kHz*/  ,0x03 , 0x00}
    { /* 8  */ LTE_MIPI_NULL, 0                   , 0             , 0                  ,{ { 0     /*100 kHz*/  ,0    , 0   }, { 0     /*1
```

```
/*-----------------------------------*/
/* 0th Band Setting for Filter mode */
/*-----------------------------------*/
#define  BAND_FILTER_INDICATOR0_SetDefault                LTE_BandNone
#define  BAND_FILTER_INDICATOR0_POWER_COMP_SetDefault     0
#define  BAND_FILTER_INDICATOR0_COUPLER_COMP_SetDefault   0
/*-----------------------------------*/
```


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Note4: C2K Modem

- C2K BPI do not need PMASK

90 modem

```
/* BPI mask and data.
/* Only bit5~bit20(BPI5~BPI20) are effective. Ple
/* bits to 0.
/*-----------------------------------------------
/* -------- PDATA_BAND_A Start ---------*/
#define  PMASK_BAND_A_PR1       0x00004860
#define  PDATA_BAND_A_PR1       0x00004800
#define  PMASK_BAND_A_PR2       0x00004860
#define  PDATA_BAND_A_PR2       0x00004800
#define  PMASK_BAND_A_PR2B      0x00004860
#define  PDATA_BAND_A_PR2B      0x00004800
#define  PMASK_BAND_A_PR3       0x00004860
#define  PDATA_BAND_A_PR3       0x00000000
#define  PMASK_BAND_A_PT1       0x00044860
#define  PDATA_BAND_A_PT1       0x00044800
#define  PMASK_BAND_A_PT2       0x00044860
#define  PDATA_BAND_A_PT2       0x00044800
#define  PMASK_BAND_A_PT2B      0x00044860
#define  PDATA_BAND_A_PT2B      0x00044800
#define  PMASK_BAND_A_PT3       0x00040000
#define  PDATA_BAND_A_PT3       0x00000000
/* -------- PDATA_BAND_A End ---------*/
/* -------- PDATA_BAND_A RXD Start ---*/
```

93 Modem

```
/*-----------------------------------------------------------------*/
/* -------- PDATA_BAND_A Start ---------*/
#define  PDATA_BAND_A_PR1_SetDefault       0x0000A000
#define  PDATA_BAND_A_PR2_SetDefault       0x0000A000
#define  PDATA_BAND_A_PR2B_SetDefault      0x0000A000
#define  PDATA_BAND_A_PR3_SetDefault       0x00000000
#define  PDATA_BAND_A_PT1_SetDefault       0x0000A000
#define  PDATA_BAND_A_PT2_SetDefault       0x0000A000
#define  PDATA_BAND_A_PT2B_SetDefault      0x0000A000
#define  PDATA_BAND_A_PT3_SetDefault       0x00000000
/* -------- PDATA_BAND_A End ---------*/
```

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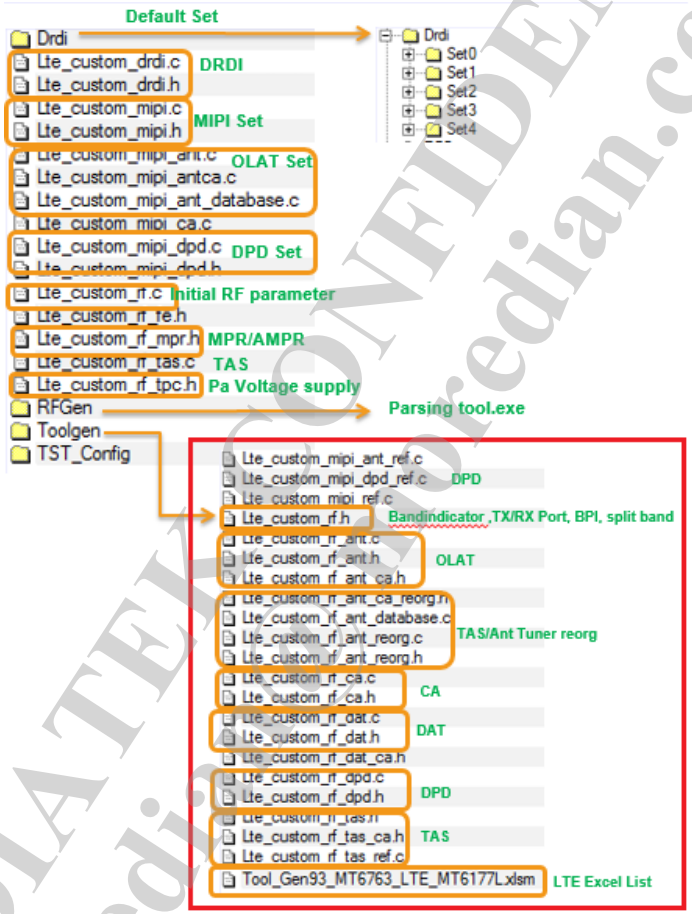
Note5: Custom Excel configuration & file generation tool

- We use tool to generate a part of files and it includes as below file of red box



- Tool link: mcu/common/tools/RFGen/Parsing Tool.exe
- Excel link: Toolgen/Tool_Gen93_MT6177L_LTE.xlsm/ Tool_Gen93_MT6763_LTE_MT6177L.xlsm

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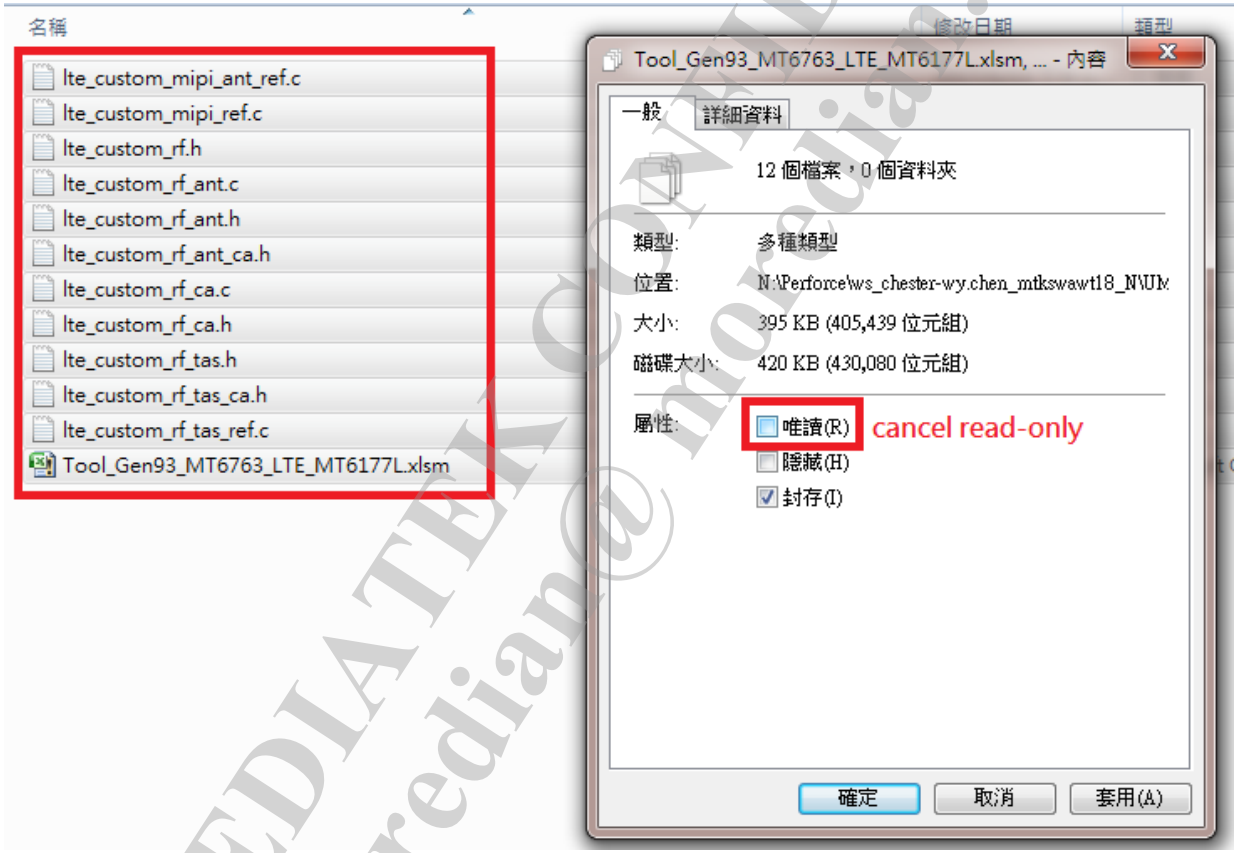
Note6-1: Custom Excel configuration & file generation tool

- **You must CANCEL read-only the excel file and all the toolgen file**



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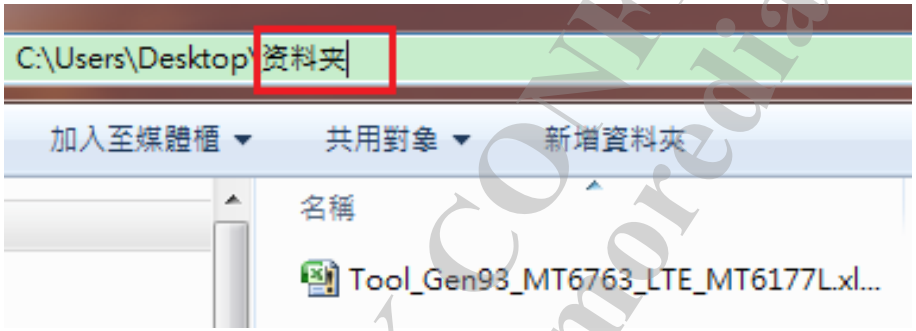
Note6-2:Custom Excel configuration & file generation tool

- **Excel and tool location CAN NOT include Simplified Chinese characters**

Any Simplified Chinese characters is not allowed on the excel location



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Note7: Custom Excel configuration & file generation tool

- We will have SOP to help you configure the Excel document

Tool Version (Do not change)						
93_77M						
DRDI Set						
SetDefault			Tool limit: Order cannot be changed			
SingleBand Setting						
BAND_INDICATOR_ID	(LTE_BAND)	SUPPORT(SW capability)	RX_IO_SEL	RXD_IO_SEL	PDATA_PR1	PDATA_PR2
BAND_INDICATOR0	LTE_Band1	SW_CAPABILITY_SUPPORT	RX_IO_PRX2	RX_IO_DRX1	0x00000000	0x00000000
BAND_INDICATOR1	LTE_Band2	SW_CAPABILITY_SUPPORT	RX_IO_PRX7	RX_IO_DRX2	0x00000000	0x00000000
BAND_INDICATOR2	LTE_Band3	SW_CAPABILITY_SUPPORT	RX_IO_PRX1	RX_IO_DRX4	0x00000000	0x00000000
BAND_INDICATOR3	LTE_Band4	SW_CAPABILITY_SUPPORT	RX_IO_PRX3	RX_IO_DRX1	0x00000000	0x00000000
BAND_INDICATOR4	LTE_Band5	SW_CAPABILITY_SUPPORT	RX_IO_PRX5	RX_IO_DRX8	0x00000000	0x00000000
BAND_INDICATOR5	LTE_Band7	SW_CAPABILITY_SUPPORT	RX_IO_PRX6	RX_IO_DRX5	0x00000000	0x00000000
BAND_INDICATOR6	LTE_Band8	SW_CAPABILITY_SUPPORT	RX_IO_PRX10	RX_IO_DRX9	0x00000008	0x00000008
BAND_INDICATOR7	LTE_Band12	SW_CAPABILITY_SUPPORT	RX_IO_PRX8	RX_IO_DRX10	0x00000004	0x00000004
BAND_INDICATOR8	LTE_Band17	SW_CAPABILITY_SUPPORT	RX_IO_PRX8	RX_IO_DRX10	0x00000004	0x00000004
BAND_INDICATOR9	LTE_Band20	SW_CAPABILITY_SUPPORT	RX_IO_PRX10	RX_IO_DRX9	0x00000002	0x00000002
BAND_INDICATOR10	LTE_Band25	SW_CAPABILITY_SUPPORT	RX_IO_PRX7	RX_IO_DRX2	0x00000000	0x00000000
BAND_INDICATOR11	LTE_Band26	SW_CAPABILITY_SUPPORT	RX_IO_PRX5	RX_IO_DRX8	0x00000000	0x00000000
BAND_INDICATOR12	LTE_Band28	SW_CAPABILITY_SUPPORT	RX_IO_PRX8	RX_IO_DRX10	0x00000001	0x00000001
BAND_INDICATOR13	LTE_Band34	SW_CAPABILITY_SUPPORT	RX_IO_PRX9	RX_IO_DRX7	0x00000000	0x00000000

- CS0021-GAK1A-AND-V1.2EN_Platform_System_RF_LTE_RF_Custom_Setting_Application_Note
- LTE Custom Excel And File Generation Tool(MT6177)
- LTE custom Excel and file generation tool(MT6177m)V1.1
- Note: The Sop of Paring tool is contained by these above files

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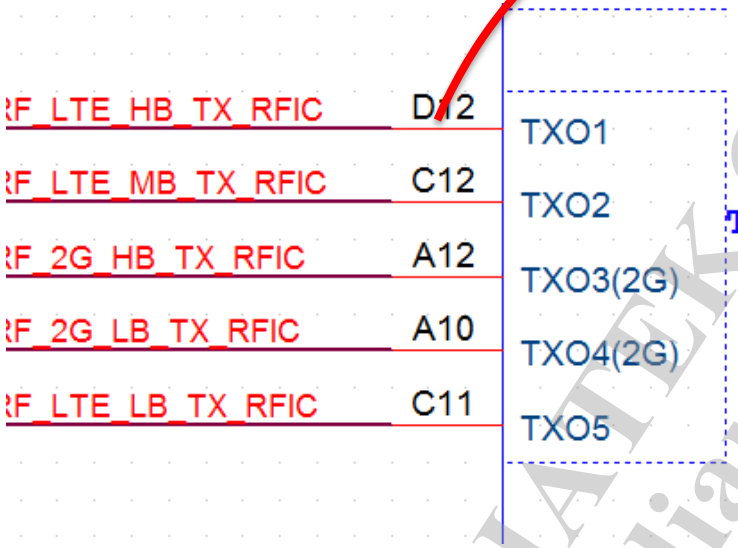
Note8: Mt6177M TX Port Selection

ball name of MT6177M	RF	
	LTE	WCDMA
TXO1	TX_IO_HB1	x
TXO2	TX_IO_MB1	UL1_TX_MB1
TXO3(2G)	x	x
TXO4(2G)	x	x
TXO5	TX_IO_LB2	UL1_TX_LB2

MT6177M_Design_Notice




```
/*-----------------------------------------------------------*/
/*  TX_IO_SEL Definition                                     */
/*-----------------------------------------------------------*/
#define  LTE_Band2_TX_IO_SEL_SetDefault                TX_IO_MB1
#define  LTE_Band4_TX_IO_SEL_SetDefault                TX_IO_MB1
#define  LTE_Band5_TX_IO_SEL_SetDefault                TX_IO_LB2
#define  LTE_Band7_TX_IO_SEL_SetDefault                TX_IO_HB1
#define  LTE_Band12_TX_IO_SEL_SetDefault               TX_IO_LB2
#define  LTE_Band28_TX_IO_SEL_SetDefault               TX_IO_LB2
```

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Note9: Mt6177M RX Port Selection

RFIO port mapping vs. customer file

ball name of MT6177M	RFIO port select_Customer file				
	LTE	WCDMA	2G	C2K	TDSCDMA
TXO1	TX_IO_HB1	x	x	x	x
TXO2	TX_IO_MB1	UL1_TX_MB1	x	TXO2	TDS_TX_TXO2
TXO3(2G)	x	x	No need to define	x	TDS_TX_TXO3 (2G reuse)
TXO4(2G)	x	x	No need to define	x	x
TXO5	TX_IO_LB2	UL1_TX_LB2	x	TXO5	x
PRX1	RX_IO_PRX1	LNA_PRX1	IORX_PRX1	PRX1	TDS_PRX1
PRX2	RX_IO_PRX2	LNA_PRX2	IORX_PRX2	PRX2	TDS_PRX2
PRX3	RX_IO_PRX3	LNA_PRX3	IORX_PRX3	PRX3	TDS_PRX3
PRX4	RX_IO_PRX4	LNA_PRX4	IORX_PRX4	PRX4	TDS_PRX4
PRX5	RX_IO_PRX5	LNA_PRX5	IORX_PRX5	PRX5	TDS_PRX5
PRX6	RX_IO_PRX6	LNA_PRX6	IORX_PRX6	PRX6	TDS_PRX6
PRX7	RX_IO_PRX7	LNA_PRX7	IORX_PRX7	PRX7	TDS_PRX7
PRX8	RX_IO_PRX8	LNA_PRX8	IORX_PRX8	PRX8	TDS_PRX8
SWHB	RX_IO_PRX9	LNA_PRX9	IORX_PRX9	PRX9	TDS_PRXHB
SWLB	RX_IO_PRX10	LNA_PRX10	IORX_PRX10	PRX10	x
DRX1	RX_IO_DRX1	LNA_DRX1	x	DRX1	x
DRX2	RX_IO_DRX2	LNA_DRX2	x	DRX2	x
DRX3	RX_IO_DRX3	LNA_DRX3	x	DRX3	x
DRX4	RX_IO_DRX4	LNA_DRX4	x	DRX4	x
DRX5	RX_IO_DRX5	LNA_DRX5	x	DRX5	x
DRX6	RX_IO_DRX6	LNA_DRX6	x	DRX6	x
DRX7	RX_IO_DRX7	LNA_DRX7	x	DRX7	x
DRX8	RX_IO_DRX8	LNA_DRX8	x	DRX8	x
DRX9	RX_IO_DRX9	LNA_DRX9	x	DRX9	x
DRX10	RX_IO_DRX10	LNA_DRX10	x	DRX10	x

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Note10: USID INITIAL Setting

- Please make sure initial MIPI component which you use in mml1_custom_mipi.c.
- The same USID with different MIPI PORT is OK.

Do not change it in 93 modem but 90/91 Modem must be changed

- For the same USID with same MIPI Port, we should change it in mml1_custom_mipi.c
- All components of RF FE must be initialed with corresponding to MIPI Port if the set from mipi.c file of rat are different to initial table then it lead to modem assert.

```
const MML1_MIPI_INITIAL_CW_T MML1_MIPI_INITIAL_CW_SetDefault[MML1_MIPI_MAX_INITIAL_CW_NUM] =
{
   // elm type     , port_sel        , data_seq  ,      USID              , addr , data   , wait_time(us)
   {MML1_MIPI_PA   , MML1_MIPI_PORT0, MML1_REG_W, MIPI_USID_PA0_SetDefault    , {0x1C, 0x38} , 0 }, // Spe
   {MML1_MIPI_ASM  , MML1_MIPI_PORT1, MML1_REG_W, MIPI_USID_ASM0_SetDefault   , {0x1C, 0x38} , 0 }, // Spe
   {MML1_MIPI_ASM  , MML1_MIPI_PORT3, MML1_REG_W, MIPI_USID_ASM1_SetDefault   , {0x1C, 0x38} , 0 }, // Spe
   {MML1_MIPI_ASM  , MML1_MIPI_PORT1, MML1_REG_W, MIPI_USID_ASM2_SetDefault   , {0x1C, 0x38} , 0 }, // Spe
   {MML1_MIPI_ASM  , MML1_MIPI_PORT3, MML1_REG_W, MIPI_USID_ASM3_SetDefault   , {0x1C, 0x38} , 0 }, // Spe
   {MML1_MIPI_ANT  , MML1_MIPI_PORT2, MML1_REG_W, MIPI_USID_ANT0_SetDefault   , {0x1C, 0x38} , 0 }, // Spe
   {MML1_MIPI_PA   , MML1_MIPI_PORT1, MML1_REG_W, MIPI_USID_PA1_SetDefault    , {0x1C, 0x38} , 0 },
   {MML1_MIPI_END_PATTERN,0,0,0,{0,0},0},
   {MML1_MIPI_END_PATTERN,0,0,0,{0,0},0},
};

/*****************************************************************************
 * MML1 MIPI Change USDI Table Data
 *****************************************************************************/
const MML1_MIPI_USID_CHANGE_T MML1_MIPI_USID_CHANGE_TABLE_SetDefault[MML1_MIPI_MAX_USID_CHANGE_NUM] =
{
   // USID change type   , port_sel        , current USID , PRODUCT_ID , MANUFACTORY_ID   new USID
   {USID REG W           , MML1 MIPI PORT1 , 0xF          , 0x85        , 0x338           , 0xD     },
```

No Matching

Error Ex: lte_custom_mipi.c LTE Band1 Tx data CW

LTE_MIPI_PA , **LTE_MIPI_PORT0** , LTE_REG_W , **MIPI_USID_ASM0_default** ,{ { 19200 /*100 kHz*/ ,0x00 , 0x0C}….

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Note11: eLAN Driver setting

- Must close eLNA setting in mml1_custom_elna.h if it do not need eLNA support otherwise it lead to invalid control for BPI* (as below yellow * show)

```
/*-----------------------------------------------------------------------------*/
/*  Set "GAIN MODE" BPI data for the specific ELNA:                            */
/*  1.PIN0_SetDefault                                                          */
/*    (1) MML1_ELNA_PIN_NONE        : no use                                   */
/*    (2) real number               : define the location of PIN0              */
/*  2.PIN0_ON_DATA_SetDefault                                                  */
/*    (1) real number               : define the data of ELNA ON for PIN0      */
/*    (note) ignore this setting when MML1_ELNA_PIN_NONE                       */
/*  3.PIN0_BYPASS_DATA_SetDefault                                              */
/*    (1) real number               : define the data of ELNA BYPASS for PIN0  */
/*    (note) ignore this setting when MML1_ELNA_PIN_NONE                       */
/*-----------------------------------------------------------------------------*/
/*-----------------------------------------------------------------------------*/
/* PIN selected by all indexes will apply to rg_bpi_top_tpc_agc_AND_en[19:0].  */
/* FDD/C2K/LTE need to set corresponding bits of bpi_out_wlc[19:0] to use ELNA. */
/*-----------------------------------------------------------------------------*/
// The settings for ELNA_NONE
#define  PDATA_MML1_FE_ELNA_NONE_PIN0_SetDefault              MML1_ELNA_PIN_NONE  // the 1s
#define  PDATA_MML1_FE_ELNA_NONE_PIN1_SetDefault              MML1_ELNA_PIN_NONE  // the 2n
#define  PDATA_MML1_FE_ELNA_NONE_PIN0_ON_DATA_SetDefault      0                   // the ON
#define  PDATA_MML1_FE_ELNA_NONE_PIN1_ON_DATA_SetDefault      0                   // the ON
#define  PDATA_MML1_FE_ELNA_NONE_PIN0_BYPASS_DATA_SetDefault  0                   // the BY
#define  PDATA_MML1_FE_ELNA_NONE_PIN1_BYPASS_DATA_SetDefault  0                   // the BY

// The settings for ELNA1
#define  PDATA_MML1_FE_ELNA1_PIN0_SetDefault                  MML1_ELNA_PIN_NONE  // the 1st BP
#define  PDATA_MML1_FE_ELNA1_PIN1_SetDefault                  MML1_ELNA_PIN_NONE  // the 2nd BP
#define  PDATA_MML1_FE_ELNA1_PIN0_ON_DATA_SetDefault          1                   // the ON mod
#define  PDATA_MML1_FE_ELNA1_PIN1_ON_DATA_SetDefault          1                   // the ON mod
#define  PDATA_MML1_FE_ELNA1_PIN0_BYPASS_DATA_SetDefault      0                   // the BYPASS
#define  PDATA_MML1_FE_ELNA1_PIN1_BYPASS_DATA_SetDefault      0                   // the BYPASS

// The settings for ELNA2
#define  PDATA_MML1_FE_ELNA2_PIN0_SetDefault                  MML1_ELNA_PIN_NONE
#define  PDATA_MML1_FE_ELNA2_PIN1_SetDefault                  MML1_ELNA_PIN_NONE
#define  PDATA_MML1_FE_ELNA2_PIN0_ON_DATA_SetDefault          0
#define  PDATA_MML1_FE_ELNA2_PIN1_ON_DATA_SetDefault          1
#define  PDATA_MML1_FE_ELNA2_PIN0_BYPASS_DATA_SetDefault      1
#define  PDATA_MML1_FE_ELNA2_PIN1_BYPASS_DATA_SetDefault      1

// The settings for ELNA3
#define  PDATA_MML1_FE_ELNA3_PIN0_SetDefault                  MML1_ELNA_PIN_NONE
#define  PDATA_MML1_FE_ELNA3_PIN1_SetDefault                  MML1_ELNA_PIN_NONE
#define  PDATA_MML1_FE_ELNA3_PIN0_ON_DATA_SetDefault          0
#define  PDATA_MML1_FE_ELNA3_PIN1_ON_DATA_SetDefault          0
#define  PDATA_MML1_FE_ELNA3_PIN0_BYPASS_DATA_SetDefault      0
#define  PDATA_MML1_FE_ELNA3_PIN1_BYPASS_DATA_SetDefault      0
```

```
/*-----------------------------------------------------------------------------*/
/*  Set "GAIN MODE" BPI data for the specific ELNA:                            */
/*  1.PIN0_SetDefault                                                          */
/*    (1) MML1_ELNA_PIN_NONE        : no use                                   */
/*    (2) real number               : define the location of PIN0              */
/*  2.PIN0_ON_DATA_SetDefault                                                  */
/*    (1) real number               : define the data of ELNA ON for PIN0      */
/*    (note) ignore this setting when MML1_ELNA_PIN_NONE                       */
/*  3.PIN0_BYPASS_DATA_SetDefault                                              */
/*    (1) real number               : define the data of ELNA BYPASS for PIN0  */
/*    (note) ignore this setting when MML1_ELNA_PIN_NONE                       */
/*-----------------------------------------------------------------------------*/
/*-----------------------------------------------------------------------------*/
/* PIN selected by all indexes will apply to rg_bpi_top_tpc_agc_AND_en[19:0].  */
/* FDD/C2K/LTE need to set corresponding bits of bpi_out_wlc[19:0] to use ELNA. */
/*-----------------------------------------------------------------------------*/
// The settings for ELNA_NONE
#define  PDATA_MML1_FE_ELNA_NONE_PIN0_SetDefault              MML1_ELNA_PIN_NONE  // th
#define  PDATA_MML1_FE_ELNA_NONE_PIN1_SetDefault              MML1_ELNA_PIN_NONE  // th
#define  PDATA_MML1_FE_ELNA_NONE_PIN0_ON_DATA_SetDefault      0                   // th
#define  PDATA_MML1_FE_ELNA_NONE_PIN1_ON_DATA_SetDefault      0                   // th
#define  PDATA_MML1_FE_ELNA_NONE_PIN0_BYPASS_DATA_SetDefault  0                   // th
#define  PDATA_MML1_FE_ELNA_NONE_PIN1_BYPASS_DATA_SetDefault  0                   // th

// The settings for ELNA1 :B1,  PRX, BPI,  On mode,    w/  2nd SAW
#define  PDATA_MML1_FE_ELNA1_PIN0_SetDefault                  4                   // the 1st
#define  PDATA_MML1_FE_ELNA1_PIN1_SetDefault                  5                   // the 2nd
#define  PDATA_MML1_FE_ELNA1_PIN0_ON_DATA_SetDefault          1                   // the ON
#define  PDATA_MML1_FE_ELNA1_PIN1_ON_DATA_SetDefault          1                   // the ON
#define  PDATA_MML1_FE_ELNA1_PIN0_BYPASS_DATA_SetDefault      0                   // the BY
#define  PDATA_MML1_FE_ELNA1_PIN1_BYPASS_DATA_SetDefault      1                   // the BY

// The settings for ELNA2 :B2,  PRX, BPI,  On mode,    w/  2nd SAW
#define  PDATA_MML1_FE_ELNA2_PIN0_SetDefault                  8
#define  PDATA_MML1_FE_ELNA2_PIN1_SetDefault                  9
#define  PDATA_MML1_FE_ELNA2_PIN0_ON_DATA_SetDefault          1
#define  PDATA_MML1_FE_ELNA2_PIN1_ON_DATA_SetDefault          1
#define  PDATA_MML1_FE_ELNA2_PIN0_BYPASS_DATA_SetDefault      0
#define  PDATA_MML1_FE_ELNA2_PIN1_BYPASS_DATA_SetDefault      1

// The settings for ELNA3 :B1,  DRX, BPI,  On mode,    w/  2nd SAW
#define  PDATA_MML1_FE_ELNA3_PIN0_SetDefault                  6
#define  PDATA_MML1_FE_ELNA3_PIN1_SetDefault                  7
#define  PDATA_MML1_FE_ELNA3_PIN0_ON_DATA_SetDefault          1
#define  PDATA_MML1_FE_ELNA3_PIN1_ON_DATA_SetDefault          1
#define  PDATA_MML1_FE_ELNA3_PIN0_BYPASS_DATA_SetDefault      0
#define  PDATA_MML1_FE_ELNA3_PIN1_BYPASS_DATA_SetDefault      1
```

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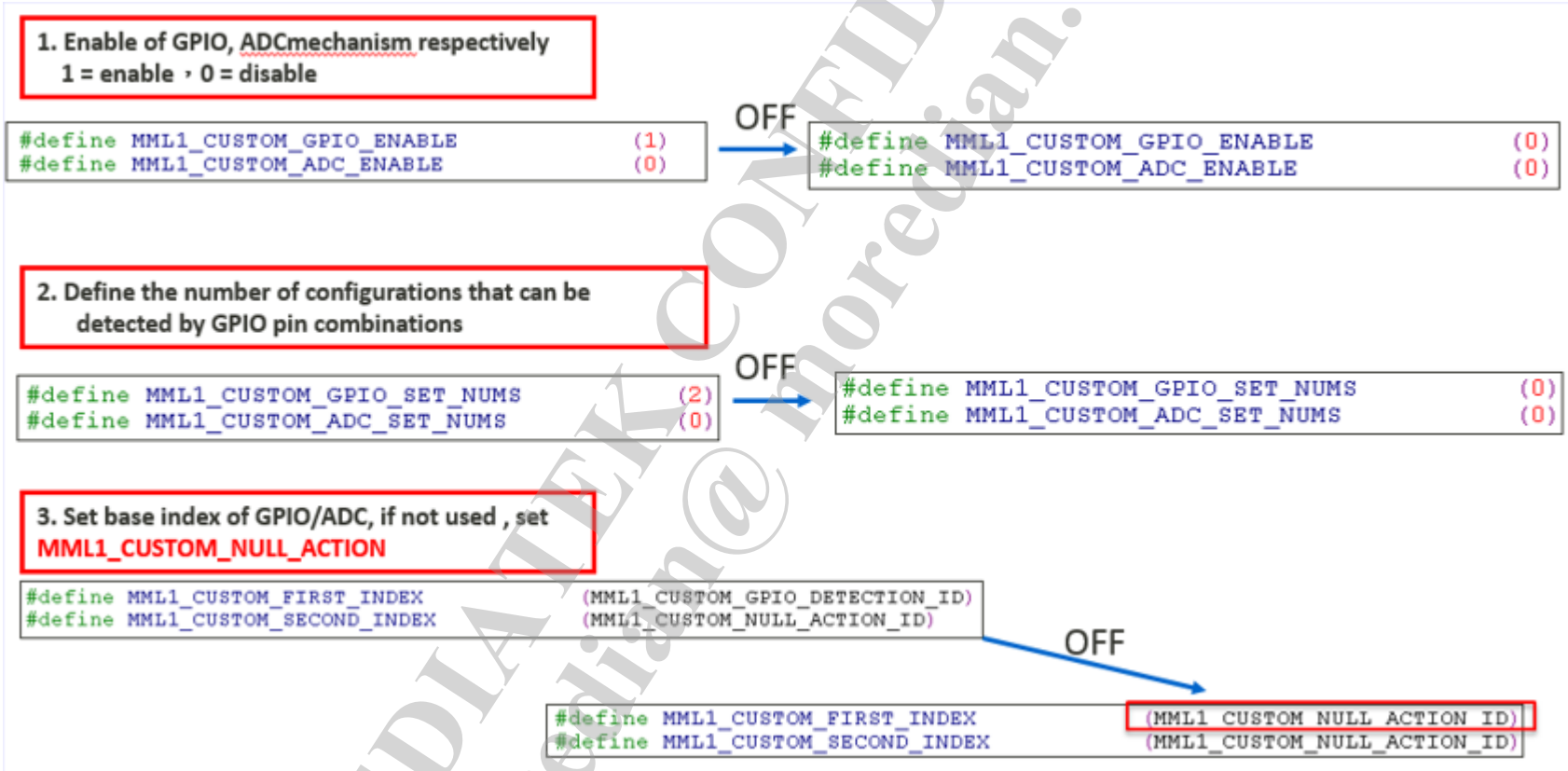
Note12-1: DRDI Driver setting

- If DRDI do not need to support, must close the setting in mml1_custom_drdi.h as below otherwise it leads to invalid setting for all default file



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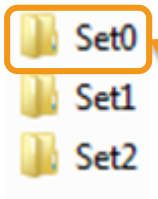
Note12-2: DRDI Driver setting

- If we use DRDI, we should configure mapping in mml1_custom_drdi.c
- All RAT, please refer to DRDI reference document
- Ex. 2G Remapping

DRDI Set0




```
kal_uint16 MML1_DRDI_GGE_ReMapTable[] =
{  /* 00  ~  (MML1_CUSTOM_TOTAL_SET_NUMS-1) */
   /* 00 */
       0,
   #if IS_MML1_DRDI_ENABLE
   /*      01,  02,  03,  04,  05,  06,  07,  08,  09, */
             1,   0,   0,   4,   5,   6,   7,   8,   9,
   /* 10,  11,  12,  13,  14,  15,  16,  17,  18,  19, */
      0,   11,  12,  13,  14,  15,  16,  17,  18,  19,
   /* 20,  21,  22,  23,  24,  25,  26,  27,  28,  29, */
      20,  21,  22,  23,  24,  25,  26,  27,  28,  29,
   /* 30,  31,  32,  33,  34,  35,  36,  37,  38,  39, */
      30,  31,  32,  33,  34,  35,  36,  37,  38,  39,
   /* 40,  41,  42,  43,  44,  45,  46,  47,  48,  49, */
      40,  41,  42,  43,  44,  45,  46,  47,  48,  49,
   /* 50,  51,  52,  53,  54,  55,  56,  57,  58,  59, */
      50,  51,  52,  53,  54,  55,  56,  57,  58,  59,
   /* 60,  61,  62,  63,  64,  65,  66,  67,  68,  69, */
      60,  61,  62,  63,  64,  65,  66,  67,  68,  69,
   /* 70,  71,  72,  73,  74,  75,  76,  77,  78,  79, */
      70,  71,  72,  73,  74,  75,  76,  77,  78,  79,
   /* 80,  81,  82,  83,  84,  85,  86,  87,  88,  89, */
      80,  81,  82,  83,  84,  85,  86,  87,  88,  89,
   /* 90,  91,  92,  93,  94,  95,  96,  97,  98,  99, */
      90,  91,  92,  93,  94,  95,  96,  97,  98,  99,
   /*100, 101, 102, 103, 104, 105, 106, 107, 108, 109, */
     100, 101, 102, 103, 104, 105, 106, 107, 108, 109,
```

Ex: GPIO list

Configuration Index	GPIO Input Voltage 3RD_PIN	GPIO Input Voltage 2ND_PIN	GPIO Input Voltage 1ST PIN
0 (Set 0)	0	0	0 (low potential)
1 (Set 1)	0	0	1
...	...	...	...
6 (Set 6)	1	1	0
7 (Set 7)	1	1	1

One index maps to one HW configuration hybrid type

組態編號	GPIO輸入電位 (pin 2)	GPIO輸入電位 (pin 1)	GPIO (pin1/2) 對應準位	ADC輸入電壓準位	組態編號計算方法
0 (Set0)	0	0	0	0	0x2+0
1 (Set1)	0	0	0	1	0x2+1
2 (Set2)	0	1	1	0	1x2+0
3 (Set3)	0	1	1	1	1x2+1
4 (Set4)	1	0	2	0	2x2+0
5 (Set5)	1	0	2	1	2x2+1
6 (Set6)	1	1	3	0	3x2+0
7 (Set7)	1	1	3	1	3x2+1

Ex: GPIO pin 1 = 0，pin 2 = 1，ADC input voltage = 1，the index will be 5 (= 2x2 + 1)

Second index
First index
First index base (1)
2x2+1
Second index base (2)

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Note13: C2K Tx No Power issue

- Tx On Event set ASM to the correct TRX Port
- Tx On Event set PA Enable
- TX On Event must not set PA Bias CW even through Bias is zero
- Tx Gate On set PA Enable
- TX Gate On does not set Pa Bias
- TPC set PA Bias
- TPC Event should be earlier than TX gate on event

```
/* TX Event */
C2K_MIPI_EVENT_TABLE_T C2K_BAND_A_MIPI_TX_EVENT_SetDefault[] =
{
   /* No.     elm type      , data idx      , evt_type        , evt_offset              */
   /*                         { start, stop },                  ( us )                  */
   { /* 0   */ C2K_MIPI_PA   ,   { 0     , 0     }, C2K_MIPI_TRX_ON      , C2K_MIPI_PA_TX_ON0_SetDefault   },
   { /* 1   */ C2K_MIPI_PA   ,   { 1     , 1     }, C2K_MIPI_TRX_OFF     , C2K_MIPI_PA_TX_OFF0_SetDefault },
   { /* 2   */ C2K_MIPI_PA   ,   { 2     , 2     }, C2K_MIPI_TX_GATE_ON  , C2K_MIPI_PA_TX_GATE_ON0_SetDefault  },
   { /* 3   */ C2K_MIPI_PA   ,   { 3     , 3     }, C2K_MIPI_TX_GATE_OFF , C2K_MIPI_PA_TX_GATE_OFF0_SetDefault },
   { /* 4   */ C2K_MIPI_ASM  ,   { 4     , 5     }, C2K_MIPI_TRX_ON      , C2K_MIPI_ASM_TX_ON0_SetDefault },
   { /* 5   */ C2K_MIPI_ANT  ,   { 6     , 6     }, C2K_MIPI_TRX_ON      , C2K_MIPI_ANT_TX_ON0_SetDefault },
   { /* 6   */ C2K_MIPI_NULL,    { 0     , 0     }, C2K_MIPI_EVENT_NULL, 0                          },
C2K_MIPI_DATA_SUBBAND_TABLE_T C2K_BAND_A_MIPI_TX_DATA_SetDefault[] =
{
  //No.      elm type     , port_sel          , data_seq       , USID                     ,{ { subband-0 freq    ,addr ,data }, { subband-1 f
  { /* 0 */ C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W      , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x00 ,0x20} },
            C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W      , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x01 ,0x00} },
            C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W      , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x03 ,0x00} },
  { /* 1 */ C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W      , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x00 ,0x00} },
  { /* 2 */ C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W      , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x00 ,0x20} },
  { /* 3 */ C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W      , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x00 ,0x00} },

 /*MIPI PA     */
 /* TX ON     */
 #define   C2K_MIPI_PA_TX_ON0_SetDefault                 M_US(10)
 #define   C2K_MIPI_PA_TX_ON1_SetDefault                 M_US(0)
/*MIPI PA     */
/* TX OFF     */
#define   C2K_MIPI_PA_TX_OFF0_SetDefault                M_US(10)
#define   C2K_MIPI_PA_TX_OFF1_SetDefault                M_US(0)
```

Tx On Pa Enable

0x01,0x03 Bias register; No reserve in Tx Event CW

Gate on Pa Enable

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Note14: TDSCDMA TX Reuse TXM （2G H Band PA）and USID define

- TXM Reuse need configure in MIPI.h and USID use constant ID defined in mml1_custom_mipi.h

```
/*-------------------------------------------------------------------------*/
/*   MIPI Module CONFIGURATION                                             */
/*-------------------------------------------------------------------------*/
/*MT6177M*/   #define  TDD_TXM_FLAG_BAND34_SetDefault      (0 <<0)  /*1: TXM DEVICE*/
                                                                    /*0: NORMAL DEVICE*/
/*MT6177M*/   #define  TDD_TXM_FLAG_BAND39_SetDefault      (0 <<1)  /*1: TXM DEVICE*/
                                                                    /*0: NORMAL DEVICE*/

/*MT6177M*/   #define  TDD_ASM_USID_BAND34_SetDefault     (MIPI_USID_ASM0_SetDefault <<3)
/*MT6177M*/   #define  TDD_ASM_USID_BAND39_SetDefault     (MIPI_USID_ASM0_SetDefault <<3)
/*MT6177M*/   #define  TDD_PA_USID_BAND34_SetDefault      (MIPI_USID_ASM0_SetDefault <<3)
/*MT6177M*/   #define  TDD_PA_USID_BAND39_SetDefault      (MIPI_USID_ASM0_SetDefault <<3)
/*MT6177M*/   #define  TDD_ETM_USID_SetDefault            (0 << 3)//no use
/*MT6177M*/   #define  TDD_MIPI_ANT_SetDefault            (MIPI_USID_ANT0_SetDefault <<3)

/*-------------------------------------------------------------------------*/
```

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Note15: How to disable the 2G Band

- Project make file : BAND_SUPPORT **= QUAD**
- Custom\modem\l1_rf\mt6763_2g_mt6177l_sp)\M12193.c

  Enable or Disable 2G Band

  - DRDI disable

```
const sl1CustomBandSupport l1d_custom_band_support_SetDefault=
  {
    1, //Support GSM850  Band  // 0 disable，1 enable
    1, //Support GSM900  Band  // 0 disable，1 enable
    1, //Support DCS1800 Band // 0 disable，1 enable
    1, //Support PCS1900 Band // 0 disable，1 enable
  };
```

  - DRDI Enable custom\modem\l1_rf\mt6763_2g_mt6177l_sp\drdi\set*\M12193.c

```
const sl1CustomBandSupport l1d_custom_band_support_Set*=
{
  1, //Support GSM850  Band// 0 disable，1 enable
  1, //Support GSM900  Band// 0 disable，1 enable
  1, //Support DCS1800 Band// 0 disable，1 enable
  1, //Support PCS1900 Band// 0 disable，1 enable
};
```

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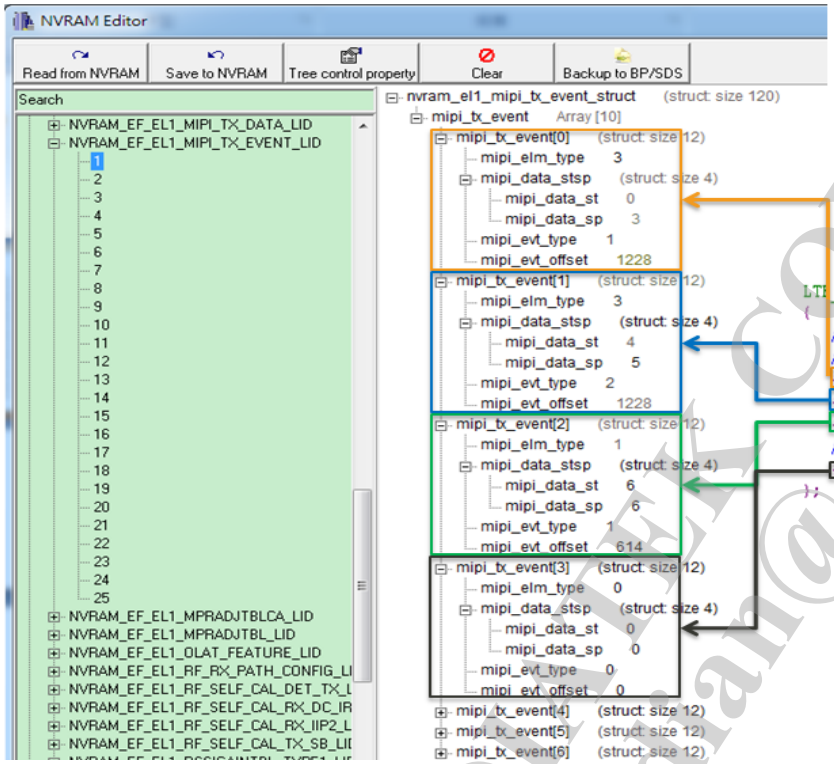
Note16: LTE Tx Timing tuning by NVRAM

- The value in NVRAM is 61.44*US2OFFCNT while MT6737 is 26*US2OFFCNT



file: lte_custom_mipi.c

```
#define LTE_FDD_MIPI_PA_TX_ON0_SetDefault     US20FFCNT(20)

#define LTE_FDD_MIPI_PA_TX_OFF0_SetDefault    US20FFCNT(20)

LTE_MIPI_EVENT_TABLE_T LTE_Band1_MIPI_TX_EVENT_SetDefault[] =
{
/* No.    elm type    , data idx      , evt_type          , evt_offset          */
/*                      [ start, stop ],                   ( us )               */
{ /* 0 */ LTE_MIPI_PA  , { 0    , 3    }, LTE_MIPI_TRX_ON    , LTE_FDD_MIPI_PA_TX_ON0_SetDefault  }, //PA On
{ /* 1 */ LTE_MIPI_PA  , { 4    , 5    }, LTE_MIPI_TRX_OFF   , LTE_FDD_MIPI_PA_TX_OFF0_SetDefault }, //PA Off
{ /* 2 */ LTE_MIPI_ASM , { 6    , 6    }, LTE_MIPI_TRX_ON    , LTE_FDD_MIPI_ASM_TX_ON0_SetDefault }, //WIN on
//{ /* 3 */ LTE_MIPI_ASM , { 7    , 7    }, LTE_MIPI_TRX_OFF   , LTE_FDD_MIPI_ASM_TX_OFF0_SetDefault },//WIN off
{ /* 4 */ LTE_MIPI_NULL, { 0    , 0    }, LTE_MIPI_EVENT_NULL, 0                    },
};

#define LTE_FDD_MIPI_ASM_TX_ON0_SetDefault    US20FFCNT(10)
```

NOTE:
US2OFFCNT(10) = 10 * 6144/100 = 614.4 → 614
US2OFFCNT(20) = 20 * 6144/100 = 1228.8 → 1228

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Note17: LTE_MIPI_PA Element type used

- The **LTE_MIPI_PA** of element type does not be used into RX Event Table otherwise it leads to modem assert/exception as the below

Assert fail: **lrfmipidata.c 1242 0x3 0x6 0x0** - MMF_PCO

Note: If the 3P4T of MMMB PA for LTE TDD Band is used, do not set LTE_MIPI_PA and must set LTE_MIPI_ASM in Rx Event Table

```
LTE_MIPI_EVENT_TABLE_T LTE_Band38_MIPI_RX_EVENT_SetDefault[] =
{
    /* No.     elm type     , data idx       , evt_type          , evt_offset              */
    /*                        { start, stop },                    ( us )                   */
    { /* 0  */ LTE_MIPI_ASM , { 0    , 0    }, LTE_MIPI_TRX_ON   , LTE_TDD_MIPI_ASM_RX_ON0_SetDefault  },
    { /* 1  */ LTE_MIPI_PA , { 1    , 1    }, LTE_MIPI_TRX_ON   , LTE_TDD_MIPI_PA_TX_ON0_SetDefault   }, //3P4T TRX Port On
    { /* 2  */ LTE_MIPI_ASM , { 2    , 2    }, LTE_MIPI_TRX_OFF  , LTE_TDD_MIPI_ASM_RX_OFF0_SetDefault },
    { /* 3  */ LTE_MIPI_PA , { 3    , 3    }, LTE_MIPI_TRX_OFF  , LTE_TDD_MIPI_PA_TX_OFF0_SetDefault  },
    { /* 4  */ LTE_MIPI_NULL, { 0    , 0    }, LTE_MIPI_EVENT_NULL, 0                              },
};
```

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Note18: Ant tuner setting

- LTE
  - Rule1: TAS closed by band, ant tuner set in OLAT
  - Rule2: TAS opened by band, ant tuner **set only** in CATB Table only
  - Rule3: TAS HW Support by band*, configuration of ant tuner must set in CATB Table
  - Rule4: Open or close TAS by Band* in different design stage, CATB and OLAT both set for ant tuner
  - Rule5: TAS opened for NCCA band , both CATB and OLAT both set for the band of NCCA

Note: LTE does not recommend configuring a tuner in a regular location because we have a place where OLAT tuner is specifically configured. Refer to DCC:《MT6293_TAS_Csutomization_SOP.ppt》pp. 42~51

- Other RAT
  - Rule: Recommend to set a tuner in a regular location TX/RX BPI

But considering that if TAS is likely to close some bands at a certain stage, when TAS is closed, it is important to configure the tuner in regular location in RF Driver Code

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93 Modem typical Case study Case1

Description

Mt6739 Project Modem unable start

Root cause

The hw version of Mt6739 does not support 700M Band (B71) and DRDI does not close

[1][core1,vpe0,tc0(vpe2)] Fatal Error (0x10e, 0x90a46cc1, 0xcccccccc) - TIMER_H, Caller Address: 0x90a46cc1
Product: LR12A.R2.MP TK_MD_BASIC Version: MOLY.LR12A.R2.MP.V20.1 BuildTime: 2018/04/26 15:23

Main Chip	L+G only	L+W/L+L/ 600MHz	L+W/L+L/ 600MHz/ HPUE
5-Mode	6739WA	6739WW	-
6-Mode	-	6739CW	6739CH

0504-modem-rf\mml1_rf\MT6739_MMRF_MT6177M\mml1_custom_drdi.h
#define MML1_CUSTOM_GPIO_ENABLE (0)
#define MML1_CUSTOM_ADC_ENABLE (1)

Set1

SingleBand Setting		
BAND_INDICATOR_ID	(LTE_BAND)	SUPPORT(SW capability)
BAND_INDICATOR0	LTE_Band1	SW_CAPABILITY_SUPPORT
...	...	...
BAND_INDICATOR16	LTE_Band66	SW_CAPABILITY_SUPPORT
BAND_INDICATOR17	LTE_Band71	SW_CAPABILITY_SUPPORT

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93 Modem typical Case study Case2

Description

Mt6763 modem assert:

fatal error code 1,2,3 = [0x00001010, 0xFFFFFFFF, 0x00000000]MD Offender:DSP_1st

Root cause

The hw version of Mt6763 does not support CAT7 (UL CCA0) but UL CCA set in driver code(need to close UL CCA)

BAND_INDICATOR_ID	(LTE_BAND)	RX_eLNAIDX	RXD_eLNAIDX	CCA_Support(TX)
BAND_INDICATOR0	LTE_Band1	MML1_FE_ELNA_NONE	MML1_FE_ELNA_NONE	NO_CCA_SUPPORT
BAND_INDICATOR1	LTE_Band3	MML1_FE_ELNA_NONE	MML1_FE_ELNA_NONE	NO_CCA_SUPPORT
BAND_INDICATOR2	LTE_Band5	MML1_FE_ELNA_NONE	MML1_FE_ELNA_NONE	NO_CCA_SUPPORT
BAND_INDICATOR3	LTE_Band7	MML1_FE_ELNA_NONE	MML1_FE_ELNA_NONE	NO_CCA_SUPPORT
BAND_INDICATOR4	LTE_Band8	MML1_FE_ELNA_NONE	MML1_FE_ELNA_NONE	NO_CCA_SUPPORT
BAND_INDICATOR5	LTE_Band20	MML1_FE_ELNA_NONE	MML1_FE_ELNA_NONE	NO_CCA_SUPPORT
BAND_INDICATOR6	LTE_Band34	MML1_FE_ELNA_NONE	MML1_FE_ELNA_NONE	NO_CCA_SUPPORT
BAND_INDICATOR7	LTE_Band38	MML1_FE_ELNA_NONE	MML1_FE_ELNA_NONE	NO_CCA_SUPPORT
BAND_INDICATOR8	LTE_Band39	MML1_FE_ELNA_NONE	MML1_FE_ELNA_NONE	NO_CCA_SUPPORT
BAND_INDICATOR9	LTE_Band40	MML1_FE_ELNA_NONE	MML1_FE_ELNA_NONE	NO_CCA_SUPPORT
BAND_INDICATOR10	LTE_Band41	MML1_FE_ELNA_NONE	MML1_FE_ELNA_NONE	NO_CCA_SUPPORT

INTRA BAND CCA Configuration				HW capability	SW capability	HW capability
Downlink	Uplink	UL_CC1_FE_Route(No used)	BW_COMBINATION_SETS	Calibration	UE Capability	generate by tool
1C	1A		0x1	TRUE	Enable	TRUE
3B	3A		0x1	TRUE	Enable	TRUE
3C	3A		0x1	TRUE	Enable	TRUE
3C	3C		0x1	FALSE	Disable	FALSE
5B	5A		0x3	TRUE	Enable	TRUE
5B	5B		0x3	FALSE	Disable	FALSE
7B	7A		0x1	TRUE	Enable	TRUE
7C	7A		0x7	TRUE	Enable	TRUE
7C	7C		0x7	FALSE	Disable	FALSE

		No UL CCA	Support UL CCA
		MT6763	MT6763T
6-mode	cat-7		MT6763V/CT
	cat-6	MT6763V/B	
5-mode	cat-7		MT6763V/WT
	cat-6	MT6763V/V	

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93 Modem typical Case study Case3

Description

Mt6763 modem assert:

[1][core0,vpe1,tc1(vpe1)] Fatal Error (Cross Core Exception) Triggered by USIP : ECT \ status(0x00000042): (0x3108, 0x61a79dac)

Root cause

The hw version of Mt6763V/**V** does not support 6 Mode but modem driver set 6 Mode in driver (it must be used to 5M Modem image)

		MT6763	MT6763T
6-mode	cat-7		MT6763V/CT
	cat-6	MT6763V/B	
5-mode	cat-7		MT6763V/WT
	cat-6	MT6763V/V	

```
ECT status(0x00000042): (0x3108, 0x6199d1ec)"
```

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93 Modem typical Case study Case4

Description

Mt6739 project CTA network C2K registration fail

Root cause

1.C2K BC0 TX Event set PA Bias(need to remove bias set CW)

2.TX On/off timing is 20us(need to change 20us)

3.Tx On event does not set pa enable(need set pa enable)

```
/* TX Event */
C2K_MIPI_EVENT_TABLE_T C2K_BAND_A_MIPI_TX_EVENT_SetDefault[] =
{
   /* No.      elm type      , data idx       , evt_type        , evt_offset          */
   /*                         { start, stop },                  ( us )                */
   { /* 0  */ C2K_MIPI_PA   ,    { 0    , 0    }, C2K_MIPI_TRX_ON      , C2K_MIPI_PA_TX_ON0_SetDefault  },
   { /* 1  */ C2K_MIPI_PA   ,    { 1    , 1    }, C2K_MIPI_TRX_OFF     , C2K_MIPI_PA_TX_OFF0_SetDefault },
   { /* 2  */ C2K_MIPI_PA   ,    { 2    , 2    }, C2K_MIPI_TX_GATE_ON  , C2K_MIPI_PA_TX_GATE_ON0_SetDefault  },
   { /* 3  */ C2K_MIPI_PA   ,    { 3    , 3    }, C2K_MIPI_TX_GATE_OFF , C2K_MIPI_PA_TX_GATE_OFF0_SetDefault },
   { /* 4  */ C2K_MIPI_ASM  ,    { 4    , 5    }, C2K_MIPI_TRX_ON      , C2K_MIPI_ASM_TX_ON0_SetDefault },
   { /* 5  */ C2K_MIPI_ANT  ,    { 6    , 6    }, C2K_MIPI_TRX_ON      , C2K_MIPI_ANT_TX_ON0_SetDefault },
   { /* 6  */ C2K_MIPI_NULL,     { 0    , 0    }, C2K_MIPI_EVENT_NULL, 0                },
C2K_MIPI_DATA_SUBBAND_TABLE_T C2K_BAND_A_MIPI_TX_DATA_SetDefault[] =
{
   //No.      elm type     , port_sel          , data_seq      , USID                ,{ { subband-0 freq    ,addr ,data }, { subband-1 f
   { /* 0 */ C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W     , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x00 ,0x20} }, Tx On  Pa Enable
            C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W     , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x01 ,0x00} }, 0x01,0x03 Bias register;
            C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W     , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x03 ,0x00} }, No reserve in Tx Event CW
   { /* 1 */ C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W     , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x00 ,0x00} },
   { /* 2 */ C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W     , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x00 ,0x20} }, Gate on Pa Enable
   { /* 3 */ C2K_MIPI_PA  , C2K_MIPI_PORT0    , C2K_REG_W     , MIPI_USID_PA0_SetDefault    ,{ { 8150  /*100 kHz*/ , {0x00 ,0x00} },

/*MIPI PA     */
/* TX ON    */
#define  C2K_MIPI_PA_TX_ON0_SetDefault          M_US(10)
#define  C2K_MIPI_PA_TX_ON1_SetDefault          M_US(0)
/*MIPI PA     */
/* TX OFF    */
#define  C2K_MIPI_PA_TX_OFF0_SetDefault         M_US(10)
#define  C2K_MIPI_PA_TX_OFF1_SetDefault         M_US(0)
```

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93 Modem typical Case study Case5

Description

Mt6739 BPI 5/6 do not control by Modem

Root cause

BPI* are set by ELNA file in early default sw branch (if hw does not support eLNA, need to set MML1_ELNA_PIN_NONE)

```
/*-----------------------------------------------------------------------------
/*-----------------------------------------------------------------------------
/* PIN selected by all indexes will apply to rg_bpi_top_tpc_agc_AND_en[19:0].
/* FDD/C2K/LTE need to set corresponding bits of bpi_out_wlc[19:0] to use ELNA.
/*-----------------------------------------------------------------------------
// The settings for ELNA_NONE
#define  PDATA_MML1_FE_ELNA_NONE_PIN0_SetDefault              MML1_ELNA_PIN_NONE
#define  PDATA_MML1_FE_ELNA_NONE_PIN1_SetDefault              MML1_ELNA_PIN_NONE
#define  PDATA_MML1_FE_ELNA_NONE_PIN0_ON_DATA_SetDefault      0
#define  PDATA_MML1_FE_ELNA_NONE_PIN1_ON_DATA_SetDefault      0
#define  PDATA_MML1_FE_ELNA_NONE_PIN0_BYPASS_DATA_SetDefault  0
#define  PDATA_MML1_FE_ELNA_NONE_PIN1_BYPASS_DATA_SetDefault  0

// The settings for ELNA1 :B1,  PRX, BPI,  On mode,     w/  2nd SAW
#define  PDATA_MML1_FE_ELNA1_PIN0_SetDefault                  4                  // t
#define  PDATA_MML1_FE_ELNA1_PIN1_SetDefault                  5                  // t
#define  PDATA_MML1_FE_ELNA1_PIN0_ON_DATA_SetDefault          1                   //
#define  PDATA_MML1_FE_ELNA1_PIN1_ON_DATA_SetDefault          1                   //
#define  PDATA_MML1_FE_ELNA1_PIN0_BYPASS_DATA_SetDefault      0                   //
#define  PDATA_MML1_FE_ELNA1_PIN1_BYPASS_DATA_SetDefault      1                   //
```

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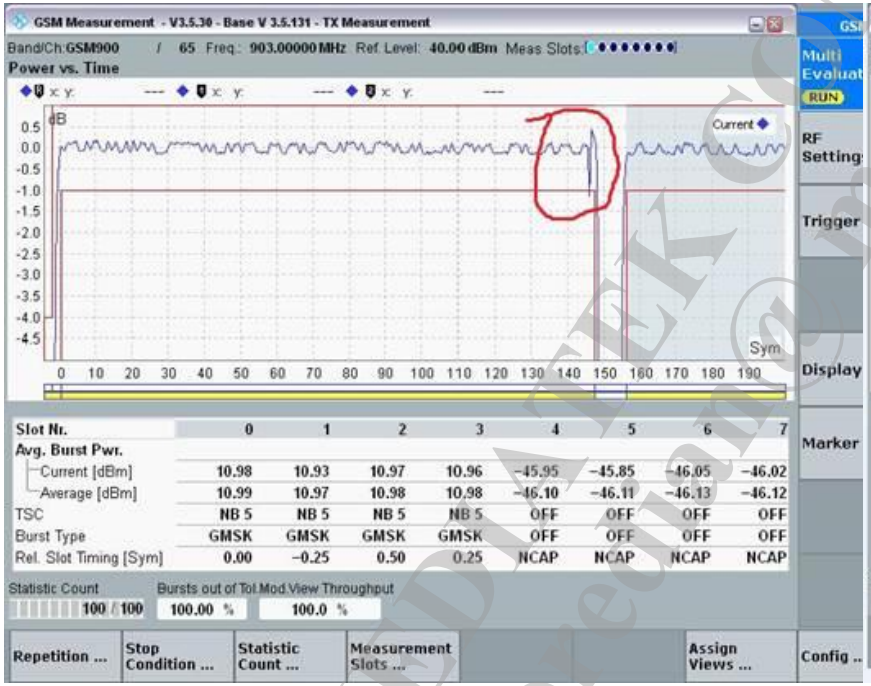
93 Modem typical Case study Case6

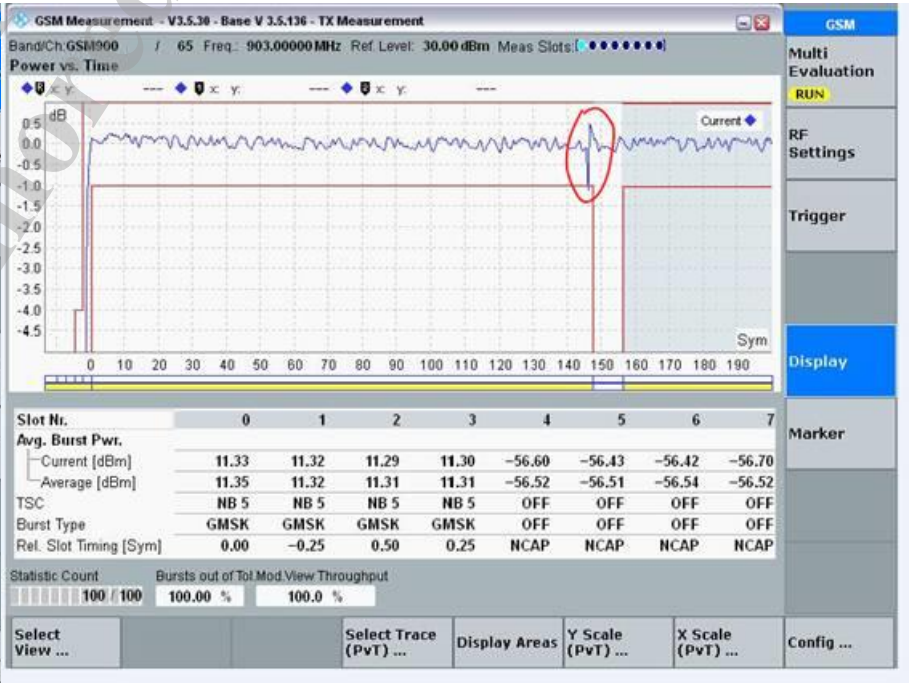
➢ Description

Mt6739 2G GPRS multi-slot PVT test FAIL (CASE 13.16.2.4.1) for some TXM

➢ Root cause

QB_MIPI_TXMID0_GG_SetDefault value is changed from 20 to 5 in order to move spur to the middle of the slot





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93 Modem typical Case study Case7

Description

Mt6739 modem assert:

md1:(MCU_core1.vpe1.tc1(VPE3)) [ASSERT] file:mcu/l1core/modem/el1/el1d/src/tpc/ltpcctrl.c line:8668

p1:0x00000000 p2:0x00000000 p3:0x00000000

Root cause

The USID of CW for TPC Section is not matching to HW design so modem can not get any respond from MMMB PA

1) mml1_custom_mipi.c/mml1_custom_mipi.h

```
#define MIPI_USID_PA0_SetDefault        0x000B
```

2)lte_custom_mipi

```
LTE_MIPI_DATA_TABLE_T LTE_Band39_MIPI_TPC_DATA_SetDefault[] =
{
  //No.    elm type      , port_sel      , data_seq    , USID                    , address
  {/* 0  */ LTE_MIPI_PA_SEC, LTE_MIPI_PORT0   , LTE_REG_W   , MIPI_USID_PA0_SetDefault
LTE_MIPI_PA_SECTION_ADDRESS  , LTE_MIPI_PA_SECTION_DATA0}, // PA mode, path sel
  {/* 1  */ LTE_MIPI_PA_SEC, LTE_MIPI_PORT0   , LTE_REG_W   , MIPI_USID_PA0_SetDefault
LTE_MIPI_PA_SECTION_ADDRESS  , LTE_MIPI_PA_SECTION_DATA1}, // PA bias
```

LTE B39 TPC_DATA Table MIPI Port : Port0, UISD_PA0:0x0B

```
LTE_MIPI_TPC_SECTION_TABLE_T LTE_Band39_MIPI_PA_SECTION_DATA_SetDefault[] =
{
  {
  18800, /*100kHz*/
  MIPI_USID_ASM0_SetDefault, /*USID*/
```

No Matching

LTE B39 TPC_SECTION Table USID ASM0 :0x0F

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93 Modem typical Case study Case8

Description

Mt6739 modem assert:

Assert fail: **ltpcctrl.c 8557 0x0 0x0 0x0** - 0CMMN_E

Root cause

The MIPI CW is sent to RF Part of USID being 0X0F by MIPI1 bus but modem does not get any respond from the Part because HW MIPI bus of the RF part is MIPI0.

The MIPI port of CW set error because DRDI is enable so that the set of customer is invalid.

mml1_customer_drdi.h

#define MMl1_CUSTOM_GPIO_ENABLE (0)

#define MMl1_CUSTOM_ADC_ENABLE (1)

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93 Modem typical Case study Case9

Description

Mt6739 modem assert:

Assert fail: META_DLL_HANDLE[4152][2084]: SYSTEM: <0> Confirm: sysCB():

"[1][core0,vpe1,tc1(vpe1)] Assert fail**: lrfroutedatabase.c 2434** - (LISR)

Root cause

There are interval set of Bandnone for Bandindicator in R1 Modem Branch.

Need to check in patch:MOLY00287936 in R1 sw modem version.

This issue have modified in R2 or Later modem Version.

Note:

SingleBand Setting						
BAND_INDICATOR_ID	(LTE_BAND)	SUPPORT(SW capability)	RX_IO_SEL	RXD_IO_SEL	PDATA_PR1	PDATA_PR2
BAND_INDICATOR0	LTE_Band1	SW_CAPABILITY_SUPPORT	RX_IO_PRX10	RX_IO_DRX10	0x00000000	0x00000000
BAND_INDICATOR1	LTE_BandNone	SW_CAPABILITY_NOT_SUPPORT	RX_IO_NON_USED	RXD_IO_NON_USED	0x00000000	0x00000000
BAND_INDICATOR2	LTE_Band3	SW_CAPABILITY_SUPPORT	RX_IO_PRX7	RX_IO_DRX7	0x00000000	0x00000000
BAND_INDICATOR3	LTE_BandNone	SW_CAPABILITY_NOT_SUPPORT	RX_IO_NON_USED	RXD_IO_NON_USED	0x00000000	0x00000000
BAND_INDICATOR4	LTE_Band5	SW_CAPABILITY_SUPPORT	RX_IO_PRX4	RX_IO_DRX4	0x00000000	0x00000000
BAND_INDICATOR5	LTE_Band7	SW_CAPABILITY_SUPPORT	RX_IO_PRX13	RX_IO_DRX13	0x00000000	0x00000000
BAND_INDICATOR6	LTE_Band8	SW_CAPABILITY_SUPPORT	RX_IO_PRX2	RX_IO_DRX2	0x00000000	0x00000000
BAND_INDICATOR7	LTE_Band38	SW_CAPABILITY_SUPPORT	RX_IO_PRX9	RX_IO_DRX9	0x00000000	0x00000000
BAND_INDICATOR8	LTE_Band39	SW_CAPABILITY_SUPPORT	RX_IO_PRX14	RX_IO_DRX14	0x00000000	0x00000000

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93 Modem typical Case study Case10

Description

Mt6739 project, EVM of LTEband1/3/8/7/28 fail (EVM RMS 8.9%) or In band emission fail for **20M/10M BW but 1.4~5M BW**

Root cause

Bandwidth index is treat Bandindicator index in Code of some sw branch.

If the num of support Lte Band is more than 6[not include], self cal can be obtain correct default value and the result of self cal is no question.

If the num of support Lte Band is less than 6, the result of self calibration for 20M BW is abnormal

when self calibration c

Solution:

Patch**: MOLY00315091; This patch is checked in R2 MP SW Branch**

Note: after the Patch is used , DUT must be calibrated again

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93 Modem typical Case study Case11

Description

Mt6739 project, reused 2G H Band PA for LTE B34/B39;

ACLR is very poor(-34)

output of the Vramp does not exist;

Modem version: MOLY.LP12A.R2.MP.V18

Root cause

The SW Branch does not support the feature of reuse TXM for LTE B34/B39

Solution:

1) Patch: MOLY00285265
2) lte_custom_rf_tpc.h

#define LTE_Band34_VPA_SOURCE_SetDefault **VPA_SOURCE_HW_VAPC**

#define LTE_Band39_VPA_SOURCE_SetDefault **VPA_SOURCE_HW_VAPC**

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93 Modem typical Case study Case12

Description

Mt6739 project, the conduct sensitivity of W B1/B2 RSSI is abnormal between android 7.0 (RSSI -60) and android 8.1(RSSI -72) for same one PCB Board

Root cause

The set of eLNA for W Band is active in Android 8.1 but android 7.0 though design of hw does not support

```
/*****************************************************************/
/*      eLNA IDX setting                                         */
/*****************************************************************/
/* ------------------- RX eLNA Idx setting -------------------- */
#define  UMTSBand1_RX_eLNA_IDX_SetDefault       MML1_FE_ELNA1
#define  UMTSBand2_RX_eLNA_IDX_SetDefault       MML1_FE_ELNA2
#define  UMTSBand3_RX_eLNA_IDX_SetDefault       MML1_FE_ELNA_NONE
#define  UMTSBand4_RX_eLNA_IDX_SetDefault       MML1_FE_ELNA_NONE
#define  UMTSBand5_RX_eLNA_IDX_SetDefault       MML1_FE_ELNA_NONE
#define  UMTSBand6_RX_eLNA_IDX_SetDefault       MML1_FE_ELNA_NONE
#define  UMTSBand7_RX_eLNA_IDX_SetDefault       MML1_FE_ELNA_NONE
#define  UMTSBand8_RX_eLNA_IDX_SetDefault       MML1_FE_ELNA_NONE
#define  UMTSBand9_RX_eLNA_IDX_SetDefault       MML1_FE_ELNA_NONE
#define  UMTSBand10_RX_eLNA_IDX_SetDefault      MML1_FE_ELNA_NONE
#define  UMTSBand11_RX_eLNA_IDX_SetDefault      MML1_FE_ELNA_NONE
#define  UMTSBand19_RX_eLNA_IDX_SetDefault      MML1_FE_ELNA_NONE

/* ------------------- RXD eLNA Idx setting -------------------- */
```

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93 Modem RF Driver reference document list1

MMRF Driver setting

CS0021-GAK1J-AND-V1.0EN_Platform_System_RF_MMRF_RF_Error_Check_Application_Note
CS0021-GAK1K-AND-V1.0EN_Platform_System_RF_MMRF_RF_Custom_Setting_Application_Note

LTE Driver Setting

CS0021-GAK1A-AND-V1.2EN_Platform_System_RF_LTE_RF_Custom_Setting_Application_Note.docx
CS0021-GAK1G-AND-V1.1EN_Platform_System_RF_LTE_RF_Error_Check_Application_Note
CS0021-GAK1F-AND-V1.0EN_Platform_System_RF_LTE_RF_Default_Value_Settings
LTE Custom Excel And File Generation Tool(MT6177)
LTE custom Excel and file generation tool(MT6177m)
MT6177-Update_NVRAM_By_GP_Tool

WCDMA

CS0021-GAK1B-AND-V1.0EN_Platform_System_RF_WCDMA_RF_Custom_Settings_Application_Note
CS0021-GAK1H-AND-V1.0EN_Platform_System_RF_WCDMA_RF_Error_Check_Application_Note
How_to_use_NVRAM_editor_to_modify_3G_FDD_RF_settings

TDSCDMA

[MT6177]3G_TDD_How_to_Configure_RF_Custom_File
[MT6177]3G_TDD_MT6177_ASSERT_Description
TDSCDMA_RF_MT6763_RF_NVRAM_LID_Introduction_Application_Note

C2K

CS0021-GAK1P-AND-V1.4EN_Platform_System_RF_CDMA_RF_Custom_Settings_Application_Note

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93 Modem RF Driver reference document list2

2/3/4G MIPI

CS0021-GAK1D-AND-V1.1EN_Platform_System_RF_MIPI_Customization_Application_Note

DRDI（单软多硬）

CS0021-GAK1O-AND-v1.0EN_Platform_System_RF_DRDI_Customization_Application_Note

ELNA

CS0021-GAK1L-AND-V1.0EN_Platform_System_RF_eLNA_Customization_Application_Note
CS0021-GAK1AB-AND-V1.0EN_Platform_System_RF_ELNA_Module_Design Consideration

TAS

CS0021-GAK1I-AND-V1.0EN_Platform_System_RF_TAS_ Customization_Setting_Application_Note

RF

Platform_System_RF_Calibration_and_Test_Flow_Application_Note

Nvram LID edit

CS0021-GAK1C-AND-v1.3EN_Platform_System_RF_RF_NVRAM_LID_Introduction_Application_Note

GP tool sop

CS0021-GAK1N-AND-V1.0EN_Platform_System_RF_MMRF_GP_Tool_SOP_Application_Note

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Q &A

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