CONFIDENTIAL B MEDIATEK MIPI General Introduction ACS1/RF 20180521

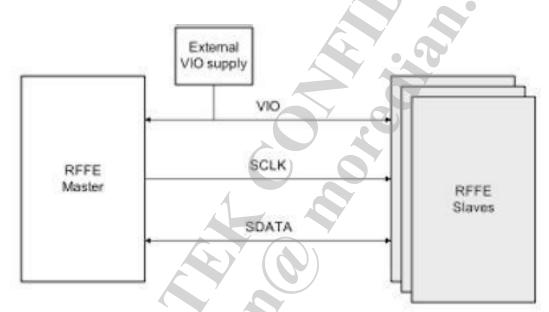
Overview

- > RF FE MIPI Basic conception
 - ❖ MIPI的物理连接
 - ❖ 软件中MIPI控制行为要素
 - MIPI HW PORT BUS
 - MIPI USID
 - MIPI Event/Data
 - ❖ MIPI data的波形解析
 - MIPI timing——Unit
 - MIPI timing—One MIPI Data time
 - MIPI timing——RX WIN
 - MIPI timing——TX
 - 93 modem PA on event timing
 - 93 modem ASM/PA on event timing
 - 93 modem TPC event timing check
- MIPI Configuration Guide
 - 2G Part
 - TDSCDMA Part
 - WCDMA Part
 - LTE Part
 - C2K Part
- > Reference document



MIPI的物理连接

▶ 从物理连接上看,MIPI interface只有VIO, SCLK, SDATA三个网络。



▶ 同一个MIPI port理论上可以最多挂载15个不同USID的器件。

Note: MIPI的data/clock线上挂载的到地电容不要超过20pF!



软件中MIPI控制行为要素

> MIPI port

定义和BB接口的物理连接。

> USID

器件的固有标识,用于识别当前被操控器件。

> Event

定义TRX ON/OFF的时候,需要执行的步骤。

> Data

完成Event定义,所需要执行的MIPI data。一连串的MIPI data组成一个MIPI Event

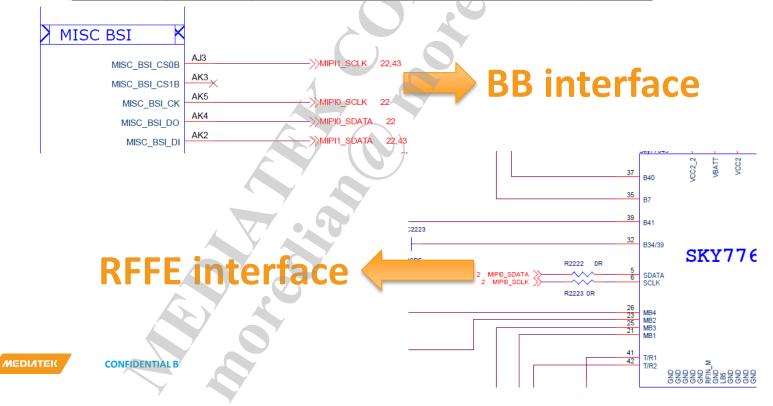
> Timing

定义每一个Event执行的时间点。

MIPI HW PORT BUS

▶ 93 Modem提供4个MIPI port,供给外部MIPI器件使用。 建议Follow reference design MIPI 分配,Default Code 修改比较小

CHINA+EU							
port	device	2G	3G	TDS	C2K	LTE	Other
MIPI-0	TXM / eLNA	ASM / PA	ASM	ASM / PA	ASM	ASM	B38/B41 PRx eLNA
MIPI-1	PA1(Sky77651) / PA2(Sky77652) /PA3(QM52042) / PMIC(RF7061)		PA1 / PA2	PA2	PÁ1/PA2	PA1/PA2	PMIC(HPUE)
MIPI-2	DRX ASM / eLNA		ASM	ASM	ASM	ASM	B38/B41 DRx eLNA
MIPI-3	ANT tuner	OLAT (TAS)					



MIPI USID

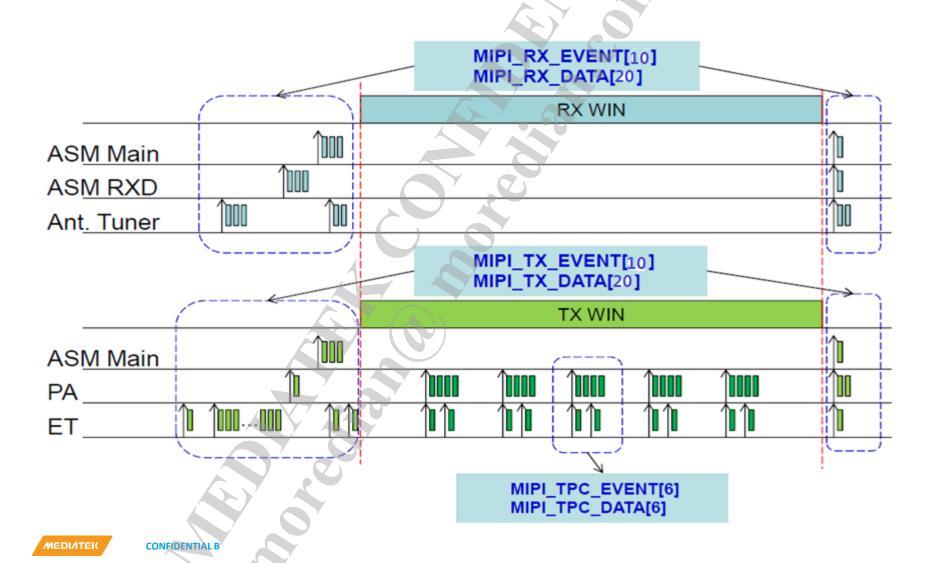
> 通常在器件的datasheet中,即可找到其USID:

	Register 30, Address 0x1E (MAN_ID)								
Register 30	Description	Trigger Support	R/W	Default					
[7:0]	MANUFACTURER_ID[7:0]	No	R	10100101	Manufacturer ID = 0x1A5				
	Register 31, Address 0x1F (USID)								
Register 31	Description	Trigger Support	R/W	Default	į				
[7:6]	Reserved	No	R	00					
[5:4]	MANUFACTURER_ID[9:8]		R	01	Manufacturer ID = 0x1A5				
[3:0]	USID		R/W	1111	USID = 0xF				
	Register 32, Address 0x20 (EXT_PRODUCT_ID)								
Register 32	Description	Trigger Support	R/W	Default					
[7:0]	EXT_PRODUCT_ID	No	R	00000100	EXT_PRODUCT_ID = 0x04				

Note: 当同一个MIPI Port上的器件出现USID冲突时,需要在mml1_custom_mipi.c里修改USID定义。

MIPI Event /Data

上在RF链路上有很多器件,要完成TRX ON/OFF的动作,需要将这些器件一一设置。每个Event由一连串的data组合而成



MIPI Event/Data

- lte_custom_mipi.c Limited number of items in LTE RF MIPI data &event tables
- 93 modem LTE Rx Off event (data num <=8 笔)

	_			
		Case	Max Num.	L
		RX Event	10	
TTE_MIPI_EVENT_TABLE_T LTE_Bandi_MIPI_RX_EVENT_SetDefault[] -	\rightarrow	RX Data	20	
/* No. elm type , data idx , evt_type , evt_offset		TX Event	10	l I
/* { start, stop }, (us) {	_	TX Data	20	
/* 1 */ LTE_MIPI_ASM , { 2	ASM_F	ANT Event	5	
};		ANT Data	10	
LTE_MIPI_DATA_SUBBAND_TABLE_T LTE_Band1_MIPI_RX_DATA_SetDefault[] =		Sub-band Num	10	
<pre>//No. elm type , port_sel , data_seq , USID { /* 0 */ LTE_MIPI_ASM , LTE_MIPI_PORTO , LTE_REG_W , MIPI_USID_ASMO_SetDefault</pre>	Sub-band Num per data	5		
/* 2 */ LTE_MIPI_ASM , LTE_MIPI_PORTO , LTE_REG_W , MIPI_USID_ASMO_SetDefault { /* 3 */ LTE_MIPI_ASM , LTE_MIPI_PORT2 , LTE_REG_W , MIPI_USID_ASM1_SetDefault	<pre></pre>	TPC Event	6	
{	,{ {	TPC Data	6	
NOTE: Data number cannot exceed 12 in each event		TPC section	9	
e.g. start: 2, stop: 15 , 15-2=13 >12 (X)		TPC Section Data	5	
e.g. Start: 2, Stop. 15, 15-2-15 >12 (A)		TAS Event	10	
		TAS Data	10	
9250 /*100 kHz*/ ,0x02 ,0x00 }, (9337 /*100 kHz*/ ,0x02 ,0x00 }, { 9425 /*100 kHz*/ ,0x02 ,0x00 }, { 9512 /*	*100 kH *100 kH *100 kH *100 kH	3 freq ,addr ,data z*/ ,0x02 ,0x03 }, { z*/ ,0x01 ,0x03 }, { z*/ ,0x02 ,0x00 }, { z*/ ,0x01 ,0x00 }, { z*/ ,0x01 ,0x00 }, { 100 kHz*/ ,0 ,0	}, { subband-4 9600 /*100 kHz* 9600 /*100 kHz* 9600 /*100 kHz* 9600 /*100 kHz* }, { 0 /*10	·/

MIPI Event / Data

▶ 所需要的MIPI Data从datasheet中可以获得。要仔细辨清该往哪个寄存器里写什么样的data。

Register 0	Description	Trigger Support	R/W	Default	Notes
[7]	Trigger Select	Trigger0	R/W	0	0 = Trigger 0,1,2 or'd together
					1 = Trigger 0,1,2 fire independently
[6:3]	PA Band Select Control Mode		R/W	0000	Control Mode
					0000 = PA's Disabled
		/		, 6	0001 = MB1_TX
					0010 = MB2_TX
					0011 = MB3_TX
	Sky	77652-11 HM MMN	B∕PA		0100 = MB4_TX
			ľ	, 0	0101 = MB5_TX
		7			0110 = HB2_TX
					0111 = HB3_TX
					1000 = HB1_TX
		11			1001 = HB4_TX
					1010 = Don't Care
					1011 = Don't Care
		F) (W)			1100 = Don't Care
					1101 = Don't Care
					1110 = Don't Care
	У				1111 = PA's Disabled (High switch isolation)
[2]	PA Enable	.60	R/W	0	PA Enable
	A Y A				0 = PA Off
					1 = PA 0n
[1]	PA Mode		R/W	0	PA Mode
		Y			0 = HPM
					1 = LPM
[0]	Reserved		R/W	0	Zero required

MIPI Event / Data

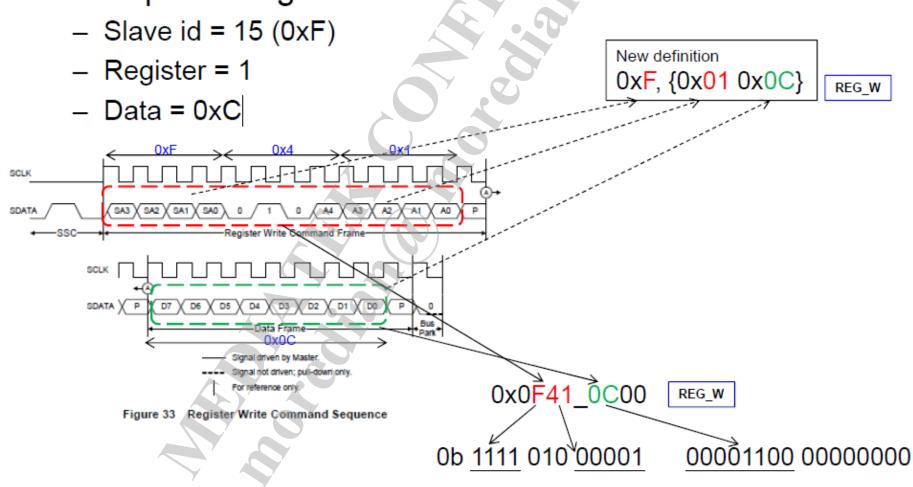
▶ 所需要的MIPI Data从datasheet中可以获得。要仔细辨清该往哪个寄存器里写什么样的data。

D.V		T	(i				
Bit osition	Description	Trigger Support	R/W	Default	Sky779	28-11 Notes	
				Register	0, Address 0x00 (PA Control)		
7]	Reserved	Trigger0	R/W	0	Reserved; (set to 1)		
[6]	Reserved			0	Reserved; (set to zero)		
[5]	Gain Control (linear)			0	-	= reduced gain	
[4:0]	TxFEM Mode Control			00000	0x00 = PA off 0x	OB = LB EDGE/Linear Tx	0x0F = HB EDGE/Linear Tx
					0x0A = LB GMSK/Vramp Tx 0x	OE = HB GMSK/Vramp Tx	Other = Reserved (Do Not Use)
				Register	1, Address 0x01 (BIAS_CTRL)		•
[7:4]	PA Stage 3 Bias	Trigger0	R/W	0000	0000 = 250 μA 01	110 = 1750 µA	1100 = 3250 μA
	(DAC3)				0001 = 500 μA 01	111 = 2000 μA	1101 = 3500 μA
					$0010 = 750 \mu\text{A}$	000 = 2250 μA	1110 = 3750 μA
					0011 = 1000 μA 10	001 = 2500 μA	1111 = 4000 μA
					0100 = 1250 μA	010 = 2750 μA	
					0101 = 1500 μA 10	011 = 3000 μA	
[3:0]	PA Stage 1-2 Bias			0000	0000 = 250 μA 01	110 = 1750 μA	1100 = 3250 μA
	(DAC12)				0001 = 500 μA 01	111 = 2000 μA	1101 = 3500 μA
					0010 = 750 μA 10	000 = 2250 μA	1110 = 3750 μA
					0011 = 1000 μA 10	001 = 2500 μA	1111 = 4000 μA
				1	0100 = 1250 μA 10	010 = 2750 μA	-
				14	0101 = 1500 μA 10	011 = 3000 μA	
	'			Register	2, Address 0x02 (ASM_CTRL)		•
[7:4]	(RESERVED)	Trigger0	R/W	0000	Reserved (set to all zeroes)		
[3:0]	LB Switch Control		R/W	0000	0000 = Standby	0011 = L_TRx3	0110 = L_TRx6
				- / ($0001 = L_TRx1$	0100 = L_TRx4	0111 = L_TRx7
					0010 = L_TRx2	0101 = L_TRx5	1111 = LB PA Out
							Other = isolation
			7	Register :	3, Address 0x03 (ASM_CTRL2)		
[7:5]	HB Switch Control	Trigger0	Ŕ/W	000	000 = Standby	010 = H_TRx2	100 = H_TRx4
					001 = H_TRx1	011 = H_TRx3	Other = isolation
[4:0]	(RESERVED)	V.		00000	(Reserved; set to zero)		
		Y		Register	4, Address 0x04 (CPL_CTRL)		
[7:5]	(RESERVED)	Trigger0		000	(Reserved; set to zero)		•
[4:3]	Coupler Mode		R/W	00	00 = Standby	10 = MB Coupler ON	
					01 = LB Coupler ON	11 = HB Coupler ON	
[2]	Coupler Directionality		R/W	0	0 = Forward	1 = Reverse	
[1:0]	(RESERVED)		R/W	00	Reserved; set to 00		
				Register (5, Address 0x05 (ASM_CTRL3)		
[7:4]	(RESERVED)		R/W	0x00	Reserved (set to zero)		
[3:0]	MB Switch Control			0000	0000 = Standby	0011 = M_TRx3	1111 = MB PA Out
4		7			$0001 = M_TRx1$	$0100 = M_TRx4$	
			1	I	0010 = M_TRx2	$0101 = M_TRx5$	Other = isolation

MIPI data的波形解析

→ 当问题难以厘清时,往往需要手动量取MIPI信号波形做确认。 如下所示为MIPI data的物理形状解析和表达格式:

Example of Register write command



MIPI timing—Unit

- MTK platform RAT timing unit
 - ❖ 2G timing Unit QB , 1QB=0.923uS
 - ❖ 3G WCDMA uS
 - ❖ 3G TDSCDMA echip, echip=(1/8)chip=0.78125/8=0.09765625uS=0.1us
 - ♦ 4G LTE uS
 - ❖ C2K uS
- > 93 Modem NVRAM Edit Timing Value related to L1 code Timing Value

```
Output
2G timing
Nvram Value= L1 Code value
```

- ♦ 3G WCDMA Nvram Value= [(L1 Code value)*3.84]
 ul1d_mipi_public.h #define US2CHIPCNT(us) ((us)*3.84)
- ❖ 3G TDSCDMA 不建议修改
- * 4G LTE Nvram Value=[(L1 Code value)*61.44]
 mml1_mipi_public.h #define US2OFFCNT(us) ((us)*6144/100);
- C2K Nvram Value=L1 code Value

MIPI timing——One MIPI Data time

- ➤ MTK不同平台RF FE Modem One MIPI data time period[Tcd]
 - ❖ MT6177M/MT6177 Modem MIPI CLK 25M
 One MIPI data time period = 24/25MHz=0.96uS
 - MT6176 Modem MIPI CLK 22.75M
 One MIPI data time period = 24/22.75MHz=1.05uS
 - MT6169 Modem MIPI CLK 20M
 One MIPI data time period = 24/20MHz=1.2uS
- ▶ 目前通常采用的MIPI command sequence, 一笔MIPI data 含有24bits, 具体如下图

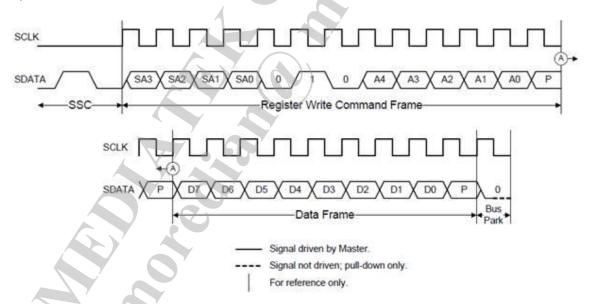




Figure 33 Register Write Command Sequence

MIPI timing——RX WIN

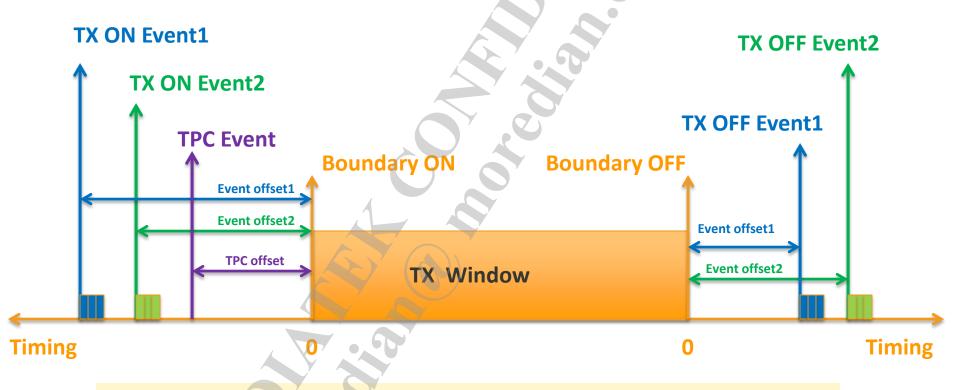
- ▶ 通常以TX/RX Boundary 作为时序的参考基准点,对某一笔MIPI Event定义 其ON或OFF的时间
- LTE Rx Window Timing



Note:请参考默认设定的时序值! 时序改的太过分可能会导致编译错误, 或其他奇怪的问题。

MIPI timing——TX

- ▶ 通常以TX/RX Boundary 作为时序的参考基准点,对某一笔MIPI Event定义 其ON或OFF的时间。
- LTE TX Window timing



Note: 请参考默认设定的时序值!

改的太过分可能会导致编译错误, 或其他奇怪的问题。

尤其注意TPC的timing要放在PA ON的后面!

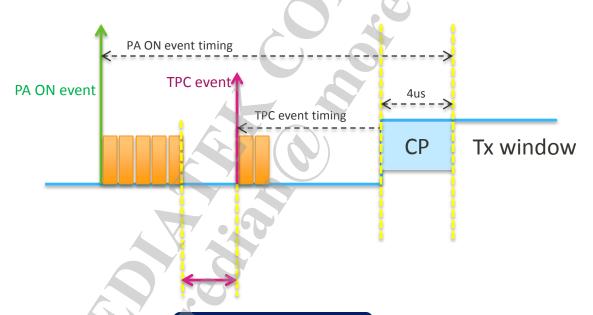
MEDIATEK

93 modem PA on event timing (1/2)

>LTE Timing

Criteria:

The timing difference between PA ON event timing - (PA on data #)*Tcd and TPC event timing should be larger than 5.5us



At least >= 5.5us

PA ON event timing - (PA on data #)*Tcd
- TPC event >= 5.5us



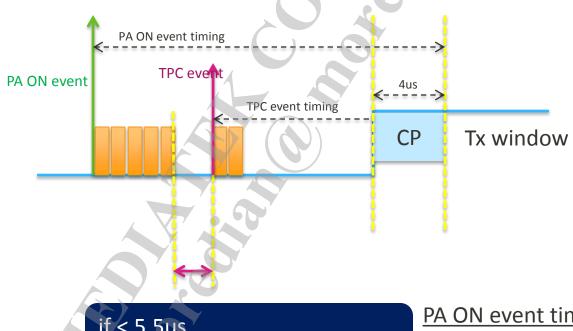


93 modem PA on event timing (2/2)

>LTE Timing

Criteria:

The timing difference between PA ON event timing - (PA on data #)*Tcd and TPC event timing should be larger than 5.5us





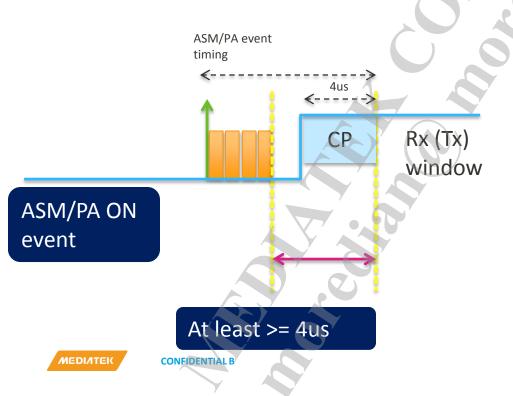
if < 5.5us confidential => Show Warning message!!! PA ON event timing - (PA on data #)*Tcd
- TPC event >= 5.5us

93 modem ASM/PA on event timing (1/2)

>LTE Timing

Criteria:

The timing of ASM/PA ON event timing - (ASM/PA on data #)*Tcd should be larger than 4us (due to CP 4us consideration)



ASM/PA ON event timing - (ASM/PA on data #)*Tcd >= 4us

93 modem ASM/PA on event timing (2

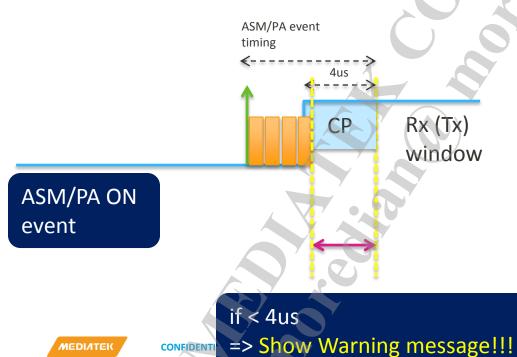
>LTE Timing

Criteria:

MEDIATEK

CONFIDENTI

The timing of ASM/PA ON event timing -(ASM/PA on data #)*Tcd should be larger than 4us (due to CP 4us consideration)



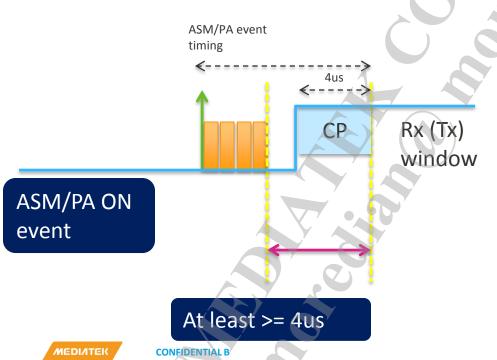
ASM/PA ON event timing - (ASM/PA on data #)*Tcd >= 4us

93 modem TPC event timing check

>LTE Timing

Criteria:

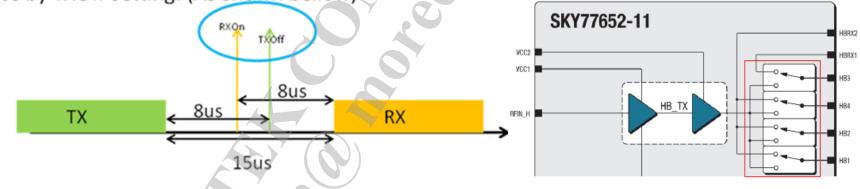
The timing of TPC event timing – (TPC Data #)*Tcd should be larger than 4us (due to CP 4us consideration)



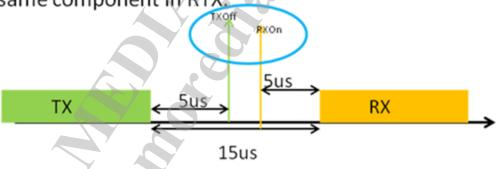
TPC event timing - (TPC on data #)*Tcd >= 4us

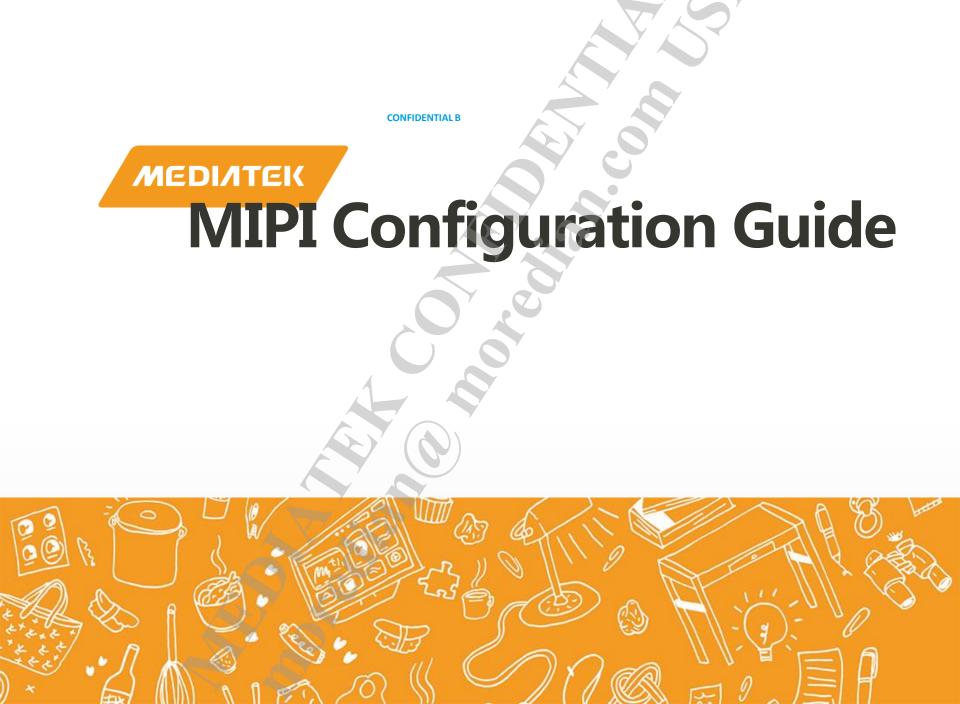
93 modem LTE TDD event timing

- >LTE Timing
 - LTE TDD TX OFF&RX ON timing Limit: Tx_OFF +Rx_ON(Left most Event) <=15us</p>
 - 3P4T Switch are shared to Tx Path and Rx Path for LTE TDD MMMB PA
- In some scenario, Timing difference between TX and RX burst will less than 15us. If you use the same component in RTX, RXOn Setting will be replace by TXOff Setting. (As Shown bellow)

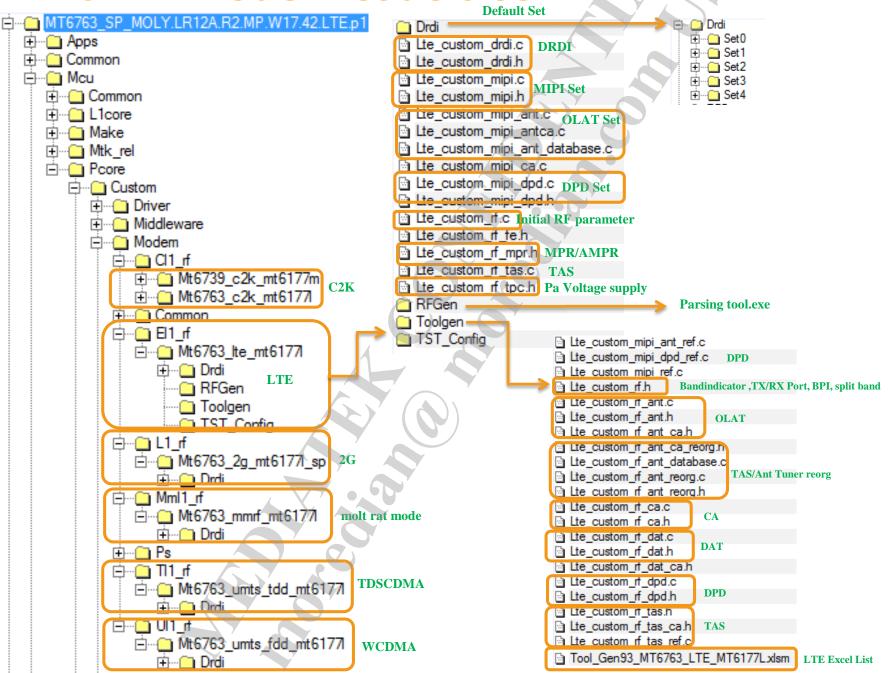


So we suggest that RXOn And TXOff timing should be less than 5us,if you use the same component in RTX.





MT6177 Modem code tree



90/91 MIPI的相关设定文件

********	File Name	Defines
	l1d_custom_mipi.h	2G_MIPI_ENABLE; T/Rx events timing(should not modify)
	l1d_custom_mipi.c	MIPI Register and Data
l1_rf	l1d_custom_rf.h	BPI Timing; BPI configration; T/Rx Ports; power rollback
	m12193.c	ini default value
	tl1d_custom_rf.h	TDS_MIPI_ENABLE; BPI configration; T/Rx Ports
	tl1d_custom_mipi.h	MIPI Register and Data
tl1_rf	t12193.h	BPI & MPI Timing;
	t12193.c	ini default value
	tl1d_custom_drdi.h	Dynamic Radio-setting Dedicated Image(DRDI),单软多硬
	ul1d_custom_mipi.h	3G_MIPI_ENABLE; 定义了在ulld_custom_mipi.e 中每个band的event/data的个数(should not modify)
	ul1d_custom_mipi.c	MIPI Register and Data; TPC
ul1_rf	ul1d_custom_rf.h	BPI configuration; PRx/DRx/Tx ports and Power rollback; Band indicator
	wcustomdata.c wcustomdata.h	Dynamic Radio-setting Dedicated Image(DRDI),单软多硬
	u12193.c	.ini default value
	lte custom drdi.h	
	lte_custom_drdi.c	Dynamic Radio-setting Dedicated Image(DRDI),单软多硬
el1_rf	lte_custom_mipi.h	MIPI_FRONT_END_ENABLE; 定义了在Ite_custom_mipi.c中每个band的event/data的个数(should not modify)
C11_11	lte_custom_mipi.c	MIPI Register and Data; TPC
	lte_custom_rf.h	BPI configration;PRx/DRx/Tx ports and Power rollback; Band indicator
	lte_custom_rf.c	ini default value
	mml1_custom_drdi.h mml1_custom_drdi.c	Dynamic Radio-setting Dedicated Image(DRDI),单软多硬
	mml1_custom_mipi.h	USID
mml1_rf	mml1_custom_mipi.c	在同一MIPI port, 使用不同vender提供的MIPI元件, 但USID一样时, 可在此文件中将某一元件的USID更换为另一unique的USID
	mml1_custom_rf.h	CLK enable

93 MIPI的相关设定文件(1)

	File Name	Defines
	l1d_custom_mipi.h	2G_MIPI_ENABLE; T/Rx events timing(should not modify)
	11d custom mipi.c	MIPI Register and Data
	l1d_custom_rf.h	BPI Timing; BPI configration; T/Rx Ports; power rollback
l1_rf	m12193.c	ini default value
	l1d_custom_rf_dat.h	Dat [Dynamic_Antenna_Tuner] L1D_DAT_ENABLE, Ant tuner state setting
	l1d_custom_rf_dat.c	Dat [Dynamic_Antenna_Tuner] L1D_DAT_CAT_A/B_DATABASE_Set
	l1d_custom_rf_tas.h	TAS [Transmit Antenna Switch];TAS Enable,Ant State Setting
	l1d_custom_rf_tas.c	L1D_TAS_CAT_A/B_DATABASE_Set
	tl1d_custom_rf.h	TDS_MIPI_ENABLE; BPI configration; T/Rx Ports
	tl1d_custom_mipi.h	MIPI Register and Data ;TAS Enable,
	t12193.h	BPI & MPI Timing;
	t12193.c	ini default value.
tl1_rf	tl1d_custom_drdi.h	Dynamic Radio-setting Dedicated Image(DRDI),单软多硬
	tl1d_custom_rf_dat.h	Dat [Dynamic_Antenna_Tuner] TL1D_DAT_ENABLE, Ant tuner state setting
	tl1d_custom_rf_dat.c	Dat [Dynamic_Antenna_Tuner] TL1D_DAT_CAT_A/B_DATABASE_Set
	tl1d_custom_rf_tas.h	TAS [Transmit Antenna Switch];TAS Enable,Ant State Setting
	tl1d_custom_rf_tas.c	TL1D_TAS_CAT_A/B_DATABASE_Set
	ul1d_custom_mipi.h	3G_MIPI_ENABLE;定义了在如11d_custom_mipi.c中每个band的event/data的个数(should not modify)
	ul1d_custom_mipi.c	MIPI Register and Data; TPC
	ul1d_custom_rf.h	BPI configration;PRx/DRx/Tx ports and Power rollback; Band indicator
	wcustomdata.c	Dynamic Radio-setting Dedicated Image(DRDI),单软多硬
	wcustomdata.h	Dynamic Radio-setting Dedicated image(DRD1), 中秋夕坡
	u12193.c	ini default value.
ul1_rf	ul1d_custom_rf_ca.h	CA CC0&CC1, TRX Port/TRX BPI/MIPI Route Setting; No Care
	ul1d_custom_mipi_ca.c	CA MIPI Rx Route Setting; No Care
	ul1d_custom_rf.c	NCCA Setting/ PA PMIC supply Setting; No Care
	ul1d_custom_rf_dat.h	Dat [Dynamic_Antenna_Tuner] UL1D_DAT_ENABLE, Ant tuner state setting
	ul1d_custom_rf_dat.c	Dat [Dynamic_Antenna_Tuner] UL1D_DAT_CAT_A/B_DATABASE_Set
	ul1d_custom_rf_tas.h	TAS [Transmit Antenna Switch];TAS Enable,Ant State Setting
	ul1d_custom_rf_tas.c	UL1D_TAS_CAT_A/B_DATABASE_Set
	ul1d_custom_rf_dpd.h	Digital Pre-Distortion(DPD)/
	ul1d_custom_rf_dpd.c	DPD Enable, dpd_apt_temperature_th_by_rfic/PCFE power threshold setting

93 MIPI的相关设定文件(2)

717.	File Name	Defines	
	lte_custom_drdi.h	D ' D !' " D !' ' II (DDD) # 4/2 #	
	lte_custom_drdi.c	Dynamic Radio-setting Dedicated Image(DRDI),单软多硬	
	lte_custom_mipi.h	MIPI_FRONT_END_ENABLE; 定义了在Ite_custom_mipi.c中每个band的event/data的个数 (should not modify)	
	lte_custom_mipi.c	MIPI Register and Data; TPC	
	lte_custom_mipi_ca.c	CA new route MIPI Route Setting	
	lte_custom_rf.c	ini default value	
	lte_custom_mipi_ant.c	OLAT[open loop ant tuner] NCA,ant tuner MIPI setting	Manual setting
	lte_custom_mipi_antca.c	OLAT[open loop ant tuner] CA ant tuner MIPI setting	
	lte_custom_mipi_ant_database.c	TAS DPDT BPI setting, TAS Ant tuner MIPI Seting	
	lte_custom_rf_mpr.h	LTE MPR/AMPR Setting	
	lte_custom_rf_tpc.h	PA PMIC supply setting/sptial RB Tx Power Backoff/temp THRES setting	
	lte_custom_rf_tas.c	EL1D_TAS_CAT_A/B_DATABASE_Set	
	lte_custom_rf_fe.h	BPI Timing setting	
	lte_custom_mipi_dpd.h	Dat [Dynamic_Antenna_Tuner] UL1D_DAT_ENABLE, Ant tuner state setting	
	lte_custom_mipi_dpd.c	DPD Enable, dpd_apt_temperature_th_by_rfic/PCFE power threshold setting	
el1_rf	lte_custom_rf.h	Bandindicator,BPI configuration,PRx/DRx/Tx ports ;ELNA HPUE;Split&Filter Band	
	lte_custom_rf_ca.h	Rx Alternate FE route/Tx Alternate FE route define	
	lte_custom_rf_ca.c	CA capability setting	
	lte_custom_rf_ant.h	OLAT Tuner Setting	
	lte_custom_rf_ant.c	CA OLAT Tuner Setting	
	lte_custom_rf_ant_ca.h	OLAT ANT_Tuner, ANT_ALTERNATE_CONFIGURE Setting[CA No single Band route]	
	lte_custom_mipi_ant_ref.c	OLAT MIPI TX&RX Setting	
	lte_custom_rf_ant_database.c	Reorge Ant Tuner Database Setting, LTE_ANT_CAT_A/B_DATABASE_Set[DAT/TAS]	
	lte_custom_rf_ant_reorg.h	Reorge By band Ant tuner setting	Toolgen /Parsing Tool. Gen
	lte_custom_rf_ant_ca_reorg.h	Reorge CA Ant tuner state setting	file from
	lte_custom_rf_ant_reorg.c	Reorge ant tuner mapping	Tool_Gen93_MT67**_LT
	lte_custom_rf_dat.h	Dat [Dynamic_Antenna_Tuner] EL1D_DAT_ENABLE, Ant tuner state setting	E_MT6177*.xlsm
	lte_custom_rf_dat.c	Dat EL1D_DAT_CAT_A/B_DATABASE_Seting	
	lte_custom_rf_dat_ca.h	Dat CA EL1D_DAT_ENABLE, Ant tuner state setting	
	lte_custom_rf_dpd.c	DPD Enable, dpd_apt_temperature_th_by_rfic/PCFE power threshold setting	
	lte_custom_rf_dpd.h	Digital Pre-Distortion(DPD)/	
	lte_custom_mipi_dpd_ref.c	Digital Pre-Distortion(DPD)/	
	lte_custom_rf_tas.h	TAS [Transmit Antenna Switch];TAS Band Enable,Ant State Setting	
	lte_custom_rf_tas_ca.h	TAS CA(PCC/SCC_ TAS Enable,Ant State Setting	
	lte_custom_rf_tas_ref.c	TAS database table setting, LTE_TAS_CAT_A&B_DATABASE_Set Setting	

93 MIPI的相关设定文件(3)

	File Name	Defines	Note
	c2k_custom_drdi.c	Dynamic Radio-setting Dedicated Image(DRDI),单软多硬	
	c2k_custom_drdi.h		
	c2k_custom_elna.c	C2K eLAN Set	
	c2k_custom_elna.h		
	c2k_custom_mipi.c	MIPI Set	
	c2k_custom_mipi.h	MIPI timng	
	c2k_custom_rf.c	Initial rf parameter	
	c2k_custom_rf.h	Bandindicator/TRX Port/BPI	
Cl1_rf	c2k_custom_rf_dat.c	Dat CL1D_DAT_CAT_A/B_DATABASE_Seting	
	c2k_custom_rf_dat.h	Dat [Dynamic_Antenna_Tuner] CL1D_DAT_ENABLE, Ant tuner state setting	
	c2k_custom_rf_dpd.c	DPD Enable	
	c2k_custom_rf_dpd.h	DPD	
	c2k_custom_rf_tas.c	CL1D_TAS_CAT_A/B_DATABASE_Set	
	c2k_custom_rf_tas.h	TAS [Transmit Antenna Switch];TAS Band Enable,Ant State Setting	
	c2k_custom_rf_tuner.c	OLAT[open loop ant tuner] ant tuner MIPI setting	
	c2k_custom_rf_tuner.h	Ant state set	
	c2k_custom_rf_tas_tst.h	TST bandindicator enable/TST Ant state by band	
	mml1_custom_drdi.h	- Dynamic Radio-setting Dedicated Image(DRDI),单软多硬	
	mml1_custom_drdi.c		
	mml1_custom_mipi.h	USID define	
		Initial CW Table Setting; LPM(sleep mode) CW Setting;同一MIPI port, 使用不同vender提供的	
	mml1_custom_mipi.c	MIPI元件, 但USID一样时, 可在此文件中将某一元件的USID更换为另一unique的USID;	
mml1_rf		will fort, Posid 行动, 小在此文件车前来 为时间105id 文获为为 unique 105id,	
111111111_11	mml1_custom_rf.h	CLK enable is invalid(*.DWS Setting by DCT Tool)	
	mml1_custom_elna.h	ELNA Enable/ Control Type/timing/BPI Control Logical setting	
	mml1_custom_elna.c	ELNA MIPI setting	
	mml1_custom_ext_buck_ldo.c	HPUE External DC-DC Setting	
	mml1_custom_rf.c	TADC for 8 temperature mapping	
	mml1_custom_rf.h	CLK enable and CLK buffer Drivering are invalid(*.DWS Setting by DCT Tool); IQ SWAP;	



MML1--USID

▶ 在mml1_custom_mipi.h中定义使用到器件的USID

```
#define MIPI USID INITO SetDefault
                                          0x0000
#define MIPI USID ASM0 SetDefault
                                           0x000C // Main 3P18T(TXM)
#define MIPI USID ASM1 SetDefault
                                           0x000A // DRX ASM DP12T(LMB)
#define MIPI_USID_ASM2_SetDefault
                                           0x000B // DRX ASM SP6T(HB)
#define MIPI USID ASM3 SetDefault
                                           0x0009
#define MIPI USID PA0 SetDefault
                                          0x000F // HMB PA
#define MIPI USID PA1 SetDefault
                                          0x000D //LB PA
#define MIPI_USID_PA2_SetDefault
                                          0x000E //B42 PA
#define MIPI USID ANTO SetDefault
                                          0x0006
#define MIPI USID TAS SetDefault
                                          0x0007
#define MIPI USID EXT VPA SetDefault
                                          0x0005
```

➤ 在mml1_custom_mipi.c,修改USID,同一个MIPI port上挂载的器件有USID 冲突时,在mml1_custom_mipi.c中修改掉其中一个器件的USID。按照如下示意:90 modem即使不同组MIPI BUS,也不允许相同的USID设置

```
* MML1 MIPI Change USDI Table Data
const MML1_MIPI_USID_CHANGE_T MML1_MIPI_USID_CHANGE_TABLE_SetDefault[MML1_MIPI_MAX_USID_CHANGE_NUM] =
                                  , current USID PRODUCT_ID , MANUFACTORY ID new USID
 // USID change type , port_sel_
 {USID_REG_W
                     , MML1_MIRI_PORTO , 0xE
                                                 , 0x9B
                                                            , 0x1A5
                                                                                }, // Main 3P18T
                     , MML1_MIPI_PORT1 , 0xF
 {USID_REG_W
                                                 , 0x00
                                                           , 0x1A5
                                                                              }, // LB PA
                                                                        , 0xD
                     , MML1 MIPI PORT1 , 0xF
 {USID_REG_W
                                                 , 0x10
                                                            , 0x286
                                                                        , 0xE
                                                                              }, // B42 PA
 {USID_REG_W
                     , MML1 MIPI PORT2 , 0x9
                                                                                }, // DRX ASM SP6T(HB)
                                                 , 0x18
                                                            , 0x134
                                                                        , 0xB
 {USID_NULL,0,0,0,0,0,0}
```

Note:如果是完全相同的两个器件,则无法区分修改!



MML1--Initial&LPM CW Table

▶ 在mml1_custom_mipi.c, 做RF FE HW Part的初始化

Note: Initial Table 初始化的MIPI Port及USID 必须与HW 设计一致,且各个RAT MIPI.c, CW 中MIPI 及USID也必须与一致,否则会出现Modem Assert

► 在mml1_custom_mipi.c,LPM(Sleep mode) CW Table 设置

```
const MML1_MIPI_LPM_CW_T MML1_MIPI_LPM_CW_SetDefault[MML1_MIPI_MAX_LPM_CW_NUM] =
                                                     , addr , data , wait_time(us)
  // elm type , port_sel
                            , data_seq , USID
  {MML1 MIPI ASM , MML1 MIPI PORTO, MML1 REG W, MIPI USID ASMO SetDefault
                                                                                , {0x1C, 0xB8} , 0 }, // Specific ID, Standard MIPI, PM_TRIG = normal mode
  {MML1_MIPI_ASM , MML1_MIPI_PORT1, MML1_REG_W, MIPI_USID_PA0_SetDefault
                                                                                , {0x1C, 0xB8} , 0 }, // Specific ID, Standard MIPI, PM_TRIG = normal mode
  {MML1_MIPI_ASM, MML1_MIPI_PORT1, MML1_REG_W, MIPI_USID_PA1_SetDefault
                                                                                , {0x1C, 0xB8} , 0 }, // Specific ID, Standard MIPI, PM_TRIG = normal mode
  {MML1_MIPI_ASM, MML1_MIPI_PORT1, MML1_REG_W, MIPI_USID_PA2_SetDefault
                                                                                , {0x1C, 0xB8} , 0 }, // Specific ID, Standard MIPI, PM_TRIG = normal mode
  {MML1 MIPI ASM, MML1 MIPI PORT2, MML1 REG'W, MIPI USID ASM1 SetDefault , {0x1C, 0x88}, 0 }, // Specific ID. Standard MIPI, PM TRIG = normal mode
  {MML1_MIPI_ASM , MML1_MIPI_PORT2, MML1_REG_W, MIPI_USID_ASM2_SetDefault , {0x1C, 0x88} , 0 }, // Specific ID, Standard MIPI, PM_TRIG = normal mode
  {MML1_MIPI_END_PATTERN,0,0,0,{0,0},0},
  {MML1_MIPI_END_PATTERN,0,0,0,{0,0},0},
  {MML1_MIPI_END_PATTERN,0,0,0,{0,0},0},
  {MML1_MIPI_END_PATTERN,0,0,0,{0,0},0},
  {MML1_MIPI_END_PATTERN,0,0,0,{0,0},0,0},
  {MML1_MIPI_END_PATTERN,0,0,0,(0,0},0},
  {MML1_MIPI_END_PATTERN,0,0,0,{0,0},0,0},0},
  {MML1_MIPI_END_PATTERN,0,0,0,{0,0},0},
  {MML1_MIPI_END_PATTERN,0,0,0,(0,0},0},
  {MML1_MIPI_END_PATTERN,0,0,0,{0,0},0},
```

MML1--ELNA CW

mml1_custom_elna.h, ELNA category setting/control interface/Settling time/PIN selected

```
//ELNA Catgory Setting:
 #define MML1_FE_ELNA_NONE_CATEGORY_SetDefault
                                                    MML1_ELNA_OFF
 #define MML1 FE ELNA1 CATEGORY SetDefault
                                                    MML1 ELNA OFF
                                                    MML1 ELNA OFF
 #define MML1 FE ELNA2 CATEGORY SetDefault
 #define MML1_FE_ELNA3_CATEGORY_SetDefault
                                                    MML1_ELNA_OFF
                                                    MML1 ELNA OFF
 #define MML1_FE_ELNA4_CATEGORY_SetDefault
 #define MML1 FE ELNA5 CATEGORY SetDefault
                                                    MML1 ELNA OFF
 #define MML1 FE ELNA6 CATEGORY SetDefault
                                                    MML1_ELNA_OFF
 #define MML1_FE_ELNA7_CATEGORY_SetDefault
                                                    MML1_ELNA_OFF
 #define MML1_FE_ELNA8_CATEGORY_SetDefault
                                                    MML1_ELNA_OFF
 #define MML1 FE ELNA9 CATEGORY SetDefault
                                                    MML1 ELNA OFF
 #define MML1_FE_ELNA10_CATEGORY_SetDefault
                                                    MML1_ELNA_OFF
 #define MML1 FE ELNA11 CATEGORY SetDefault
                                                    MML1 ELNA OFF
 #define MML1_FE_ELNA12_CATEGORY_SetDefault
                                                    MML1_ELNA_OFF
//Select eLNA control interface
 #define MML1 FE ELNA NONE CONTROL INTERFACE SetDefault MML1 CONTROL NONE
 #define MML1 FE ELNA1 CONTROL INTERFACE SetDefault
                                                             MML1 CONTROL NONE
 #define MML1 FE ELNA2 CONTROL INTERFACE SetDefault
                                                             MML1 CONTROL NONE
 #define MML1 FE ELNA3 CONTROL INTERFACE SetDefault
                                                              MML1 CONTROL NONE
 #define MML1 FE ELNA4 CONTROL INTERFACE SetDefault
                                                              MML1 CONTROL NONE
 #define MML1 FE ELNA5 CONTROL INTERFACE SetDefault
                                                              MML1 CONTROL NONE
 #define MML1 FE ELNA6 CONTROL INTERFACE SetDefault
                                                             MML1 CONTROL NONE
 #define MML1_FE_ELNA7_CONTROL_INTERFACE_SetDefault
                                                             MML1 CONTROL NONE
 #define MML1 FE ELNA8 CONTROL INTERFACE SetDefault
                                                             MML1 CONTROL NONE
 #define MML1 FE ELNA9 CONTROL INTERFACE SetDefault
                                                             MML1 CONTROL NONE
 #define MML1 FE ELNA10 CONTROL INTERFACE SetDefault
                                                              MML1 CONTROL NONE
 #define MML1_FE_ELNA11_CONTROL_INTERFACE_SetDefault
                                                              MML1_CONTROL_NONE
 #define MML1 FE ELNA12 CONTROL INTERFACE SetDefault
                                                              MML1 CONTROL NONE
//PIN selected
// The settings for ELNA1
#define PDATA MML1 FE ELNAX PINO SetDefault
                                                    MML1 ELNA PIN NONE
                                                                       // the 1st BPI pin number for the ELNA control, set MML1_ELNA_PIN_NONE if the BPI control is not used.
#define PDATA_MML1_FE_ELNAX PIN1 SetDefault
                                                    MML1 ÉLNA PIN NONE // the 2nd BPI pin number for the ELNA control, set MML1 ELNA PIN NONE if the BPI contorl is not used.
                                                                       // the ON mode BPI setting (1 or 0) for the 1st BPI pin
#define PDATA_MML1_FE_ELNAX_PIN0_ON_DATA_SetDefault
#define PDATA_MML1_FE_ELNAX_PIN1_ON_DATA_SetDefault
                                                                      // the ON mode BPI setting (1 or 0) for the 2nd BPI pin
#define PDATA MML1 FE ELNAX PINO BYPASS DATA SetDefault 0
                                                                      // the BYPASS mode BPI setting (1 or 0) for the 1st BPI pin
#define PDATA_MML1_FE_ELNAX_PIN1_BYPASS_DATA_SetDefault 0
                                                                      // the BYPASS mode BPI setting (1 or 0) for the 1st BPI pin
```

Note: X=0,1.....12,详细参照ELNA 配置相关文档,如果没有做ELNA,请将Pin Control 设置成MML1_ELNA_PIN_NONE,否则会造成该BPI不受控



MML1--clock buffer

▶ 在mml1_custom_rf.h文件中的clock enable已经无效,都放在*.DWS中处理 (DCT Tool Setting)

```
/* Enable or disable the clock1, 2, 3, and 4 output */
  / * 1 : Enable
     0 : Disable
                                                       * CLK1 is enabled for BB */
  #define MML1_CLK1_EN_SetDefault
  #define MML1_CLK2_EN_SetDefault
  #define MML1_CLK3_EN_SetDefault
  #define MML1 CLK4 EN SetDefault
            CONFIDENTIAL B
MEDIATEK
```



CONFIDENTIAL B

GSM Part

GSM Part --RX

> 列出RX通路ON/OFF时所需的操作步骤:

Event No.	Event Type	Action	Data	Data No.
1	DV ON		将ASM M Port 设置成Idle	0
1	RX ON	设置到Idle状态	将ASM H Port 设置成Idle	1
2	RX ON	设置L TRX Port Active状态	打开ASM L Port对应的RX Path	2
3	RX OFF	关闭RX 通路	将ASM 设置成idle状态	3

Note: Ex:Sky77928-11,

Off Event Sky77928-11,2G/TD/LTE TD 需要SW Reset 0x23,0x80;



GSM Part --RX

RX部分的格式设置介绍:

element

{ /* 0 */ GGE_MIPL_ASM

{ /* 1 */ GGE MIPI ASM

{ /* 2 */ GGE_MIPI_ASM

data idx

type , { start, stop }

```
Fiming在11d custom mipi.h中定义
```

```
Event RX Timing Define
                                                               *MT6177L*/ #define QB_MIPI_RX_ON0_Set0
                                                              /*MT6177L*/ #define QB_MIPI_RX_ON1_Set0
                                                                                                       65
                                                               173
                                                              173
                                                              /*MT6177L*/ //#define OB MIPI RX ON4
                                                                                                173
                                                              /*MT6177L*/ //#define OB MIPI RX ON5
                                                                                                173
                                                              /*MT6177L*/ //#define QB_MIPI RX ON6
                                                                                                173
                                                              /*MT6177L*/ //#define QB_MIPI_RX_ON7
                                                                                                173
                                                               *MT6177L*/ #define QB_MIPI_RX_OFF0_Set0
                                                               *MT6177L*/ //#define QB_MIPI_RX_OFF1
                                                                                                173
                                                              \sqrt{*MT6177L*} / / \# define QB_MIPI_RX_OFF2
                                                                                                173
                                                              /*MT6177L*/ //#define QB_MIPI_RX_OFF3
                                                                                                173
                                                              /*MT6177L*/ //#define QB MIPI RX OFF4
                                                                                                173
                                                                                            Timing
const sGGE_MIPI_CTRL_TABLE_BAND GGE_MIPI_CTRL_TABLE_GSM900_Set0=
    /* GGE_MIPI_CTRL_TABLE_GSM900.mipi_rx_ctrl_table.mipi_rxctrl_event[] */
                                                          , event timing */
                                                           ( OB )
                                                                              QB MIPI RX ONO Set0
                                                   GGE MIPI TRX ON
                                                                              QB_MIPI_RX_ON1_Set0
                                                   GGE MIPI TRX ON
                                                                              OB MIPI RX OFF0 Set0
                                                   GGE MIPI TRX OFF
                                                          Event
                                                           Data
                                                            ,{ { subband arfcn, addr, data }, { subband arfcn, ad
                                                                                       , 0x05, 0x00 }, {
                                                                              124
                                                                                       , 0x03, 0x00 }, {
```

```
/* GGE_MIPI_CTRL_TABLE_GSM900.mipi_rx_ctrl_table.mipi_rxctrl_data[] */
    /* No. elm type , port select
                                     , data format
 { /* 0 */ GGE_MIPI_ASM , GGE_MIPI_PORTO
                                                                     ,MIPI_USID_ASM0_Set0 ,{ {
                                              GGE_MIPI_REG_W
 { /* 1 */ GGE MIPI ASM , GGE MIPI PORTO
                                              GGE MIPI REG W
                                                                     ,MIPI_USID_ASM0_Set0 ,{ {
 { /* 2 */ GGE_MIPI_ASM , GGE_MIPI_PORTO
                                                                     ,MIPI USID ASM0 Set0 ,{ { 124
                                                                                                          , 0x02, 0x02 }, {
                                              GGE_MIPI_REG_W
       3 */ GGE MIPI ASM , GGE MIPI PORTO
                                              GGE MIPI REG W EXT 1ST ,MIPI USID ASM0 Set0 ,{ { 124
                                                                                                             , 0x23, 0x80
```

event type



GSM Part --TX

> 详细列出TX通路ON/OFF时所需的操作步骤:

Event No.	Event Type	Action	Data	Data No.
1	1 77.01	LIM TRY Down 次军时间水大	将ASM MTRX Port设成Idle mode	0
T	TX ON	HM TRX Port 设置Idle状态	将ASM HTRX Port设成Idle mode	1
		Enable PA	设定0x01寄存器的Bias	2
2	TX ON		设置0X00,设定GMSK/8PSK LB PA out	3
			设定0x02,切换 L TRX Port	4
3	TX OFF	关闭TX 通路	将ASM设成low Power 或SW Reset	5

GSM Part --TX

TX部分的格式设置介绍:

```
*MT6177L*/ #define QB_MIPI_TX_ON0_Set0
                                                                                                                      23
                                                                              *MT6177L*/ #define OB MIPI TX ON1 Set0
                                                                                                                      246
                                                                             *MT6177L*/ #define QB_MIPI_TX_ON2_Set0
                                                                                                                      10
                                                                              *MT6177L*/ #define QB_MIPI_TX_ON3_Set0
                                                                              *MT6177L*/ //#define QB_MIPI_TX_ON4
                                                                              *MT6177L*/ //#define QB_MIPI_TX_ON5
                                                                              *MT6177L*/ //#define OB MIPI TX ON6
                                                                                                               173
                                                                             *MT6177L*/ #define QB_MIPI_TX_OFF0_Set0
                                                                              *MT6177L*/ #define QB_MIPI_TX_OFF1_Set0
                                                                             /*MT6177L*/ //#define QB MIPI TX OFF3
                                                                                                               173

_<sup>*</sup>MT6177L*/ //#define QB_MIPI_TX_OFF4

                                                                                                               173
        *GGE MIPI CTRL TABLE GSM900.mipi tx ctrl table.mipi txctrl event[] */
                     element
                                   data idx
                                                 event type
                                                                    event timing */
                                                                                                     Timing
                      type , { start, stop },
        { /* 0 */ GGE MIPI ASM ,
                                                          GGE MIPI TRX ON
                                                                                        QB MIPI TX ON1 Set0
           /* 1 */ GGE MIPI PA
                                                   4 } GGE MIPI TRX ON
                                                                                        QB MIPI TX ON2 Set0
                                                                                        OB MIPI_TX_OFF1_Set0
           /* 2 */ GGE MIPI ASM ,
                                                          GGE MIPI TRX OFF
                                                                 Event
* GGE_MIPI_CTRL_TABLE_GSM900.mipi_tx_ctrl_table.mipi_txctrl_data[] *,
          elm type , port select
                               , data format
                                                              , { { subband arfcn, addr, data }, { subband arfcn, addr, data }, { sub
{ /* 0 */ GGE_MIPI_ASM , GGE_MIPI_PORTO
                                      , GGE_MIPI_REG_W
                                                             ,MIPI_USID_ASM0_Set0 , { { 124
                                                                                              , 0x05, 0x00 }, { GGE_NL
 /* 1 */ GGE MIPI ASM , GGE MIPI PORTO
                                       , GGE_MIPI_REG_W
                                                             ,MIPI_USID_ASM0_Set0 , { {
                                                                                              , 0x03, 0x00 }, {
                                                                                                             GGE NU
 /* 2 */ GGE_MIPI_ASM , GGE_MIPI_PORTO
                                       , GGE MIPI REG W
                                                             ,MIPI_USID_ASM0_Set0 , { {
                                                                                              , 0x01, 0xF7 }, { GGE_NU
 /* 3 */ GGE_MIPI_PA , GGE_MIPI_PORTO
                                      , GGE_MIPI_REG_W
                                                             MIPI USID ASMO SetO , {
                                                                                              , 0x00, GGE MIPI PA G8 }
                                                            ,MIPI_USID_ASM0_Set0_, { {
 /* 4 */ GGE_MIPI_ASM , GGE_MIPI_PORTO
                                        GGE MIPI_REG_W
                                                                                              , 0x02, 0x0F }, { GGE_NL
 /* 5 */ GGE MIPI ASM , GGE MIPI PORTO
                                        GGE MIPI REG W EXT 1ST ,MIPI USID ASM0 Set0 , { 124
                                                                                                 .0x23,0x80 }, { GG
        这里才是真正设定GMSK/8PSK模式的地方:
          /* GGE MIPI CTRL TABLE GSM900.mipi tx ctrl table.mipi txctrl pa data */
          { /* GMSK Data */
            /* subband0 data , subband1 data , subband2 data , subband3 data , subband4 data */
                                     , 0x8A
                0x8A
                            0x8A
            /* 8PSK Data 🥙
              subband0 data , subband1 data , subband2 data , subband3 data , subband4 data */
     MEDI
                0x8B
```

Timing在l1d custom mipi.h中定义

GSM Part --TX

> TX部分的格式设置介绍:

❖ 设置Multi-Slot TX CW Table, register address/Value, MIPI Port 设置正确





TDSCDMA

CONFIDENTIAL B

MEDIATEK

> tl1d_custom_mipi.h文件中需要特别注意的地方:

此处并非USID!

TDS代码中用这个slave id区分器件, 从而分配时序。

```
MIPI Module FIXED
             #define TDD PA Set0
                                                    /*DO NOT CHANGE*
/*MT6177L*/
             #define TDD ASM Set0
                                                     / *DO NOT CHANGE*
                                             0x2
             #define TDD_ETM_Set0
                                                     / *DO NOT CHANGE*
/*MT6177L*/
                                             0x3
             #define DATA NULL Set0
                                                     /*DO NOT CHANGE*/
/*MT6177L*/
                                            OXFFFF
             #define DEVICE NULL Set0
/*MT6177L*/
                                            OxFOFO
                                                    /*DO NOT CHANGE*/
             #define PA FLAG Set0
                                                     *DO NOT CHANGE*/
/*MT6177L*/
                                            0xF000
```

设置TDD_TXM_FLAG_BAND34/39_Set0,如果band34/39 Tx reuse TXM

TDSCDMA

▶ tl1d_custom_mipi.h 重新定义USID by band and MIPI

```
#define TDD ASM USID BAND34 Set0
                                                   (MIPI USID ASM0 Set0 <<3)
/*MT6177L*/
            #define TDD_ASM_USID_BAND39_Set0
                                                   (MIPI USID ASM0 Set0 <<3)
/*MT6177L*/
            #define TDD PA USID BAND34 Set0
                                                  (MIPI USID ASM0 Set0 <<3)
/*MT6177L*/
            #define TDD PA USID BAND39 Set0/
                                                  (MIPI_USID_ASM0_Set0 <<3)
/*MT6177L*/
            #define TDD ETM USID Set0
                                                  (0 << 3)//no use
/*MT6177L*/
   MIPI Port
            #define MIPI PORTO Set0
/*MT6177L*/
                                             (0 <<12) /*PORT_NUM<<12*/
            #define MIPI_PORT1_Set0
/*MT6177L*/
                                             1/<<12) /*PORT NUM<<12*/
            #define MIPI_PORT2_Set0
/*MT6177L*/
                                             (ź <<12) /*PORT_NUM<<12*/
            #define MIPI PORT3 Set0
                                             (3 <<12) /*PORT NUM<<12*/
/*MT6177L*/
/*MT6177L*/
            #define MIPI PORT4 Set0
                                            (4 <<12) /*PORT_NUM<<12*/
            #define MIPI PORT5 Set0
                                            (5 <<12) /*PORT_NUM<<12*/
/*MT6177L*/
            #define MIPI PORT6 Set0
                                            (6 <<12) /*PORT_NUM<<12*/
/*MT6177L*/
            #define MIPI PORT7 Set0
                                            (7 <<12) /*PORT_NUM<<12*/
/*MT6177L*/
            #define MIPI USID INITO PORTO Set0
/*MT6177L*/
                                                 0x0000
            #define MIPI USID ASMO PORTO Set0
/*MT6177L*/
                                                 0x000F
            #define MIPI USID ASMO PORT3 Set0
/*MT6177L*/
                                                 0x003F
            #define MIRI USID ASM1 PORTO Set0
/*MT6177L*/
                                                 0x0008
            #define MIPI_USID_ASM2_PORTO_Set0
/*MT6177L*/
                                                 0x000A
            #define MIPI USID ASM3 PORTO Set0
/*MT6177L*/
                                                 0x0009
            #define MIPI_USID_PA0_PORTO_Set0
/*MT6177L*/
                                                0x000F
            #define MIPI USID PA0 PORT3 Set0
/*MT6177L*/
                                                0x003F
            #define MIPI USID PA1 PORTO Set0
/*MT6177L*/
                                                0x000E
            #define MIPI USID ANTO PORTO Set0
/*MT6177L*/
                                                 0x0006
```

TDSCDMA--RX ON/OFF

```
typedef enum
                                TDSCDMA_REG_R = 0,
                                                        0x05, 0x01 TXM 切换到B39 Rx Port
                                TDSCDMA REG W
                               TOP TYPE;
/*MIPI Data Table For Band39*/
/*Data Num Do Not Exceed 16 For Each Scenario*/
  /*Band39 Rx On Data*/
                              PORT
                                          OPERATION :
    {/* 0*/ TDD_ASM_Set0 | MIPI_PORT0_Set0 , TDSCDMA_REG_W |,
                                                          TDD ASM USID BAND39 Set0 , 0x05, 0x01 },
    {/* 1*/ DATA NULL Set0, 0
Module一定要设对,否则会调用错时序!
                                             #define TDD ASM USID BAND34 Set0
                                                                           (MIPI_USID_ASM0_Set0 <<3)
有些器件如sky779XX,又是ASM又是PA。
                                             #define TDD ASM USID BAND39 Set0
                                                                           (MIPI USID ASM0 Set0 <<3)
                                             #define TDD PA USID BAND34 Set0
                                                                          (MIPI_USID_ASM0_Set0 <<3)
在RX的Event里面就把它定义成
                                             #define TDD_PA_USID_BAND39_Set0
                                                                          (MIPI_USID_ASM0_Set0 <<3)
                                             #define TDD ETM USID Set0
                                                                       (0 << 3)//no use
MIPI_ASM, 在TX Event里面就把他定义
成MIPI PA。
*Band39 Rx Off Data*/
                                           OPERATION ,
             MODULE
                             PORT
                                                            USID
                                                                            , ADDR, DATA*/
 {/* 0*/ TDD_ASM_Set0 , MIPI_PORT0_Set0 TDSCDMA_REG_W , TDD_ASM_USID_BAND39_Set0 , 0x05, 0x00 },
                        MIPI PORTO SetO, TDSCDMA REG W, TDD ASM USID BAND39 SetO, 0x23, 0x80 },
 {/* 1*/ TDD ASM Set0
```

Note: Ex:Sky77928-11,Off Event Sky77928-11,2G/TD/LTE TD 需要SW Reset 0x23,0x80;

МЕДІЛТЕК

TDSCDMA--TX on

▶ TX On Table element type 必须设置为TDD_PA_Set*,I Bias 取自Vendor提供的参考List

```
/*Band39 Tx On Data*/
                                    PORT
                                                  OPERATION,
                                                                   USID
                    MODULE
                                                                                   ADDR, DATA
                              MIPL PORTO SetO TOSCOMA REG W TOD PA USID BAND39 SetO
         {/* 1*/ TDD ASM Set0 , MIPI PORTO Set0 , TDSCDMA REG W , TDD ASM USID BAND39 Set0 , 0x04, 0x10 },
                                                                                                               ASM On
         {/* 2*/ TDD ASM Set0 , MIPI PORTO Set0 , TDSCDMA REG W , TDD ASM USID BAND39 Set0 , 0x05, 0x0F },
     /*PA Mode Data for BAND39*/
     /*Data Num Do Not Exceed 8 for Each Scenario*/
                                                                                                       Max data num = 8
                               , MIPI_PORTO_Set0 , TDSCDMA_REG_W , TDD_PA_USID_BAND39_Set0 , 0x00, 0x8F },//PA HIGH MODE
                              , MIPI PORTO SetO , TDSCDMA REG W , TDD PA USID BAND39 SetO , 0x01, 0x8E },//PA HIGH MODE
H Mode
                              , MIPI_PORTO_Set0 , TDSCDMA_REG_W , TDD_PA_USID_BAND39_Set0 , 0x04, 0x10 },//PA HIGH MODE
          {/* 3*/ TDD PA Set0 , MIPI PORTO Set0 , TDSCDMA REG W , TDD PA USID BAND39 Set0 , 0x02 , 0x00 },//PA HIGH MODE
           (/* 4*/ DATA NULL Set0, 0
          {/* 5*/ DATA_NULL_Set0, 0
                                               , 0
                                                                              , 0 , 0
                                                                                      },//PA HIGH MODE
          {/* 6*/ DATA NULL Set0, 0
                                                                                      }//PA HIGH MODE
                                               . 0
                     MODULE
                                     PORT
                                                   OPERATION ,
                                                                    USID
                                                                                    , ADDR, DATA*/
                              , MIPI_PORTO_Set0 , TDSCDMA_REG_W , TDD_PA_USID_BAND39_Set0 , 0x00, 0xAF },//PA_MIDDLE_MODE
                              , MIPI_PORTO_Set0 _TDSCDMA_REG_W , TDD_PA_USID_BAND39_Set0 , 0x01, 0x28 },//PA MIDDLE MODE
                              , MIPI_PORTO_Set0 , JDSCDMA REG_W , TDD_PA_USID_BAND39_Set0 , 0x04, 0x10 },//PA MIDDLE MODE
M Mode //* 3*/ TDD_PA_Set0
                               , MIPI_PORTO_Set0 , TDSCDMA_REG_W , TDD_PA_USID_BAND39_Set0 , 0x02, 0x00 },//PA_MIDDLE_MODE
          {/* 4*/ DATA NULL Set0, 0
          {/* 5*/ DATA_NULL_Set0, 0
                                                                                      },//PA MIDDLE MODE
          {/* 6*/ DATA_NULL_Set0, 0
                                                                                      }//PA MIDDLE MODE
                                                                    USID
                                                                                     ADDR. DATA*/
                               , MIPI_PORTO_Set0_TDSCDMA_REG_W , TDD_PA_USID_BAND39_Set0_, 0x00, 0xAF },//PA_MIDDLE_MODE
                               , MIPI_PORTO_Set0 , TDSCDMA_REG_W , TDD_PA_USID_BAND39_Set0 , 0x01, 0x28 },//PA_MIDDLE_MODE
L Mode
                               , MIPI_PORTO_Set0 , TDSCDMA_REG_W , TDD_PA_USID_BAND39_Set0 , 0x04, 0x10 },//PA_MIDDLE_MODE
                               , MIPI_PORTO_Set0_TDSCDMA_REG_W , TDD_PA_USID_BAND39_Set0 , 0x02, 0x00 },//PA_MIDDLE_MODE
                                                         , 0
          {/* 5*/ DATA NULL Set0.0
                                                                                      },//PA MIDDLE MODE
          {/* 6*/ DATA_NULL_Set0, 0
                                                        , 0
                                                                                      }//PA MIDDLE MODE
       MEDIATEK
                      CONFIDENTIAL B
```

TDSCDMA--TX off

Note: Ex:Sky77928-11,Off Event Sky77928-11,2G/TD/LTE TD 需要SW Reset 0x23,0x80;

WEDIATEK



WCDMA--RX

Event No.	Event Type	Action	Data	Data No.
1	DV ON	・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・	打开PRX ASM TRX Path	0
1 RX ON	KX ON	设置到active状态	打开DRX ASM TRX Path	1
2	RX OFF	设置到Idle状态	PRX ASM Idle mode	2-3
2	2		DRX ASM Idle mode	4

```
const UL1_MIPI_EVENT_TABLE_T UMTS_MIPI_RX_EVENT_UMTSBand1_Set0[UL1_MIPI_RX_EVENT_NUM] =
 / * No.
          elm type , data idx
                               , evt type
                                            evt offset
               { start, stop },
                                       ( us )
 { /* 0 */ UL1 MIPI ASM
                                        }, UL1_MIPI_TRX_ON, US2CHIPCNT(200)
       */ UL1_MIPI_ASM_RXD,
                                        }, UL1_MIPI_TRX_ON, US2CHIPCNT(200)
                                                                                  Timing fixed!
      2 */ UL1 MIPI ASM
                                        UL1 MIPI TRX OFF, US2CHIPCNT(10)
       */ UL1 MIPI ASM RXD,
                                          UL1_MIPI_TRX_OFF, US2CHIPCNT(10)
```

```
const UL1_MIPI_DATA_SUBBAND_TABLE_T UMTS MIPI_RX_DATA_UMTSBand1_Set0[UL1_MIPI_RX_DATA_NUM] =
                                                      { sub 0 ,addr, data }},{ sub 1 ,addr, data }},{ sub 2 ,addr, data}}, { sub 3, addr, d
          elm type , port sel
                               , data seg , userid,
 //No.
                               UL1_MIPI_PORTO, UL1_REG_W
 { /* 0 */ UL1_MIPI_ASM,
                                                              , MIPI_USID_ASM0_Set0, { { 21124 , {0x05, 0x05}}, { 21262 , {0x05, 0x05}}}
  { /* 1 */ UL1_MIPI_ASM_RXD, UL1_MIPI_PORT2, UL1_REG_W
                                                              MIPI_USID_ASM1_Set0, { { 21124 ,{0x00, 0x04}}, { 21262 ,{0x00, 0x04}}}
  { /* 2 */ UL1_MIPI_ASM,
                               UL1_MIPI_PORTO, UL1_REG_W
                                                              , MIPI_USID_ASM0_Set0, { { 21124 ,{0x05, 0x00}}}, { 21262 ,{0x05, 0x00}}
  { /* 3 */ UL1 MIPI ASM,
                               UL1 MIPI PORTO, UL1 REG W
                                                              , MIPI_USID_ASM0_Set0, { { 21124 ,{0x04, 0x00}}, { 21262 ,{0x04, 0x00}}}
  { /* 4 */ UL1_MIPI_ASM_RXD, UL1_MIPI_PORT2, UL1_REG_W
                                                              , MIPI USID ASM1 Set0, { { 21124 ,{0x00, 0x00}}, { 21262 ,{0x00, 0x00}}}
```

每个subband都要修改!



WCDMA--TX

Event No.	Event Type	Action	Data	Data No.
			设置寄存器0x00 idle mode	0
_	T. OFF	DA: JI. JE	设置寄存器0x01 idle mode	
1	Tx OFF	PA idle 状态	设置寄存器0x02 idle mode	
			设置寄存器0x03 idle mode	3
		2G TX Port Off	设置寄存器0x00 TX Off mode	4
		H TRX Port off	H TRX Port Off mode	5
2	TX On	L TRX Port off	L TRX Port Off mode	6
		M TRX Port active	设置寄存器0x05 on mode	7
		Tx Coupler Active	设置寄存器0x04 Tx Coupler	0 1 2 3 4 5

WCDMA——TX

```
const UL1_MIPI_EVENT_TABLE_T UMTS_MIPI_TX_EVENT_UMTSBand1_Set0[UL1_MIPI_TX_EVENT_NUM] =
      /* No.
                elm type , data idx
                                          , evt type
                                                          , evt offset
                                                                                  Timing Fixed!
                    { start, stop },
                                                  ( us )
  { /* 0 */ UL1 MIPI PA, | { 0
                                           }, UL1 MIPI TRX OFF,
                                                                        US2CHIPCNT(10) },
  { /* 1 */ UL1_MIPI_ASM, { 4 , 8
                                           }, UL1_MIPI_TRX_ON,
                                                                        US2CHIPCNT(200) }
const UL1 MIPI DATA SUBBAND TABLE T UMTS MIPI TX DATA UMTSBand1 Set0[UL1 MIPI TX DATA NUM] =
                                                                                                         Data
 //No.
          elm type , port_sel

    , data_seq , user id,

                                                      { { sub 0 ,addr, data }},{ sub 1 ,addr, data }},{ sub 2 ,addr, data}}, { sub 3, add
 { /* 0 */ UL1_MIPI_PA , UL1_MIPI_PORT1, UL1_REG_W ,
                                                       MIPI_USID_PA0_Set0
                                                                              , { { 19224 ,{0x00, 0x00}}, { 19362 ,{0x00, 0x00}}},
                                                                              , { { 19224 , {0x01, 0x00}}, { 19362 , {0x01, 0x00}},
  { /* 1 */ UL1_MIPI_PA , UL1_MIPI_PORT1, UL1_REG_W
                                                       MIPI USID PAO Set0
  { /* 2 */ UL1_MIPI_PA , UL1_MIPI_PORT1, UL1_REG_W
                                                       MIPI USID PA0 Set0
                                                                              , { { 19224 ,{0x02, 0x00}}, { 19362 ,{0x02, 0x00}},
  { /* 3 */ UL1 MIPI PA , UL1 MIPI PORT1, UL1 REG W
                                                       MIPI USID PA0_Set0
                                                                               { { 19224 ,{0x03, 0x00}}, { 19362 ,{0x03, 0x00}}},
  { /* 4 */ UL1_MIPI_ASM , UL1_MIPI_PORTO, UL1_REG_W
                                                       MIPI_USID_ASM0_Set0
                                                                               { { 19224 ,{0x00, 0x80}}, { 19362 ,{0x00, 0x80}},
                                                                              , { { 19224 ,{0x02, 0x00}}, { 19362 ,{0x02, 0x00}},
  { /* 5 */ UL1 MIPI ASM , UL1 MIPI PORTO, UL1 REG W
                                                       MIPI USID ASM0 Set0
 { /* 6 */ UL1_MIPI_ASM , UL1_MIPI_PORTO, UL1_REG_W
                                                        MIPI USID ASM0 Set0
                                                                               { { 19224 ,{0x03, 0x00}}, { 19362 ,{0x03, 0x00}}},
 { /* 7 */ UL1_MIPI_ASM , UL1_MIPI_PORTO, UL1_REG_W ,
                                                        MIPI USID ASM0 Set0
                                                                              , { { 19224 ,{0x05, 0x05}}}, { 19362 ,{0x05, 0x05}}},
  { /* 8 */ UL1 MIPI ASM , UL1 MIPI PORTO, UL1 REG W
                                                        MIPI USID ASM0 Set0
                                                                              , { { 19224 , {0x04, 0x10}}, { 19362 , {0x04, 0x10}}
```

Note:

- ❖ WCDMA TX部分不用配置PA ON, PA ON的data都在TPC段配置。这样可以减少几笔 data, 改善某些test case的margin。
- ❖ 由TX Event的定义可以看出,data0~3是设成PA OFF的。如果这个地方错填了PA ON的值,会导致WCDMA待机电流居高不下。

WCDMA--TX

CONFIDENTIAL B

MEDIATEK

▶ 为什么WCDMA TX没有设ASM OFF?

```
const UL1_MIPI_EVENT_TABLE_T UMTS_MIPI_TX_EVENT_UMTSBand1_Set0[UL1_MIPI_TX_EVENT_NUM] =
                                             , evt offset
            elm type , data idx
                                , evt_type
    /* No.
                { start, stop },
                                      ( us )
 { /* 0 */ UL1_MIPI_PA, { 0 , 3 }, UL1_MIPI_TRX_OFF,
                                                        US2CHIPCNT(10) },
 { /* 1 */ UL1_MIPI_ASM, { 4 , 8 }, UL1_MIPI_TRX_ON,
                                                        US2CHIPCNT(200) },
   ASMO ON
                                                                                  ASM OFF
              ASM&PA ON
                                                                     PA OFF
                                         TX
                                                                   TX OFF
      RX ON
                 TX ON
                                                                                    RX OFF
                                                                     ASM OFF
```

❖ 假设在TX OFF的时候就关闭ASM, 那么RX通路也会

被同时关闭, 在某些场景下会失去网络链接!

WCDMA--TPC

{UL1_MIPI_PA , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,

```
const UL1 UMTS MIPI TPC T UMTS MIPI TPC UMTSBand1 Set0 =
  / * Event */
 /* No.
              elm type , data idx
                                                  evt_offset
                    { start, stop },
  { /* 0, Prf_7 */ UL1_MIPI_PA, { 0
                                                                 , US2CHIPCNT(20) / *highest power*/
                                           }, UL1_MIPI_TPC_SET
  { /* 1, Prf_6 */ UL1_MIPI_PA, { 4
                                           }, UL1_MIPI_TPC_SET
                                                                 , US2CHIPCNT(20)
  { /* 2, Prf_5 */ UL1_MIPI_PA, { 8
                                           }, UL1_MIPI_TPC_SET
                                                                 , US2CHIPCNT(20)
  { /* 3, Prf_4 */ UL1_MIPI_PA, { 12 , 15
                                                                 , US2CHIPCNT(20)
                                          }, UL1 MIPI TPC SET
  { /* 4, Prf_3 */ UL1_MIPI_PA, { 16
                                          }, UL1_MIPI_TPC_SET
                                                                 US2CHIPCNT(20)
  { /* 5, Prf 2 */ UL1 MIPI PA, { 20 , 23
                                          }, UL1 MIPI TPC SET/
                                                                  US2CHIPCNT(20)
  { /* 6, Prf_1 */ UL1_MIPI_PA, { 24 , 27
                                                                 US2CHIPCNT(20)
                                          }, UL1_MIPI_TPC_SET
  { /* 7, Prf 0 */ UL1 MIPI PA, { 28 , 31
                                         }, UL1_MIPI_TPC_SET
                                                                 , US2CHIPCNT(20) }, /*lowest power*/
```

PA的状态都由TPC设置段决定

按从上而下的顺序,WCDMATX功率由高到低!每一档位的设定请结合校准使用的ini文件,参考Vendor给的值。

 $\{\{19224, \{0x03, 0x86\}\}, \{19362, \{0x03, 0x86\}\}, \{19500, \{0x03, 0x86\}\}, \{19638, \{0x03, 0x86\}\}, \{19776, \{0x03, 0x86\}\}\}$

```
, data_seq, user id,
                                                                                                          {{sub 0, addr, data}}, {{sub 1, addr, data}}, {{sub 2, addr, data} , {{sub 3, addr, data}}, {{sub 4, addr, data}
//elm type , port_sel
 {UL1_MIPI_PA
                                                                                                                                                               {{19224, {0x00, 0x1C}}}, {19362, {0x00, 0x1C}}, {19500, {0x00, 0x1C}}, {19638, {0x00, 0x1C}}, {19776, {0x00, 0x1C}}
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                 , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               {{19224, {0x01, 0xCA}}, {19362, {0x01, 0xCB}}, {19500, {0x01, 0xCB}}, {19638, {0x01, 0xCC}}, {19776, {0x01, 0xCC}}
 {UL1_MIPI_PA
 {UL1 MIPI PA
                                 , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                             (\{\{19224, \{0x02, 0x20\}\}, \{19362, \{0x02, 0x20\}\}, \{19500, \{0x02, 0x20\}\}, \{19638, \{0x02, 0x20\}\}, \{19776, \{0x02, 0x20\}\})
 {UL1_MIPI_PA
                                 , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0;
                                                                                                                                                               \{\{19224, \{0x03, 0x8B\}\}, \{19362, \{0x03, 0x8B\}\}, \{19500, \{0x03, 0x8B\}\}, \{19638, \{0x03, 0x8B\}\}, \{19776, \{0x03, 0x8B\}\}\}
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                                {{19224, {0x00, 0x1c}}, {19362, {0x00, 0x1c}}, {19500, {0x00, 0x1c}}, {19638, {0x00, 0x1c}}, {19776, {0x00, 0x1c}}
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               \{\{19224, \{0x01, 0x47\}\}, \{19362, \{0x01, 0x47\}\}, \{19500, \{0x01, 0x47\}\}, \{19638, \{0x01, 0x47\}\}, \{19776, \{0x01, 0x47
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                                \{\{19224, \{0x02, 0x20\}\}, \{19362, \{0x02, 0x20\}\}, \{19500, \{0x02, 0x20\}\}, \{19638, \{0x02, 0x20\}\}, \{19776, \{0x02, 0x20\}\}\}
 {UL1 MIPI PA
                                  , UL1 MIPI PORT1 , UL1 REG W , MIPI USID PAO Set0,
                                                                                                                                                                {{19224, {0x03, 0x86}}, {19362, {0x03, 0x86}}, {19500, {0x03, 0x86}}, {19638, {0x03, 0x86}}, {19776, {0x03, 0x86}}
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               {{19224, {0x00, 0x1C}}, {19362, {0x00, 0x1C}}, {19500, {0x00, 0x1C}}, {19638, {0x00, 0x1C}}, {19776, {0x00, 0x1C}}
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               \{\{19224, \{0x01, 0x46\}\}, \{19362, \{0x01, 0x46\}\}, \{19500, \{0x01, 0x46\}\}, \{19638, \{0x01, 0x46\}\}, \{19776, \{0x01, 0x46
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               \{\{19224, \{0x02, 0x20\}\}, \{19362, \{0x02, 0x20\}\}, \{19500, \{0x02, 0x20\}\}, \{19638, \{0x02, 0x20\}\}, \{19776, \{0x02, 0x20\}\}\}
 {UL1_MIPI_PA
                                 , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                                \{\{19224, \{0x03, 0x86\}\}, \{19362, \{0x03, 0x86\}\}, \{19500, \{0x03, 0x86\}\}, \{19638, \{0x03, 0x86\}\}, \{19776, \{0x03, 0x86\}\}\}
 {UL1_MIPI_PA
                                 , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               \{\{19224, \{0x00, 0x1C\}\}, \{19362, \{0x00, 0x1C\}\}, \{19500, \{0x00, 0x1C\}\}, \{19638, \{0x00, 0x1C\}\}, \{19776, \{0x00, 0x1C\}\}\}
 {UL1_MIPI_PA
                                 , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               \{\{19224, \{0x01, 0x36\}\}, \{19362, \{0x01, 0x36\}\}, \{19500, \{0x01, 0x36\}\}, \{19638, \{0x01, 0x36\}\}, \{19776, \{0x01, 0x36\}\}, \{19638, \{0x01, 0x36\}\}, \{19776, \{0x01, 0x36
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                                {{19224, {0x02, 0x20}}, {19362, {0x02, 0x20}}, {19500, {0x02, 0x20}}, {19638, {0x02, 0x20}}, {19776, {0x02, 0x20}}
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                                {{19224, {0x03, 0x86}}, {19362, {0x03, 0x86}}, {19500, {0x03, 0x86}}, {19638, {0x03, 0x86}}, {19776, {0x03, 0x86}}
 {UL1_MIPI_PA
                                                                                                                                                                  {19224, {0x00, 0x1C}}, {19362, {0x00, 0x1C}}, {19500, {0x00, 0x1C}}, {19638, {0x00, 0x1C}}, {19776, {0x00, 0x1C}}
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               \{\{19224, \{0x01, 0x35\}\}, \{19362, \{0x01, 0x35\}\}, \{19500, \{0x01, 0x35\}\}, \{19638, \{0x01, 0x35\}\}, \{19776, \{0x01, 0x35\}\}\}
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                                  {19224, {0x02, 0x20}}, {19362, {0x02, 0x20}}, {19500, {0x02, 0x20}}, {19638, {0x02, 0x20}}, {19776, {0x02, 0x20}}
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               {{19224, {0x03, 0x86}}, {19362, {0x03, 0x86}}, {19500, {0x03, 0x86}}, {19638, {0x03, 0x86}}, {19776, {0x03, 0x86}}
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W
                                                                                                            MIPI_USID_PA0_Set0,
                                                                                                                                                               \{\{19224, \{0x00, 0x1C\}\}, \{19362, \{0x00, 0x1C\}\}, \{19500, \{0x00, 0x1C\}\}, \{19638, \{0x00, 0x1C\}\}, \{19776, \{0x00, 0x1C\}\}\}
 {UL1_MIPI_PA
                                 , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                                \{\{19224, \{0x01, 0x25\}\}, \{19362, \{0x01, 0x25\}\}, \{19500, \{0x01, 0x25\}\}, \{19638, \{0x01, 0x25\}\}, \{19776, \{0x01, 0x25\}\}\}
 {UL1_MIPI_PA
                                 , UL1_MIPI_PORT1 , UL1_REG_W ,
                                                                                                            MIPI_USID_PA0_Set0,
                                                                                                                                                               \{\{19224, \{0x02, 0x20\}\}, \{19362, \{0x02, 0x20\}\}, \{19500, \{0x02, 0x20\}\}, \{19638, \{0x02, 0x20\}\}, \{19776, \{0x02, 0x20\}\}\}
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               \{\{19224, \{0x03, 0x86\}\}, \{19362, \{0x03, 0x86\}\}, \{19500, \{0x03, 0x86\}\}, \{19638, \{0x03, 0x86\}\}, \{19776, \{0x03, 0x86\}\}\}
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                                  [{19224, {0x00, 0x1C}}, {19362, {0x00, 0x1C}}, {19500, {0x00, 0x1C}}, {19638, {0x00, 0x1C}}, {19776, {0x00, 0x1C}}
 {UL1 MIPI PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W ,
                                                                                                           MIPI USID PA0 Set0,
                                                                                                                                                               \{\{19224, \{0x01, 0x16\}\}, \{19362, \{0x01, 0x16\}\}, \{19500, \{0x01, 0x16\}\}, \{19638, \{0x01, 0x16\}\}, \{19776, \{0x01, 0x16\}\}\}
 {UL1_MIPI_PA
                                                                                                                                                                \{\{19224, \{0x02, 0x20\}\}, \{19362, \{0x02, 0x20\}\}, \{19500, \{0x02, 0x20\}\}, \{19638, \{0x02, 0x20\}\}, \{19776, \{0x02, 0x20\}\}\}
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
 {UL1_MIPI_PA
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               {{19224, {0x03, 0x86}}, {19362, {0x03, 0x86}}, {19500, {0x03, 0x86}}, {19638, {0x03, 0x86}}, {19776, {0x03, 0x86}}
 {UL1 MIPI PA
                                                                                                                                                               \{\{19224, \{0x00, 0x1C\}\}, \{19362, \{0x00, 0x1C\}\}, \{19500, \{0x00, 0x1C\}\}, \{19638, \{0x00, 0x1C\}\}, \{19776, \{0x00, 0x1C\}\}\}
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                  , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               \{\{19224, \{0x01, 0x15\}\}, \{19362, \{0x01, 0x15\}\}, \{19500, \{0x01, 0x15\}\}, \{19638, \{0x01, 0x15\}\}, \{19776, \{0x01, 0x15\}\}\}
 {UL1_MIPI_PA
 {UL1 MIPI PA
                                 , UL1_MIPI_PORT1 , UL1_REG_W , MIPI_USID_PA0_Set0,
                                                                                                                                                               \{\{19224, \{0x02, 0x20\}\}, \{19362, \{0x02, 0x20\}\}, \{19500, \{0x02, 0x20\}\}, \{19638, \{0x02, 0x20\}\}, \{19776, \{0x02, 0x20\}\}\}
```

MEDIATEK

CONFIDENTIAL B

LTE Part

LTE--RX

LTE FDD Band RX通路ON/OFF时所需的操作步骤

Event No.	Event Type	Action	Data	Data No.
0	a By an	:ひ架列はは小井本	将PRX ASM设成active mode	0
0	RX ON	设置到Idle状态	打开DRX ASM对应的TRX Path	1
1	1 DV 055	VV 문지나의 작가수	将PRX ASM设成idle mode	2
	RX OFF	设置到Idle状态	将DRX ASM设成low power mode	

```
Timing在Ite custom mipi.h中定义
                                                                          *MIPI ASM
                                                                          / *FDD RX ON */
                                                                         #define LTE FDD MIPI ASM RX ONO Set0
                                                                                                                 US2OFFCNT(15)
                                                                         #define LTE FDD MIPI ASM RX ON1 Set0 US2OFFCNT(0)
                                                                          *MIPI ASM
                                                                         /*FDD RX OFF */
                                                                         #define LTE_FDD_MIPI_ASM_RX_OFF0_Set0 US2OFFCNT(5)
LTE_MIPI_EVENT_TABLE_T LTE_Band1_MIPI_RX_EVENT_Set0[] =
                                                                         #define LTE FDD MIPI ASM RX OFF1 Set0 US2OFFCNT(0)
 / * No.
                                    , evt_type Fventevt_offset
                      , data idx
           elm type
                    { start, stop }
                                                ( us )
 { /* 0 */ LTE_MIPI_ASM , { 0
                                                              LTE FDD MIPI ASM RX ON0 Set0 },
                                         LTE MIPI TRX ON
                                                                                                           Timing
                                                              LTE_FDD_MIPI_ASM_RX_OFF0_Set0},
 { /* 1 */ LTE MIPI ASM , { 2
                                         LTE_MIPI_TRX_OFF
      2 */ LTE_MIPI_NULL, { 0
                                         LTE MIPI EVENT NULL, O
LTE_MIPI_DATA_SUBBAND_TABLE_T LTE_Band1_MIPI_RX_DATA_Set0[] =
                                                                                                     Data
                                               , USID
  //No.
          elm type
                     , port_sel
                                  , data_seq
                                                                   ,{ { subband-0 freq _,addr ,data }, { subband-1 freq
                                                        , MIPI_USID_ASM0_Set0 | ,{ { 21100 /*100 kHz*/ ,0x05 ,0x05 }
  { /* 0 */ LTE MIPI ASM , LTE MIPI PORTO , LTE REG W
                                                                               ,{ { 21100 /*100 kHz*/ ,0x00 ,0x04 }
  { /* 1 */ LTE MIPI ASM , LTE MIPI PORT2
                                                        , MIPI USID ASM1 Set0 |
                                          , LTE REG W
  { /* 2 */ LTE_MIPI_ASM, LTE_MIPI_PORTO
                                                                               ,{ { 21100 /*100 kHz*/ ,0x05 ,0x00 }
                                          , LTE REG W
                                                        , MIPI USID ASM0 Set0
  { /* 3 */ LTE MIPI ASM , LTE MIPI PORT2
                                          , LTE REG W
                                                        , MIPI_USID_ASM1_Set0 | ,{ { 21100 /*100 kHz*/ ,0x00 ,0x00 }
    * 4 */ LTE MIPI NULL, 0
                                              , 0
```

LTE--RX > LTE TDD Band [B38/40/41]

MEDIATEK

CONFIDENTIAL B

Event No.	Event Type	Action	Data	Data No.
•	DV ON	设置到ASM Active状态	打开PRX ASM对应的TRX Path	0
0 RX ON 设置	设直到ASIVI ACTIVE认念	打开DRX ASM对应的TRX Path	1	
1	RX ON	设置到3P4T Active状态	将PA 3P4T 切换成TX output	2
	2 RX OFF	设置到Idle状态	将 PRX ASM设成idle mode	3
2			将DRX ASM设成idle mode	4
			将MMM PA 3P4T开关关闭	5

```
#define LTE TDD MIPI ASM RX ONO Set0
                                                                              #define LTE_TDD_MIPI_ASM_RX_ON1_Set0 US2OFFCNT(0)
LTE MIPI EVENT TABLE T LTE Band40 MIPI RX EVENT Set0[] =
                                                                             /*TDD RX OFF */
                                                                              #define LTE TDD MIPI ASM RX OFFO Set0 US2OFFCNT(5)
                                                                              #define LTE_TDD_MIPI_ASM_RX_OFF1_Set0_US2OFFCNT(0)
  /* No.
             elm type
                          , data idx
                                         , evt type
                                                           evt_offset
                                                                                                        Timing
                       { start, stop }
                                                      (us) Fvent
  { /* 0 */ LTE MIPI ASM , { 0
                                              LTE MIPI TRX ON
                                                                     LTE TOD MIPI ASM RX ONO Seto
   { /* 1 */ LTE MIPI ASM ,
                                              LTE MIRI TRX OFF
                                                                      LTE TDD MIPI ASM RX OFF0 Set0
   { /* 2 */ LTE MIPI NULL,
                                              LTE MIRI EVENT NULL, 0
};
LTE MIPI DATA SUBBAND TABLE T LTE Band40 NIPI RX DATA Set0[] =
                                                                                                Data
 //No.
          elm type
                                                                     ,{ { subband-0 freq __,addr ,data }, { subband-1 freq
                     , port_sel
                                                                                 ,{ { 23000 /*100 kHz*/ ,0x03 ,0x40 }, {
  { /* 0 */ LTE MIPI ASM , LTE MIPI PORTO
                                            LTE REG W
                                                          , MIPI USID ASM0 Set0
  { /* 1 */ LTE MIPI ASM , LTE MIPI PORT2
                                                                                 ,{ { 23000 /*100 kHz*/ ,0x00 ,0x08 }, {
                                           LTE REG W
                                                          , MIPI USID ASM2 Set0
                                                                                 ,{ { 23000 /*100 kHz*/ ,0x02 ,0x02 },
  { /* 2 */ LTE MIPI ASM , LTE MIPI PORT1
                                           LTE REG W
                                                          , MIPI USID PA0 Set0
                                                                                 ,{ { 23000 /*100 kHz*/ ,0x03 ,0x00 }, {
  { /* 3 */ LTE MIPI ASM , LTE MIPI PORTO
                                           , LTE REG W
                                                          , MIPI USID ASM0 Set0
  { /* 4 */ LTE_MIPI_ASM / LTE_MIPI_PORT2
                                           , LTE_REG_W
                                                                                 ,{ { 23000 /*100 kHz*/ ,0x00 ,0x00 }, {
                                                          , MIPI_USID_ASM2_Set0
                                                                                  ,{ { 23000 /*100 kHz*/ ,0x02 ,0x00 },
  { /* 5 */ LTE MIPI ASM, LTE MIPI PORT1
                                           , LTE REG W
                                                          , MIPI USID PA0 Set0
  { / * 6 */ LTE MIPI NULL, T
                                                                        0 / *100 kHz*/ ,0 ,0 }, {
                                                                                                    0 /*100 kHz*/ ,0
```

> 列出TX通路ON/OFF时所需的操作步骤:

Event No.	Event Type	Action	Data	Data No.
			设定PA寄存器0	0
	TV ON	Fachla DA	设定PA寄存器1	1
0	TX ON	Enable PA	设定PA寄存器4	2
			设定TXM coupler 寄存器0x04	3
-	TV OFF	关闭PA	设定PA寄存器0	4
1	TX OFF	关闭 TXM TX Coupler	设定TXM Tx Coupler off	5
2	TX ON	打开ASM	将ASM切到TRX Port	6

Note: 和WCDMA一样, FDD-LTE在TX OFF的时候不能关闭ASM, 但是TDD-LTE在TX OFF的时候可以关闭ASM。目前设定都是TX不去关ASM, 都由RX去关ASM。



```
Timing在Ite_custom_mipi.h中定义
```

, MIPI_USID_ASM0_Set0 ,{ | { 19200 / *100 kHz*/

/*100 kH2*/ ,0 ,0 }, { 0

,0x05 , 0x05},

/*100 kHz*/

```
/ *FDD TX ON / */
                                                                 #define LTE FDD MIPI ASM TX ONO Set0
                                                                                                      US20FFCNT(15)
                                                                 #define LTE_FDD_MIPI_ASM_TX_ON1_Set0
                                                                                                      US2OFFCNT(0)
    LTE FDD Band
                                                                  *MIPI PA
                                                                 /*FDD TX ON _*/
                                                                 #define LTE FDD MIPI PA TX ONO SetO
                                                                                                      US20FFCNT(25)
                                                                 #define LTE FDD MIPI PA TX ON1 Set0
                                                                                                      US2OFFCNT(0)
                                                                  /*MIPI PA
                                                                  *FDD TX OFF
                                                                 #define LTE_FDD_MIPI_PA_TX_OFF0_Set0 US2OFFCNT(20)
                                                                 #define LTE_FDD_MIPI_PA_TX_OFF1_Set0 US2OFFCNT(0)
LTE MIPI EVENT TABLE T LTE Band1 MIPI TX EVENT Set0 =
                                                                                           Timing
                                                    Event
  /* No.
                                                    evt_offset
           elm type
                      , data idx
                                   , evt type
                    { start, stop }.
  { /* 0 */ LTE_MIPI PA
                                        LTE MIPI TRX ON
                                                            LTE FDD MIPI PA TX ONO Set0 }, // PA On
  { /* 1 */ LTE MIPI PA
                                                          LTE FDD MIPI PA TX OFFO Set0 }, // PA Off
                                        LTE MIPI TRX OFF
  { /* 2 */ LTE MIPI ASM ,
                                       LTE MIPI TRX ON ALTE FDD MIPI ASM TX ONO SetO }, V/WIN on
  { /* 3 */ LTE MIPI NULL, { o
                                      , LTE MIPI EVENT NULL, o
LTE_MIPI_DATA_SUBBAND_TABLE_T LTE_Band1 MIPI_TX DATA_Set0[] =
                                                                                                         Data
                                                                    ,{ { subband-0 freq __,addr ,data }, { subband-1 freq
 // No.
          elm type
                   , port sel
                                   , data seq
                                               USID
                                           , LTE REG W
                                                                                ,{ { 19200 / *100 kHz*/
  { /* 0 */ LTE MIPI PA , LTE MIPI PORTÏ
                                                          , MIPI USID PA0 Set0
                                                                                                        .0x00 .0x0C}
  { /* 1 */ LTE_MIPI_PA , LTE_MIPI_PORT1
                                                         MIPI USID PA0 Set0
                                                                                  { 19200 / *100 kHz*/
                                            LTE_REG_W
                                                                                                        ,0x01 , 0x00}, ·
                                           LTE_REG_W
                                                                                  { 19200 /*100 kHz*/
        */ LTE MIPI PA , LTE MIPI PORT1
                                                          , MIPI USID PA0 Set0
                                                                                                        ,0x03 , 0x00},
                                            LTE_REG_W
                                                         , MIPI_USID_ASMU_set0 , { 19200 / *100 kHz*/
  { /* 3 */ LTE MIPI PA
                       , LTE MIPL PORTO
                                                                                                        ,0x04 , 0x10},
                                                          , MIPI_USID_PA0_Set0
                                                                                ,{ { 19200 /*100 kHz*/
  , LTE MIPI PORT1
                                            LTE REG W
                                                                                                        ,0x00 , 0x00},
  { /* 5 */ LTE MIPI PA , LTE MIPI PORTO
                                           LTE REG W
                                                         , MIPI USID ASM0 Set0 ,{ |{ 19200 /*100 kHz*/
                                                                                                        ,0x04 , 0x00},
```

, LTE REG W

, 0

/*MIPI ASM

};

{ /* 6 */ LTE MIPI ASM , LTE MIPI PORTO

{ /* 7 */ LTE_MIPI_NULL, 0

LTE TDD Band

❖ TX通路ON/OFF时所需的操作步骤:

Event No.	Event Type	Action	Data	Data No.
		,	设定PA寄存器0	0
		Fueble DA	设定PA寄存器1	1
	TV ON	Enable PA	设定PA寄存器2	2
0	TX ON		设定PA寄存器3	3
	TX OFF	打开TXM Coupler	设定TXM寄存器4	4
		DRX ASM Idle	设定DRX ASM Idle	5
1		关闭PA	设定PA寄存器0	6
1		关闭PA 3P4T	设定PA寄存器4	7
2	TX ON	打开ASM	将ASM TXM 切到TRX Port	8

Note: 和WCDMA一样, FDD-LTE在TX OFF的时候不能关闭ASM, 但是TDD-LTE在TX OFF的时候可以关闭ASM。目前设定都是TX不去关ASM, 都由RX去关ASM。



> LTE TDD

```
Timing在Ite_custom_mipi.h中定义
```

#define LTE TDD MIPI ASM TX ON1 Set0 US2OFFCNT(0)

US20FFCNT(15)

#define LTE TDD MIPI ASM TX ONO Set0

/*MIPI ASM */ /*TDD TX ON . */

/*MIPI PA

```
/*TDD TX ON */
                                                                  #define LTE_TDD_MIPI_PA_TX_ONO_Set0
                                                                                                         US2OFFCNT(25)
                                                                  #define LTE_TDD_MIPI_PA_TX_ON1_Set0
                                                                                                         US20FFCNT(0)
                                                                  /*MIPI PA
                                                                  / *TDD TX OFF */
                                                                  #define LTE_TDD_MIPI_PA_TX_OFF0_Set0 US2OFFCNT(20)
                                                                  #define LTE_TDD_MIPI_PA_TX_OFF1_Set0 US2OFFCNT(0)
LTE_MIPI_EVENT_TABLE_T LTE_Band40_MIPI_TX_EVENT_Set0[] =
                                                                                           Timing
 / * No.
          elm type
                     , data idx
                                  , evt_type
                                                 , evt offset
                   { start, stop },
                                             (us) Fyent
                                                        , LTE_TDD_MIPI_PA_TX_ON0_Set0 }, //PA On
 { /* 0 */ LTE_MIPI_PA , { 0
                                     LTE MIPI TRX ON
                                                        , LTE_TDD_MIPI_PA_TX_OFF0_Set0 }, //PA_Off
 { /* 1 */ LTE_MIPI_PA , { 6
                                    }, LTE MIPI TRX OFF
 { /* 2 */ LTE MIPI ASM | { 8
                                    } LTE MIPI TRX ON
                                                         , LTE_TDD_MIPI_ASM_TX_ON0_Set0 }, //TDD ASM at Tx on
  }, LTE MIPI EVENT NULL, 0
 LTE MIPI DATA SUBBAND TABLE T LTE Band40 MIPI TX DATA Set0[] =
                                                                                                       Data
                                                                     ,{ { subband-0 freq __,addr ,data }, { subband-1 freq
                                                  , USID
   //No.
            elm type
                    , port sel
                                     data seq
                                            LTE_REG_W
                                                                                ,{ { 23000 /*100 kHz*/ ,0x02 , 0x00},
   { /* 0 */ LTE MIPI PA , LTE MIPI PORT1
                                                          , MIPI USID PA0 Set0
                                            , LTE REG W
   { /* 1 */ LTE MIPI PA , LTE MIPI PORT1
                                                                                ,{ { 23000 / *100 kHz*/ ,0x00 , 0x44},
                                                          , MIPI USID PA0 Set0
                                                                                ,{ { 23000 /*100 kHz*/ ,0x01 , 0x00},
   { /* 2 */ LTE_MIPI_PA , LTE_MIPI_PORT1
                                            , LTE REG W
                                                          , MIPI USID PA0 Set0
                                                                                ,{ { 23000 /*100 kHz*/ ,0x03 , 0x00},
   { /* 3 */ LTE MIPI PA , LTE MIPI PORT1
                                            , LTE REG W
                                                          , MIPI USID PA0 Set0
   { /* 4 */ LTE_MIPI_PA , LTE_MIPI_PORTO
                                            , LTE REG W
                                                          , MIPI_USID_ASMU_Set0 ,{ { 23000 /*100 kHz*/ ,0x04 , 0x18},
   { /* 5 */ LTE_MIPI_PA , LTE_MIPI\PORT2
                                            LTE REG W
                                                          , MIPI_USID_ASM2_Set0 , { { 23000 / *100 kHz*/ ,0x00 , 0x00},
                                                          , MIPI_USID_PA0_Set0 |, { { 23000 / *100 kHz*/ ,0x00 , 0x00},
   { /* 6 */ LTE MIPI PA , LTE MIPI PORT1
                                             LTE REG W
                                                          , MIPI_USID_ASM0_Set0 ,{ { 23000 /*100 kHz*/ ,0x04 , 0x00},
   { /* 7 */ LTE MIPI PA , LTE MIPI PORTO
                                             LTE REG W
                                                           , MIPI_USID_ASM0_Set0 ,{ { 23000 /*100 kHz*/ ,0x03 , 0x40}
   { /* 8 */ LTE MIPI ASM , LTE MIPI PORTO
                                             , LTE REG W
                                               , LTE_REG_W
                                                             , MIPI_USID_ASM0_Set0 ,{ { 23000 / *100 kHz*/ ,0x03 , 0x0
   //{ /* 7 */ LTE MIPI ASM , LTE MIPI PORTO
   { /* 8 */ LTE_MIPI_NULL, 0
                                                                   ,{ { 0  /*100 kHz*/ ,0 ,0 }, { 0  /*100 kHz*/ ,0
                                                 , 0
```

LTE--TPC

```
LTE MIPI EVENT TABLE T LTE Band1 MIPI TPC EVENT Set0[] =
      / * No.
                            , data idx
                                           , evt type
                                                               evt offset
                elm type
                                                                                TPC的timing必须晚于PA ON!
                          { start, stop },
                                                        ( us/)
                                             LTE MIPI TPC SET US2OFFCNT(10)
                                                                                             Timing
      { /* 0 */ LTE MIPI PA , { 0 , 2
      { /* 1 */ LTE MIPI NULL, { 0 |
                                        . 0 }, LTE MIPI EVENT NULL, 0
LTE_MIPI_DATA_TABLE_T LTE_Band1_MIPI_TPC_DATA_Set0[] =
 //No. elm type , port_sel , data_seg , USID
 {/* 0 */ LTE_MIPI_PA_SEC, LTE_MIPI_PORT1 , LTE_REG_W , LTE_MIPI_PA_SECTION_USID
                                                                , LTE_MIPI_PA_SECTION_ADDRESS , LTE_MIPI_PA_SECTION_DATA0}
                                                                , LTE_MIPI_PA_SECTION_ADDRESS , LTE_MIPI_PA_SECTION_DATA1}
 {/* 1 */ LTE_MIPI_PA_SEC, LTE_MIPI_PORT1 , LTE_REG_W , LTE_MIPI_PA_SECTION_USID
 {/* 2 */ LTE MIPI PA SEC, LTE MIPI PORT1 , LTE REG W , LTE MIPI PA SECTION USID
                                                                , LTE MIPI PA SECTION ADDRESS , LTE MIPI PA SECTION DATA2}
 {/* 3 */ LTE MIPI NULL , 0
        LTE_MIPI_TPC_SECTION_TABLE_T LTE_Band1_MIPI_PA_SECTION_DATA_Set0[] =
           19200, / *100kHz*/
           MIPI_USID_PA0_Set0, / *USID*/
             // PAEn=1
             // PA_SEC_DATA0, PA_SEC_DATA1, PA_SEC_DATA2, PA_SEC_DATA3, PA_SEC_DATA4
             // {addr, data}, {addr, data}, {addr, data}, {addr, data}, {addr, data}
             {{ { 0x1 , 0x15}, { 0x3 , 0x86} ,{ 0x0 , 0x1C} , { 0x0 , 0x0} , { 0x0 , 0x0}}},
             共9个档位、功
             {{ { 0x1 , 0x37}, { 0x3 , 0x86} ,{ 0x0 , 0x1C} , { 0x0 , 0x0} , { 0x0 , 0x0}}},
                                                                                    率从低到高,
              {{ { 0x1 , 0x87}, { 0x3 , 0x86} , { 0x0 , 0x1C} , { 0x0 , 0x0} , { 0x0 , 0x0}}},
                                                                                    最后一档设为
             \{\{\{0x1,0x99\},\{0x3,0x86\},\{0x0,0x1C\},\{0x0,0x0\},\{0x0,0x0\}\}\},
                                                                                    PA OFF
             [{ { 0x1 , 0x9B}, { 0x3 , 0x8B} ,{ 0x0 , 0x1C} , { 0x0 , 0x0} , { 0x0 , 0x0}}},
             \{\{\{0x1,0x9B\},\{0x3,0x8B\},\{0x0,0x1C\},\{0x0,0x0\},\{0x0,0x0\}\}\},
             [{ { 0x1 , 0x00}, { 0x3 , 0x00} , { 0x0 , 0x00} , { 0x0 , 0x0} , { 0x0 , 0x0}}},//SRS
```

► lte_custom_rf.h LTE B28 TRX Port BPI SET

#define BAND INDICATOR12 Set0 LTE Band28

#define BAND_INDICATOR12_SUPPORT_Set0 SW_CAPABILITY_SUPPORT

#define LTE_Band28_RX_IO_SEL_Set0 RX_IO_PRX

#define LTE Band28 RXD IO SEL Set0 RX IO DRX5

#define PDATA_LTE_Band28_PR1_Set0 0x00000000

#define PDATA_LTE_Band28_PR2_Set0 0x00000000

#define PDATA_LTE_Band28_PR3_Set0 LTE_PDATA_OFF

#define LTE_Band28_RX_eLNAIDX_Set0 MML1_FE_ELNA_NONE

#define LTE_Band28_RXD_eLNAIDX_Set0 MML1_FE_ELNA_NONE

#define LTE_Band28_TX_IO_SEL_Set0 TX_IO_LB1

#define PDATA_LTE_Band28_PT1_Set0 0x000000000

#define PDATA_LTE_Band28_PT2_Set0 0x000000000

#define PDATA_LTE_Band28_PT3_Set0 LTE_PDATA_OFF

/* Definition for the band splitting */

> lte_custom_rf.h LTE 28B TRX PORT BPI SET

```
// How to set the band-splitting frequency?
// For example, the DL frequencies of the 1st and 2nd sub-bands are 758~780.4MHz and 780.5~802.9MHz, so we défine
// BAND_SPLIT_INDICATOR1_DL_END1 as 7805 [ = (780.4+0.1)*10 ]
// BAND SPLIT INDICATOR1 DL END2 as 8030 [ = (802.9+0.1)*10 ]
// 1. The unit for the frequency definition is 100kHz
// 2. BAND_SPLIT_INDICATOR1_DL_ENDn defines the end DL frequency of each part of splitting band PLUS 0.1 MHz
// 3. Since there are only TWO sub-bands, BAND_SPLIT_INDICATOR1_DL_END3 should be 0.
// 4. The way to define the UL frequency is the same as the way DL does
// [Example]
// BAND_SPLIT_INDICATORO
                                    LTE Band28
// BAND_SPLIT_INDICATOR0_NUM
                                      2 // the num of part of splitting band
// BAND SPLIT INDICATORO Part1 DL END 7805 // the end DL frequency of the 1st part of splitting band PLUS 0.1MHz, unit: 100KHz, set to 0 if no part is split
// BAND_SPLIT_INDICATOR0_Part2_DL_END 8030 // the end DL frequency of the 2nd part of splitting band PLUS 0.1MHz, unit: 100KHz, set to 0 if no part is split
// BAND_SPLIT_INDICATOR0_Part3_DL_END 0 // the end DL frequency of the 3rd part of splitting band PLUS 0.1MHz, unit: 100KHz, set to 0 if no part is split or only two parts are split
// BAND_SPLIT_INDICATOR0_Part1_UL_END 7255 // the end UL frequency of the 1st part of splitting band PLUS 0.1MHz, unit: 100KHz, set to 0 if no part is split
// BAND_SPLIT_INDICATOR0_Part2_UL_END 7480 // the end UL frequency of the 2nd part of splitting band PLUS 0.1MHz, unit: 100KHz, set to 0 if no part is split
/ BAND SPLIT INDICATORO Part3 UL END 0 // the end UL frequency of the 3rd part of splitting band PLUS 0.1MHz, unit: 100KHz, set to 0 if no part is split or only two parts are split
                                                                                    * LTE_Band28- Part1 Split Band Settings */
                                                                                   #define LTE_Band28_Part1_RX_TBL_IDX_Set0
                                                                                                                                       TBL_IDX12
  0th Split Band Settings */
                                                                                   #define LTE_Band28_Part1_TX_TBL_IDX_Set0
                                                                                                                                       TBL IDX12
                                                      LTE_Band28
                                                                                    * LTE_Band28- Part2 Split Band Settings */
#define BAND_SPLIT_INDICATORO_Set0
#define BAND SPLIT INDICATORO NUM Set0
                                                                                   #define LTE_Band28_Part2_RX_TBL_IDX_Set0
                                                                                                                                       TBL_IDX25
#define BAND_SPLIT_INDICATORO_Part1_DL_END_Set0
                                                              7805
                                                                                   #define LTE_Band28_Part2_TX_TBL_IDX_Set0
                                                                                                                                       TBL IDX28
#define BAND_SPLIT_INDICATORO_Part2_DL_END_Set0
                                                              8030
                                                                                   #define LTE_Band28_Part2_RX_IO_SEL_Set0
                                                                                                                                       RX_IO_PRX5
#define BAND_SPLIT_INDICATORO_Part3_DL_END_Set0
                                                                                   #define LTE_Band28_Part2_RXD_IO_SEL_Set0
                                                                                                                                       RX_IO_DRX5
#define BAND_SPLIT_INDICATORO_Part1_UL_END_Set0
                                                                                   #define LTE_Band28_Part2_TX_IO_SEL_Set0
                                                                                                                                       TX_IO_LB1
#define BAND SPLIT INDICATORO Part2 UL END Set0
                                                              7480
                                                                                   #define PDATA_LTE_Band28_Part2_PR1_Set0
                                                                                                                                        0x00000002
#define BAND_SPLIT_INDICATORO_Part3_UL_END_Set0
                                                                                   #define PDATA_LTE_Band28_Part2_PR2_Set0
                                                                                                                                        0x00000002
                                                                                   #define PDATA LTE Band28 Part2 PR3 Set0
                                                                                                                                        LTE_PDATA_OFF
                                                                                   #define PDATA_LTE_Band28_Part2_PT1_Set0
                                                                                                                                        0x00000000
                                                                                   #define PDATA_LTE_Band28_Part2_PT2_Set0
                                                                                                                                        0x00000000
                                                                                   #define PDATA_LTE_Band28_Part2_PT3_Set0
                                                                                                                                        LTE_PDATA_OFF
                                                                                   #define PDATA_LTE_Band28_Part2_VM0_Set0
                                                                                                                                        {0,0,0,0,0,0,0,0,0}
                                                                                   #define PDATA_LTE_Band28_Part2_VM1_Set0
                                                                                                                                        {0,0,0,0,0,0,0,0,0}
                                                                                        -----*/
                                                                                   /* LTE_Band28- Part3 Split Band Settings */
                                                                                   /*----*/
                                                                                   #define LTE Band28 Part3 RX TBL IDX Set0
                                                                                                                                       TBL IDX INVALID
                                                                                   #define LTE_Band28_Part3_TX_TBL_IDX_Set0
                                                                                                                                       TBL_IDX_INVALID
                                                                                   #define LTE_Band28_Part3_RX_IO_SEL_Set0
                                                                                                                                       RX_IO_NON_USED
                                                                                   #define LTE_Band28_Part3_RXD_IO_SEL_Set0
                                                                                                                                        RXD_IO_NON_USED
                                                                                   #define LTE Band28 Part3 TX IO SEL Set0
                                                                                                                                       TX IO NON USED
                                                                                   #define PDATA_LTE_Band28_Part3_PR1_Set0
                                                                                                                                       0x00000000
                                                                                   #define PDATA LTE Band28 Part3 PR2 Set0
                                                                                                                                        0x00000000
                                                                                   #define PDATA_LTE_Band28_Part3_PR3_Set0
                                                                                                                                        LTE_PDATA_OFF
                                                                                   #define PDATA LTE Band28 Part3 PT1 Set0
                                                                                                                                        0x00000000
          MEDIATEK
                            CONFIDENTIAL B
                                                                                   #define PDATA_LTE_Band28_Part3_PT2_Set0
                                                                                                                                        0x00000000
                                                                                   #define PDATA_LTE_Band28_Part3_PT3_Set0
                                                                                                                                        LTE_PDATA_OFF
                                                                                   #define PDATA_LTE_Band28_Part3_VM0_Set0
                                                                                                                                        {0,0,0,0,0,0,0,0,0}
                                                                                   #define PDATA_LTE_Band28_Part3_VM1_Set0
                                                                                                                                        {0,0,0,0,0,0,0,0,0}
```

> lte_custom_mipi.c

```
LTE MIPI EVENT TABLE T LTE Band28 MIPI RX EVENT Set0[] =
       / * No.
                  elm type
                                                                   evt offset
                               , data idx
                                               , evt_type
                            { start, stop },
                                                            ( us )
       { /* 0 */ LTE_MIPI_ASM , { 0 , 1 }, LTE_MIPI_TRX_ON , LTE_FDD_MIPI_ASM_RX_ONO_Set0 },
       { /* 1 */ LTE_MIPI_ASM , { 2
                                               }, LTE_MIPI_TRX_OFF , LTE_FDD_MIPI_ASM_RX_OFF0_Set0},
                                          , 3
        { /* 2 */ LTE MIPI NULL, { 0
                                                }, LTE MIPI EVENT NULL, 0
     LTE_MIPI_DATA_SUBBAND_TABLE_T LTE_Band28_MIPI_RX_DATA_Set0[] =
                                                                                  ,{ { subband-0
      //No.
                 elm type , port sel
                                            , data seq
                                                           , USID
       { /* 0 */ LTE_MIPI_ASM , LTE_MIPI_PORT0
                                                     , LTE_REG_W
                                                                       MIPI_USID_ASM0_Set0
       { /* 1 */ LTE_MIPI_ASM , LTE_MIPI_PORT2
                                                     , LTE_REG_W
                                                                      , MIPI_USID_ASM1_Set0
       { /* 2 */ LTE_MIPI_ASM , LTE_MIPI_PORTO
                                                     , LTE_REG_W
                                                                       MIPI_USID_ASM0_Set0
       { /* 3 */ LTE_MIPI_ASM , LTE_MIPI_PORT2
                                                     , LTE_REG_W
                                                                       MIPI USID ASM1 Set0
       { /* 4 */ LTE_MIPI_NULL, 0
                                                                                      0 /*100 kH
                                                          , 0
                               28A
                                                                                                     28B
freq _,addr ,data }, { subband-1 freq _,addr ,data }, { subband-2 freq
                                                               addr ,data } { subband-3 freq addr ,data }, { subband-4 freq addr ,data },
   7580 /*100 kHz*/ ,0x02 ,0x05 }, { 7692 /*100 kHz*/ ,0x02 ,0x05 }, { 7692 /*100 kHz*/ ,0x02 ,0x05 }, { 7805 /*100 kHz*/ ,0x02 ,0x04 }, { 7917 /*100 kHz*/ ,0x02 ,0x04 }, { 8030 /*100 kHz*/ ,0x02 ,0x04 }, }
   7580 /*100 kHz*/ ,0x01 ,0x06 }, { 7692 /*100 kHz*/ ,0x01 ,0x06 }, { 7692 /*100 kHz*/ ,0x01 ,0x06 }, { 7805 /*100 kHz*/ ,0x01 ,0x05 }, { 7917 /*100 kHz*/ ,0x01 ,0x05 }, { 8030 /*100 kHz*/ ,0x01 ,0x05 }, }
   7580 /*100 kHz*/,0x02,0x00 }, { 7692 /*100 kHz*/,0x02,0x00 }, { 7692 /*100 kHz*/,0x02,0x00 }, { 7805 /*100 kHz*/,0x02,0x00 }, { 7917 /*100 kHz*/,0x02,0x00 }, { 8030 /*100 kHz*/,0x02,0x00 }, }
   7580 /*100 kHz*/ ,0x01 ,0x00 }, { 7692 /*100 kHz*/ ,0x01 ,0x00 }) {\ 7805 /*100 kHz*/ ,0x01 ,0x00 }, { 7917 /*100 kHz*/ ,0x01 ,0x00 }, { 8030 /*100 kHz*/ ,0x01 ,0x00 }, \
                                                                 }, { 0/*100 kHz*/,0 ,0 }, { 0/*100 kHz*/,0 ,0 },} },
z*/,0 ,0 }, { 0/*100 kHz*/,0 ,0 }, { 0/*100 kHz*/,0 ,0
```

> lte_custom_mipi.c

```
LTE MIPI_EVENT_TABLE_T LTE_Band28 MIPI_TX_EVENT_Set0[] =
 /* No.
          elm type
                    , data idx
                                 , evt type
                                                  evt offset
                  { start, stop },
                                            ( us )
                                   }, LTE_MIPI_TRX_ON , LTE_FDD_MIPI_PA_TX_ONO_Set0 }, //PA On
 { /* 1 */ LTE_MIPI_PA , { 4 , 5
                                  }, LTE MIPI TRX OFF , LTE FDD MIPI PA TX OFF0 Set0 }, //PA OFF
 { /* 2 */ LTE MIPI ASM , { 6
                             , 6 }, LTE_MIPI_TRX_ON , LTE_FDD_MIPI_ASM_TX_ON0_Set0 }, //WIN on
 { /* 4 */ LTE MIPI NULL, { 0
                                  }, LTE_MIPI_EVENT_NULL, 0
   LTE_MIPI_DATA_SUBBAND_TABLE_T LTE_Band28_MIPI_TX_DATA_Set0[] =
              elm type
                      , port sel
                                       , data_seq
                                                    , USID
                                                                        .{ { subband-
     { /* 0 */ LTE MIPI PA , LTE MIPI PORT1
                                             , LTE REG W
                                                              MIPI USID PA1 Set0
     { /* 1 */ LTE MIPI PA , LTE MIPI PORT1
                                             , LTE REG W
                                                             . MIPI USID_PA1_Set0
     { /* 2 */ LTE MIPI PA , LTE MIPI PORT1
                                              , LTE REG W
                                                             MIPI USID PA1 Set0
                                                             MIPI USID_ASMO_Set0
     { /* 3 */ LTE MIPI PA , LTE MIPI PORTO
                                              , LTE REG W
     { /* 4 */ LTE MIPI PA , LTE MIPI PORT1
                                              , LTE REG W
                                                             , MIPI USID PA1 Set0
     { /* 5 */ LTE MIPI PA , LTE MIPI PORTO
                                              , LTE REG W
                                                             , MIPI USID ASMO SetO ,
     { /* 6 */ LTE MIPI ASM , LTE MIPI PORTO
                                                            , MIPI USID ASM0 Set0
                                               , LTE REG W
     { /* 7 */ LTE MIPI NULL, 0
                                                                           0 /*100 |
```

28A

```
28B
I- 0 freq _,addr ,data }, { subband-1 freq _,addr ,data }, { subband-2 freq
                                                                               addr ,data }, { subband-3 freq ,addr ,data }, { subband-4 freq ,addr ,data },
                                                                               7255 /*100 kHz*/ ,0x00 , 0x05 }, { 7367 /*100 kHz*/ ,0x00 , 0x05 }, { 7480 /*100 kHz*/ ,0x00 , 0x05
     7030 /*100 kHz*/ ,0x00 , 0x05 }, { 7142 /*100 kHz*/ ,0x00 , 0x05 }
     7030 /*100 kHz*/ ,0x01 , 0x00 }, { 7142 /*100 kHz*/ ,0x01 ,, 0x00 }
                                                                               7255/*100 kHz*/,0x01,0x00},{ 7367/*100 kHz*/,0x01,0x00},{ 7480/*100 kHz*/,0x01,0x00
                                                                               7255 /*100 kHz*/ ,0x03 , 0x00 }, { 7367 /*100 kHz*/ ,0x03 , 0x00 }, { 7480 /*100 kHz*/ ,0x03 , 0x00 }, } , 7255 /*100 kHz*/ ,0x04 , 0x08 }, { 7367 /*100 kHz*/ ,0x04 , 0x08 }, { 7480 /*100 kHz*/ ,0x04 , 0x08 }, } ,
     7030 /*100 kHz*/ ,0x03 , 0x00 }, { 7142 /*100 kHz*/ ,0x03 , 0x00 },
     7030 /*100 kHz*/ ,0x04 , 0x08 }, { 7142 /*100 kHz*/ ,0x04 , 0x08
    7030 /*100 kHz*/ ,0x00 , 0x00 }, { 7142 /*100 kHz*/ ,0x00 , 0x00 }
                                                                               7255 /*100 kHz*/ ,0x00 , 0x00 }, { 7367 /*100 kHz*/ ,0x00 , 0x00 }, { 7480 /*100 kHz*/ ,0x00 , 0x00 },} },
     7030 /*100 kHz*/ ,0x04 , 0x00 }, { 7142 /*100 kHz*/ ,0x04 , 0x00 },
                                                                               7255 /*100 kHz*/ ,0x04 , 0x00 }, { 7367 /*100 kHz*/ ,0x04 , 0x00 }, { 7480 /*100 kHz*/ ,0x04 , 0x00
     7030 /*100 kHz*/ ,0x02 , 0x05 }, { 7142 /*100 kHz*/ ,0x02 , 0x05 }
                                                                              .0x02 , 0x02 , 0x04 }, { 7367 /*100 kHz*/ ,0x02 ,0x04 }, { 7480 /*100 kHz*/ ,0x02 ,0x04 }, { 7480 /*100 kHz*/
                                          ,0 }, { 0 /*100 kHz*/,0 ,0 }, { 0 /*100 kHz*/,0 ,0 }, { 0 /*100 kHz*/,0 ,0 }, }
 kHz*/ ,0 ,0 }, { 0 /*100 kHz*/ ,0
```

Note: LTE B28 其他配置(如CA,Ant Tuner, TAS等参照相关文档; TRX PORT, BPI 等均在Excel List 配置完毕,由Parsing tool Gen 出Code,做编译



LTE--Tx Bypass No Support

▶ Tool_Gen93_MT6763_LTE_MT6177L.xlsm 不能配置LTE_Band_filter Bandindicator 及相关设置

Band Filter setting	最新的Excel	会变为不可选择			
Band_Filter_Indicator_ID	(LTE_BAND)	CCA_Support(TX)	Filter_TX_IO_SEL	Filter_PT1	Filter_PT2
BAND_FILTER_INDICATOR0	LTE_BandNone	NO_CCA_SUPPORT	TX_IO_NON_USED	0x00000000	0x00000000
BAND_FILTER_INDICATOR1	LTE_BandNone	NO_CCA_SUPPORT	TX_IO_NON_USED	0x00000000	0x00000000
BAND_FILTER_INDICATOR2	LTE_BandNone	NO_CCA_SUPPORT	TX_IO_NON_USED	0x00000000	0x00000000
BAND_FILTER_INDICATOR3	LTE_BandNone	NO_CCA_SUPPORT			
BAND_FILTER_INDICATOR4	LTE_BandNone	NO_CCA_SUPPORT	Y		

▶ lte_custom_mipi.c CW Table 配置与非Filter Table 即可, Filter Table 不用配置

```
LTE_MIPI_EVENT_TABLE_T LTE_Band38/40/41_MIPI_FILTER_TX_EVENT_Default/Set*[] =

LTE_MIPI_DATA_SUBBAND_TABLE_T LTE_Band38/40/41_MIPI_FILTER_TX_DATA_Default/Set*[] =

LTE_MIPI_EVENT_TABLE_T LTE_Band38/40/41_MIPI_FILTER_TPC_EVENT_Default/Set0[] =

LTE_MIPI_TPC_SECTION_TABLE_T LTE_Band38/40/41_MIPI_FILTER_PA_SECTION_DATA_Default/Set*[] =
```





C2K Part



- ▶ 下面列举了93 modem在9个工作场景下,需要对哪些RF前端器件进行设置。
 - 1) Y: 表示需要设置 N: 表示不需要设置
 - 2) TX Gate On/OFF 被Tx ON/OFF 替代
 - 3) TX ON/TX Gate On Event 配置PA Enable,禁止配置PA Bias
 - 4) TX On Timing 由20us调整10us

SCENARIOS	ASM	ASM TUNER	DASM	DASM TUNER	PA Enable	Bias For PA
RX ON	Υ	Υ	N	N	N	N
RX OFF	Υ	Υ	N	N	N	N
RXD ON	N	N	Y	Y	N	N
RX OFF	N	N	Y	Υ	N	N
TX ON	Υ	Y	N	N	Y	N
TX OFF	N	N	N	N	Y	N
TX GATE ON	N	N	N	N	Υ	N
TX GATE OFF	N	N	N	N	Υ	N
TX TPC	N	N	N	N	N	Υ

C2K--RX

列出C2K RX通路ON/OFF时所需的操作步骤

Event No.	Event Type	Action	Data	Data No.
		设置ASM Tx Off	寄存器0x00, Tx off	0
_	DV ON	设置ASM M TRX Port Off	寄存器0x05, off	1
0	RX ON	设置ASM H TRX Port Off	寄存器0x03, off	2
		设置ASM L TRX Port on	寄存器0x02, on	3
1	RX OFF	寄存器0x02, on	寄存器0x02, off	4
2	DV ON	设置DP12T M Port Isolation	寄存器0x00, Isolation	5
3	RX ON	设置DP12T L Port active	寄存器0x01, Active	6
4	RX OFF	设置DP12T M idle	寄存器0x00, Idle	7
		设置DP12T L idle	寄存器0x01, Idle	8

Note: C2K BC0

TXM:Sky77928-11 MMMB PA:Sky77651-11

DRX Switch:sky13552-669



C2K--RX

> RX部分的设置格式:

```
Timing在c2k_custom_mipi.h中定义
```

```
*MIPLASM */
* RX ON */
#define C2K MIPI ASM RX ONO Set0
                                         M_US(10)
#define C2K MIPI ASM RX ON1 Set0
                                         M_US(0)
* RX OFF */
#define C2K_MIPI_ASM_RX_OFF0_Set0
                                          M_US(5)
#define C2K MIPI ASM RX OFF1 Set0
                                          M_US(0)
*MIPI ASM
* DRX ON
#define C2K MIPI ASM DRX ONO Set0
                                          M US(11)
#define C2K MIPI ASM DRX ON1 Set0
                                          M_US(0)
/*MIPI ASM
/* DRX OFF
#define C2K MIPI ASM DRX OFFO Set0
                                          M US(6)
#define C2K MIPI ASM DRX OFF1 Set0
                                          M_US(0)
```

```
/* Rx Events */
C2K MIPI EVENT TABLE T C2K BAND A MIPI RX EVENT Seto[] =
                                                                                   Timing
  / * No.
                                              evt_offset
           elm type , data idx
                                , evt type
                 { start, stop },
                                         us 1
         */ C2K MIPI ASM
                                                              C2K MIPI ASM RX ONO Set0 },
         */ C2K MIPI ASM /
                                                              C2K MIPI ASM RX OFF0 Set0).
                                 4
                                        C2K MIPI TRX OFF
         */ C2K MIPI ASM ,
                                , 6
                                       C2K MIPI RX DIV ON
                                                              C2K MIPI ASM DRX ON0 Set0}
         */ C2K_MIPI ASM .
                                       C2K MIPI RX DIV OFF
                                                              C2K MIPI ASM DRX OFF0 Set0
            C2K MIPI NULL, { 0
                                       C2K MIPI EVENT NULL, 0},
```

```
/* Rx Data */
                                                                                                        Data
C2K MIPI DATA SUBBAND TABLE T C2K BAND A MIPI RX DATA Set0[] =
                     , port sel
                                   , data seg
                                                 USID
                                                              ,{ { subband-0 freq
 //No.
          elm type
                                                                                 ,add<del>r ,data }, { subband-1 freq __,addr ,da</del>t
                                              C2K REG W
                                                            MIPI USID ASM0 Set0 ,{|{ 8600 /*100 kHz*/ , {0x00 ,0x80}}
 { /* 0 */ C2K MIPI ASM , C2K MIPI PORTO
 { /* 1 */ C2K MIPI ASM , C2K MIPI PORTO
                                              C2K REG W
                                                             MIPI USID ASM0 Set0
                                                                                   ,{|{ 8600 /*100 kHz*/ , {0x05 ,0x00}}
 { /* 2 */ C2K MIPI_ASM , C2K_MIPI_PORTO
                                             C2K REG W
                                                             MIRI USID ASM0 Set0
                                                                                      { 8600 /*100 kHz*/ , {0x03 ,0x00}
 { /* 3 */ C2K MIPI ASM , C2K MIPI PÒŔTÓ
                                              C2K REG W
                                                            , MIPI USID ASM0 Set0
                                                                                      { 8600 /*100 kHz*/ , {0x02 ,0x06}
                                                            , MIPI_USID_ASMO Set0 ✓
 { /* 4 */ C2K MIPI ASM , C2K MIPI PORTO
                                             C2K REG W
                                                                                       8600 /*100 kHz*/ , {0x02 ,0x00}
 { /* 5 */ C2K MIPI ASM , C2K MIPI PORT2
                                             C2K REG W
                                                            , MIPI USID ASM1 Set0
                                                                                      { 8600 /*100 kHz*/ , {0x00 ,0x1F}
 { /* 6 */ C2K MIPI ASM , C2K MIPI PORT2
                                                                                      { 8600 /*100 kHz*/ , {0x01 ,0x03}
                                              C2K REG W
                                                            , MIPI USID ASM1 Set0
 { /* 7 */ C2K MIPI ASM , C2K MIPI PORT2
                                              C2K REG W
                                                            , MIPI USID ASM1 Set0
                                                                                   ,{|{ 8600 /*100 kHz*/ , {0x00 ,0x00}}
 { /* 8 */ C2K MIPI ASM , C2K MIPI PORT2
                                                                                   ,{|{ 8600 /*100 kHz*/ , {0x01 ,0x00}}
                                            , C2K REG W
                                                            , MIPI USID ASM1 Set0
 { /* 12 */ C2K MIPI NULL 0
                                                                 /*100 kHz*/ , {0
                                                                                                  /*100 kHz*/ , {0 ,0
```

C2K--TX

> 列出TX通路ON/OFF时所需的操作步骤:

		i		
Event No.	Event Type	Action	Data	Data No.
0	0 TX ON	Enable PA	将PA设成active mode	0
U		Enable PA	设定PA寄存器2	1
1	TX OFF	Dis-enable PA	设定PA寄存器0	2
3	TX Gate On	Enable PA	将PA设成active mode	3
3	TX Gate OFF	Dis-enable PA	将PA设成standby mode	4
4	TX ASM ON	ASM Active	切换到正确的ASM TRX Port	5-7

Note:

- 93 modem Tx On Event 不能关闭ASM
- 93 modem Tx On 不能设置PA Bias 寄存器 (清零也不行)
- 93 Modem Tx On/Gate On,同时配置Pa Enable
- 93 modem Tx OFF/Gatet OFF 关闭PA



C2K--TX

Timing在C2K_custom_mipi.h中定义

>TX部分的设置格式:

```
/* TX Event */
C2K_MIPI_EVENT_TABLE_T C2K_BAND_A MIPI_TX_EVENT_Set0[]
                                                                                     Timing
                                               Event
 / * No.
                                             evt offset
                   , data idx
                               , evt type
          elm type
                 { start, stop }
                                       ( us )
 { /* 0 */ C2K_MIPI_PA ,
                                                            C2K MIPI PA TX ONO SetO }.
                                     C2K_MIPI_TRX_ON
 { /* 1 */ C2K_MIPI_PA ,
                                     C2K_MIPI_TRX_OFF
                                                            C2K_MIPI_PA_TX_OFF0_Set0 },
                                     C2K_MIPI_TX_GATE_ON
  C2K MIPI PA TX GATE ONO SetO },
                                                            C2K MIPI PA TX GATE OFF0 Set0 },
 { /* 3 */ C2K MIPI PA
                                     C2K MIPI TX GATE OFF
                                                            C2K MIPI ASM TX ON0 Set0 }.
  { /* 4 */ C2K MIPI ASM .
                                     C2K MIPI TRX ON
                                     C2K MIPI EVENT NULL,
  { /* 6 */ C2K MIPI NULL,
```

```
/* TX Data */
                                                                                                         Data
C2K_MIPI_DATA_SUBBAND_TABLE_T C2K_BAND_A_MIPI_TX_DATA_Set0[] =
                                                           ,{ { subband-0 freq
                                                                              addr.data }. { subband-1 freq .addr.da
 //No.
          elm type
                    , port sel
                                  , data seg
                                               USID
  { /* 0 */ C2K_MIPI_PA
                       , C2K_MIPI_PORT1
                                            C2K_REG_W
                                                         , MIPI_USID_PA1_Set0
                                                                                   8150 /*100 kHz*/, {0x00,0x94}},
  { /* 1 */ C2K MIPI PA
                                                                                  8150 /*100 kHz*/ , {0x02 ,0x00} },
                        , C2K MIPI PORT1
                                           C2K REG W
                                                         , MIPI USID PA1 Set0
                                                                                  8150 /*100 kHz*/, {0x00,0x00} },
                        , C2K_MIPI_PORT1
        */ C2K_MIPI_PA
                                            C2K REG W
                                                         MIPI USID PA1 Set0
  { /* 3 */ C2K MIPI PA
                                                         , MIPI USID PA1 Set0
                                                                                   8150 /*100 kHz*/ , {0x00 ,0x94} },
                         C2K MIPI PORT1
                                           C2K REG W
                                                                                  8150 /*100 kHz*/, {0x00,0x90} },
        */ C2K MIPI PA
                         C2K MIPI PORT1
                                           , C2K REG W
                                                         , MIPI USID PA1 Set0
  { /* 5 */ C2K_MIPI_ASM , C2K_MIPI_PORTO
                                          , C2K REG W
                                                         , MIPI USID ASM0 Set0
                                                                                  8150 /*100 kHz*/, {0x00,0x80} },
                                                                                  8150 /*100 kHz*/, {0x02,0x06} },
  { /* 6 */ C2K MIPI ASM, C2K MIPI PORTO
                                          , C2K REG W
                                                         , MIPI USID ASM0 Set0
  , C2K REG W
                                                         , MIPI USID ASM0 Set0
                                                                               { { 8150 /*100 kHz*/ , {0x04 ,0x0B} },
  { /* 8 */ C2K MIPI NULL, 0.
                                                             0 /*100 kHz*/ , {0
                                                                               ,<del>0 }},{ 0/*100kHz*/,{0,0</del>
```

MEDIATEK

C2K--TPC

```
/* TPC Event */
C2K MIPI EVENT TABLE T C2K BAND A MIPI TPC EVENT Set0[] =
  / * No.
            elm type , data idx , evt_type
                                                       , evt offset
                                                  ( us )
                      { start, stop },
                                 { 0 , 2 }, C2K_MIPI_TPC_SET , 5
  { /* 0 */ C2K MIPI PA ,
                                                                                    TCP Timing
  { /* 1 */ C2K MIPI NULL, { 0
                                           }, C2K MIPI EVENT NULL, 0
C2K_MIPI_TPC_SECTION_TABLE_T C2K_BAND_A_MIPI_PA_SECTION_DATA_1XRTT_Set0[C2K_MIPI_SUBBAND_NUM] =
    8150, / *100kHz*/
    MIPI_USID_PA1_Set0, / *USID*/
     // PAEn=1
     // PA_SEC_DATA0, PA_SEC_DATA1, PA_SEC_DATA2, PA_SEC_DATA3, PA_SEC_DATA4
     // {addr, data}, {addr, data}, {addr, data}, {addr, data}, {addr, data}
      /* 0 */ {{{ 0x1, 0x24}, { 0x2, 0x00}, { 0x3, 0x80}, { 0x0, 0x0 }, { 0x0, 0x0 }}},
      /*1*/\{\{\{0x1,0x35\},\{0x2,0x00\},\{0x3,0x80\},\{0x0,0x0\},\{0x0,0x0\}\}\}\}
      /*2*/\{\{\{0x1,0x35\},\{0x2,0x00\},\{0x3,0x80\},\{0x0,0x0\},\{0x0,0x0\}\}\},
                                                                              共8个档位,功
      /* 3 */ {{{ 0x1, 0x65}, { 0x2, 0x00}, { 0x3, 0x80}, { 0x0, 0x0 }, { 0x0, 0x0 }}},
                                                                              率从低到高,
      /* 4 */ \{\{\{0x1, 0x65\}, \{0x2, 0x00\}, \{0x3, 0x80\}, \{0x0, 0x0\}, \{0x0, 0x0\}\}\}\},
      /*5*/\{\{\{0x1,0x85\},\{0x2,0x00\},\{0x3,0x88\},\{0x0,0x0\},\{0x0,0x0\}\}\}\},
      /* 6 */ {{{ 0x1, 0x86}, { 0x2, 0x00}, { 0x3, 0x88}, { 0x0, 0x0 }, { 0x0, 0x0 }}},
      /* 7 */ {{{ 0x1, 0x98}, { 0x2, 0x00}, { 0x3, 0x88}, { 0x0, 0x0 }, { 0x0, 0x0 }}},
       Note:
        1)TPC Bias timing比TX_ON 开的早一些,但是这里TPC Timing 5us 是失效的,实际取决与HW
         响应时间, 大约10uS, 稍早于SW TX ON 10uS
        2)TPC 不能设置PA Enable
```

C2K--TPC

```
/* TPC Event */
C2K_MIPI_EVENT_TABLE_T C2K_BAND_A_MIPI_TPC_EVENT Set0[] =
 /* No. elm type
                        , data idx , evt_type
                                                       , evt_offset
 }, TCP Timing
                                           }, C2K MIPI EVENT NULL, 0
/*** EVDO TPC Sections ***/
C2K_MIPI_TPC_SECTION_TABLE_T C2K_BAND_A_MIPI_PA_SECTION_DATA_EVDO_Set0[C2K_MIPI_SUBBAND_NUM] =
   8150, /*100kHz*/
   MIPI_USID_PA1_Set0, / *USID*/
    // PAEn=1
    // PA_SEC_DATA0, PA_SEC_DATA1, PA_SEC_DATA2, PA_SEC_DATA3, PA_SEC_DATA4
    // {addr, data}, {addr, data}, {addr, data}, {addr, data}, {addr, data}
     /* 0 */ {{{ 0x1, 0x24}, { 0x2, 0x00}, { 0x3, 0x80}, { 0x0, 0x0 }, { 0x0, 0x0 }},
     /* 1 */ {{{ 0x1, 0x35}, { 0x2, 0x00}, { 0x3, 0x80}} { 0x0, 0x0 }, { 0x0, 0x0 }}},
                                                                        共8个档位,功
     /*2*/\{\{\{0x1,0x35\},\{0x2,0x00\},\{0x3,0x80\},\{0x0,0x0\},\{0x0,0x0\}\}\},
     /* 3 */ {{{ 0x1, 0x65}, { 0x2, 0x00}, { 0x3, 0x80}} { 0x0, 0x0 }, { 0x0, 0x0 }},
                                                                        率从低到高,
    /* 4 */ \{\{\{0x1, 0x65\}, \{0x2, 0x00\}, \{0x3, 0x80\}, \{0x0, 0x0\}, \{0x0, 0x0\}\}\},\
    /*5*/{{{ 0x1, 0x85}, { 0x2, 0x00}, { 0x3, 0x80}, { 0x0, 0x0 }, { 0x0, 0x0 }}},
     /* 6 */ {{{ 0x1, 0x87}, { 0x2, 0x00}, { 0x3, 0x86}, { 0x0, 0x0 }, { 0x0, 0x0 }}},
     /*7*/\{\{\{0x1,0xB7\},\{0x2,0x00\},\{0x3,0x86\},\{0x0,0x0\},\{0x0,0x0\}\}\},
     Note:
      1)TPC Bias timing比TX_ON 开的早一些,但是这里TPC Timing 5us 是失效的,实际取决与HW
       响应时间, 大约10uS, 稍早于SW TX ON 10uS
      2)TPC 不能设置PA Enable
```

Reference document

MMRF Driver setting

CS0021-GAK1J-AND-V1.0EN_Platform_System_RF_MMRF_RF_Error_Check_Application_Note CS0021-GAK1K-AND-V1.0EN_Platform_System_RF_MMRF_RF_Custom_Setting_Application_Note

LTE Driver Setting

CS0021-GAK1A-AND-V1.2EN_Platform_System_RF_LTE_RF_Custom_Setting_Application_Note.docx CS0021-GAK1G-AND-V1.1EN_Platform_System_RF_LTE_RF_Error_Check_Application_Note CS0021-GAK1F-AND-V1.0EN_Platform_System_RF_LTE_RF_Default_Value_Settings LTE Custom Excel And File Generation Tool(MT6177) LTE custom Excel and file generation tool(MT6177m) MT6177-Update_NVRAM_By_GP_Tool

> WCDMA

 $CS0021\text{-}GAK1B\text{-}AND\text{-}V1.0EN_Platform_System_RF_WCDMA_RF_Custom_Settings_Application_Note \\ CS0021\text{-}GAK1H\text{-}AND\text{-}V1.0EN_Platform_System_RF_WCDMA_RF_Error_Check_Application_Note \\ How_to_use_NVRAM_editor_to_modify_3G_FDD_RF_settings$

TDSCDMA

[MT6177]3G_TDD_How_to_Configure_RF_Custom_File [MT6177]3G_TDD_MT6177_ASSERT_Description TDSCDMA_RF_MT6763_RF_NVRAM_LID_Introduction_Application_Note

C2K

 $CS0021\text{-}GAK1P\text{-}AND\text{-}V1.4EN_Platform_System_RF_CDMA_RF_Custom_Settings_Application_Note$



Reference document

> 2/3/4G MIPI

CS0021-GAK1D-AND-V1.1EN_Platform_System_RF_MIPI_Customization_Application_Note

▶ DRDI (单软多硬)

CS0021-GAK1O-AND-v1.0EN Platform System RF DRDI Customization Application Note

> ELNA

CS0021-GAK1L-AND-V1.0EN_Platform_System_RF_eLNA_Customization_Application_Note CS0021-GAK1AB-AND-V1.0EN_Platform_System_RF_ELNA_Module_Design Consideration

> TAS

CS0021-GAK1I-AND-V1.0EN_Platform_System_RF_TAS_ Customization_Setting_Application_Note

> RF Calibration

MTK RF Calibration Application Note
Platform_System_RF_Calibration_and_Test_Flow_Application_Note

Nvram LID edit

CS0021-GAK1C-AND-v1.3EN_Platform_System_RF_RF_NVRAM_LID_Introduction_Application_Note

GP tool

CS0021-GAK1N-AND-V1.0EN_Platform_System_RF_MMRF_GP_Tool_SOP_Application_Note

MEDIATEK

everyday genius

Copyright © MediaTek Inc. All rights reserved.