SPECIFICATION
FOR
LCM Module

MODULE No:	KD015QVFMN002
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2019.10.09	V1.0	ALL	FIRST ISSUE
2020.05.15	V1.1	ALL	Add module weight information
2022.09.21	V1.2	ALL	SECOND ISSUE

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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorpho us silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Pan el, driver circuit, back-light unit. The resolution of a 1.5'TFT-LCD contains 240X240 pixels, and can di splay up to 65K/262K colors

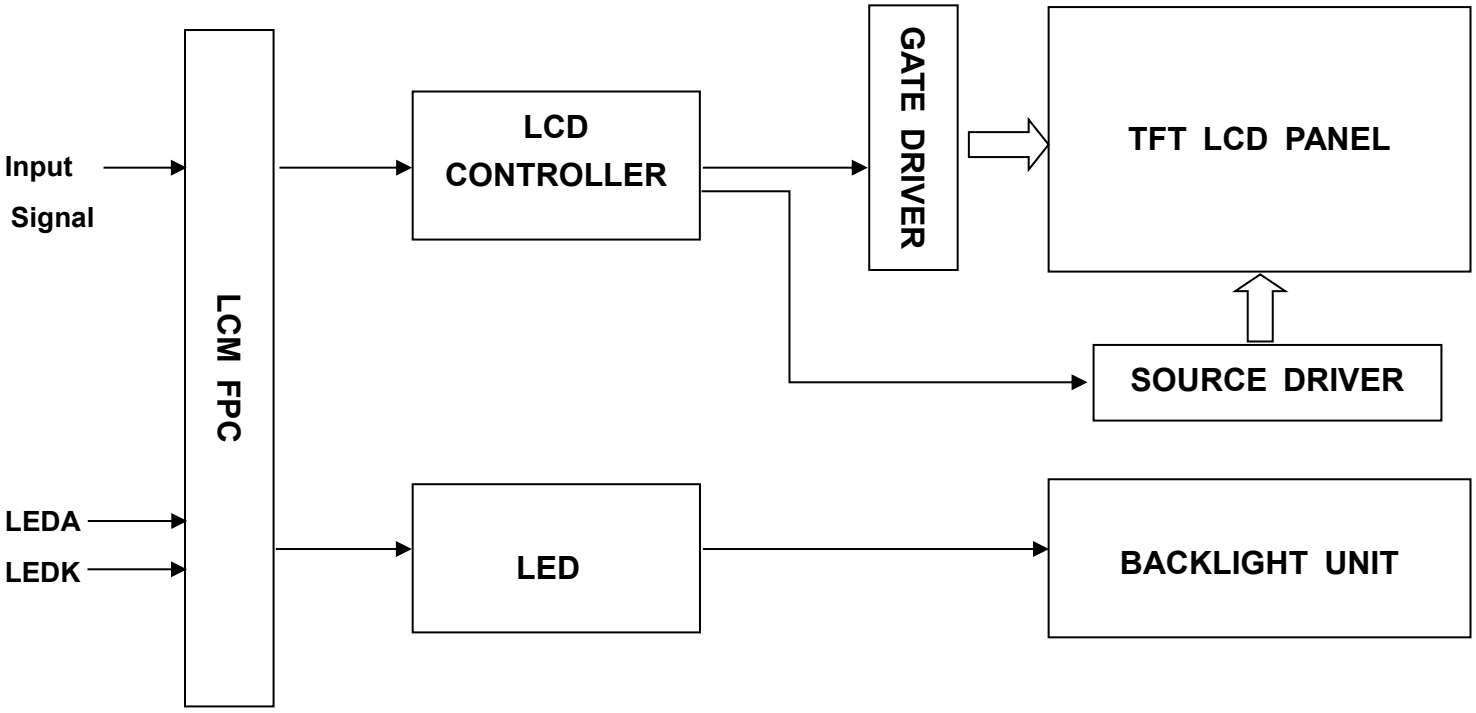
* Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	27.72(H) *27.72(V) (1.5inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	240(RGB)*240	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.1155 (H) x 0.1155 (V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ST7789V	-	-
LCM Interface	8/9/16/18Bit MCU 3/4SPI+16/18Bit RGB 3-line/4-line Serial Interface	-	
Display mode	Transmissive/Normally Black	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

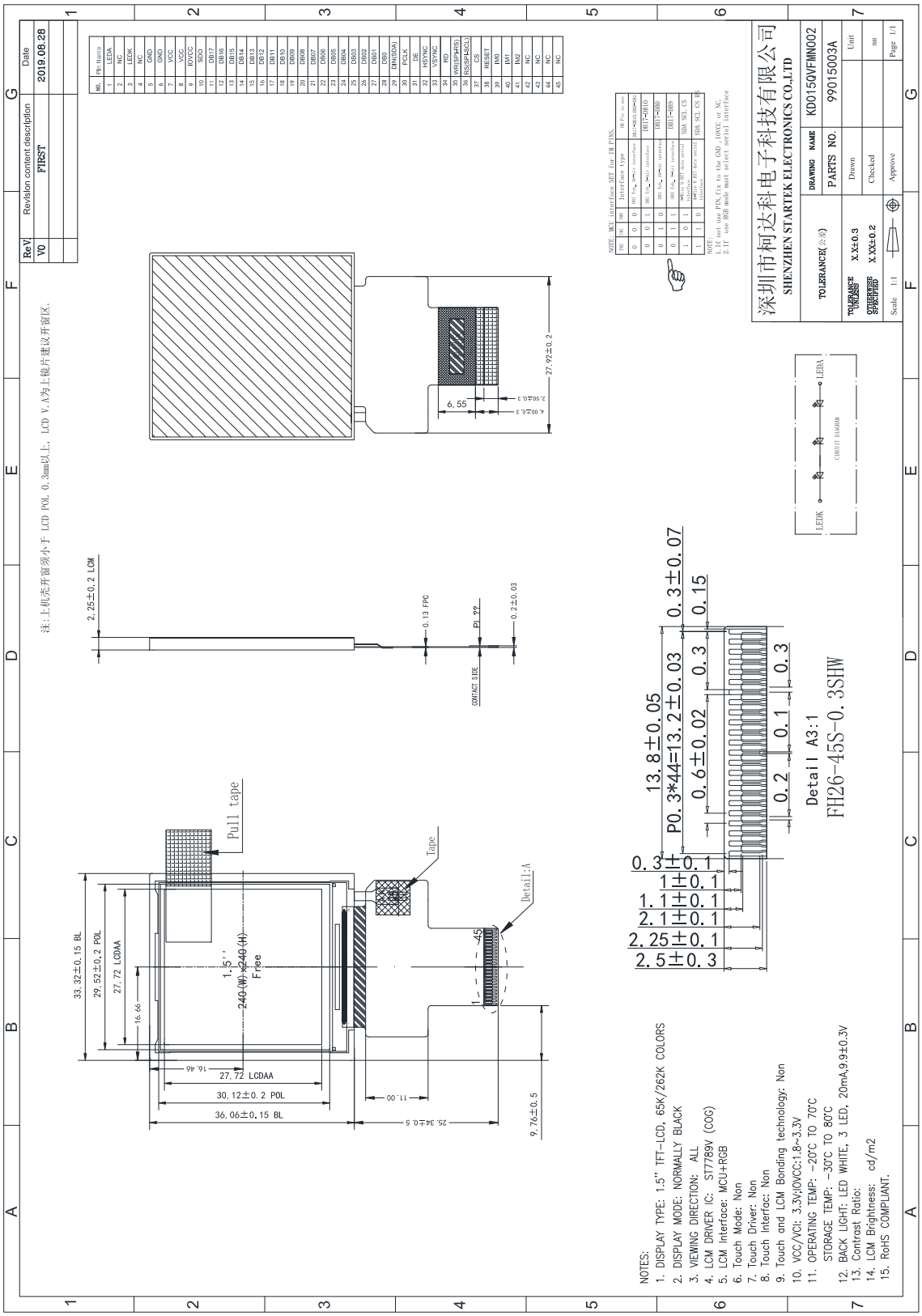
* Mechanical Informations

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		33.32		mm	-
	Vertical(V)		36.06		mm	-
	Depth(D)		2.25		mm	-
Weight			3		g	-

1. Block Diagram



2. Outline dimension



3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	LEDA	Anode pin of backlight	P
2	NC	--	--
3	LEDK	Cathode pin OF backlight	P
4	NC	--	--
5	GND	Ground.	P
6	GND		
7	VCC/VCI	Supply voltage(3.3V).	P
8	VCC/VCI		
9	IOVCC	Supply voltage(1.65-3.3V).	P
10	SDO	SPI interface output pin. The data is output on the falling edge of the SCL signal. If not used, let this pin open.	O
11-28	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode . Fix to GND level when not in use	I/O
29	DIN(SDA)	When IM3: Low, SPI interface input/output pin. When IM3: High, SPI interface input pin. The data is latched on the rising edge of the SCL signal. If not used, please fix this pin at IOVCC or GND level	I/O
30	PCLK	Dot clock signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.	I
31	DE	Data enable signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
32	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
33	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
34	RD	Serves as a read signal and MCU read data at the rising edge. fix this pin at IOVCC or GND when not in use.	I

35	WR(SPI-RS)	Write enable in MCU parallel interface. Display data/command selection pin in 4-line serial interface. Second Data lane in 2 data lane serial interface. If not used, please fix this pin at IOVCC or GND.	I
36	RS(SPI-SCL)	Display data/command selection pin in parallel interface. This pin is used to be serial interface clock. RS='1': display data or parameter. RS='0': command data. If not used, please fix this pin at IOVCC or GND.	I
37	CS	Chip select input pin ("Low" enable). fix this pin at IOVCC or GND when not in use.	I
38	RESET	This signal will reset the device and must be applied to properly initialize the chip.	I
39	IM0	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at IOVCC and GND.	I
40	IM1		
41	IM2		
42	NC	--	--
43	NC	--	--
44	NC	--	--
45	NC	--	--

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	600	800	--		(1)(2)
Response time	Rising+ Falling	$T_{R+}T_F$		--	30	40	msec	
Color gamut		S(%)		40	46	--	%	(1)
Color Filter Chromacicity	White	W_X		0.249	0.289	0.329		(1)
		W_Y		0.248	0.298	0.338		
	Red	R_X		0.543	0.583	0.623		
		R_Y		0.322	0.362	0.402		
	Green	G_X		0.272	0.312	0.352		
		G_Y		0.493	0.533	0.573		
	Blue	B_X		0.114	0.154	0.194		
		B_Y		0.053	0.093	0.133		
Viewing angle	Hor.	$Θ_L$	CR>10	60	80	--		(1)
		$Θ_R$		60	80	--		
	Ver.	$Θ_U$		60	80	--		
		$Θ_D$		60	80	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

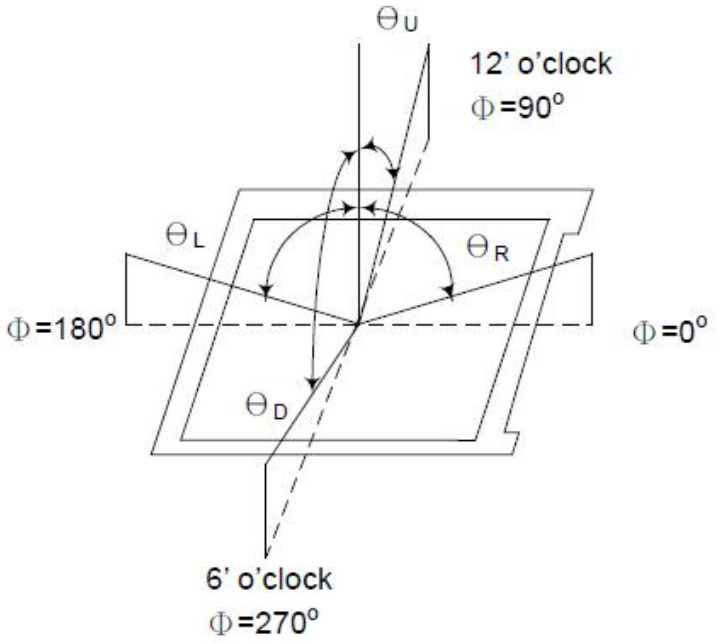
Ambient temperature : 25±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

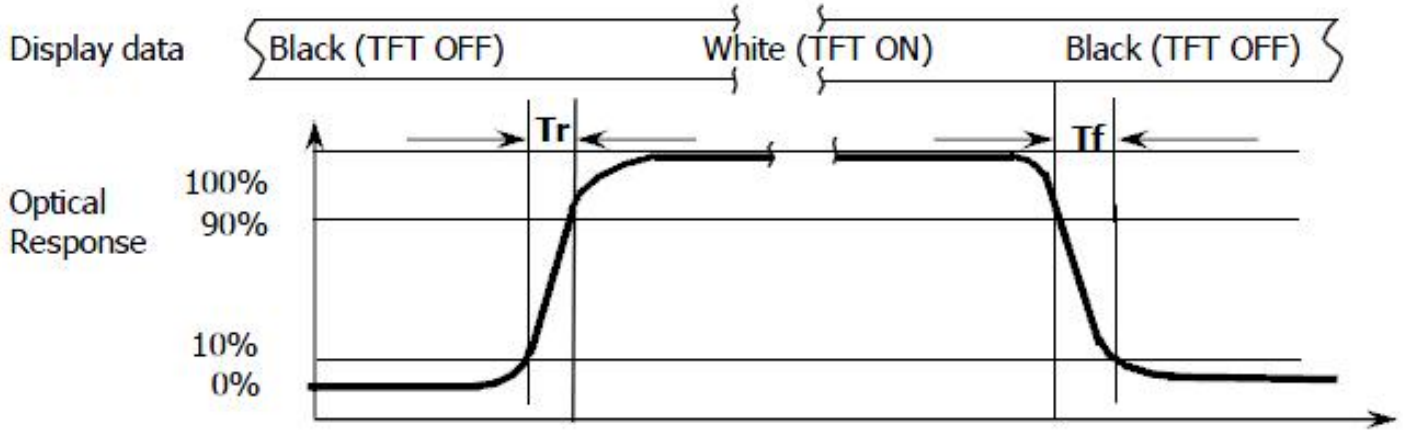
Note (1): Definition of Viewing Angle :



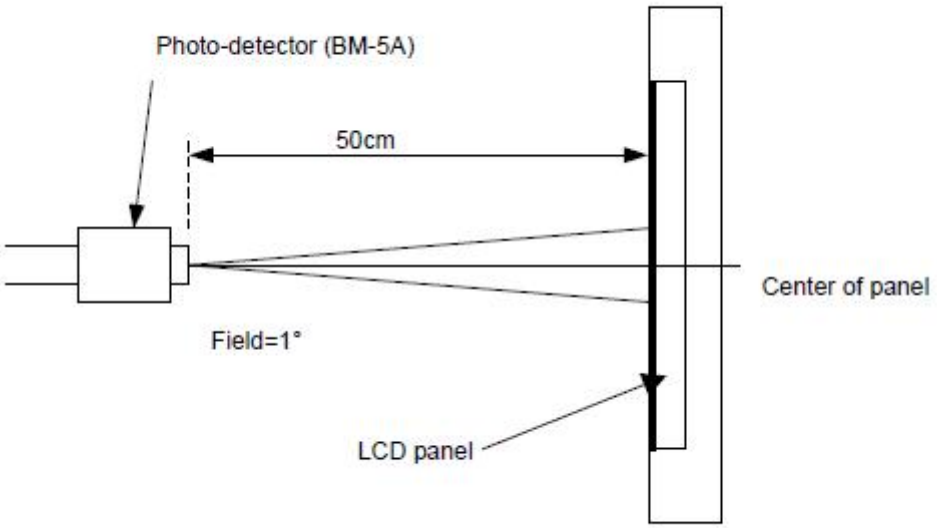
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCC	-0.3	4.6	**V**
Interface Operation Voltage	IOVCC	-0.3	4.6	**V**
Operating temperature	T_{OP}	-20	+70	℃
Storage temperature	T_{ST}	-30	+80	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCC	2.4	3.3	3.6	V	
Interface Operation Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current consumption	IDD	--	7	14	mA	
Level input voltage	V_{IH}	0.7 IOVCC		IOVCC	V	
	V_{IL}	GND		0.3 IOVCC	V	
Level output voltage	V_{OH}	0.8 IOVCC		IOVCC	V	
	V_{OL}	GND		0.2 IOVCC	V	

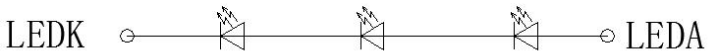
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 3 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	15	20	--	mA	
Forward Voltage	V_F	--	9.9	--	V	
LCM Luminance	L_V	450	500	--	cd/m2	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

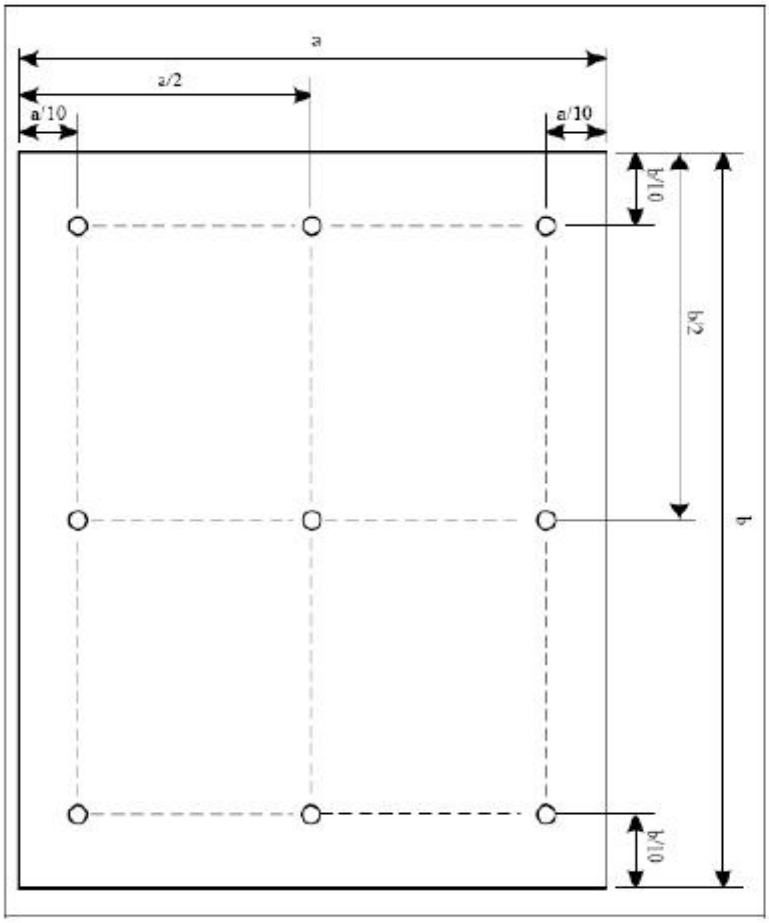
SNote (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.



CIRCUIT DIAGRAM

NOTE 3：Luminance Uniformity of these 9 points is defined as below:

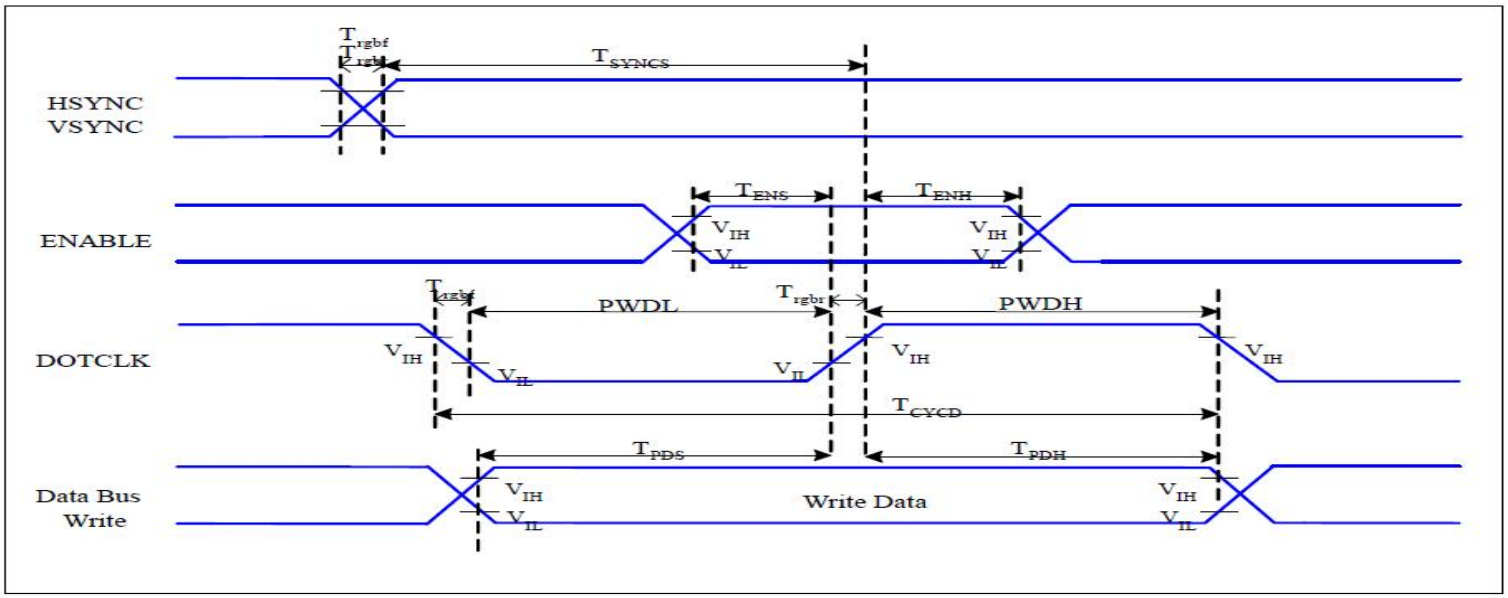


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. AC Characteristic

6.1 RGB Interface Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

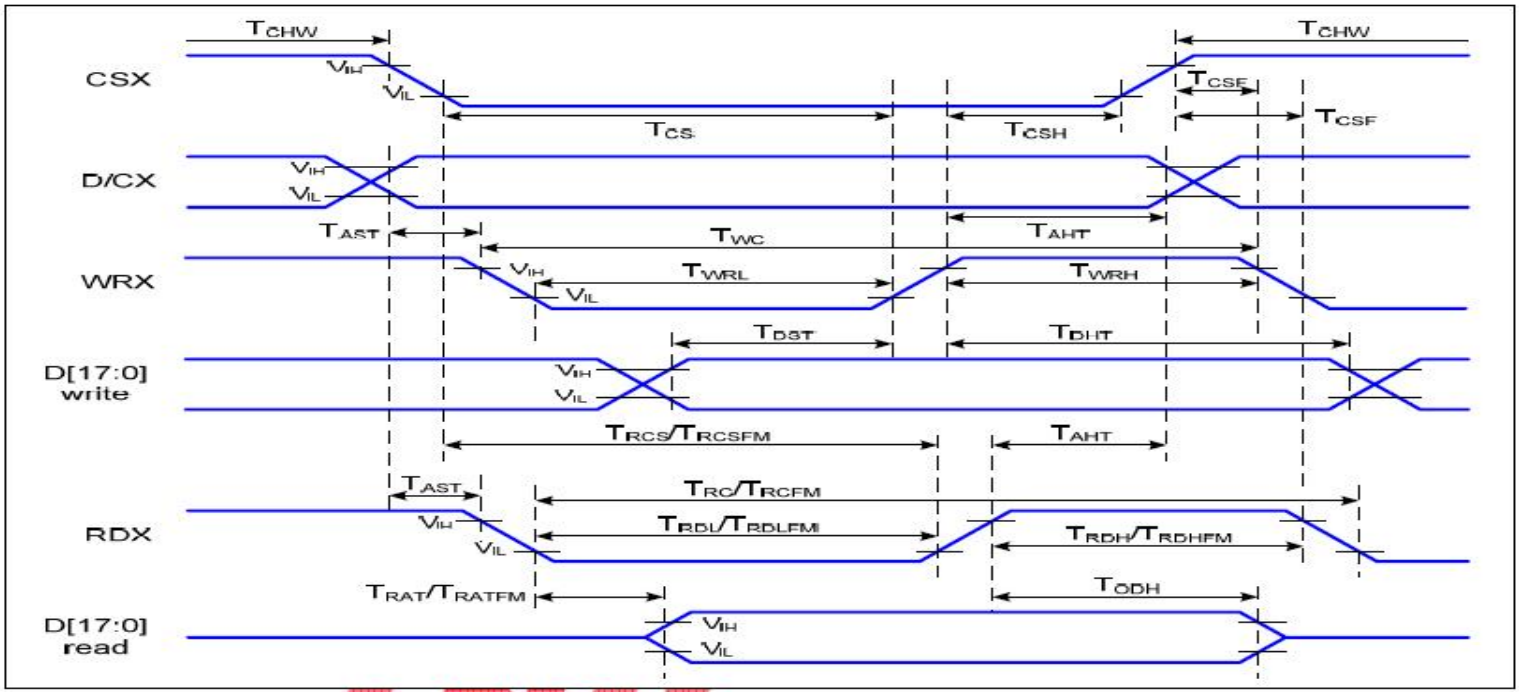
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	25	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	

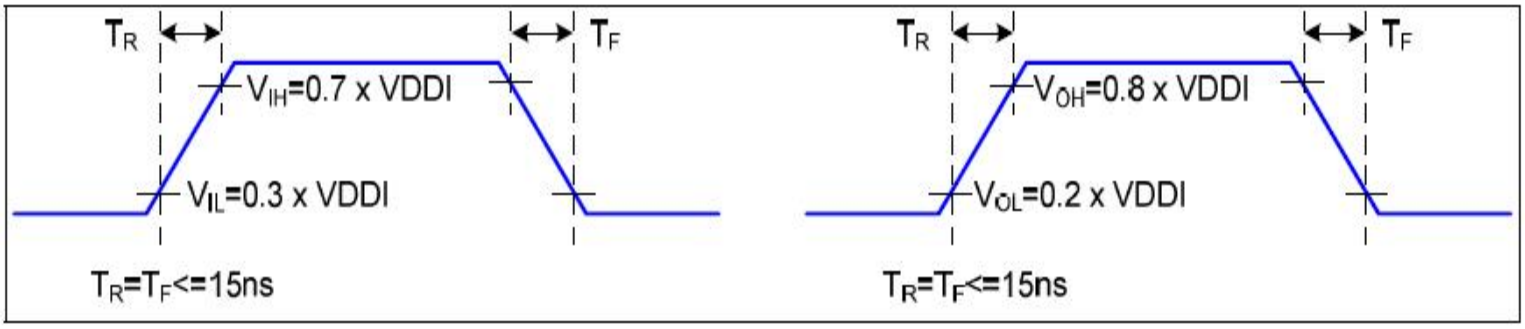
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	25	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	25	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	55	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	25	-	ns	
	T_{PDH}	PD Data Hold Time	25	-	ns	

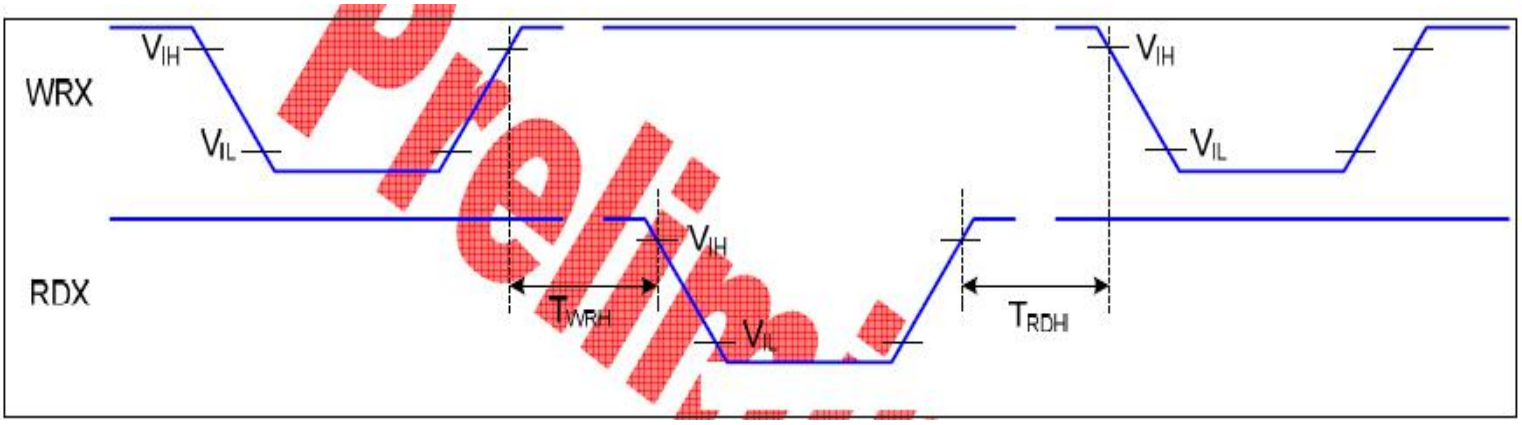
6.2 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF

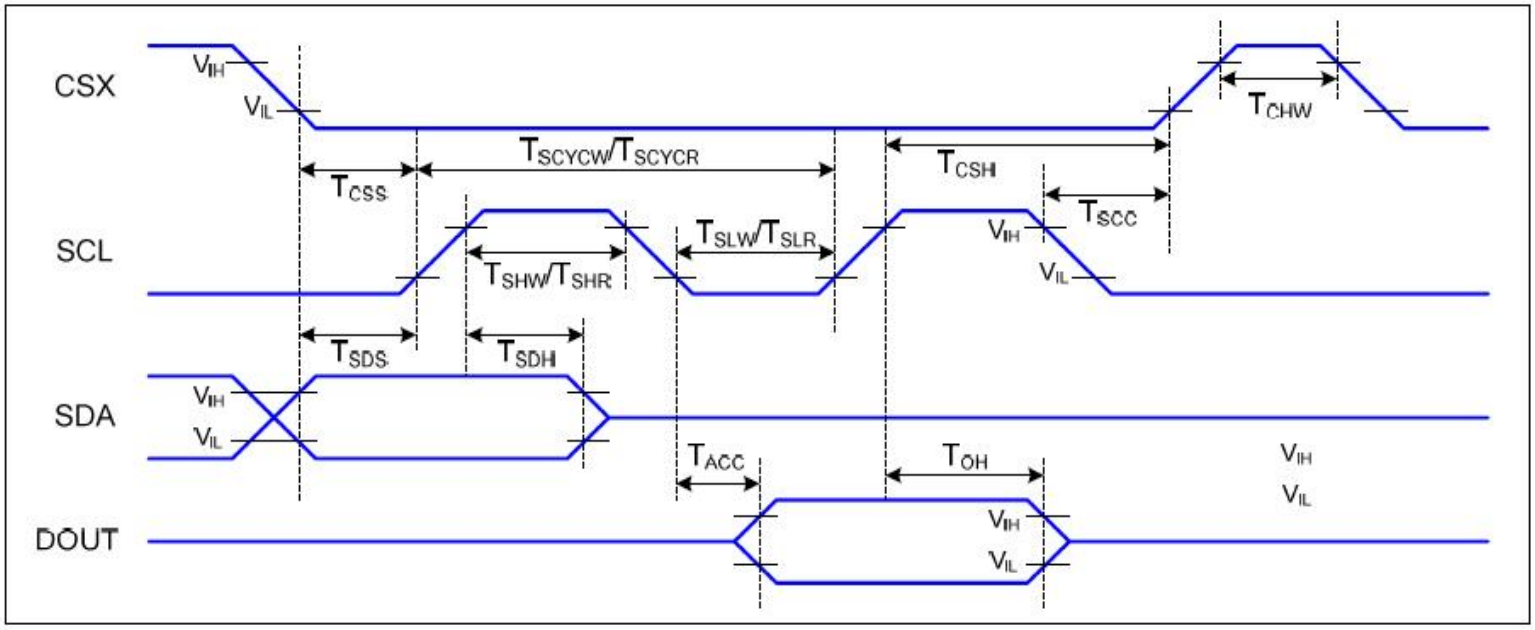
	T_{DHT}	Data hold time	10		ns
	T_{RAT}	Read access time (ID)		40	ns
	T_{RATFM}	Read access time (FM)		340	ns
	T_{ODH}	Output disable time	20	80	ns





Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.3 Serial Interface Characteristics (3-line serial)

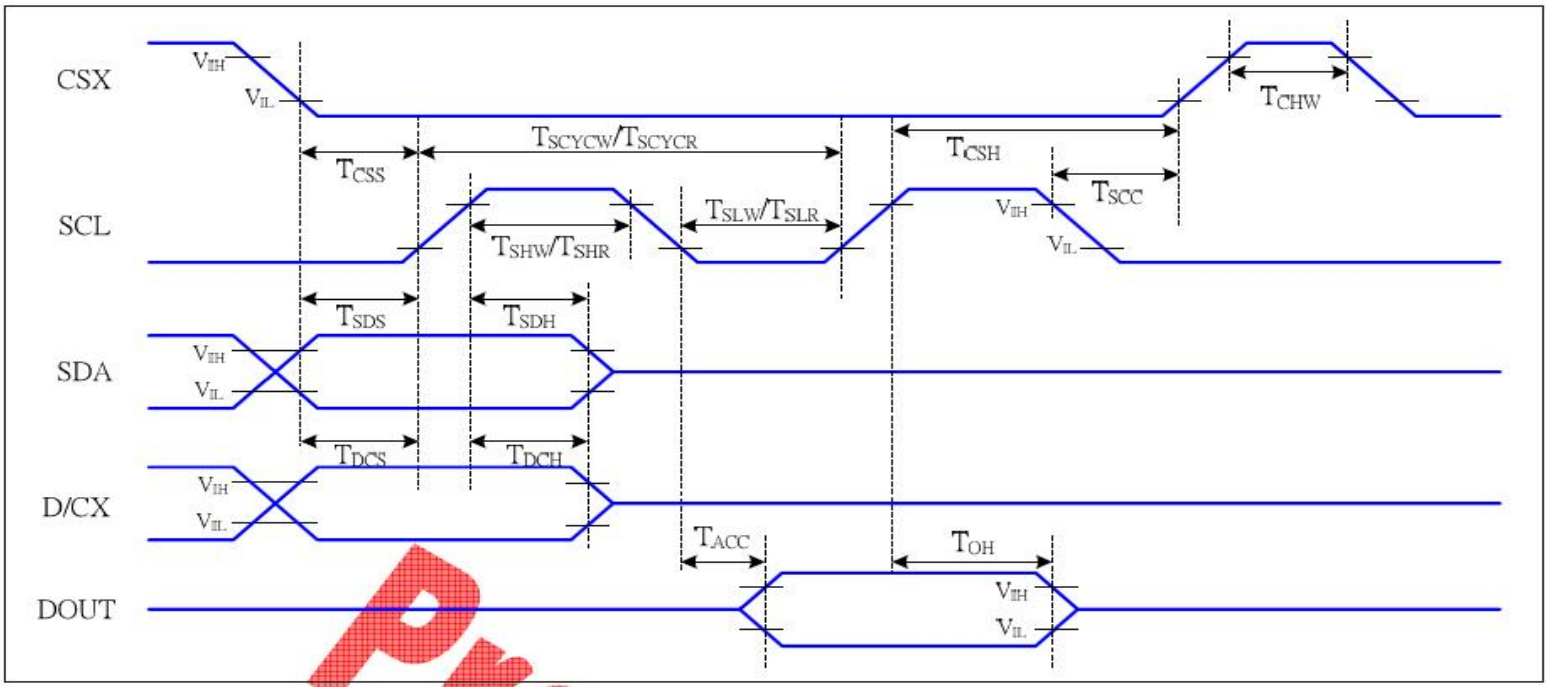


VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

6.4 Serial Interface Characteristics (4-line serial)



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.5 Reset Timing

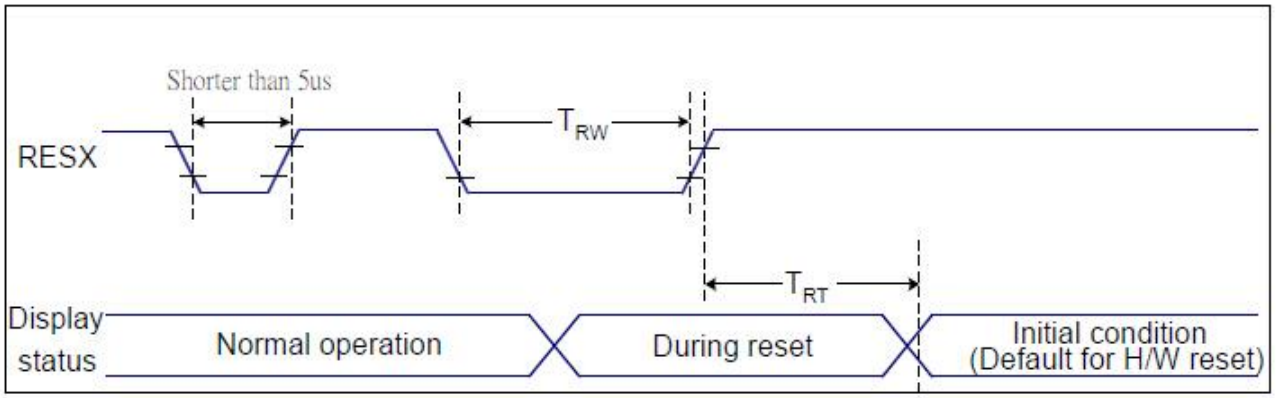


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

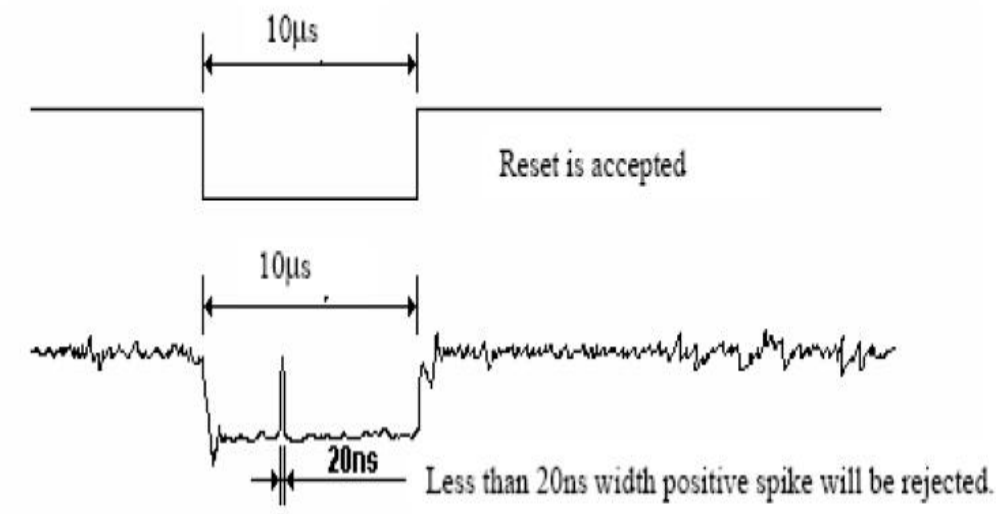
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

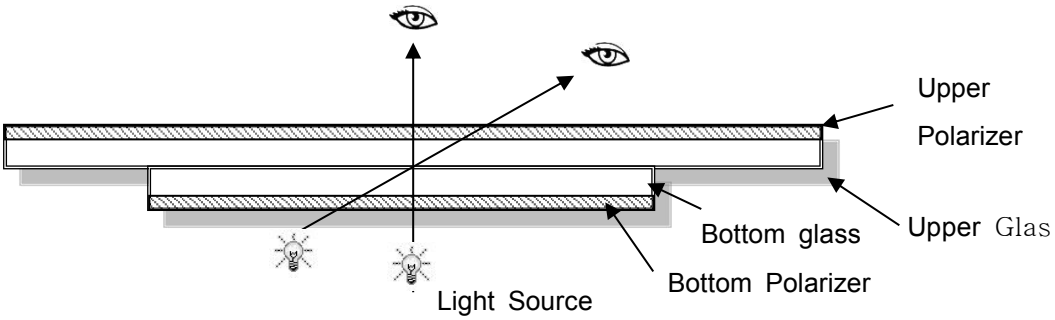
Temperature : 25±5℃

Humidity : 65%±10%RH

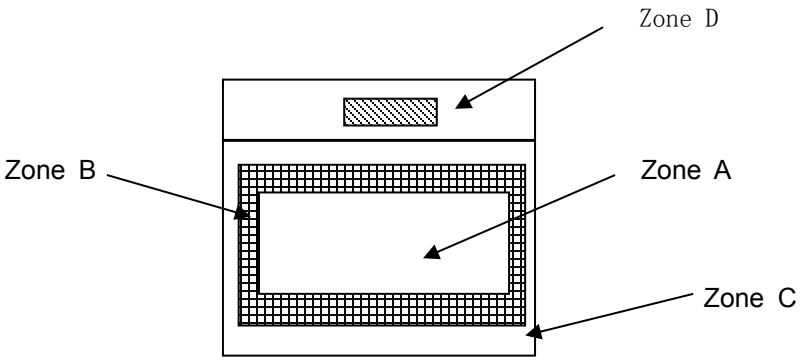
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

AQL:

Major defect	Minor defect
0.65	1.5

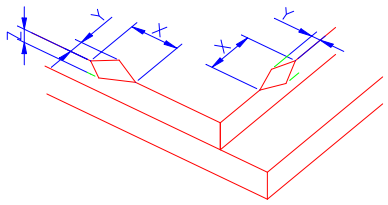
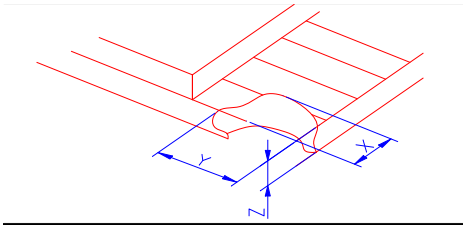
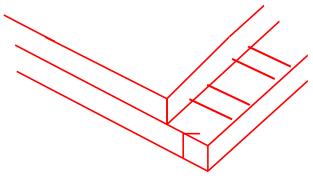
LCD: Liquid Crystal Display , LCM: Liquid Crystal Module,

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc…	Major
2	Missing	Missing components and etc…	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc…	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

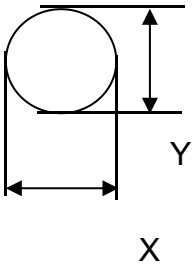
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

7.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



Φ=(X+Y)/2

① light dot（ black/white spot , pinhole, stain，etc.）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

② Dim spot（light leakage、dent、dark spot，etc）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧6mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	3(distance≧6mm)		
Φ>0.4	0		

3.0 LCD Pixel defect

Pixel bad points

Item	Zone A	Acceptable Qt
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

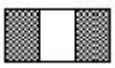
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

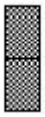
C) 2 dot adjacent = 1 pair = 2 dots

Picture:

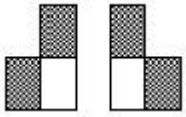
2 dot adjacent



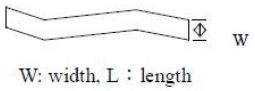
2 dot adjacent



2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)
 

N：Count</td>
<td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.04</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.04<W≤0.05</td><td>L≤2.0</td><td colspan="2">N≤1</td></tr>
<tr><td>W>0.05</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color& Brightness.</td>
<td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura/Waving/ Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10℃,30 min ↔ +60℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

6. The color fading mura of polarizing filter should not care.

9. Cautions and Handling Precautions

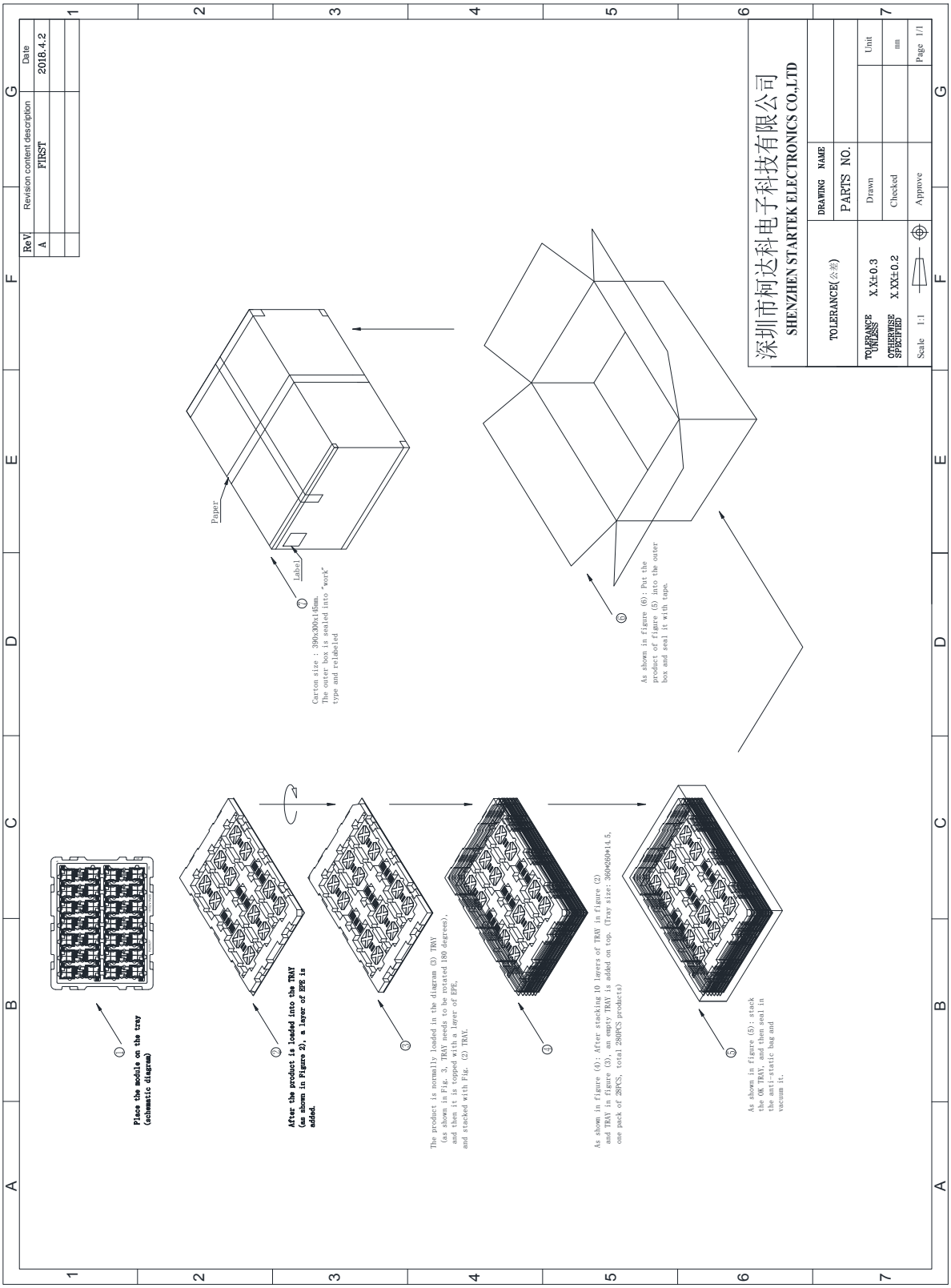
9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

10. Packing


深圳市柯达科电子科技有限公司
SHENZHEN STARTEK ELECTRONICS CO.,LTD
Rev
Revision content description
Date
A
FIRST
2018.4.2
TOLERANCE(公差)
DRAWING NAME
PARTS NO.
Drawn
Checked
Approve
Unit
mm
Scale 1:1
Page 1/1
Paper
Label
Carton size : 360x360x140mm.
The outer box is sealed into "work" type and relabeled
As shown in figure (6): Put the product of figure (5) into the outer box and seal it with tape.
Place the module on the tray (schematic diagram)
After the product is loaded into the TRAY (as shown in Figure 2), a layer of EPE is added.
The product is normally loaded in the diagram (3) TRAY (as shown in Fig. 3, TRAY needs to be rotated 180 degrees), and then it is topped with a layer of EPE, and stacked with Fig. (2) TRAY.
As shown in figure (4): After stacking 10 layers of TRAY in figure (2) and TRAY in figure (3), an empty TRAY is added on top. (Tray size: 360*260*14.5, one pack of 2SPCS, total 280PCS products)
As shown in figure (5): stack the OK TRAY, and then seal in the anti-static bag and vacuum it.